CS220 Quiz#2

General instructions: Please write brief explanation for your answers. If you submit multiple times, your last submission will be used for grading. Please provide an email address below where your responses can be sent.

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Q1. Consider a single-channel DIMM card with a 64-bit channel. The channel has four ranks. The DIMM card uses x4 chips and each chip has eight banks. If each bank has 16384 rows and 2048 columns,what is the total capacity of the DIMM card in bits? (1 point)

Channel Width=64 bits
At a time, all chips in a rank are activated.
Each chip spits out 4 bits, since they are x4 chips. Therefore we require 64/4= 16 chips in a rank.
There are 4 ranks, thus total number of chips = 16*4=64
Number of rows/bank = 16384= 2^14
Number of columns/bank = 2048 = 2^11
Number of bits/column= 2048*4 [Each column is made up of 4 bitlines] = 2^13
Total number of bits/bank = 2^14*2^13=2^27 bits/bank
Number of banks=8
Total number of bits in each chip=2^27*8= 2^30 bits
Number of chips=64
Total capacity of DRAM = 2^30*64= 2^36 bits= 64Gb = 8GB

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Q2. Suppose the following five access requests have come to a particular bank of a DRAM module, where each request is listed as (row number, column number): (17, 41), (11, 41), (15, 9), (17, 30), (15, 30). Write down the sequence in which the requests must be sent to the bank such that it takes the minimum amount of time to complete all the requests. Initially, the bank is in the precharged state. (1 point)

The requests having the same row numbers should be grouped together, to reduce the total amount of time. This is because, exploitation of spatial locality enables us to save some time in the precharging of the bitlines.

One optimal ordering may be:

(17,41), (17,30), (11,41),(15,9),(15,30)

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Q3. An SRAM module with 8M rows and eight-bit width is implemented using eight ranks of 1K x 1024-bit SRAM chips. To get eight-bit output, the chips in one of the ranks are selected. Calculate the number of address bits used to generate the row address, column address, and chip select. (1 point)

Total number of bits in the SRAM = 8*2^20*8 = Number of rows*columns = 2^26 bits
Each SRAM chip in 1 rank is 1k*1024.
Thus number of address bits reqd for row address= log(1k)=10 bits.
Each SRAM chip spits out data worth 1024 bits. This is sent to a multiplexor. Therefore we require log(1024)=10 bits as input to all the multiplexors.

Bits reqd to generate row address=10
Bits reqd to generate column address=10
Chip select= 3 bits(since there are 8 ranks)
Total: 23 bits, which is also equal to 8M bits.(number of rows in the SRAM)

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Q4. A finite state machine (FSM) having 600 states is implemented using a state sequencer, a microcode ROM, and 25 dispatch ROMs. The FSM also has 13 next states that do not come from the dispatch ROMs and nor is it equal to (current state + 1). The FSM takes a nine-bit input. Compute the minimum width (in bits) of the microinstructions and the total size (in bits) of each dispatch ROM. (1+1 points)

1+1

FSM takes a 9 bit input. Thus, each dispatch ROM must be having 2^9 rows.
Since there are 600 states, each dispatch ROM row's width is log(600). Thus we need 10 bits for each row of one dispatch ROM.
Total size of each dispatch ROM = 10*2^9 bits. Also, there are 25 such dispatch ROMs.

In the multiplexor, number of inputs are= 1(increment)+13(next states that come neither from the dispatch ROMs nor is equal to current state+1)+25(corresponding to the dispatch roms) = 39
Thus we need log(39) bits=6 bits for the microinstruction.

Note: wherever I write log(x), I actually mean the ceiling of log base 2 of x.

Q5. Write down the binary representation of the decimal fraction 20.6875 in normalized scientific notation. You can write x to the power of y as (x^y). (1 point)

20 in binary is 10100
0.6875*2=1.375
0.375*2=0.75
0.75*2=1.50
0.50*2=1.00
Thus 20.6875= 10100.1011 = 1.01001011*2^(4) in normalized form.
Actually, even the exponent is represented as binary internally, but here I have written it as 4.

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