CS220A Quiz#1

Please write brief explanation for your answers. Do not submit the quiz more than once. Please provide an email address below where your responses can be sent.

Email address *

sohamg@iitk.ac.in

Your name *

Soham Ghosal

6/6

Excellent!

Your roll number *

180771

Q1. Suppose you would like to design a PLA that can implement an arbitrary 11-input Boolean function where each input is a single-bit variable. The OR plane of the PLA has just one horizontal line because at a time it can implement only one function. (a) What is the number of input lines in the PLA (i.e., horizontal lines in the AND plane)? (b) What is the number of vertical lines in the AND plane? If this PLA is used to realize a function whose output is one irrespective of the input values, (c) how many intersections would have dots in the AND plane and (d) how many intersections would have dots in the OR plane? (0.5+0.5+0.5+0.5 points) Note: you need not worry about the exact mechanism through which the PLA would be programmed torealize a desired 11-input function. Also, do not worry about minimizing the Boolean function's SoP representation.

a) Horizontal Lines in AND plane= Number of inputs*2=22(One line for the input, and one for the complement)
b) Vertical Lines in AND plane=Number of distinct minterms= 2^11=2048(Since every output is 1, we will have 2048 corresponding distinct minterms)
c) Number of intersection which have dots in the AND plane=2^11*11=22528. Each minterm will have some contribution from the first input(either a or a_bar),some contribution from the second input(either b or b_bar)...upto the 11th input. Therefore each column would have 11 dots. Number of columns is 2^11.
d) Number of intersection in the OR plane=2^11=2048, since all the distinct minterms will be ORed.

2

Q2. Consider implementing the following four three-input functions using a ROM: (i) A + B + C, (ii) max(A, B, C), (iii) quotient of (A*B)/C, and (iv) remainder of (A*B)/C, where the inputs are A, B, C. If each input is 8-bit wide and is interpreted as a non-negative number, calculate the number of rows and number of columns in the ROM. Assume that when the divisor of a division operation is zero, both the quotient and remainder are stored as zero. (0.5+0.5 points)

Each input = 8bits
Total input size=8*3=24 bits
We need to store outputs for all possible inputs.
Thus the ROM needs 2^24=16777216 rows.

Number of bits in the output = 8(A+B+C)+8(max(A,B,C))+16((A*B)/C)+8(remainder)=40.

A+B+C will be 8 bits, max(A,B,C) will be 8 bits
A*B might take 16 bits at max, thus (A*B)/C might take 16 bits.
Remainder of (A*B)/C is definitely less than C. Therefore it will take 8 bits at max.

Thus, number of columns in ROM= Number of output bits = 40.

0.5+0.5

Q3. Suppose the inputs to a one-bit full adder are sent from three flip-flops A, B, C. The sum and carry outputs are sent to two flip-flops D and E, respectively. All five flip-flops receive the same clock signal. Assume zero clock skew. It takes 590 picoseconds to compute the sum bit and 810 picoseconds to compute thecarry output. The propagation delay through each of A, B, C is 140 picoseconds, while that through each of D and E is 200 picoseconds. The setup timeof each of A, B, C is 240 picoseconds, while the setup time of each of D and E is 290 picoseconds. The hold time of all flip-flops is 90 picoseconds. What is the minimum clock cycle time required for correct storage of sum and carry outputs? (1 point)

Clock time period>= T(skew)+T(propagation delay)+T(f)+T(setup)
T(skew)=0.
T(f) = 590ps(for sum) and 810ps(carry). We will consider the max of these, since we want a lower bound. Thus T(f)=810 ps.
T(propagation delay){For the input flipflops} = 140 ps
T(setup) = Setup time for the output flipflops = 290 ps
Thus minimum clock cycle time = 810+140+290=1240 ps
The hold time doesnot play a role in this, since propagation delay>hold time.

1

Q4. A register file having 64 registers each of width 16 bits has 5 read ports and 4 write ports. Each port uses its own decoder and no decoder is shared across ports. What is the number of input bits and output bits to each decoder? (0.5+0.5 points) What is the total number of wordlines and bitlines in the register file? (0.5+0.5 points)

Number of registers=64
Number of decoders=Number of ports=5+4=9
Number of input bits to each decoder=log(64)=6
Number of output bits from each decoder=2^6=64
Number of wordlines=Number of ports*Number of output bits from each decoder=9*64=576
Number of bitlines=Number of ports*Width of each register=9*16=144

2