CS220A Quiz#1

Please write brief explanation for your answers. Do not submit the quiz more than once. Please provide an email address below where your responses can be sent.

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Q1. Suppose you would like to design a PLA that can implement an arbitrary 11-input Boolean function where each input is a single-bit variable. The OR plane of the PLA has just one horizontal line because at a time it can implement only one function. (a) What is the number of input lines in the PLA (i.e., horizontal lines in the AND plane)? (b) What is the number of vertical lines in the AND plane? If this PLA is used to realize a function whose output is one irrespective of the input values, (c) how many intersections would have dots in the AND plane and (d) how many intersections would have dots in the OR plane? (0.5+0.5+0.5+0.5 points) Note: you need not worry about the exact mechanism through which the PLA would be programmed torealize a desired 11-input function. Also, do not worry about minimizing the Boolean function's SoP representation.

(a) Number of horizontal lines is 22 (each input bit and its inversion).
(b) Number of vertical lines is equal to the number of minterms. Using 11 Boolean variables, one can construct 2048 different minterms. So, the number of vertical lines is 2048.
(c) One way to implement 1 is to have all minterms. So, for each vertical line, 11 intersections would have dots. So, the total number of dots in AND plane is 22528.
(d) We will OR all minterms. So, there will be 2048 dots in the OR plane.

Q2. Consider implementing the following four three-input functions using a ROM: (i) A + B + C, (ii) max(A, B, C), (iii) quotient of (A*B)/C, and (iv) remainder of (A*B)/C, where the inputs are A, B, C. If each input is 8-bit wide and is interpreted as a non-negative number, calculate the number of rows and number of columns in the ROM. Assume that when the divisor of a division operation is zero, both the quotient and remainder are stored as zero. (0.5+0.5 points)

(a) Total number of inputs is 24. So, the number of rows is 2^{24} i.e., 16777216.
(b) To compute the number of columns, we need to find out the maximum number of bits needed to store each of the functions. Since each input can range from 0 to 255, A+B+C would need 10 bits; max(A, B, C) would need 8 bits; quotient of (A*B)/C is maximized when A=B=255 and C=1 needing 16 bits; remainder of (A*B)/C would need 8 bits. So, the total number of columns is 42.

Q3. Suppose the inputs to a one-bit full adder are sent from three flip-flops A, B, C. The sum and carry outputs are sent to two flip-flops D and E, respectively. All five flip-flops receive the same clock signal. Assume zero clock skew. It takes 590 picoseconds to compute the sum bit and 810 picoseconds to compute thecarry output. The propagation delay through each of A, B, C is 140 picoseconds, while that through each of D and E is 200 picoseconds. The setup timeof each of A, B, C is 240 picoseconds, while the setup time of each of D and E is 290 picoseconds. The hold time of all flip-flops is 90 picoseconds. What is the minimum clock cycle time required for correct storage of sum and carry outputs? (1 point)

Minimum clock cycle time = propagation delay through input flip-flops + max. delay through combinational logic + setup time of output flip-flops = max(140, 140, 140) + max(590, 810) + max(290, 290) picoseconds = 1240 picoseconds.

Q4. A register file having 64 registers each of width 16 bits has 5 read ports and 4 write ports. Each port uses its own decoder and no decoder is shared across ports. What is the number of input bits and output bits to each decoder? (0.5+0.5 points) What is the total number of wordlines and bitlines in the register file? (0.5+0.5 points)

The decoder decodes a register number. So, the number of input bits to the decoder is 6 and the number of output bits is 64. Number of wordlines = number of registers*number of ports = 576. Number of bitlines = width of registers*number of ports = 144.