CS220 Quiz#6

General instructions: Please write brief explanation for your answers. If you submit multiple times, your last submission will be used for grading. Please provide an email address below where your responses can be sent.

Email address *

mainakc@cse.iitk.ac.in

Your name *

Mainak Chaudhuri

Your roll number *

0

Q1. Consider a pipelined processor with ten stages S1, S2, ..., S10 with individual stage latencies 1 ns, 2 ns, ..., 10 ns. Suppose the branch instructions complete execution in stage S8. The processor has a branch predictor integrated in the S1 stage. On a correct prediction, there is no loss in performance. A program running on this processor has 25% branch instructions. This program suffers from only control hazard and no other hazards. Assume that there is no branch delay slot. This program experiences a branch prediction accuracy of 75%. If the program executes a total of 100 instructions, compute its execution time in nanoseconds (ns). [2 points]

Cycle time of the pipeline = latency of the longest stage = 10 ns
Let us first assume that there is no hazard. So, the pipeline starts completing one instruction in every cycle after the first nine cycles. So, execution time without any hazard = 109*10 ns = 1090 ns. Now due to control hazard only the mispredicted branch instructions are affected. Each misprediction leads to loss of seven cycles. So, additional time lost in dealing with control hazard = 25*0.25*7*10 ns = 437.5 ns. So, the total execution time = 1527.5 ns.

Q2. The designers of the processor in Q1 are trying to increase the clock frequency of the processor by subdividing any one of the ten stages into two substages. What is the best achievable frequency for this processor by this method? Express your answer in MHz. [1 point]

The longest stage needs to be subdivided. So, now we have an eleven-stage pipeline with stage latencies 1 ns, 2 ns, 3 ns, 4 ns, 5 ns, 6 ns, 7 ns, 8 ns, 9 ns, 5 ns, 5 ns. So, the best frequency achievable is 1000/9 MHz or 111.11 MHz.

Q3. Consider a cache of 512 KB capacity and 32-byte block size. At what associativity would the tag length get maximized? What is the maximum tag length if the address is 36-bit long? Assume that a simple hash function that computes (A % number of sets) is used to extract the set index, where A is the block address. [1+1 points]

The cache has 16384 blocks. The tag length is maximized when the cache is fully-associative. In this case, that corresponds to an associativity of 16384. The maximum tag length = length of address - length of block offset = 36 - 5 bits = 31 bits.

Q4. Consider a cache with 512 sets and 32-byte block size. The address length is 32 bits. Let the address be A[31:0]. The set index is computed using the function A[31:23] XOR A[22:14] XOR A[13:5]. What should be the tag length? [1 point]

Since none of the original bits of the address can be recovered from the set index of a block, the tag needs to store all the address bits except the block offset. This is needed to make sure that all blocks in a set can be distinguished unambiguously. So, the tag length should be 27 bits.