CS220 Quiz#6

General instructions: Please write brief explanation for your answers. If you submit multiple times, your last submission will be used for grading. Please provide an email address below where your responses can be sent.

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Excellent!

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Q1. Consider a pipelined processor with ten stages S1, S2, ..., S10 with individual stage latencies 1 ns, 2 ns, ..., 10 ns. Suppose the branch instructions complete execution in stage S8. The processor has a branch predictor integrated in the S1 stage. On a correct prediction, there is no loss in performance. A program running on this processor has 25% branch instructions. This program suffers from only control hazard and no other hazards. Assume that there is no branch delay slot. This program experiences a branch prediction accuracy of 75%. If the program executes a total of 100 instructions, compute its execution time in nanoseconds (ns). [2 points]

Individual instruction latency is 10 cycles, but ideally can finish one instruction every cycle after the pipeline is full.

Clock cycle=max(all stage latencies) = 10ns

Total instructions=100
Branch instructions=25
Non branch instructions=75
Branch instructions correctly predicted=18.75
Wrongly predicted=6.25

Ideal CPI when the pipeline is full=1
For branch instructions, penalty when predicted wrongly=7 cycles(cycle 2 to cycle 8)
CPI for this processor = 1+0.25*(1-0.75)*7=1.4375

2

Therefore the total time required for execution = 100(no.of instructions)*1.4375*(10)ns=1437.5ns

Thus the execution time is 1437.5 ns

Q2. The designers of the processor in Q1 are trying to increase the clock frequency of the processor by subdividing any one of the ten stages into two substages. What is the best achievable frequency for this processor by this method? Express your answer in MHz. [1 point]

The longest stage, ie. Stage 10 should be subdivided, into two substages.
Thus 10ns is divided into two stages taking 5 ns each.
Now the longest stage latency is of 9 ns.
Then clock cycle can be taken to be 9 ns.

1

Best achievable frequency = 1000/9=111.11MHz

Q3. Consider a cache of 512 KB capacity and 32-byte block size. At what associativity would the tag length get maximized? What is the maximum tag length if the address is 36-bit long? Assume that a simple hash function that computes (A % number of sets) is used to extract the set index, where A is the block address. [1+1 points]

Total capacity=2^19 bytes
2^5 bytes block size
Tag length will be maximized when this is fully associative(associativity=number of blocks)
Address is 36 bit long.

2

Number of blocks=2^19/2^5=2^14 blocks= Required Associativity

Maximum tag length=36-5-0(since fully associative, only 1 set)=31 bits.

Q4. Consider a cache with 512 sets and 32-byte block size. The address length is 32 bits. Let the address be A[31:0]. The set index is computed using the function A[31:23] XOR A[22:14] XOR A[13:5]. What should be the tag length? [1 point]

2^9 sets
2^5 bytes block size
Address=32 bits

Number of bits in set index=9 bits(XOR of 3 9bit numbers could be 9 bits at max)
Block offset is of 5 bits(log 32)

1

Tag length = 32-5-9=18 bits