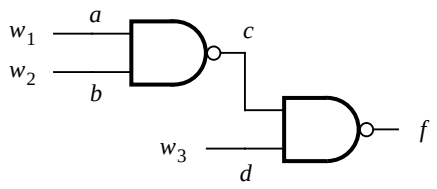
Chapter 11

11.1. Label the wires in the circuit of Figure P11.1 as follows:

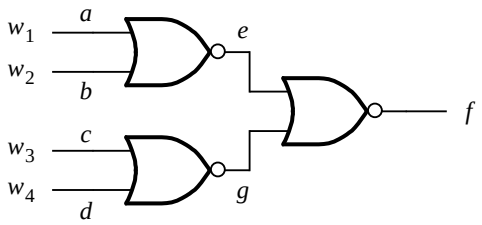


A complete fault table is

Test $w_1w_2w_3$	Fault detected									
	$a/0$	$a/1$	$b/0$	$b/1$	$c/0$	$c/1$	$d/0$	$d/1$	$f/0$	$f/1$
000								√	√	
001					√		√			√
010								√	√	
011		√			√		√			√
100								√	√	
101				√	√		√			√
110									√	
111	√		√			√			√	

A minimal test set must include the tests $w_1w_2w_3 = 011, 101$, and 111, which cover all faults except $d/1$. The latter fault can be detected by choosing one of $000, 010,$ or 100.

11.2. Label the wires in the circuit of Figure P11.2 as follows:



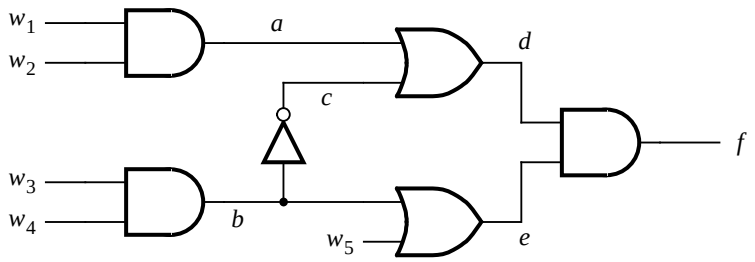
A complete fault table is

Test $w_1w_2w_3w_4$	Fault detected													
	$a/0$	$a/1$	$b/0$	$b/1$	$c/0$	$c/1$	$d/0$	$d/1$	$e/0$	$e/1$	$g/0$	$g/1$	$f/0$	$f/1$
0000														√
0001		√		√					√					√
0010		√		√					√					√
0011		√		√					√					√
0100						√		√			√			√
0101			√				√			√		√	√	
0110			√		√					√		√	√	
0111			√							√			√	
1000						√		√			√			√
1001	√						√			√		√	√	
1010	√				√					√		√	√	
1011	√									√			√	
1100						√		√			√			√
1101							√					√	√	
1110					√							√	√	
1111										√		√	√	

A possible minimal test set consists of $w_1w_2w_3w_4$ = $0001, 0110, 1000,$ and 1001.

11.3. The two functions differ only in the vertex $x_1x_2x_3x_4 = 0111$. Therefore, the circuits can be distinguished by applying this input valuation.

11.4. Label the wires in the circuit of Figure P11.3 as follows:



Path $w_1 - a - d - f$ is sensitized with $w_2w_3w_4w_5$ = 111x
Path $w_2 - a - d - f$ is sensitized with $w_1w_3w_4w_5$ = 111x
Path $w_3 - b - c - d - f$ is sensitized with $w_1w_2w_4w_5$ = 0x11
Path $w_3 - b - e - f$ is sensitized with $w_1w_2w_4w_5$ = 1110
Path $w_4 - b - c - d - f$ is sensitized with $w_1w_2w_3w_5$ = 0x11
Path $w_4 - b - e - f$ is sensitized with $w_1w_2w_3w_5$ = 1110
Path $w_5 - e - f$ is sensitized with $w_1w_2w_3w_4$ = xx0x

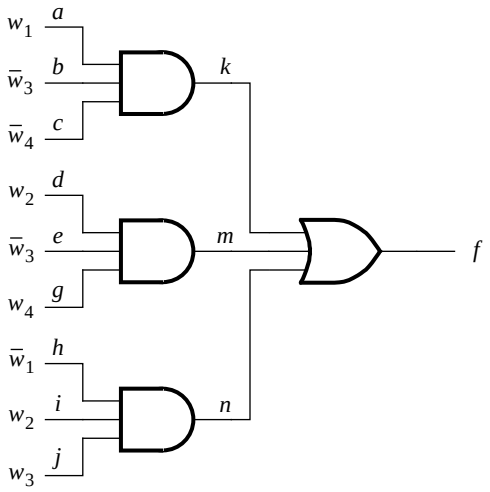
As an input signal to each path it is necessary to apply both 0 and 1 to give two tests. A possible test set is $w_1w_2w_3w_4w_5$ = 01111, 11110, 1011x, 0x011, 11010, 0x101, and 11100

11.5. The tests are $w_1w_2w_3w_4$ = 1111, 1110, 0111, and 1111.

11.6. Test 0100 detects $w_1/1,\ c/1,\ d/1,\ w_4/1$, and $f/1$.
Test 1010 detects $b/0,\ d/0,\ w_3/0$, and $f/0$.
Test 0011 detects $f/0$.
Test 1111 detects $f/0$.
Test 0110 detects $w_1/1,\ w_2/0,\ b/1,\ c/1,\ d/1,\ w_4/1$, and $f/1$.
Thus 11 different single faults can be detected using these four tests. Since the circuit has 8 wires, there can be 16 single $s/0$ or $s/1$ faults. Therefore, the tests cover 69% of single faults.

11.7. Test 0100 detects $w_1/1,\ b/0,\ c/0,\ g/1,\ h/0,\ k/0$, and $f/1$.
est 1010 detects $w_2/1,\ w_4/1,\ b/0,\ c/0,\ g/1,\ h/0,\ k/0$, and $f/1$.
Test 0011 detects $w_3/0,\ w_4/0,\ b/0,\ c/1,\ g/0,\ h/1$, and $f/0$.
Test 0110 detects $w_1/1,\ w_4/1,\ b/0,\ c/0,\ g/1,\ h/0,\ k/0$, and $f/1$.
Thus 15 different single faults can be detected using these four tests. Since the circuit has 10 wires, there can be 20 single $s/0$ or $s/1$ faults. Therefore, the tests cover 75% of single faults.

11.8. Label the wires in the circuit of Figure 11.5 as follows:



Test 0100 detects $a/1,\ g/1,\ j/1,\ k/1,\ m/1,\ n/1$, and $f/1$.
Test 1010 detects $b/1,\ k/1,\ m/1,\ n/1$,, and $f/1$.
Test 0011 detects $i/1,\ k/1,\ m/1,\ n/1$, and $f/1$.
Test 0110 detects $h/0,\ i/0,\ j/0,\ n/0$, and $f/0$.

Thus 14 different single faults can be detected using these four tests. Since the circuit has 13 wires, there can be 26 single $s/0$ or $s/1$ faults. Therefore, the tests cover 54% of single faults.

11.9. Cannot detect if the input wire w_1 is stuck-at-1. The reason is that this circuit is highly redundant. It realizes the function $f = w_3(\overline{w}_1 + \overline{w}_2)$, which can be implemented with a simpler circuit.

11.10. In a circuit in which all gates have a fan-out of 1 there exists a single path from any primary input to the output of the circuit. A test for a fault on a primary input sensitizes the path that leads from this input to the output of the circuit, thus testing for faults along this path. Therefore, a test set that tests all faults on the primary inputs, will also test all faults on the sensitized paths.

11.11. Test set $= \{0000, 0111, 1111, 1000\}$. It would work with XORs implemented as shown in Figure 4.28c.

For n bits, the same patterns can be used; thus
Test set $= \{00\cdots00, 011\cdots1, 11\cdots1, 100\cdots0\}$.

11.12. In the decoder circuit in Figure 6.16c the four AND gates are enabled only if the En signal is active. The required test set has to include all four valuations of w_1 and w_2 when $En = 1$. It is also necessary to test if the En wire is stuck at 1, which can be accomplished with the test $w_1w_2En = 000$. Therefore, a complete test set comprises w_1w_2En = 000, 001, 011, 101, and 111.

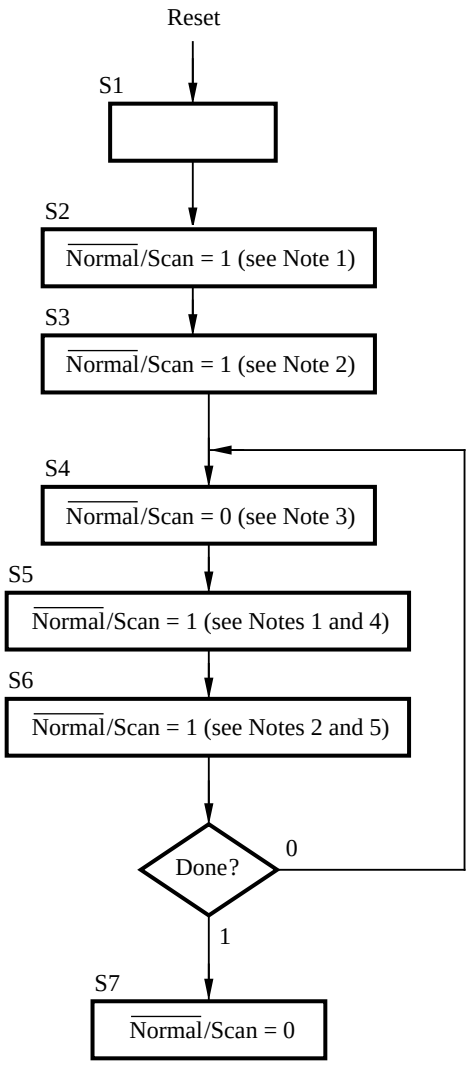
11.13. Test 1100 detects $w_1/0,\ w_2/0,\ b/1,\ c/0,\ g/0,\ k/1$, and $f/0$.
Test 0010 detects $w_4/1,\ b/0,\ c/0,\ g/1,\ h/0,\ k/0$, and $f/1$.
Test 0110 detects $w_1/1,\ w_4/1,\ b/0,\ c/0,\ g/1,\ h/0,\ k/0$, and $f/1$.

11.14. Label the output wires of the top three AND gates in Figure 11.12 as a, b, and c, respectively. Then the paths in the combinational part of the circuit are sensitized as follows.

Path $\overline{y}_1 - a - Y_1$ is sensitized with $w = 1$ and $y_2 = 0$.
Path $w - a - Y_1$ is sensitized with $y_1 = 0$ and $y_2 = 0$.
Path $w - b - Y_1$ is sensitized with $y_1 = 1$ and $y_2 = 1$.
Path $w - b - Y_2$ is sensitized with $y_1 = 0$ and $y_2 = 1$.
Path $y_2 - b - Y_1$ is sensitized with $w = 1$ and $y_1 = 1$.
Path $y_2 - b - Y_2$ is sensitized with $w = 1$ and $y_1 = 0$.
Path $w - c - Y_2$ is sensitized with $y_1 = 1$ and $y_2 = 0$.
Path $y_1 - c - Y_2$ is sensitized with $w = 1$ and $y_2 = 0$.
Path $y_1 = z$ is sensitized with $y_2 = 1$.
Path $y_2 = z$ is sensitized with $y_1 = 1$.

All 8 valuations of signals w, y_1 and y_2 have to be applied to sensitize these paths. It takes 26 clock cycles to perform the tests.

11.15. For simplicity, in the ASM chart it is assumed that testing begins one clock cycle after *Resetn* is de-asserted. States S2 to S6 depict the actions listed on page 666. We assume that external circuitry places the test data values on the *Scan-in* and *w* ports, and checks the generated results at *Scan-out* and *z*.



Notes

Note 1: Scan-in has test value for y_2

Note 2: Scan-in has test value for y_1

Note 3: *w* has test value

Note 4: Scan-out has test result for y_2

Note 5: Scan-out has test result for y_1

11.16. Assume that the circuit has been reset by applying *Resetn* = 0. Then, let *Resetn* = 1 and observe the behavior indicated in the following table.

Clock cycle	$\overline{\text{Normal}}$/ Scan	Scan-in	Scan-out	w	z	Transition tested
1	1	0	0	x	x	Reset
2	1	0	0	x	x	
3	0	x	x	0	0	A → A
4	1	0	0	x	x	
5	1	1	0	x	x	
6	0	x	x	0	0	B → A
7	1	0	0	x	x	
8	1	0	0	x	x	
9	0	x	x	1	0	A → B
10	1	0	0	x	x	
11	1	1	1	x	x	
12	0	x	x	1	0	B → C
13	1	1	1	x	x	
14	1	0	0	x	x	
15	0	x	x	0	0	C → A
16	1	1	0	x	x	
17	1	0	0	x	x	
18	0	x	x	1	0	C → D
19	1	1	1	x	x	
20	1	1	1	x	x	
21	0	x	x	0	1	D → A
22	1	1	0	x	x	
23	1	1	0	x	x	
24	0	x	x	1	1	D → D
25	1	x	1	x	x	
26	1	x	1	x	x	

11.17. The Verilog code for Figure 11.12 is

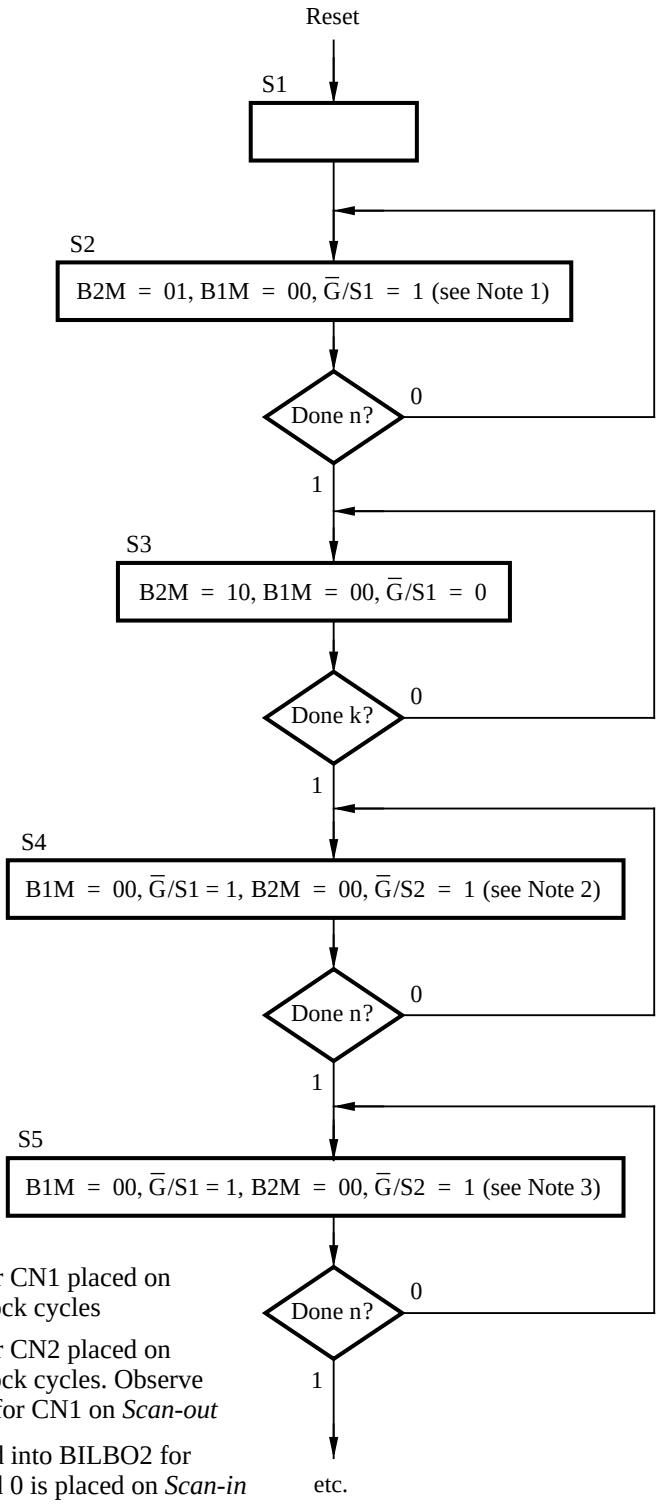
```
module prob11_17 (w, scanin, norm_scan, z, scanout, Resetn, Clock);
   input w, scanin, norm_scan, Resetn, Clock;
   output z, scanout;
   reg z, scanout;
   reg [2:1] y, Y, D;

   // Define the combinational circuitry
   always @(w or y or scanin or norm_scan)
   begin
      Y[1] = (w & ~y[1]) | (w & y[2]);
      Y[2] = (w & y[2]) | (w & y[1]);
      z = y[1] & y[2];
      if (norm_scan == 0)
      begin
         D[1] = Y[1];
         D[2] = Y[2];
      end
      else
      begin
         D[1] = scanin;
         D[2] = y[1];
      end
      scanout = y[2];
   end

   // Define the flip-flops
   always @(negedge Resetn or posedge Clock)
      if (Resetn == 0)  y <= 0;
      else  y <= D;

endmodule
```

11.18. For simplicity, it is assumed in the ASM chart that testing begins when the reset signal is de-asserted. The ASM chart corresponds to the first three steps listed on page 675; the other steps are similar and are not shown. In the ASM chart, B1M represents the two-bit signal M_1M_2 for BILBO1 and B2M represents M_1M_2 for BILBO2. Similarly, $\overline{G}/S1$ and $\overline{G}/S2$ represent the $\overline{G}/S$ signals for BILBO1 and BILBO2. Assume that there are n flip-flops in each BILBO register and that k clock cycles are used when running each BILBO circuit as a PRBS generator.



Notes

Note 1: Initial test data for CN1 placed on *Scan-in* over *n* clock cycles

Note 2: Initial test data for CN2 placed on *Scan-in* over *n* clock cycles. Observe generated results for CN1 on *Scan-out*

Note 3: BILBO1 is shifted into BILBO2 for *n* clock cycles and 0 is placed on *Scan-in*