Chapter 2

2.1. The proof is as follows:

$$(x+y) \cdot (x+z) = xx + xz + xy + yz$$

$$= x + xz + xy + yz$$

$$= x(1+z+y) + yz$$

$$= x \cdot 1 + yz$$

$$= x + yz$$

2.2. The proof is as follows:

$$(x+y) \cdot (x+\overline{y}) = xx + xy + x\overline{y} + y\overline{y}$$

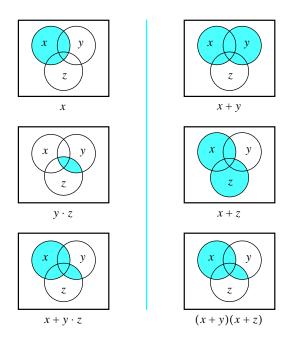
$$= x + xy + x\overline{y} + 0$$

$$= x(1+y+\overline{y})$$

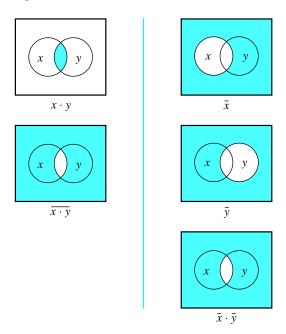
$$= x \cdot 1$$

$$= x$$

2.3. Proof using Venn diagrams:

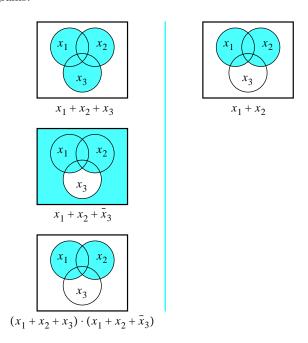


2.4. Proof of 15a using Venn diagrams:

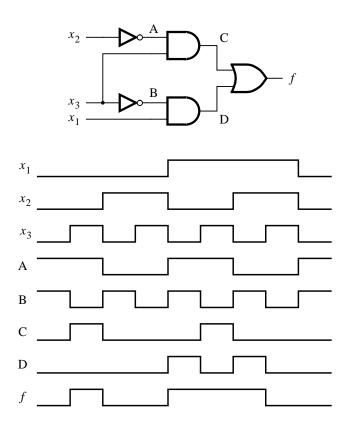


A similar proof is constructed for 15b.

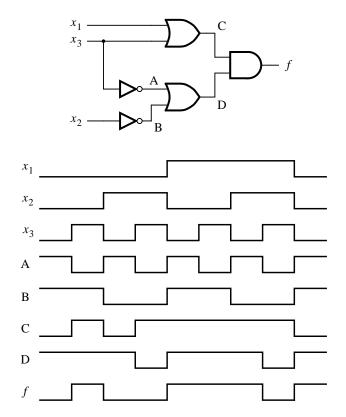
2.5. Proof using Venn diagrams:



- 2.6. A possible approach for determining whether or not the expressions are valid is to try to manipulate the left and right sides of an expression into the same form, using the theorems and properties presented in section 2.5. While this may seem simple, it is an awkward approach, because it is not obvious what target form one should try to reach. A much simpler approach is to construct a truth table for each side of an expression. If the truth tables are identical, then the expression is valid. Using this approach, we can show that the answers are:
 - (a) Yes
 - (b) Yes
 - (c) No
- 2.7. Timing diagram of the waveforms that can be observed on all wires of the circuit:



2.8. Timing diagram of the waveforms that can be observed on all wires of the circuit:



2.9. Starting with the canonical sum-of-products for f get

$$f = \overline{x_1}\overline{x_2}x_3 + \overline{x_1}x_2\overline{x_3} + \overline{x_1}x_2x_3 + x_1\overline{x_2}\overline{x_3} + x_1\overline{x_2}x_3 + x_1x_2\overline{x_3} + x_1x_2x_3$$

$$= x_1(\overline{x_2}\overline{x_3} + \overline{x_2}x_3 + x_2\overline{x_3} + x_2x_3) + x_2(\overline{x_1}\overline{x_3} + \overline{x_1}x_3 + x_1\overline{x_3} + x_1x_3)$$

$$+ x_3(\overline{x_1}\overline{x_2} + \overline{x_1}x_2 + x_1\overline{x_2} + x_1x_2)$$

$$= x_1(\overline{x_2}(\overline{x_3} + x_3) + x_2(\overline{x_3} + x_3)) + x_2(\overline{x_1}(\overline{x_3} + x_3) + x_1(\overline{x_3} + x_3))$$

$$+ x_3(\overline{x_1}(\overline{x_2} + x_2) + x_1(\overline{x_2} + x_2))$$

$$= x_1(\overline{x_2} \cdot 1 + x_2 \cdot 1) + x_2(\overline{x_1} \cdot 1 + x_1 \cdot 1) + x_3(\overline{x_1} \cdot 1 + x_1 \cdot 1)$$

$$= x_1(\overline{x_2} + x_2) + x_2(\overline{x_1} + x_1) + x_3(\overline{x_1} + x_1)$$

$$= x_1 \cdot 1 + x_2 \cdot 1 + x_3 \cdot 1$$

$$= x_1 + x_2 + x_3$$

2.10. Starting with the canonical product-of-sums for f can derive:

$$f = (x_1 + x_2 + x_3)(x_1 + x_2 + \overline{x_3})(x_1 + \overline{x_2} + x_3)(x_1 + \overline{x_2} + \overline{x_3}) \cdot (\overline{x_1} + x_2 + x_3)(\overline{x_1} + x_2 + \overline{x_3})(\overline{x_1} + \overline{x_2} + x_3)$$

$$= ((x_1 + x_2 + x_3)(x_1 + x_2 + \overline{x_3}))((x_1 + \overline{x_2} + x_3)(x_1 + \overline{x_2} + \overline{x_3})) \cdot ((\overline{x_1} + x_2 + x_3)(\overline{x_1} + x_2 + x_3))$$

$$= (x_1 + x_2 + x_3\overline{x_3})(x_1 + \overline{x_2} + x_3\overline{x_3}) \cdot (\overline{x_1} + x_2 + x_3\overline{x_3})(\overline{x_1} + \overline{x_2} + x_3\overline{x_3})$$

$$= (x_1 + x_2)(x_1 + \overline{x_2})(\overline{x_1} + x_2)(\overline{x_1} + x_3)$$

$$= (x_1 + x_2 \overline{x}_2)(\overline{x}_1 + x_2 x_3)$$

$$= x_1(\overline{x}_1 + x_2 x_3)$$

$$= x_1 \overline{x}_1 + x_1 x_2 x_3$$

$$= x_1 x_2 x_3$$

2.11. Derivation of the minimum sum-of-products expression:

$$f = x_1 x_3 + x_1 \overline{x}_2 + \overline{x}_1 x_2 x_3 + \overline{x}_1 \overline{x}_2 \overline{x}_3$$

$$= x_1 (\overline{x}_2 + x_2) x_3 + x_1 \overline{x}_2 (\overline{x}_3 + x_3) + \overline{x}_1 x_2 x_3 + \overline{x}_1 \overline{x}_2 \overline{x}_3$$

$$= x_1 \overline{x}_2 x_3 + x_1 x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 + \overline{x}_1 x_2 x_3 + \overline{x}_1 \overline{x}_2 \overline{x}_3$$

$$= x_1 x_3 + (x_1 + \overline{x}_1) x_2 x_3 + (x_1 + \overline{x}_1) \overline{x}_2 \overline{x}_3$$

$$= x_1 x_3 + x_2 x_3 + \overline{x}_2 \overline{x}_3$$

2.12. Derivation of the minimum sum-of-products expression:

$$f = x_1 \overline{x}_2 \overline{x}_3 + x_1 x_2 x_4 + x_1 \overline{x}_2 x_3 \overline{x}_4$$

$$= x_1 \overline{x}_2 \overline{x}_3 (\overline{x}_4 + x_4) + x_1 x_2 x_4 + x_1 \overline{x}_2 x_3 \overline{x}_4$$

$$= x_1 \overline{x}_2 \overline{x}_3 \overline{x}_4 + x_1 \overline{x}_2 \overline{x}_3 x_4 + x_1 x_2 x_4 + x_1 \overline{x}_2 x_3 \overline{x}_4$$

$$= x_1 \overline{x}_2 \overline{x}_3 + x_1 \overline{x}_2 (\overline{x}_3 + x_3) \overline{x}_4 + x_1 x_2 x_4$$

$$= x_1 \overline{x}_2 \overline{x}_3 + x_1 \overline{x}_2 \overline{x}_4 + x_1 x_2 x_4$$

2.13. The simplest POS expression is derived as

$$f = (x_1 + x_3 + x_4)(x_1 + \overline{x}_2 + x_3)(x_1 + \overline{x}_2 + \overline{x}_3 + x_4)$$

$$= (x_1 + x_3 + x_4)(x_1 + \overline{x}_2 + x_3)(x_1 + \overline{x}_2 + x_3 + x_4)(x_1 + \overline{x}_2 + \overline{x}_3 + x_4)$$

$$= (x_1 + x_3 + x_4)(x_1 + \overline{x}_2 + x_3)((x_1 + \overline{x}_2 + x_4)(x_3 + \overline{x}_3))$$

$$= (x_1 + x_3 + x_4)(x_1 + \overline{x}_2 + x_3)(x_1 + \overline{x}_2 + x_4) \cdot 1$$

$$= (x_1 + x_3 + x_4)(x_1 + \overline{x}_2 + x_3)(x_1 + \overline{x}_2 + x_4)$$

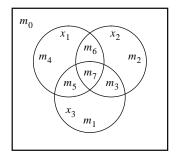
2.14. Derivation of the minimum product-of-sums expression:

$$f = (x_1 + x_2 + x_3)(x_1 + \overline{x}_2 + x_3)(\overline{x}_1 + \overline{x}_2 + x_3)(x_1 + x_2 + \overline{x}_3)$$

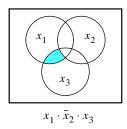
$$= ((x_1 + x_2) + x_3)((x_1 + x_2) + \overline{x}_3)(x_1 + (\overline{x}_2 + x_3))(\overline{x}_1 + (\overline{x}_2 + x_3))$$

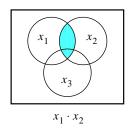
$$= (x_1 + x_2)(\overline{x}_2 + x_3)$$

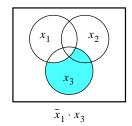
2.15. (a) Location of all minterms in a 3-variable Venn diagram:



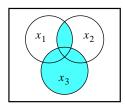
(b) For $f = x_1 \overline{x}_2 x_3 + x_1 x_2 + \overline{x}_1 x_3$ have:





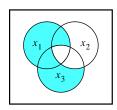


Therefore, f is represented as:



$$f = x_3 + x_1 x_2$$

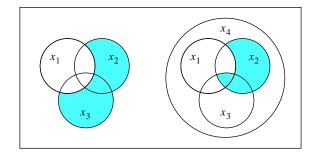
2.16. The function in Figure 2.18 in Venn diagram form is:



2.17. In Figure P2.1a it is possible to represent only 14 minterms. It is impossible to represent the minterms $\overline{x}_1\overline{x}_2x_3x_4$ and $x_1x_2\overline{x}_3\overline{x}_4$.

In Figure P2.1b, it is impossible to represent the minterms $x_1x_2\overline{x}_3\overline{x}_4$ and $x_1x_2x_3\overline{x}_4$.

2.18. Venn diagram for $f = \overline{x}_1 \overline{x}_2 x_3 \overline{x}_4 + x_1 x_2 x_3 x_4 + \overline{x}_1 x_2$ is



2.19. The simplest SOP implementation of the function is

$$f = \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 + x_1 x_2 \overline{x}_3 + x_1 x_2 x_3$$
$$= (\overline{x}_1 + x_1) x_2 x_3 + x_1 (\overline{x}_2 + x_2) \overline{x}_3$$
$$= x_2 x_3 + x_1 \overline{x}_3$$

2.20. The simplest SOP implementation of the function is

$$f = \overline{x}_1 \overline{x}_2 x_3 + \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 + x_1 x_2 \overline{x}_3 + x_1 x_2 x_3$$

$$= \overline{x}_1 (\overline{x}_2 + x_2) x_3 + x_1 (\overline{x}_2 + x_2) \overline{x}_3 + (\overline{x}_1 + x_1) x_2 x_3$$

$$= \overline{x}_1 x_3 + x_1 \overline{x}_3 + x_2 x_3$$

Another possibility is

$$f = \overline{x}_1 x_3 + x_1 \overline{x}_3 + x_1 x_2$$

2.21. The simplest POS implementation of the function is

$$f = (x_1 + x_2 + x_3)(x_1 + \overline{x}_2 + x_3)(\overline{x}_1 + x_2 + \overline{x}_3)$$

= $((x_1 + x_3) + x_2)((x_1 + x_3) + \overline{x}_2)(\overline{x}_1 + x_2 + \overline{x}_3)$
= $(x_1 + x_3)(\overline{x}_1 + x_2 + \overline{x}_3)$

2.22. The simplest POS implementation of the function is

$$f = (x_1 + x_2 + x_3)(x_1 + x_2 + \overline{x_3})(\overline{x_1} + x_2 + \overline{x_3})(\overline{x_1} + \overline{x_2} + \overline{x_3})$$

$$= ((x_1 + x_2) + x_3)((x_1 + x_2) + \overline{x_3})((\overline{x_1} + x_3) + x_2)((\overline{x_1} + x_3) + \overline{x_2})$$

$$= (x_1 + x_2)(\overline{x_1} + \overline{x_3})$$

2.23. The lowest cost circuit is defined by

$$f(x_1, x_2, x_3) = x_1x_2 + x_1x_3 + x_2x_3$$

2.24. The truth table that corresponds to the timing diagram in Figure P2.3 is

x_1	x_2	x_3	f
0	0	0	1
$0 \\ 0$	0 1	1 0	0
0	1	1	1
1	0	0	0
1	0	1	1
1 1	1 1	0 1	1 0
1	1	1	U

The simplest SOP expression is $f = \overline{x}_1 \overline{x}_2 \overline{x}_3 + \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 x_3 + x_1 x_2 \overline{x}_3$.

2.25. The truth table that corresponds to the timing diagram in Figure P2.4 is

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

The simplest SOP expression is derived as follows:

$$f = \overline{x}_1 \overline{x}_2 x_3 + \overline{x}_1 x_2 \overline{x}_3 + \overline{x}_1 x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3 + x_1 x_2 x_3$$

$$= \overline{x}_1 (\overline{x}_2 + x_2) x_3 + \overline{x}_1 \overline{x}_2 (\overline{x}_3 + x_3) + (\overline{x}_1 + x_1) x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3$$

$$= \overline{x}_1 \cdot 1 \cdot x_3 + \overline{x}_1 x_2 \cdot 1 + 1 \cdot x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3$$

$$= \overline{x}_1 x_3 + \overline{x}_1 x_2 + x_2 x_3 + x_1 \overline{x}_2 \overline{x}_3$$

2.26. (a)

x_1	x_0	y_1	y_0	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

(b) The simplest POS expression is

$$f = (x_1 + \overline{y}_1)(\overline{x}_1 + y_1)(x_0 + \overline{y}_0)(\overline{x}_0 + y_0)$$

2.27. (a)

x_1	x_0	y_1	y_0	f
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

(b) The canonical SOP expression is

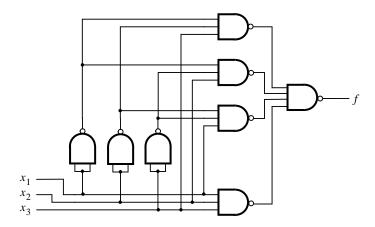
$$f = \overline{x}_1 \overline{x}_0 \overline{y}_1 \overline{y}_0 + \overline{x}_1 x_0 \overline{y}_1 \overline{y}_0 + \overline{x}_1 x_0 \overline{y}_1 y_0 + x_1 \overline{x}_0 \overline{y}_1 \overline{y}_0 + x_1 \overline{x}_0 \overline{y}_1 y_0 + x_1 \overline{x}_0 y_1 \overline{y}_0$$

$$+ x_1 x_0 \overline{y}_1 \overline{y}_0 + x_1 x_0 \overline{y}_1 y_0 + x_1 x_0 y_1 \overline{y}_0 + x_1 x_0 y_1 y_0$$

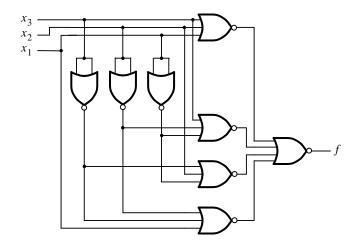
(c) The simplest SOP expression is

$$f = x_1 x_0 + \overline{y}_1 \overline{y}_0 + x_1 \overline{y}_0 + x_0 \overline{y}_1$$

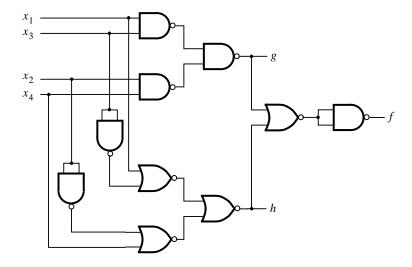
2.28. Using the ciruit in Figure 2.25a as a starting point, the function in Figure 2.24 can be implemented using NAND gates as follows:



2.29. Using the ciruit in Figure 2.25b as a starting point, the function in Figure 2.24 can be implemented using NOR gates as follows:

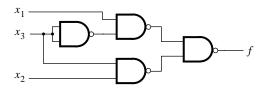


2.30. The circuit in Figure 2.33 can be implemented using NAND and NOR gates as follows:



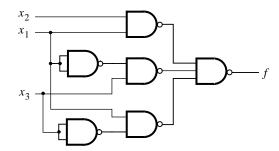
2.31. The minimum-cost SOP expression for the function $f(x_1,x_2,x_3)=\sum m(3,4,6,7)$ is $f=x_1\overline{x}_3+x_2x_3$

The corresponding circuit implemented using NAND gates is



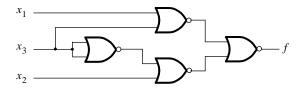
2.32. A minimum-cost SOP expression for the function $f(x_1,x_2,x_3)=\sum m(1,3,4,6,7)$ is $f=x_1x_2+x_1\overline{x}_3+\overline{x}_1x_3$

The corresponding circuit implemented using NAND gates is



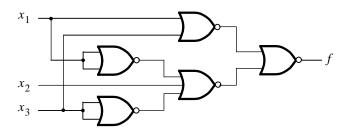
2.33. The minimum-cost POS expression for the function $f(x_1,x_2,x_3)=\sum m(3,4,6,7)$ is $f=(x_1+x_3)(x_2+\overline{x}_3)$

The corresponding circuit implemented using NOR gates is



2.34. The minimum-cost POS expression for the function $f(x_1, x_2, x_3) = \sum m(1, 3, 4, 6, 7)$ is $f = (x_1 + x_3)(\overline{x}_1 + x_2 + \overline{x}_3)$

The corresponding circuit implemented using NOR gates is



2.37. The circuit in Figure 2.25a can be implemented using;

endmodule

2.38. The circuit in Figure 2.25b can be implemented using;

```
module prob2_38 (x1, x2, x3, f);
input x1, x2, x3;
output f;

not (notx1, x1);
not (notx2, x2);
not (notx3, x3);
or (a, x1, x2, x3);
or (b, notx1, notx2, x3);
or (c, notx1, x2, notx3);
or (d, x1, notx2, notx3);
and (f, a, b, c, d);
```

endmodule

2.39. The simplest circuit is obtained in the POS form as

$$f = (x_1 + x_2 + x_3)(\overline{x}_1 + \overline{x}_2 + \overline{x}_3)$$

Verilog code that implements the circuit is

```
\begin{array}{l} \textbf{module} \ \ prob2\_39 \ (x1, x2, x3, f);\\ \textbf{input} \ \ x1, x2, x3;\\ \textbf{output} \ \ f;\\ \\ \textbf{or} \ (g, x1, x2, x3);\\ \textbf{or} \ (h, \sim\!\!x1, \sim\!\!x2, \sim\!\!x3);\\ \textbf{and} \ (f, g, h); \end{array}
```

endmodule

2.40. The simplest circuit is obtained in the SOP form as

$$f = \overline{x}_2 + \overline{x}_1 x_3 + x_1 \overline{x}_3$$

Verilog code that implements the circuit is

$$\label{eq:module_prob2_40} \begin{split} & \textbf{module} \ \ prob2_40 \ (x1, x2, x3, f); \\ & \textbf{input} \ \ x1, x2, x3; \\ & \textbf{output} \ \ f; \\ & \textbf{assign} \ f = \sim & x2 \ | \ (\sim & x1 \ \& \ x3) \ | \ (x1 \ \& \ \sim & x3); \end{split}$$

endmodule

2.41. The Verilog code is

```
\label{eq:module_prob2_41} \begin{split} & \textbf{module} \ \ prob2\_41 \ (x1, x2, x3, x4, f1, f2); \\ & \textbf{input} \ \ x1, x2, x3, x4; \\ & \textbf{output} \ \ f1, f2; \\ & \textbf{assign} \ \ f1 = (x1 \ \& \ \sim \! x3) \ | \ (x2 \ \& \ \sim \! x3) \ | \ (\!\sim \! x3 \ \& \ \sim \! x4) \ | \ (x1 \ \& \ x2) \ | \ (x1 \ \& \ \sim \! x4); \\ & \textbf{assign} \ \ f2 = (x1 \ | \ \sim \! x3) \ \& \ (x1 \ | \ x2 \ | \ \sim \! x4) \ \& \ (x2 \ | \ \sim \! x3) \ | \ \sim \! x4); \end{split}
```

endmodule

2.42. The Verilog code is

```
\label{eq:module_prob2_42} \begin{split} & \textbf{module} \ \ prob2\_42 \ (x1, x2, x3, x4, f1, f2); \\ & \textbf{input} \ \ x1, x2, x3, x4; \\ & \textbf{output} \ \ f1, f2; \\ \\ & \textbf{assign} \ \ f1 = (x1 \ \& \ x3) \ \big| \ (\sim\!x1 \ \& \ \sim\!x3) \ \big| \ (x2 \ \& \ x4) \ \big| \ (\sim\!x2 \ \& \ \sim\!x4); \\ & \textbf{assign} \ \ f2 = (x1 \ \& \ x2 \ \& \ \sim\!x3 \ \& \ \sim\!x4) \ \big| \ (\sim\!x1 \ \& \ \sim\!x2 \ \& \ x3 \ \& \ x4) \ \big| \\ & (x1 \ \& \ \sim\!x2 \ \& \ \sim\!x3 \ \& \ x4) \ \big| \ (\sim\!x1 \ \& \ x2 \ \& \ x3 \ \& \ \sim\!x4); \\ \end{split}
```

endmodule