cadence®

Voltus IC Power Integrity Solution Known Problems and Solutions

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Contents

1

Voltus Known Problems and Solutions

This Known Problems and Solutions (KP&S) document describes important Cadence Change Requests (CCRs) for Voltus IC Power Integrity Solution and tells you how to solve or work around these problems.

Fixed CCRs are listed in the README file accompanying this release.

Identified in Previous Releases

CCR 1240119: Distributed processing is taking more hosts than specified

Description: When running IR Drop Analysis in the multi-CPU mode using the LSF job submission script, distributed processing uses more number of hosts than specified. For example, when "`set_multi_cpu_usage -remoteHost 2 -cpuPerRemoteHost 8`" is specified, it takes four hosts instead of two hosts. In the LSF mode, distributed processing submits only one LSF job per slave and is unable to run multiple jobs on the same host machine.

Solution: Use the RSH mode to run 2 distributed hosts with 4 slave processes.

CCR 1109065: Leakage value changing with changing order of Liberty files

Description: If there is a change in the order in which Liberty files are read in, leakage interpolation leads to different values.

Solution: Specify the Liberty files based on the voltage values, which must be sorted in the ascending order, to have better voltage-based interpolation. This also applies to temperature-based

interpolation. This will be fixed in a later release.

CCR 1105272: Current Characterization flow not working with .lib containing only scalar energy

Description: If internal power tables in a .lib has only scalar energy values, even if .lib has internal-power with the “when” condition, the current characterization flow cannot parse the power table correctly.

Solution: Edit the .lib to specify the `internal_power` table with the slew and load template. This will be fixed in a later release.

CCR 1104014: Generating a die model without virtual ground can result in unstable Spice simulation

Description: Creating a die model with `create_die_model -model_transform_method {res_shielding}` and disabling global node zero (`-disable_global_node_zero true`), can lead to stability issues when running the die model in Spice simulators.

Solution: You can create a die model with `-disable_global_node_zero` set to `false`. This will be fixed in a later release.

CCR 1095292: Ignore fillers creating large unconnected section

Description: If fillers are used to preserve connectivity on the M1 layer, ignoring them using `set_rail_analysis_mode -ignore_fillers true` would result in disconnects in the power-grid.

Solution: Use follow-pin routing for the M1 (and sometimes M2) layer, therefore, ignoring filler cells from analysis does not result in connectivity problems. This will be fixed in a later release.

CCR 1093337: Event-based Power Profiler calculates leakage power using average duty cycle

Description: When running the event-based vector profiling flow, the leakage power numbers will not be event-based but still will be calculated based on the average duty cycle.

Solution: This will be fixed in a later release.

CCR 1088489: set_switching_activity -clock only supports scaling of a single clock

Description: The `-clock` parameter of the `set_switching_activity` command does not support scaling of multiple clocks at the same time.

Solution: You can specify the command multiple times with different clocks.

CCR 1072855: Incorrect CPU time reported in log file

Description: In this release, the CPU time reported in the log file may not include all the child processes.

Solution: This will be fixed in a later release.

CCR 1071791: Library generation fails if Spice model contains 'LG' or 'WG'

Description: During library characterization, if there is a Spice netlist and model containing 'LG' and 'WG' as the length and width parameter names, Voltus Library Simulator gives an error message and power-grid library building fails. The Library Simulator cannot recognize 'LG' and 'WG,' and expects only 'l' and 'w' for parameter names (case-insensitive) to compute current distribution.

Solution: Replace 'LG' and 'WG' parameters with 'l' and 'w'. This will be fixed in a later release.

CCR 964264: Die model generation takes a long time with -model_transform_method

Description: When the `create_die_model -model_transform_method {res_shielding}` parameter is used for die model generation, the time taken to generate the die model is expected to increase by about 2x in comparison to die model generation without this parameter.

Solution: This will be fixed in a later release.

CCR 859844: Need to support non 0 capacitance filler cells for Decap Optimization flow

Description: If a cell is tagged as a filler cell, and you provide capacitance value for it during library generation, the cell capacitance will be ignored during rail analysis and decap optimization.

Solution: This will be fixed in a later release.

CCR 853412: Native power-up flow has an accuracy problem when PSW has large device length inside

Description: Concurrent power-up analysis using `set_rail_analysis_mode -powering_up_rails` produces inaccurate results when a design is using custom long-channel power-gate cells. The problem stems from the modeling of such long-channel power-gate cells that require longer simulation times during library characterization to accurately capture slew and delay.

Solution: This will be fixed in a later release.