Synopsys® Custom Infrastructure Overview

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About This Manual

This document highlights the common use model and features of the Synopsys® Custom Infrastructure technology. It provides an overview of the Synopsys products that run on the Custom Infrastructure environment.

This preface includes the following sections:

- New in This Release
- Related Products, Publications, and Trademarks
- Conventions
- Customer Support
- · Statement on Inclusivity and Diversity

New in This Release

Information about new features, enhancements, and changes, known limitations, and resolved Synopsys Technical Action Requests (STARs) is available in the Custom Infrastructure Release Notes on the SolvNetPlus site.

Related Products, Publications, and Trademarks

For additional information about the Custom Compiler tool, see the documentation on the Synopsys SolvNetPlus support site at the following address:

https://solvnetplus.synopsys.com

You might also want to see the documentation for the following related Synopsys products:

- Custom Compiler™
- PrimeSim™ SPICE and PrimeSim™ Pro
- PrimeSim™ HSPICE®
- PrimeSim™ XA
- PrimeWave Design Environment™
- PrimeWave Reliability Environment™
- OptoCompiler™

- StarRC™ Parasitic Explorer
- IC Validator™

Conventions

The following conventions are used in Synopsys documentation.

Convention	Description
Courier	Indicates syntax, such as write_file.
Courier italic	<pre>Indicates a user-defined value in syntax, such as write_file design_list</pre>
Courier bold	<pre>Indicates user input—text you type verbatim—in examples, such as prompt> write_file top</pre>
Purple	 Within an example, indicates information of special interest. Within a command-syntax section, indicates a default, such as include_enclosing = true false
[]	Denotes optional arguments in syntax, such as write_file [-format fmt]
	Indicates that arguments can be repeated as many times as needed, such as pin1 pin2 pinN.
I	Indicates a choice among alternatives, such as low medium high
\	Indicates a continuation of a command line.
1	Indicates levels of directory structure.
Bold	Indicates a graphical user interface (GUI) element that has an action associated with it.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy .
Ctrl+C	Indicates a keyboard combination, such as holding down the Ctrl key and pressing C.

Customer Support

Customer support is available through SolvNetPlus.

Accessing SolvNetPlus

The SolvNetPlus site includes a knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. The SolvNetPlus site also gives you access to a wide range of Synopsys online services including software downloads, documentation, and technical support.

To access the SolvNetPlus site, go to the following address:

https://solvnetplus.synopsys.com

If prompted, enter your user name and password. If you do not have a Synopsys user name and password, follow the instructions to sign up for an account.

If you need help using the SolvNetPlus site, click REGISTRATION HELP in the top-right menu bar.

Contacting Customer Support

To contact Customer Support, go to https://solvnetplus.synopsys.com.

Statement on Inclusivity and Diversity

Synopsys is committed to creating an inclusive environment where every employee, customer, and partner feels welcomed. We are reviewing and removing exclusionary language from our products and supporting customer-facing collateral. Our effort also includes internal initiatives to remove biased language from our engineering and working environment, including terms that are embedded in our software and IPs. At the same time, we are working to ensure that our web content and software applications are usable to people of varying abilities. You may still find examples of non-inclusive language in our software or documentation as our IPs implement industry-standard specifications that are currently under review to remove exclusionary language.

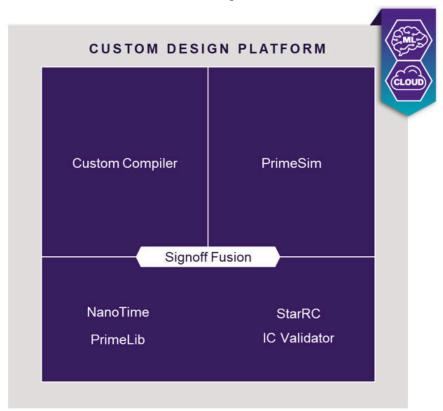
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Overview of Custom Infrastructure

This topic introduces the tools on the Synopsys Custom Design Platform and provides an overview of the Custom Infrastructure technology.

The Synopsys Custom Design Platform is a unified suite of design and verification tools that accelerate the development of robust custom designs. The platform features industry-leading circuit simulation engines and fast, easy-to-use schematic editor, layout editor, and simulation and analysis environment, complemented with best-in-class technologies for parasitic extraction, reliability analysis, and physical verification.

Figure 1 Tools on the Custom Design Platform



The Custom Infrastructure technology is a complete user environment which is the foundation for the Custom Design Platform and the tools which are built on it. When any of these tools are invoked, the tool-specific, interactive GUI and functionalities are provided by the Custom Infrastructure technology.

The Custom Design Platform consists of the following tools:

- The Custom Compiler tool:
 - A fast, user-friendly solution for custom design and layout, especially for advanced node designs
 - The PrimeWave Design Environment provides design analysis environment for netlisting and simulation. The analog circuit simulation tools, and a waveform viewer for pre- and post-layout circuit is used for simulation and analysis.
 - The PrimeWave Reliability Environment provides a workflow driven custom design environment for application-specific setup and analysis for the PrimeSim Circuit Check and EMIR simulation tools
- · Circuit simulation tools including:
 - The PrimeSim SPICE simulator, which is the fast and accurate SPICE simulator for custom digital and analog/RF designs
 - The PrimeSim Pro simulator, which provides the speed and capacity for modern DRAM and flash memory designs
 - The PrimeSim HSPICE simulator, which provides signoff reference for foundation IP and signal and power integrity analyses
 - The PrimeSim XA simulator, which is the number one FastSPICE simulator for mixed-signal SOC and SRAM designs
- The StarRC extraction and IC Validator tools, which provide key differentiated value to the platform through two powerful fusion technologies:
 - Extraction fusion, which provides faster design closure enabling designers to extract parasitics from partially-completed layout with the StarRC tool
 - DRC fusion, which reduces costly layout iterations by catching design rule errors during layout with the IC Validator tool

2

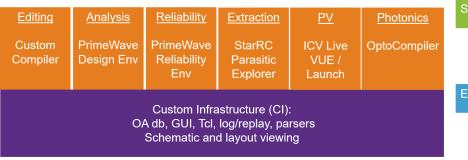
Custom Infrastructure Features

This topic discusses the features of the Custom Infrastructure environment.

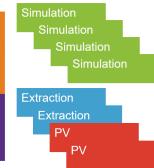
The Custom Infrastructure environment, as the name suggests, provides a unified, consistent, interactive user-interface and workflow for running all Synopsys products in the Synopsys custom design flow. This means that, the products can take advantage of the Custom Infrastructure features to enable specific design activities, as required, without the need to have a full custom design editing tool.

Running Synopsys products on the Custom Infrastructure environment facilitates seamless design flow and contributes to faster turnaround time.

Figure 2 Unified Interactive Infrastructure
Interactive Tools



Batch Engines



The Custom Infrastructure environment enables all interactive tools providing design editing, analysis, reliability, extraction, physical verification, and specialized functions like Photonics, to utilize a common window framework, with common schematic and layout viewing capabilities. The environment also enables these tools to work seamlessly with the best-in-class simulation, extraction, and physical verification engines from Synopsys.

The interactive tools are able to consistently use the Custom Infrastructure capabilities, such as viewport settings, layer-purpose-pairs, selections and visibility, object and logical information selections, rendering, highlighting, shadow mode, hierarchical descend, return, and edit-in-place, contributing to a continuous, whole design flow experience.

The components of the Custom Infrastructure environment are:

OpenAccess (OA) database:

The technology data, used by the interactive tools that run on this platform, is the standard OA technology data. The Custom Compiler tool, for example, uses cellViews (schematic, symbol, or layout) of the hierarchical OA design database for creating and editing designs and for design reviews.

GUI (see Figure 3 and Figure 4):

The Custom Infrastructure user interface includes the following main components:

- Home tab: This tab is pinned by default and lets you launch applications, open the Console assistant, access command menus and recent views, and open new tabs.
 The menu bar contains the File, Tools, License, Options, Window, and Help menus.
- Console tab: The command input text box in this tab accepts Tcl commands, and absolute or relative coordinates, for canvas design operations. The three Console panes namely the Output, History, and Errors/Warnings display the log of the current session, all commands executed in the session, including those that occur as a result of GUI inputs, and the error and warning messages for the session, respectively.

Home
Tab

Tabel Library Managar

PrineWave Design

Elbrary Managar

PrineWave Design

Environment

Syllusys

Tabs for Application

Tabs for Application

Tabs for Recent

Designs

Figure 3 Software User Interface



Figure 4 Standard Toolbar and Console Menus and Tabs

- Tabs for tools and designs: These tabs open the various tools and designs in new tabs within the same window.
- Tool Command Language (Tcl):

Tcl commands, objects, and preferences are available for designing, for interacting with the environment, and for customizing interfaces to obtain the preferred design experience. Tcl commands are categorized into several namespaces based on their function, such as db:: for database operations and le:: for layout editing purposes.

You can execute individual Tcl commands in the **Console** pane or in the command input text box in the **Console** tab. You can also run Tcl scripts to automate Tcl command sequences.

Log/Replay:

When you start a session, you have the option of rerunning the commands and other operations of a previous session. using the log file of the session. You can replay in an interactive debug mode. You can set breakpoints in the log file, to stop/continue the replay at each breakpoint. You can later remove the breakpoints.

Parsers:

XML parser for parsing the technology data and the configuration files for Process Design Kits (PDKs) for DRC, LVS, and PVE, the LEF/DEF parser, and the Parameter Expression Language (PEL) parser.

Schematic and layout viewers:

The schematic viewer shows the schematic of your circuit with the design components and the connections between the devices, including power and signal connections.

The layout viewer shows the physical layout of the circuit with the physical arrangement of the electrical wires and the components.

Cross-probes:

You can create and use device and net cross-probes, to probe the schematic and/ or parasitic views. When you select the probe for an instance or net in one view, the system automatically highlights the element in the alternate views.

3

Products on Custom Infrastructure

This topic provides an overview of the products that run on the Custom Infrastructure environment.

The following products are built on and run on the Custom Infrastructure environment:

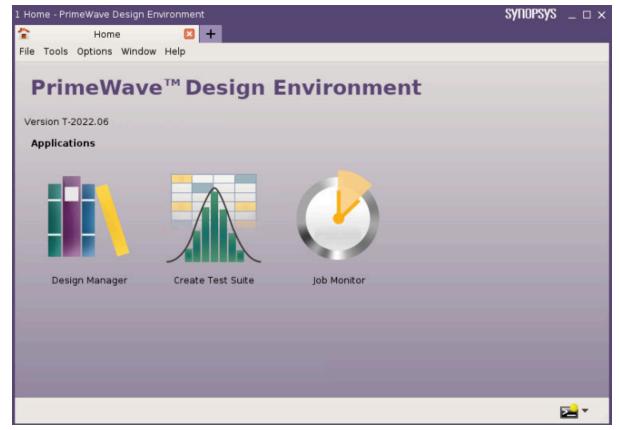
This topic includes the following sections:

- PrimeWave Design Environment
- PrimeWave Reliability Environment
- OptoCompiler
- StarRC Parasitic Explorer

PrimeWave Design Environment

The PrimeWave Design Environment tool runs on the Custom Infrastructure technology. The tool provides a custom environment for netlisting and simulation, using the analog circuit simulation tools, and a waveform viewer for pre- and post-layout circuit simulation and analysis.

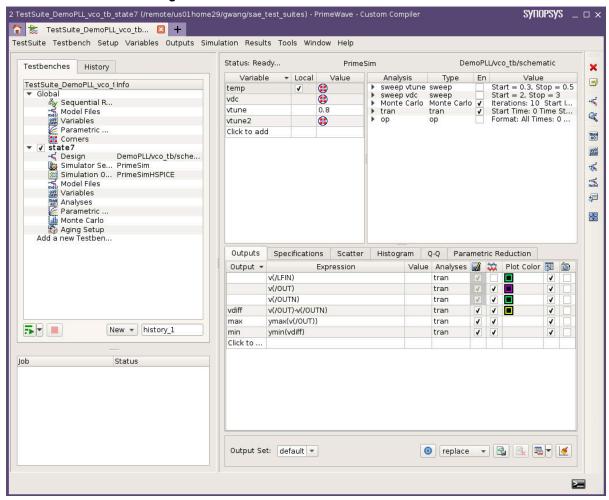
Figure 5 PrimeWave Design Environment on Custom Infrastructure



Note:

Some of the features shown in Figure 6 are limited availability. For information about these features, refer to SolvNetPlus article #000036534 "How to Enable the PrimeWave Design Environment Flow-Based Interface" or consult your Synopsys representative.

Figure 6 PrimeWave Design Environment: Testbenches



Tb_Opamp 🗵 🎹 Tb_Opamp - Result... 🗵 🗞 Job Monitor File History Testbench Table Help Histogram Scatter Q-Q Multiple-Axis Testbenches Testbenches (histor... ▼ = corner1 ▼ smallSignalSetup corner Charts Summaries 1.70825e+06 0 533182 temp MON...RLO dc_gain ugf pm Filter: Filter ▼ All 1.90872e+06 Multiple-Axis Descriptio ✓ [Check All]

✓ [temp

✓ MONTE_CARLO

✓ Edgain:ac ✓ III pm:ac
✓ III ugf:ac MON...RLO ugf Re-evaluate Simulation done

Figure 7 PrimeWave Design Environment: Results Viewer

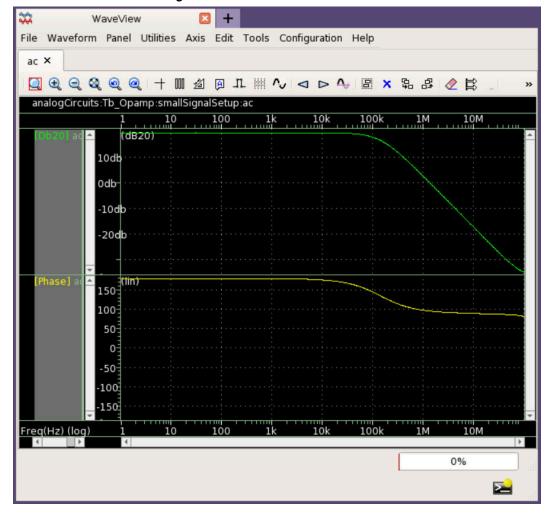


Figure 8 PrimeWave Design Environment: Waveform Viewer

For detailed information on the PrimeWave Design Environment tool, see the PrimeWave™ Design Environment User Guide and the PrimeWave™ Design Environment WaveView Tool User Guide.

PrimeWave Reliability Environment

The PrimeWave Reliability Environment tool runs on the Custom Infrastructure technology. The tool provides a workflow driven custom design environment for application-specific setup and analysis for the PrimeSim Circuit Check and EMIR simulation tools.

The workflow includes importing schematic/layout views and generating netlists from the resulting OpenAccess (OA) database based on available iPDKs. It sets up analysis test benches using PrimeWave Design Environment, and easily analyzes the results using

advanced visualization. It provides efficient debugging on application-specific OA views which are easy to customize.





The PrimeSim CCK App available in the PrimeWave Reliability Environment can be used in both Custom Compiler and 3rd party schematic viewing tools. It consists of a circuit check setup wizard with push-button setup, run, and debug features. The OA view is used to save setup, violation, waiver data with bottom-up waiver flow support, and schematic annotations of results.

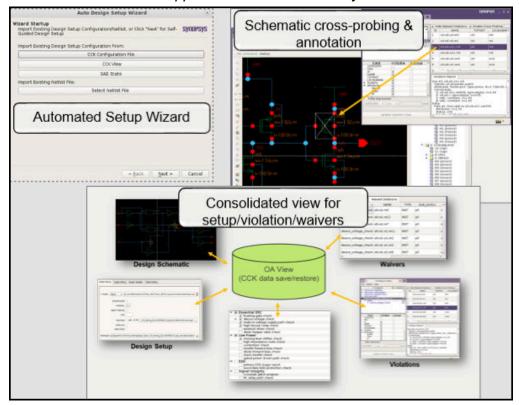
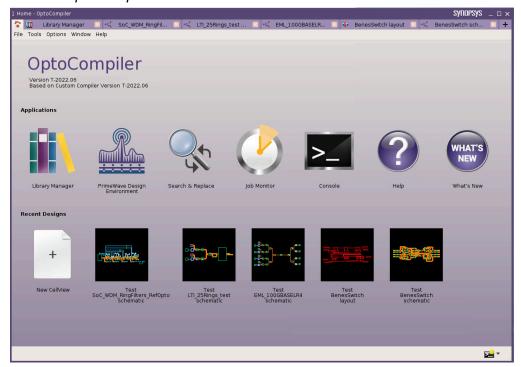


Figure 10 PrimeSim CCK App for PrimeWave Reliability Environment

OptoCompiler

The OptoCompiler tool, which is the industry-standard Photonic Integrated Circuit (PIC) design tool, runs on the Custom Infrastructure environment.

Figure 11 OptoCompiler on Custom Infrastructure



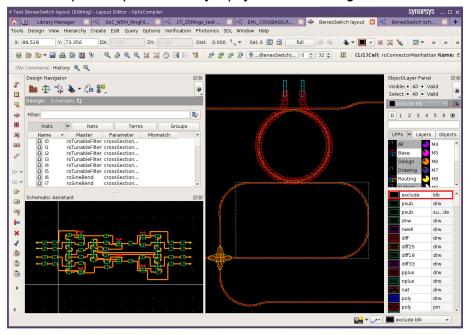


Figure 12 OptoCompiler in the Synopsys Custom Design Flow

The notable features of this solution include:

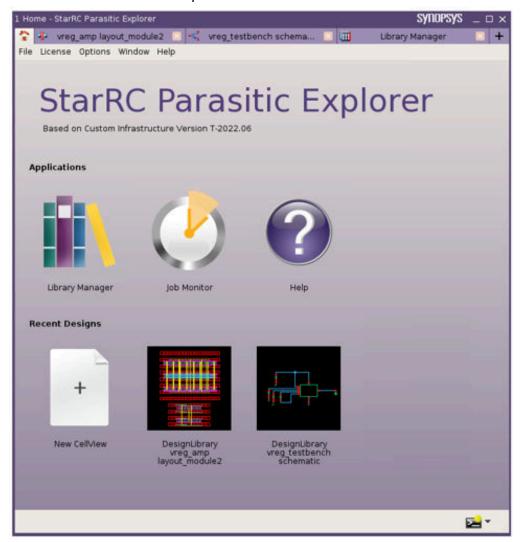
- · Unified platform for co-design
- Complete AMS capability from Synopsys
- Interactive environment
- · Photonic-aware layout synthesis
- Smart design features
- · Interoperability with other Synopsys products

For a detailed introduction to the OptoCompiler tool, see *About the OptoCompiler Tool* in the *OptoCompiler User Guide*. For information on how to use the OptoCompiler tool, see the *OptoCompiler User Guide*.

StarRC Parasitic Explorer

The StarRC Parasitic Explorer tool runs on the Custom Infrastructure environment. The tool helps you query parasitic resistors and capacitors stored in the Galaxy parasitic database (GPD) created by the StarRC extraction tool.

Figure 13 StarRC Parasitic Explorer on Custom Infrastructure



Open/short violations Design StarRC ▶ Short: 10 and v_2_i|8 X 1 X 2 X 3 X 4 X 5 X 6 X 7 Short between net 10 and net amp2| 12 Layer = pgate BBox=(2.845 0.9.4700),(2.9950,10.4700) Associated Objects No Associated Objects No Parent Markers GPD compare capacitance 23.5340675243 6.8 2.0 16.73 246.09 % 25.0667833836 6.8 2.0 18.27 268.63 % vdd! 3.73984222313 0.28 --3.46 1235.66 % outpl 2.68513529784 0.3 -- 2.39 795.05 % NBIAS 3.46492730617 0.3 -- 3.16 1054.98 % outm3 1.62383050754 0.3 -- 1.32 441.28 % outp2 1.04346499492 0.3 -- 0.74 247.82 outm2 1.04909267061 1.0 -- 0.05 4.91 %

Figure 14 StarRC Parasitic Explorer Features

For a detailed introduction to the StarRC Parasitic Explorer tool, see *Parasitic Explorer Features* in the *StarRC Parasitic Explorer User Guide*. For information on how to use the StarRC Parasitic Explorer tool, see *Using the Parasitic Explorer Tool* in the *StarRC Parasitic Explorer User Guide*.