Project 4: Multi-level cache 구현

20191146 정소희

files: (zipped in 201911146_정소희.zip)

cache.c (code file)

201911146_report_p4.pdf (project report file)

compile environment:

`gcc -o3 -o runfile cache.c -lm`

version: wsl2, gcc (Ubuntu 9.4.0-1ubuntu1~20.04) 9.4.0 환경에서 컴파일 되었다.

running environment:

c code file

version: wsl2 환경에서 Ubuntu 20.04.4 LTS에서 실행되었다.

실행 방법:

`./runfile <-c capacity> <-a associativity> <-b block_size> <-lru 또는 -random> <trace file name>`

Example:

```
$ ./runfile -c 4 -a 1 -b 16 -random 400_perlbench.out
```

과제 설명:

L1, L2 cache를 주어진 과제 지침에 맞추어 emulate 하는 프로그램이다.

struct cache block을 define하여 array를 static하게 선언하였다.

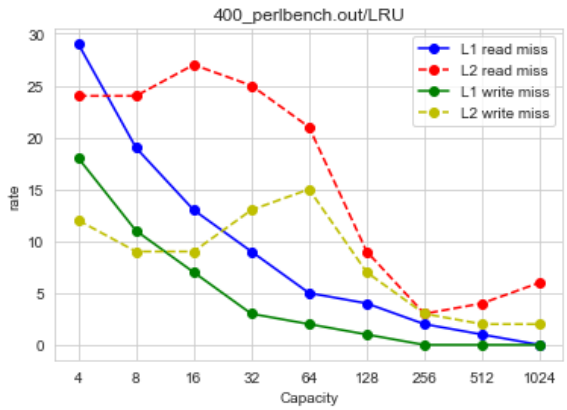
두 모든 교체 정책에서 l2 miss에서 evict할시, l2가 l1의 superset이 될수 있도록 맞추어 확인하였다.

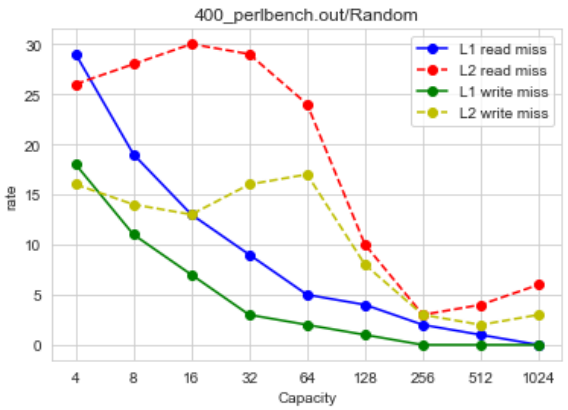
같은 폴더 내에 있는 out 파일에 대해서만 실행 가능하다.

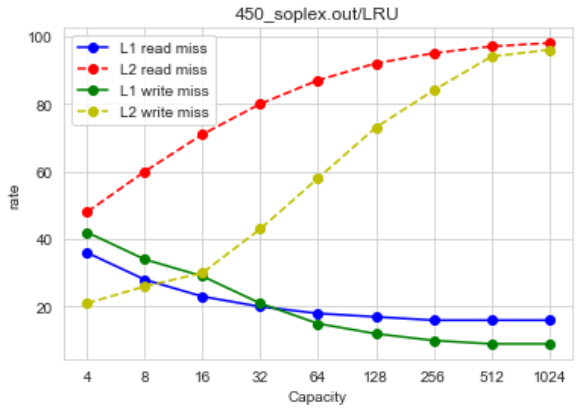
프로그램의 출력 값으로 `<filname_option.out>` 이 나온다.

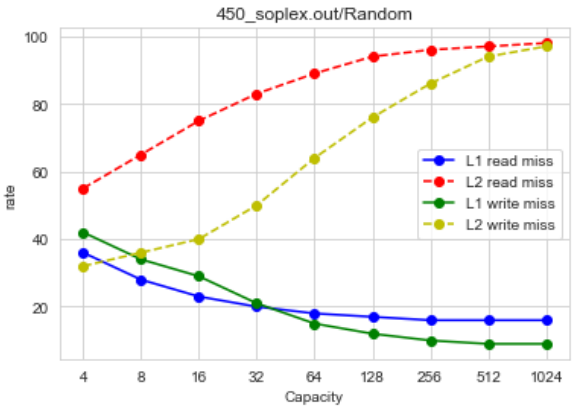
과제 결과:

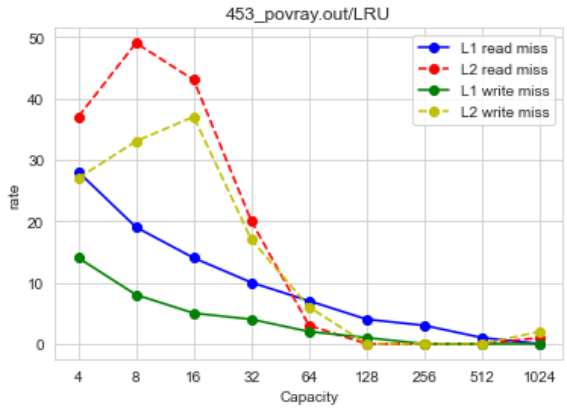
associativity 4, block size 32, cache size (4~1024), (lru and random)에 대한 표이다.

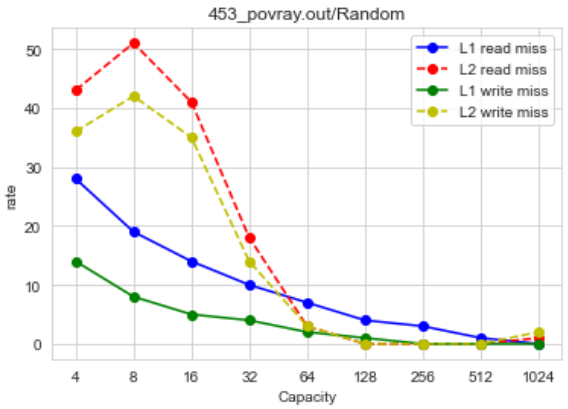

400_perlbench.out/LRU
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
5
10
15
20
25
30

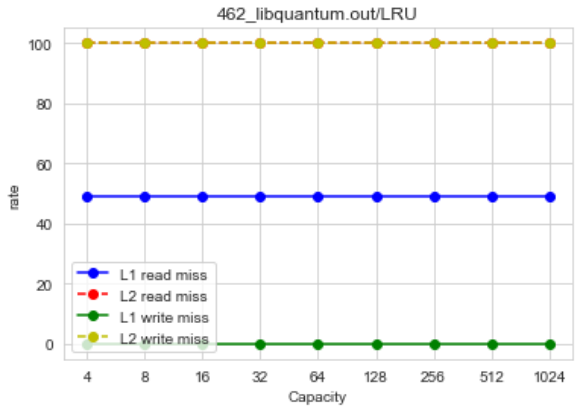

400_perlbench.out/Random
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
5
10
15
20
25
30

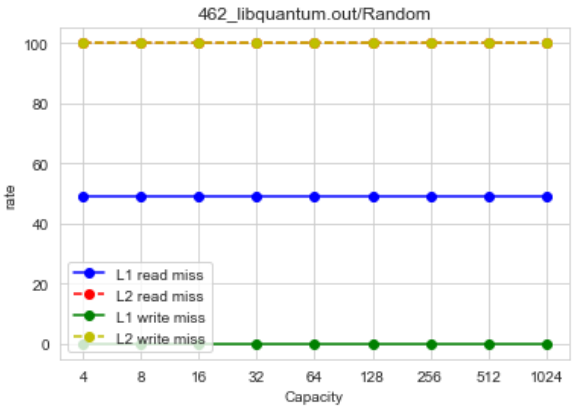

450_soplex.out/LRU
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
20
40
60
80
100

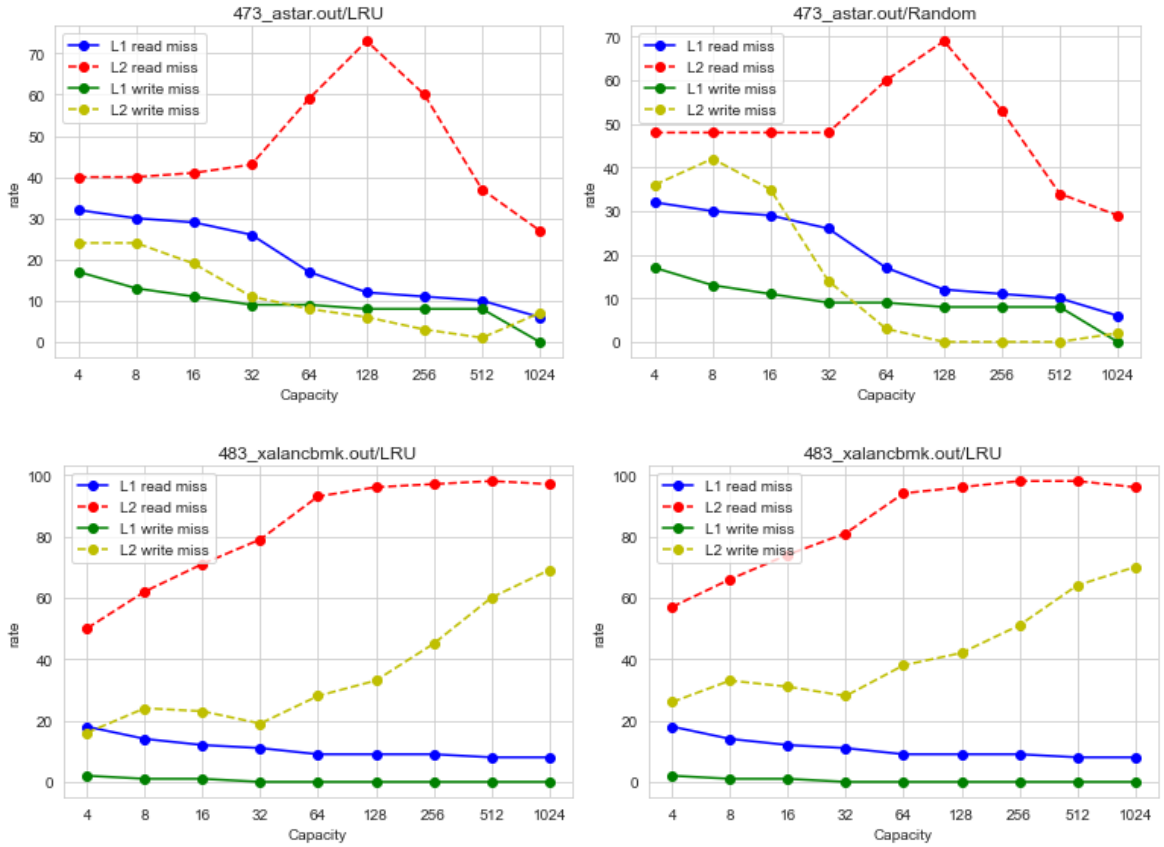

450_soplex.out/Random
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
20
40
60
80
100


453_povray.out/LRU
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
10
20
30
40
50


453_povray.out/Random
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
10
20
30
40
50

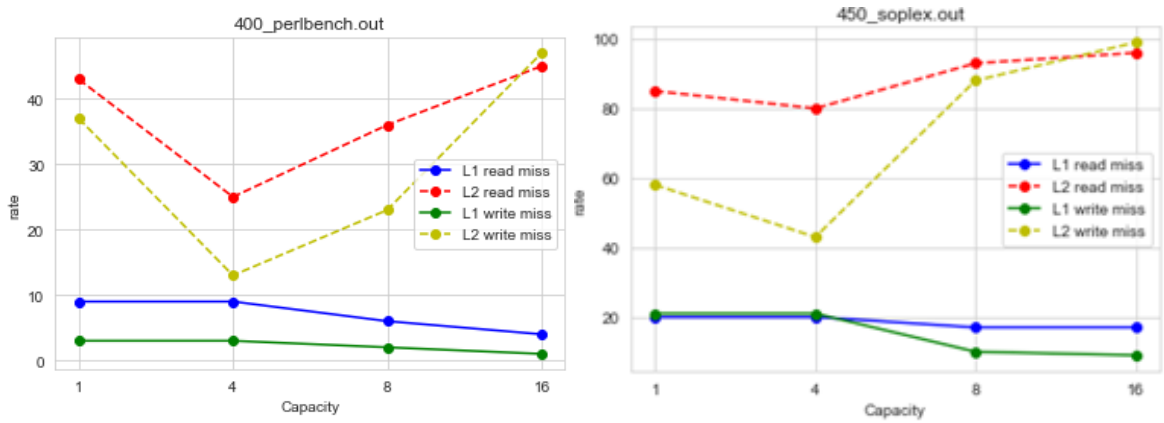

462_libquantum.out/LRU
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
20
40
60
80
100

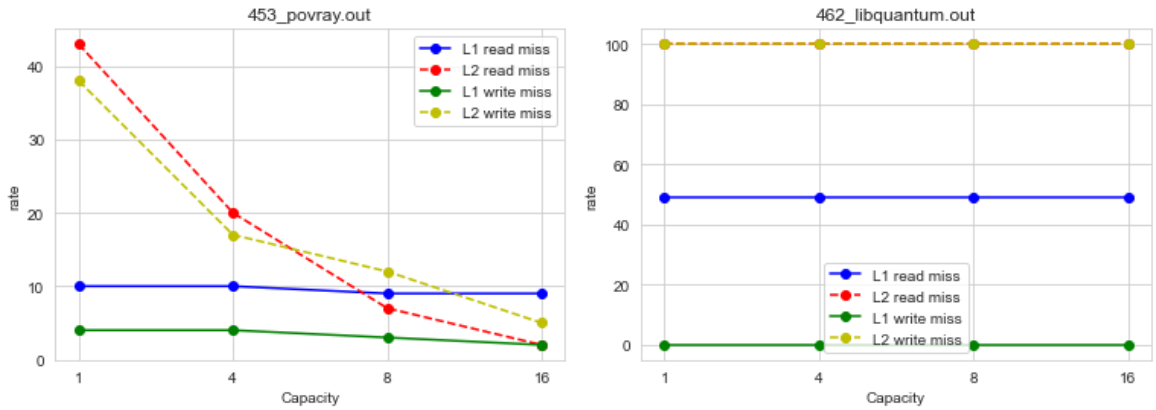

462_libquantum.out/Random
L1 read miss
L2 read miss
L1 write miss
L2 write miss
rate
Capacity
4
8
16
32
64
128
256
512
1024
0
20
40
60
80
100

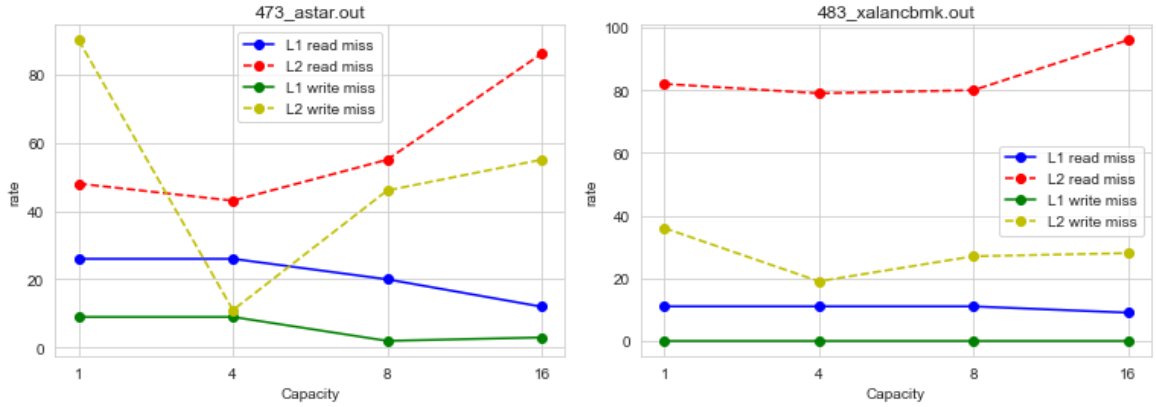


Cache Capacity가 증가할 수록, L1의 Miss rate는 낮아지는 추세를 보인다. (462.out 제외)
Random과 LRU는 거의 비슷한 값을 보인다.

associativity (1,4,8,16), block size 32, cache size 32, lru에 대한 표이다.

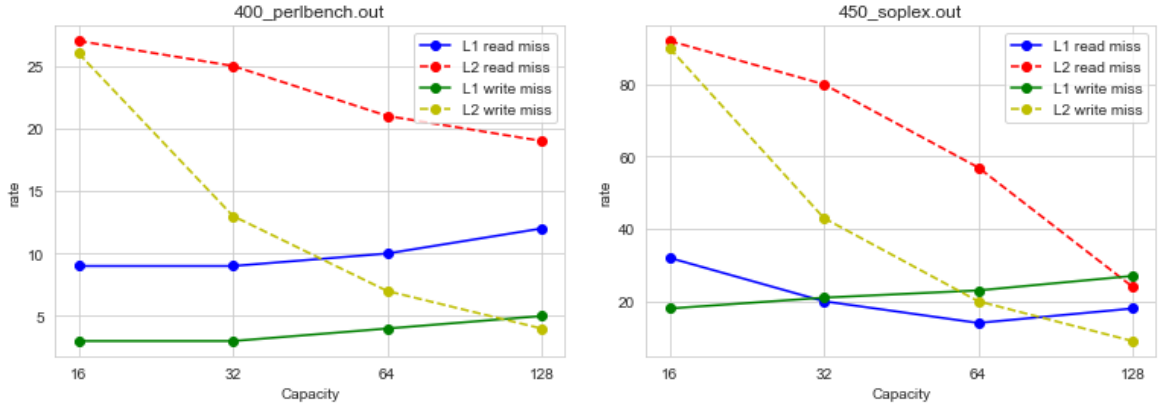


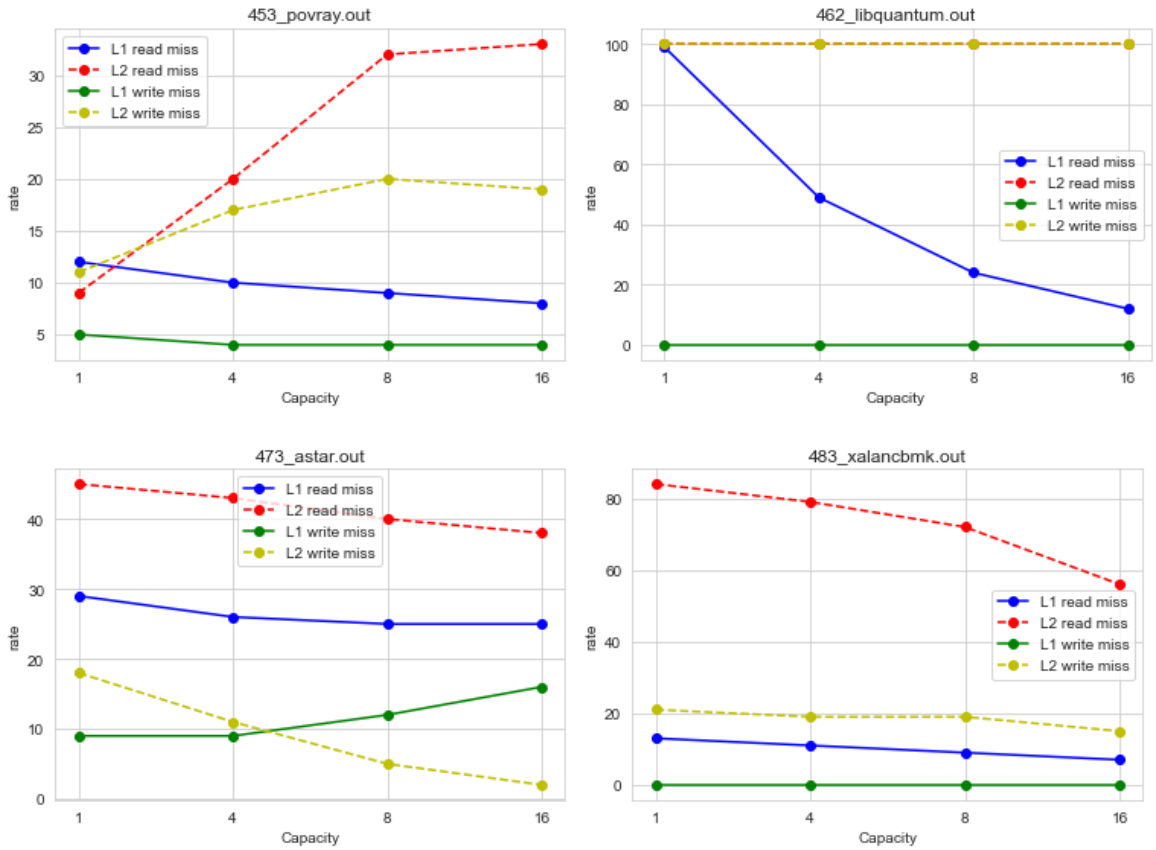




associativity가 커질수록 약간의 L1 miss rate가 낮아지는 추세를 보인다.

associativity 4, block size (16,32,64,128), lru, cache size 32에 대한 표이다.





Block가 커질수록 L1 miss rate가 낮아지는 test set도 존재하지만 커지는 test set역시 존재한다.