2 Placing and Routing Standard Cell Designs

(continued)

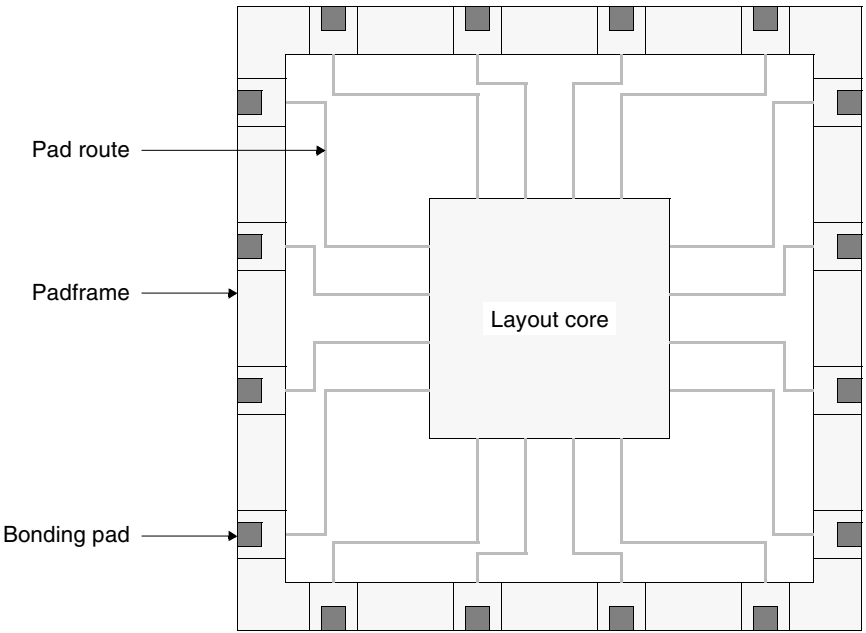
Introduction

L-Edit/ SPR (Standard Cell Place and Route) places and routes a design using a user-provided EDIF or TPR netlist and a standard cell source library as input. SPR includes three options:

- *Core place and route* generates a core cell using standard cells from a standard cell library. Parameters for standard cell core place and route can be specified in the dialog **SPR Core Setup** (page 2-44).
- *Padframe generation* creates a user-specified padframe with pad cells from the standard cell library. Parameters for padframe generation are specified in the dialog **SPR Padframe Setup** (page 2-68).
- *Pad routing* routes signals, including power and ground, between the layout core of a chip and its padframe. Parameters for pad routing are specified in the dialog **SPR Pad Route Setup** (page 2-81).

You can perform the three SPR operations in one step or separately. L-Edit can perform a pad route against a single pregenerated core cell or a set of core cells and/or other customized building blocks, as long as the layout core of the chip is composed in one cell. Similarly, L-Edit can perform a pad route against a pregenerated padframe, which can also be built in any manner, as long as it forms a single padframe cell and conforms to SPR constraints.

Running all three operations produces a completed design like the following:



Chip with core, padframe, and pad routing.

Required Files

To run SPR, the following files are required:

- A design file (**.tdb**).
- A netlist file (**.tpr**, **.edf**, **.edn**, or **.edi**). This file contains a textual description of your schematic design and identifies the cells that are required from the standard cell library file.
- A standard cell library such as **morbn20d.tdb**, which contains the standard cells and pad cells required for your design. This particular file is a component of the Tanner Research standard cell library *SCMOSLib*. You can also create your own standard cell library.

Note: To place and route a design, you must first define (in your design file) a technology setup appropriate to your standard cell library. If you start L-Edit with an empty design file, use **File > New** to copy the technology setup from an existing TDB file or a technology file such as **morbn20.tdb** before setting up or running SPR. Alternatively, you can simply open a design file that already contains the correct technology setup.

SPR Process Overview

To place and route a design using L-Edit/ SPR, you will typically perform the following steps:

- ☑ Create a schematic representation of your design.
- ☑ Export the schematic as a netlist in either EDIF or TPR format. L-Edit supports EDIF version 2 0 0, EDIF level 0, keywordLevel 0, viewType NETLIST.
- ☑ Launch L-Edit. Use **File > New** to create your design file (layout file). Import the design information (technology setup) from your cell library into the design file by entering your cell library file name in the **Copy TDB setup from file** field of the **New File** dialog.
- ☑ Use **File > Save** to label and save your initial design file with an appropriate name.
- ☑ Choose **Tools > SPR > Setup**. In the **SPR Setup** dialog (see SPR Setup on page 2-36) specify the names of the standard cell library file and the netlist file. Also specify the power and ground node and port names as used in your schematic. (These names must match the names of the power and ground ports in the standard cells.)

☑ Click the **Initialize Setup** button. This will read the netlist and initialize the following setup dialogs with netlist information: critical nets, I/O signals, padframe layout, and core and padframe signals of the pad route.

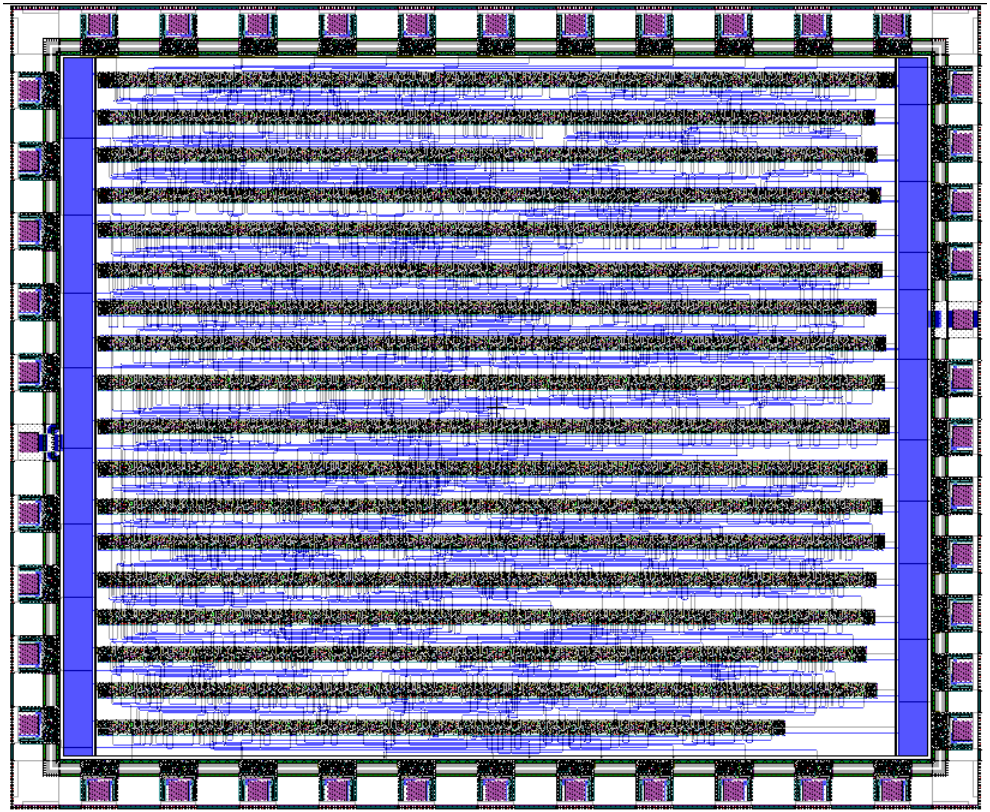
☑ Click the buttons **Core Setup**, **Padframe Setup**, and **Pad Route Setup**, respectively, to specify the remaining setup parameters for core placement and routing (see SPR Core Setup on page 2-44), padframe generation (see SPR Padframe Setup on page 2-68), and pad routing (see SPR Pad Route Setup on page 2-81).

☑ Choose **Tools > SPR > Place and Route**. Select the appropriate option (**Core place and route**, **Padframe generation**, or **Pad route**) singly or in any combination. Depending on your standard cell design, uncheck or check the **Global input signal routing** option. (Global input signal routing requires special buses to be available in your standard cells, see Global Input Signal Routing (Clock Routing) on page 2-32 for further details). Decide on your core configuration. For example, select **Square** if you want to obtain a square core shape. Check or uncheck the placement and routing optimization options. Specify the output options—for example, whether you want to label nodes with ports (to support node recognition during extraction) or whether you want to generate files containing nodal capacitances and SDF information.

☑ Click the **Run** button. Depending on your selected options, SPR will generate up to three new cells: a core cell, a padframe cell, and/or a chip cell (which contains the core, the padframe and the padroute). If these cells already exist in your design file, SPR will prompt you before overwriting them.

☑ When processing is complete, SPR will output an **SPR Complete** dialog providing summary statistical information for your design. (You can use **Tools > SPR > Summary** at any time to display a text file with further details.)

☑ Click the **OK** button in the summary dialog to display the completed design. The example shown below includes 990 standard cells (3,510 gates). On a 450 MHz Pentium II PC with 128 MB RAM, using both placement and routing optimization, SPR can generate this design in less than ten minutes.



☑ Confirm that the dimensions of the core and/or padframe fall within the size limitation imposed by your vendor. If not, you need to re-run SPR with either a different core configuration or increased placement and routing optimization (see Placement Optimization on page 2-103).

☑ Verify the design using L-Edit/DRC (see Checking Design Rules on page 3-10) and L-Edit/Extract (see Running the Extractor on page 3-97).

☑ Save the design in GDSII format and send it to your vendor for fabrication.

Design Tips

If you use an EDIF netlist and your netlist cell and/or port names differ from the names used in the standard cell library, use the **Mapping Table** button on the **SPR Setup** dialog (see Mapping Table on page 2-39) to generate a mapping table that allows you to assign the correlating names. SPR will use this mapping information when it discovers a discrepancy between a cell or port name in your netlist and your cell library.

Before running SPR on a new layout, use the **Initialize Setup** button (see Initializing Setup on page 2-43) to automatically enter pad-related information (for example, I/O signal configuration) from your netlist into the setup dialogs. SPR will only refer to the netlist if a dialog is empty. In this case, L-Edit will automatically fill the dialog fields with the netlist information.

We recommend that new users first generate a core separately. The dialogs that require I/O signal information (**SPR Core Setup—I/O Signals**) can be filled out either manually or, if pads or I/O signals are available in the netlist, initialized with the netlist information using the **Initialize Setup** feature. The padframe should be created next, taking the core dimensions into consideration. Finally, you can generate the new chip cell by performing a pad route using the core and padframe cells.

Core Generation and Pad Routing

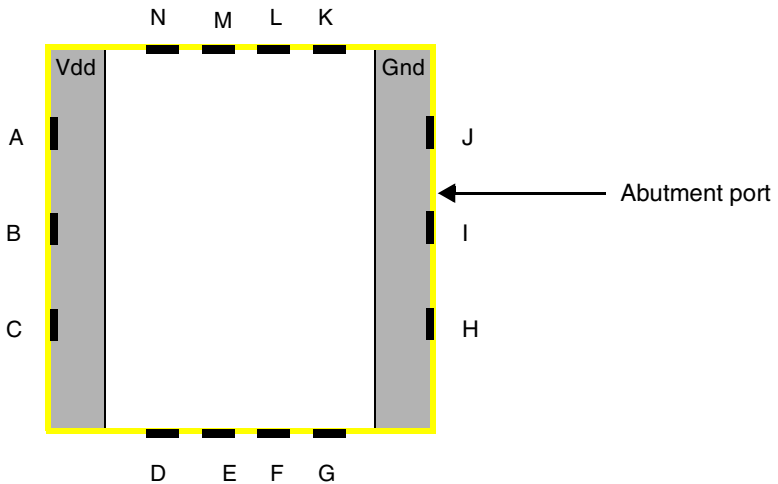
In pad routing, L-Edit routes signals only between the outer edge of the core and the inner edge of the padframe. Therefore, the core's position and dimensions are critical, but its internal geometry is not.

L-Edit determines the core's position by searching for an abutment port, which defines the edges of the core cell. The program creates the abutment port on the layer defined as the Icon layer. To define the Icon layer, choose **Setup > Special Layers**. For further information, see Special Layers on page 1-182.

The core and pad routing must adhere to the following constraints:

- The core must contain signal ports along its edges for every signal going to the padframe.
- Signal ports on the core and padframe must be ordered such that no signal running between core and padframe crosses over another signal, except for power and ground.
- However, signals may cross power or ground rails only if the materials used for routing are different (for example, *Metal2* for I/O signals and *Metal1* for power and ground).
- Power and ground lines are of the same material and may not cross.

The following figure illustrates the placement of signal ports along the core.



Core with abutment port and signal ports (A - N).

The pad router can only route a single core to the padframe. To use several core cells, you must create a new cell, instance each core cell, manually wire the instances together and finally surround the contents of this new cell with an abutment port and signal ports as described above. L-Edit then treats this new cell as a “single” core for the purposes of pad routing. You specify the name of

this newly created core cell and other necessary information in the dialogs **SPR Core Setup–General** (page 2-45) and **SPR Pad Route Setup–General** (page 2-84).

Multiple core cells can also be placed and routed using the L-Edit/ BPR feature (see the chapter Placing and Routing Block Designs on page 2-144.)

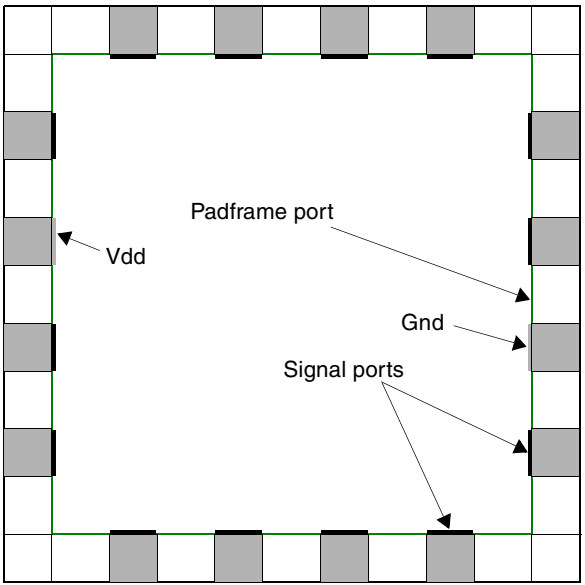
A netlist is not required if you perform a separate pad route with pregenerated core and padframe cells.

Padframe Generation and Pad Routing

In padframe routing, L-Edit routes signals only as far as the inner edge of the padframe. Therefore, the padframe's position and dimensions are critical, but its internal geometry is not. To indicate the region in which the core may be placed, L-Edit places a rectangular padframe port on the inner edge of the padframe.

For each signal going to the core, the padframe must contain one signal port along its inner edge. Signal ports for each signal going to the core must be placed on the padframe in the same order and on the same side as the signal ports around the core cell. These ports may be at the top level (in the padframe cell itself) or they may be one level lower in the hierarchy (in a pad cell instanced by the padframe). Power and ground pads must be on different sides of the padframe. L-Edit cannot route directly between the pads on the padframe—it can only route between the padframe and the core.

The following illustration shows a padframe with ports for signals, power, and ground.



Padframe with ports for signals, power, and ground. The padframe port defines the inner edge of the padframe.

A padframe can be generated using two methods:

Generating a Padframe from a Netlist with Pad Cells

- ☑ If the netlist contains pad cells, use the **Initialize Setup** button to automatically include pad cell *instance* names and their location in the **SPR Padframe Setup—Layout** dialog.
- ☑ Fill out the remaining input fields, like padframe size and padframe cell name. In the **SPR Setup** dialog, provide the names of the cell library that contains the pad cells and the appropriate netlist.
- ☑ Run SPR with **Padframe generation** turned on.

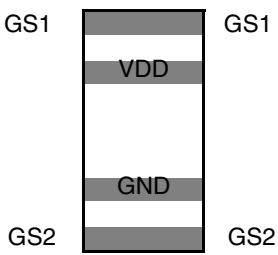
Generating a Padframe Without a Netlist or Without with Pad Cells

- ☑ If the netlist does not contain pad cells or if no netlist is available, manually input pad *cell* names and their location in the **SPR Padframe Setup—Layout** dialog.
- ☑ Fill out the remaining input fields, like padframe size and padframe cell name.
- ☑ In the **SPR Setup** dialog, provide the name of the cell library that contains the pad cells and leave the netlist input field blank.
- ☑ Run SPR with **Padframe generation** turned on.

Global Input Signal Routing (Clock Routing)

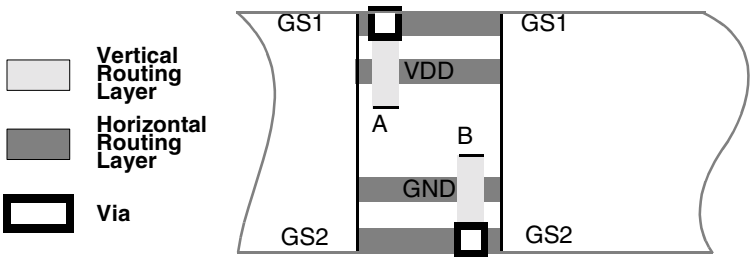
Global input signal routing is used to route as many as two I/O signals, such as clock nets, independently from other signals.

For global input signal routing, standard cells must contain two global signal buses, with four global signal ports, placed above and below the power and ground buses The following illustration shows a standard cell (top view) with two global signal buses. **GS1** and **GS2** are global signal ports of this standard cell.



Standard cell (top view) with two global signal buses.
GS1 and **GS2** are global signal ports of this standard cell.

During core routing, L-Edit connects signal ports belonging to global signal nets (labeled **A** and **B** in the illustration below) to the dedicated global signal bus.

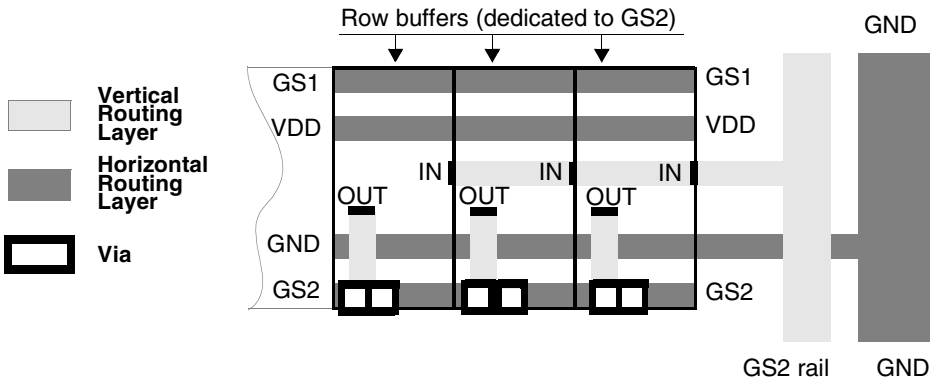


Internal signal ports of the two global signal nets connected with the dedicated global signal buses.

After placement, L-Edit adds buffer cells to both ends of the standard cell rows. L-Edit calculates the number of buffer cells required for each row by dividing the number of standard cells connected to the global signal nets by the driving force, which the user specifies in the dialog **SPR Core Setup–Global Signals** (page 2-59).

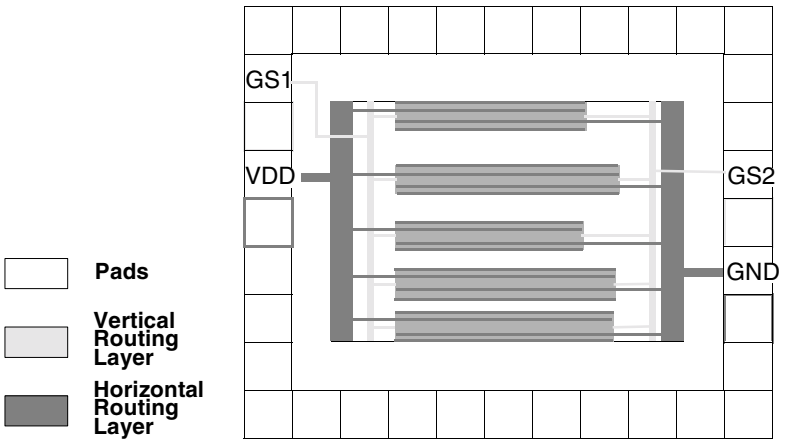
Buffer cells are dedicated to one of the two global signal buses. Each buffer cell contains an **IN** port that is accessible from the side and placed on the vertical layer. The **IN** port of the outermost buffer cell is connected with the vertical global signal rail on this side.

The vertical global signal rail is placed on the vertical layer, inside of the vertical power rail. It is twice as wide as the IN port of the buffer cell(s) on this side.



Buffer cells (right side) and their connection with the global signal rail GS2

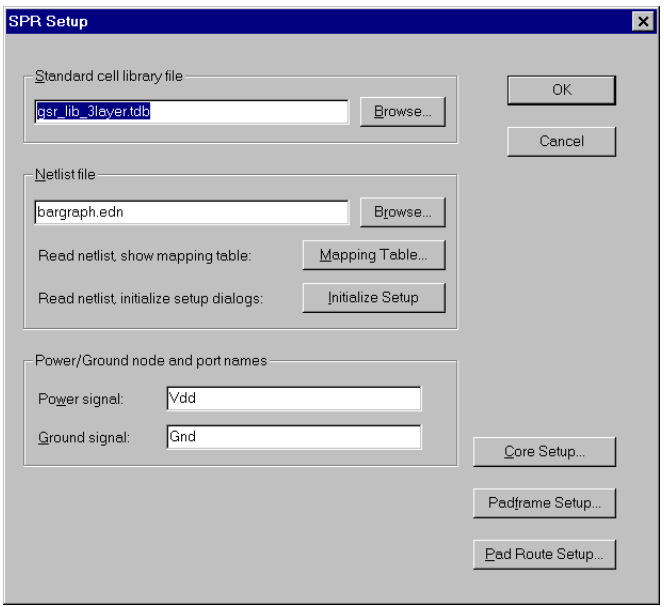
Pad routing connects the vertical global signal rails to the appropriate ports on the padframe. Layer assignment for global signal pad routing is equivalent to the layer assignment for regular I/O signals leaving the core. The pads of the global signal nets have to be located either on the left (for the left global signal rail) or on the right side (for the right global signal rail).



Global input signal and power routing

SPR Setup

Before running SPR, you must set the appropriate options. Use **Tools > SPR > Setup** to open the **SPR Setup** dialog.



Specify the following:

Standard cell library file

File containing the standard cells and pad cells that L-Edit uses to generate your design. If your design file already contains the required cells, you may use it instead of the standard cell library. Enter the full pathname if the file is not in the current L-Edit directory.

Netlist file

File containing a textual description of your schematic design, which identifies the cells required from the standard cell library. This file is always required when you place and route a core. It is optional when you perform only pad routing or padframe generation.

Two types of netlist files are supported:

- TPR—Tanner Place and Route Format, produced by S-Edit
- EDIF—EDIF version 2 0 0, EDIF level 0, keywordLevel 0, viewType NETLIST. (Acceptable filename extensions are **.edf**, **.edn**, and **.edi**.)

	A SPICE netlist can also be used if it is first converted to TPR with a conversion tool such as NetTran.
Mapping Table	Accesses the dialog **Mapping Table** (page 2-39) to map cell and port names between the EDIF netlist and the standard cell library.
Initialize Setup	Reads pad-related information from the netlist and completes the fields in the setup dialogs that specify critical nets, padframe layout, core signals, and padframe signals. If these fields already contain information, SPR will prompt you to keep or overwrite the values. (See Initializing Setup on page 2-43.)
Power signal	Schematic netlist name of the power node. The power signal must have the same name as the power port in the standard cells.
Ground signal	Schematic netlist name of the ground node. The ground signal must have the same name as the ground port in the standard cells.

When you have typed the correct information in these fields, click the appropriate button—**Core setup**, which opens **SPR Core Setup–General** (page 2-45), **Padframe setup**, which opens **SPR Padframe Setup–General** (page

2-69), or **Pad route setup**, which opens **SPR Pad Route Setup–General** (page 2-84)—to continue SPR setup.

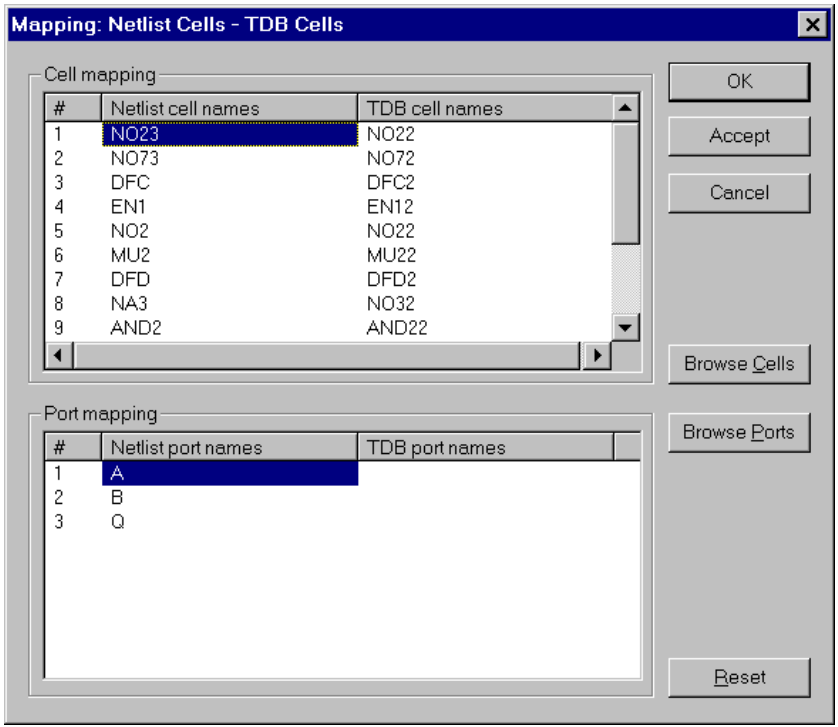
Each of these dialogs contains a **Reset** button, which resets all fields and options to the values they held when you accessed the dialog.

If you are using an EDIF netlist and it has different cell and port names than those used in the cell library, you must map these names correctly. For additional information on this topic, see the section Mapping Table, below.

Mapping Table

L-Edit invokes the **Mapping Table** dialog while processing the EDIF netlist whenever it finds a discrepancy between the cell or port names. You can also click **Mapping Table** in the **SPR Setup** dialog to directly generate a mapping table before running SPR.

Mapping information is saved in the design file. If you change the netlist (within the same design file), the mapping table will display values for previously mapped cells and ports.


Mapping: Netlist Cells - TDB Cells
Cell mapping
Netlist cell names TDB cell names
1 NO23 NO22
2 NO73 NO72
3 DFC DFC2
4 EN1 EN12
5 NO2 NO22
6 MU2 MU22
7 DFD DFD2
8 NA3 NO32
9 AND2 AND22
Port mapping
Netlist port names TDB port names
1 A
2 B
3 Q
OK
Accept
Cancel
Browse Cells
Browse Ports
Reset

Use this dialog to define the correspondence between:

- Cells in the EDIF netlist and cells in the standard cell library file.
- Ports in the EDIF netlist and ports in the standard cell library file, within individual cells.

  Port mapping is only required if a port name discrepancy occurs. However, if you map one port in an individual cell, you must map all ports in that cell.

  If your cell interface in the EDIF file contains ports which are not connected in your design, you can label them as "not used" during the mapping process.

To map a cell, click the netlist or TDB cell name, or **Browse Cells**. To map a port, click the netlist or TDB port name, or **Browse Ports**. L-Edit displays a dialog in which you select the correct cell or port.

Cell mapping

A numbered list of cells named in the EDIF netlist.

- **Netlist cell names**—list of cells named in the EDIF netlist.
- **TDB cell names**—list of cells contained in the standard cell library file.

To map a cell, click on a cell name, or **Browse Cells**. L-Edit displays a dialog where you can select the correct cell.

Port mapping

A numbered list of ports named in the specified cell in the EDIF netlist.

- **Netlist port names**—list of ports named in the EDIF netlist.
- **TDB port names**—list of ports contained in the standard cell library file.

To map a port, click on the netlist or TDB port name or **Browse Ports**. L-Edit displays a dialog in which you select the correct port.

Browse Cells

Opens a dialog containing a list of cells contained in the specified standard cell library file.

Browse Ports

Opens a dialog containing a list of ports for the specified cell in the specified standard cell library file.

Accept

Saves mapping input and closes the **Mapping Table** dialog.

OK	Saves mapping input, checks that all EDIF cells and ports are mapped, and closes the **Mapping Table** dialog.

Initializing Setup

The **Initialize Setup** function keeps the setup dialogs and the netlist synchronized. You should use it when you create a new design and whenever the netlist is changed or updated. When you click the **Initialize Setup** button, SPR updates the following dialog values with values from the netlist:

- Critical nets in **SPR Core Setup—Placement**, if any
- I/O signal specifications in **SPR Core Setup—I/O Signals**
- Pad route specifications in **SPR Pad Route Setup—Padframe Signals** and **SPR Pad Route Setup—Core Signals**
- Padframe specifications in **SPR Padframe Setup—Layout**

You cannot cancel or undo this operation.

SPR Core Setup

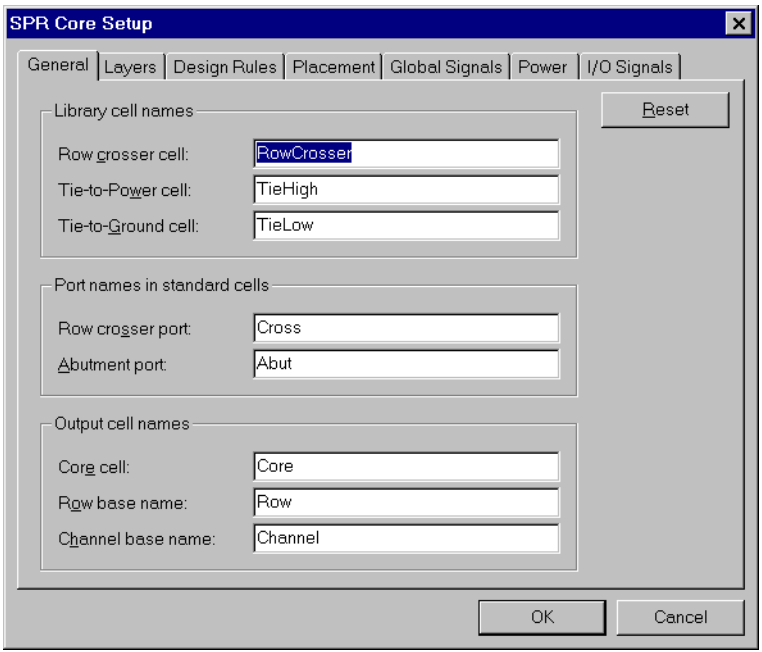
In this dialog, you define the parameters L-Edit will use to generate your design core. The dialog consists of seven tabs:

- **General**
- **Layers**
- **Design Rules**
- **Placement**
- **Global Signals**
- **Power**
- **I/O Signals**

Each tab contains a **Reset** button, which resets all fields and options to the values they held when you accessed the dialog.

SPR Core Setup–General

The **General** tab contains fields used to define the library cells, standard cell ports, and output cells used in generating the core.



L-Edit requires three special standard cells in a library set: a *row crosser cell*, the *tie-to-power* cell, and the *tie-to-ground* cell. They are used for node connections only and are not included in the netlist.

Specify the following:

Library cell names

Row crosser cell, **Tie-to-Power cell**, and **Tie-to-Ground cell**, as they are named in the standard cell library. These cells must be part of the standard cell library. For detailed design information on these cells, see Special Standard Cells on page 2-130.

A **row crosser cell** contains one row cross port and is placed to make up a cross-row pass to route wires across a standard cell.

The **tie-to-power cell** is needed where a standard cell has a pin directly tied to Vdd.

The **tie-to-ground cell** is needed where a standard cell has a pin directly tied to Gnd.

Port names in standard cells

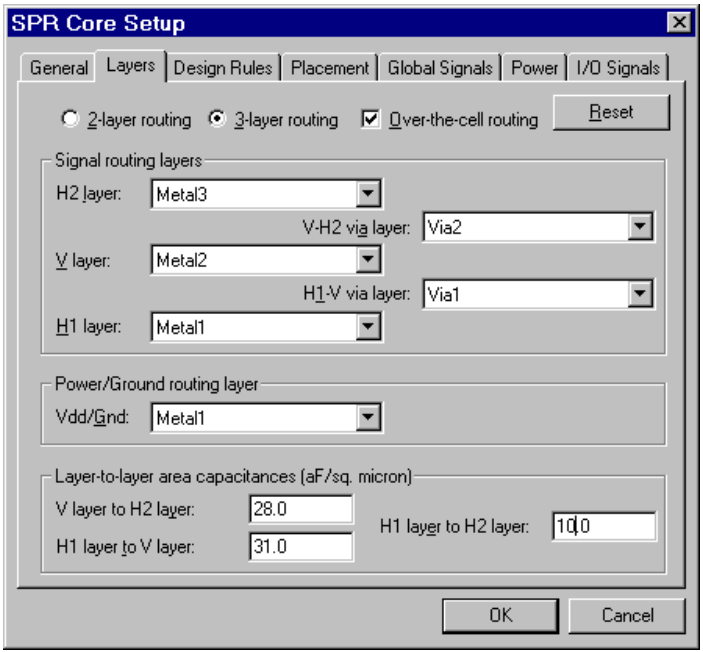
Names of the **Row crosser port** and **Abutment port** as they are named in the standard cell library.

	A **row crosser port** defines crossing paths to route wires across a standard cell row. This port must be placed on the vertical routing layer. The **abutment port** surrounds the standard cell and defines its edges.
Core cell	The name of the core cell to be created.
Row base name	The base name of the row cells to be created.
Channel base name	The base name of the channel cells to be created.

SPR Core Setup–Layers

The **Layers** tab contains fields that define the layers L-Edit will use to route the core. You use it to specify whether two or three layers are used for routing. If you use three layers, you can also select over-the-cell (OTC) routing.

This tab also contains fields for the layer-to-layer capacitance between routing layers. These capacitance values are used for extracting nodal capacitances, which are written to the CAP file (see Nodal Capacitance Files (CAP) on page 2-107).



Click on **2-layer routing** or **3-layer routing** to choose a routing configuration. If you use three-layer routing, **Over-the-cell routing** will be an available option.

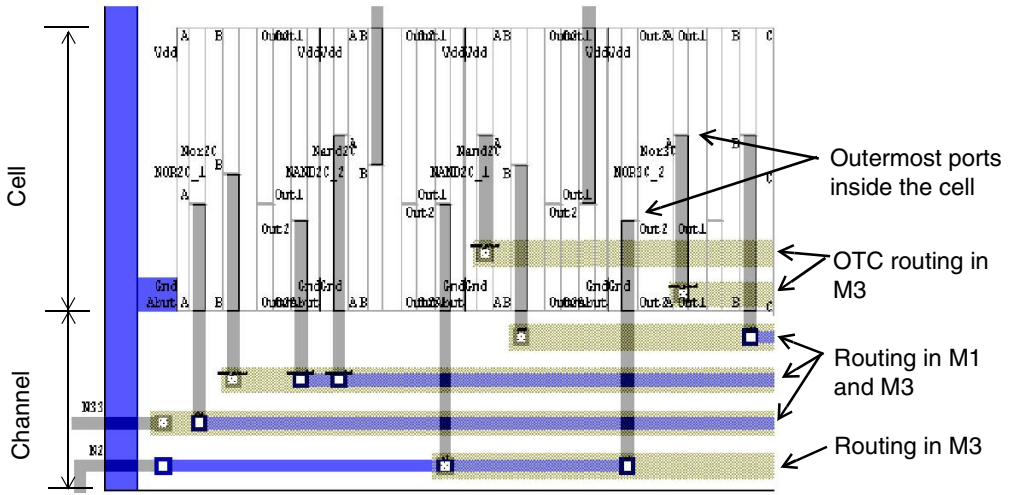
Specify the following:

Signal routing layers	Specify the routing layers and the via layer(s) to be used for channel routing.
Power/Ground routing layers	Specify the routing layers for power and ground. This assignment must be consistent with the layer assignment of the power and ground buses within the standard cells (usually in the H1 layer).
Layer-to-layer area capacitances	Enter the layer-to-layer capacitances between your routing layers (in aF/sq. micron). These values are only required if the **Write CAP file** option in the **Standard Cell Place and Route** dialog is checked.

Over-the-Cell Routing

Over-the-cell (OTC) routing uses tracks above the cells, in the H2 layer, between the channel edge and the “outermost” port inside the cells, for routing.

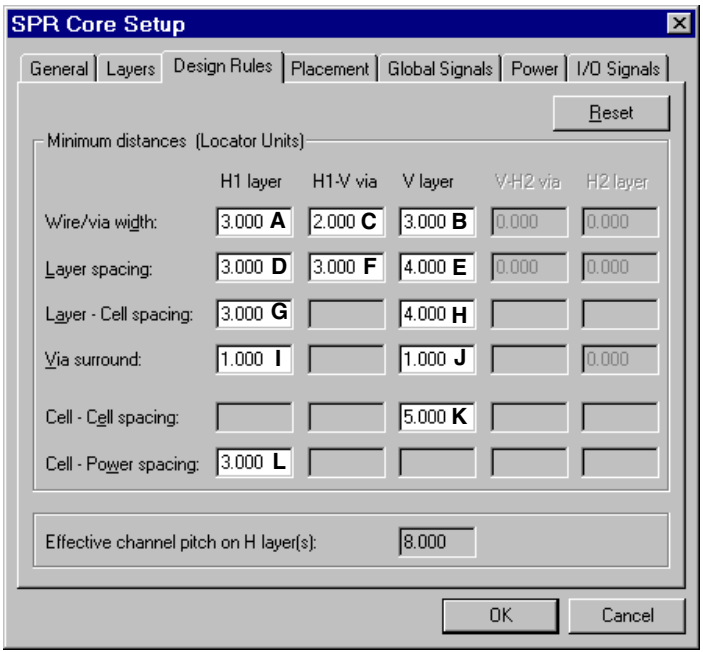
A special algorithm sorts net segments to utilize these tracks as effectively as possible. The number of OTC tracks depends directly on how you have placed your ports inside the standard cells. If all ports are lined up in the center of the standard cell, a maximum number of OTC tracks can be utilized.



Layout example of three metal layers with OTC routing.

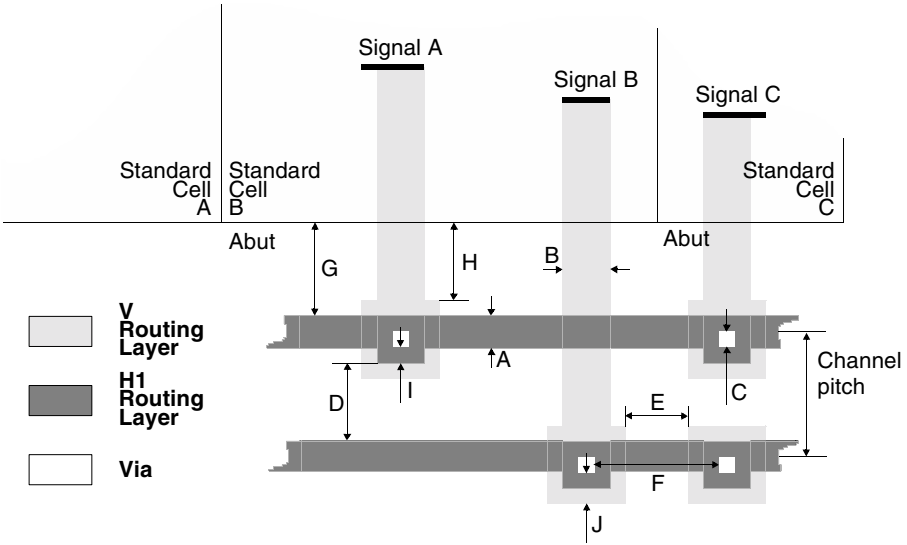
SPR Core Setup–Design Rules

Use the **Design Rules** tab to specify the design rules L-Edit must follow to route the core in conformance with the technology used to fabricate your design.

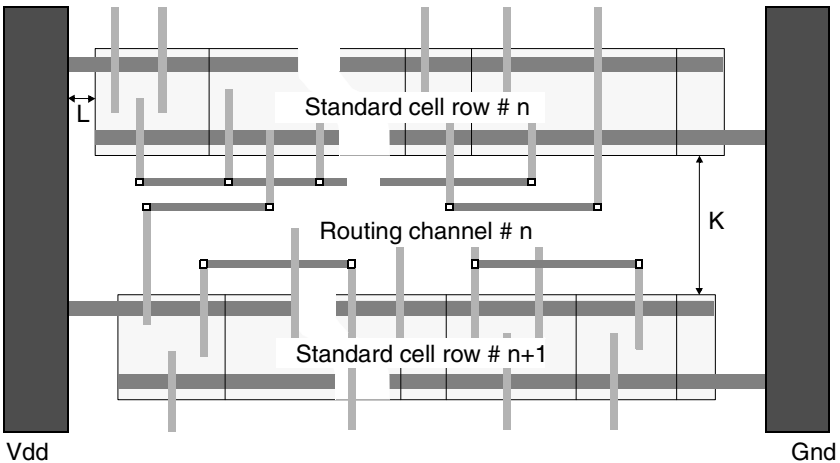


The figures SPR widths, spaces, and via surrounds in 2-layer routing on page 2-53 and Minimum cell-cell and cell-power spaces on page 2-54 illustrate the application of design rules in 2-layer routing. The letters in the dialog fields provide a key for the labels in the illustrations and the values they represent.

This tab also displays the effective channel pitch on the H layer(s) in a read-only field. (The channel pitch is the distance between the centerlines of two neighboring horizontal routing segments.) This value is internally calculated according to your design rules.



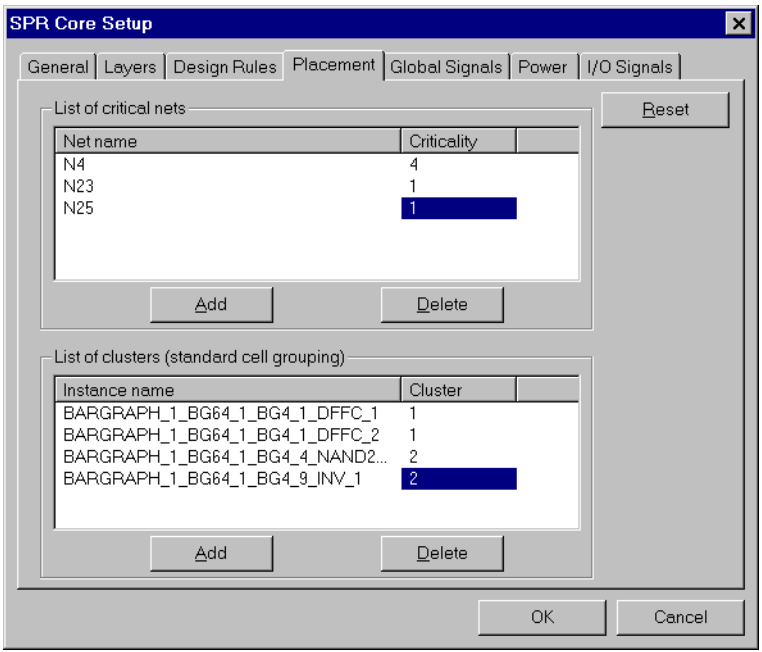
SPR widths, spaces, and via surrounds in 2-layer routing



Minimum cell-cell and cell-power spaces

SPR Core Setup–Placement

This tab contains options for controlling the outcome of the automatic placer.



Specify the following options:

Net Name	Enter a net name.
Criticality	Enter an integer criticality value. A positive integer value denotes a higher priority net, a negative integer value reduces the importance of the net during placement. See Assigning Net Criticality on page 2-57 for further details. To add a new critical net, click **Add**. To delete a critical net, select it and click **Delete**.
Instance Name	Instance name of a standard cell to be included in a cluster.
Cluster	Enter an integer value. All cell instances with the same cluster number are placed within one cluster. See Clustering Standard Cells on page 2-58 for further details. To add a new cell instance to a cluster, click **Add**. To delete a cell instance from a cluster, highlight the instance name and click **Delete**.

Assigning Net Criticality

Nets that are critical in your layout can be specified in the **List of critical nets**. Criticality is expressed as an integer value that may be positive or negative. The higher the criticality value, the higher the priority of the net during placement. (A positive value net is given a higher priority, a negative value net is given a lower priority during placement.) The value for any net that is not specified in this table is zero.

The consideration of net criticality in L-Edit/SPR is based on two assumptions:

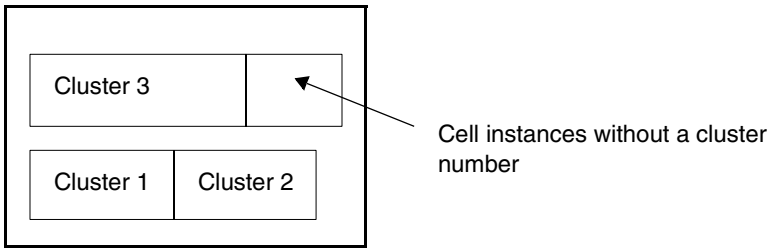
- The numerical value of the criticality describes the relative importance of a net compared to others. For example, if the criticality of net A is twice the criticality assigned to net B, then the placer considers it as twice as important to reduce the length of net A compared to net B.
- The critical values are scaled internally according to the largest value that has been entered, with the largest value assigned to a fixed internal value. Hence, if net A is the only net with an assigned criticality, than any criticality value greater than zero for this net would lead to the same result.

Net criticality can be entered either by using the EDIF netlist attribute *criticality*, or directly in the **SPR Core Setup—Placement** dialog. If SPR finds criticality values in this dialog, it will ignore any criticality values found in the netlist. To transfer criticality values from the netlist into this dialog, use the **Initialize Setup** button (see Initializing Setup on page 2-43).

Clustering Standard Cells

The **List of clusters** allows you to group standard cells together. All cell instances assigned the same cluster number are placed side by side, from left to right, in the order in which they appear in this table. Cell clusters cannot be "broken"—they must fit on one row. Note that row crossers might be inserted between two cells within one cluster.

Note: If you turn off placement optimization, cell clustering can also be used to place your cells in a specific sequence. SPR always places cell instances from left to right inside a cluster according to their sequence in the list of clusters. Without placement optimization, clusters are placed according to their number, starting with the lowest row, from left to right (see the figure on the following page). Cell instances that are not included in any cluster are placed subsequently, in the sequence of the netlist.

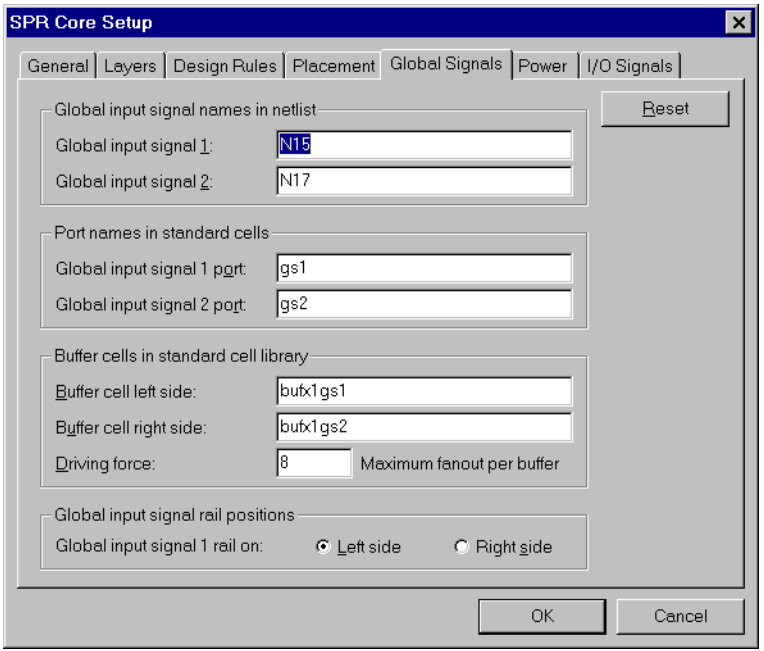


Core with two rows containing clusters that are placed with placement optimization turned off.

SPR Core Setup–Global Signals

This tab contains options used to route global input signals. If you do not check the option **Global input signal routing** in the **Standard Cell Place and Route**

dialog (see Standard Cell Place and Route on page 2-95), you can ignore this dialog.



Specify the following options:

Global input signal names in netlist

Specify one or two signals for global routing.

Ports names in standard cell

Names of the bus ports in the standard cells that will be used for each global input signal. This port name assignment subsequently defines the bus, rail, and pad positions used to route each global signal net (see Global Input Signal Routing (Clock Routing) on page 2-32).

Buffer cells in standard cell library

Names of the buffer cells to be placed on the left and right side of the standard cell rows. If your design has only one global input signal, specify one buffer cell on the same side as the global input signal rail.

Driving force

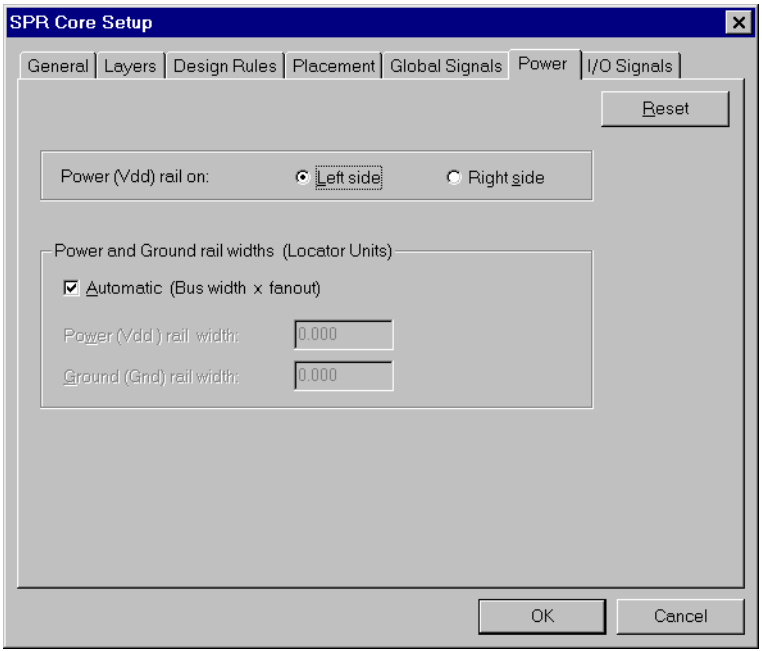
Driving force is the driving capability (fanout) of one buffer cell—the maximum number of standard cells that can be driven by this buffer cell. The value must be greater than or equal to 1. L-Edit calculates the number of buffer cells to place on the edge of each standard cell row by dividing the number of driven cells in the row by this value.

Global input signal 1 rail on Click the option button for whether the **Global input signal 1 rail** should be on the **Left side** or the **Right side** of the core. L-Edit will place the rail for **Global input signal 2** on the opposite side.

Note: The assignment of global signal bus ports to each global signal net determines the assignment of these nets to either the upper or lower global signal bus. Because buffer cells are specifically connected to either the upper or lower global signal bus, this port assignment also determines which global signal net the left and right global signal rails represent.

SPR Core Setup–Power

This tab contains options for the placement and width of power and ground rails.



Specify the following options:

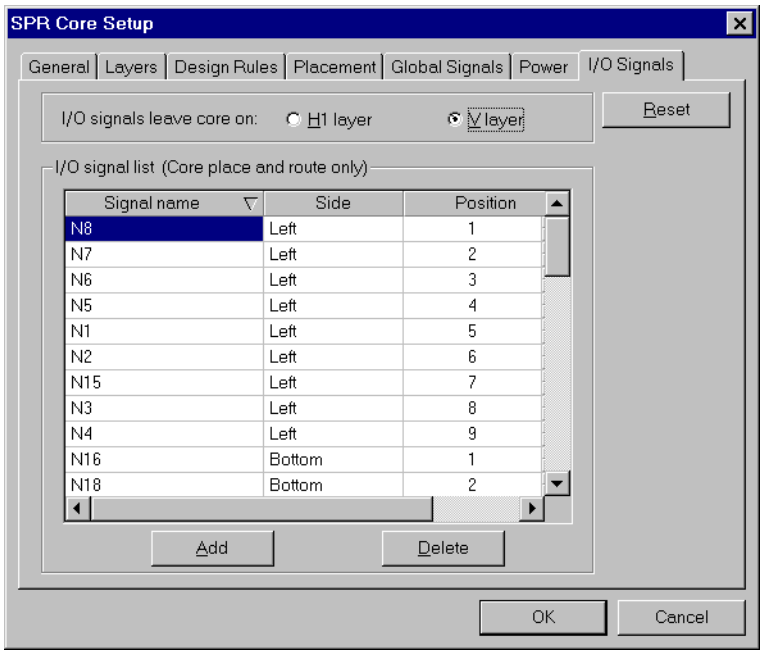
Power (Vdd) rail on:	Power and ground rails can be placed either on the left or right side of the core cell. This choice will be overwritten by the location of the power and ground pads if the padframe is generated simultaneously and a conflict is detected.
Automatic (Bus width x fanout)	Check here if you want your power and ground rail widths to be calculated internally by SPR. In this case, the width is determined by multiplying the bus width (in the rows) with the number of rows to be driven.
Power (Vdd) rail width	The width of the Vdd rail in locator units (if **Automatic** is unchecked).
Ground (Gdd) rail width	The width of the Gnd rail in locator units (if **Automatic** is unchecked).

SPR Core Setup–I/O Signals

This tab contains options for the location of input/output signals around the core. **Initialize Setup** will complete this dialog automatically if your netlist contains

pad connections or interface I/O signals (for EDIF netlists only; see EDIF Files on page 2-326).

You do not fill out the **I/O signal list** if you perform core place and route in conjunction with pad routing and padframe generation.



Specify the following options:

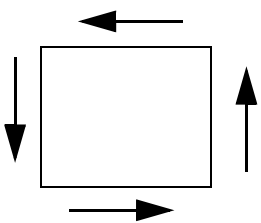
I/O signals leave core on

Layer (H1 or V) on which I/O signals will leave the core. Options are **H1 layer** and **V layer**. If you perform pad routing, this layer must be identical to the pad routing layer for I/O signals (see SPR Pad Route Setup–Layers on page 2-85).

I/O signal list

Defines the name of each I/O signal, the side from which it exits, and its relative position on that side.

Use the **Position** value to specify the relative position of a signal on a given side proceeding counter-clockwise. The higher the value, the later a signal's position on a side. For each side, signals are ordered as follows:



Left:	top to bottom
Bottom:	left to right
Right:	bottom to top
Top:	right to left

Only the left and right core edges can be used for routing global input signals. It is also recommended that you do not use the uppermost and lowermost pads for global signals.

To add a signal to the list, click **Add**. A **New Signal** is highlighted and can be edited. The name of the signal must be the same as in the netlist. To delete a signal, highlight the signal in the list and click **Delete**.

SPR Padframe Setup

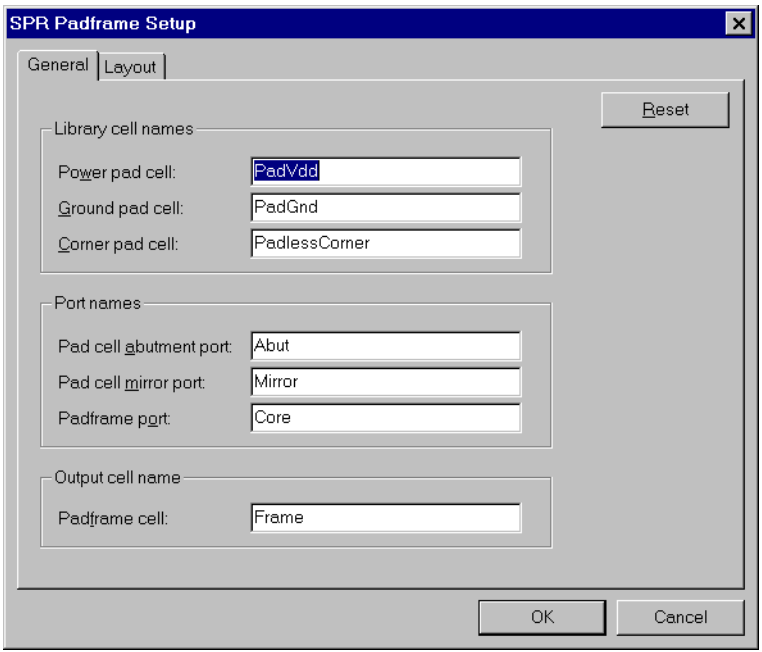
In padframe generation, L-Edit takes pad cells from the standard cell library, places them in a rectangular ring, and if required, connects them together. The exact size and shape of this padframe is determined by the *maximum* of (1) the configuration specifications of the core cell and (2) the actual size of the padframe after all specified pads have been placed abutting one another in their respective positions. The type of pad placed in each position depends on the name indicated in the setup procedure.

To set parameters for padframe generation, click **Padframe Setup** in the **SPR Setup** dialog. L-Edit will display the **SPR Padframe Setup** dialog.

The dialog consists of two tabs—**General** and **Layout**. Each tab contains a **Reset** button, which will reset all fields and options to the values they held when you accessed the tab.

SPR Padframe Setup–General

This tab contains fields used to specify the cells and ports in the standard cell library that L-Edit will use for padframe generation.



Specify the following options:

Library cell names

Specify the name of the **Power pad cell**, the **Ground pad cell**, and the **Corner pad cell** to be drawn from the standard cell library.

Port names

Names of the ports used to define the dimensions, positions, and orientation of the pad cells and padframe. These include the following:

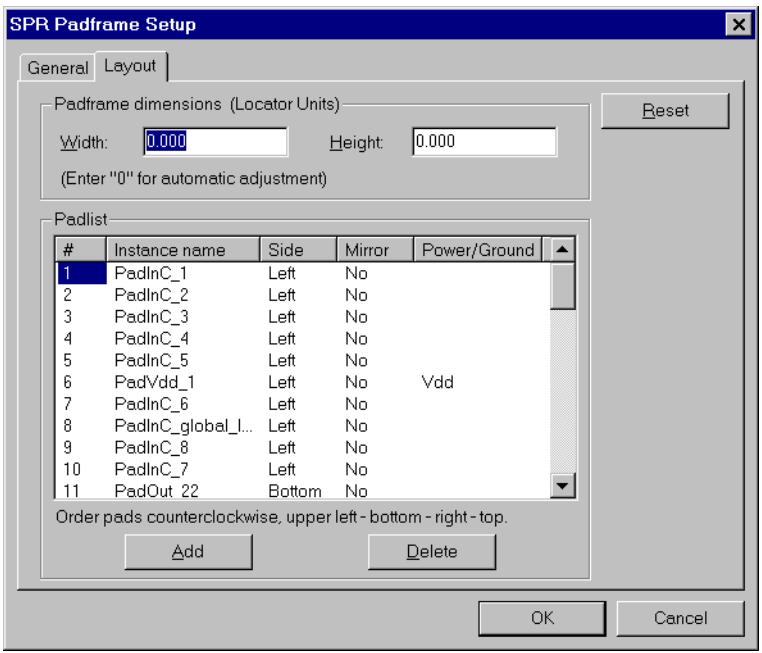
- **Pad cell abutment port**—enter the name of the port used to define the edge of each pad cell.
- **Pad cell mirror port**—enter the name of the port used in the standard cell library to designate mirror ports in pad cells (for additional information, see Mirror Ports on page 2-139). L-Edit will place pad cells with this port name in a special orientation.
- **Padframe port**—enter the name of the port used to define the inner edge of the padframe.

Output cell name

Specify the name of the generated **Padframe cell**.

SPR Padframe Setup–Layout

Use this tab to specify the padframe's size and the location of the pads, plus individual characteristics of each pad in the padframe. **Initialize Setup** will complete this dialog automatically if your netlist contains pad connections.



Specify the following:

Padframe dimensions (Locator Units)

Width and **Height** of the padframe. If you enter zero for any or both of the dimensions, L-Edit automatically determines the minimum size required.

The **Padlist** presents a numbered list of pads with their locations and attributes. Corner pads are not listed. If the padlist is empty, L-Edit will use the pad configuration in the netlist. The padlist contains the following columns:

#

The number of the pad in the padframe. L-Edit orders pads counterclockwise along each side according to this number.

Instance name

The name of the pad instance. The name of the pad must be the same as the instance name in the netlist file. Pad cell names can be entered if no netlist is provided. (Padframe generation only.) See Pad Cells on page 2-132 for naming conventions and restrictions.

To add an instance to the list, click **Add**. A **New Pad** is highlighted and can be edited. To delete a pad, highlight it by clicking any of its attributes and click **Delete**.

Side

The side of the padframe on which the pad is placed. Pads must be entered into the pad list in the order *left—bottom—right—top*.

Mirror

Select either **Yes** or **No**. When you enter **Yes** for a given pad, L-Edit mirrors the pad through its vertical axis—unless this mirroring will conflict with mirroring information present in the cell library. For additional information, see Mirroring on page 2-79.

Power/Ground

Enter **Vdd** and **Gnd** to designate particular pads as power and ground. Only one **Vdd** pad and one **Gnd** pad may be placed, and they must be on different sides.

If the design requires more than one power or ground pad in the padframe, list a "temporary" pad in your schematic or in the padframe setup. After padframe generation, edit the layout to remove the "temporary" pad and place a **Vdd** or **Gnd** pad in its place, making connections as required. (See SPR Padframe Setup on page 2-68.)

Adding Pads

L-Edit automatically places corner pads. If the padframe schematic contains fewer pads than the number required by the chip foundry for a complete padframe layout, you must complete the padframe by one of two methods:

- Adding placeholder pads at the appropriate locations in the padframe setup (for example, to have a total of 10 pads on each side of a 40-pin frame).
- Adding the required number of unconnected pad instances to the schematic, with module ports to specify their location.

Pad Naming and Ordering

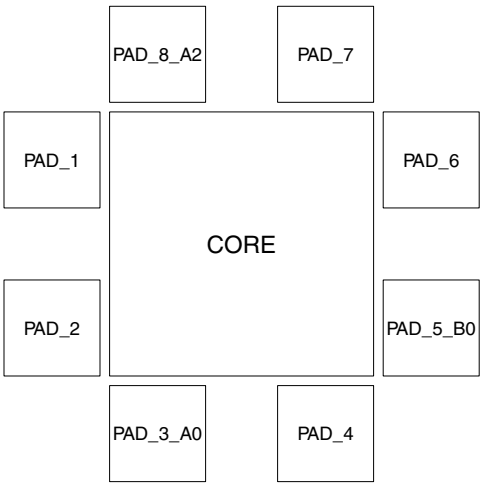
Pad names entered in the padlist must meet one of the following criteria:

- The name must be exactly the same (except for case) as the instance name in the netlist file. For example, if the pad instance name is **U21_3**, enter **U21_3** as the pad name.
- The name must match (except for case) the instance name in the netlist up to (but not including) the first occurrence of a **<** in the netlist instance name. For example, if the pad instance name is **U21<1<333**, enter **U21** as the pad name.
- The name must be exactly the same (except for case) as one of the pad cells in the standard cell library—for example, **OPad** or **VddPad**. Use this criterion when you only perform padframe generation; no netlist input is required in the **SPR Setup** dialog.

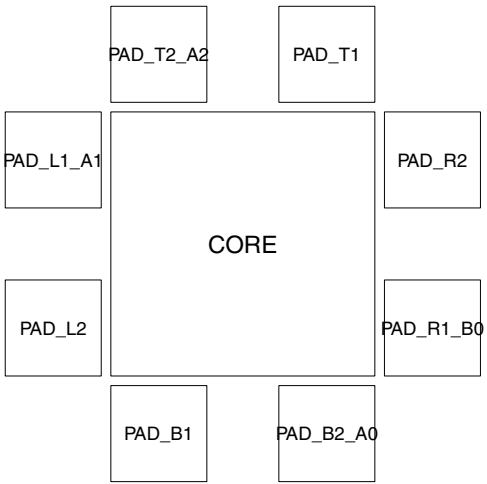
You can also specify pad information in the schematic (or directly in the netlist) by placing pads connected to the appropriate signals in the design. If the pads are to be in a specific order, then attach module ports to the **PAD** pins of each pad. (The **PAD** pin represents the location where a bonding wire will connect this signal to a pin on the chip.) These module port names must all be in one of the following formats. (In the following table, ***n*** is a number from 1 to the number of pads in the design, ***s*** is the first character of a side—**L** for left, **R** for right, and so on—and ***x*** is any string of characters.)

For information on defining pads in an EDIF netlist, see EDIF Files on page 2-326.

Format	*Examples*	*Results*
PAD_*n*	**PAD_1** **PAD_2**	The pads are placed in order. For example, **PAD_1** is placed in the top of the left side of the padframe, **PAD_2** just below it, and so on, traversing counterclockwise around the padframe. The more detailed form provides for port labeling. (See the figure Pad order—Example 1 on page 2-78.)
PAD_*n_x*	**PAD_1_CLOCK** **PAD_2_DATA**	
PAD_*sn*	**PAD_L1** **PAD_L2** **PAD_B1**	The pads are placed in counterclockwise order on the given side. For example, **PAD_L1** is placed at the top of the left side of the padframe, and **PAD_L2** just below it. **PAD_B1** is placed on the far left of the bottom of the padframe, and **PAD_B2** just to the right of it. The more detailed form provides for port labeling. (See the figure Pad order—Example 2 on page 2-79.)
PAD_*sn_x*	**PAD_L1_CLOCK** **PAD_T3_ENABLE**	



Pad order—Example 1



Pad order—Example 2

Mirroring

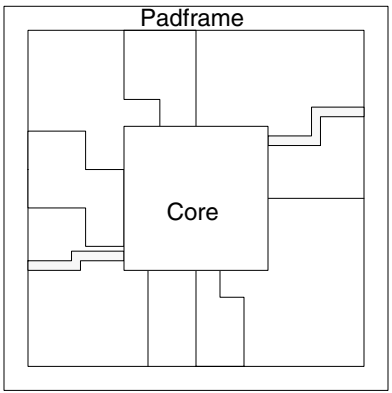
Mirroring is used to mirror pads at specific locations. Incorrect mirroring could cause your chip to malfunction. Standard cell libraries provided by Tanner EDA

contain information for automatic pad mirroring, if required. Where more specific mirroring information is needed, it is provided in the standard cell library file setup.

To use this information, use **File > Replace Setup**. Type the name of the standard cell library file in the **From file** field. In the **SPR** group, select only **Padframe setup**. (For placing mirroring information into your own pad cells, see Pad Cells on page 2-132.)

SPR Pad Route Setup

The L-Edit pad router is a two-layer router. It first routes the power bus on one layer, then the signals on another layer. For each side of the padframe, there is a one-to-one correspondence between “connected” signals on the padframe and “connected” signals on the core. In other words, the uppermost “connected” signal on the left side of the padframe is routed to the uppermost “connected” signal on the left side of the core, the next “connected” signal down on the left side of the padframe is routed to the next “connected” signal down on the left side of the core, and so on. Each side of the padframe must have the same number of “connected” signals as there are on the corresponding side of the core.



Pad router example

To set parameters for pad routing, click **Pad Route Setup** in the **SPR Setup** dialog. L-Edit will display the **SPR Pad Route Setup** dialog.

The dialog consists of five tabs:

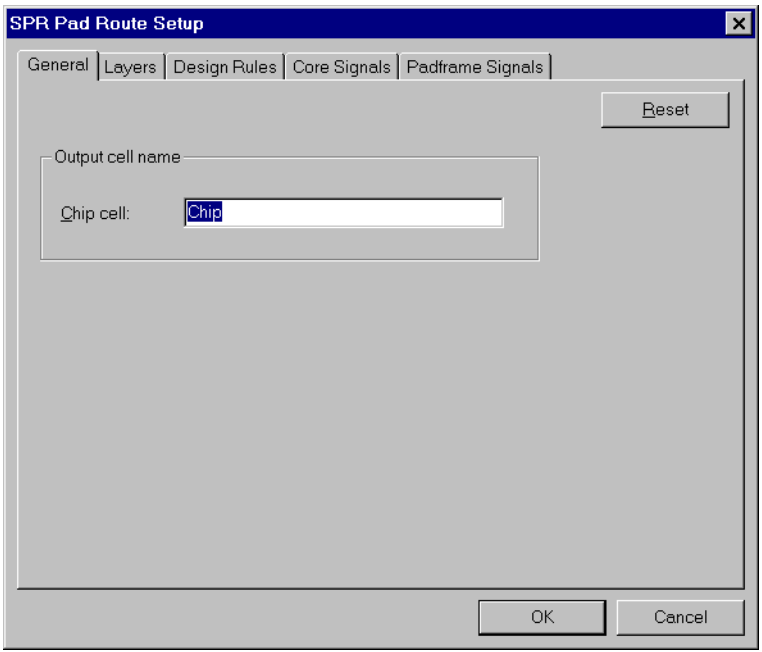
- **General**
- **Layers**
- **Design Rules**

- **Core Signals**
- **Padframe Signals**

Each tab contains a **Reset** button, which resets all fields and options to the values they held when you accessed the tab.

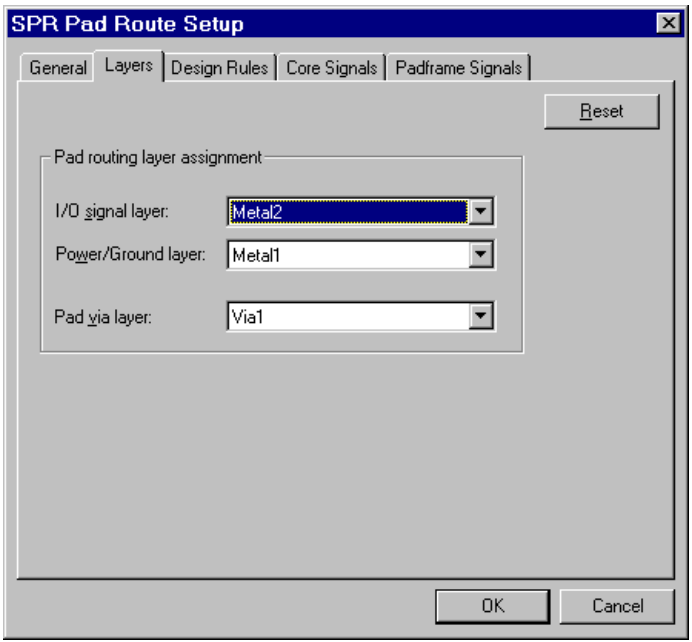
SPR Pad Route Setup–General

In the **General** tab, enter the name of the **Chip cell**. The chip cell contains the core and the padframe instance, and it is where the pad routing will be placed.



SPR Pad Route Setup–Layers

The **Layers** tab is used to specify pad routing layers for I/O signals, power/ground signals, and pad vias (if needed).



Specify the following options:

I/O signal layer

Layer on which I/O signals are routed. In pad routing, I/O signals must be assigned to the same layer as that specified in **SPR Core Setup–I/O Signals** (page 2-64).

Power/ground signals

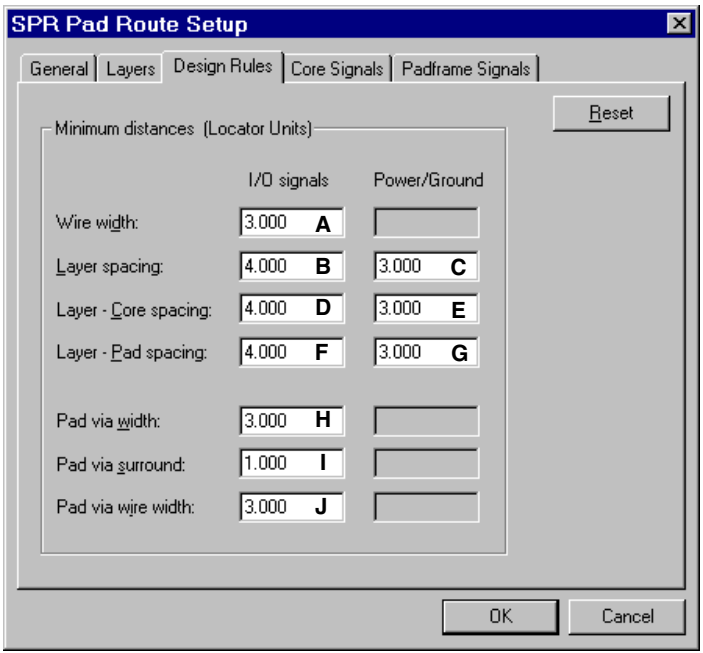
Layer on which power/ground signals are routed. These must be routed on a different layer than I/O signals.

Pad via layer

Layer on which pad vias are drawn. L-Edit inserts pad vias if the ports of *all* pad cells are placed on a layer other than the I/O signal layer.

SPR Pad Route Setup–Design Rules

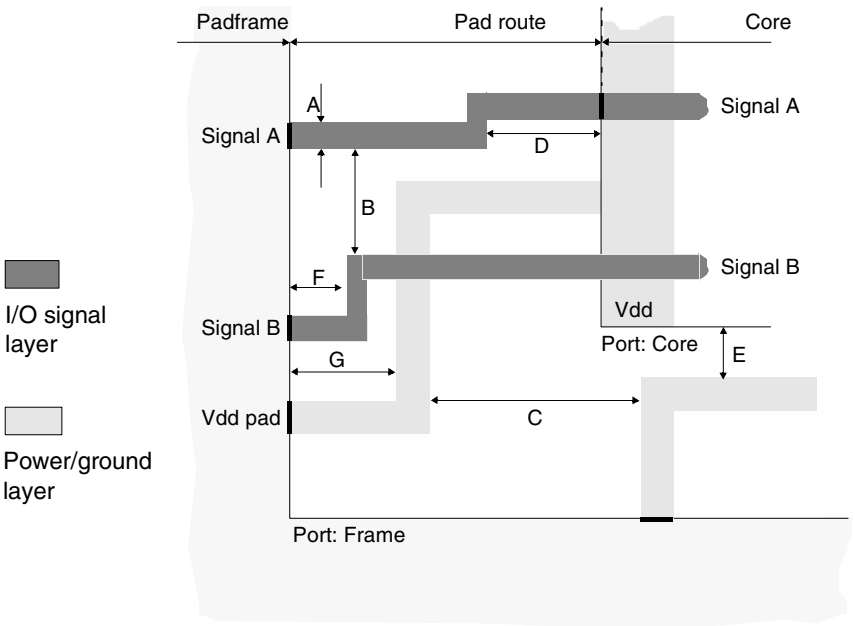
Use the **Design Rules** tab to specify design rule values L-Edit will use to perform pad routing that conforms to the fabrication technology used for your design. (The letters correspond to dimensions shown on pages 2-89 and 2-90.)



Values entered in this dialog are applied in the design as illustrated in the figures "Layer widths and spaces used in pad routing" and "Layer, core and pad spacing used in pad routing", below.

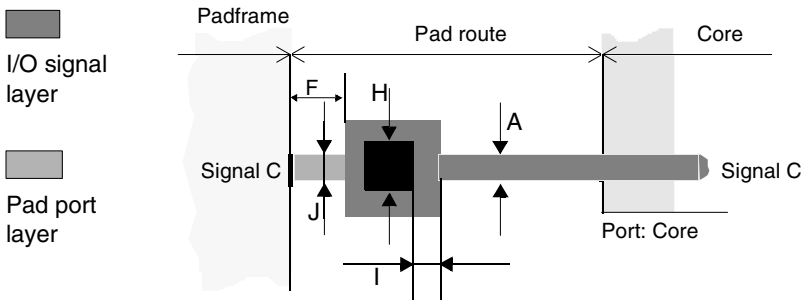
The letters in the dialog fields provide a key for the labels in the following illustrations and the values they represent.

If the pad cell ports are on the pad routing layer, L-Edit applies the following design rules.



Layer widths and spaces used in pad routing

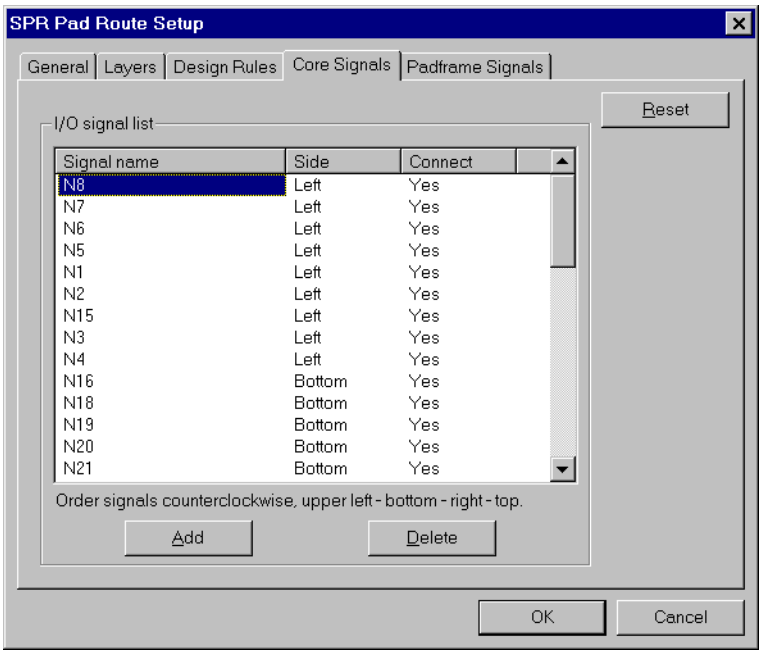
For I/O signals, *all* pad cell ports must be located on the same layer, but that layer need not coincide with the pad routing layer. In this case, L-Edit inserts a pad via, using the design rules illustrated below.



Design rules for pad via

SPR Pad Route Setup–Core Signals

Use the **Core Signals** tab to specify the signals entering or exiting the core. **Initialize Setup** will complete this dialog automatically if your netlist contains pad connections.



Enter the following information in the **I/O signal list**

Signal name

Defines the names of all signals exiting or entering the core, beginning with the first signal on the upper left side of the core and proceeding counter-clockwise. Edit the **Signal name**, **Side**, or **Connect** (**Yes** or **No**) by selecting the item and typing the desired value.

This list must contain as many signals as there are ports around the core.

To add a signal to the list, click **Add**. A **New signal** is highlighted and can be edited. To delete a signal, highlight it (by clicking any of its attributes) then click **Delete**.

Side

Side on which the signal is routed between the core and padframe. Options are:

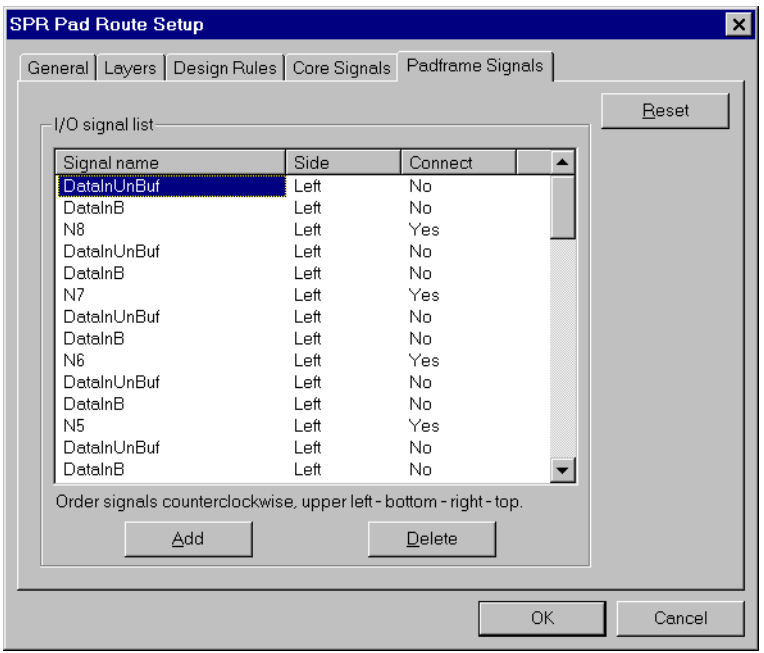
- **Left**
- **Bottom**
- **Right**
- **Top**

Connect

Options are **Yes** and **No**. To connect a signal to the padframe, type **Yes**; otherwise type **No**.

SPR Pad Route Setup–Padframe Signals

Use the **Padframe Signals** tab to specify a list of signals entering or exiting the padframe. **Initialize Setup** will complete this dialog automatically if your netlist contains pad connections.



Enter the following information in the **I/O signal list**:

Signal name

Defines the names of all signals exiting or entering the padframe, beginning with the first signal on the upper-left side of the padframe and proceeding counterclockwise.

This list must contain as many signals as there are pads around the padframe.

To add a signal to the list, click **Add**. A **New signal** is highlighted and can be edited. To delete a signal, highlight it by clicking any of its attributes then click **Delete**. To edit a signal, highlight it by clicking any of its attributes then click again to make the field editable.

Side

Side on which the signal is routed between the core and padframe. Options are:

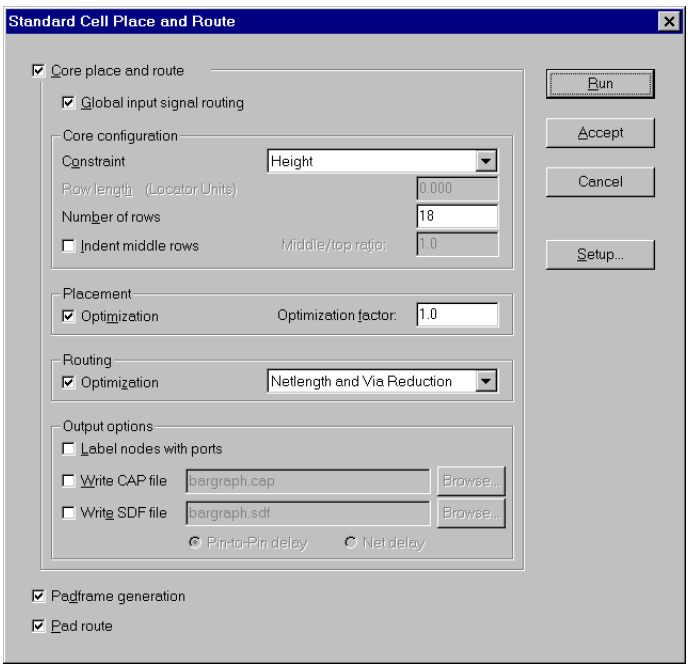
- **Left**
- **Bottom**
- **Right**
- **Top**

Connect

Options are **Yes** and **No**. To connect a signal to the padframe, type **Yes**; otherwise type **No**.

Standard Cell Place and Route

Use **Tools > SPR > Place and Route** to display the following dialog:



You can run the following three modules either in one step or separately:

- **Core place and route**—generates the design core using the options specified in **SPR Core Setup** (page 2-44).
- **Padframe generation**—generates the padframe using the options specified in **SPR Padframe Setup** (page 2-68).
- **Pad route**—routes between the padframe and the core using options specified in **SPR Pad Route Setup** (page 2-81).

Global input signal routing allows you to perform a separate route of up to two input signal nets. This option is only available when you select **Core place and route**.

Clicking **Setup** opens the **SPR Setup** (page 2-36) dialog.

Specify the following:

Constraint

Specifies the factors used to constrain core size and shape. Options include:

- **Square**—Generates a core with four sides of approximately equal length.
- **Width**—Generates a core using the specified **Row length**.
- **Height**—Generates a core using the specified **Number of rows**.
- **Width and Height**—Generates a core using the specified **Row length** and **Number of rows**.

Selecting **Width and Height** will interrupt SPR after placement if the program cannot meet both constraints. In such a case, L-Edit will ask you whether you want to abort or continue the SPR run.

Row length

Nominal length of rows placed in the core. Available only when **Constraint** is set to **Width** or **Width and Height**. This value is only an approximation, because the actual row length varies according to the number of row crosser cells inserted during routing.

Number of rows

Number of rows in the finished core. Available only when **Constraint** is set to **Height** or **Width and Height**. Increasing the number of rows makes the core taller and thinner; decreasing it makes the core shorter and wider.

Indent middle rows

Generates a core using the value entered in **Middle/top ratio**. This value is the ratio of the target length of the middle row of cells to that of the top and bottom rows.

Refer to Indent Middle Rows on page 2-102 for guidelines on values for this field.

This value must be between 0 and 1 (inclusive); the default value is 1. Using 1 for the **Middle/top ratio** is equivalent to turning off the **Indent middle rows** option.

Optimization (in **Placement** group)	Reduces core size by minimizing the overall netlength. When this option is off, L-Edit places cells according to their sequence in the netlist.
Optimization factor	Controls the degree of optimization and thus the quality of the placement. The higher the value, the greater the total placement time. Available only when **Optimization** is checked. See Optimization Factor on page 2-104 for guidelines on values for this field.

Optimization (in **Routing** group)

Optimizes routing by minimizing netlength, reducing the number of required vias, or both. When you select **Optimization** in the Routing group you must also specify one of the following options:

- **Netlength and Via Reduction**—invokes a postrouting algorithm that minimizes netlength (by shortening net loops) and reduces the number of generated vias (by eliminating unnecessary layer changes between net segments).
- **Netlength Reduction**—invokes a postrouting algorithm that minimizes netlength.
- **Via Reduction**—invokes a postrouting algorithm that reduces the number of generated vias.

Label nodes with ports

Places ports with the names of nodes onto the layout. You can use this option to extract a SPICE netlist with the original node names. This feature is also useful when it is necessary to perform any manual modifications to the results of the router, because it allows you to trace individual nodes as they wind through the core. For additional information on this option, see Label Nodes on page 2-107.

Write CAP file

Writes out a file of nodal properties, including nodal capacitances, after routing. Type the filename in the adjacent field or click **Browse** to select a file from a standard file browser. For additional information on this option, see Nodal Capacitance Files (CAP) on page 2-107.

Write SDF file

Writes out a file that lists the delays due to routing in standard delay format (SDF). Type the filename in the adjacent field or click **Browse** to select a file from a standard file browser.

Selecting the **Write SDF file** option gives you two delay options. **Pin-to-Pin delay** calculates the interconnection delay between a driver pin and a reciever pin. **Net delay** calculates the delay of the longest path of the interconnection. For additional information on this option, see Standard Delay Format Files (SDF) on page 2-113.

Indent Middle Rows

One factor affecting the width of standard cell rows is the number of *row crosser* cells inserted in a row. A row crosser is a small cell which contains a row crosser port but no logic; it simply provides a path for a signal to move through a row. When L-Edit needs to route a signal across a row of cells and no other cell in the row contains an unused row crosser port, the program inserts a row crosser cell.

Statistically, more row crossers are required in the middle rows of a design than in top or bottom rows, because the middle is more congested with logic. Hence, the middle rows might become significantly wider than they were estimated to be by the placement optimizer.

Select **Indent middle rows** for designs that have a significant number of row crosser cells added to their middle rows. If an initial SPR run produces a design

whose middle rows are significantly wider than the top or bottom rows, use a **Middle/top ratio** of less than 1.

Placement Optimization

The core of a standard cell design contains rows of *standard cells*, which are designed to abut one another horizontally to form power and ground connections.

You can produce a more compact design by selecting **Optimization** in the **Placement** group. With **Optimization** on, L-Edit considers the positions and connections of standard cells and alters those positions where necessary to achieve a more compact layout. For example, if the output of a DFF is connected to the input of an inverter, the optimizer might relocate the DFF or the inverter to make the wire between them as short as possible.

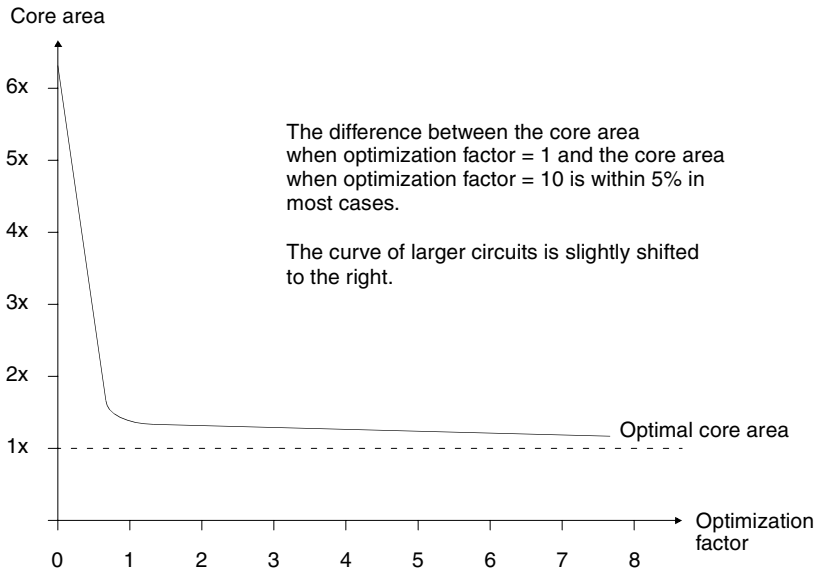
With **Optimization** off, L-Edit simply places cells according to their sequence in the netlist.

When you select **Optimization**, you must also choose an **Optimization factor**. This factor enables you to control the degree of optimization and thus the quality of the placement. The higher the optimization value, the greater the total placement time will be. For additional information on this field, see Optimization Factor, below.

Optimization Factor

L-Edit uses a *simulated annealing algorithm* to optimize placement (described in Sechen, see References on page 2-120). The optimizer algorithm randomly chooses pairs of cells and determines whether their locations should be exchanged in order to reduce the overall net length.

The **Optimization factor** is a measure of the number of states which the optimizer looks at per cell for every temperature step of the process, and so controls the placement time. For example, the placement for an optimization factor of 2 should be about an order of magnitude slower than a placement for an optimization factor of 0.2. Although it is possible to obtain better final results by increasing the factor by one or two orders of magnitude, a factor of 1 represents a balanced trade-off between total placement time and final core area. The following figure shows the average relationship between the final optimized core area and the optimization factor. Clearly, the improvement to the core area is not large for factors greater than 1.



Optimization factor and core area for circuits up to 1000 standard cells.

Note: To minimize core size, it is best to run SPR several times with different optimization factors of around 1 rather than running it once with a single large optimization factor.

An optimization factor of 0 is not equivalent to "no optimization." The optimizer will still run through placement, the row evener, global routing, and detailed routing with a minimal running time and a minimal effect on the placement optimization of the design. This is a good value to use while experimenting with other optimization controls (for example, changing the number of rows).

You can bypass placement optimization by clearing the **Optimization** check box. This is the fastest method for generating layout, but the final core will be significantly larger than a core produced with optimization.

Note: To avoid excessive complexity in channel routing, it is recommended that you always turn **Placement Optimization** on for circuits with more than 2,000 standard cells.

Output Options

Label Nodes

The **Label nodes with ports** switch instructs L-Edit to place ports on the layout (in the vertical routing layer) using the same port names as those used in the design schematic. You can use this option to extract a SPICE netlist with the original node names. This feature is also useful when it is necessary to perform any manual modifications to the results of the router, because it allows you to trace individual nodes as they wind through the core.

Nodal Capacitance Files (CAP)

The option **Write CAP file** instructs L-Edit to compute the capacitance, length, and area added to each node due to routing. L-Edit writes the results to a plain-text file with the filename extension **.cap**.

Each line in the file is in the format:

node capacitance NoOfTerminals Length AreaOnH1 AreaOnV AreaOnH2

where *node* is the name of the node, *capacitance* is an integer denoting capacitance of this node in hundredths of a picofarad, *NoOfTerminals* is the number of pins attached to this node, and *Length* is the length of the interconnect

of this node. *AreaOnH1*, *AreaOnV*, and *AreaOnH2* denote the area of the route taken by this node on the H1, V, and H2 layers.

Note: To use this file in a simulation, you must convert it to SPICE format using a translator such as NetTran.

Node capacitances are calculated based on the capacitance per unit area for a particular routing layer and the area occupied by the node. The capacitance per unit area for a layer is the capacitance between a particular routing layer and the substrate or the capacitance between two routing layers. Node capacitances also consider the fringe capacitance per unit length between the edges of the routing and the substrate.

The base values for capacitance between a layer and substrate or layer and another layer, as well as the fringe capacitance between the routing layer and the substrate, are entered by the user. These capacitance values are process-dependent and should be available from your chip foundry.

In the following discussion, we assume the horizontal routing layers to be *Metal1* and *Metal3* and the vertical routing layer to be *Metal2*. The capacitance on a node C_{node} is computed as

$$\begin{aligned} C_{node} &= C_{A,M1S}A_{M1} + C_{A,M2S}A_{M2} + C_{A,M3S}A_{M3} && \text{[non-overlap]} \\ &+ C_{O,M1M2}A_{M1M2} + C_{O,M1M3}A_{M1M3} && \text{[overlap M1]} \\ &+ C_{O,M2M1}A_{M2M1} + C_{O,M2M3}A_{M2M3} && \text{[overlap M2]} \\ &+ C_{O,M3M1}A_{M3M1} + C_{O,M3M2}A_{M3M2} && \text{[overlap M3]} \\ &+ C_{F,M1S}P_{M1} + C_{F,M2S}P_{M2} + C_{F,M3S}P_{M3} && \text{[fringe]} \end{aligned} \tag{2-1}$$

with

$$C_{O,M1M2} = C_{A,M1S} + C_{A,M1M2} \tag{2-2}$$

$$C_{O,M1M3} = C_{A,M1S} + C_{A,M1M3} \tag{2-3}$$

$$C_{O,M2M1} = C_{A,M1M2} \tag{2-4}$$

$$C_{O,M2M3} = C_{A,M2S} + C_{A,M2M3} \tag{2-5}$$

$$C_{O,M3M1} = C_{A,M1M3} \quad (2\text{-}6)$$

$$C_{O,M3M2} = C_{A,M2M3} \quad (2\text{-}7)$$

where

$C_{A,MXS}$	Area capacitance per unit area between the *MetalX* layer and the substrate (entered using **Setup > Layers—General**).
$C_{A,MXMY}$	Area capacitance per unit area between the *MetalX* layer and the *MetalY* layer (entered in the **SPR Core Setup–Layers** (page 2-47) dialog).
$C_{O,MYMX}$	Overlap capacitance per unit area on *MetalX* when overlapped by routing on *MetalY* (calculated by SPR).
$C_{F,MXS}$	Fringe capacitance per unit length between the *MetalX* layer and the substrate (entered using **Setup > Layers—General**).

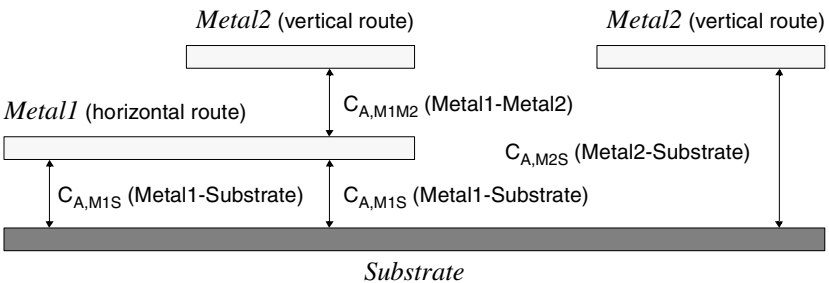
A_{MX}	Area covered by the route of this node in *MetalX* with no overlap to any routing in any other layer (calculated by SPR).
A_{MXMY}	Area covered by the route of this node in *MetalX* that overlaps with routing in *MetalY* layer (calculated by SPR).
P_{MX}	Perimeter of all routing segments of this node in *MetalX* (calculated by SPR).

Two-Layer Example

It is important to know how to extract numbers from the foundry's actual process parameter sheet for entry in the dialog. In the following two-layer example, the process parameters are taken from a typical 2-micron *N*-well process. The value given for each layer (except for the last entry) is the area capacitance between the specified layer and the substrate, in aF/μm^2.

Layer	***C_A***
Poly—Substrate	55
N Diff—Substrate	128
P Diff—Substrate	322

Layer	C_A
Metal1— Substrate ($C_{A,M1S}$)	25
Metal2—Substrate ($C_{A,M2S}$)	20
Metal1—Metal2 ($C_{A,M1M2}$)	38



Interconnect capacitances in two-layer routing

Capacitance values are entered with two setup commands.

Dialog	*Values entered*
Setup Layers—General, **Layer-to-substrate [Area] capacitance** field	$C_{A,M1S}$ = **25** and $C_{A,M2S}$ = **20** are entered for *Metal1* and *Metal2*, respectively.
SPR Core Setup–Layers, **Layer-to-layer area capacitance** field	$C_{A,M1M2}$ = **38** is entered.

The overlap capacitances of *Metal1* and *Metal2* are internally calculated as follows:

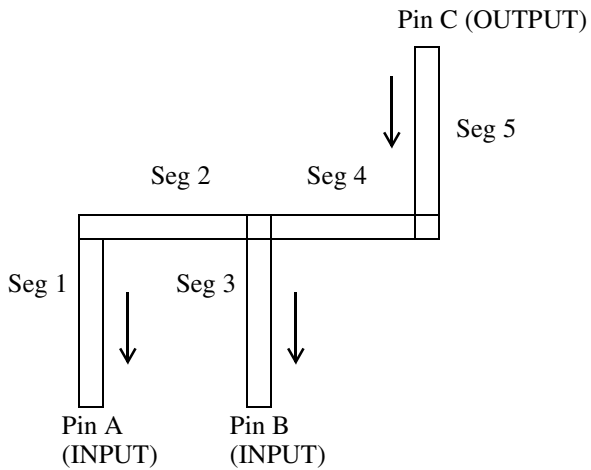
- An overlapping node on *Metal1* sees an overlap capacitance of $C_{A,\,M1S} + C_{A,M1M2}$.
- An overlapping node on *Metal2* sees an overlap capacitance of $C_{A,M1M2}$ only.
- Thus, $C_{O,M1M2} = C_{A,M1S} + C_{A,M1M2} = 63$ and $C_{O,M2M1} = C_{A,M1M2} = 38$.

Standard Delay Format Files (SDF)

When you run SPR with the option **Write SDF file**, L-Edit computes the delays due to routing and outputs the results into a standard delay format (SDF) file with the filename extension **.sdf**.

The L-Edit interconnect delay calculation is based on the Elmore delay model. The capacitance and resistance is extracted segment by segment and distributed as a π model.

Each segment of the interconnect is associated with a lumped ***R*** and ***C*** value.



The ***R*** and ***C*** values are determined by

$$R = R_{square} \cdot (Length\ of\ segment / Width\ of\ segment) \quad (2\text{-}8)$$

$$C = C_{area} \cdot Area\ of\ segment + C_{fringe} \cdot Perimeter\ of\ segment \quad (2\text{-}9)$$

where width of segment is defined as the wire edge that connects to the pin and

$$Perimeter = 2 \cdot (Length\ of\ segment + Width\ of\ segment) \quad (2\text{-}10)$$

Note: Capacitance with respect to the substrate is the only capacitance component that is considered. No attempt is made to include layer-to-layer or crosstalk capacitance terms.

The detailed ***R*** and ***C*** values are calculated as follows:

For a segment located on Metal*n*:

$$R = R_{Mn} \cdot Number\ of\ squares = R_{Mn} \cdot (L_{seg} / W_{seg}) \quad (2\text{-}11)$$

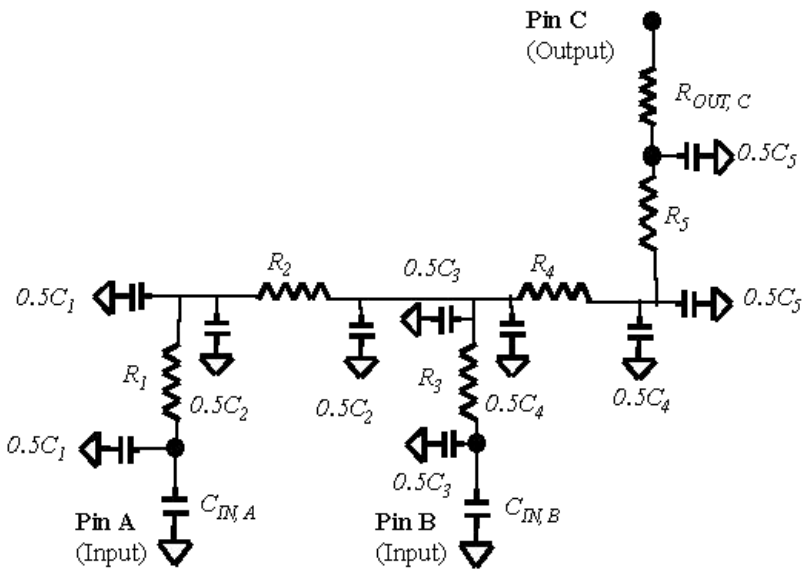
$$C = C_{A,\,MnS} \cdot A_{Mn} + C_{F,\,MnS} \cdot \dot{P}_{Mn} \quad (2\text{-}12)$$

where

R_{Mn}	Resistivity (resistance per square) of the Metal*n* layer	Entered in **Setup Layers—General**.
$C_{A,MnS}$	Area capacitance per unit area between the Metal*n* layer and the substrate	Entered in **Setup Layers—General**.
$C_{F,MnS}$	Fringe capacitance per unit length between the Metal*n* layer and the substrate	Entered in **Setup Layers—General**.
L_{seg}, W_{seg}	Length and width of the segment	Calculated by SPR
A_{Mn}	Area covered by the segment of this node in Metal*n*	Calculated by SPR
P_{Mn}	Perimeter of the segment of this node in Metal*n*	Calculated by SPR

Note: The area and perimeter term includes the small amount of overlap between layers. The error resulting from this inclusion is negligible.

The ***R*** and ***C*** values for each segment are distributed as a π model. For the above interconnection, the ***R*** and ***C*** values are distributed as follows:



Pin-to-Pin Delay Calculation

The pin-to-pin delay is the interconnection delay between a driver pin and a receiver pin. In this example, the pin **C** is the driver pin and the pins **A** and **B** are the receiver pins.

(2-13)

$$\begin{aligned} Delay(PinC-PinA) &= R_5 \cdot 0.5C_5 + R_4 \cdot (0.5C_4 + C_5) \\ &+ R_2 \cdot (0.5C_2 + C_3 + C_4 + C_5) \\ &+ R_1 \cdot (0.5C_1 + C_2 + C_3 + C_4 + C_5) \\ &+ R_{out,C} \cdot C_{in,A} + (R_{out,C} + R5 + R4 + R2 + R1) \cdot C_{in,A} \\ &+ (C_{in,A} + C1 + C2 + C3 + C_{in,B} + C4 + C5) \cdot R_{out,C} \end{aligned}$$

(2-14)

$$\begin{aligned} Delay(PinC-PinB) &= R_5 \cdot 0.5C_5 + R_4 \cdot (0.5C_4 + C_5) \\ &+ R_2 \cdot (0.5C_2 + C_3 + C_4 + C_5) \\ &+ R_3 \cdot (0.5C_3 + C_2 + C_1) \\ &+ R_{out,C} \cdot C_{in,B} + (R_{out,C} + R5 + R4 + R3) \cdot C_{in,A} \\ &+ (C_{in,A} + C1 + C2 + C3 + C_{in,B} + C4 + C5) \cdot R_{out,C} \end{aligned}$$

This delay calculation corresponds to the 63.2% threshold voltage of the single-pole response.

Net Delay Calculation

The net delay is the delay of the longest path of the interconnection. In this example, the longest path is from **A** to **C**; therefore, the net delay is calculated using Elmore delay as:

$$\begin{aligned} Netdelay &= R_5 \cdot 0.5C_5 \\ &+ R_4 \cdot (0.5C_4 + C_5) \\ &+ R_2 \cdot (0.5C_2 + C_3 + C_4 + C_5) \\ &+ R_1 \cdot (0.5C_1 + C_2 + C_3 + C_4 + C_5) \end{aligned} \tag{2-15}$$

This delay calculation corresponds to the 63.2% threshold voltage of the single-pole response.

References

Sechen, Carl. 1988. *VLSI Placement and Global Routing Using Simulated Annealing*. Boston: Kluwer Academic Publishers.