3 Standard Cell Library Designer's Guide

Standard Cell Library

The cells in a standard cell library must meet certain constraints of dimension and port positions for proper use by L-Edit. Usually, a standard cell library includes two types of cells:

- *Standard* cells, which L-Edit can place and route.
- *Pad* cells, an optional set, which L-Edit uses in padframe generation and routing.

Standard Cells

Abutment Ports

Each standard cell should have a special abutment port whose name is consistent with the **Abutment port** entry in the **SPR Core Setup–General** (page 2-45) dialog. The dimensions and position of an abutment port correspond to the boundaries of the cell to which it belongs. The abutment port must have the same height in all standard cells in a library set.

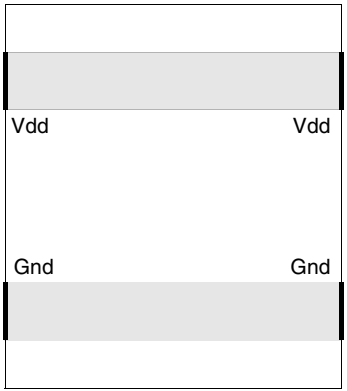
Note: Channel routing will take less time when the abutment ports are of a uniform width and spacing. Abutment port widths should also be integer values.

Power Ports

Power buses enter and exit at the ends of the standard cell rows, run horizontally along the row, and connect to power ports within each cell, which must be placed on both sides of a standard cell at the cell boundary. Power port names are specified in the **Power Signal** and **Ground Signal** fields in the **SPR Setup** dialog.

Ports for a power terminal (Vdd or Gnd) must have the same height and position relative to the abutment port in every standard cell of a library set. The width of

power ports has to be zero. The power rail can run along the left or right side of the core, as specified in the **SPR Core Setup–I/O Signals** (page 2-64) dialog.



Typical power bus arrangement and power port positions.

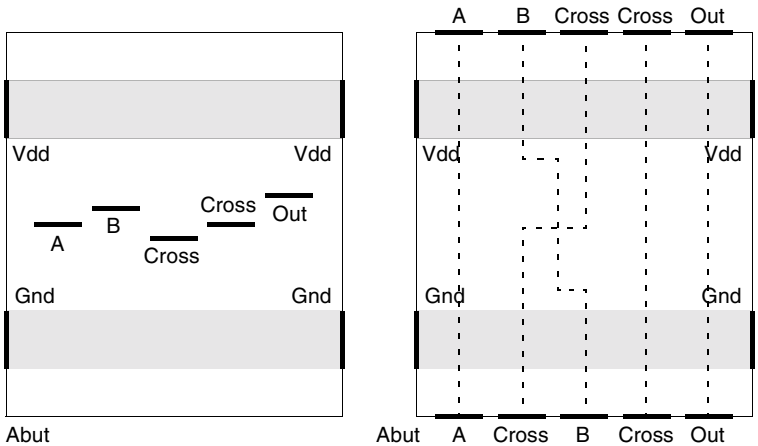
Signal Ports

Signals other than power and ground are routed to ports through the top or bottom sides of a standard cell. A signal port must have a height of zero and a

name complying with that of standard cell primitives in the netlist, and it must be placed on the same layer as the vertical routing wires.

Signal ports for signal routings must be placed at related layout geometry where the signals are available. Signal port positions must comply with the relevant design rules (see **SPR Core Setup–Design Rules** (page 2-51)), with predefined routing width and space specifications. Signal ports can be either inside the standard cell or on its boundary (see the illustration Signal port positions in standard cells on page 2-126.)

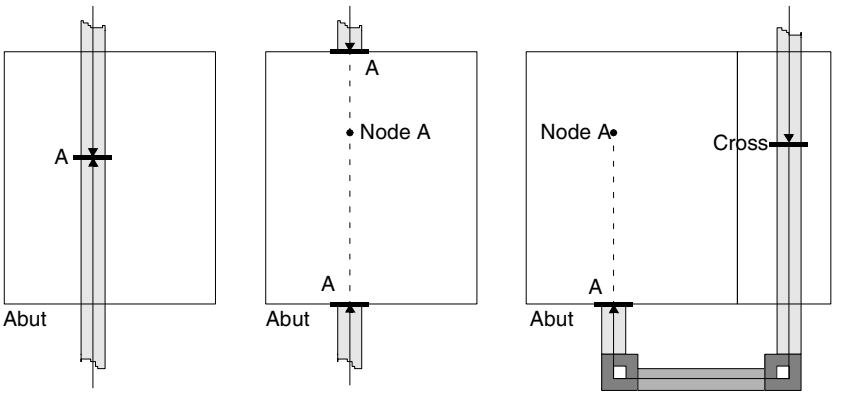
Note: Channel routing will take less time when the signal ports are of a uniform width and spacing. Signal port widths should also be integer values.



(a) Signal ports in cell interior (b) Signal ports on cell edges

Signal port positions in standard cells

There are three options for routing wires to fit specific layout features of a standard cell set.



Option 1: Vertical routing wires are allowed to overlap a standard cell and allowed to enter the cell from the top or bottom.

Option 2: Vertical routing wires are *not* allowed to overlap any portions of a standard cell. They are allowed to reach ports at either top or bottom edges of the cell. It is assumed that every pair of the same named ports relates to the same internally connected node.

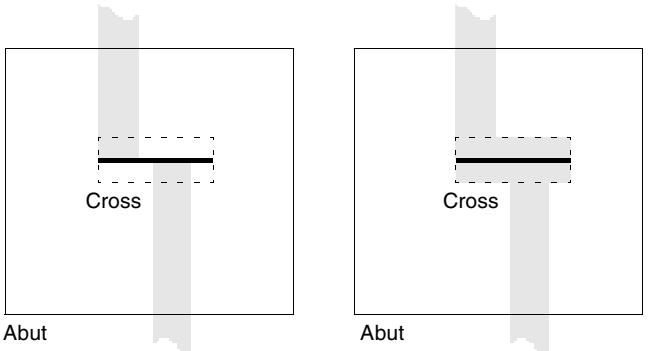
Option 3: Vertical routing wires are only allowed to reach from a designated side of a standard cell. In this example, a wire coming from the upper routing channel reaches the signal port A (at the bottom edge of the cell) through an additional row crosser cell and an additional horizontal routing wire in the lower channel.

Routing wire arrangements in standard cells

Row Crosser Ports

To route wires between two routing channels—that is, across a standard cell row—L-Edit uses user-specified row crosser ports that identify crossing paths on standard cell rows. (Row crosser ports illustrated in figures in this chapter have the port name **Cross**.) The use of row crosser ports is illustrated in a regular standard cell in the figure Signal port positions in standard cells on page 2-126 and in a dedicated row cross cell in the figure Routing wire arrangements in standard cells on page 2-127 (Option 3). In a regular standard cell, it is a good practice to place as many row crosser ports as design rules and SPR constraints allow. This helps L-Edit increase area efficiency, because if there are no more row crosser ports in standard cells within a certain row span, L-Edit may have to insert a row crosser cell.

A row crosser cell is a standard cell that contains only one row crosser port and is placed only to make up a cross-row pass. In the figure Signal port positions in standard cells on page 2-126 (b), L-Edit will treat the pairs of port **Cross** as a crossing pass between the routing channels above and below the current standard cell row. As with signal ports, it is assumed that the pair are internally connected with layout geometry in related layers in the standard cell. L-Edit picks pairs of row crosser ports from left to right. Dotted lines in the figure connect related upper and lower signal ports. The figure SPR box generation for design rule correctness of a row crosser port on page 2-129 illustrates how L-Edit automatically generates extra geometry around a row crosser port to ensure design rule correctness at that location.



(a) Dotted line indicates the region around a cross port where design rules may potentially be violated during SPR.

(b) During SPR, L-Edit automatically generates a box in the vertical routing layer to ensure design rule correctness.

SPR box generation for design rule correctness of a row crosser port

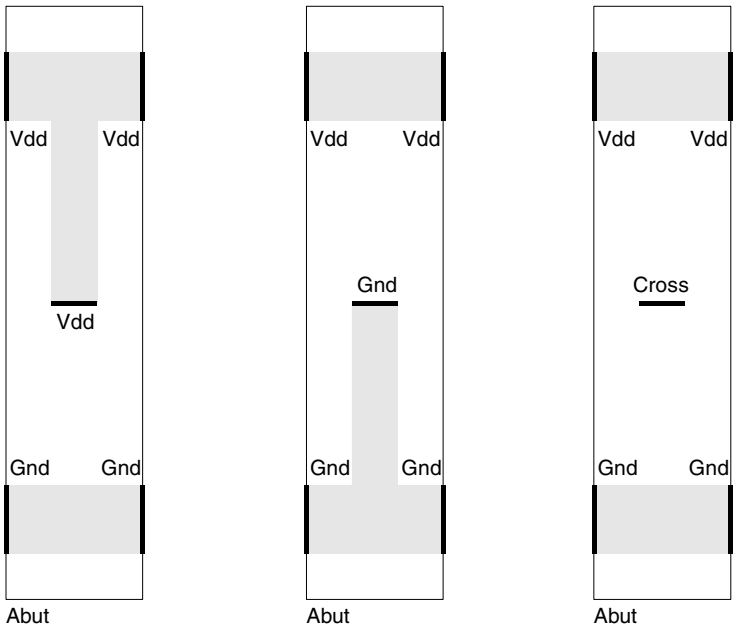
Note: Row crosser ports must be placed on the vertical routing layer. SPR will not recognize such a port when it is placed on the horizontal routing layer.

Special Standard Cells

L-Edit requires three special standard cells to be included in a library cell set. These cells are not standard cell primitives like the ones included in the netlist; they are for node connections only.

The *Tie-to-Power Cell* and *Tie-to-Ground Cell* are needed where a standard cell has a pin directly tied to Vdd or Gnd. The *Row Crosser Cell* is a special standard cell that contains only a row crosser port. Its sole purpose is to allow a connection between two channels located above and below a standard cell row. The figure Connection cells in a standard cell set, below illustrates these three typical connection cells.

Although a given SPR operation might not require these three cells—the use of the Tie-to-Power cell or Tie-to-Ground cell depends on the specific netlist, and the use of row crosser cells depends on the actual routing condition—L-Edit treats them as prerequisite and elementary parts of the standard cell library. Specify the names of the Tie-to-Power, Tie-to-Ground, and row crosser cells in the **SPR Core Setup–General** (page 2-45) dialog. L-Edit will report an error if any of these three cells are missing in the standard cell library.



Connection cells in a standard cell set

Pad Cells

Abutment Ports

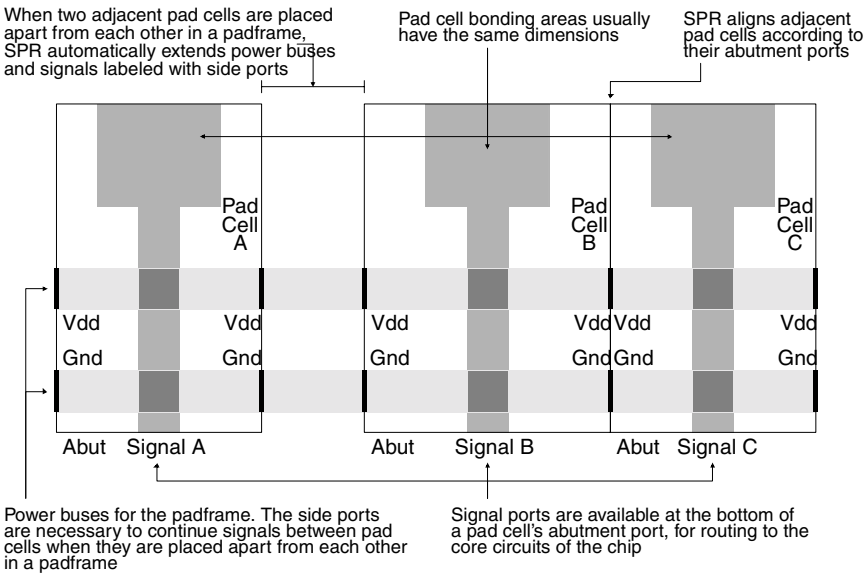
Each pad cell should have a special abutment port whose name is consistent with the entry **Pad cell abutment port** in the **SPR Padframe Setup–General** (page 2-69) dialog. The dimensions of an abutment port geometry specify the boundaries of the cell to which it belongs. The abutment port must have the same height in all pad cells in a library set.

Connection Ports Between Pad Cells

When pad cells are placed in a padframe, power buses and signal buses (if specified) run horizontally across each pad cell. During padframe generation, L-Edit places pads in a user-specified padframe and fills the gaps between pads with cell connections to assure continuity of power and/or signal buses to all pads. These interpad connections must have dedicated ports on two sides of the pad cell boundary. Power ports in all pad cells in a library set must have the same height and the same position along the cell boundary. The existence of interpad connection ports in a particular layer specifies a connection in that layer.

The figure Typical pad cells lined up in a segment of a padframe on page 2-134 (simplified so that only straight signal passes and power buses are shown) illustrates connections between pad cells **A** and **B**. In padframe generation,

L-Edit can optimize the padframe under certain conditions so that adjacent pads are attached to each other, as shown between pad cells **B** and **C**. In this case, the abutment ports (labeled **Abut**) specify the pad cell boundaries and allow L-Edit to abut and align pad cells. The same figure also shows typical arrangements of power bus ports (on the sides) and signal ports (on the bottoms) in pad cells.



Typical pad cells lined up in a segment of a padframe

Signals from Pad to Layout Core

In order to interface with the layout core of a chip, signal ports must be available on the bottom boundary of a pad cell. A signal port is a zero-height port with its width equal to the layout path of the dedicated signal.

Power Supply Pads

In padframe generation, L-Edit automatically places one Vdd pad cell and one Gnd pad cell into the frame. Their cell names can be customized in the **SPR Padframe Setup** (page 2-68) dialog. A power supply pad cell is subject to the same structure constraints as a normal signal pad. There must be at least one pair of power supply pads in a padframe, which provide both power connections to all pads in the padframe and to the layout core of the chip. It is not necessary to specify these power supply pad cells as library primitives in your netlist. If your design requires secondary power supply pads, specify them in the netlist as you would regular signal pads.

Corner Pad Cells

Standard cell libraries must include a special corner pad cell, which is required to complete a padframe. This cell will be oriented and placed at all four corners of the padframe. A corner pad usually contains no active circuit, signal path, or bounding area because it does not directly face the layout core. Corner cells continue the power bus and other signal connections between two perpendicular

sides of the padframe. They may also contain certain electrostatic discharge (ESD) protection guardbands in structures as they are built in regular pad cells. For proper extension of power buses and signals, corner pad cells must meet the same design requirements as regular pad cells. In particular, they must contain side ports like those created in regular pad cells.

Pad Cells Without Bond Pads

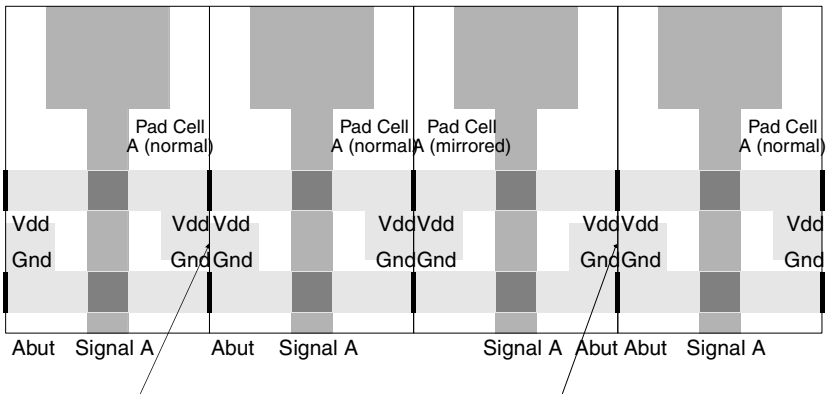
In some cases, a pad cell is needed to fill a gap in a segment of a padframe. Pad cell sets are allowed to have pad cells without bonding pads. Such a pad will not be bondable, but it can serve as a padframe spacer cell. L-Edit allows any such unbondable pad cells to occupy a pad slot in the padframe specification, as specified in the **SPR Padframe Setup** (page 2-68) dialog. The figure Mirror-labeled pads in a padframe on page 2-140 illustrates how pad slots are indexed in the **SPR Padframe Setup**—**Layout** dialog. Typical uses of such spacers are as padframe corner cells and padframe spacer cells. L-Edit requires corner cells to complete a padframe; spacer cells may be useful optional cells when specific padframe geometry and dimensions are required by a chosen process vendor. Since no signal paths lead to the layout core of the chip, it is not necessary to include these types of pad cells in the netlist primitive set.

Pad Orientations

The **Mirror** switch in the **SPR Padframe Setup**—**Layout** dialog, set by typing **Yes** or **No** in the **Mirror** column of the padlist, instructs L-Edit to mirror an individual pad when placing it in a padframe. This feature is especially useful

when a pad cell contains asymmetrical features that would affect intercell connections. In the figure Using a mirrored pad cell in a padframe, below, pad cell **A** has a wider ground bus on the left side and wider power bus on the right. Consequently, a power short exists between the first pad cell **A** on the left and its duplicate on the right—i.e., Vdd in the left pad cell **A** has been connected to Gnd in the duplicate pad cell **A** on the right. The power short has been avoided in the

next two duplicated pairs of pad cell **A**, because the third pad cell **A** has been placed in its mirrored orientation.



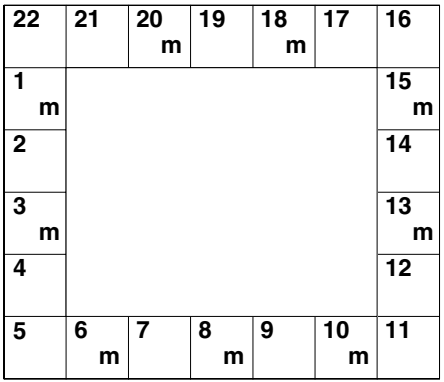
Using a mirrored pad cell in a padframe

Mirror Ports

You can specify a **Pad cell mirror port** in the **SPR Padframe Setup–General** (page 2-69) dialog. When L-Edit encounters a pad cell with the specified mirror port name, the program automatically alters this pad cell's orientation when placing it adjacent to another pad cell labeled as a mirror port. In addition, this mirroring feature can be propagated through a padframe's corner pad cell if the corner pad cell has also been labeled with a mirror port.

The figure Mirror-labeled pads in a padframe on page 2-140 shows an example of an SPR-generated padframe with some typical mirroring effects. All pad cells

and padframe corner cells contain mirror ports. Pad cells labeled **m** are in mirrored orientation, while other cells are on their normal orientation.

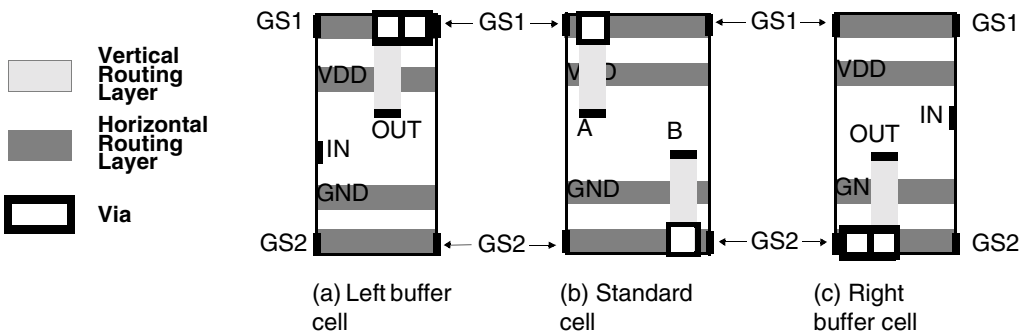


Mirror-labeled pads in a padframe

Designing Cells for Global Signal Routing

Global Signal Port Definitions

For global input signal routing, standard cells and buffer cells are extended by two global signal buses, which are located above and below the power buses on the horizontal layer. Each bus contains two ports (labeled **GS1** and **GS2** in the following figure). These port names are defined during cell design, and they thus become part of the cell definition in the standard cell library.



Global signal ports (GS1 and GS2) in standard cells and buffer cells

Global signal port names are assigned to the global input signals in the **SPR Core Setup–Global Signals** (page 2-59) dialog. Note that in this dialog, SPR users also assign a specific net name to each of the global input signals. Thus, the assignment of a global input signal port to each of the global input signals determines which signal bus (upper or lower) represents a specific global signal net. Because buffer cells are specifically dedicated to either the upper or lower global signal bus, this port assignment also determines:

- Which global signal rail (left or right) represents a specific global signal net.
- The side of the padframe on which the pad of this net is placed.

As an example, let **NetA** be the name of a signal designated **Global Input Signal 1**. Assume that the standard cell library contains buffer cells designed as those shown in the figure Global signal ports (GS1 and GS2) in standard cells and buffer cells on page 2-141, with the left buffer cell connecting to the upper global signal bus, which is labeled with the port **GS1**. If port **GS1** is designated as the port for **Global Input Signal 1** (which is **NetA**), the following will occur:

- In the standard cells, the internal signal port for **NetA** will be connected to the upper global signal bus because **GS1** is its assigned port name.
- Because the left-side buffer cell is designed such that it drives the upper global signal bus, the left global signal rail will carry **NetA**.
- Subsequently, it will be necessary to specify that **NetA** exit the left padframe edge (see **SPR Pad Route Setup–Padframe Signals** (page 2-93)).

Note: Because buffer cells are specifically dedicated to either the upper or lower global signal bus, buffer cell design determines the relationship between port names and the side on which the net associated with this port leaves the core. The buffer cell designer thus determines the side of the padframe to which global signal ports are ultimately connected.

Buffer Cell Input Ports

Besides meeting all general design constraints imposed on standard cells, buffer cells used in global input signal routing must also meet the following constraints:

- Each buffer cell must contain an input port located on one side of its abutment port. The left buffer cell has its input port on the left side of its abutment port; the right buffer cell has its input port on the right side of its abutment port.
- Input ports on buffer cells must be vertical ports (height > 0, width = 0) and reside on the vertical routing layer.

The height of the input port determines the width of the global signal rail connected with it. The width of the global signal rail will be twice the height of the input port. Buffer cell input port names can be arbitrary.