7 LVS Command-Line Syntax

Running LVS from the Command Prompt

You can invoke LVS from a DOS command prompt, specifying input and output files plus all verification options on the command line, and achieve the same results as you would when running LVS under Windows. Additionally, for batch-mode operation, LVS must be invoked from a DOS command prompt.

To invoke LVS, change to the LVS directory on your hard disk, or make sure that the LVS directory is in your path. Then enter the LVS command at the DOS prompt:

LVS `[options] "netlist1" "netlist2"`

netlist1 and ***netlist2*** are the two netlist files to be compared. Specify the full path for any file not in the current directory and enclose the entire filename and path in quotation marks.

Filenames and paths with spaces in them are legal, but depending on the DOS operating system version you are using, arguments longer than 112 characters may not be allowed. Exceeding this length will result in the error message “Unrecognized line argument” and termination of LVS processing.

options are command-line arguments, which provide additional operating instructions to LVS.

Each of these arguments is discussed in Options on page 3-245.

Batch-File Syntax

An LVS batch file will contain text like the following:

```
start /w lvs "C:\Program Files\Tanner EDA\L-Edit Pro
   v8.00\Samples\LVS\ex2_1.spc" "C:\Program Files\Tanner
   EDA\L-Edit Pro v8.00\Samples\LVS\ex2_2.spc" -o
   "C:\Program Files\Tanner EDA\L-Edit Pro
   v8.00\Samples\LVS\ex2.lvs" -nrcl -c1245 -dv5.000 -
   dg0.010 -vfa -q
```

Each verification listed in a batch file must begin with the command **start /w**. This command instructs DOS to start LVS with the first set of options and wait for the program to exit before launching it again. Without this command, only the first verification run listed in the batch file would succeed. LVS would fail to run subsequent verifications.

Note that in contrast to the simple command-line example on the previous page, which lists options before the netlist files, this batch-file example lists options following the netlist files. The command **File > Export Batch File** uses this syntax in creating batch files, but in fact, either syntax is legal. If you create a batch file directly in a text editor, you can list command-line options before or after the netlist files. LVS accepts either syntax.

Running a Batch File

To run a batch file, enter the following command from a DOS command prompt:

```
filename.bat
```

where ***filename*.bat** is the name of the batch file.

LVS will start up and run the verifications listed in the batch file. The program will create a user-specified output file, as specified by the **-o** command-line option.

You can view the resulting output file using the LVS text window or any other text editor.

Note: LVS does not support launching of multiple instances. If you are running LVS under Windows, you must first exit the program before running a batch file from the DOS command line.

Options

Options are preceded by a dash or minus sign (**-**) and are separated by spaces. You can specify options before or after the two netlist files—LVS accepts either syntax.

Where options have arguments, such as **-c*nnn***, the option can be typed with or without a space between the option and the argument—as **-c*nnn*** or **-c *nnn***. LVS accepts either syntax.

Except where specifically noted, command-line options are case-insensitive.

Ignore Bulk Nodes (-b)

This option is the inverse of **Consider bulk nodes (substrate) during iteration matching** in the setup window.

The **-b** option instructs LVS to ignore bulk (substrate) nodes on semiconductor devices during the iteration matching process. (By default, LVS takes bulk nodes into consideration.) A typical digital design will always have the bulk nodes of elements connected to power or ground. Ignoring the bulk nodes while processing such files will reduce memory usage and increase processing speed.

The bulk node parameter is optional in the netlist input file. If you instruct LVS to consider bulk nodes but all of the bulk nodes are not present in the netlists, the iteration process will result in fragmentation.

Consider Parameters (-c*nnnn*)

The **-c*nnnn*** option tells LVS what parametrical information to consider during iteration matching and trial matching. ***nnnn*** is a series of single-digit integers from the following list. This option corresponds to the following options in the setup window (see **Setup Window—Advanced Parameters** (page 3-164).

1 Consider resistance, capacitance, and inductance for R, C, and L elements.

2 Consider L and W for MOSFETs.

3 Consider AS, AD, PD and PS for MOSFETs.

4 Consider areas of B, D, J, and Q elements.

5 Consider Z0 for T elements.

6 Consider TD, F, and NL for T elements.

7 Consider NRD, NRS, NRG, and NRB for MOSFETs.

For example, to consider resistance, capacitance and inductance; L and W; and NRD, NRS, NRG, and NRB, use **-c127**.

Maximum Value Difference (-dv *n*)

This option corresponds to **Maximum element-value tolerance** in the setup window (see **Setup Window—Advanced Parameters** (page 3-164).

The **-dv*n*** option, where ***n*** is a percent value between 0 and 100, defines the maximum amount two parameter values may differ and still compare as equal. This value is often referred to as the *slew rate*. The number is expressed as a percentage of the larger parametrical value. The default is 5% (**-dv5**). Noninteger values are permitted (for example, **-dv4.5**). This option takes effect only when the **-c127** option is used.

For example, if **element1** had a capacitance of 15.5 fF and **element2** had a capacitance of 16.1 fF, they would be considered equivalent with **-dv4**, but not with **-dv3**.

See also Consider Parameters (-cnnnn) on page 3-246.

Maximum Geometrical Difference (-dg*n*)

This option corresponds to **Maximum geometric-value tolerance** in the setup window (see **Setup Window—Advanced Parameters** (page 3-164)).

The **-dg*n*** option works in exactly the same manner as **-dv*n***, except that it operates on geometrical comparisons, such as L and W for MOSFETs. The default value is 0.01% (**-dg0.01**). This option has an effect only when the **-c3456** option is used.

See also Consider Parameters (-cnnnn) on page 3-246.

Element Description File (-e"*file*")

This option corresponds to **Element description file** in the setup window (see **Setup Window—File** (page 3-158).

The **-e"*file*"** option specifies the location of the element description file named ***file***. Specify the full path if needed, and enclose the entire filename and path in quotation marks. LVS recognizes standard SPICE elements such as resistors, inductors, capacitors. If you use a nonstandard element, however, you will need to define it in an element description file and use this option to instruct LVS to read in the file. The netlist files can include elements described in the element description file by using them as a subcircuit element.

Granularity (-%g=*n*)

The **-%g=*n*** option controls the granularity of the percentages displayed while LVS is iterating. The default is g = 5; LVS will report its progress to the screen in increments of 5%, based on the total number of nodes and how many it has already processed. Setting g = 0 turns off the reporting.

Note: This option can only be set on the command line and will only affect the completion percentage reported to the output file. Because LVS does not display the verification window when run in batch mode, use of this option is inappropriate for that mode.

Fast Iteration (-i)

This option corresponds to **Fast iteration: consider fanout only** in the setup window (see **Setup Window—Performance** (page 3-167).

The **-i** option instructs LVS to perform a fast iteration. By default LVS considers fanout and element types when performing topological iteration, but specifying **-i** instructs LVS to consider only fanout during this process.

Specifying **-i** increases the speed of the iteration process preparation, where LVS forms the initial element and node classes. When performing a single verification, LVS would normally prompt the user for permission to continue iteration on detection of a mismatch in the element or node count at this point. In batch mode, however, LVS would always continue iteration even on an element or node count mismatch. Therefore, specifying **-i** is inappropriate for batch-mode operation.

List Elements and Nodes (-l*file*)

This option corresponds to **Node and element list** in the setup window (see **Setup Window—File** (page 3-158).

The **-l** option instructs LVS to list the nodes and elements into a file of the specified name. Specify the full path if you wish to create this file in a directory other than the current directory.

Warning: This option will typically create a *very* large output file if the input circuits are even of moderate complexity.

Nonpolarized Elements (-n[rcl])

These options correspond to the following options in the setup window; see **Setup Window—File** (page 3-158):

- **Consider bulk (substrate) nodes during iteration matching**
- **Consider resistors as polarized elements**
- **Consider capacitators as polarized elements**
- **Consider inductors as polarized elements**

The **-n**[**rcl**] option instructs LVS to consider these elements as nonpolarized. If this option is not specified, LVS considers these elements to be polarized; that is, the two terminals of such an element are considered topologically different during the matching process.

The arguments **r**, **c**, and **l** specify which elements LVS is to consider as nonpolarized (**r**=capacitors, **l**=inductors, and **c**=resistors). Specifying **-n** without an additional argument instructs LVS to consider all these elements as nonpolarized; specifying **-nrcl** achieves the same result.

Optimize Network (–O[i])

The **-O** option corresponds to **Optimize network**; the additional option [**i**] corresponds to **Include elements without parameters**. Both options are located in the setup window; see **Setup Window—Advanced Parameters** (page 3-164).

The **-O** option (uppercase **O** required) instructs LVS to optimize the two netlists for parallel and series resistors and capacitors and parallel MOSFETs. Inclusion of the additional condition **[i]** instructs LVS to ignore parameters for the devices.

Without **[i]**:

- Devices without parametric information are not included in the optimization. This can result in fragmentation during the later iteration process.
- Parallel and series resistors and capacitors are collapsed into single devices with recalculated equivalent values for resistance and capacitance.

With **[i]**:

- All parallel MOSFETs are optimized (even though they may have different length parameters), as well as all series and parallel capacitors and resistors.
- Equivalent resistance and capacitance values are not calculated for parallel and series resistors and capacitors.

With [**i**], MOSFET transistors in parallel are collapsed if their length parameters are equal and the width parameters available, or irrespective of their length and width parameters. Without **[i]**, the width of the resulting device will be the sum of the widths of the parallel transistors. With **[i]**, no resulting value is calculated.

If **-O** is specified by itself (without **[i]**), LVS automatically considers parameters for resistance, capacitance, inductance, and L and W for MOSFETs. This is equivalent to specifying **-c12** on the command line. This is done for your convenience so that the recalculated values can be compared.

The optimizer treats the polarity of capacitors and resistors depending on the **-n** option on the command line. If **-n** (nonpolarized treatment of R and C elements) is specified, the following circuit can be optimized in two ways:

```
C1 A B C=30pF
C2 B A C=30pF
R1 A GND 12k
```

It is assumed here that even if this is part of a much larger circuit node, node **B** has only two pins. Doing a series optimization, we can replace **C1** and **C2** with a single capacitor **C3** with an equivalent capacitance of 15 pF:

```
C3 A A C=15 pF
R1 A GND 12k
```

However, with parallel optimization, the two capacitors **C1** and **C2** could just as well be considered to be in parallel, since nodes **A** and **B** are interchangeable on a nonpolar device, with the result:

```
C3 A B C=60pF
R1 A GND 12k
```

Both of these are valid optimization results. With the **-n** option, LVS may use two different approaches to optimization of the two netlists being compared. This will certainly result in fragmentation since the two resulting topologies are completely different. If your circuit contains cases like these, you should not use the **-n** option.

Output file (-o"*file*")

This option corresponds to **Output file** in the setup window; see **Setup Window—File** (page 3-158). The **-o"*file*"** option (lowercase **o** required) creates a separate output file named ***file***.

Note: In batch-mode operations, LVS does not write results to the verification window. Therefore, an output file is required to preserve verification results.

Prematch File (-p"*file*")

This option corresponds to **Prematch file** in the setup window (see **Setup Window—File** (page 3-158)).

The **-p"*file*"** option instructs LVS to equate the elements and nodes listed in the prematch file named ***file*** before beginning the iterative matching process. Specify the full path if this file will not be created in the current directory.

The prematch file is a text file created by the user to equate certain elements and nodes before LVS begins its processing. For further information, see Prematch File Format on page 3-266.

P-SPICE Syntax (-pspice)

This option corresponds to the option **Operate in P-Spice syntax mode** in the setup window.

The **-pspice** option operates LVS in P-SPICE syntax mode. The default syntax mode for input files is H-SPICE. The **-pspice** option must be specified if your files are produced by P-SPICE.

Quiet (-q)

This option is the inverse of **Show information on screen** in the setup window; see **Setup Window—Verbosity Level** (page 3-169).

The **-q** option instructs LVS not to write verification results for individual classes to the screen. This option can save some time during the later processing steps when a lot of information might otherwise be written to the screen. If you have specified an output file, the results written to that file are unaffected by this option.

Note: This option instructs LVS not to display processing information to the verification window. Because LVS does not display the verification window when run in batch mode, use of this option is inappropriate for that mode.

Replace Series Chain MOSFETs (-r[s])

The **-r** option corresponds to **Replace series MOSFETs**, while the [**s**] option corresponds to **Catch permuted MOSFETs**. Both options are located in the setup window.

The **-r**[**s**] option allows LVS to replace series chain MOSFETs with equivalent components, which reduces the processing required. This feature is intended only for fully digital designs, and is not meant for netlists representing analog designs.

The inclusion of the [**s**] flag instructs LVS to catch permuted MOSFETs and identify them for the user.

Verbosity Level (-v[fpar])

These options control output verbosity, or the amount of information displayed on the screen. They correspond to the following options in the setup window; see **Setup Window—Verbosity Level** (page 3-169):

- **Show fragmented classes**
- **Show automorph classes**
- **Show permuted classes**
- **Show detailed processing information (single-pin nodes)**

The **-v**[**fapr**] option instructs LVS to display processing information to the screen. Fragmented classes, permuted classes, automorph classes, and detailed processing information can be displayed using this option. The flags **f**, **a**, **p**, and **r** may be included in any combination, as follows.

f Show fragmented classes.

a Show automorph classes.

p Show permuted classes.

r Show detailed processing information:

- Displays single-connection nodes.
- If including a prematching file (**-p** option), LVS writes the prematched elements to the screen, as well as those elements that the program attempts to postmatch. This is useful for troubleshooting netlists returned as not identical due to fragmentation after automorphism or permutability.
- If including an element description file (**-e** option), LVS identifies which subcircuits it is not flattening (i.e. those that are designated as special elements).

Note: These options instruct LVS to display processing information to the verification window. Because LVS does not display the verification window when run in batch mode, use of these options is inappropriate for that mode.

Yes to All Questions (-y)

The **-y** option corresponds to **Continue on element/node count mismatch**, while the **-y**[**2**] option corresponds to **Detailed trial matching to resolve automorph classes**. Both are located in **Setup Window—Performance** (page 3-167).

The **-y** option automatically answers **Yes** to all program prompts. When LVS is run in batch mode, this option is the default.