

Index

SYMBOLS


? in SPICE netlist, 3-276

NUMERICS

45-degree layout
 design rule checking, 3-74
45-degree objects in generated layers, 1-476

A

abutment ports
 in pad cells, 2-132
 in standard cells, 2-123
abutment ports (SPR)
 in core cells, 2-27
activating drawing tools, 1-253
acute angles, 3-27
add mode, 1-167
adding a macro, 4-7
adding wire sections, 1-272
algorithms, 3-210
aligning objects, (UPILIB)13
anchor point, 1-255
AND operation, 1-444
application parameters, 1-111
approximating curves, 1-276
area utilization, 2-190, 2-192
arrays, 1-429
 creating, 1-429
 editing, 1-431
 flattening, 1-434
ASIC design, 3-231
assisted manual routing (BPR), 2-215
 changing layers, 2-219



defining vias for, 2-218, 2-220
layer cycling, 2-219
setup, 2-199, 2-217
wire tools, 2-198

automatic layer generation, 1-475

automatic placement (BPR)
area utilization, 2-190, 2-192
connectivity weight factor, 2-190, 2-192

automatic routing (BPR)
multiple layers, 2-215
report, 2-214
requirements, 2-197
setup, 2-199

automorph classes, 144, 3-202
detailed trial matching, 3-204
example of detailed trial matching, 3-222
fanout, 3-221
hierarchical information, 3-221
output example, 3-220
parameter matching, 3-205
prematch files, 3-203, 3-204
resolving fragmentation, 3-222

auto-panning, 247

B

batch-file syntax, 3-243

batch files, 185

batch mode, 185

bevel style (wire joins), 1-178

bin size
with DRC, 3-65
with Extract, 3-99
with Generate Layers, 1-470

bin sizing, 3-66


binding macros
to hot keys, 4-27
to menu items, 4-29

BJT
syntax in EXT file, 3-133
syntax in SPICE file, 3-273

block size mismatch, 2-190, 2-192

blocks
defined, 2-151
defining, 2-155
editing operations on, 2-223
routing keep-outs, 2-156
routing ports for, 2-157

Boolean operators for generated layers, 1-444
AND, 1-444



Grow, 1-446
NOT, 1-445, 1-457
OR, 1-445, 1-455
order of operations, 1-447
shrink, 1-446

boxes
drawing, 1-255
editing, 1-281
merging, 1-274
nibbling, 1-274

BPR
assisted manual routing, 2-215
automatic placement, 2-189
automatic routing, 2-197, 2-204
blocks for, 2-155
breakouts, 2-212
defined, 2-145
design flow, 2-8
files required for, 2-154
initialization, 2-173
keep-outs, 2-156
netlist checking, 2-183
placement, 2-187
setup, 2-199
top-level BPR cell, 2-159
top-level I/O cell, 2-160
BPR warnings, 2-184, 2-185, 2-186, 2-187,

2-220
disabling, 2-226
breakouts, 2-209, 2-212
grid, 2-209, 2-212
illustrated, 2-213
setting length, 2-209, 2-212
buffer cells, 2-33, 2-141, 2-143
input ports in, 2-143
butt style (wire ends), 1-178

C

CAP format, 2-323
capacitance, 2-107
calculation (SPR), 2-107
capacitor
syntax in EXT file, 3-128
syntax in SPICE file, 3-270
Cell >
Close As, 1-377
Copy, 1-378
Delete, 1-384, 1-413

- Fabricate, 1-420
- Flatten, 1-434
- Info, 1-414
- Instance, 1-424
- New, 1-371
- Open, 1-373
- Rename, 1-376
- Revert Cell, 1-375
- cell clustering, 2-58
- cell grouping in SPR, 2-58
- cell hierarchy, 1-3, 1-422
 - bottom up, 1-389
 - display, 1-388
 - display, copy to text view, 1-392
 - printing, 1-398
 - top down, 1-388
- cell information, 1-414
- Cell Instance, 1-153
- cell mapping (BPR), 2-180
- cell mapping (SPR), 2-24, 2-39
- cell-cell spacing (SPR), 2-54
- cell-power spacing (SPR), 2-54
- cells, 1-2
 - arrays, 1-429
 - buffer, 2-33
 - chip cell in SPR, 2-84
 - clustering, 2-58
 - copying, 1-378
 - cross-referencing, 1-153
 - deleting, 1-384
 - ground pad, 2-70, 2-135
 - hierarchy of, 1-3, 1-422
 - instanced, 1-422
 - instances of, 1-422, 1-424
 - new, 1-371
 - opening, 1-373
 - renaming, 1-376
 - reverting, 1-375
 - saving, 1-375
 - standard, 2-4
 - tie-to-ground, 2-46
 - tie-to-power, 2-46
- channel base name, 2-47
- channel pitch, 2-52
- chip cells in SPR, 2-84
- CIF, 199
 - calls, 201
 - extensions, 207
 - geometric primitives, 202
 - layers, 205
 - names, 206
 - restrictions, 207
 - scaling, 210
 - symbols, 199

- wires, 209
- CIF files, 185, 191, 194
- CIF format
 - compatible wire styles, 1-181
 - fabrication cell, 1-419
- CIF import options, 188
- circles
 - drawing, 1-256
 - editing, 1-292
- class separations, 3-197
- clear mode, 1-170
- clearing objects on generated layers, 1-474
- clock routing, 2-32
- closing files, 1-54
- clusters (SPR)
 - illustrated, 2-59
- color index, 1-109, 4-430
- color parameters, 1-107
- command line commands
 - !!, 1-316
 - array, 1-317
 - box, 1-320
 - copy, 1-321
 - goto, 1-322
 - instance, 1-322
 - layer, 1-324
 - move, 1-324
 - paste, 1-327
 - path, 1-326
 - polygon, 1-328
 - run, 1-329
 - sc, 1-317
 - text, 1-330
 - width, 1-331
- command line scripting, 1-331
- command-line arguments, 1-16
 - change current directory, 1-17
 - disable file association, 1-17
 - hide splash screen, 1-17
 - ignore configuration, 1-16
 - ignore directory pointer, 1-17
 - ignore registry info, 1-16
 - register without launch, 1-17
- command-line invocation (for LVS), 3-242
- comparing fragmented classes, 3-200
- compiled macros
 - creating, 4-18
 - debugging, 4-31
 - running, 4-13
- compiling the DLL, 4-22
- configuration files, 1-113
 - format, 1-113
- connection
 - defined, 2-151

connection selection, 2-202
connections
 highlighting, 2-200
 selecting, 2-199
connectivity weight factor, 2-190, 2-192
consider parameters (LVS command-line option), 3-246
constraints
 in SPR core generation, 2-97
copying
 cells, 1-378
 objects, 1-362
 to the Windows clipboard, 1-363
copy-protecting macro DLLs, 4-41
core generation
 constraints in SPR, 2-97
 design rules, illustrated, 2-53, 2-54
core with signal ports, illustrated, 2-27
corner pad cells, 2-135
CP statements, 2-161
creating
 arrays, 1-363, 1-429
 compiled macros, 4-18
 files, 1-48
 interpreted macros, 4-14
 layout palette, 4-32
 resources for layout palette, 4-33

critical nets, 2-327
 in SPR, 2-57, 2-331
criticality, 2-57
 in EDIF, 2-331
cross ports, 3-120
cross-coupling, 2-252
cross-section
 with etch, 1-483
 with grow/deposit, 1-483
 with implant/diffuse, 1-484
 operation of, 1-486
 process definition files for, 1-482
 process steps, 1-482
 single-step display, 1-490
curves
 approximating, 1-276
 drawing, 1-264
 straightening, 1-276
customized elements, 3-237

D

daisy chain topology, 2-237

data types, 212

debugging macros

- compiled, 4-31

- interpreted, 4-30

default text size, 1-146

defining generated layers, 1-441

delay calculation in BPR, 2-240

delay calculation report, 2-232, 2-248

deleting

- cells, 1-384

- objects, 1-366

- objects on generated layers, 1-474

- wires, 2-222

- XrefCells, 1-413

density design rules, 3-24

dependent cells, 1-410

deselection

- explicit, 1-347

- hidden, 1-348

- implicit, 1-347

- range, 1-142

- universal, 1-348

design features, 1-4

design file in SPR, 2-19

design flow

- in BPR, 2-8

- in SPR, 2-5, 2-20

design hierarchy, 1-422

Design Navigator, 1-386

design rule checking, 1-4

- 45-degree layout, 3-74

- binning, 3-65

- clearing error markers, 3-79

- correcting errors, 3-75

- density rules, 3-24

- error files, 3-77

- error markers, 3-75

- error objects, 3-75

- error ports, 3-75

- exact width rules, 3-19

- extension rules, 3-23

- finding error markers, 3-78

- generated layers, 3-14

- limitations of, 3-11

- minimum width rules, 3-18

- not exist rules, 3-19

- optimization, 3-81

- overlap rules, 3-21

- performance optimization, 3-81

- region-only check, 3-74

- rule exceptions, 3-25
 - rule lists, 3-14
 - rule sets, 3-12
 - setup, 3-12
 - spacing rules, 3-20
 - surround rules, 3-21
 - types of rules, 3-17
 - write to file, 3-14
- design rule sets
- creating, 3-12
 - editing, 3-12
 - merging, 3-13
 - outputting, 3-15
- design rule types, 3-17
- design rule violations
- clearing, 3-79
 - finding, 3-78
- design rules
- core (SPR), 2-51
 - density, 3-24
 - exact width, 3-19
 - exceptions, 3-25
 - extension, 3-23
 - minimum width, 3-18
 - not exist, 3-19
 - overlap, 3-21
 - pad routing, 2-87
 - spacing, 3-20
 - specifying, 3-69
 - surround, 3-21
- detailed trial matching, 3-204
- example, 3-222
 - output, 3-224
- Details button, 1-41
- diode
- syntax in EXT file, 3-134
 - syntax in SPICE file, 3-273
- display grid, 1-138
- displaying
- selected nets or connections, 2-200
- displaying layout interface elements, 222
- DLL
- compiling, 4-22
 - copy-protecting, 4-41
- documentation conventions, 1-8, 2-9, 3-4, 297
- Draw >
- Add Wire Section, 1-272
 - Curves, 1-276
 - Flip, 1-360
 - Group, 1-353
 - Merge, 1-274
 - Move By, 1-359
 - Nibble, 1-275
 - Nudge, 1-358

Pick Layer, 1-252
Rotate, 1-360
Slice, 1-273
Ungroup, 1-354
drawing
 automatic selection, 1-143
 boxes, 1-255
 circles, 1-256
 curves, 1-264
 objects, 1-255
 pie wedges, 1-256
 polygons, 1-257
 ports, 1-268
 rulers, 1-269
 tori, 1-257
 wires, 1-257
drawing objects, 1-422
Drawing toolbar, 1-31
drawing tools, 1-253
DRC
 bin sizing, 3-66
DRC rules
 Hole, 1-452
 inside, 1-452
 outside, 1-452
driver model information, 2-252
driving force, 2-61

duplicating objects, 1-362
dynamic link library, 4-23
dynamic-link library, 4-7

E

edge selection, 1-340, 2-189
EDIF format, 2-326
Edit >
 Clear, 1-366
 Clipboard, 1-363
 Copy, 1-362
 Cut, 1-366
 Deselect All, 1-348
 Edit In-Place, 1-432
 Edit Object(s), 1-277
 Find, 1-349
 Find Next, 1-351
 Find Previous, 1-351
 Paste, 1-364
 Paste to Layer, 1-364
 Redo, 1-368

- Select All, 1-346
- Undo, 1-367
- Edit > Goto, 176
- editing
 - boxes, 1-281
 - circles, 1-292
 - edit range, 1-142
 - graphical, 1-270
 - multiple objects, 1-279
 - objects in place, 1-432
 - objects using a macro, (UPILIB)13
 - polygons, 1-284, 1-286
 - ports, 1-298
 - rulers, 1-301
 - textual, 1-277
 - wires, 1-290
- effective channel pitch, 2-52
- electrical models, 2-231, 2-325
- electrically connected objects
 - defined, 2-151
 - editing, 2-222, 2-223
- element description file
 - format, 3-261
- element description file (LVS command-line option), 3-248
- element description file, example, 3-237
- Elmore delay, 2-114
- error files, 3-77
- error objects, 3-65, 3-75
- error ports, 3-64, 3-75
- error recovery, 1-6
- errors
 - design rule checking, 3-75
- exact width design rules, 3-19
- exchanging views, 248
- exporting files, 191
 - CIF, 191, 194
 - GDSII, 191, 195
- extend style (wire ends), 1-178
- extension design rule, 3-23
- extension design rules, 3-23
- external subcircuit models, 2-231
- Extract
 - General, 3-98
 - Output, 3-101
 - Subcircuit, 3-105
- extract definition file
 - comments, 3-124
 - connections, 3-124
 - devices, 3-126
 - format, 3-263
- extract definition files, 3-88
- extraction
 - capabilities defined, 3-84

- configuring, 3-86
- defining capacitance for resistors and capacitors, 3-87
- defining devices and connections, 3-86
- subcircuit recognition, 3-109

F

- fabrication cell, 1-419
- fanout, 3-221
- fast iteration (LVS command-line option), 3-249

File >

- Close, 1-54
- Exit, 1-80
- Export Mask Data, 191
- Export Setup, 1-88
- Import Mask Data, 185
- Info, 1-68
- New, 1-48
- Open, 1-50
- Print, 1-58

- Print Preview, 1-66
- Print Setup, 1-62
- Replace Setup, 1-82
- Save, 1-55
- Save As, 1-55

file formats

- CAP, 2-107, 2-323
- CIF, 199
- EDIF, 2-326
- element description file, 3-261
- extract definition file, 3-263
- GDSII, 211
- INI, 1-113
- LVS output file, 3-264
- node and element list file, 3-268
- prematch file, 3-266
- SDF, 2-113, 2-334
- SPICE file, 3-270
- TDB, 1-57
- TPR, 2-337
- TTX, 1-90
- XST, 1-492

file information

- accessing, 1-68

file locking, 148

file parameters, 1-145

files, 1-47

closing, 1-54
 creating, 1-48
 exiting, 1-80
 exporting, 191
 formats, 1-5
 importing, 185
 new, 1-48
 opening, 1-50
 saving, 1-55
 startup, 1-15
 Find Next/Find Previous, 1-351
 finding objects, 1-349
 flattening hierarchy, 1-434
 Flip/Rotate commands, 1-360
 floorplans, 1-4
 fragmented classes, 3-199

- comparing, 3-200
- output, 3-199, 3-229
- resolving, 3-231

 fringe capacitance

- in capacitance file, 2-109
- in SDF file, 2-115

G

GaASFET

- syntax in EXT file, 3-135, 3-136

 GDI resources, 1-24
 GDII export options, 1-153
 GDII data type, 215

- assignment of, 215, 1-365
- for ports, 1-300
- layer setup, 1-159

 GDII files, 185, 191, 195
 GDII format, 211

- compatible wire styles, 1-181
- data types, 212
- wires, 217

 GDII import options, 189
 GDII number, 1-159
 GDII properties

- editing, (UPILIB)2

 generated layers, 1-436

- 45-degree objects and, 1-476
- AND operation, 1-444
- Boolean operations, 1-444
- defining, 1-441
- design rule checking, 3-14
- for DRC and Extract, 1-475

Grow operation, 1-446
 NOT operation, 1-445, 1-457
 OR operation, 1-445, 1-455
 removing generated layers, 1-474
 showing and hiding, 1-473
 shrink operation, 1-446
 global input signal routing, 2-32, 2-96
 cell design for, 2-141
 illustrated, 2-35
 global signal buses, 2-32
 global signal ports, 2-32, 2-141
 global signal rail, 2-34
 Goto, 248, 176
 granularity (LVS command-line option), 3-248
 graphical editing, 1-270
 graphical repositioning, 1-356
 grid
 parameters, 1-138
 ground pad cell, 2-70, 2-130, 2-135
 ground rail width, 2-64
 ground signal
 in SPR, 2-38
 grouping objects, 1-353
 Grow operation, 1-446

H

header files (for UPI), 1-123, 4-8, 4-11
 Help, 1-22
 Help >
 About L-Edit, 1-23
 hiding
 generated layers, 1-473
 insides, 239
 layers, 230
 objects, 224
 hierarchical information in automorph classes,
 3-221
 hierarchical lock/unlock, 1-395
 hierarchy, 1-3
 highlight mode, 2-200, 2-203
 hot keys
 binding macros to, 4-27

I

I/O signals
 in EDIF, 2-330
 of SPR core, 2-66, 2-330
ignore bulk nodes (LVS command-line option), 3-245
importing files, 185
 CIF, 185
 GDSII, 185
include files, 4-11
incremental repositioning, 1-358
indent middle rows, 2-98, 2-102
indent ratio, 2-102
inductor
 syntax in EXT file, 3-132
 syntax in SPICE file, 3-270
INI format, 1-113
initialization (BPR), 2-173
 changes requiring re-initialization, 2-184
 re-initializing, 2-186
 requirements, 2-154
initializing setup
 SPR, 2-43
input file types, 147
inside, 1-452

insides
 hiding, 239
 showing, 239
instance caching, 1-24
instanced cell, 1-422
instances, 1-3, 1-422
 arrays of, 1-429
 creating, 1-424
 editing, 1-431
 flattening, 1-434
interconnect model information, 2-252
internal units, 1-130
interpad connections, 2-132
interpreted macros
 creating, 4-14
 debugging, 4-30
 running, 4-12

J

JFET
 syntax in EXT file, 3-137

syntax in SPICE file, 3-273

K

keep-outs

defined, 2-151

routing, 2-156, 2-208

keyboard assignments

writing to a configuration file, 1-121

keyboard settings

Setup Application, 1-119

L

label nodes with ports, 2-101, 2-107

lambda-based design, 1-6

LAmbiguousFillType, 4-575

launching L-Edit, 1-15

launching LVS, 146

layer setup, 1-83

import and exporting, (UPILIB)9

saving, (UPILIB)7

layer spacing

in core routing, 2-53

in pad routing, 2-89

layer-cell spacing (SPR), 2-53

layer-core spacing (SPR), 2-53

layer-pad spacing (SPR), 2-53

layers

adding, 1-157

CIF names, 206

hiding, 230

locking, 1-38, 1-356, 1-474

setup, 1-155

showing, 230

layer-to-layer capacitance, 2-47

layout area, 1-44

layout files

in SPR, 2-20

layout palette

creating, 4-32

creating resources for, 4-33

layout style (wire joins), 1-178

leaf-level, 239

L-Edit

building blocks, 1-2
 features, 1-2, 1-8, 2-9, 3-4, 297
 L-Edit command menus, 1-20
 Cell, 1-20, 508
 Draw, 1-20, 506
 Edit, 1-20, 500
 File, 1-20, 498
 Help, 1-21, 512
 Setup, 1-20, 509
 Tools, 1-21, 510
 View, 1-20, 502
 Window, 1-21, 511
 L-Edit program icon, 1-15
 library files, 1-153
 list elements and nodes (LVS command-line option), 3-250
 locator, 1-42
 coordinate system, 1-138
 units, 1-42, 1-140
 locking nets, 2-229
 log files (for UPI), 1-123, 4-8
 logo generation, (UPILIB)11
 LVS
 algorithms, 3-210
 limitations, 3-210
 output, 3-216
 LVS output file format, 3-264

M

Macro dialog, 4-3
 macro dialog
 adding, 4-7
 macros, 295
 adding, 4-7
 manual placement
 in SPR, 2-58
 mapping cells and ports (BPR), 2-180
 mapping cells and ports (SPR), 2-24, 2-39
 mapping table (BPR), 2-180
 mapping table (SPR), 2-24, 2-39
 maximum geometrical difference (LVS command-line option), 3-247
 maximum value difference (LVS command-line option), 3-247
 memory limits, 1-5
 MEMS design example, 3-237
 menu bar, 1-20
 menu items
 binding macros to, 4-29
 menus, 151–153
 merging objects, 1-274
 MESFET
 syntax in EXT file, 3-135, 3-136

syntax in SPICE file, 3-273
minimum bounding box, 1-314
 defined, 2-151
minimum spanning tree topology, 2-235
minimum width design rules, 3-18
mirror ports, 2-139
mirroring, 2-136
miter style (wire joins), 1-178
Mode Setup dialog, 4-6
model definition files
 in time domain simulation, 2-255
MOSFET
 syntax in EXT file, 3-139
 syntax in SPICE file, 3-273
MOSFETs
 permuted classes, 3-231
mouse buttons bar, 1-42
mouse snap grid, 1-138, 3-67
Mouse Wheel Functions, 247
Move By, 1-359
moving
 objects, 1-356
multiple object editing, 1-279

N

net criticality
 in EDIF, 2-331
 in SPR, 2-57
net delay
 calculation (SPR), 2-119
 model formula (SPR), 2-114
 syntax, 2-335
net length in SPR, 2-323
net length reduction, 2-100
net selection, 2-202
netlist browser, 2-227
netlist comparison, 3-195
 resolving discrepancies, 3-213
Netlist Navigator, 2-227
netlists
 CP statements, 2-161
 EDIF format, 2-24, 2-326
 mapping (BPR), 2-180
 mapping (SPR), 2-24, 2-39
 synchronizing with design, 2-156, 2-180, 2-183
 time domain simulation output, 2-252
 TPR format, 2-337
nets

locking, 2-229
selecting, 2-202
nibbling objects, 1-274
nodal capacitance, 2-47
files, 2-107, 2-323
nodal properties, 2-107
node and element list file, 3-268
node labeling, 3-89
nonpolarized elements (LVS command-line op-
tion), 3-250
not exist design rules, 3-19
NOT operation, 1-445, 1-457
Nudge commands, 1-358
nudging, 1-358
number of rows, 2-98
numerical repositioning, 1-359

O

objects

boxes, 1-250
circles, 1-250

copying, 1-362
deleting, 1-366
deselecting, 1-347
drawing, 1-255
duplicating, 1-362
finding, 1-349
grouping and ungrouping, 1-353
hiding, 224
instances, 1-251
moving, 1-356, (UPILIB)13
pasting, 1-364
pie wedges, 1-251
polygons, 1-250
ports, 1-251
reorienting, 1-360
repeated copying, 1-363
resizing and reshaping, 1-270
rulers, 1-251
selecting, 1-334
showing, 224
slicing, 1-273
tori, 1-251
types, 1-250
wires, 1-250
opening
cells, 1-373
files, 1-50

optimization (SPR)
 factor, 2-104
 in placement, 2-103
 in routing, 2-100
optimize network, 3-227, 3-232
optimize network (LVS command-line option),
 3-251
optimizing design rule checking, 3-81
OR operation, 1-445, 1-455
origin, 1-44
OTC routing (SPR), 2-47, 2-49
output
 automorph class example, 3-220
 detailed trial matching, 3-224
 fragmented class, 3-229
 MEMS design example, 3-237
 parameter matching example, 3-218
 parsing, 3-216
output file (LVS command-line option), 3-253
output file types, 147
overlap capacitance (SPR), 2-109
overlap design rules, 3-21
over-the-cell routing (SPR), 2-47, 2-49

P

pad cell abutment ports, 2-70, 2-132
pad cell mirror ports, 2-70, 2-139
pad cells, 2-132
 without bond pads, 2-136
 corner, 2-135
 naming and ordering, 2-76
 orientation, 2-136
pad contact layer, 2-86
pad route design rules
 illustrated, 2-89
pad routing
 to a core, 2-26
 to a padframe, 2-29
pad via, 2-90
padframe
 dimensions, 2-73
 illustrated, 2-30
 pad name requirements, 2-76
 ports, 2-29, 2-70
 routing, 2-29
 setup, 2-68
padframe generation
 with netlist, 2-31
 without netlist, 2-31

padlist, 2-73
panning, 244
parameter matching, 3-205, 3-218
parasitic capacitance, 3-271
parsing, 3-216
paste buffer, 1-364
Paste to Cursor, 1-365
pasting objects, 1-364
performance settings, 1-128
permuted classes, 3-207–3-209, 3-231
pie wedges
 drawing, 1-256
pin types
 defining, 2-232
 editing, 2-231
pin-to-pin delay
 calculation (SPR), 2-118
 model formula, 2-113
 syntax, 2-334
placement (BPR), 2-187
 automatic, 2-189, 2-190
 preservation, 2-183
placement (SPR), 2-55
polygons
 adding vertices, 1-272
 drawing, 1-257
 editing, 1-284, 1-286

 integrity checking, 3-67
 merging, 1-274
 nibbling, 1-274
port construction
 illustrated, 3-118
port mapping
 in BPR, 2-180
 in SPR, 2-39, 2-41
port text size
 in GDSII format, 219
 scaling, (UPILIB)5
ports
 definitions for global signals, 2-141
 drawing, 1-268
 editing, 1-298
 mapping (BPR), 2-180
 mapping (SPR), 2-39, 2-41
postiteration matching, 3-204
power pad cells, 2-135
power ports, 2-123
 in pad cells, 2-132
 in standard cells, 2-123
power rail width, 2-64
power rails, 2-124
power signal
 in SPR, 2-38
power supply pads, 2-135

predefined setup files, 1-49
prematch file, 3-204
 format, 3-266
 LVS command-line option, 3-254
 preiteration matching, 3-203
prematch files
 input, 3-225
 output, 3-226
 resolving fragmentation of an automorph
 class, 3-222
primitives, 1-3, 1-422
printing, 1-58
 hard copy, 1-6
printing cell hierarchy, 1-398
process definition files, 1-482, 1-492
process steps
 etch, 1-483
 grow/deposit, 1-483
 implant/diffuse, 1-484
program icon, 1-15
properties, 1-70
 adding properties, 1-76
 deleting properties, 1-77
 deleting values, 1-78
 editing properties, 1-71
 editing values, 1-78
 GDSII, (UPILIB)2

 renaming properties, 1-77
 viewing properties, 1-71
Properties dialog, 1-73
property tokens, 3-94
P-SPICE syntax (LVS command-line option),
 3-254

Q

quiet (LVS command-line option), 3-255

R

receiver model information, 2-252
recognition layer, 3-89, 3-92, 3-93, 3-126,
 3-131
Redo, 1-368
redo buffer, 1-368

- reference points, 1-314
- refreshing the screen, 241
- region-only design rule checking, 3-74
- renaming cells, 1-376
- rendering
 - color, 1-173
 - layers, 1-161, 1-166
 - modes, 1-163, 1-165
 - outlines, 1-175
 - passes, 1-163, 1-172
 - patterns, 1-172
- reorienting objects, 1-360
- repeated copying, 1-363
- replace series chain MOSFETs (LVS command-line option), 3-255
- repositioning
 - incremental, 1-358
 - numerical, 1-359
- repositioning, graphical, 1-356
- rescaling, 1-131
- resistor
 - syntax in EXT file, 3-130
 - syntax in SPICE file, 3-270
- resizing and reshaping objects, 1-270
- resolving
 - discrepancies, 3-213
 - fragmentation of an automorph class, 3-222
 - with prematch files, 3-223
 - fragmented classes, 3-231
- resolving verification errors, 3-199, 3-213
- restoring, (UPILIB)7
- Rotate/Flip commands, 1-360
- round style (wire ends and joins), 1-178
- routing
 - blocks, 2-156
 - clock signals, 2-32
 - keep-outs, 2-156, 2-208
 - over-the-cell, 2-47, 2-49
 - three-layer, 2-47
 - topologies, 2-232, 2-234
- routing guides, 2-188
 - defined, 2-152
 - display in assisted manual routing, 2-215
 - editing, 2-189
 - hiding display, 2-230
 - selecting, 2-189
- routing layers
 - changing, 2-219
 - defining, 2-204
- routing ports (BPR)
 - defined, 2-152
 - defining for blocks, 2-157
 - external, 2-161

labeling, 2-158
placement, 2-158
routing topologies, 2-235
 daisy chain, 2-237
 minimum spanning tree, 2-235
 star, 2-236
routing wires
 deleting (BPR), 2-221
 editing operations on (BPR), 2-224
 in standard cells, 2-127
 in standard cells (SPR), 2-127
row base name, 2-47
row crosser cells, 2-102, 2-128, 2-130
row crosser ports, 2-46, 2-128, 3-120
row indent ratio, 2-102
row length, 2-98
RUL files, 3-15
rule exceptions, 3-25
rule lists, 3-14
rule sets, 3-12
rule types, 3-17
rulers
 drawing, 1-269
 editing, 1-301
running
 compiled macros, 4-13
 interpreted macros, 4-12

LVS batch files, 3-244

S


saving
 cells, 1-375, (UPILIB)4
 files, 1-55
SDF calculation, 2-114
SDF format, 2-113, 2-334
selecting and deselecting
 blocks, 2-203
 cycle selection, 1-340
 deselecting objects, 1-347
 edge, 1-340
 electrically connected objects, 2-222
 explicit deselection, 1-347
 explicit selection, 1-335
 extend selection, 1-340
 hidden deselection, 1-348
 implicit deselection, 1-347
 implicit selection, 1-339
 instances, 2-203

nets or connections, 2-199
 nets, using routing guides, 2-189
 selecting objects, 1-334
 selection range, 1-142
 universal deselection, 1-348
 universal selection, 1-346
selecting drawing tools, 1-252
selecting layers, 1-252
selection
 cycle, 1-340
 edge, 1-340
 explicit, 1-335
 extend, 1-340
 implicit, 1-339
 universal, 1-346
selection box, 1-117
self-intersecting polygons, 3-67
separation into classes, 3-197
set mode, 1-167
Setup >
 Application, 1-111
 General, 1-115
 Keyboard, 1-119
 UPI, 1-123
 Warnings, 1-122
 Design, 1-130
 Curves, 1-148

 Drawing, 1-145
 Grid, 1-138
 Selection, 1-141
 Technology, 1-134
 Xref files, 1-151
Layers, 1-156, 1-437
 General, 1-158
 Rendering, 1-161
 Palette, 1-107
 Special Layers, 1-182
Setup > Design—Xref files, 1-153
setup information
 design rule check, 3-12
Setup Layers
 General, 206
setup window, 156
 Advanced Parameters, 164
 File, 158
 Options, 161
 Performance, 167
 Verbosity Level, 169
shortcut keys
 writing to a configuration file, 1-121
showing
 generated layers, 1-473
 insides, 239
 layers, 230


objects, 224
shrink operation, 1-446
signal integrity analysis, 2-252
signal ports, 2-135
 on core cells, 2-26
 global, 2-32, 2-141
 illustrated, 2-126
 in pad cells, 2-135
 on padframes, 2-29
 in standard cells, 2-124
signal types, 2-176, 2-230, 2-233
 excluding from routing, 2-233
skew in delay calculation, 2-249
slew rates, 145
slicing objects, 1-273
snapping cursor, 1-140
spacing design rules, 3-20
Special Layers Setup, 1-182
special standard cells, 2-130
specialized elements, 3-237
specifying
 design rules, 3-69
SPICE commands
 .END, 3-285
 .GLOBAL, 3-283
 .INCLUDE, 3-281
 .MODEL, 3-281

 .OPTION, 3-284
 .PARAM, 3-284
 .SUBCKT, 3-279
SPICE file, 3-270
SPICE file format
 comment lines, 3-287
 parameter values, 3-285
 passive elements, 3-270
 restrictions, 3-288
 subcircuit instances, 3-277
SPICE OUTPUT properties, 3-94
 example, 3-96
SPR
 defined, 2-17
 design files, 2-19
 design flow, 2-5, 2-20
 design tips, 2-24
 files required for, 2-19
 initializing setup, 2-43
 procedure outlined, 2-20
 setup, 2-36
 technology setup, 2-19
SPR Core Setup
 Design Rules, 2-51
 General, 2-45
 Global Signals, 2-59
 I/O Signals, 2-64



Layers, 2-47
Placement, 2-55
Power, 2-63
SPR layout files, 2-20
SPR Pad Route Setup, 2-81
 Core Signals, 2-91
 Design Rules, 2-87
 General, 2-84
 Layers, 2-85
 Padframe Signals, 2-93
SPR Padframe Setup
 General, 2-69
 Layout, 2-72
SPR Place and Route, 2-95
stacked vias, 1-164
 rendering, 1-164
standard cells, 2-123
 libraries, 2-122
 special, 2-130
standard delay format files, 2-334
Standard toolbar, 1-26
star topology, 2-236
starting L-Edit, 1-15
startup files, 1-15
status bar, 155
status bar (L-Edit), 1-40
straightening curves, 1-276

subcircuit
 syntax in EXT file, 3-141
 syntax in SPICE file, 3-277
subcircuit cell design, 3-111
subcircuit connection ports
 illustrated, 3-116
subcircuit models, 2-253, 2-255
subcircuit recognition, 3-109
 activation, 3-110
 cell design for, 3-111
 connection ports, 3-112
 connections, 3-114
 cross ports, 3-120
subcircuit recognition layer, 3-106, 3-111
subcircuit recognition polygons, 3-111
 as keep-outs, 2-157
 defined, 2-152
 illustrated, 3-115
subtract mode, 1-170
surround design rules, 3-21



T

Tanner Place and Route format, 2-337

TDB format, 1-57

technology setup

in SPR, 2-19

technology units, 1-130

text files

creating, 172

editing, 173

opening, 172

searching, 174–176

text window, 171

textual descriptions of objects, 1-41

textual editing, 1-277

three-layer routing, 2-47, 2-48

tie-to-ground cell, 2-46, 2-130

tie-to-power cell, 2-46, 2-130

time domain simulation, 2-241, 2-252

toolbars, 153–155

Drawing, 1-31

Locator, 1-42

Tools >

BPR

Automatic Placement, 2-191

Initialization, 2-174

Netlist Navigator, 2-227, 2-228

Route All, 2-204

Route Selected, 2-204

Setup, 2-201, 2-206, 2-217

Signal Integrity, 2-250

Timing Analysis, 2-243

Unroute All, 2-204

Unroute Selected, 2-204

Clear Error Layer, 3-79

Clear Generated Layers, 1-474

Cross-Section, 1-487

DRC

Setup Design Rules, 3-69

DRC Box, 3-62

Extract, 3-97

General, 3-98

Output, 3-101

Subcircuit, 3-105

Generate Layers, 1-469

Macro, 4-3

SPR

Place and Route, 2-95

Setup, 2-36

Summary, 2-22

Workgroup >

Examine XrefCell Links, 1-401

Tools > DRC, 3-62

Tools > DRC Box, 3-62

Tools > Macro, 4-4

top-level BPR cell, 2-146, 2-159

defined, 2-153

top-level I/O cell, 2-146, 2-160, 2-177

defined, 2-153

designs without, 2-171

illustrated, 2-170

in schematic, 2-266

initializing, 2-160

in schematic, 2-161, 2-162

topological matching, 3-198

topologies, 2-232, 2-234

daisy chain, 2-237

minimum spanning tree, 2-235

star, 2-236

tori

drawing, 1-257

TPR format, 2-337

transmission line

syntax in SPICE file, 3-270

TTX format, 1-90

tutorial, 188–194

U

undoing operations, 1-367

ungrouping objects, 1-353

UPI

include files, 4-11

UPI header files, 4-11

UPI library

See UPILIB

UPI operating modes, 4-6

UPILIB

Alignment Toolbar, (UPILIB)13

GDS Properties, (UPILIB)2

Importing and Exporting Layer Settings,
(UPILIB)9

Layer Manager, (UPILIB)7

Logo Generator, (UPILIB)11

Save Cell to File, (UPILIB)4

Text Resize, (UPILIB)5

user files, 1-114

user interface, 149–183

user-programmable interface, 295

V

- variable grid, 1-6
- .vdb files, 147
 - examples, 3-215
- Vdd pad cells, 2-135
- verbosity level (LVS command-line option), 3-256
- verification errors, 3-199, 3-213
- verification options, 3-245–3-258
- verification queue, 181–183
- verification window, ??–180
- vertices
 - limitations on, 198
- vertices, adding, 1-272
- via minimization (BPR), 2-209
- via model information, 2-252
- via reduction
 - in BPR, 2-209
 - in SPR, 2-100
- via surrounds (SPR), 2-53
- via widths (SPR), 2-53
- vias
 - editing operations on, 2-225
- View >
 - Design Navigator, 1-386
 - Display, 222
 - Exchange, 248
 - Goto, 248
 - Hierarchy Level >
 - Show one less level, 238
 - Show one more level, 238
 - View hierarchy level, 238
 - Home, 242
 - Insides, 239, 240
 - Layers, 231
 - Layers >
 - Hide Generated, 1-473
 - Show Generated, 1-473
 - Objects, 225
 - Pan >
 - Down, 244
 - Left, 244
 - Right, 244
 - To Cell Edge, 245
 - To Selections, 244
 - Up, 244
 - Redraw, 241
 - Toolbars, 1-26
 - Zoom >
 - In, 242
 - Mouse, 245
 - Out, 242

View > Status Bars, 1-39

viewing

- layout hierarchy, 238

- selected nets or connections, 2-200

views

- exchanging, 248

- panning, 244

- zooming, 242

W

winding number, 1-263

Window >

- Arrange Icons, 1-22

- Cascade, 1-21

- Close All Except Active, 1-22

- (open window list), 1-22

- Tile Horizontally, 1-21

- Tile Vertically, 1-22

window stretch editing, 1-272

windows

- arranging, 1-21

Windows clipboard

- copying to, 1-363

wire widths

- in core routing, 2-53

wires

- adding sections, 1-272

- adding vertices to, 1-272

- CIF-compatible styles, 1-181

- default styles, 1-181

- drawing, 1-257

- editing, 1-290

- end styles, 1-178

- end styles in automatic routing, 2-156

- GDSII-compatible styles, 1-181

- join styles, 1-178

- merging, 1-274

- nibbling, 1-274

- terminology, 1-176

- width, 1-176

workgroup files, 1-114

write CAP file, 2-101, 2-107, 2-323

write SDF file, 2-101, 2-113, 2-334

X

Xref file, 1-153

XrefCells, 1-153, 1-399

- changing the referenced cell, 1-406

- dependent cells, 1-410

- examining, 1-401

- unlinking, 1-409

- updating, 1-407

XrefCells, deleting, 1-413

XST format, 1-492

Z

zoom/selection box, 1-117

zooming, 242

Y

yes to all questions (LVS command-line option), 3-257