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Project title: A comparison of Asynchronous and Synchronous Digital Design Methods
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Asynchronous circuits don't have clocks; their proper functioning does not depend on the requirement that delay between logic layers is bounded by a fixed (clock) interval. An ideal asynchronous circuit would be completely insensitive to its component delays - it only guarantees that computations occur in correct order and that operations start only after all its dependencies are available. Several attempts have been made to popularize the asynchronous paradigm for commercial processors ([1], [2], [3]). Some commercial asynchronous systems have come up recently to work around the power wall [4].

This project explores the various options available to the circuit and system designer when making an asynchronous system. I plan to implement an complete in-order Asynchronous MIPS processor, and compare it to a synchronous implementation on area, power and (average) delay. If time permits, I want to study some theoretical aspects of the topic. For instance, asynchronous circuits are proved to consume power bounded by a constant factor of the entropy of the circuit specification [5]. Similar results on power and elasticity gives a rigorous framework for developing low-power circuits.

(Possibly Quasi-) Delay-insensitive circuits have been modeled as parallel and Communicating Sequential Processes [6]. The first part of the project will be to learn a similar formalism of Communicating Hardware Processes and describe the minimal MIPS processor.

The second part will be to synthesize and prepare the layout of the asynchronous and synchronous processor. Several tools exist for Asynchronous digital circuits (such as BEEST [7] and CellTK [8]).

The third (final) part will be to optimize the digital designs on delay, area and power metrics. Three versions of the processor is planned: completely synchronous, globally synchronous locally asynchronous (GSLA, within modules), completely asynchronous. GSLA can be useful for easier design and interfacing components of a large system but lower power overall.

The main advantages of an asynchronous circuit is savings on power due to the absence of a clock tree. Dynamic load scheduling and throttling are handled automatically due to its time-less nature. It is also inherently robust to transient variations in temperature and crosstalk. The main disadvantages are that they are harder to design, test and verify (no timing guarantees) and may need additional circuits in large systems for handshaking and consistency.

The principal motivation for this project is to study and observe these trade-offs.

References:

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