# Treball Final de Grau PAC2

**David Soler Bartomeu** 



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Universitat Oberta de Catalunya



# Introduction

In this PAC the executable file shows the creation of a window, de display of debug information and the processing of input by the user.

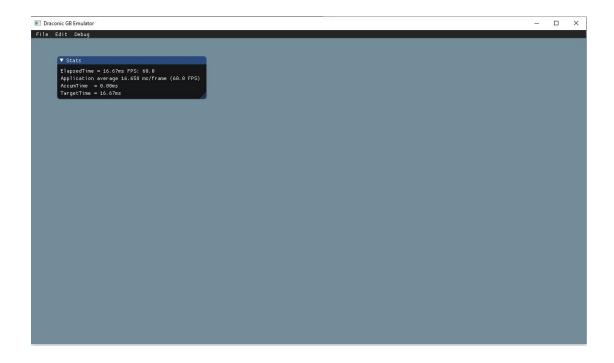
An emulator is incredibly different from a video game so in this case there is no gameplay showcased in this deliverable. The main focus of the PAC2 has been the research and gathering of information regarding Game Boy emulator development.

The development will be performed using Visual Studio Community 2019, so downloading the repo and compiling using it will be able to generate a valid executable.

Repository: <a href="https://github.com/solbarda/draconic-gb">https://github.com/solbarda/draconic-gb</a>
Explanation Video: <a href="https://youtu.be/SyZu82L3W38">https://youtu.be/SyZu82L3W38</a>

# **Execution**

The deliverables will always be on the "Entregables" folder on the root of the repo. The emulator can be run by running the 'DraconicGB.exe' program found in the folder 'Executable'. Running the program should open up a window. The window is created using SDL and the menus displayed have been created using occurred imGUI.



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# References

The following references have been used in order to gather information about the emulator as well as on how to correctly create a windows program with a user interface.

#### https://gbdev.io/pandocs/

#### Memory Map

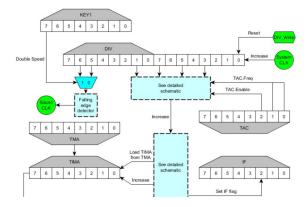
The Game Boy has a 16bit address bus, that is used to address ROM, RAM and I/O

Gener	al Mer	nory Map	
Start	End	Description	Notes
0000	3FFF	16KB ROM bank 00	From cartridge, usually a fixed bank
4000	7FFF	16KB ROM Bank 01~NN	From cartridge, switchable bank via MB (if any)
8000	9FFF	8KB Video RAM (VRAM)	Only bank 0 in Non-CGB mode Switchable bank 0/1 in CGB mode
A000	BFFF	8KB External RAM	In cartridge, switchable bank if any
C000	CFFF	4KB Work RAM (WRAM) bank 0	
D000	DFFF	4KB Work RAM (WRAM) bank 1~N	Only bank 1 in Non-CGB mode Switchable bank 1~7 in CGB mode
E000	FDFF	Mirror of C000~DDFF (ECHO RAM)	Typically not used
FE00	FE9F	Sprite attribute table (OAM	
FEA0	FEFF	Not Usable	
FF00	FF7F	I/O Registers	
FF80	FFFE	High RAM (HRAM)	
FFFF	FFFF	Interrupts Enable Register (IE)	

## https://github.com/AntonioND/giibiiadvance/blob/master/docs/TCA GBD.pdf

#### 5. Timer

The Game Boy timer subsystem is composed by the three timer registers (TIMA, TMA and TAC), and the DIV register. This is a simplified schematic:





### https://gekkio.fi/files/gb-docs/gbctr.pdf



# PROGRAMMING MANUAL Version 1.1

#### https://gbdev.io/gb-opcodes/optables/

@ Game Boy CPU (SM83) instruction set (JSON)

_			,			,					,					
	x0	x1	ж2	x3	×4	ж5	ж6	x7	x8	x9	xA	xВ	жC	хD	хE	хF
0x	NOP 1 4	LD BC, d16 3 12	LD (BC), A 1 8	1 8	INC B 1 4 Z 0 H -	DEC 8 1 4 Z 1 H -	LD B, d8 2 8	RLCA 1 4 0 0 0 C	LD (a16), SP 3 20	ADD HL, BC 1 8 - 0 H C	LD A. (8C) 1 8	DEC BC 1 8	INC C 1 4 Z 0 H -	DEC C 1 4 Z 1 H -	LD C, d8 2 8	RRCA 1 4 0 0 0 C
1x	5TOP 1 4	LD DE d16 3 12	LD (DE), A 1 8	1 8	INC D 1 4 2 0 H -	DEC D 1 4 Z 1 H -	LD D, d8 2 8	RLA 1 4 0 0 0 C	JR r8 2 12	ADD HL DE 1 8 - 0 H C	LD A. (DE) 1 8	DEC DE 1 8	INC E 1 4 2 0 H -	DEC E 1 4 Z 1 H -	LD E. d8	RRA 1 4 000C
2x	JR NZ, r8 2 12/8	LD HL d16 3 12	LD (HL+), A 1 8	INC HL 1 8	INC H 1 4 Z 0 H -	DEC H 1 4 Z 1 H -	LD H, d8 2 8	DAA 1 4 Z - 0 C	JR Z, r8 2 12/8	ADD HL, HL 1 8 - 0 H C	LD A. (HL+) 1 8	DEC HL 1 8	INC L 1 4 2 0 H -	DECL 1 4 Z 1 H -	LD L, d8 2 8	CPL 1 4 -11-
3x	JR NC, r8 2 12/8	LD SP, d16 3 12	LD (HL-), A 1 8	INC SP 1 8	INC (HL) 1 12 Z 0 H -	DEC (HL) 1 12 Z 1 H -	LD (HL), d8 2 12	SCF 1 4 -001	JR C, r8 2 12/8	ADD HL SP 1 8 - 0 H C	LD A, (HL-) 1 8	DEC SP 1 8	INC A 1 4 Z 0 H -	DEC A 1 4 Z 1 H -	LD A, d8 2 8	CCF 1 4 -00 C
4x	LD 8. 8 1.4	LD 8. C	1 4	LD 8. E 1.4	LD 8. H 1.4	1 4	LD 8. (HL) 1 8	LD 8. A 1.4	LD C. 8 1.4	14	LD C. D 1 4	14	1 4	14	LD C. (HL) 1 8	1 4
5x	LD D, B 1.4	LD D, C 1.4	LD O, D 1.4	LD D, E 1 4	LD D, H 1 4	LD D, L 1 4	LD D. (HL) 1 8	LD D, A 1 4	LD E. B 1.4	LD E, C 1.4	LD E.D 1.4	LD E. E 1.4	LD E H 1 4	1 4	LD E. (HL) 1 8	LD E.A.
6x	LD H, B 1 4	LD H, C 1 4	LD H, D 1 4	LD H, E 1 4	LD H, H 1 4	LD H, L 1 4	LD H, (HL) 1 8	LD H. A 1 4	LD L, B 1 d	LD L, C 1 4	LD L, D 1 4	1 d	LD L, H 1.4	10 L L	LD L, (HL) 1 8	LD L A 1 4
7x	LD (HL), 8 1 8	LD (HL), C 1 8	LD (HL), D 1 8	LD (HL). E 1 8	LD (HL). H	LD (HL). L 1 8	HALT 1 4	LD (HL), A 1 8	LD A, B 1.4	1 4	1 4	1 4	1 4	10 A L	LD A. (HL) 1 8	1 4
8x	ADD A, B 1 4 2 0 H C	ADD A.C 1 4 2 0 H C	ADD A.D 1.4 ZOHC	ADD A. E 1 4 Z 0 H C	ADD A, H 1 4 2 0 H C	ADD A.L 1.4 ZOHC	ADD A. (HL) 1 8 2 0 H C	ADD A.A 1.4 ZOHC	ADC A.B 1.4 ZOHC	ADC A. C 1.4 ZOHC	ADC A, D 1 4 Z 0 H C	ADC A. E 1 4 Z 0 H C	ADC A. H 1 4 2 0 H C	ADC A. L 1 4 2 0 H C	ADC A. (HL) 1 8 2 0 H C	ADC A. A 1.4 ZOHC
9x	SUB B 1 4 Z 1 H C	SUB C 1 4 Z 1 H C	SUB D 1 4 Z 1 H C	SUB E 1 4 Z 1 H C	5UB H 1 4 Z 1 H C	SUB L 1 A Z 1 H C	SUB (HL) 1 8 Z 1 H C	SUB A 1 4 Z 1 H C	SBC A, B 1 4 Z 1 H C	58C A, C 1 4 2 1 H C	SBC A D 1 4 Z 1 H C	SBC A, E 1 4 Z 1 H C	58C A H 1 4 Z 1 H C	SBCAL 14 Z1HC	SBC A, (HL) 1 8 Z 1 H C	SBC A, A 1 4 Z 1 H C
Ax	AND 8 1 4 Z 0 1 0	AND C 1 4 Z 0 1 0	AND D 1 4 Z 0 1 0	AND E 1 4 2010	AND H 1 4 Z 0 1 0	AND L 1 4 Z 0 1 0	AND (HL) 1 8 Z 0 1 0	AND A 1 4 Z 0 1 0	XOR 8 1 4 Z 0 0 0	XOR C 1 4 Z 0 0 0	XOR D 1 4 Z 0 0 0	XOR E 1 4 Z 0 0 0	XOR H 1 4 Z 0 0 0	XOR L 1 4 Z 0 0 0	XOR (HL) 1 8 Z 0 0 0	XOR A 1 4 Z 0 0 0
Вх	OR B 1 4 Z 0 0 0	ORC 1 4 Z 0 0 0	OR D 1 4 2000	OR E 1 4 2 0 0 0	ORH 1 4 Z 0 0 0	OR L 1 4 Z 0 0 0	OR (HL) 1 8 Z 0 0 0	OR A 1 4 2000	CP 8 1 4 Z 1 H C	CPC 14 Z1HC	CPD 1.4 Z1HC	CPE 14 Z1HC	CPH 1 4 Z 1 H C	CPL 14 Z1HC	CP (HL) 1 8 Z 1 H C	CPA 14 Z1HC
Cx	RET NZ 1 20/8	POP BC 1 12	JP NZ, a16 3 16/12	JP a16 3 16	CALL NZ, a16 3 24/12	PUSH BC 1 16	ADD A, d8 2 8 2 0 H C	RST 00H 1 16	RET Z 1 20/8	RET 1 16	JP Z, a16 3 16/12	PREFIX 1 4	CALL Z, a16 3 24/12	CALL a16 3 24	ADC A, d8 2 8 Z 0 H C	RST 08H 1 16
Dx	RET NC 1 20/8	POP DE 1 12	JP NC, a16 3 16/12	-	CALL NC. a16 3 24/12	PUSH DE 1 16	SUB d8 2 8 2 1 H C	RST 10H 1 16	RET C 1 20/8	RETI 1 16	JP C a16 3 16/12	-	CALL C. a16 3 24/12	-	SBC A. dB 2 B Z 1 H C	RST 18H 1 16
Ex	LDH (a8), A 2 12	POP HL 1 12	LD (C). A 1 8	-:	-	PUSH HL 1 16	AND d8 2 8 2 0 1 0	RST 20H 1 16	ADD SP, r8 2 16 0 0 H C	JP HL 1 4	LD (a16), A 3 16	-	-	-	XOR d8 2 8 2 0 0 0	RST 28H 1 16
Fx	LDH A. (a8) 2 12	POP AF 1 12 Z N H C	LD A, (C) 1 8	DI 1 4	-	PUSH AF 1 16	OR 48 2 8 2 0 0 0	RST 30H 1 16	LD HL, SP + r8 2 12 0 0 H C	LD SP, HL 1 8	LD A. (a16) 3 16	E) 1 4	-	-	CP d8 2 8 Z 1 H C	RST 38H 1 16

### https://rednex.github.io/rgbds/gbz80.7.html

# DEC [HL] Decrement the byte pointed to by HL by 1. Cycles: 3 Bytes: 1 Flags: See DEC r8 DEC r16 Decrement value in register r16 by 1. Cycles: 2 Bytes: 1 Flags: None affected. DEC SP Decrement value in register SP by 1. Cycles: 2



#### https://cturt.github.io/cinoop.html

#### Writing a Game Boy emulator, Cinoop

I've always wanted to write an emulator from scratch, but I've held off for a long time because it's probably the most adv project I've ever wanted to do.

Picking a system to emulate isn't an easy choice; the standard first emulator project seems to be a CHIP-8 emulator. Ru definitely helped me to understand a lot of emulation concepts, but it seemed a bit too basic. I felt that I got enough out through other people's emulators, and that writing my own would be a pointless exercise.

On the other hand, there's the NES and Game Boy; both of which seemed far too advanced for me!

Eventually, I decided to write a minimalist Game Boy interpreting emulator, without support for custom mappers or sour many inaccuracies). I called the project Cinoop.

Cinoop is written in C and is open source. It can be run on Windows, DS, GameCube, 3DS, Linux based OSes, PSP, at

#### https://github.com/ocornut/imgui

#### dear imgui

O build passing

(This library is available under a free and permissive license, but needs financial support to sustain its continued improvements. In addition to maintenance and stability the are many desirable features yet to be added. If your company is using dear imgui, please consider reaching out.)

Businesses: support continued development via invoiced technical support, maintenance, sponsoring contracts: E-mail: contact @ dearimgui dot org

Individuals: support continued maintenance and development with PayPal.

Dear ImGui is a **bloat-free graphical user interface library for C++**. It outputs optimized vertex buffers that you can render anytime in your 3D-pipeline enabled application. It is fast, portable, renderer agnostic and self-contained (no external dependencies).

#### https://lazyfoo.net/tutorials/SDL/

	Table of Contents
Lesson 01 <u>Hello SDL</u>	In this tutorial we will be setting up the SDL library and creating our first window.
Lesson 02 Getting an Image on the Screen	Now that we can get a window to appear, lets blit an image onto it.
Lesson 03 <u>Event Driven Programming</u>	Here we'll start handling user input by allowing the user to X out the window.
Lesson 04 <u>Key Presses</u>	Here we'll learn to handle keyboard input.
Lesson 05 Optimized Surface Loading and Soft Stretching	Now that we know how to load and blit surfaces, it's time to make our blits faster. We'll also take a smaller image and stretch it
Lesson 06 <u>Extension Libraries and Loading Other</u> <u>Image Formats</u>	Here we'll be using the SDL_image extension library to load png images.
Lesson 07 Texture Loading and Rendering	A big new feature in SDL 2.0 is hardware accelerated texture based 2D rendering. Here we'll be loading an image to render it u
Lesson 08 <u>Geometry Rendering</u>	Another new feature in SDL 2.0 is hardware accelerated primitive rendering. Here we'll be using it to render some common
Lesson 09 The Viewport	SDL 2.0 also lets you control where you render on the screen using the viewport. We'll be using the viewport to create su
Lesson 10 <u>Color Keying</u>	Here we'll use color keying to give textures transparent backgrounds.
Lesson 11 <u>Clip Rendering and Sprite Sheets</u>	Using clip rendering, you can keep multiple images on one texture and render the part you need. We'll be using this to render individual sp
Lesson 12	We'll be altering the color of rendered textures using color modulation.

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