■ General Description

The OCP7190 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a 5VDC power supply.

Audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The OCP7190 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The OCP7190 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the OCP7190 features an internal thermal shutdown protection mechanism.

The OCP7190 contains advanced pop and click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The OCP7190 is unity-gain stable and can be configured by external gain-setting resistors.

■ Key Specifications

- PSRR at 217Hz, VDC=5V (Fig.1) 62dB(typ.)
- Power Output at 5.0V & 1% THD 1W(typ.)
- Power Output at 3.3V & 1% THD 400mW(typ.)
- Shutdown Current 0.1μA(typ.)

■ Features

- Available in space-saving packages: micro SMD, MSOP
- Ultra low current shutdown mode
- BTL output can drive capacitive loads
- Improved pop and click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2V - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Thermal shutdown protection
- Unity-gain stable
- External gain configuration capability

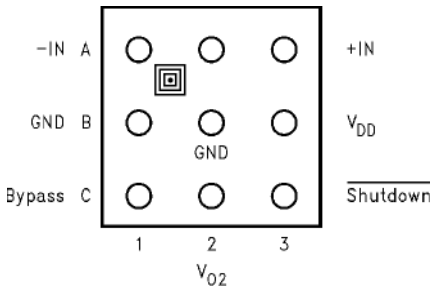
■ Applications

- Mobile Phones
- PDA
- Portable electronic devices

■ Pin Configuration

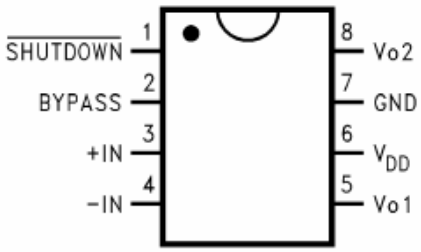
1) 9 Bump micro SMD

(Top View)



2) MSOP8L

(Top View)



■ Absolute Maximum Ratings

Supply Voltage (Note 11)		6.0V
Input Voltage		-0.3V to V_{DD}+0.3V
Junction Temperature		150℃
Storage Temperature Range		-65℃ to +150℃
Power Dissipation (Note 3)		Internally Limited
ESD Susceptibility (Note 4)		2000V
Thermal Resistance	θ_{JA}(9 Bump micro SMD, Note 12)	180℃/W
	θ_{JC}(MSOP)	56℃/W
	θ_{JA}(MSOP)	190℃/W

■ Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	2.2		5.5	V
Temperature Range	TA	-40		85	℃

■ Electrical Characteristics (V_{DD}=5V, notes 1,2,8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA=25℃

Parameter	Symbol	Condition	Typical (Note 6)	Limit (Notes7,9)	Units (Limits)
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V, I_O=0A, No Load	4	8	mA(max)
		V_{IN}=0V, I_O=0A, 8Ω Load	5	10	mA(max)
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$=0V	0.1	2.0	μA(max)
Shutdown Voltage Input High	V_{SDIH}			1.2	V(min)
Shutdown Voltage Input Low	V_{SDIL}			0.4	V(max)
Output Offset Voltage	V_{OS}		7	50	mV(max)
Resistor Output to GND(Note10)	$R_{OUT-GND}$		8.5	9.7	kΩ(max)
				7.0	kΩ(min)
Output Power(8Ω)	P_O	THD=2%(max); f=1kHz	1.0	0.8	W
Wake-up time	T_{WU}		170	220	ms(max)
Thermal Shutdown Temperature	T_{SD}		170	150	℃(min)
				190	℃(max)
Total Harmonic Distortion+Noise	THD+N	P_O=0.4Wrms; f=1kHz	0.1		%
Power Supply Rejection Radio (Note 14)	PSRR	Vripple=200mV sine p-p Input Temperature with 10 ohms to ground	62(f=217Hz) 66(f=1kHz)	55	dB(min)
Shut Down Time	T_{SDT}	8Ω load	1.0		ms(max)

■ Electrical Characteristics (V_{DD}=3V, notes 1,2,8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA=25℃

Parameter	Symbol	Condition	Typical (Note 6)	Limit (Notes7,9)	Units (Limits)
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V, I_O=0A, No Load	3.5	7	mA(max)
		V_{IN}=0V, I_O=0A, 8Ω Load	4.5	9	mA(max)
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$=0V	0.1	2.0	μA(max)
Shutdown Voltage Input High	V_{SDIH}			1.2	V(min)
Shutdown Voltage Input Low	V_{SDIL}			0.4	V(max)
Output Offset Voltage	V_{OS}		7	50	mV(max)
Resistor Output to GND(Note10)	$R_{OUT-GND}$		8.5	9.7	kΩ(max)
				7.0	kΩ(min)
Output Power(8Ω)	P_O	THD=1%(max); f=1kHz	0.31	0.28	W
Wake-up time	T_{WU}		120	180	ms(max)
Thermal Shutdown Temperature	T_{SD}		170	150	℃(min)
				190	℃(max)
Total Harmonic Distortion+Noise	THD+N	P_O=0.15Wrms; f=1kHz	0.1		%
Power Supply Rejection Radio (Note 14)	PSRR	Vripple=200mV sine p-p Input Temperature with 10 ohms to ground	56(f=217Hz) 62(f=1kHz)	45	dB(min)

■ Electrical Characteristics (V_{DD}=2.6V, notes 1,2,8)

The following specifications apply for the circuit shown in Figure 1 unless otherwise specified. Limits apply for TA=25℃

Parameter	Symbol	Condition	Typical (Note 6)	Limit (Notes7,9)	Units (Limits)
Quiescent Power Supply Current	I_{DD}	V_{IN}=0V, I_O=0A, No Load	2.6		mA(max)
Shutdown Current	I_{SD}	$V_{SHUTDOWN}$=0V	0.1		μA(max)
Output Power(8Ω)	P_O	THD=1%(max); f-1kHz	0.2		W
Output Power(4Ω)		THD=1%(max); f-1kHz	0.22		
Total Harmonic Distortion+Noise	THD+N	P_O=0.1Wrms; f=1kHz	0.08		%
Power Supply Rejection Radio (Note 14)	PSRR	Vripple=200mV sine p-p Input Temperature with 10 ohms to ground	44(f=217Hz) 44(f=1kHz)		dB

Note1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note3: The maximum power dissipation must be derated at elevated temperature and is dictated by T_{JMAX}, $\theta_{JA,}$ and the ambient temperature T_A. The maximum allowable power dissipation is PDMAX=(TJMAX-TA)/ θJA or the number given in Absolute Maximum Ratings, whichever is lower. For the OCP7190, see power derating curves for additional information.

Note4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note5: Machine Model, 220pF-240pF discharged through all pins.

Note6: Typicals are measured at 25℃ and represent the parametric norm.

Note7: Limits are guaranteed to CSMSC"s AOQL(Average Outgoing Quality Level).

Note8: For micro SMD only, shutdown current is measured in a Normal Room Environment. Exposure to direct sunlight will increase I_{SD} by a maximum of 2μA.

Note9: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Note10: ROUT is measured from each of the output pins to ground. This value represents the parallel combination

of the 10k ohm output resistors and the two 20k ohm resistors.

Note11: If the product is in shutdown mode and V_{DD} exceeds 6V (to a max of 8V V_{DD}), then most of the excess current will follow through the ESD protection circuits. If the source impedance limits the current to a max of 10mA, then the part will be protected. If the part is enabled when V_{DD} is greater than 5.5V and less than 6.5V, no damage will occur, although operational life will be reduced. Operation above 6.5V with no current limit will result in permanent damage.

Note12: All bumps have the same thermal resistance and contribute equally when used to lower thermal resistance. All bumps must be connected to achieve specified thermal resistance.

Note13: Maximum power dissipation (P_{DMAX}) in the device occurs at an output power level significantly below full output power. P_{DMAX} can be calculated using Equation 1 shown in the Application section. It may also be obtained from the dissipation graphs.

Note14: PSRR is a functional of systems gain. Specifications apply to the circuit in Figure 1 where A_V=2. Higher system gains will reduce PSRR value by the amount of gain increase. A system gain of 10 represents a gain increased by 14dB and applies to all operating voltages.

■ Typical Application Circuit

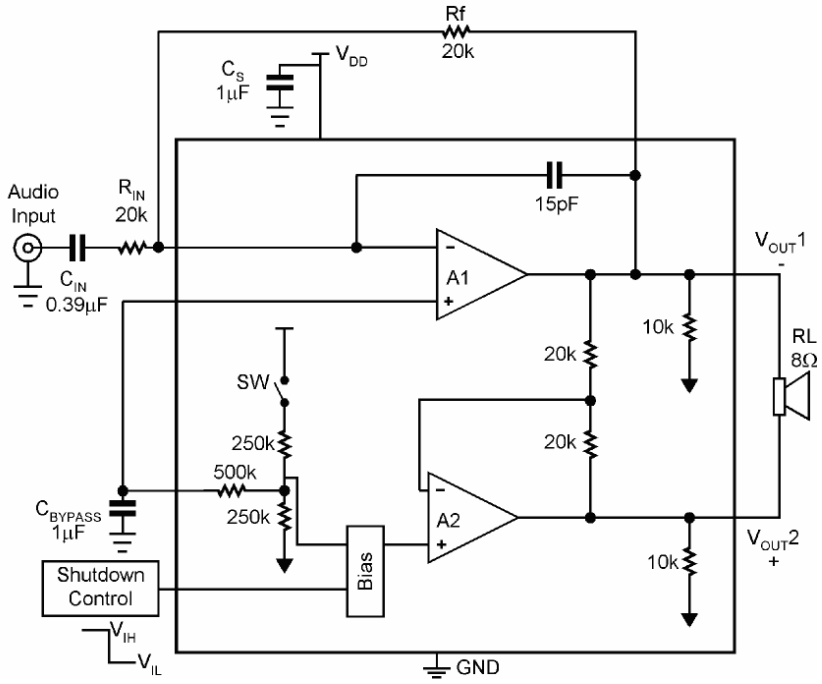


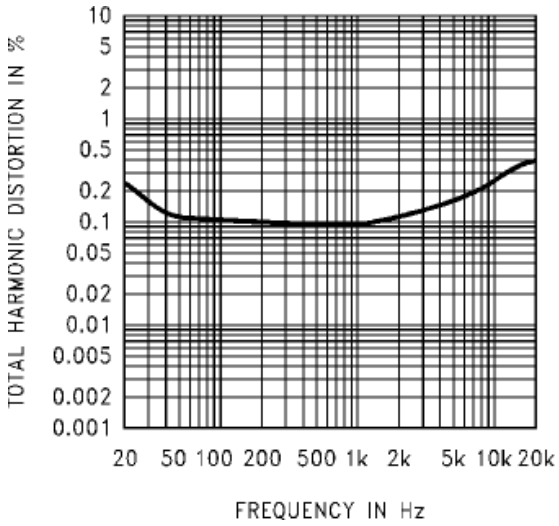
Figure 1

■ External Components Description

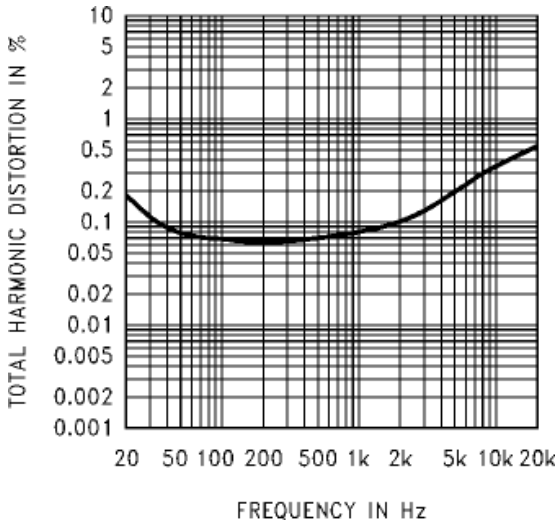
Components	Functional Description
R_{IN}	Inverting input resistance which sets the closed-loop gain in conjunction with R_f. This resistor also forms a high pass filter with C_{IN} at $f_C = 1/(2\pi R_{IN} C_{IN})$
C_{IN}	Input coupling capacitor which blocks the DC voltage at the amplifier's input terminals. Also creates a highpass filter with R_{IN} at fc $= 1/(2\pi R_{IN} C_{IN})$. Refer to the section, Proper Selection of External Components, for an explanation of how to determine the value of C_{IN}
R_f	Feedback resistance which sets the closed-loop gain in conjunction with R_{IN}
C_S	Supply bypass capacitor which provides power supply filtering. Refer to the section, Power Supply Bypassing, for information concerning proper placement and selection of the supply bypass capacitor C_{BAPASS}
C_{BAPASS}	Bypass pin capacitor which provides half-supply filtering. Refer to the section, Proper Selection of External Components, for information concerning proper placement and selection of C_{BAPASS}

■ Typical Performance Characteristics

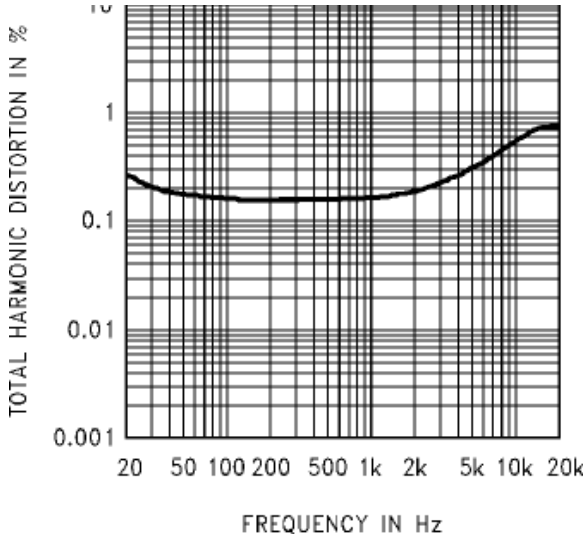
THD+N vs Frequency
at V_{DD}=5V, R_L=8Ω，and PWM=250mW, A_V=2



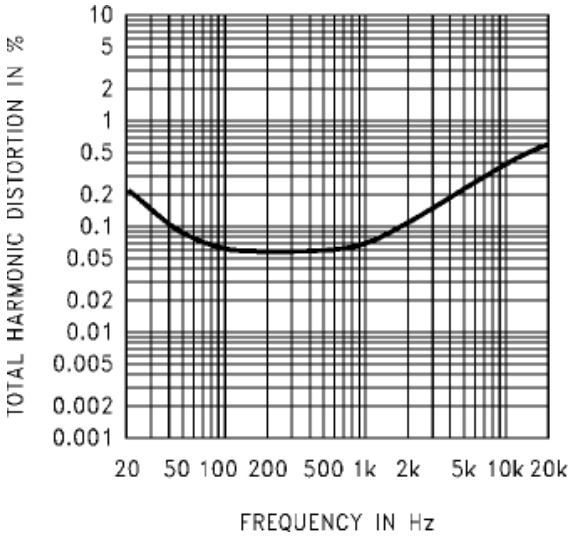
THD+N vs Frequency
at V_{DD}=3.3V, R_L=8Ω，and PWM=150mW, A_V=2



THD+N vs Frequency
at V_{DD}=3V, R_L=8Ω，and PWM=250mW, A_V=2

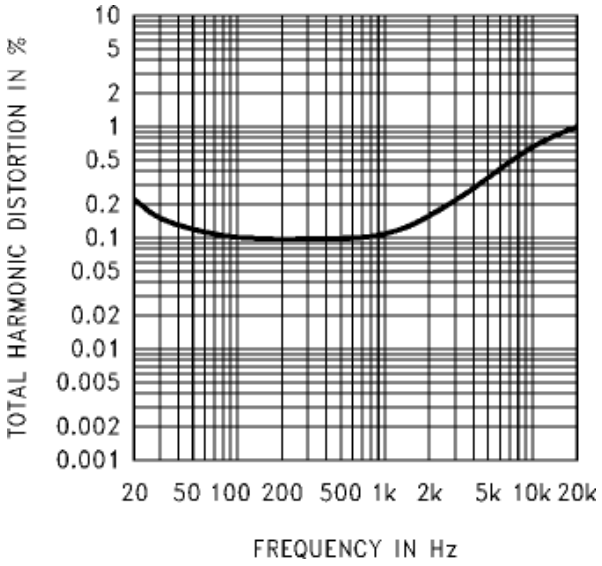


THD+N vs Frequency
at V_{DD}=2.6V, R_L=8Ω，and PWM=100mW, A_V=2

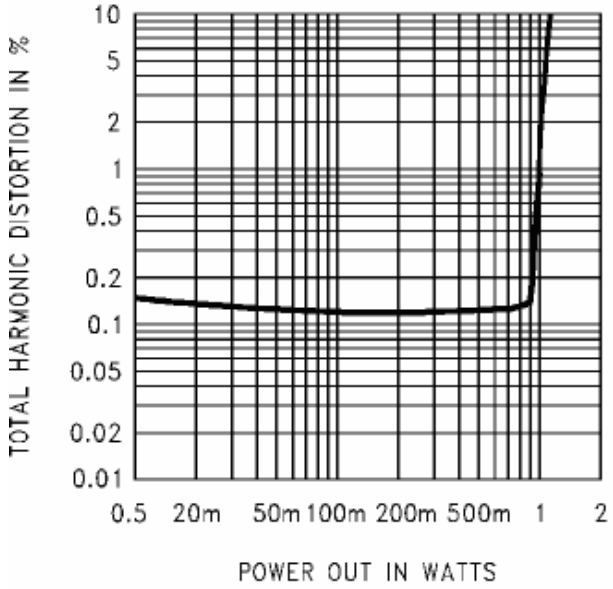


■ Typical Performance Characteristics (Continued)

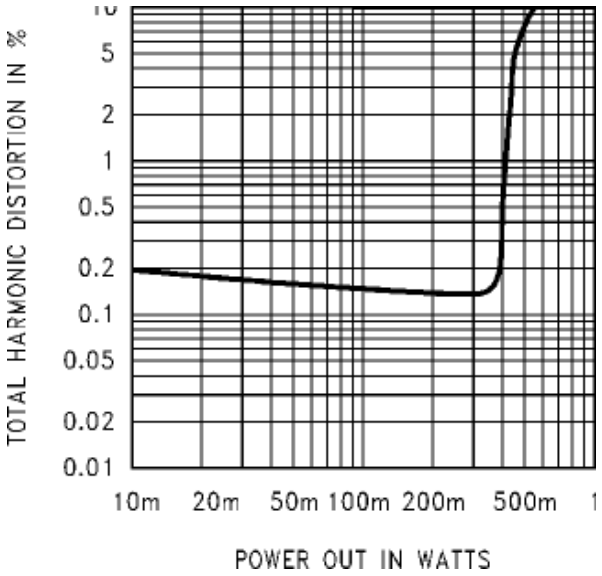
THD+N vs Frequency
at V_{DD}=2.6V, R_L=4Ω，and PWM=100mW, A_V=2



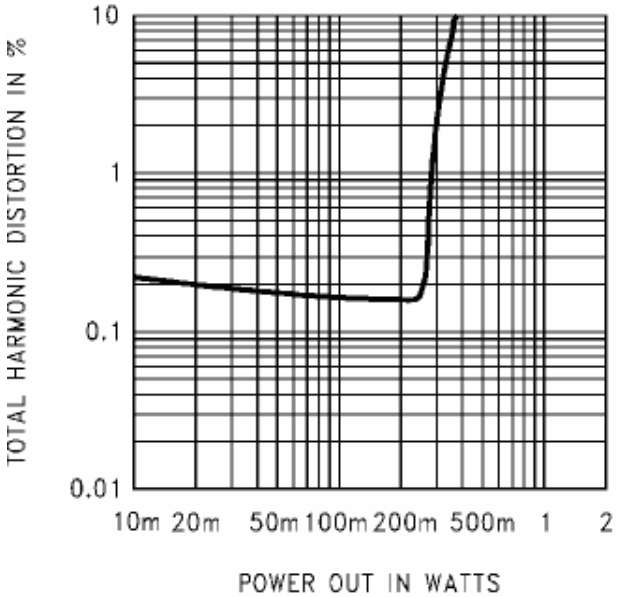
THD+N vs Power Out
at V_{DD}=5V, R_L=8Ω，1kHz, A_V=2



THD+N vs Power Out
at V_{DD}=3.3V, R_L=8Ω，1kHz, A_V=2

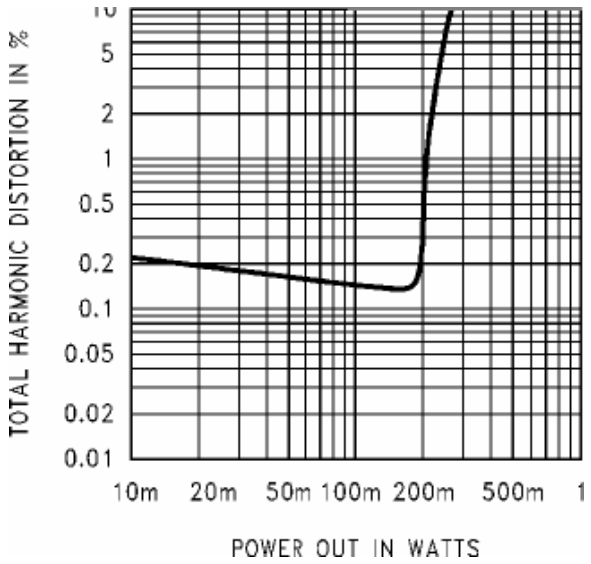


THD+N vs Power Out
at V_{DD}=3V, R_L=8Ω，1kHz, A_V=2

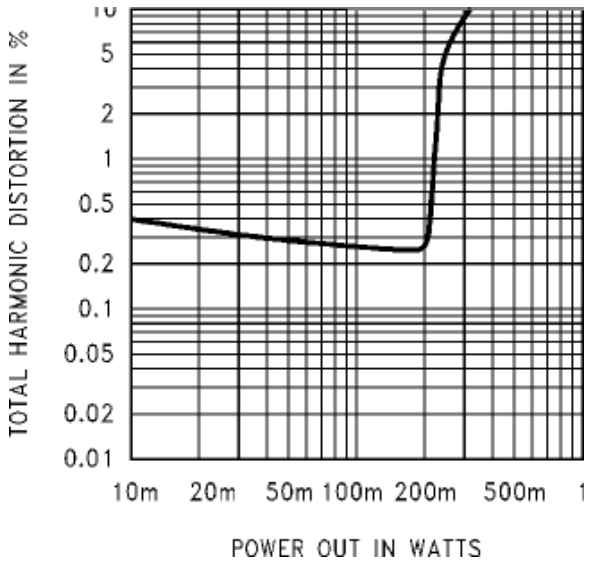


■ Typical Performance Characteristics (Continued)

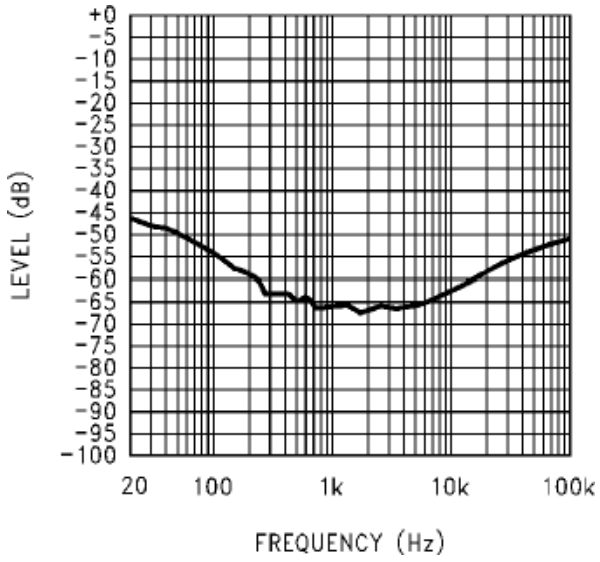
THD+N vs Power Out
at V_{DD}=2.6V, R_L=8Ω，1kHz, A_V=2



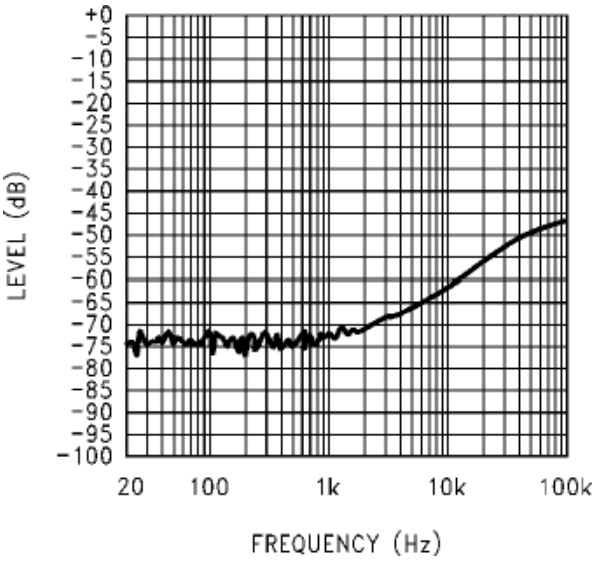
THD+N vs Power Out
at V_{DD}=2.6V, R_L=4Ω，1kHz, A_V=2



Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=5V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω

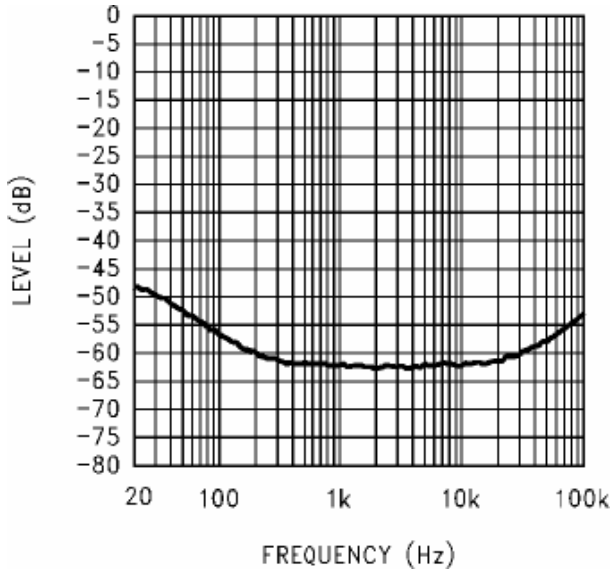


Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=5V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=Float

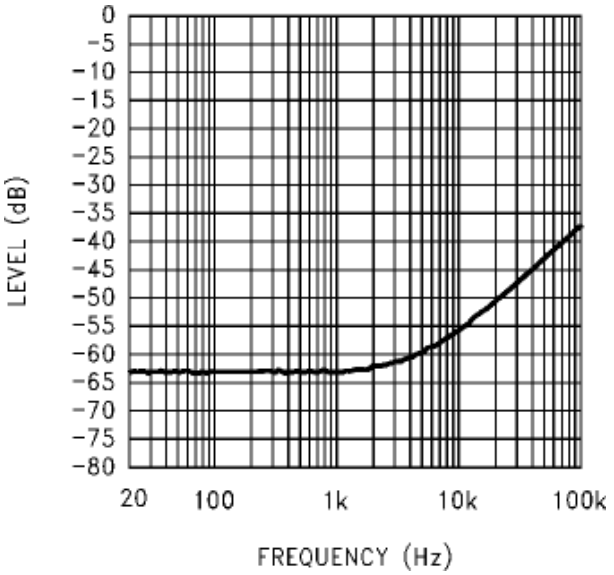


■ Typical Performance Characteristics (Continued)

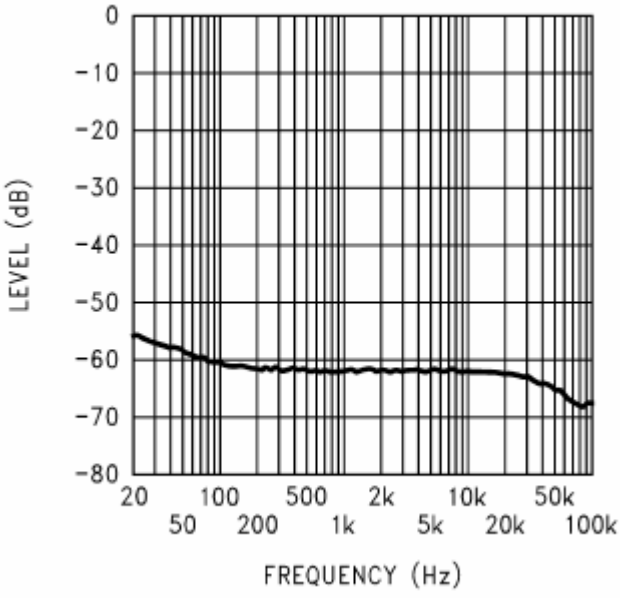
Power Supply Rejection Ratio (PSRR) at AV=4
V_{DD}=5V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω



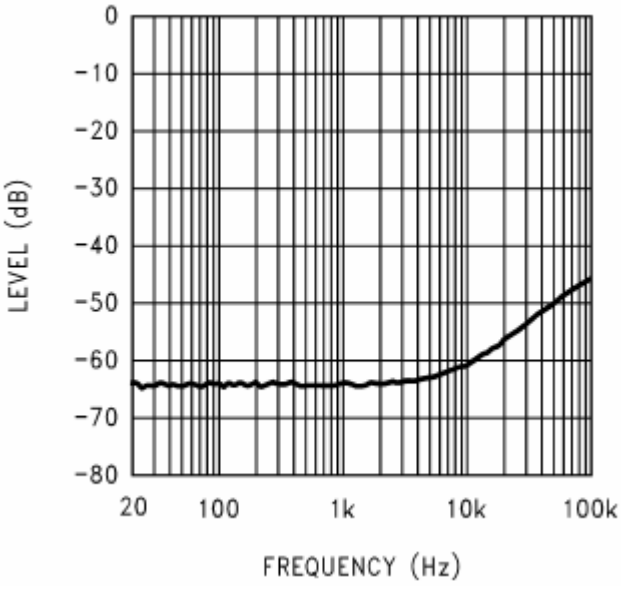
Power Supply Rejection Ratio (PSRR) at AV=4
V_{DD}=5V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=Float



Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=3V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω

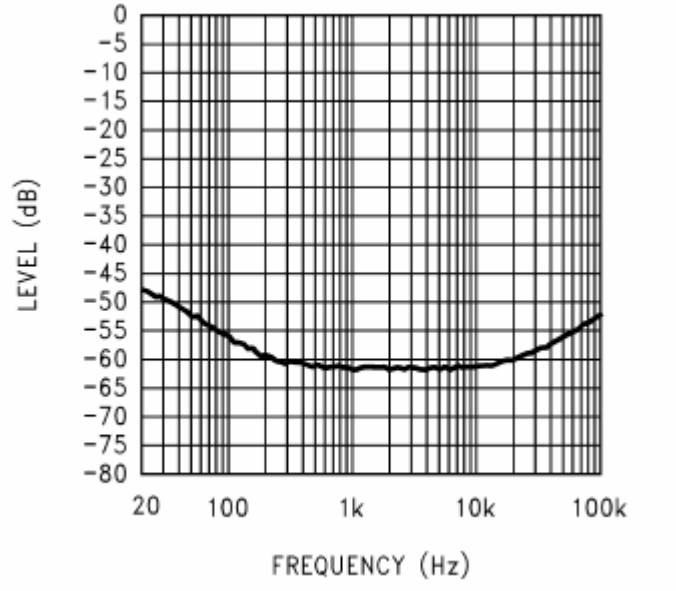


Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=3V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=Float

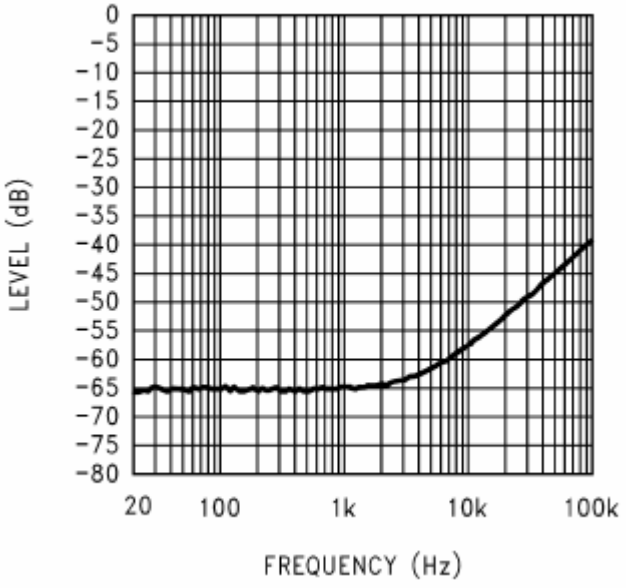


■ Typical Performance Characteristics (Continued)

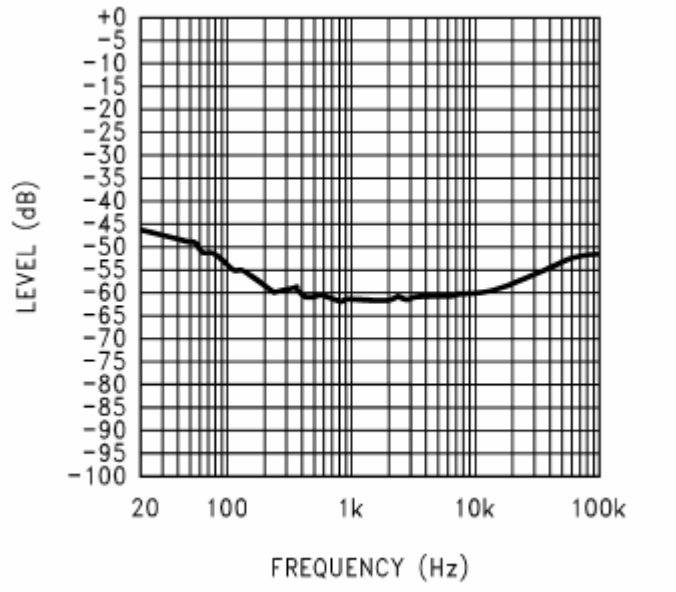
Power Supply Rejection Ratio (PSRR) at AV=4
V_{DD}=3V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω



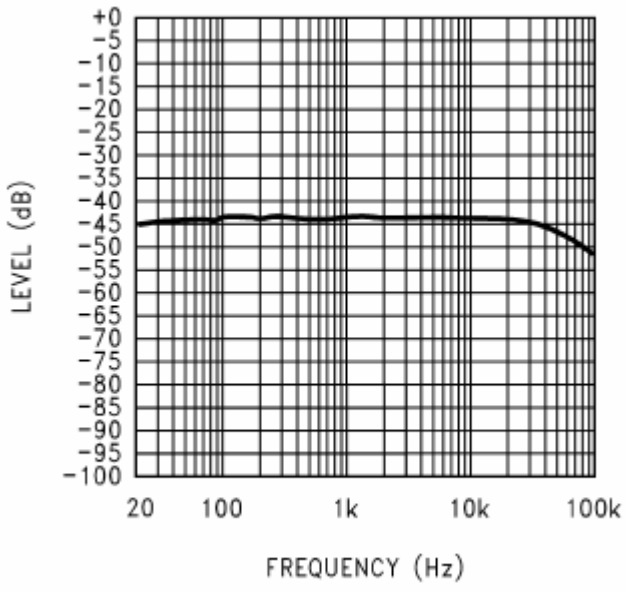
Power Supply Rejection Ratio (PSRR) at AV=4
V_{DD}=3V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=Float



Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=3.3V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω

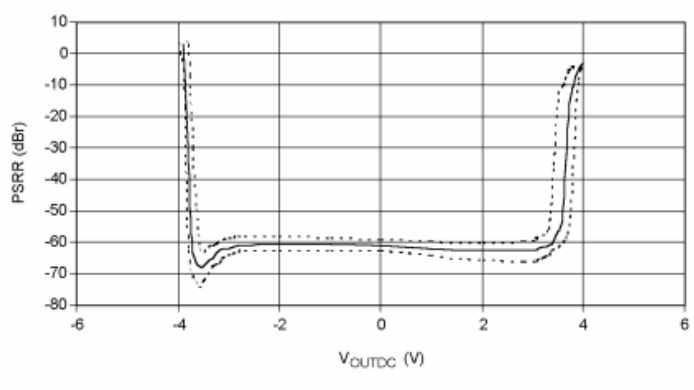


Power Supply Rejection Ratio (PSRR) at AV=2
V_{DD}=2.6V, V_{ripple}=200mvp-p, R_L=8Ω, R_{IN}=10Ω

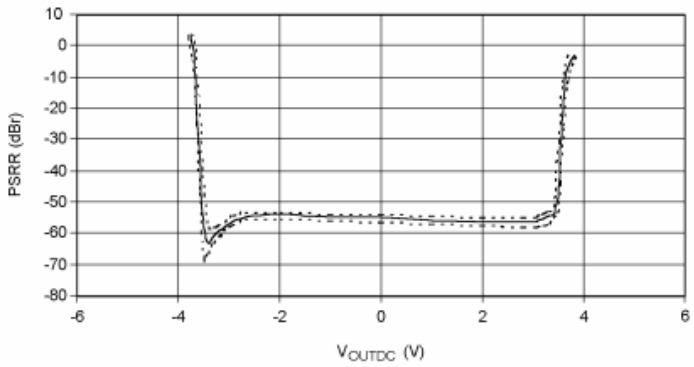


■ Typical Performance Characteristics (Continued)

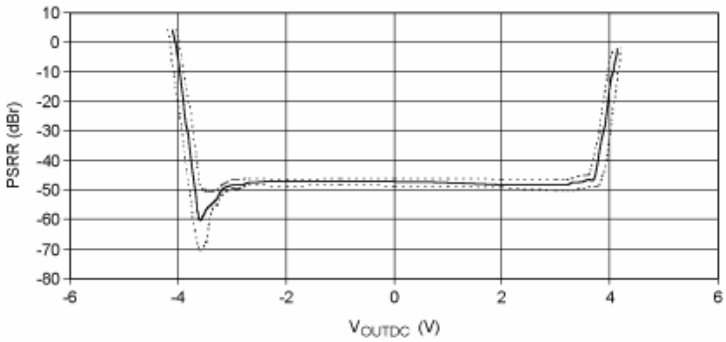
PSRR vs DC Output Voltage
V_{DD}=5V, A_V=2



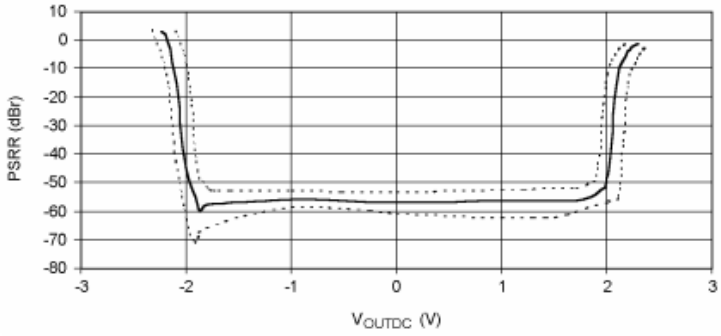
PSRR vs DC Output Voltage
V_{DD}=5V, A_V=4



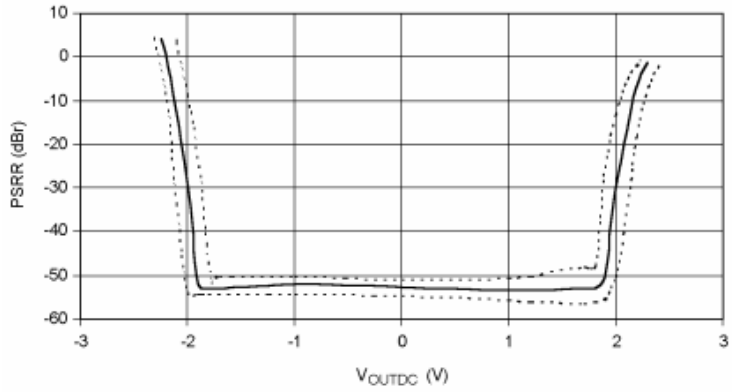
PSRR vs DC Output Voltage
V_{DD}=5V, A_V=10



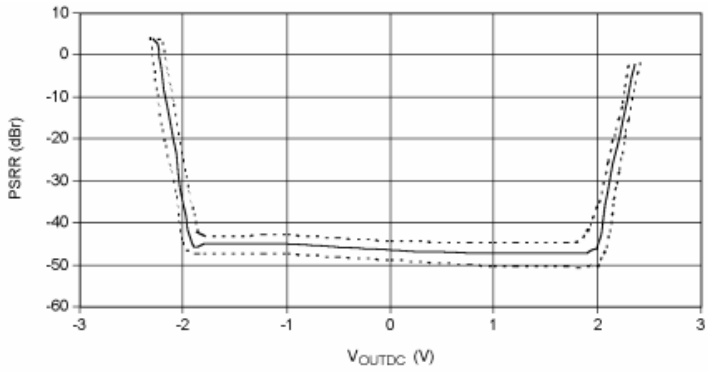
PSRR vs DC Output Voltage
V_{DD}=3V, A_V=2



PSRR vs DC Output Voltage
V_{DD}=3V, A_V=4

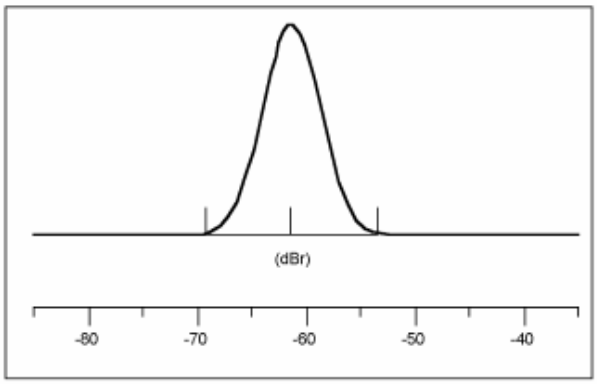


PSRR vs DC Output Voltage
V_{DD}=3V, A_V=10

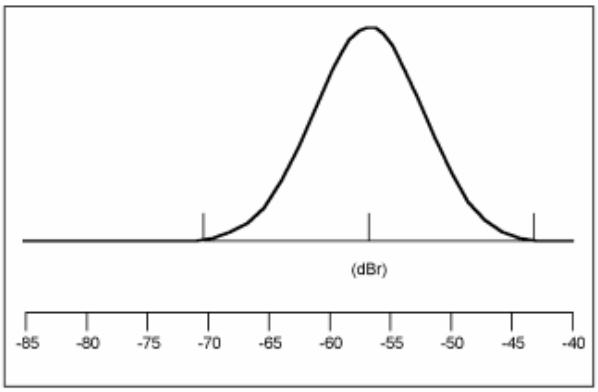


■ Typical Performance Characteristics (Continued)

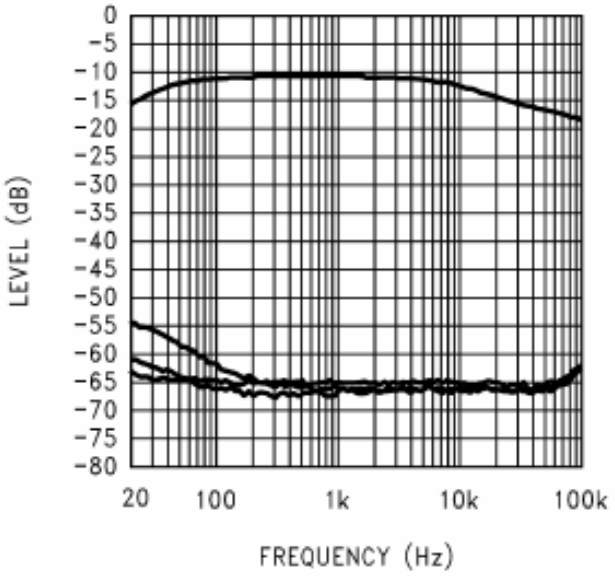
PSRR Distribution VDD=5V
217Hz, 200mvp-p, -30,+25,and+80℃



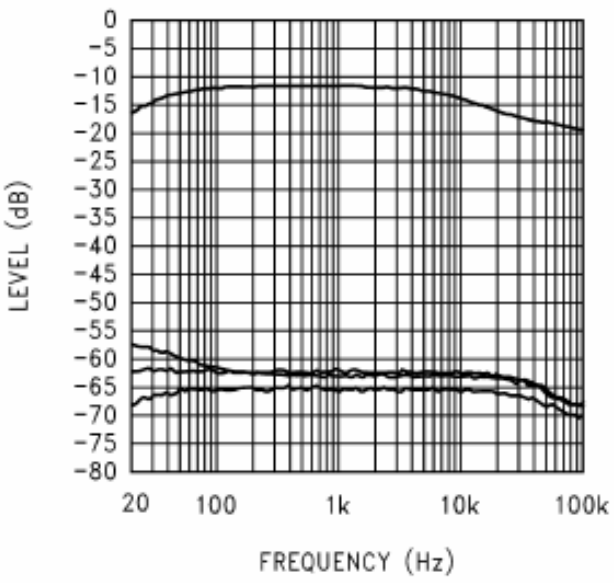
PSRR Distribution VDD=3V
217Hz, 200mvp-p, -30,+25,and+80℃



Power Supply Rejection Ration vs Bypass Capacitor Size
V_{DD}=5V, Input Grounded=10Ω, Output Load=8Ω

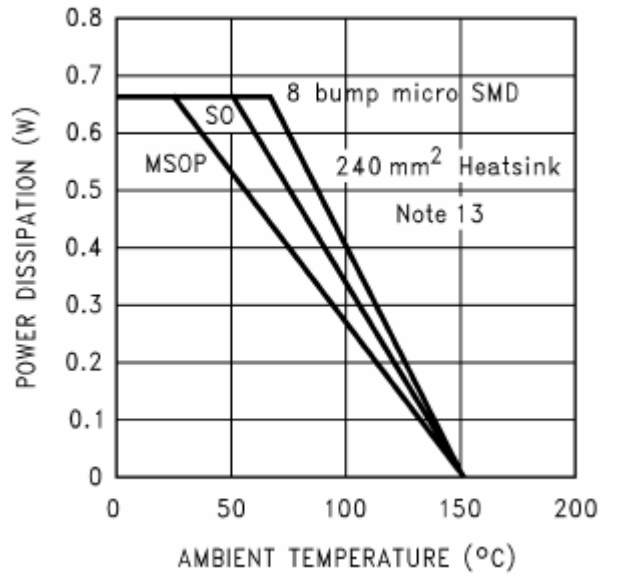


Power Supply Rejection Ration vs Bypass Capacitor Size
V_{DD}=3V, Input Grounded=10Ω, Output Load=8Ω



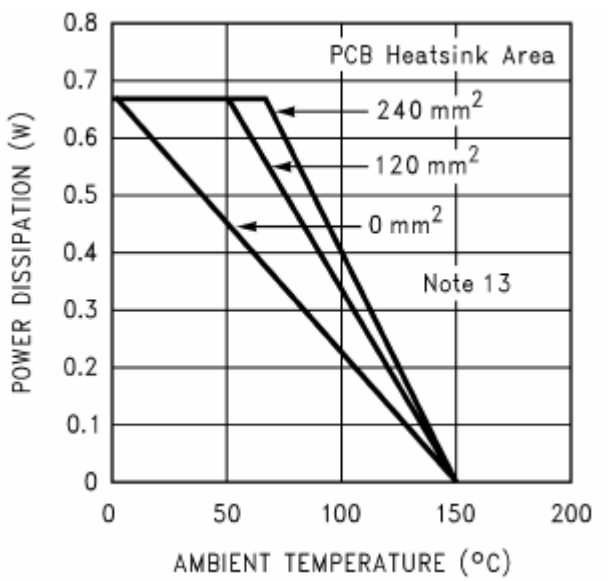
■ Typical Performance Characteristics (Continued)

Power Derating Curves (P_{DMAX}=670mW)



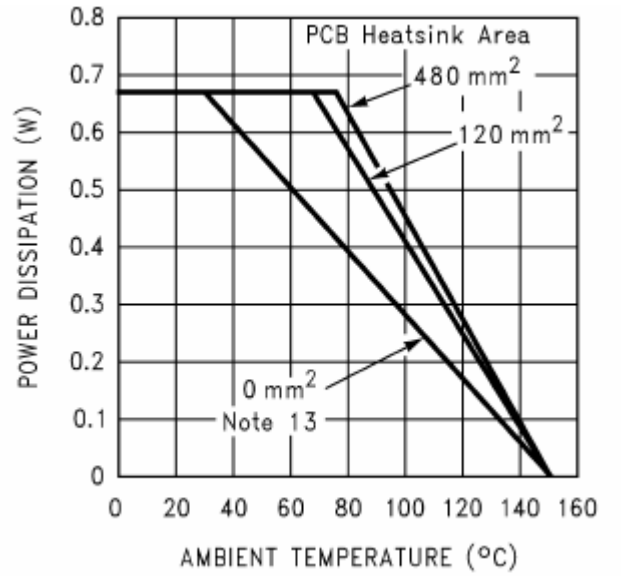
Ambient Temperature in Degrees C
Note: (P_{DMAX}=670mW for 5V, 8Ω)

Power Derating -8 bump SMD (P_{DMAX}=670mW)



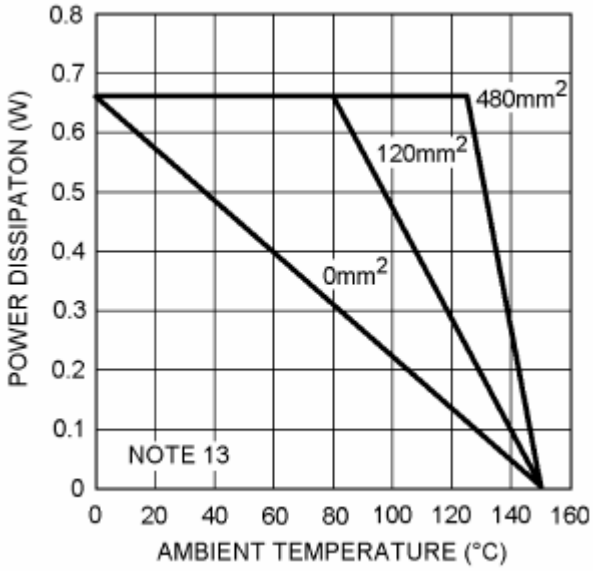
Ambient Temperature in Degrees C
Note: (P_{DMAX}=670mW for 5V, 8Ω)

Power Derating -9 bump SMD (P_{DMAX}=670mW)



Ambient Temperature in Degrees C
Note: (P_{DMAX}=670mW for 5V, 8Ω)

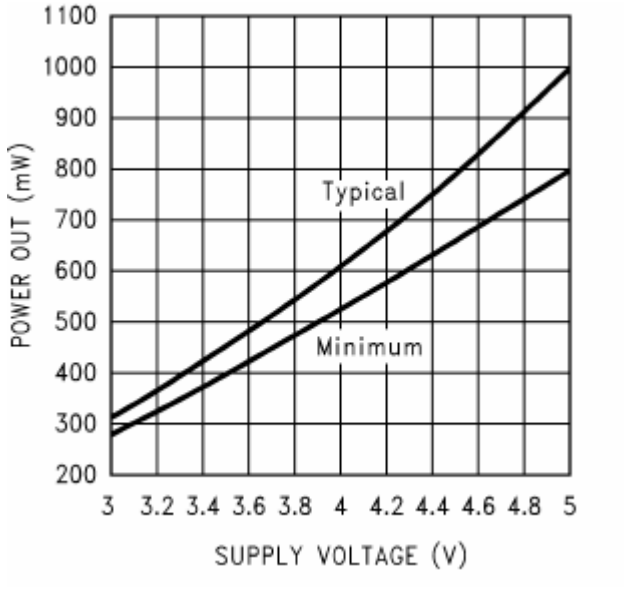
Power Derating -10 Pin LD Pkg (P_{DMAX}=670mW)



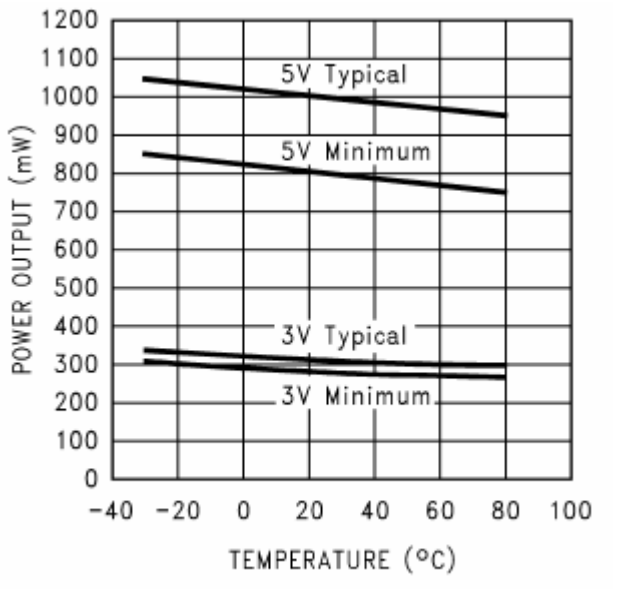
Ambient Temperature in Degrees C
Note: (P_{DMAX}=670mW for 5V, 8Ω)

■ Typical Performance Characteristics (Continued)

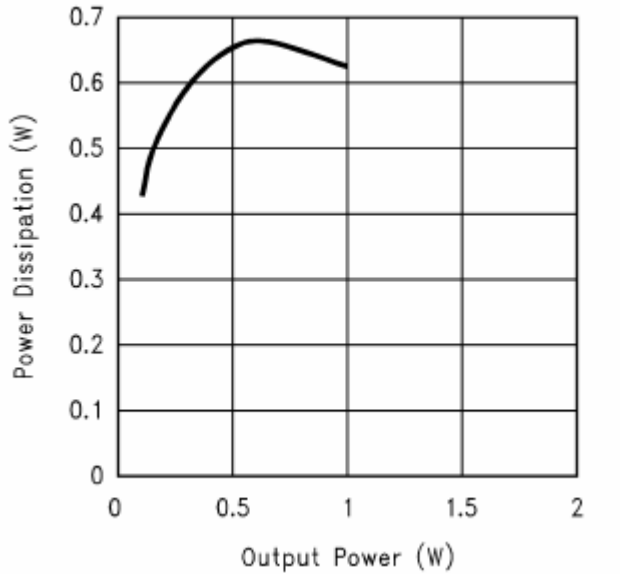
Power Output vs Supply Voltage



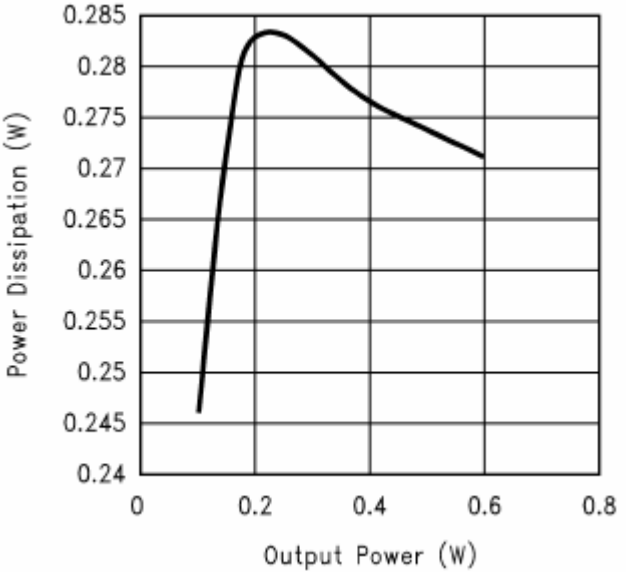
Power Output vs Temperature



Power Dissipation vs Output Power
V_{DD}=5V, 1kHz, 8Ω, THD≤1.0%

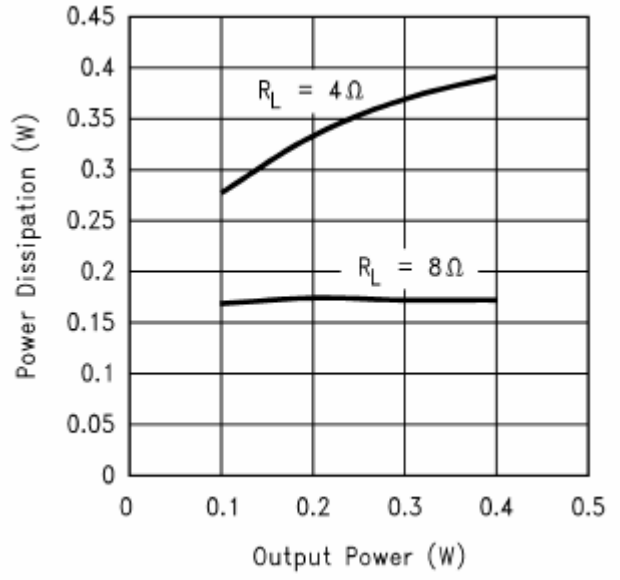


Power Dissipation vs Output Power
V_{DD}=3.3V, 1kHz, 8Ω, THD≤1.0%

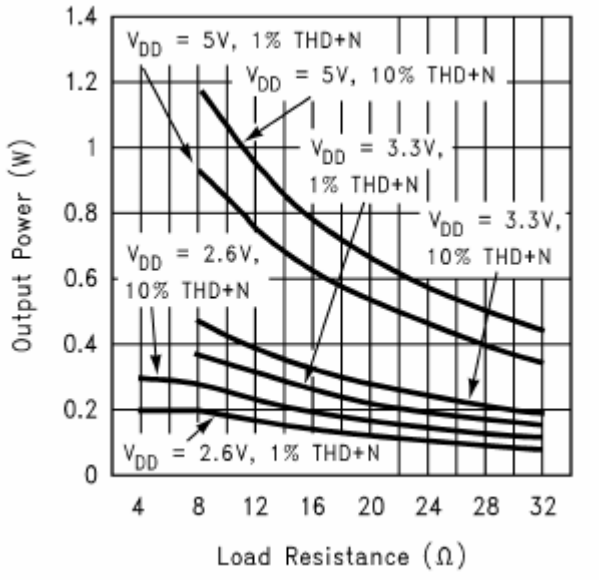


■ Typical Performance Characteristics (Continued)

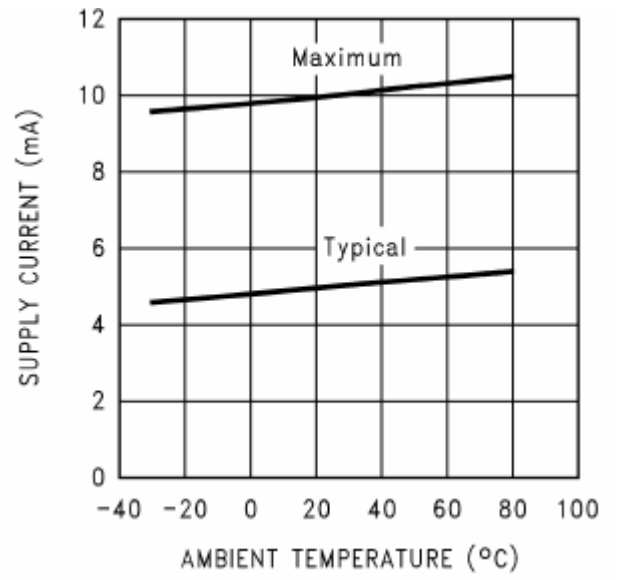
Power Dissipation vs Output Power
V_{DD}=2.6V, 1kHz,



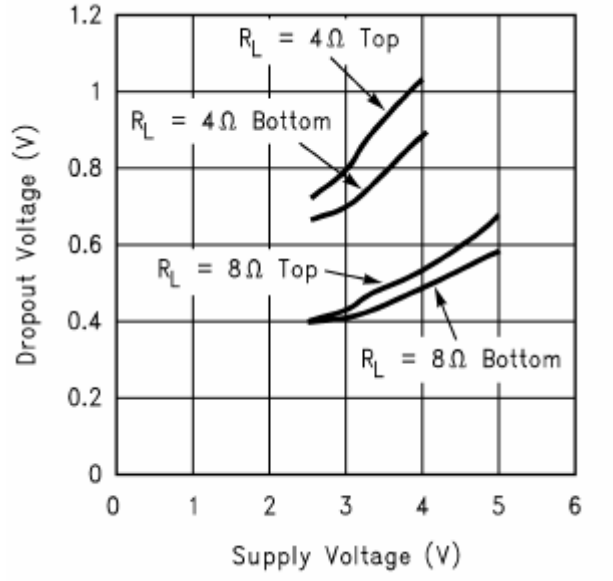
Output Power vs Load Resistance



Supply Current v s Ambient Temperature

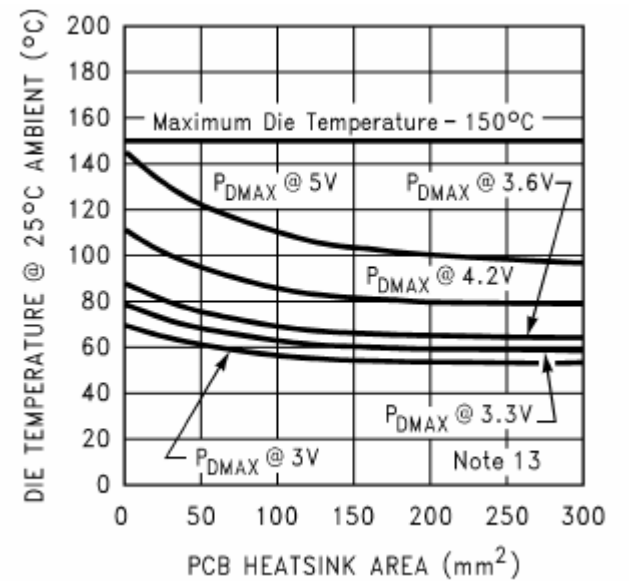


Clipping (Dropout) Voltage vs Supply Voltage

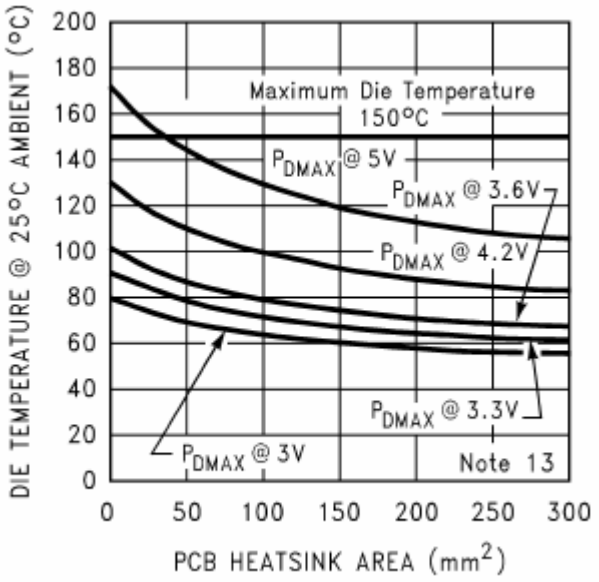


■ Typical Performance Characteristics (Continued)

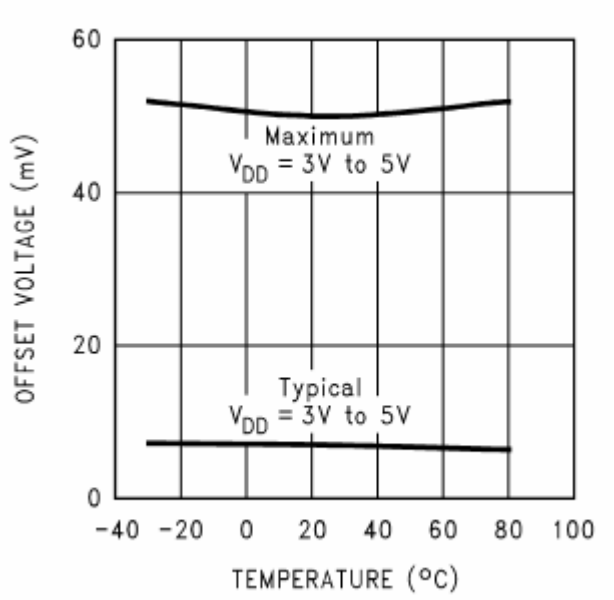
Max Die Temp at P_{DMAX}
(9 bump microSMD)



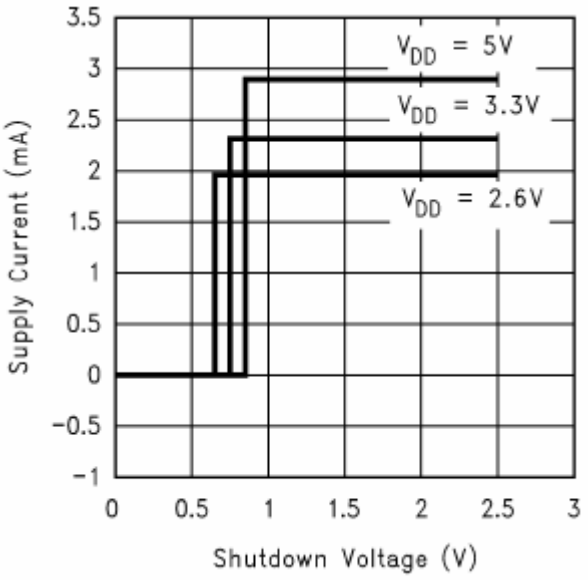
Max Die Temp at P_{DMAX}
(8 bump microSMD)



Output Offset Voltage

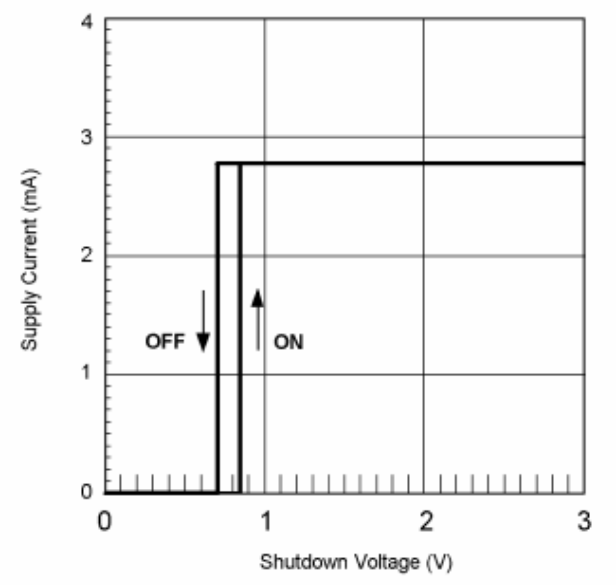


Supply Current vs Shutdown Voltage

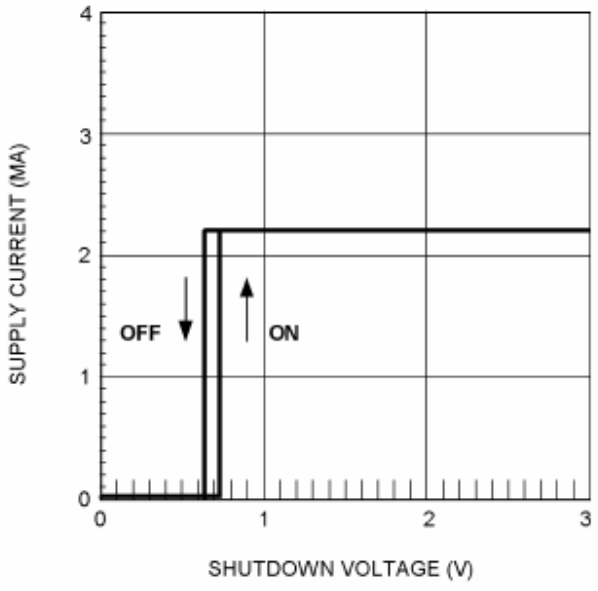


■ Typical Performance Characteristics (Continued)

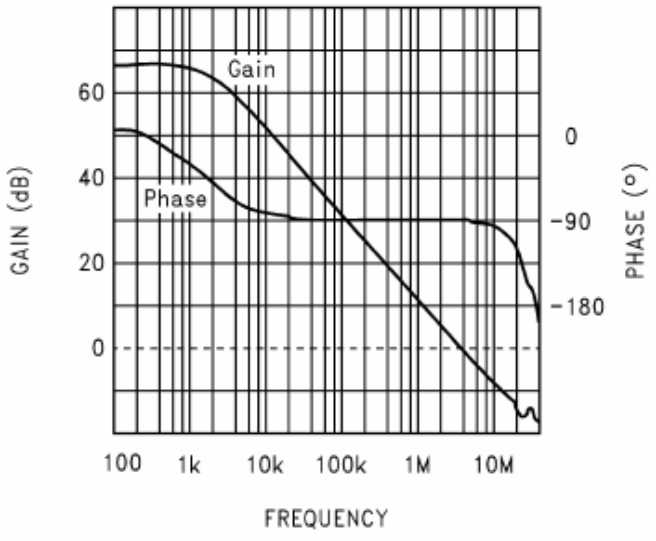
Shutdown Hysterisis Voltage
V_{DD}=5V



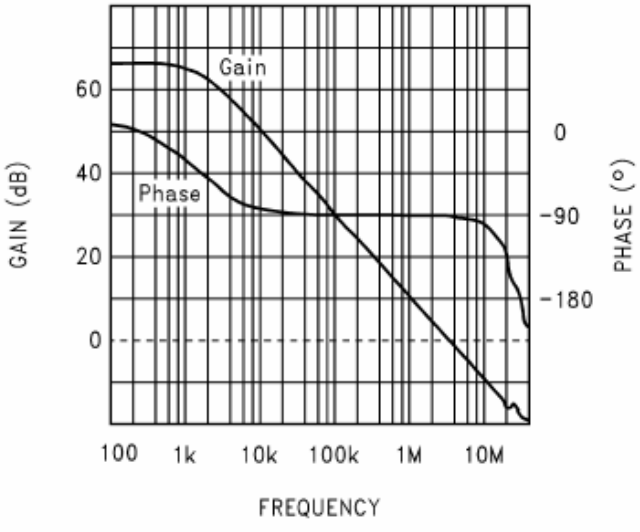
Shutdown Hysterisis Voltage
V_{DD}=3V



Open Loop Frequency Response
V_{DD}=5V, No Load

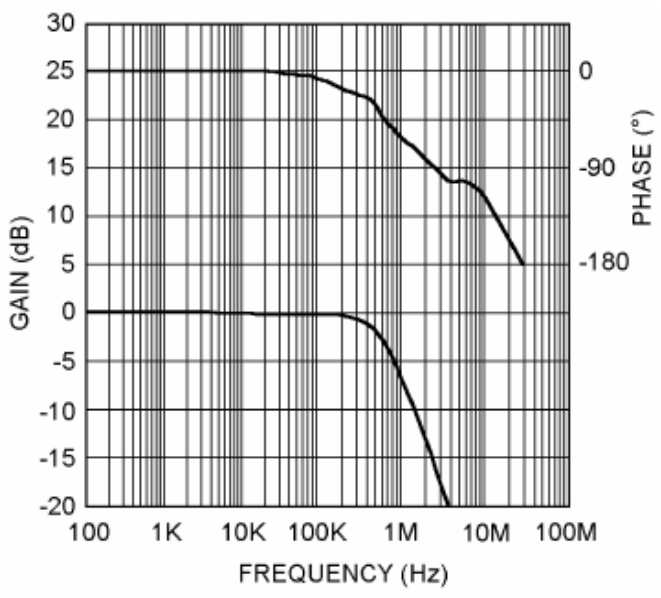


Open Loop Frequency Response
V_{DD}=3V, No Load

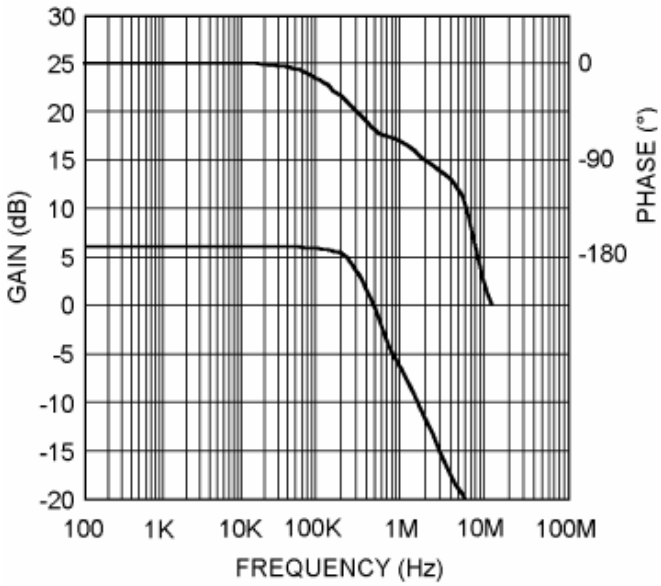


■ Typical Performance Characteristics (Continued)

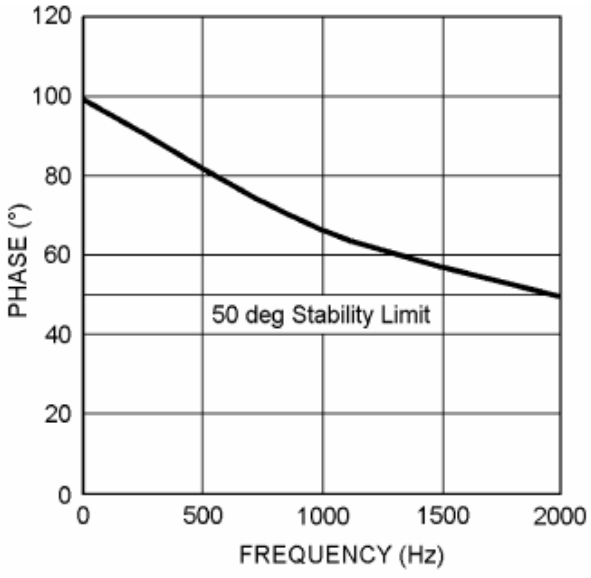
Gain/Phase Response, AV=2
V_{DD}=5V, 8Ω Load, C_{LOAD}=500pF



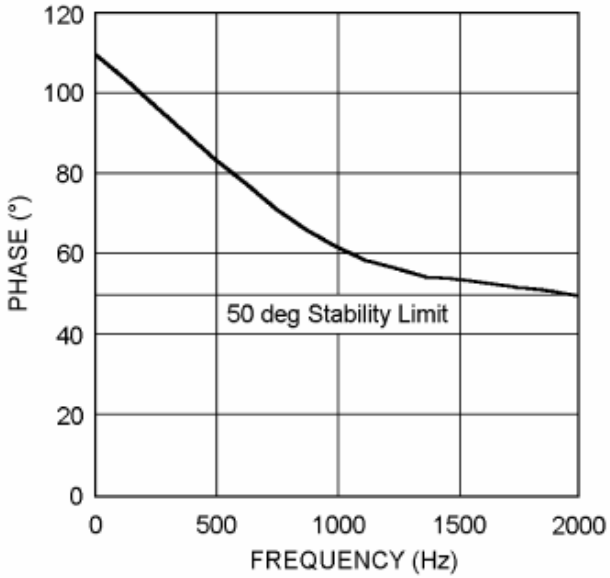
Gain/Phase Response, AV=4
V_{DD}=5V, 8Ω Load, C_{LOAD}=500pF



Phase Margin vs C_{LOAD}, AV=2
V_{DD}=5V, 8Ω Load
Capacitor to gnd on each output

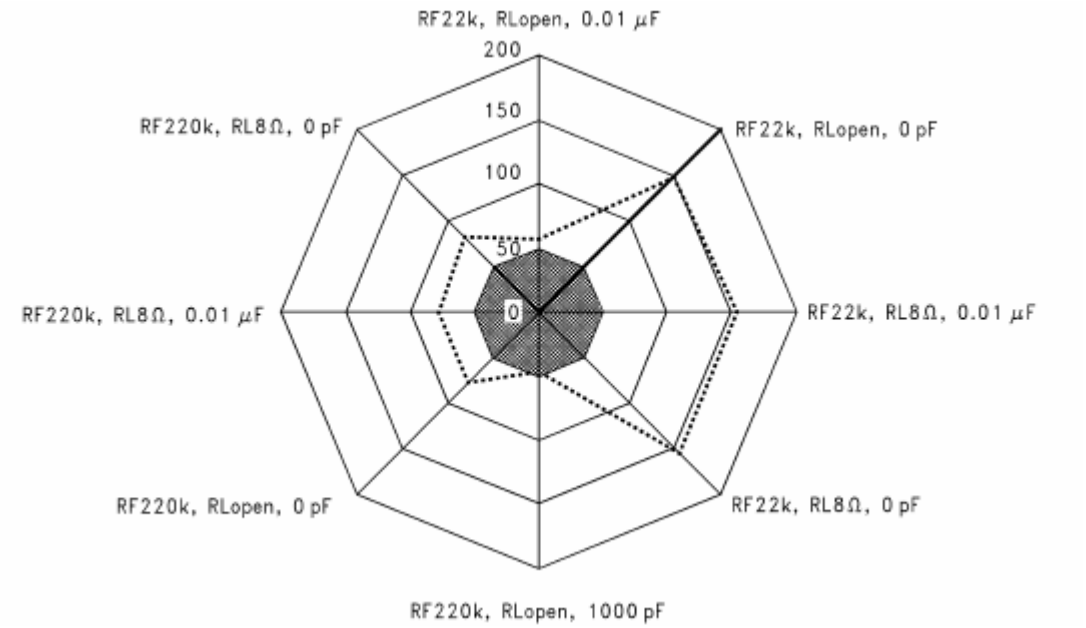


Phase Margin vs C_{LOAD}, AV=4
V_{DD}=5V, 8Ω Load
Capacitor to gnd on each output

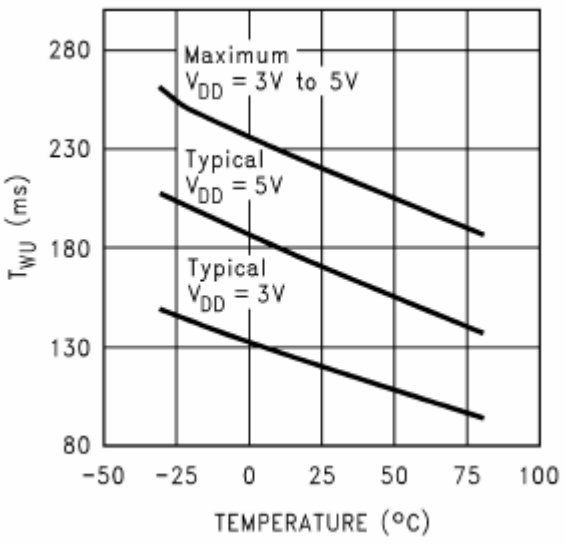


■ Typical Performance Characteristics (Continued)

Phase Margin and Limits vs Application Variables, R_{IN}=22kΩ

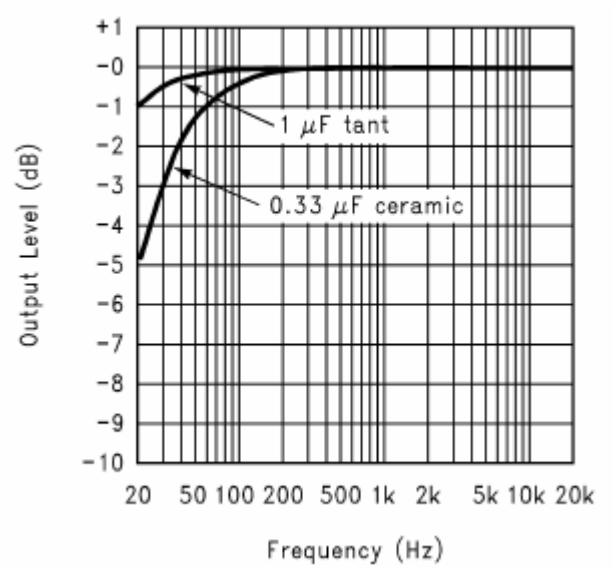


Wake Up Time (Twu)

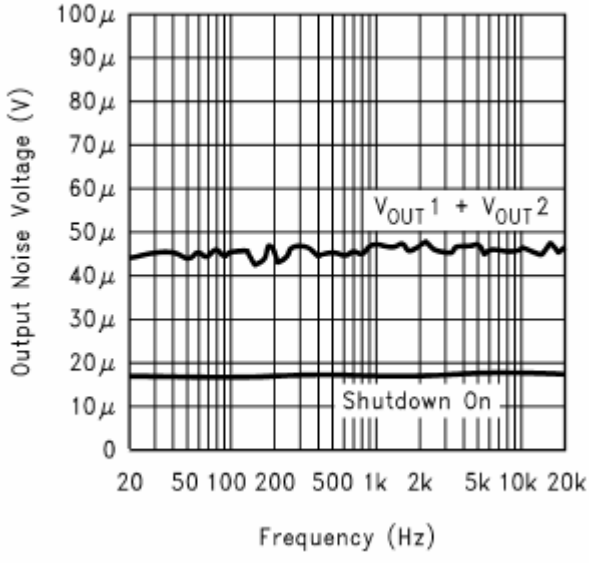


■ Typical Performance Characteristics (Continued)

Frequency Response vs Input Capacitor Size



Noise Floor



■ Application Information

Bridged Configuration Explanation

As shown in Figure1 the OCP7190 has two operational amplifiers internally, allowing for a few different amplifier configurations. The first amplifier's gain is externally configurable, while the second amplifier is internally fixed in a unity-gain, inverting configuration. The closed-loop gain of the first amplifier is set by selecting the ratio of R_f to R_{IN} while the second amplifier's gain is fixed by the two internal 20kΩ resistors. Figure 1 shows that the output of amplifier one serves as the input to amplifier two which results in both amplifiers producing signals identical in magnitude, but out of phase by 180°. Consequently, the differential gain for the IC is

$$A_{VD}=2*(R_f/R_{IN})$$

By driving the load differentially through outputs Vo1 and Vo2, an amplifier configuration commonly referred to as "bridged mode" is established. Bridged mode operation is different from the classical single-ended amplifier configuration where one side of the load is connected to ground.

A bridge amplifier design has a few distinct advantages over the single-ended configuration, as it provides differential drive to the load, thus doubling output swing for a specified supply voltage. Four times the output power is possible as compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or clipped. In order to choose an amplifier's closed-loop gain without causing excessive clipping, please refer to the Audio Power Amplifier Design section.

A bridge configuration, such as the one used in the OCP7190, also creates a second advantage over single-ended amplifiers. Since the differential outputs, Vo1 and Vo2, are biased at half-supply, no net DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, single-ended amplifier configuration. Without an output coupling capacitor, the half-supply bias across the load would result in both increased internal IC power dissipation and also possible loudspeaker damage.

Exposed-Dap Package PCB Mounting Considerations For The OCP7190

The OCP7190's exposed-DAP (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. The OCP7190 package should have its DAP soldered to the grounded copper pad (heatsink) under the OCP7190 (the NC pins, no connect, and ground pins should also be directly connected to this copper pad-heatsink area). The area of the copper pad (heatsink) can be determined from the LD Power Derating graph. If the multiple layer copper heatsink areas are used, then these inner layer or backside copper heatsink areas should be connected to each other with 4(2 x 2) vias. The diameter for these vias should be between 0.013 inches and 0.02 inches with a 0.050inch pitch-spacing. Ensure efficient thermal conductivity by plating through and solderfilling the vias.

Power Dissipation

Power dissipation is a major concern when designing a successful amplifier, whether the amplifier is bridged or single-ended. A direct consequence of the increased power delivered to the load by a bridge amplifier is an increase in internal power dissipation. Since the OCP7190 has two operational amplifiers in one package, the maximum internal power dissipation is 4 times that of a single-ended amplifier. The maximum power dissipation for a given application can be derived from the power dissipation graphs or from Equation 1.

$$P_{DMAX} = 4*(V_{DD})^2/(2\pi^2 R_L) \quad (1)$$

It is critical that the maximum junction temperature T_{JMAX} of 150℃ is not exceeded. T_{JMAX} can be determined from the power derating curves by using P_{DMAX} and the PC board foil area. By adding additional copper foil, the thermal resistance of the application can be reduced, resulting in higher P_{DMAX}. Additional copper foil can be added to any of the leads connected to the OCP7190. Refer to the application information on the OCP7190 reference design board for an example of good heat sinking. If T_{JMAX} still exceeds 150℃, then additional changes must be made. These changes can include reduced supply voltage, higher load impedance, or reduced ambient temperature. Internal power dissipation is a function of output power. Refer to the Typical Performance Characteristics curves for power dissipation information for different output powers and output loading.

Power Supply Bypassing

As with any amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. The capacitor location on both the bypass and power supply pins should be as close to the device as possible. Typical applications employ a 5V regulator with 10 µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for bypassing the supply nodes of the OCP7190. The selection of a bypass capacitor, especially C_{BYPASS}, is dependent upon PSRR requirements, click and pop performance (as explained in the section, Proper Selection of External Components), system cost, and size constraints.

Shutdown Function

In order to reduce power consumption while not in use, the OCP7190 contains a shutdown pin to externally turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. By switching the shutdown pin to ground, the OCP7190 supply current draw will be minimized in idle mode. While the device will be disabled with shutdown pin voltages less than 0.5VD C , the idle current may be greater than the typical value of 0.1 µA. (Idle current is measured with the shutdown pin grounded).

In many applications, a microcontroller or microprocessor output is used to control the shutdown circuitry to provide a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-up resistor. When the switch is closed, the shutdown pin is connected to ground and disables the amplifier. If the switch is open, then the external pull-up resistor will enable the OCP7190. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

Shutdown Output Information

For R_f = 20k ohms:

Z_{OUT1} (between Out1 and GND) = 10k||50k||R_f = 6kΩ

Z_{OUT2} (between Out2 and GND) = 10k||(40k+(10k||R_f)) = 8.3kΩ

Z_{OUT1-2} (between Out1 and Out2) =40k||(10k+(10k||R_f)) = 11.7kΩ

The -3dB roll off for these measurements is 600kHz

Proper Selection of External Components

Proper selection of external components in applications using integrated power amplifiers is critical to optimize device and system performance. While the OCP7190 is tolerant of external component combinations, consideration to component values must be used to maximize overall system quality.

The OCP7190 is unity-gain stable which gives the designer maximum system flexibility. The OCP7190 should be used in low gain configurations to minimize THD+N values, and maximize the signal to noise ratio. Low gain configurations require large input signals to obtain a given output power. Input signals equal to or greater than 1 Vrms are available from sources such as audio codecs. Please refer to the section, Audio Power Amplifier Design, for a more complete explanation of proper gain selection.

Besides gain, one of the major considerations is the closedloop bandwidth of the amplifier. To a large extent, the bandwidth is dictated by the choice of external components shown in Figure 1. The input coupling capacitor, C_{IN}, forms a first order high pass filter which limits low frequency response. This value should be chosen based on needed frequency response for a few distinct reasons.

Selection Of Input Capacitor Size

Large input capacitors are both expensive and space hungry for portable designs. Clearly, a certain sized capacitor is

needed to couple in low frequencies without severe attenuation. But in many cases the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 100Hz to 150Hz. Thus, using a large input capacitor may not increase actual system performance.

In addition to system cost and size, click and pop performance is effected by the size of the input coupling capacitor, C_{IN}. A larger input coupling capacitor requires more charge to reach its quiescent DC voltage (nominally 1/2 V_{DD}). This charge comes from the output via the feedback and is apt to create pops upon device enable. Thus, by minimizing the capacitor size based on necessary low frequency response, turn-on pops can be minimized.

Besides minimizing the input capacitor size, careful consideration should be paid to the bypass capacitor value. Bypass capacitor, C_{BYPASS}, is the most critical component to minimize turn-on pops since it determines how fast the OCP7190 turns on. The slower the OCPD7190's outputs ramp to their quiescent DC voltage (nominally 1/2V_{DD}), the smaller the turn-on pop. Choosing $_{CBYPASS}$ equal to 1.0µF along with a small value of C_{IN}, (in the range of 0.1 µF to 0.39µF), should produce a virtually clickless and popless shutdown function. While the device will function properly, (no oscillations or motorboating), with C_{BYPASS} equal to 0.1 µF, the device will be much more susceptible to turn-on clicks and pops. Thus, a value of C_{BYPASS} equal to 1.0µF is recommended in all but the most cost sensitive designs.

Audio Power Amplifier Design

A 1W/8Ω Audio Amplifier

Given:

Power Output	1 Wrms
Load Impedance	8Ω
Input Level	1 Vrms
Input Impedance	20kΩ
Bandwidth	100Hz~20kHz±0.25dB

A designer must first determine the minimum supply rail to obtain the specified output power. By extrapolating from the Output Power vs Supply Voltage graphs in the Typical Performance Characteristics section, the supply rail can be easily found. A second way to determine the minimum supply rail is to calculate the required V_{OPEAK} using Equation 2 and add the output voltage. Using this method, the minimum supply voltage would be (Vopeak + (V_{ODTOP} + V_{ODBOT})), where V_{ODBOT} and V_{ODTOP} are extrapolated from the Dropout Voltage vs Supply Voltage curve in the **T**ypical Performance Characteristics section.

$$V_{opeak} = \sqrt{(2R_L P_O)} \quad (2)$$

5V is a standard voltage which in most applications is chosen for the supply rail. Extra supply voltage creates headroom that allows the OCP7190 to reproduce peaks in excess of 1 W without producing audible distortion. At this time, the designer must make sure that the power supply choice along with the output impedance does not violate the conditions explained in the Power Dissipation section.

Once the power dissipation equations have been addressed, the required differential gain can be determined from Equation 3.

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (3)$$

$$R_f/R_{IN}=A_{VD}/2$$

From Equation 3, the minimum A_{VD} is 2.83; use A_{VD} = 3.

Since the desired input impedance is 20 kΩ, and with A_{VD} an gain of 3, a ratio of 1.5:1 of R_f to R_{IN} results in an allocation of R_{IN} = 20 kΩ and Rf = 30 Kω. The final design step is to address the bandwidth requirements which must be stated as a pair of -3 dB frequency points. Five times away from a -3 dB point is 0.17 dB down from passband response which is better than the required ±0.25 dB specified.

f_L = 100Hz/5 = 20Hz

f_H = 20kHz * 5 = 100kHz

As stated in the External Components section, R_{IN} in conjunction with C_{IN} create a highpass filter.

C_{IN}≥1/2(2π*20kΩ*20Hz)=0.397µF; use 0.39µF

The high frequency pole is determined by the product of the desired frequency pole, f_H, and the differential gain, $A_{V D}$

With a $A_{V D}$ = 3 and f_H = 100kHz, the resulting GBWP = 300kHz which is much smaller than theOCP7190 GBWP of 2.5MHz. This calculation shows that if a designer has a need to design an amplifier with a higher differential gain, theOCP7190 can still be used without running into bandwidth limitations.

Higher Gain Audio Amplifier

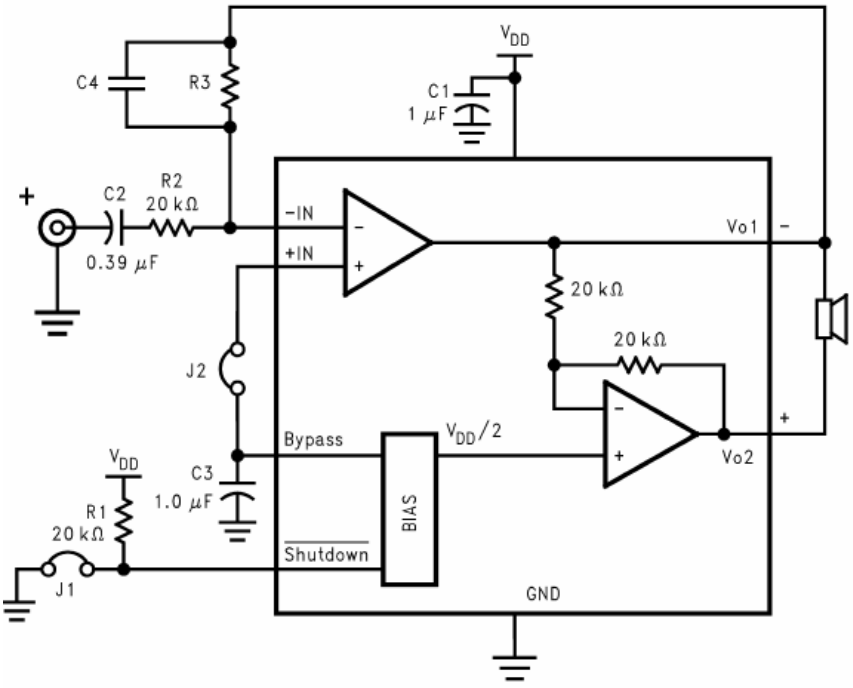


Figure 2

The OCP7190 is unity-gain stable and requires no external components besides gain-setting resistors, an input coupling capacitor, and proper supply bypassing in the typical application. However, if a closed-loop differential gain of greater than 10 is required, a feedback capacitor (C4) may be needed as shown in Figure 2 to bandwidth limit the amplifier. This feedback capacitor creates a low pass filter that eliminates possible high frequency oscillations. Care should be taken when calculating the -3dB frequency in that an incorrect combination of R3 and C4 will cause rolloff before 20kHz. A typical combination of feedback resistor and capacitor that will not produce audio band high frequency rolloff is R_3 = 20kΩ and C4 = 25pf. These components result in a -3dB point of approximately 320 kHz.

Differential Amplifier Configuration For OCP7190

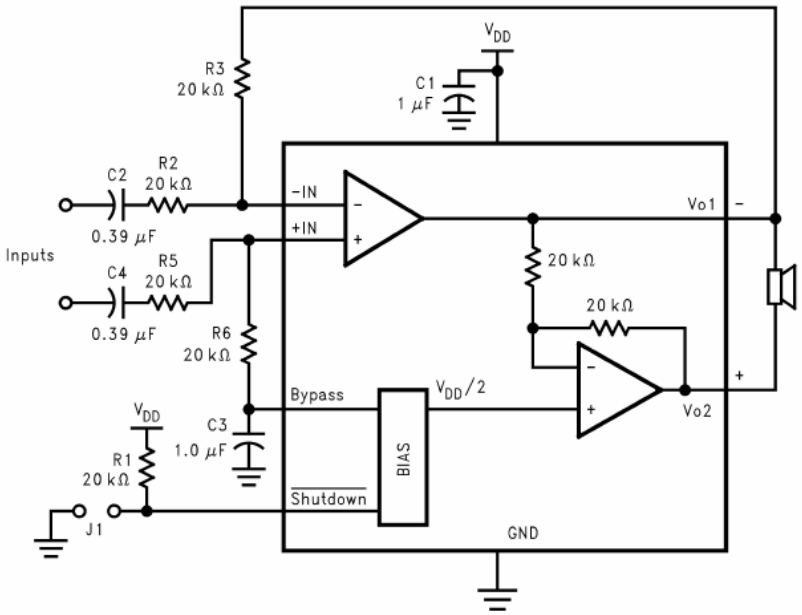


Figure3

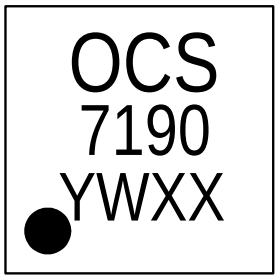
■ Ordering Information

OCP7190X X X

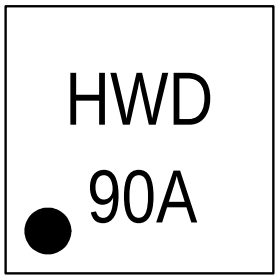
Package:	Packing:	Temperature Grade:
MS: MSOP8L B: BGA	Blank: Tube or Bluk A: Tape & Reel	D: -40~85℃

■ Marking Information

1) MSOP8L

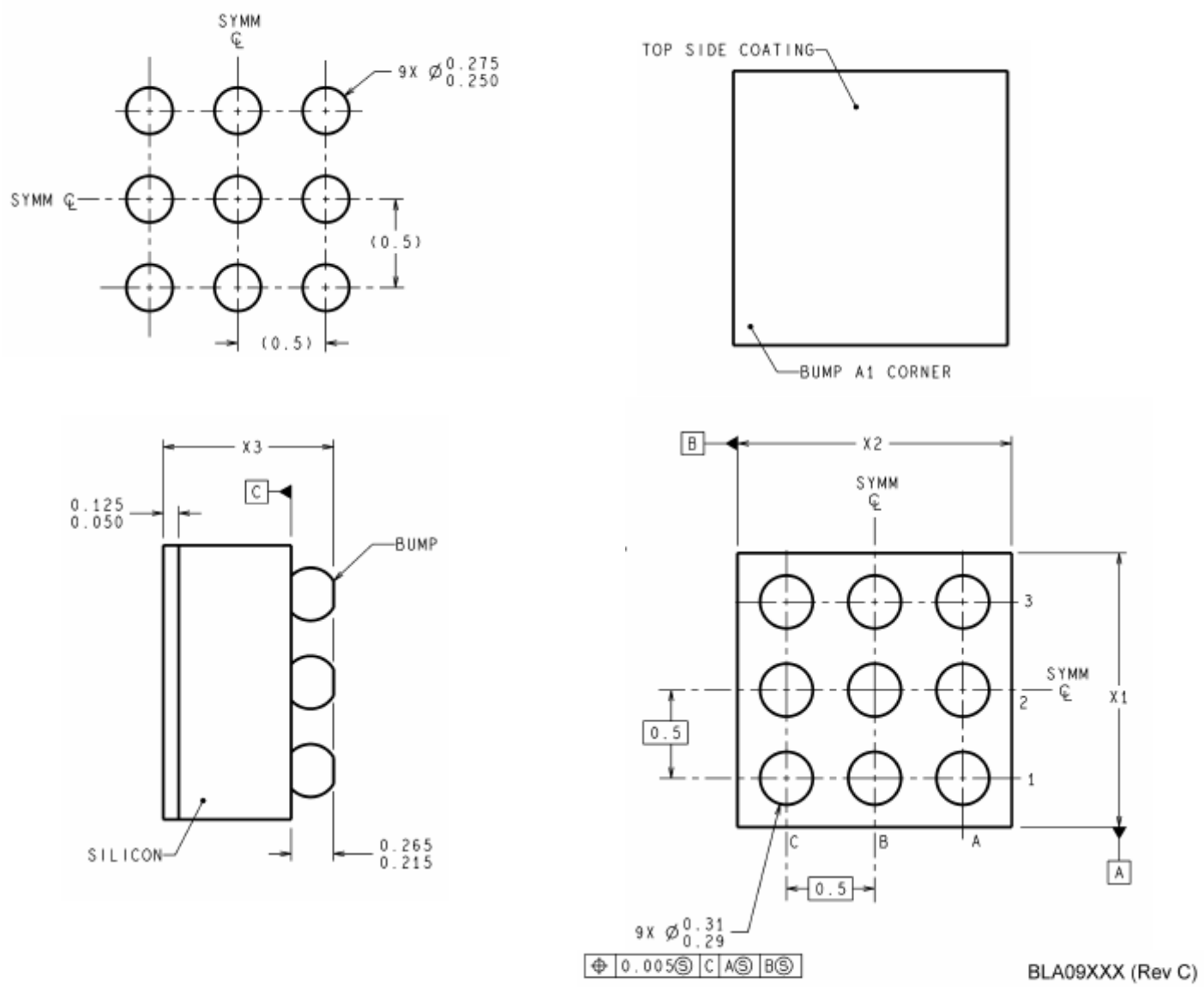


2) BGA



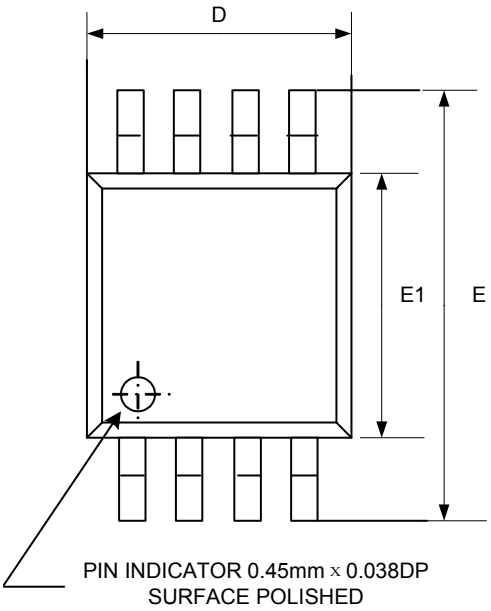
■ Package Information (Dimensions in millimeters)

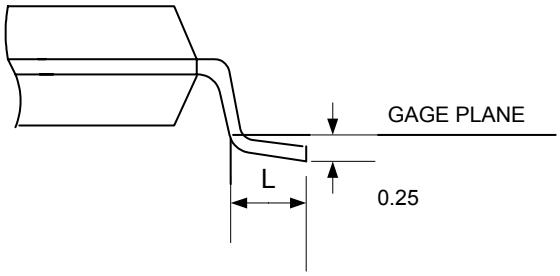
1) 9 bump micro SMD



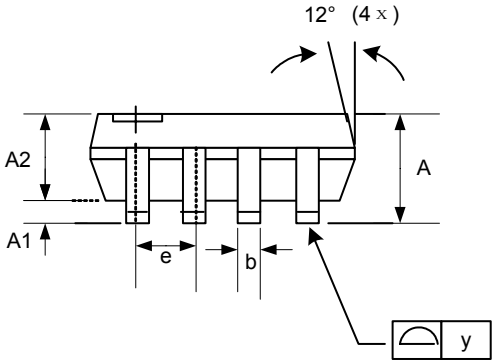
X1=1.514±0.03 X2=1.514±0.03 X3 0.945±0.10

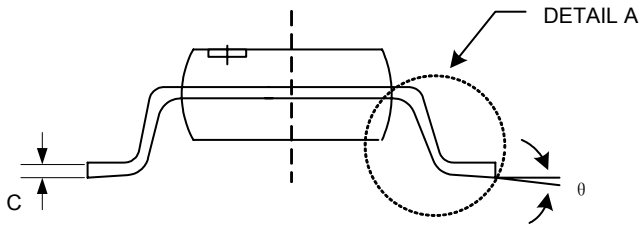
2) MSOP8L





DETAIL A





Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.81	1.02	1.09	0.032	0.040	0.044
A1	0.05		0.15	0.002		0.006
A2	0.76	0.86	0.97	0.030	0.034	0.038
b	0.28	0.30	0.38	0.011	0.012	0.015
C	0.13	0.15	0.23	0.005	0.006	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.80	4.90	5.00	0.189	0.193	0.197
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.0256	
L	0.40	0.53	0.66	0.016	0.021	0.026
y			0.076			0.003
θ	0°	3°	6°	0°	3°	6°