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LT-EL-SR-EU-BPM-0101-03

| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | INITIAL RELEASE | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

NOTES: UNLESS OTHERWISE SPECIFIED  
1. ALL RESISTOR VALUES ARE IN OHMS, 1%, 100PPM.  
2. ALL CAPACITOR VALUES ARE IN MICROFARADS, 50V.  
3. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

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|--|--|--|--|
| <div>UNLESS OTHERWISE SPECIFIED</div> <div>ALL DIMENSIONS ARE IN INCHES</div> <div>DIMENSIONS IN BRACKETS [X.XX] (WHERE PRESENT)</div> <div>ARE MILLIMETERS AND ARE FOR REFERENCE ONLY</div> <div>INTERPRET DRAWING AS PER ANSI Y14.5 0–1994R OR Y32.2.2–1975</div> <div>DIMENSIONAL TOLERANCES</div> <div><div><div>X.<math>\pm</math> 0.030</div><div>.X<math>\pm</math> 0.015</div><div>.XX<math>\pm</math> 0.015</div><div>.XXX<math>\pm</math> 0.005</div></div><div><div>BREAK EDGES &amp; SHARP CORNERS 0.005 MIN. TO 0.030 MAX</div></div></div> |  | <div><div><div><div><div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><div></div><di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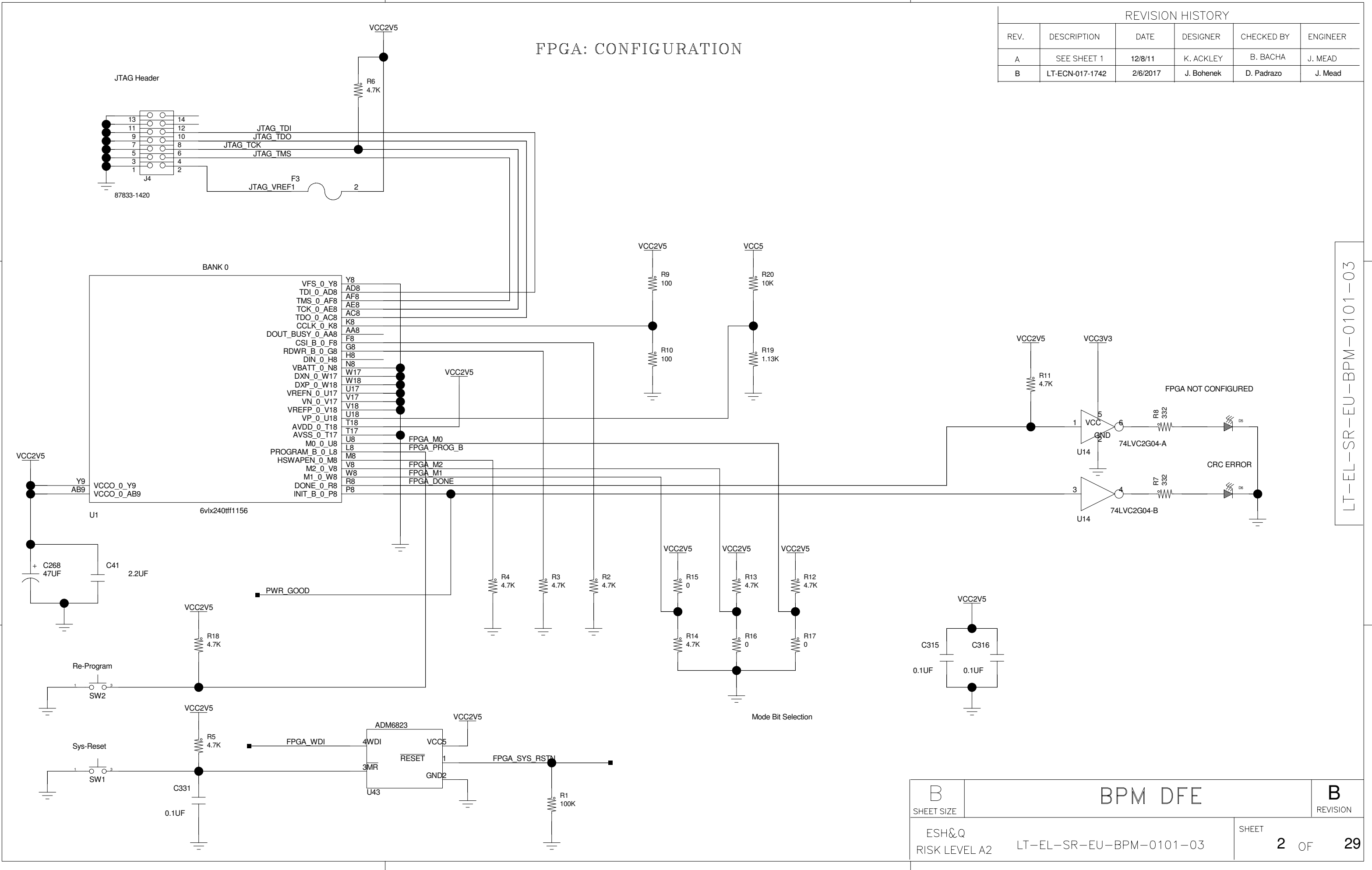
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FPGA: CONFIGURATION

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



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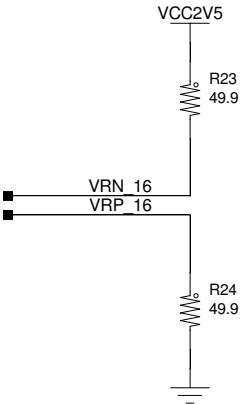
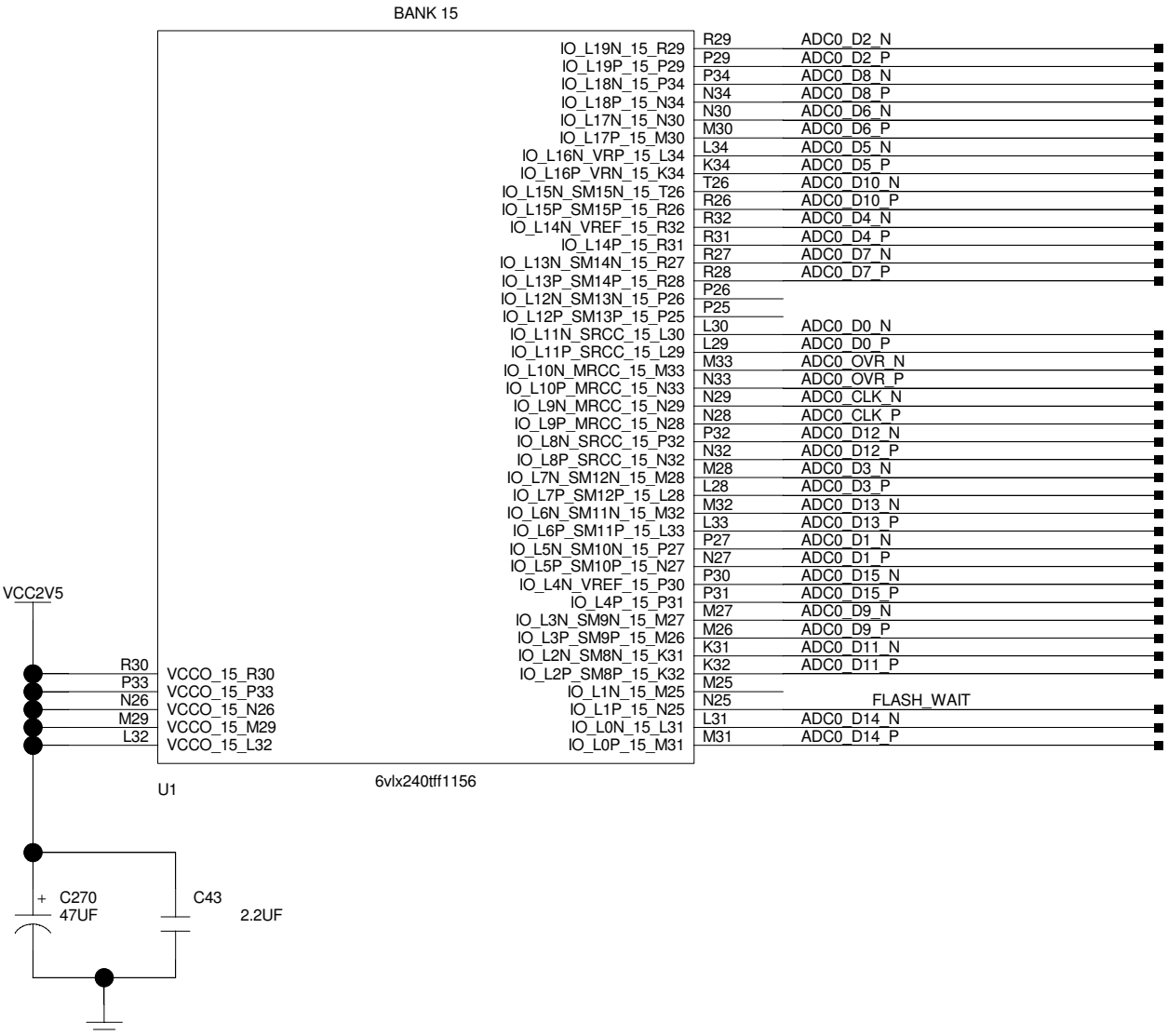
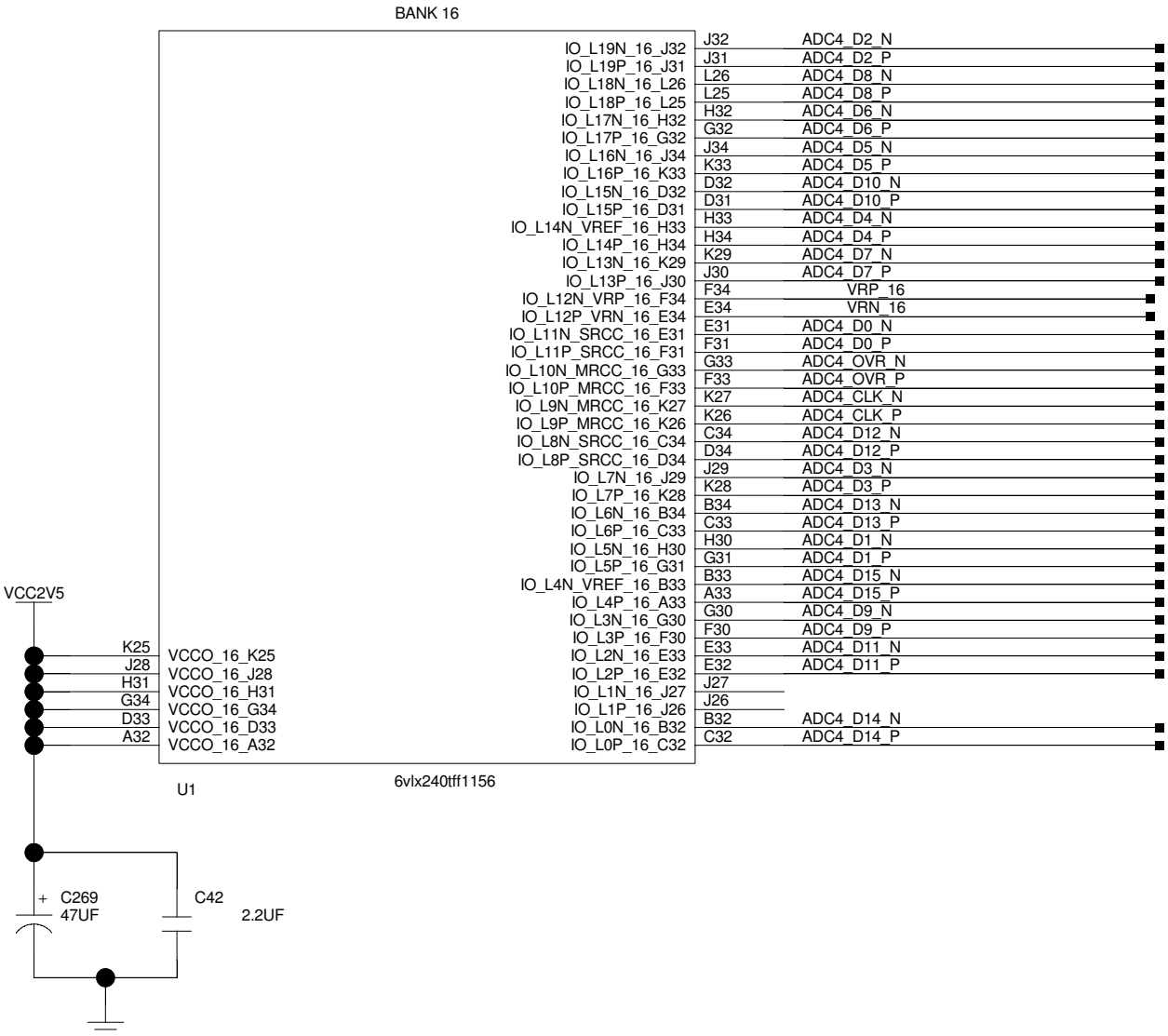
FPGA: AFE INTERFACE

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
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ADC4

ADC0



LT-EL-SR-EU-BPM-0101-03

|            |                         |  |       |          |
|------------|-------------------------|--|-------|----------|
| B          | BPM DFE                 |  |       | B        |
| SHEET SIZE | RISK LEVEL A2           |  |       | REVISION |
| ESH&Q      | LT-EL-SR-EU-BPM-0101-03 |  | SHEET | 3 OF 29  |

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FPGA: AFE INTERFACE

REVISION HISTORY

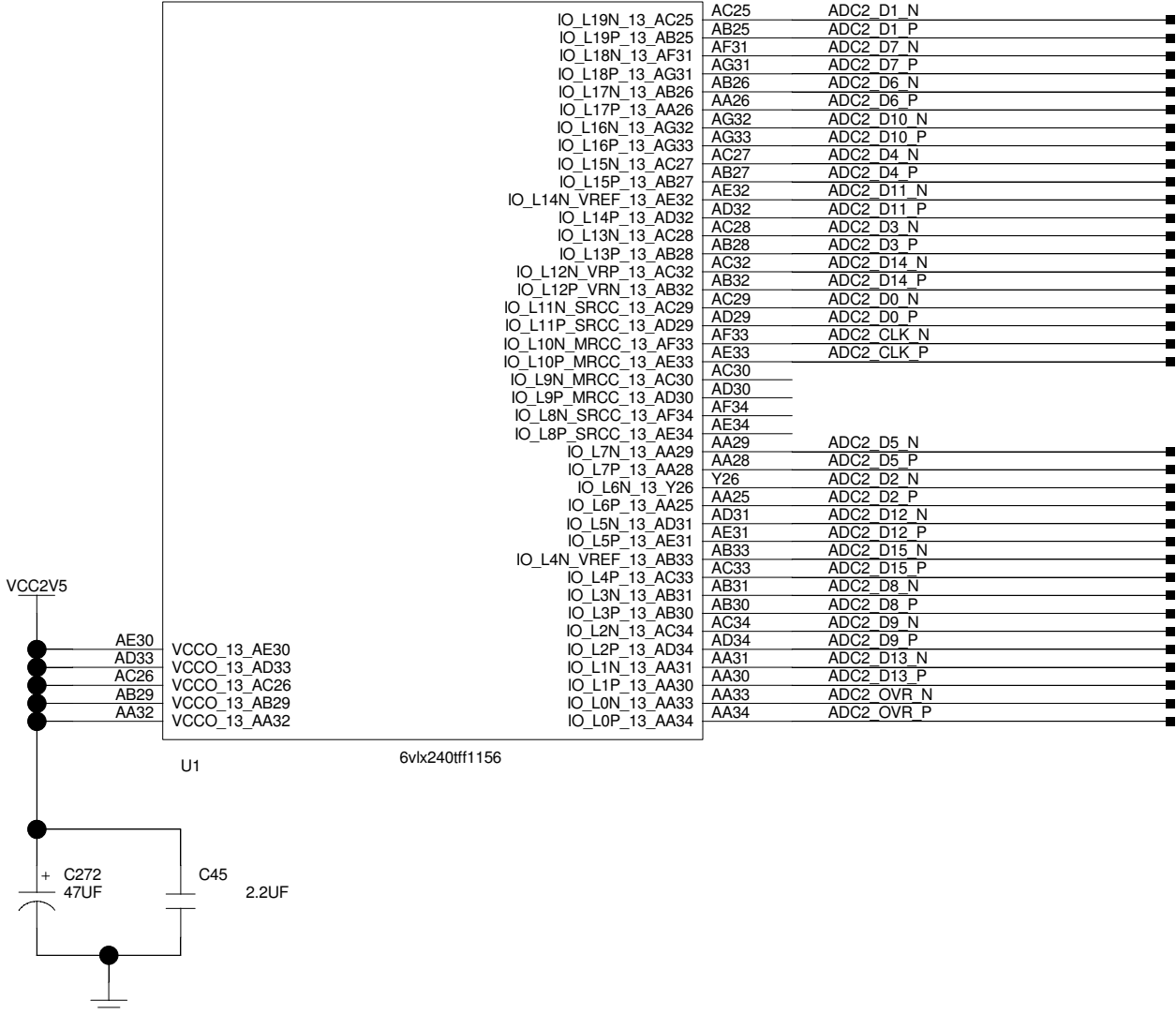
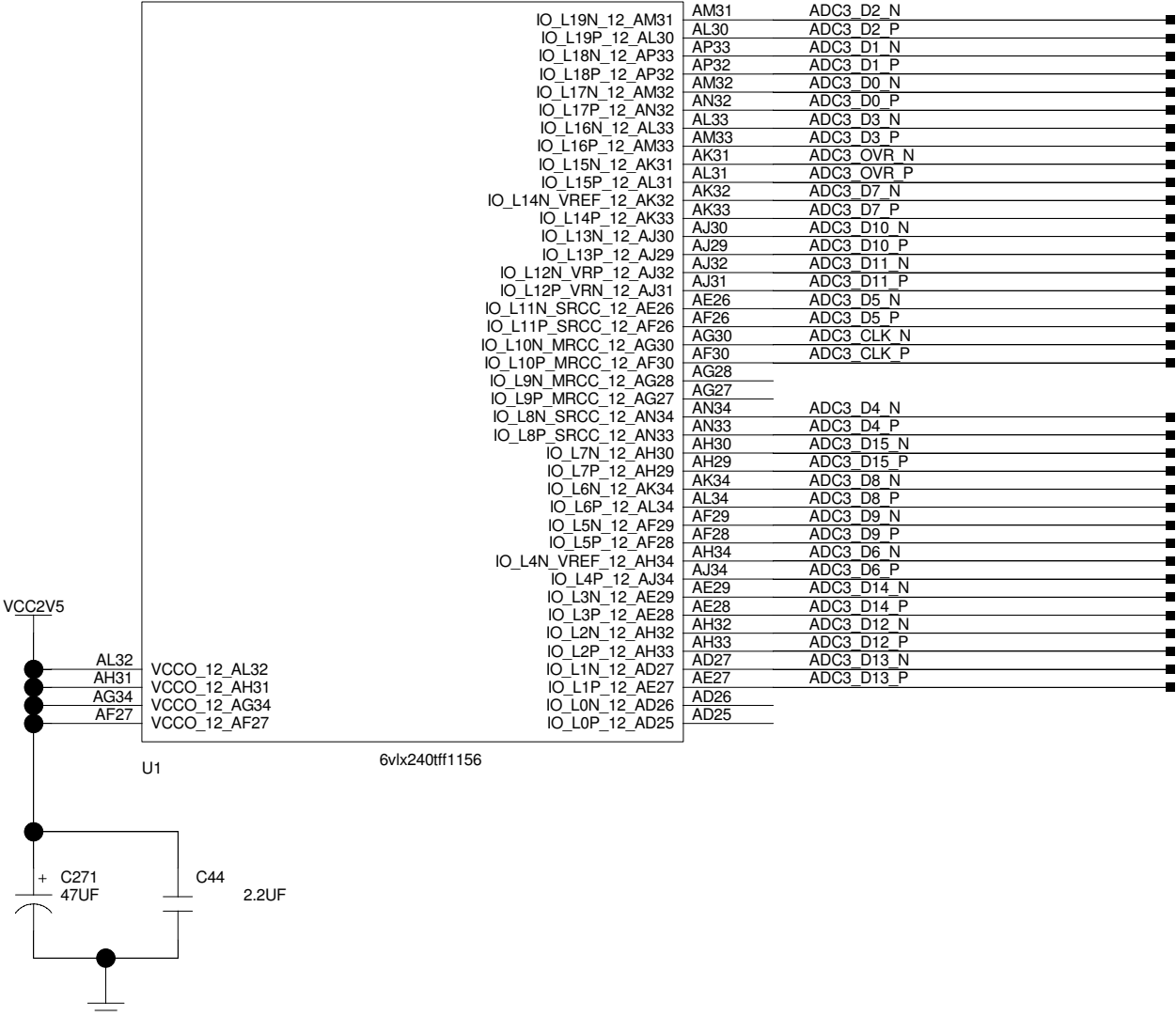
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| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
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ADC3

ADC2

BANK 12

BANK 13



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|------------------------|-------------------------|--|---------------|----|
| B                      | BPM DFE                 |  |               | B  |
| SHEET SIZE             | REVISION                |  |               |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>4 OF | 29 |

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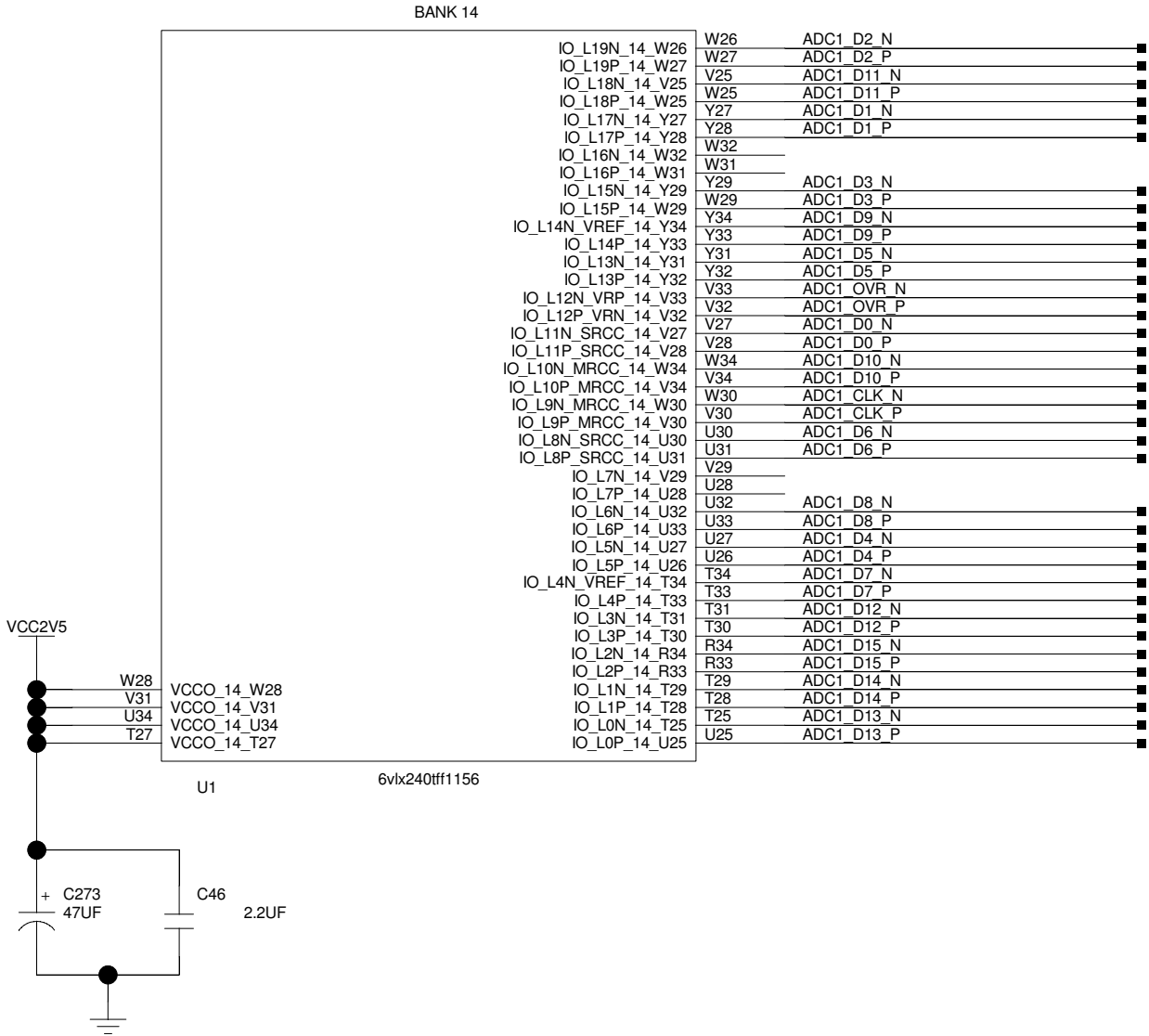
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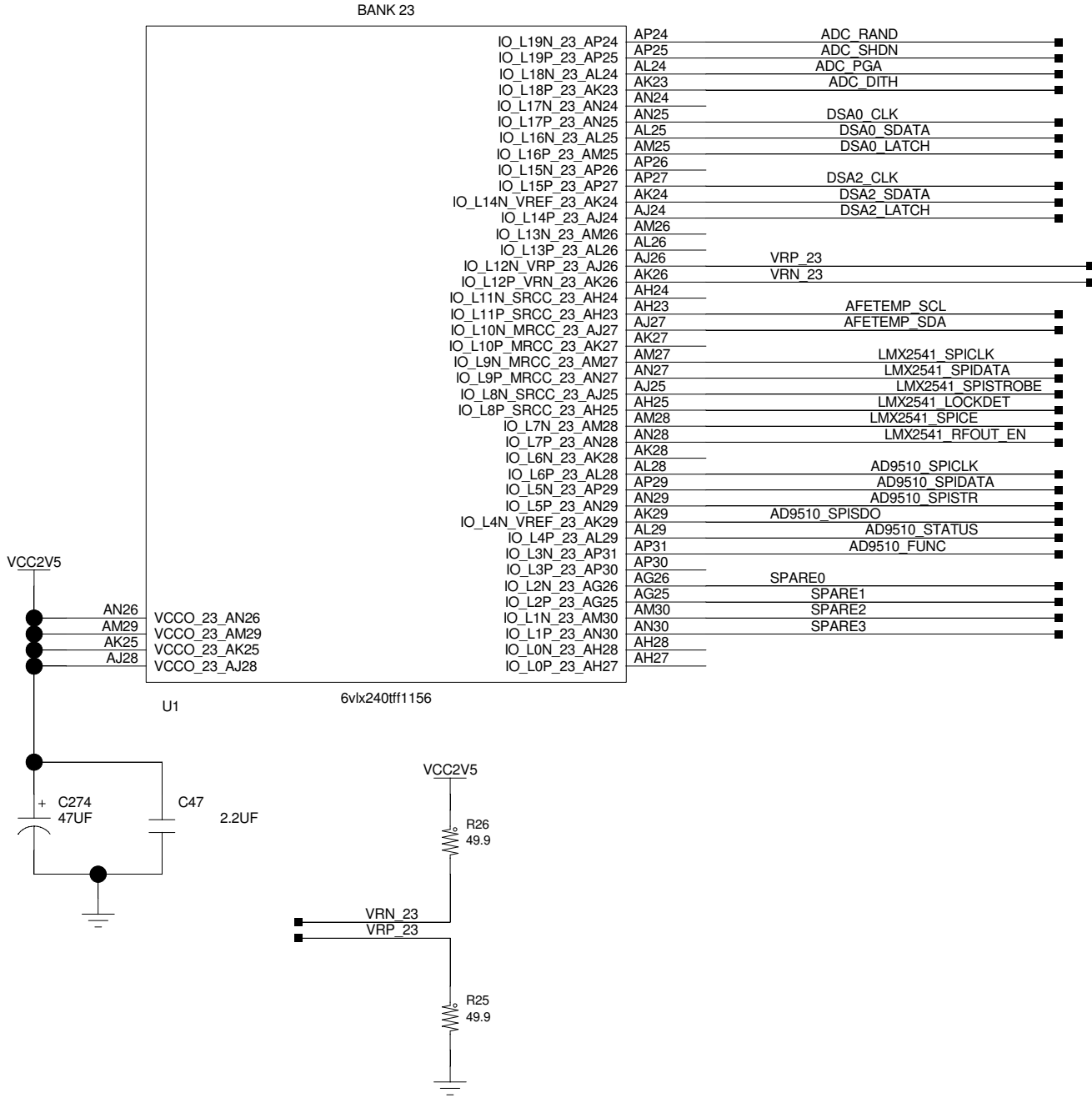
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FPGA: AFE INTERFACE

ADC1



AFE STATUS/CONTROL



LT-EL-SR-EU-BPM-0101-03

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
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|---------------|-------------------------|--|-------|---------|
| B             | BPM DFE                 |  |       | B       |
| SHEET SIZE    | REVISION                |  |       |         |
| ESH&Q         | LT-EL-SR-EU-BPM-0101-03 |  | SHEET | 5 OF 29 |
| RISK LEVEL A2 |                         |  |       |         |

C

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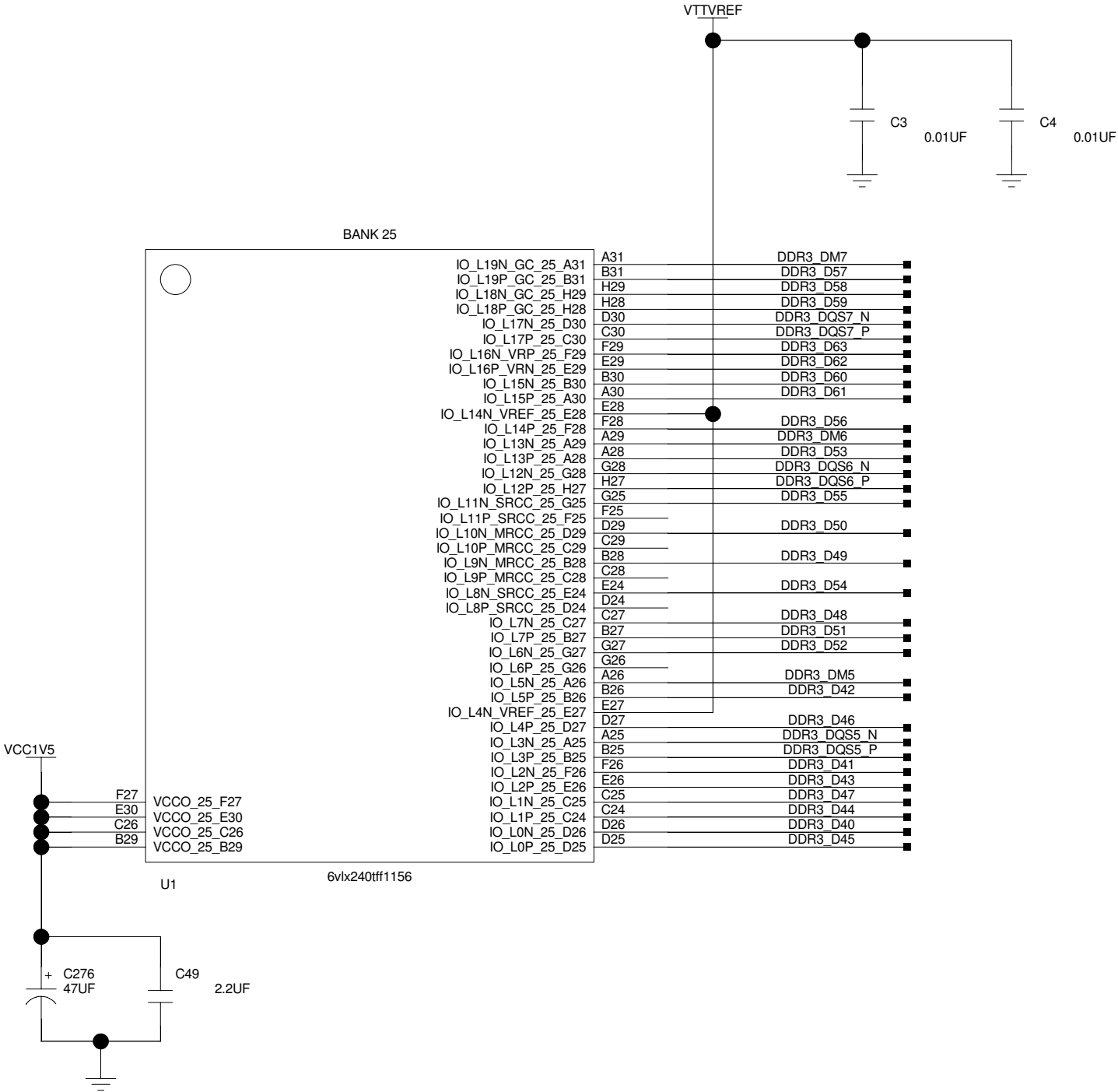
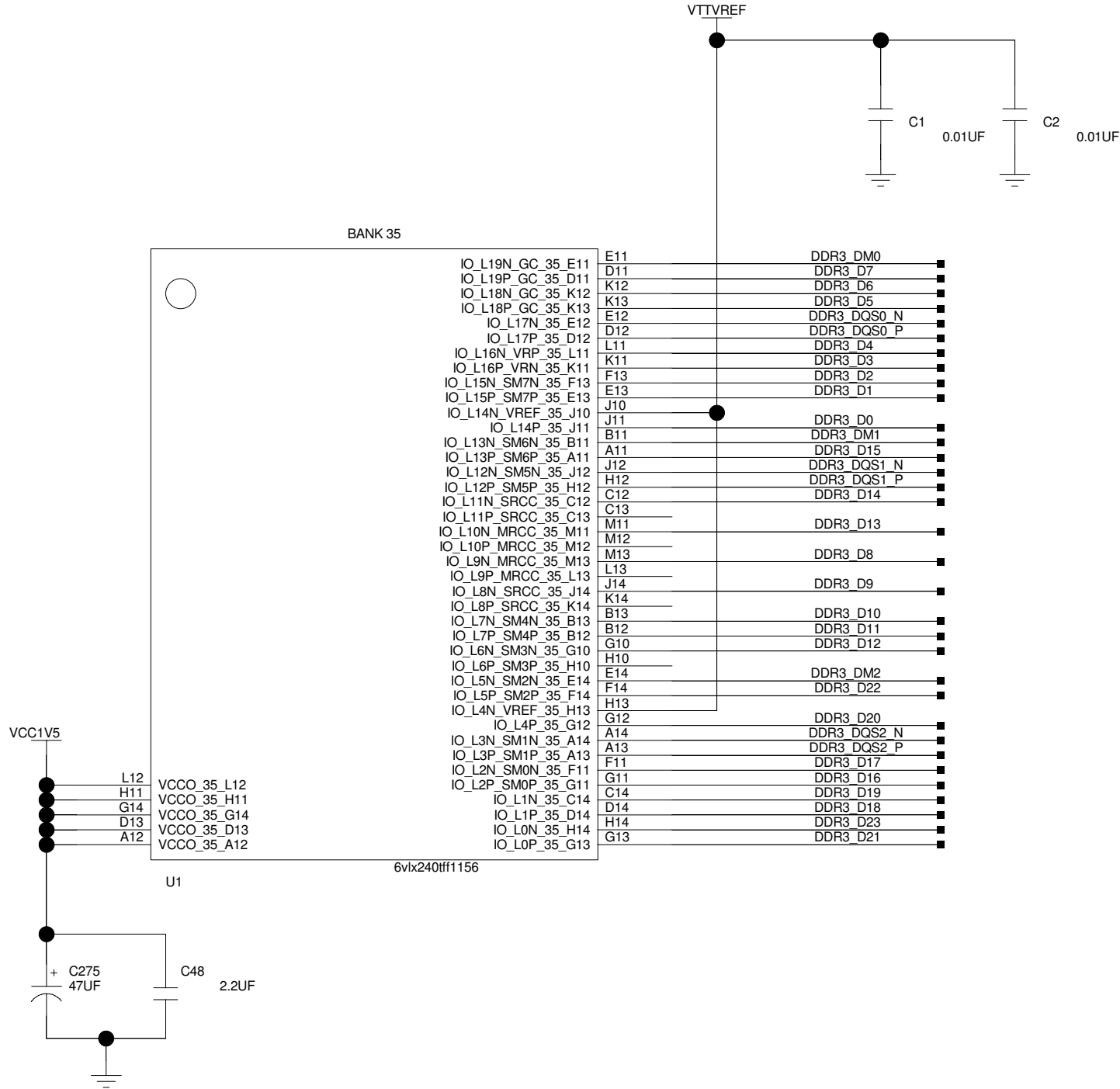
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FPGA: DDR3 MEMORY

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
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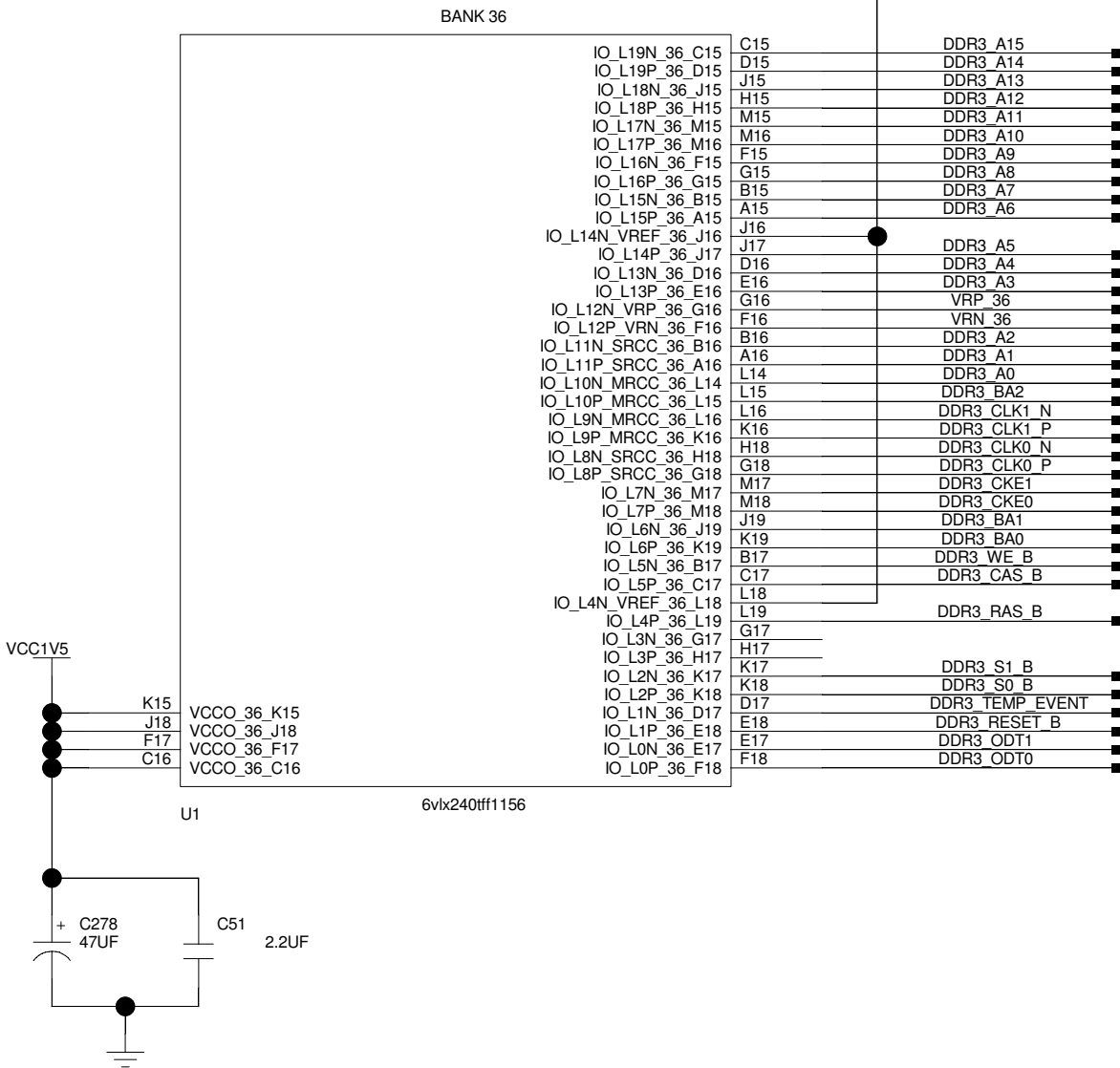
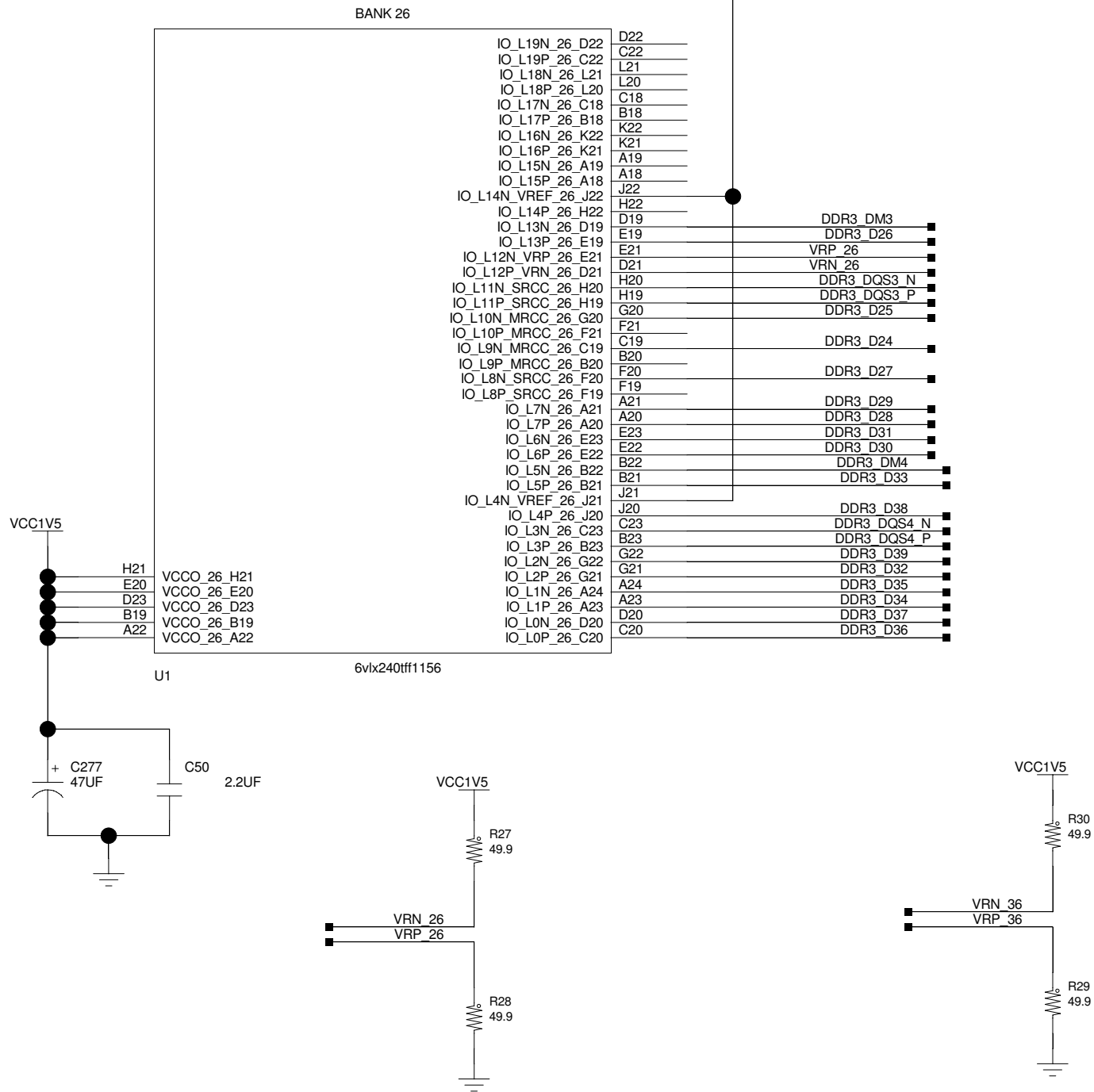
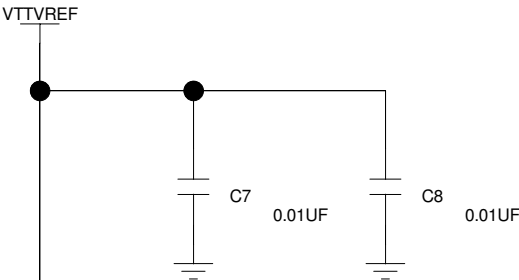
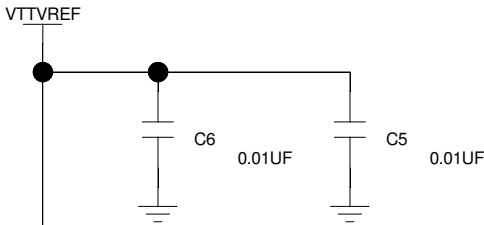
LT-EL-SR-EU-BPM-0101-03



FPGA: DDR3 MEMORY

REVISION HISTORY

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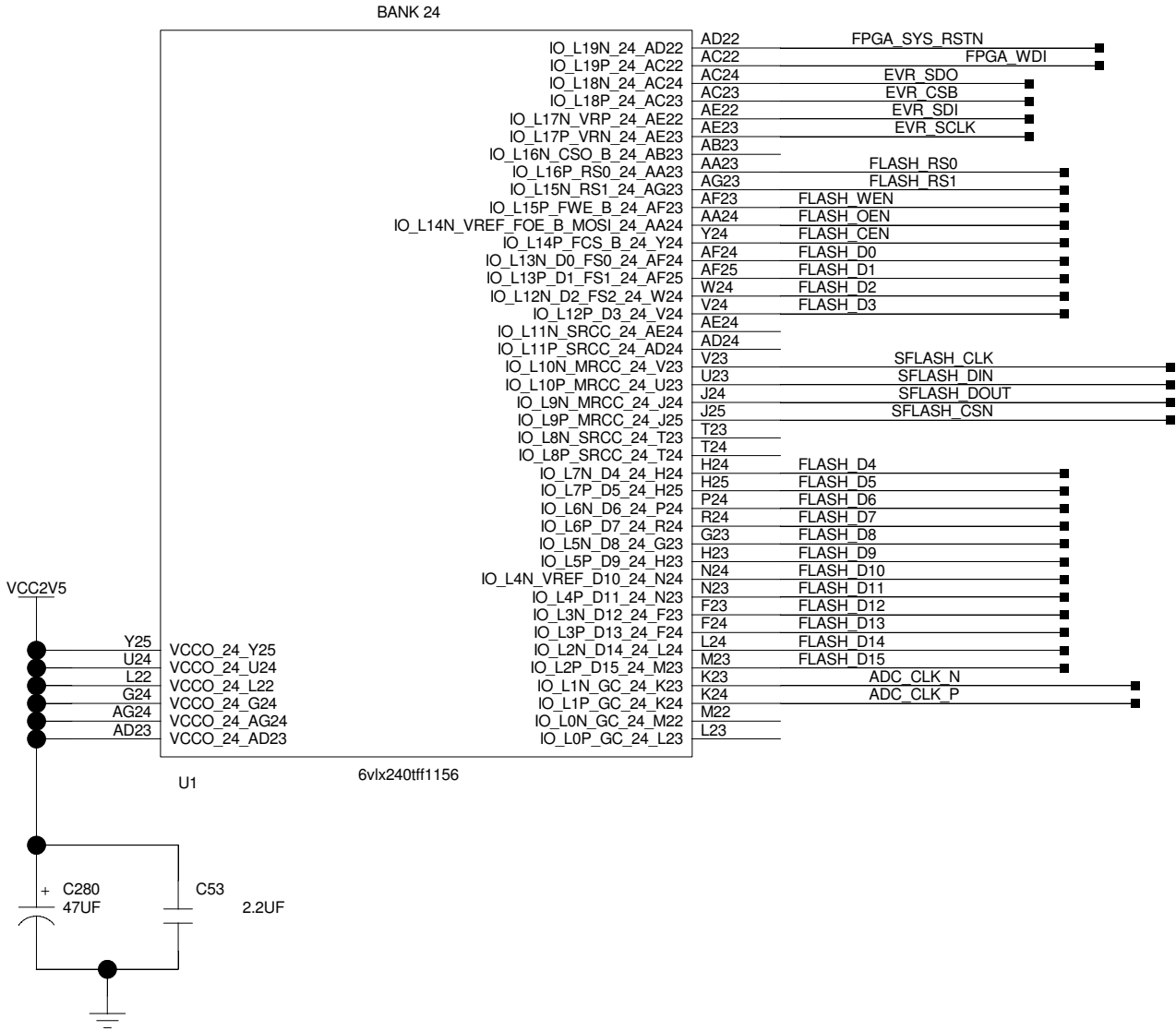
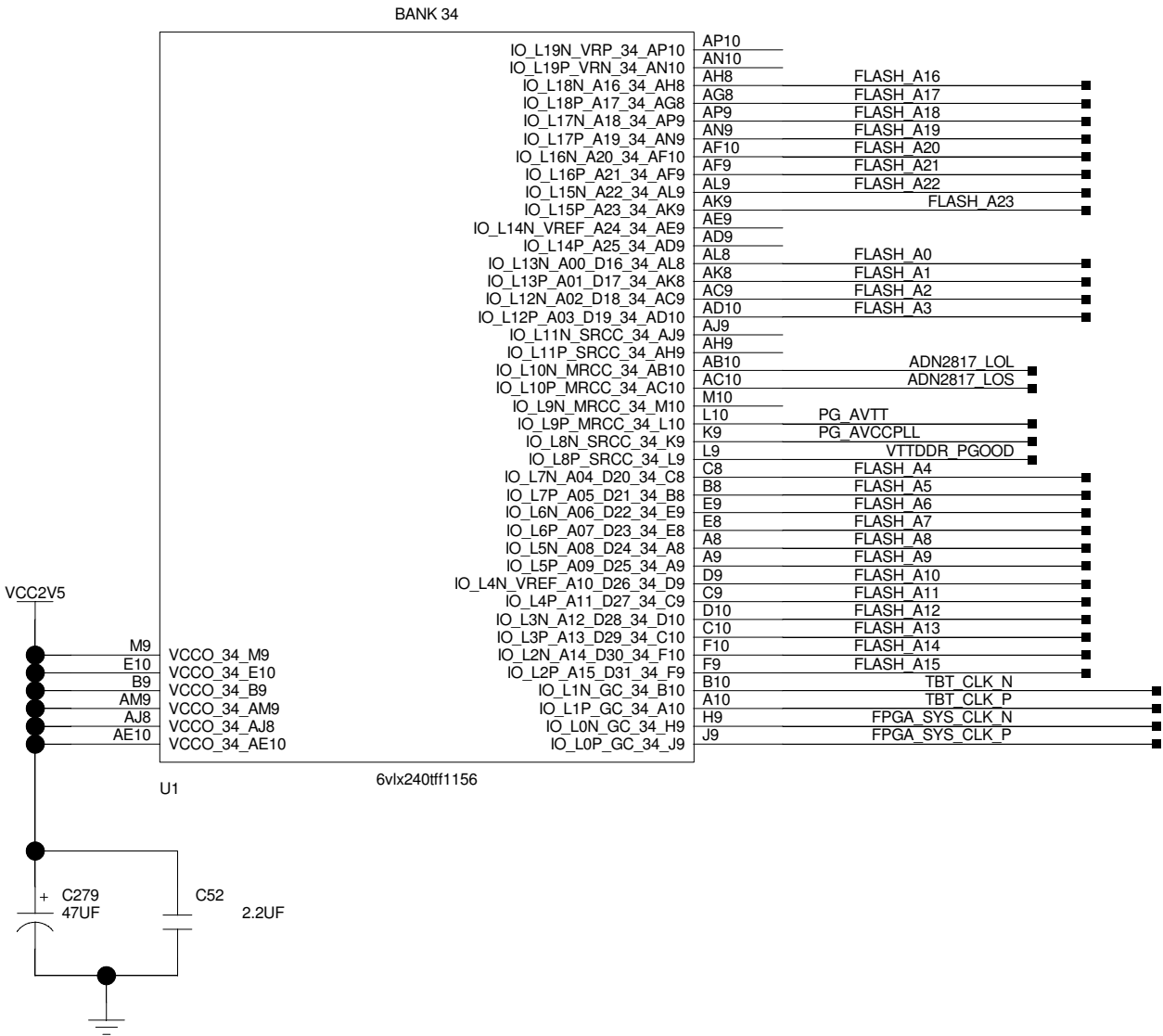


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FPGA: BPI FLASH

REVISION HISTORY

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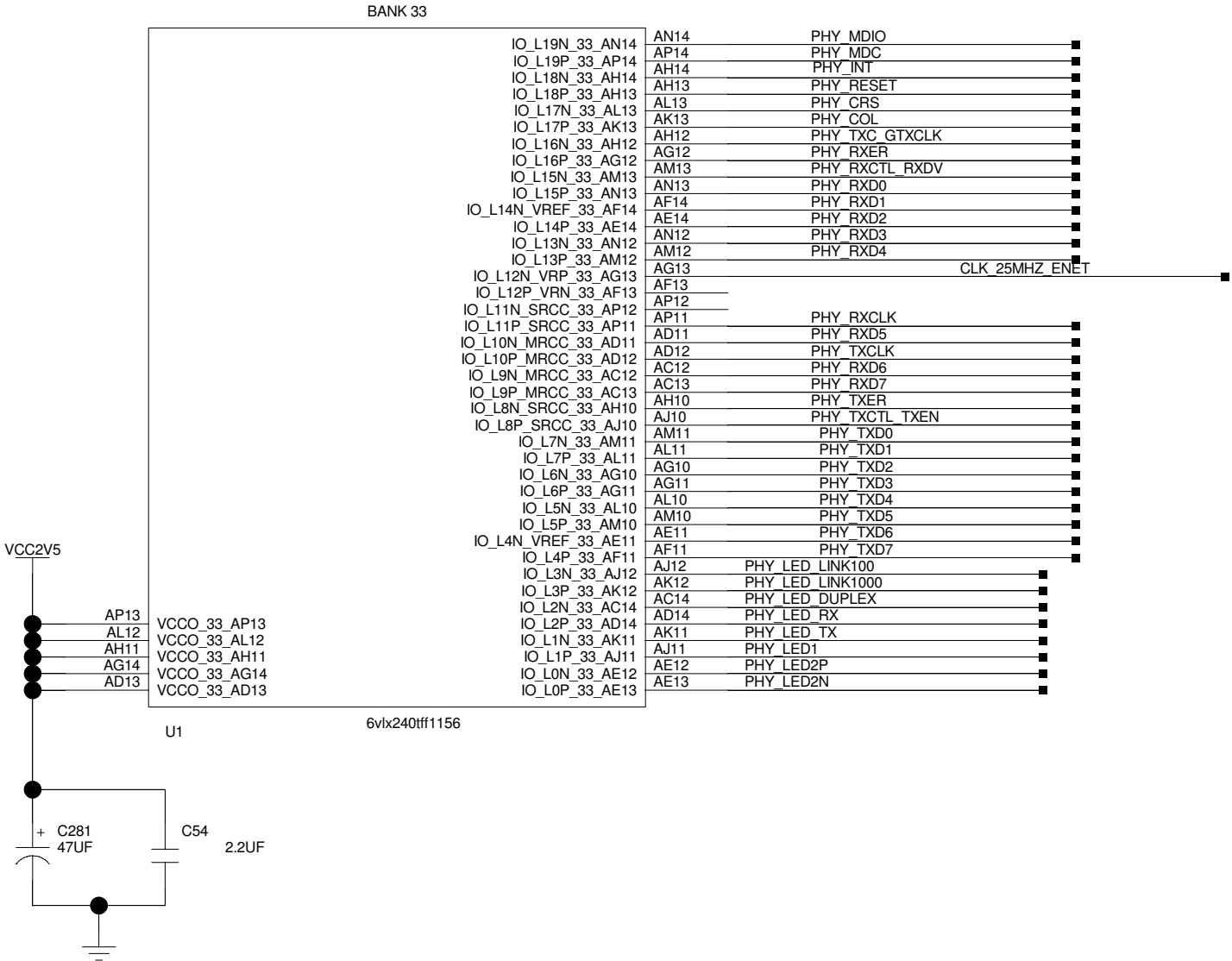
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| B                      | BPM DFE                 |       |      | B  |
| SHEET SIZE             | REVISION                |       |      |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 | SHEET | 8 OF | 29 |



FPGA: ETHERNET

REVISION HISTORY

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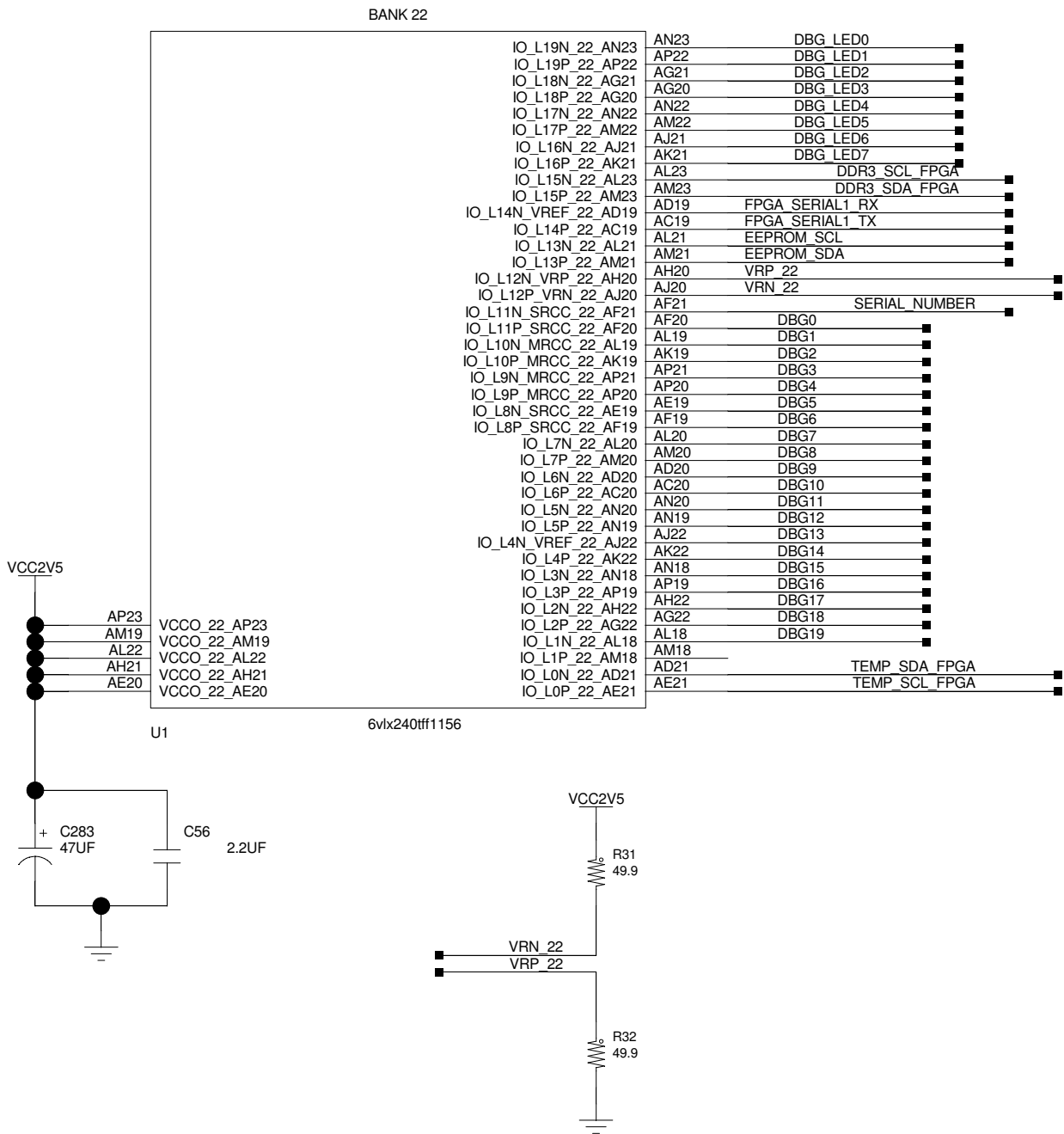
LT-EL-SR-EU-BPM-0101-03

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|---------------|-------------------------|--|-------|---------|
| B             | BPM DFE                 |  |       | B       |
| SHEET SIZE    | REVISION                |  |       |         |
| ESH&Q         | LT-EL-SR-EU-BPM-0101-03 |  | SHEET | 9 OF 29 |
| RISK LEVEL A2 |                         |  |       |         |

FPGA: MISC

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



LT-EL-SR-EU-BPM-0101-03

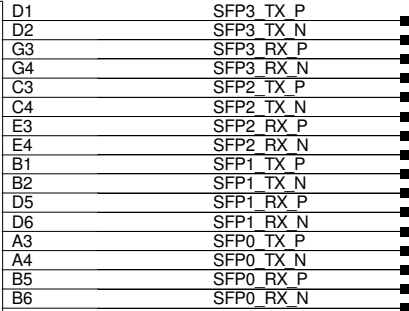
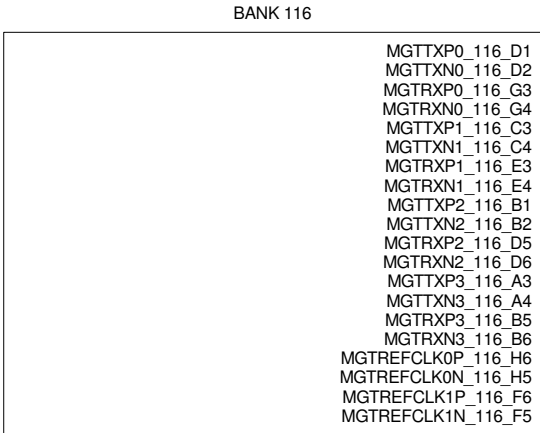
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|------------------------|-------------------------|--|----------------|----|
| B                      | BPM DFE                 |  |                | B  |
| SHEET SIZE             | REVISION                |  |                |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>10 OF | 29 |

| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

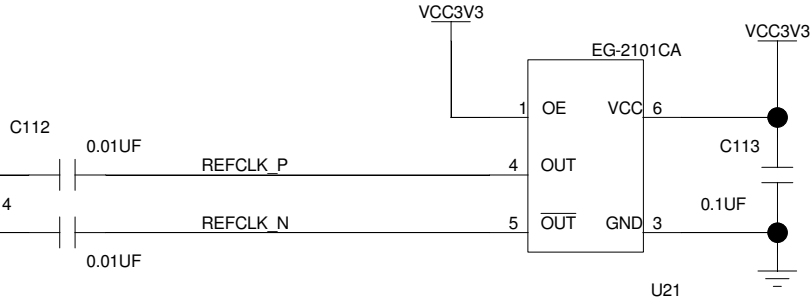
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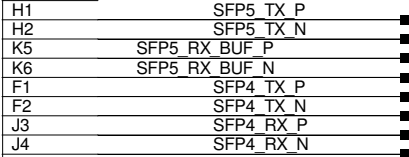
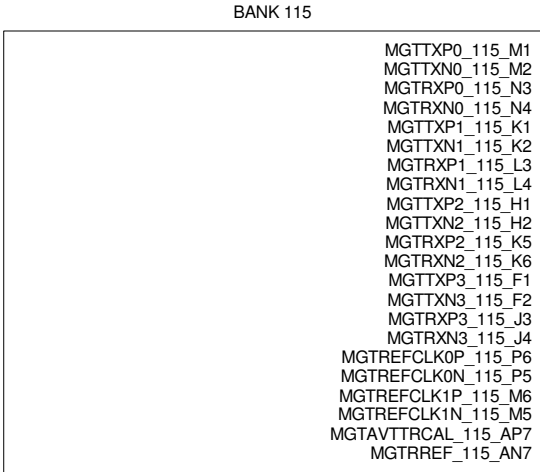
North Banks



FPGA: GTX



U1 6vlx240tff1156

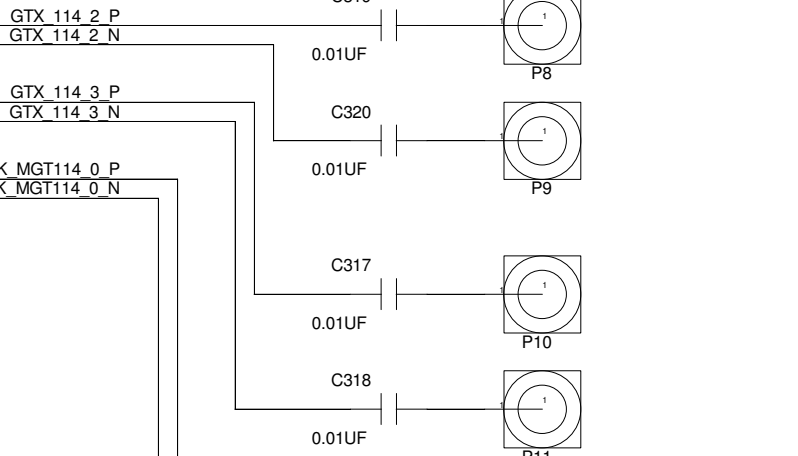
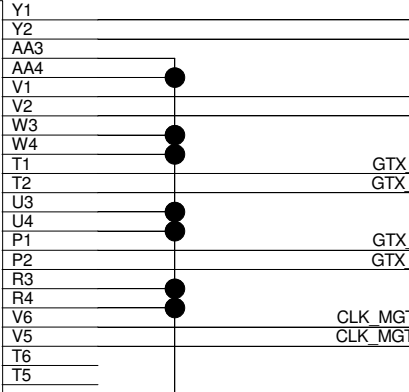
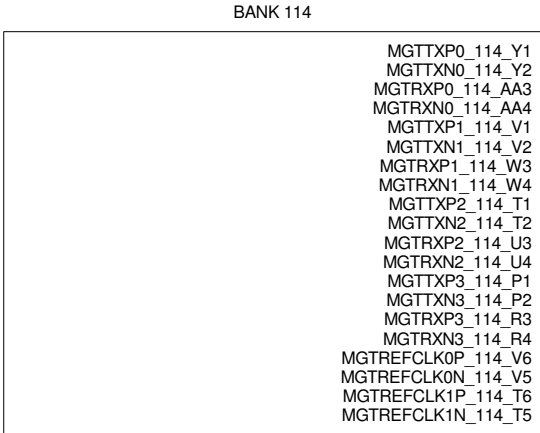


MGT\_AVTT



U1 6vlx240tff1156

South Banks



C110

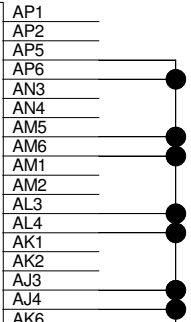
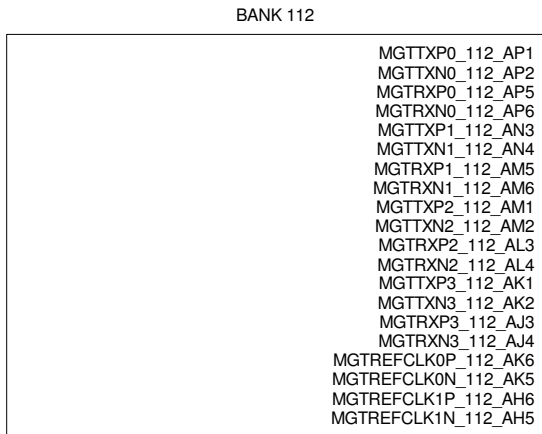
From Clk Cleaner (p23)

C111

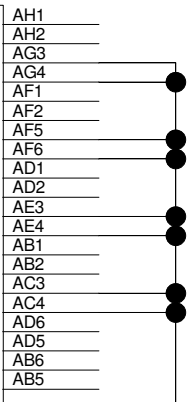
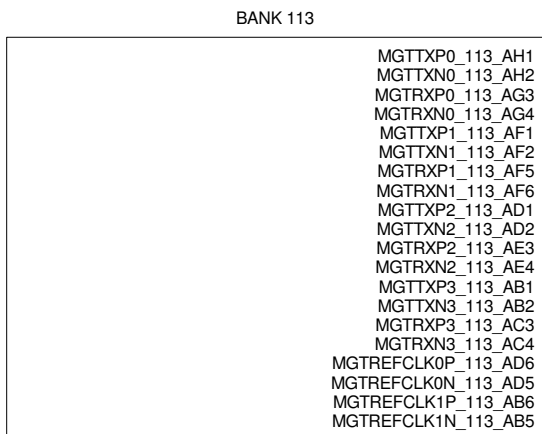
CLN\_CLK\_P

CLN\_CLK\_N

South Banks



U1 6vlx240tff1156



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LT-EL-SR-EU-BPM-0101-03

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|                        |                         |  |                   |
|------------------------|-------------------------|--|-------------------|
| B<br>SHEET SIZE        | BPM DFE                 |  | B<br>REVISION     |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>11 OF 29 |

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FPGA: POWER

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

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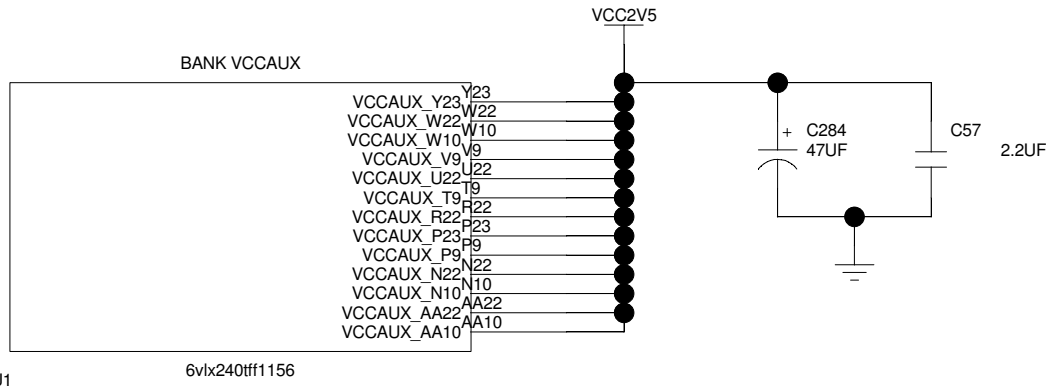
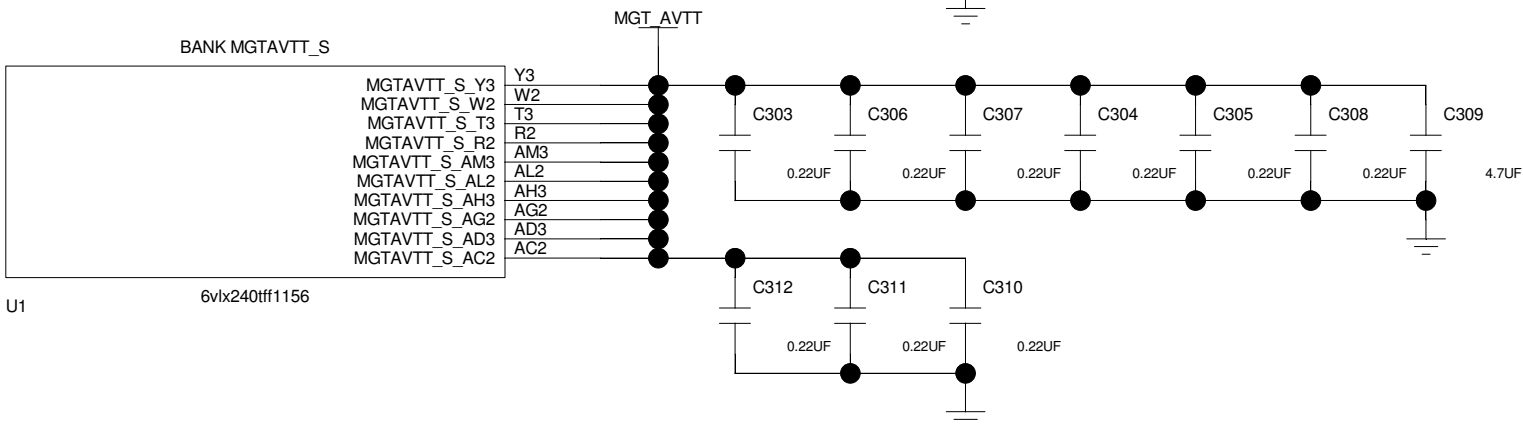
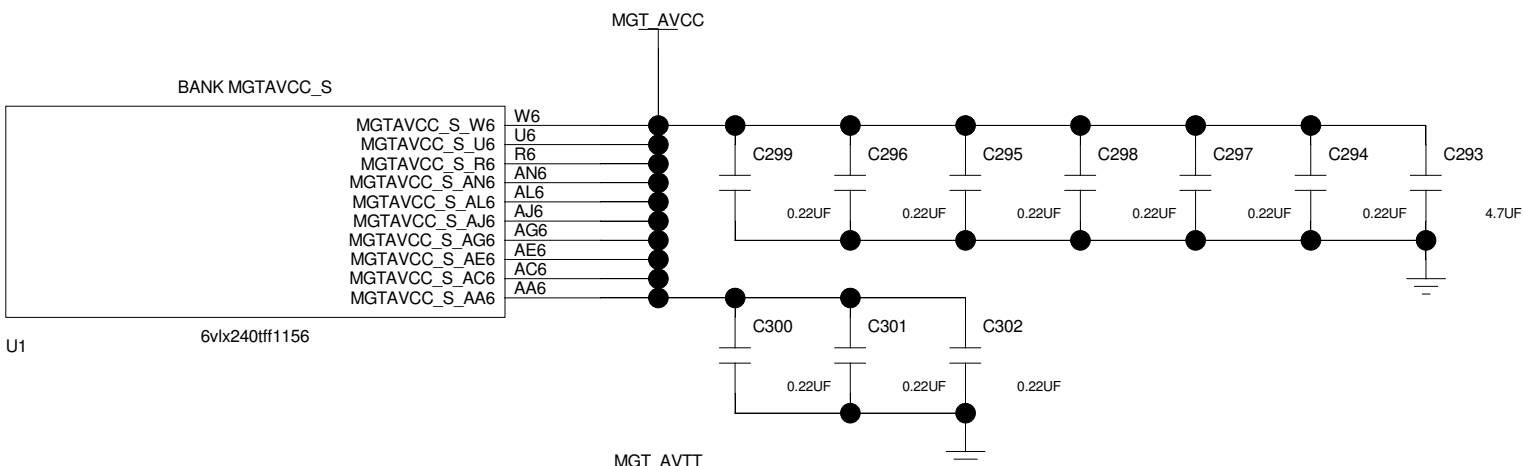
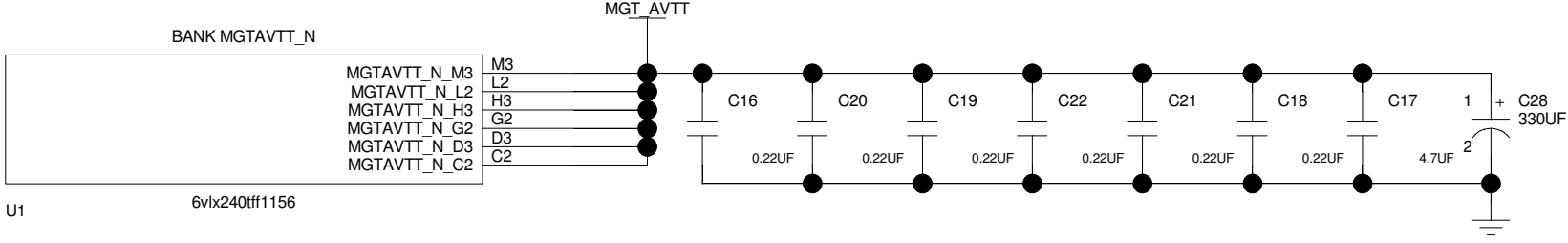
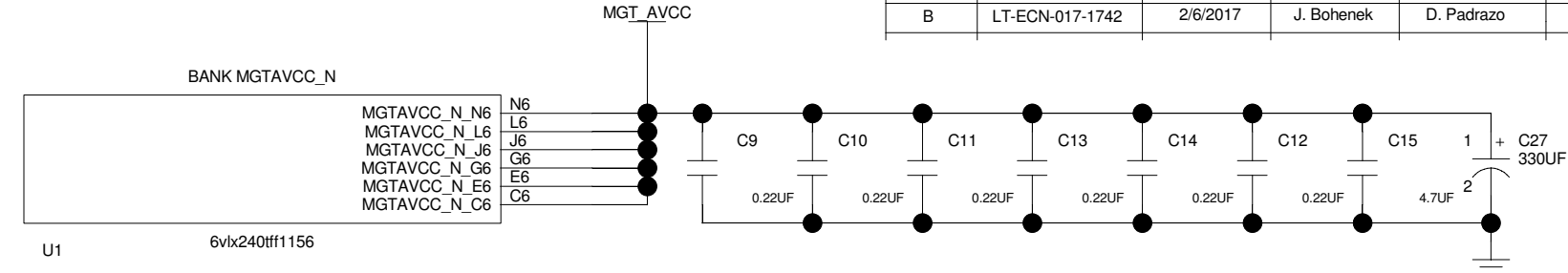
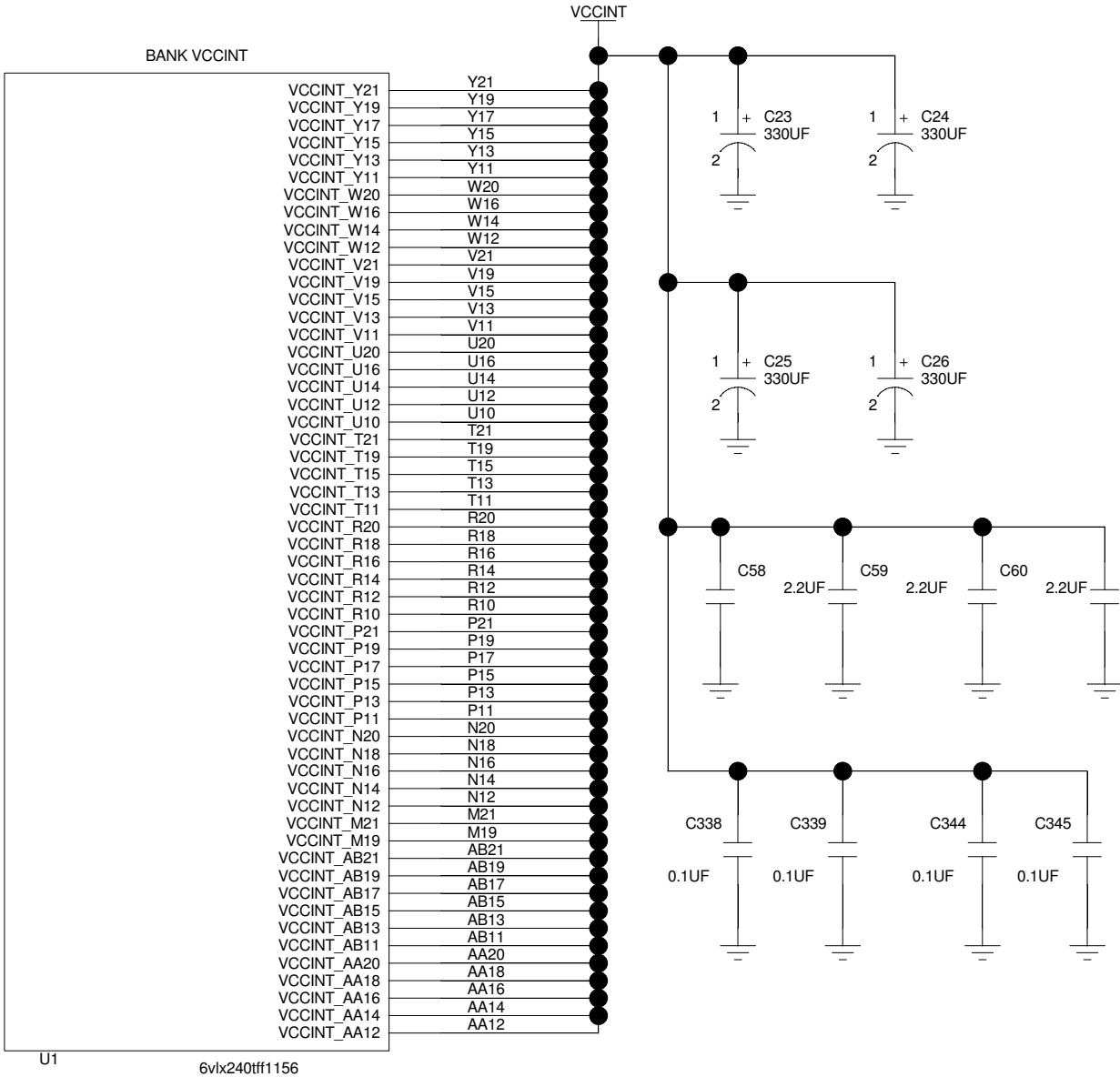
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LT-EL-SR-EU-BPM-0101-03



|                        |                         |  |                |    |
|------------------------|-------------------------|--|----------------|----|
| B                      | BPM DFE                 |  |                | B  |
| SHEET SIZE             | REVISION                |  |                |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>12 OF | 29 |

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LT-EL-SR-EU-BPM-0101-03

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REVISION

SHEET  
13 OF 29

BPM DFE

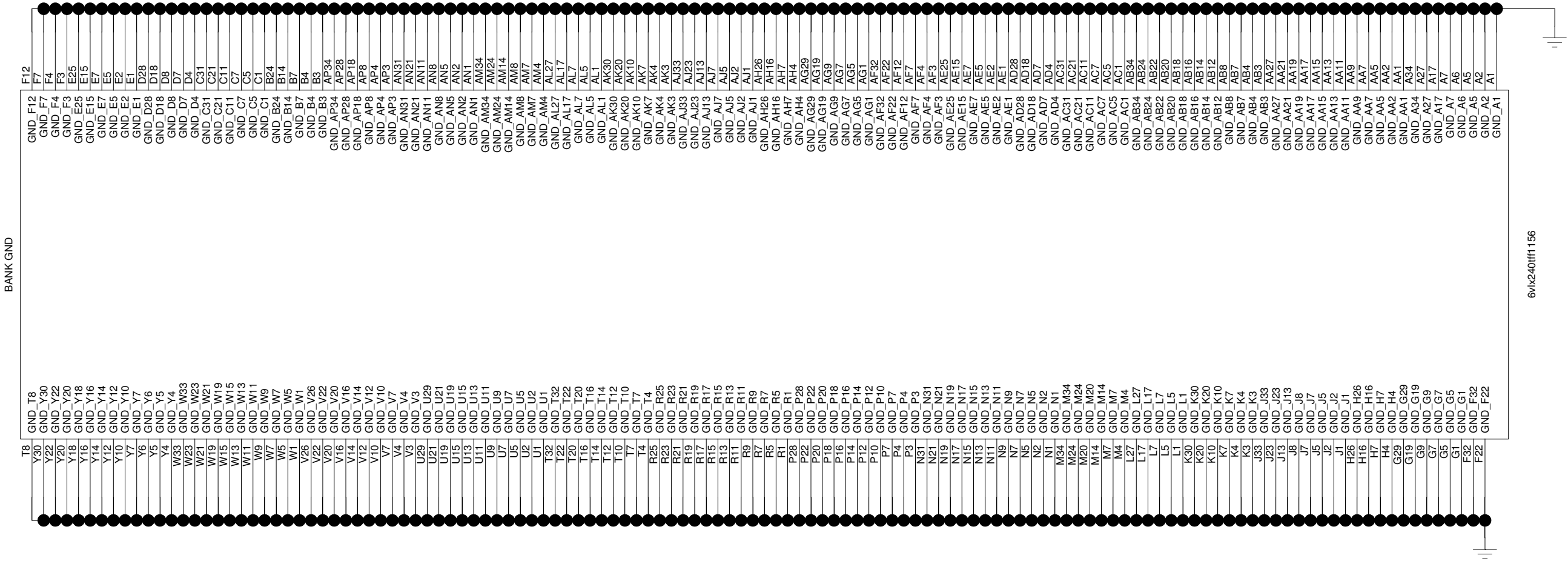
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SHEET SIZE

ESH&Q  
RISK LEVEL A2 LT-EL-SR-EU-BPM-0101-03

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

FPGA: GND





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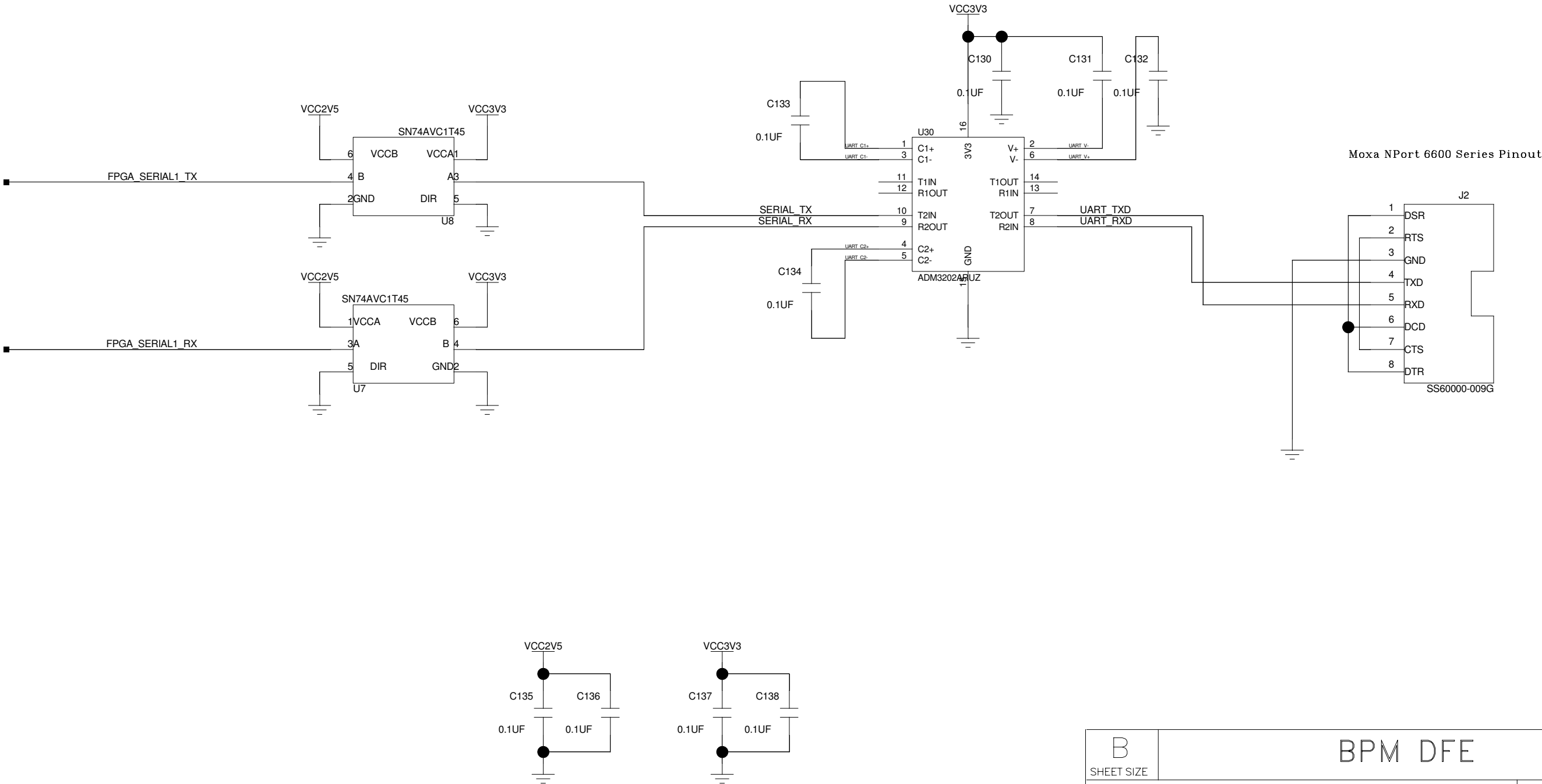
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SERIAL PORT : DCE

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | 12/8/11    | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



LT-EL-SR-EU-BPM-0101-03

|               |                         |    |    |    |
|---------------|-------------------------|----|----|----|
| B             | BPM DFE                 |    |    | B  |
| SHEET SIZE    | REVISION                |    |    |    |
| ESH&Q         | SHEET                   |    |    |    |
| RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 | 15 | OF | 29 |

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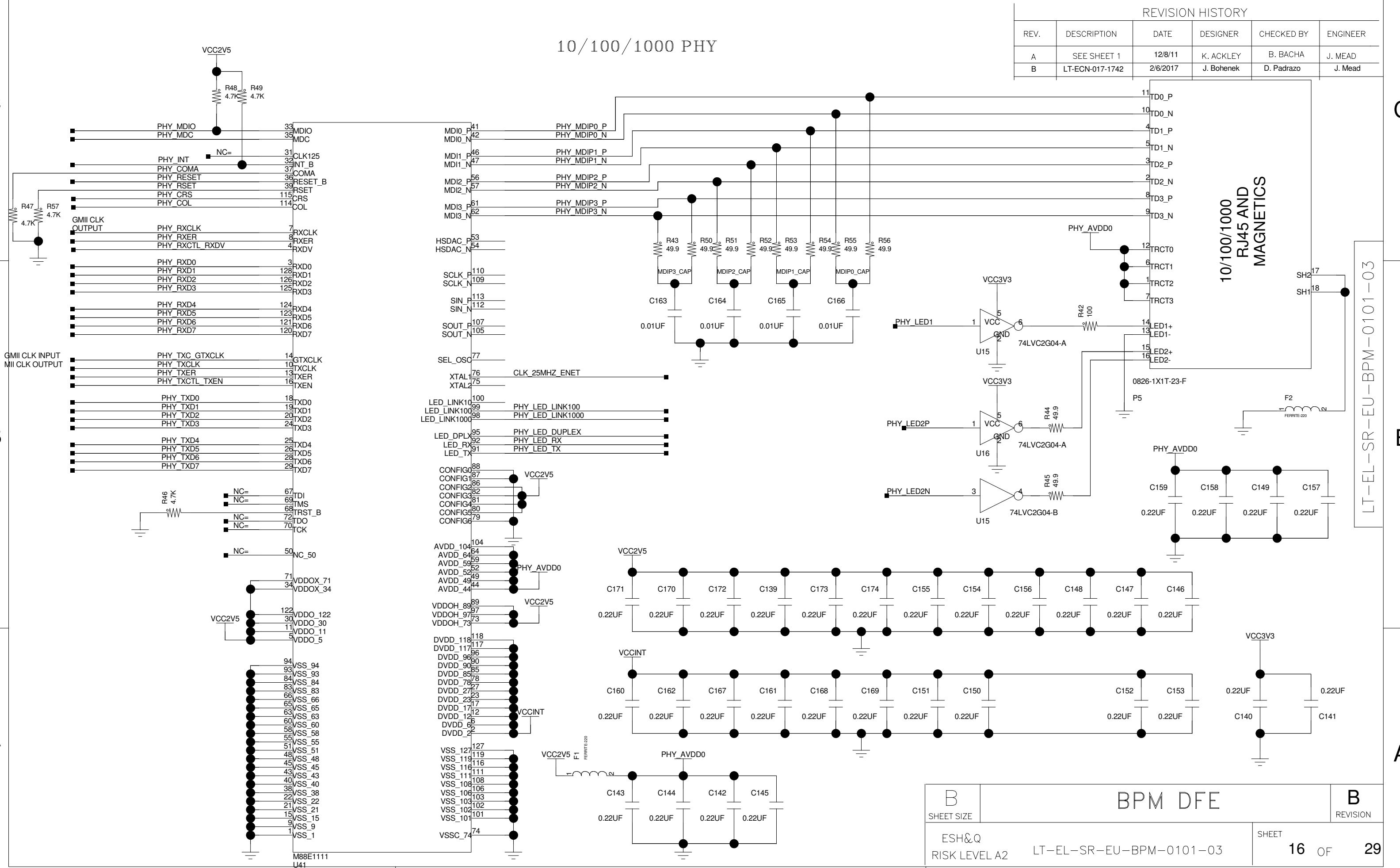
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| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

|                        |                         |  |  |                   |
|------------------------|-------------------------|--|--|-------------------|
| B<br>SHEET SIZE        | BPM DFE                 |  |  | B<br>REVISION     |
|                        |                         |  |  |                   |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  |  | SHEET<br>16 OF 29 |



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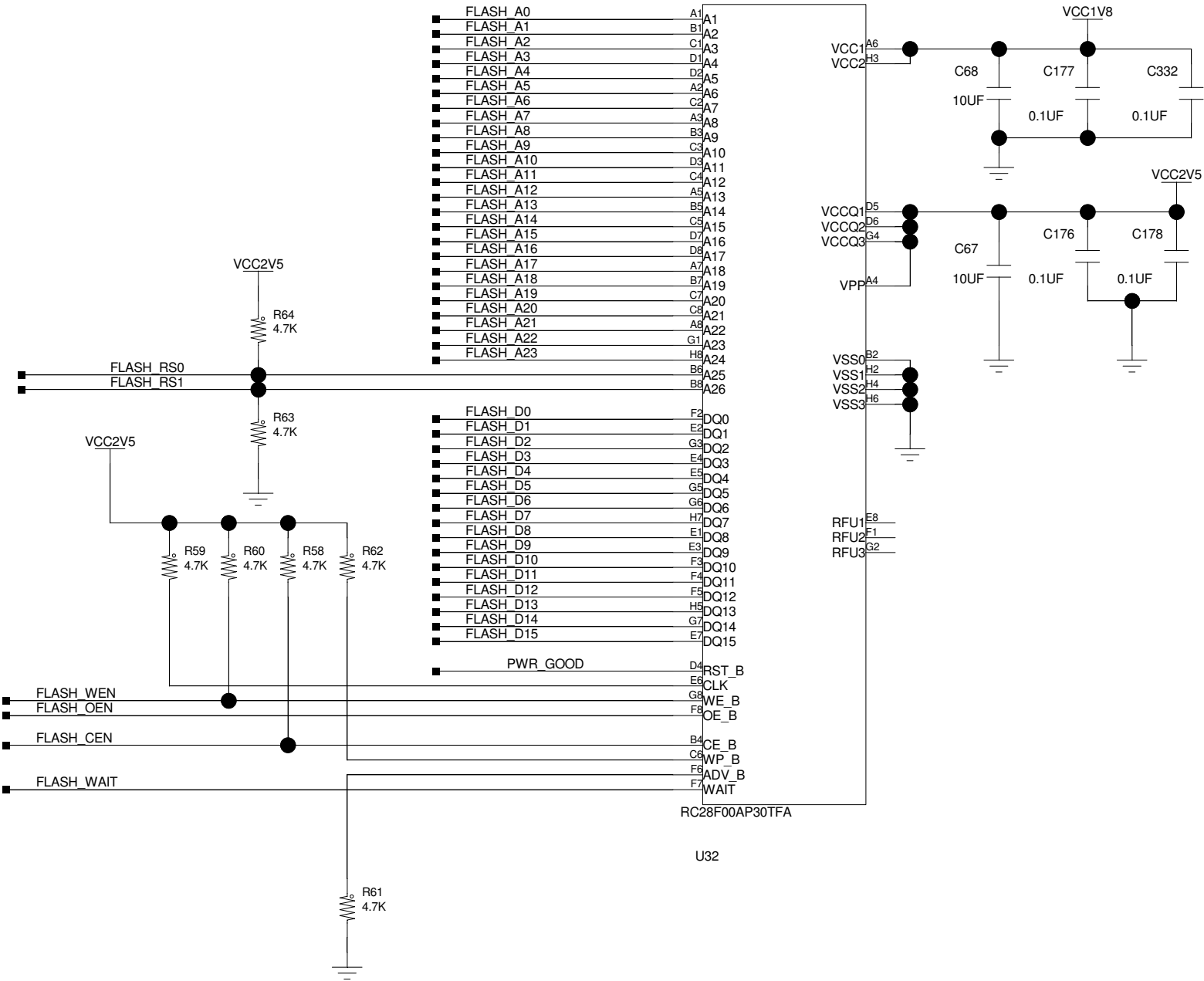
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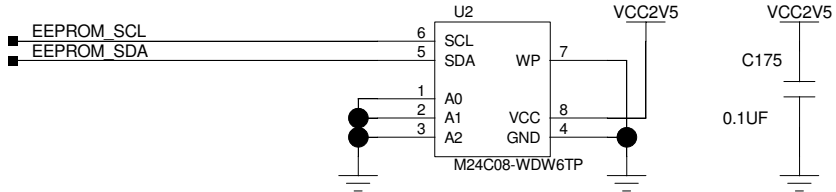
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| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

FLASH MEMORIES

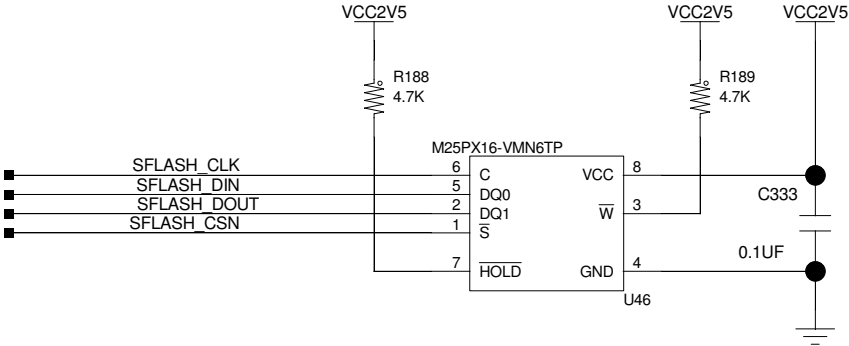
1 GBIT NOR FLASH



IIC EEPROM



SERIAL FLASH



|            |                         |  |          |
|------------|-------------------------|--|----------|
| B          | BPM DFE                 |  | B        |
|            |                         |  |          |
| SHEET SIZE | RISK LEVEL A2           |  | REVISION |
| ESH&Q      | LT-EL-SR-EU-BPM-0101-03 |  | SHEET    |
|            |                         |  | 17 OF 29 |

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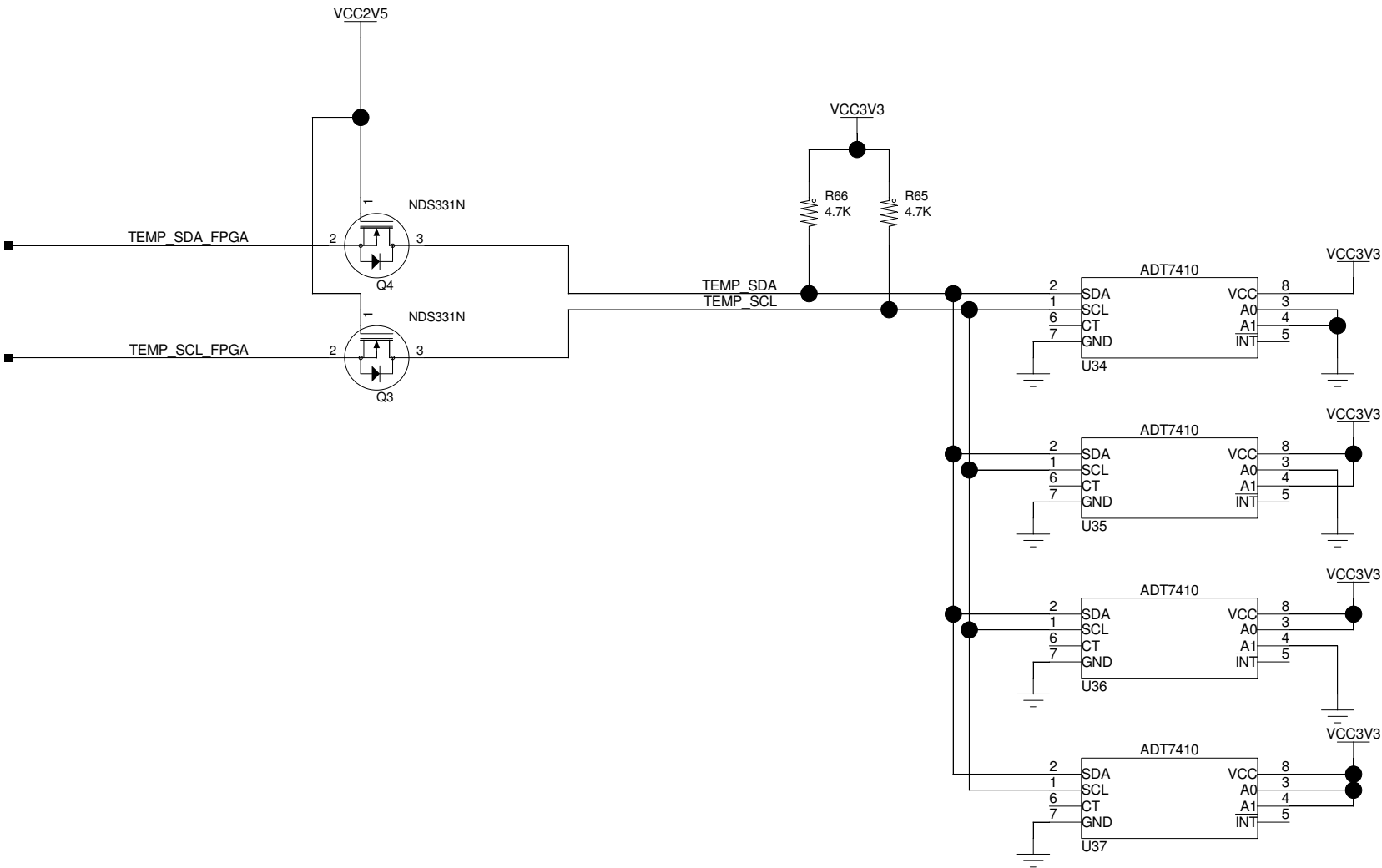
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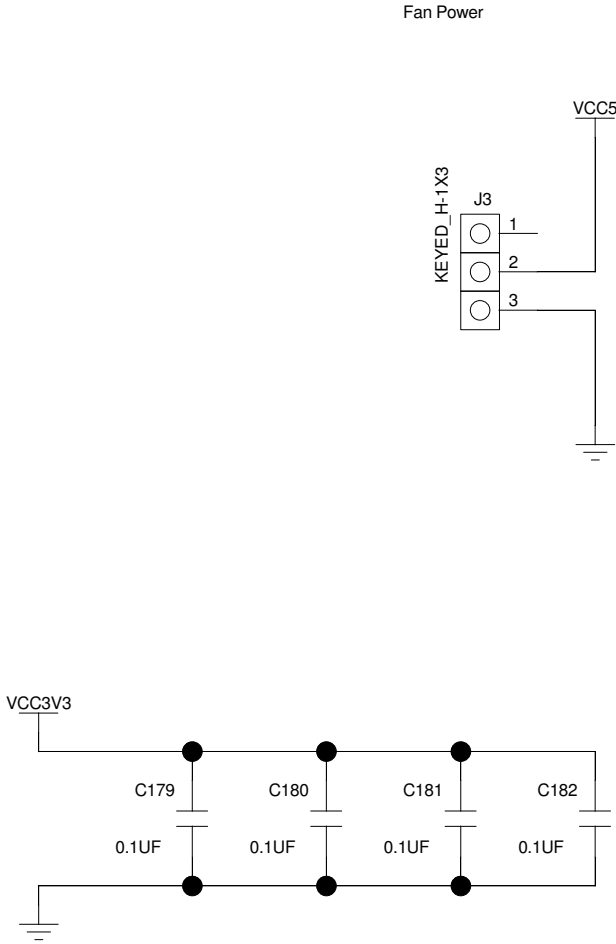
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TEMPERATURE SENSORS & SERIAL NUMBER



| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



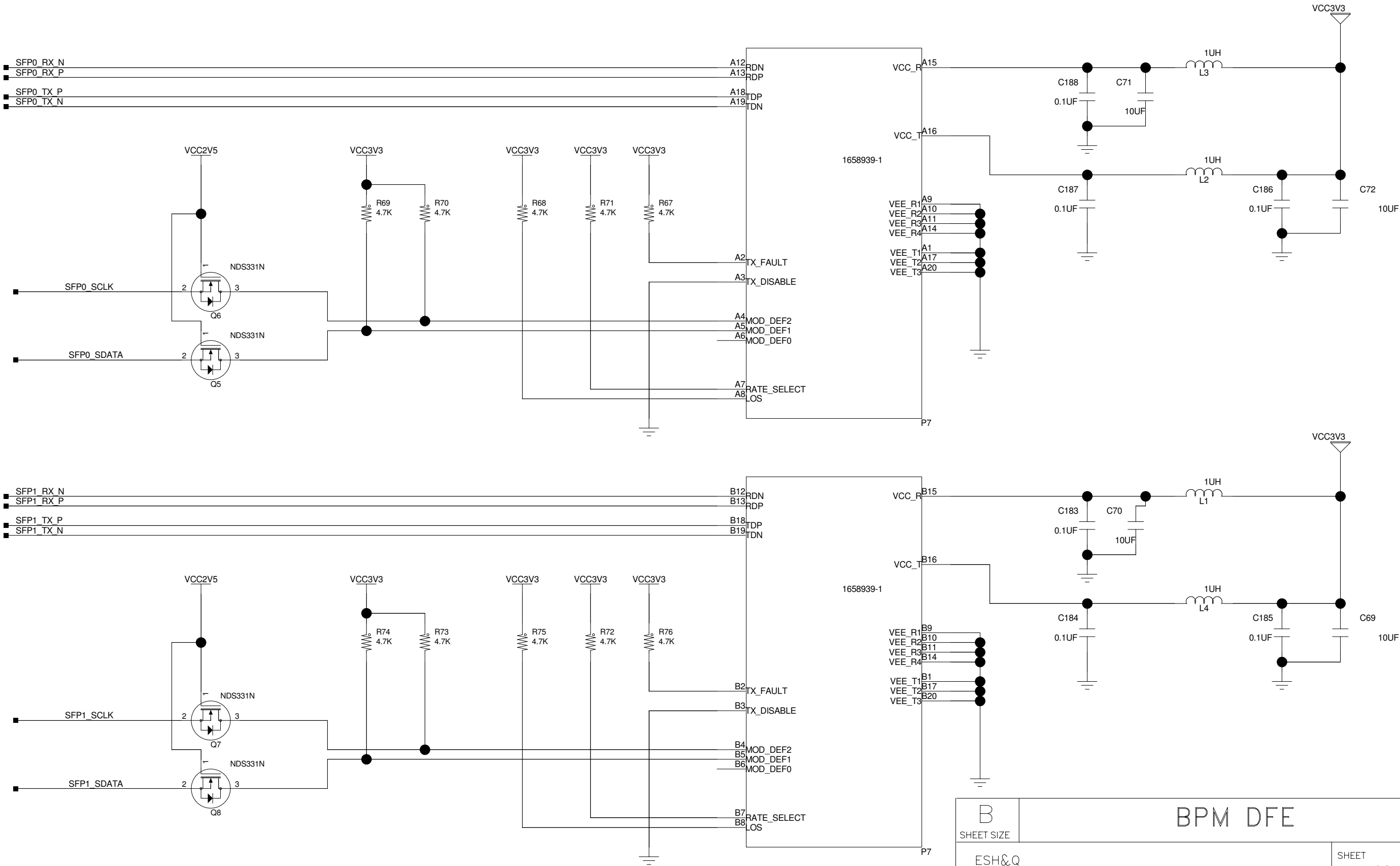
LT-EL-SR-EU-BPM-0101-03

|                        |                         |  |                   |
|------------------------|-------------------------|--|-------------------|
| B<br>SHEET SIZE        | BPM DFE                 |  | B<br>REVISION     |
|                        |                         |  |                   |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>18 OF 29 |

SFP MODULE

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



LT-EL-SR-EU-BPM-0101-03

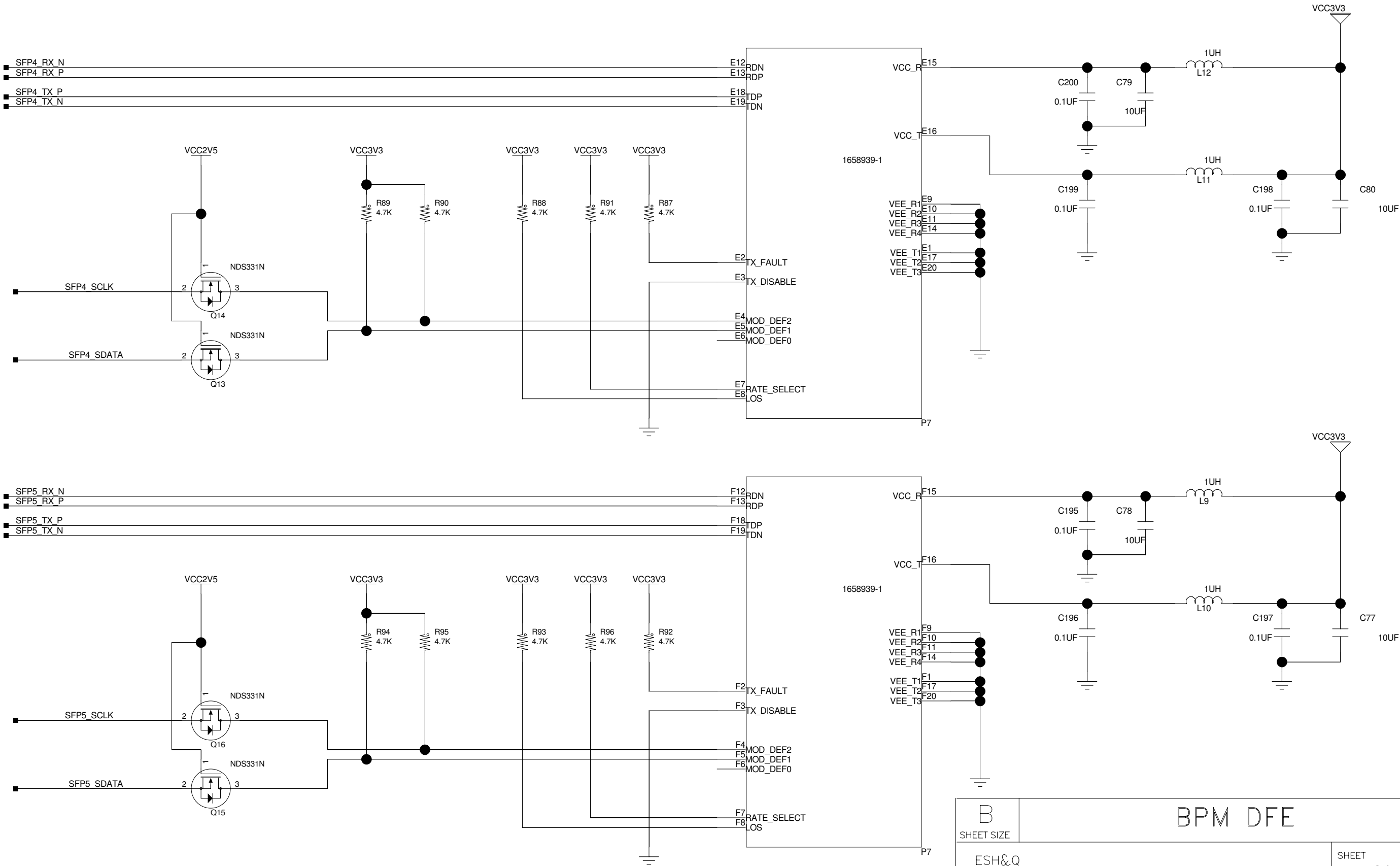
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| B             | BPM DFE                 |  |  | B |
| SHEET SIZE    | REVISION                |  |  |   |
| ESH&Q         | LT-EL-SR-EU-BPM-0101-03 |  |  |   |
| RISK LEVEL A2 | SHEET 19 OF 29          |  |  |   |



SFP MODULE

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



LT-EL-SR-EU-BPM-0101-03

|                        |                         |       |       |    |
|------------------------|-------------------------|-------|-------|----|
| B                      | BPM DFE                 |       |       | B  |
| SHEET SIZE             | REVISION                |       |       |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 | SHEET | 21 OF | 29 |

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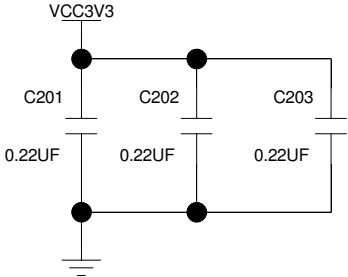
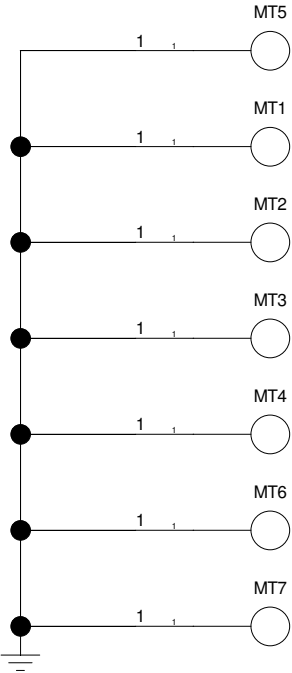
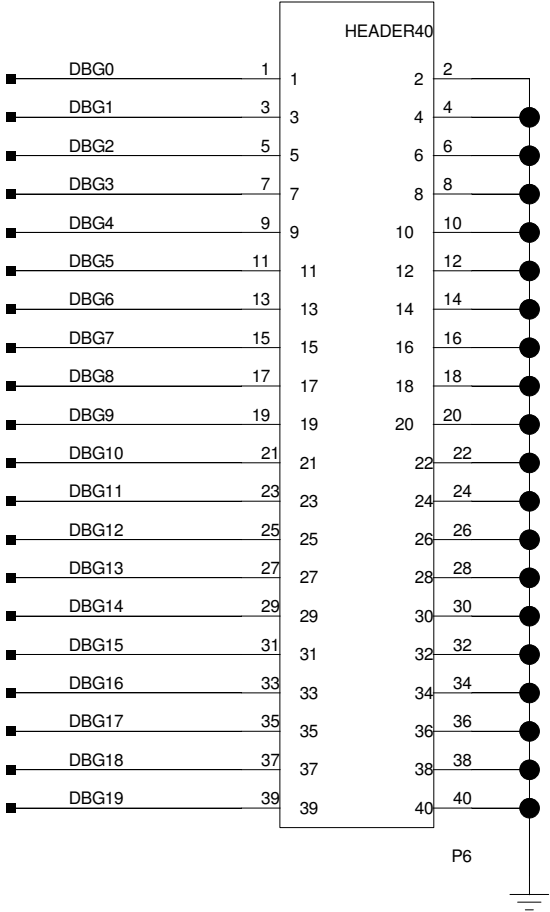
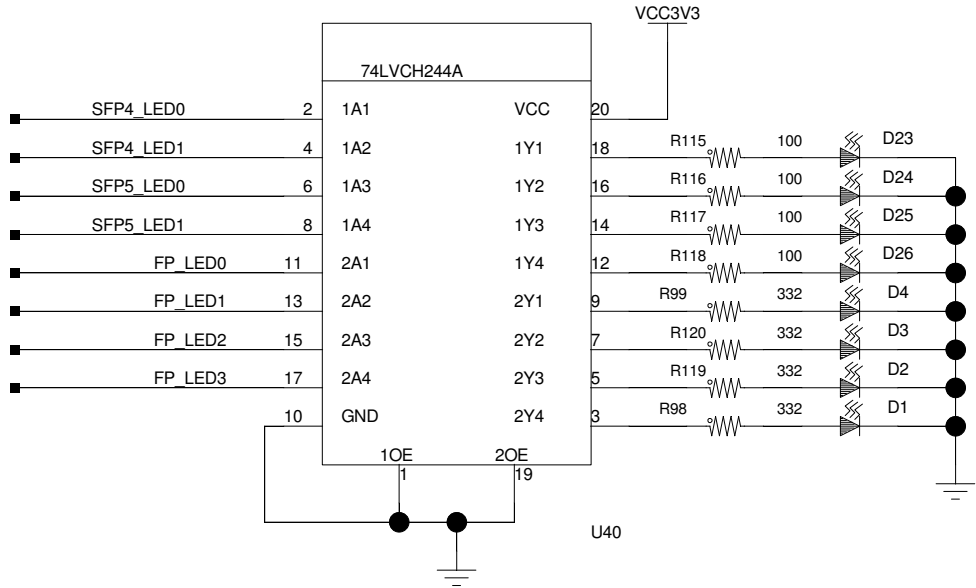
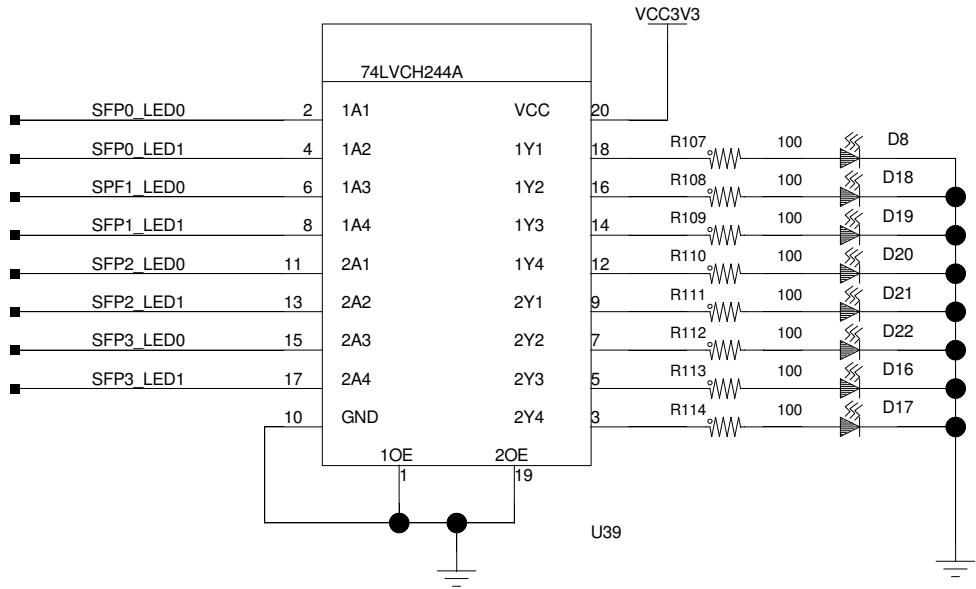
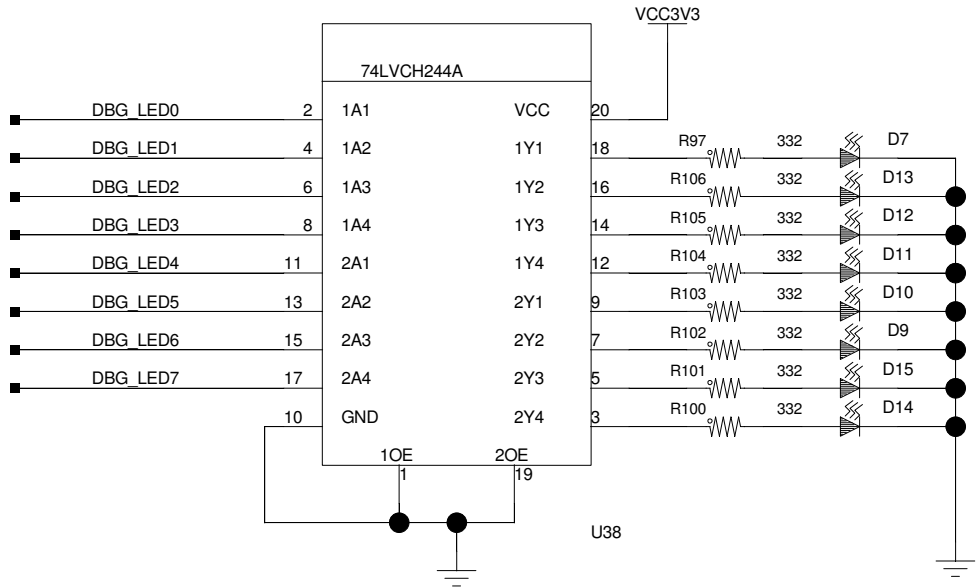
C

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| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

LED's, DEBUG HEADER

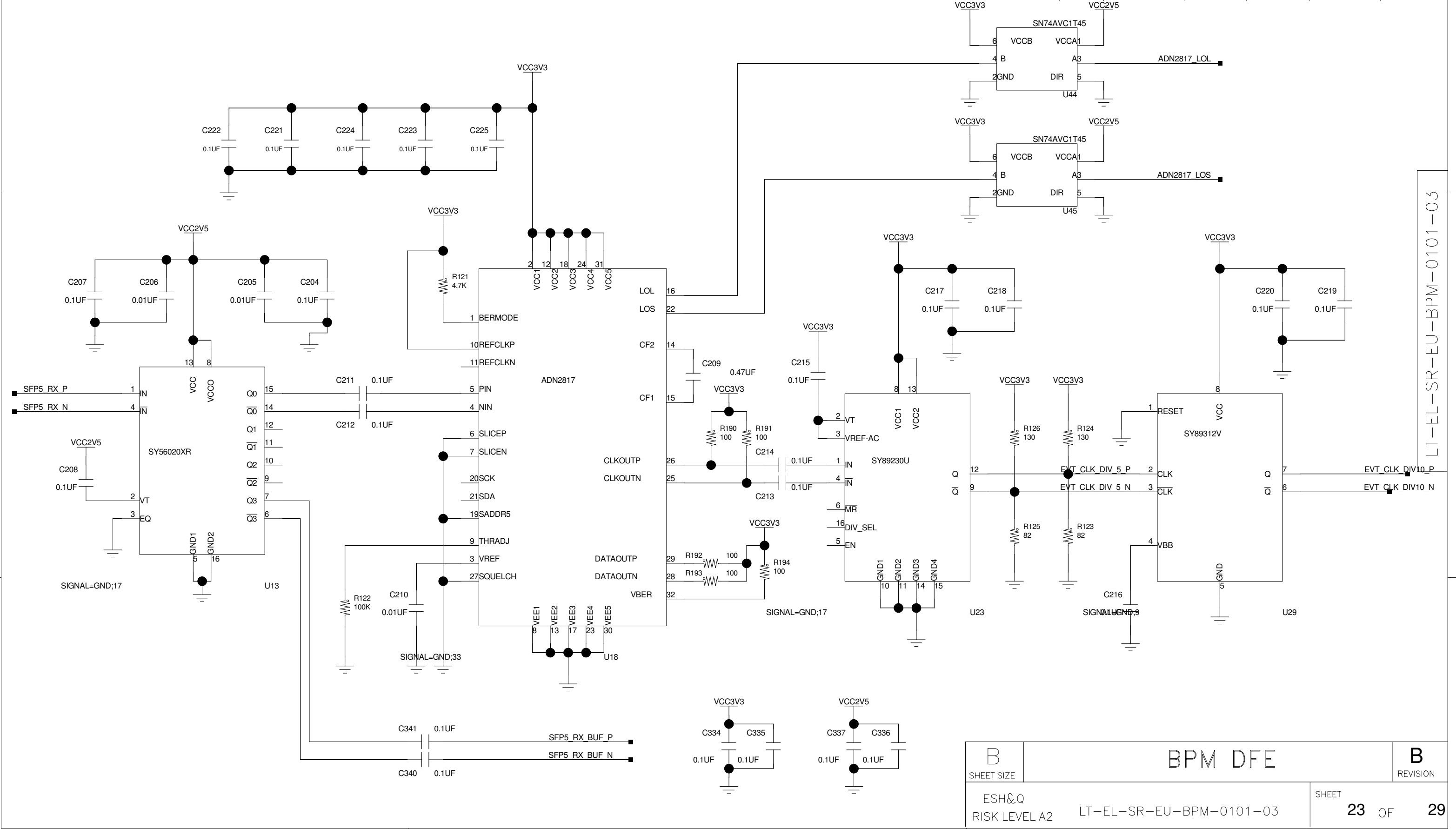


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|------------------------|-------------------------|--|----------------|
| B<br>SHEET SIZE        | BPM DFE                 |  | B<br>REVISION  |
|                        |                         |  |                |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET 22 OF 29 |

EVENT RECEIVER CLOCK EXTRACTER

REVISION HISTORY

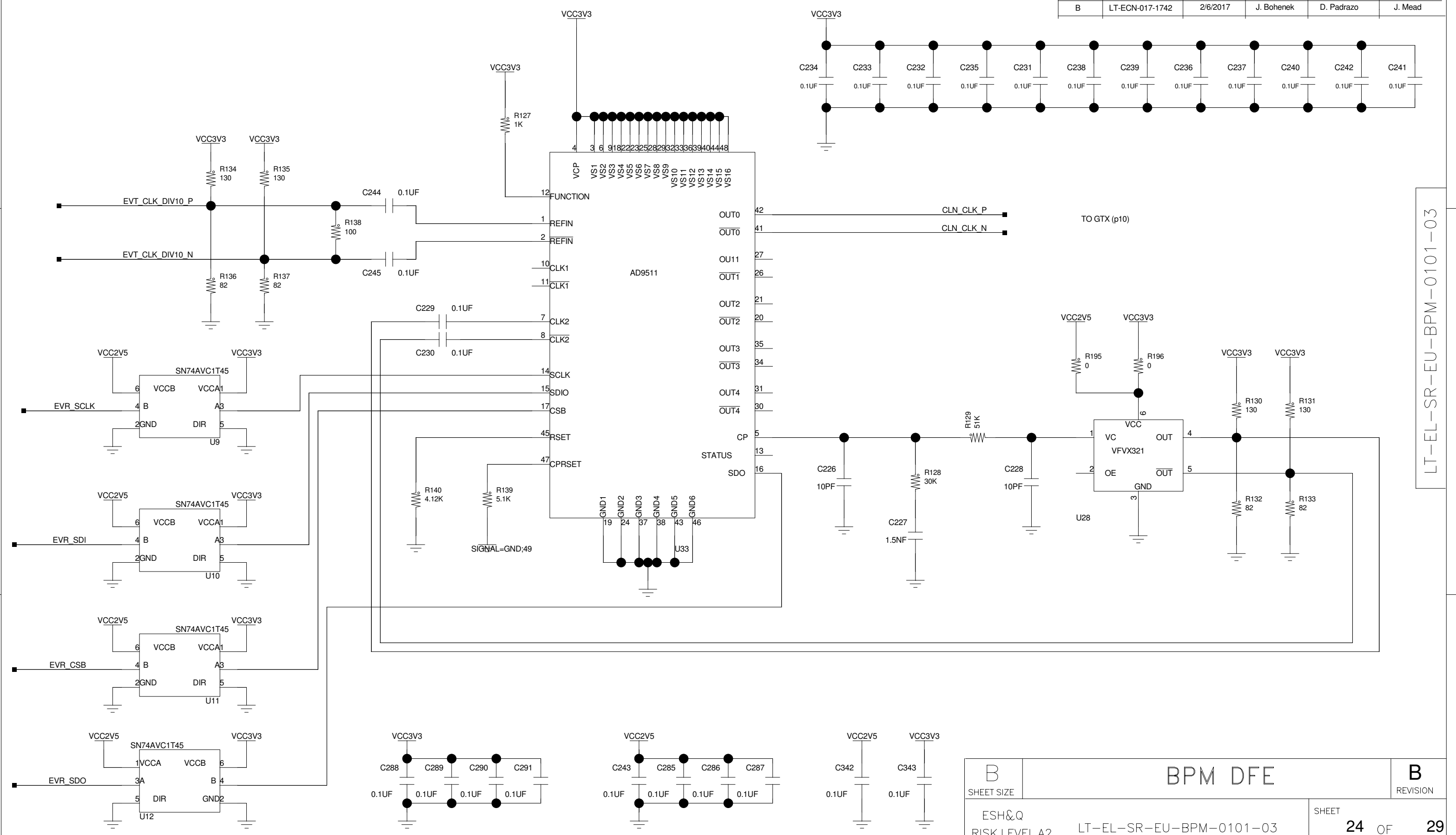
| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



EVENT RECEIVER CLOCK CLEANER

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



LT-EL-SR-EU-BPM-0101-03



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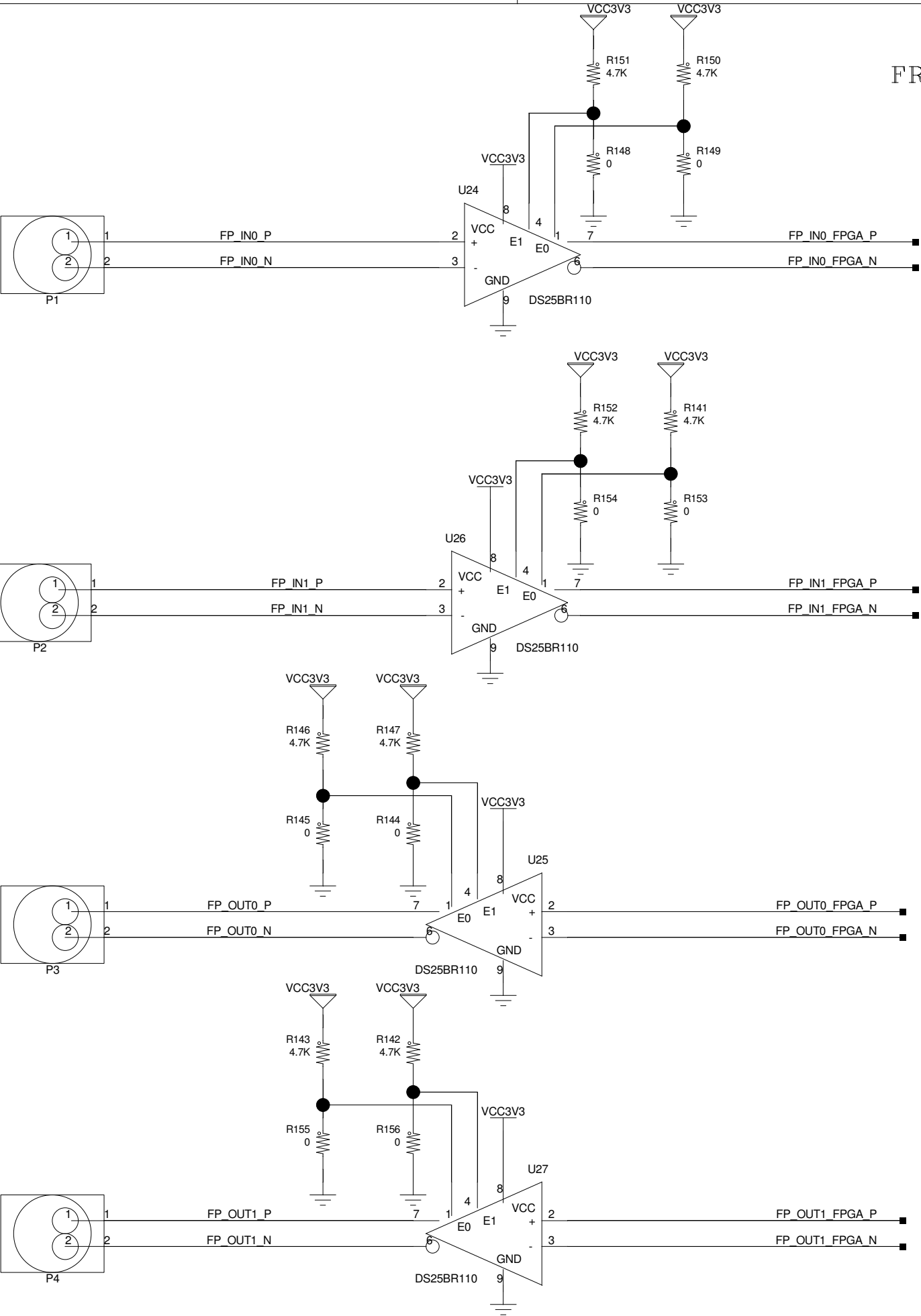
A

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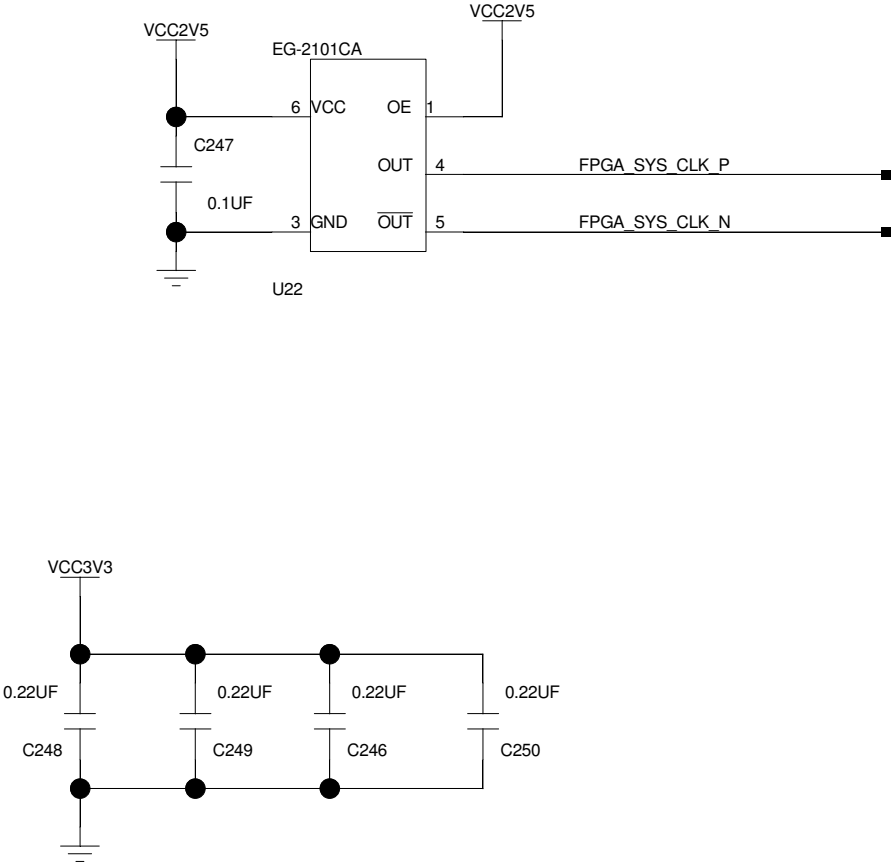
FRONT PANEL I/O



REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

System OSC



LT-EL-SR-EU-BPM-0101-03

|                        |                         |  |                |    |
|------------------------|-------------------------|--|----------------|----|
| B                      | BPM DFE                 |  |                | B  |
| SHEET SIZE             | REVISION                |  |                |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 |  | SHEET<br>25 OF | 29 |

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AFE CONNECTORS

REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

ADC 0

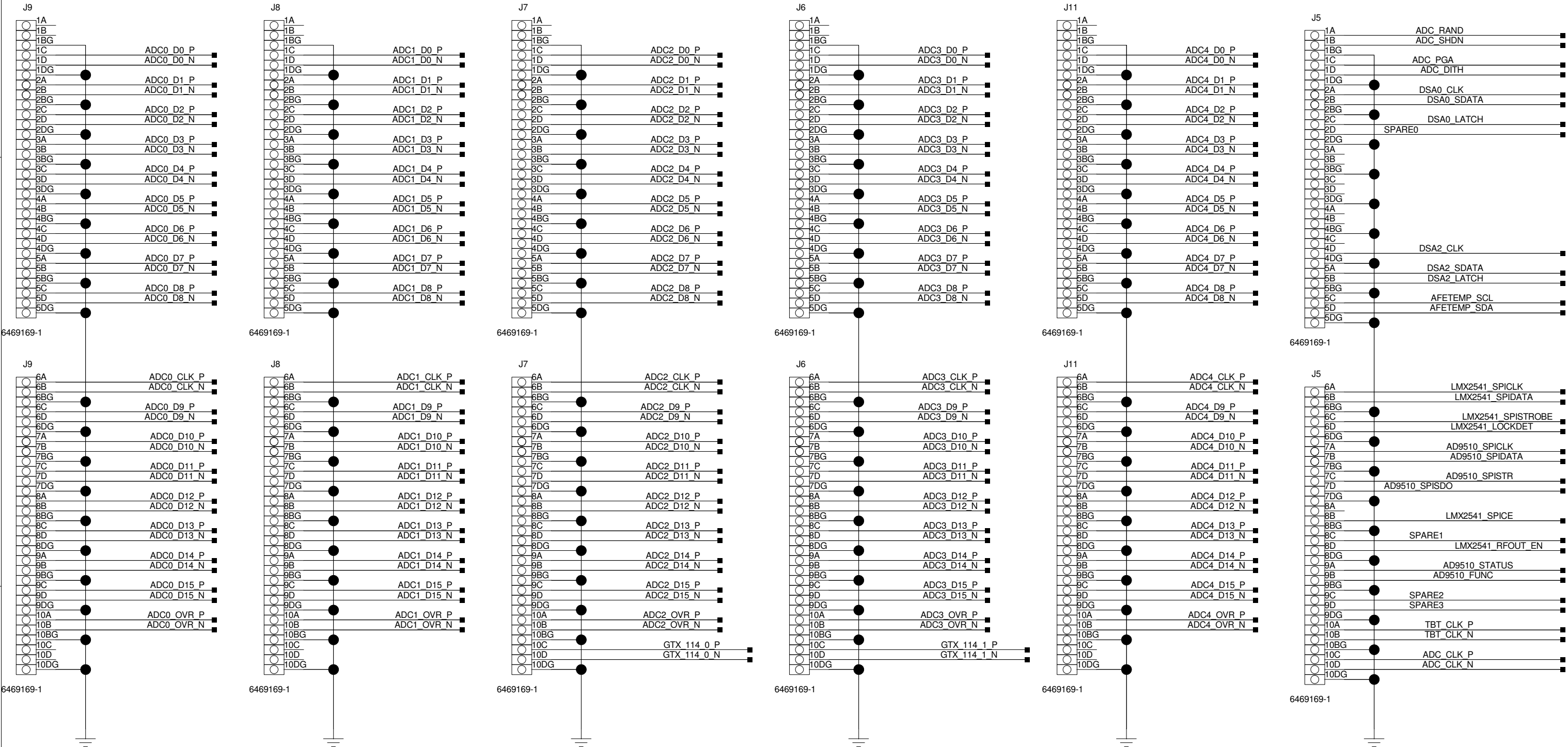
ADC 1

ADC 2

ADC 3

ADC 4

MISC



LT-EL-SR-EU-BPM-0101-03

|               |                         |  |  |   |
|---------------|-------------------------|--|--|---|
| B             | BPM DFE                 |  |  | B |
| SHEET SIZE    | REVISION                |  |  |   |
| ESH&Q         | LT-EL-SR-EU-BPM-0101-03 |  |  |   |
| RISK LEVEL A2 | SHEET 26 OF 29          |  |  |   |



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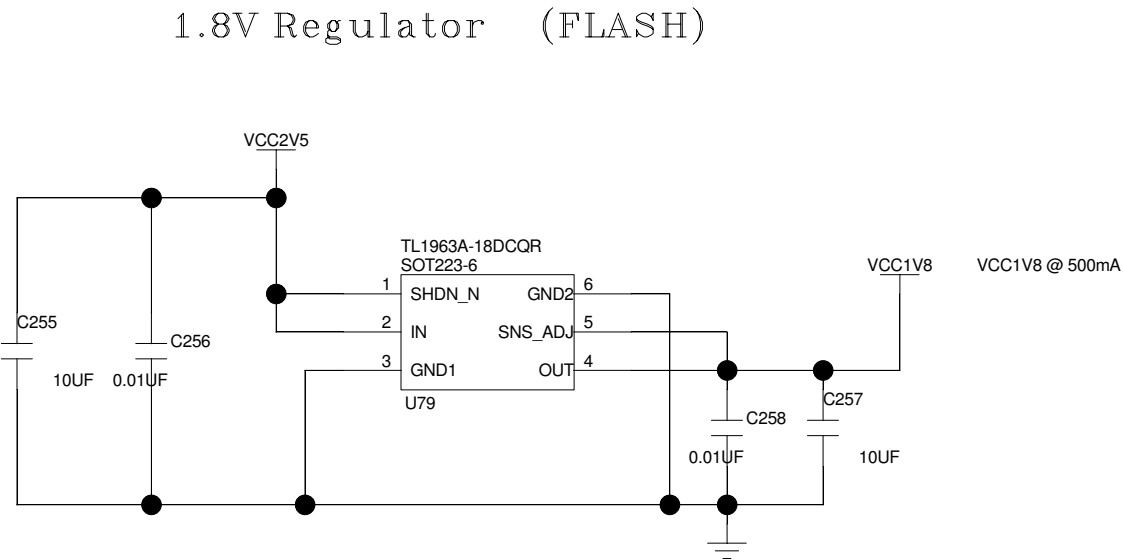
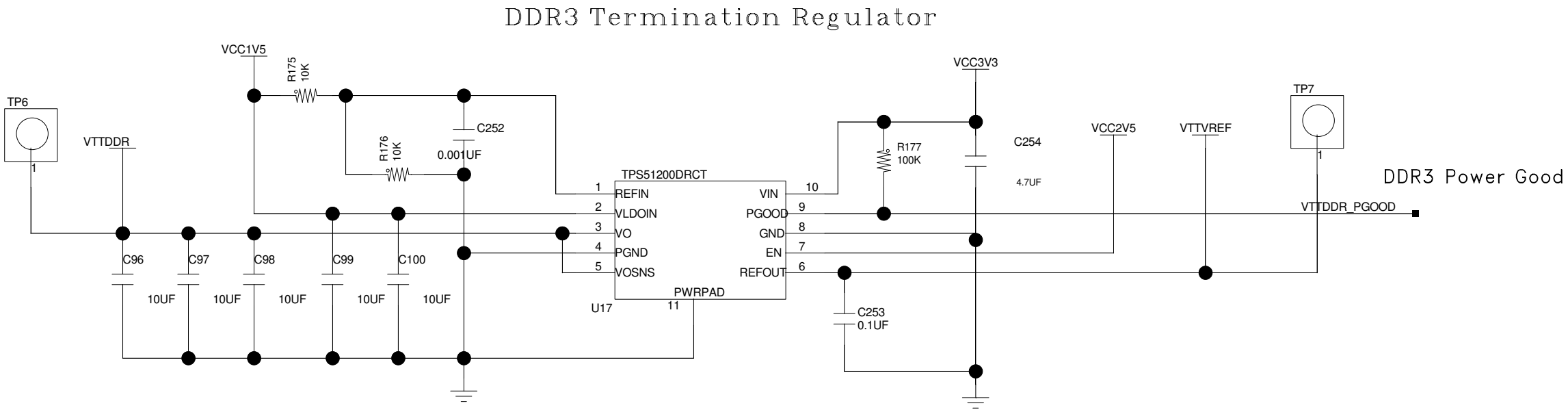
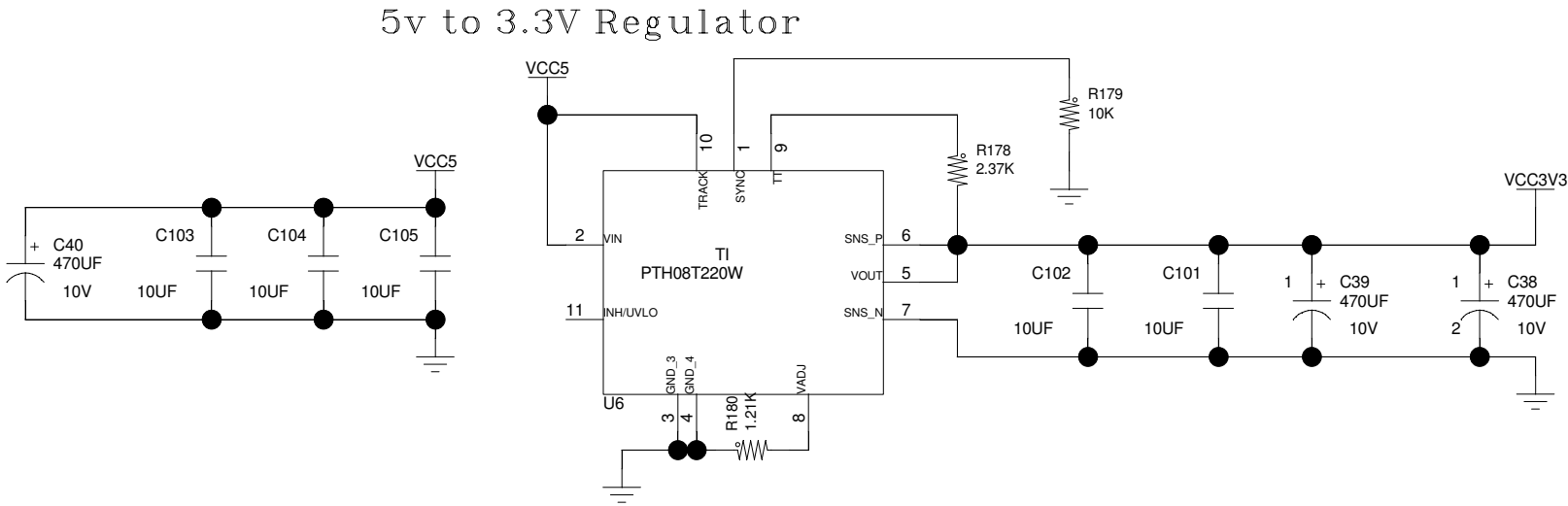
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| REVISION HISTORY |                 |          |            |            |          |
|------------------|-----------------|----------|------------|------------|----------|
| REV.             | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
| A                | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B                | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |



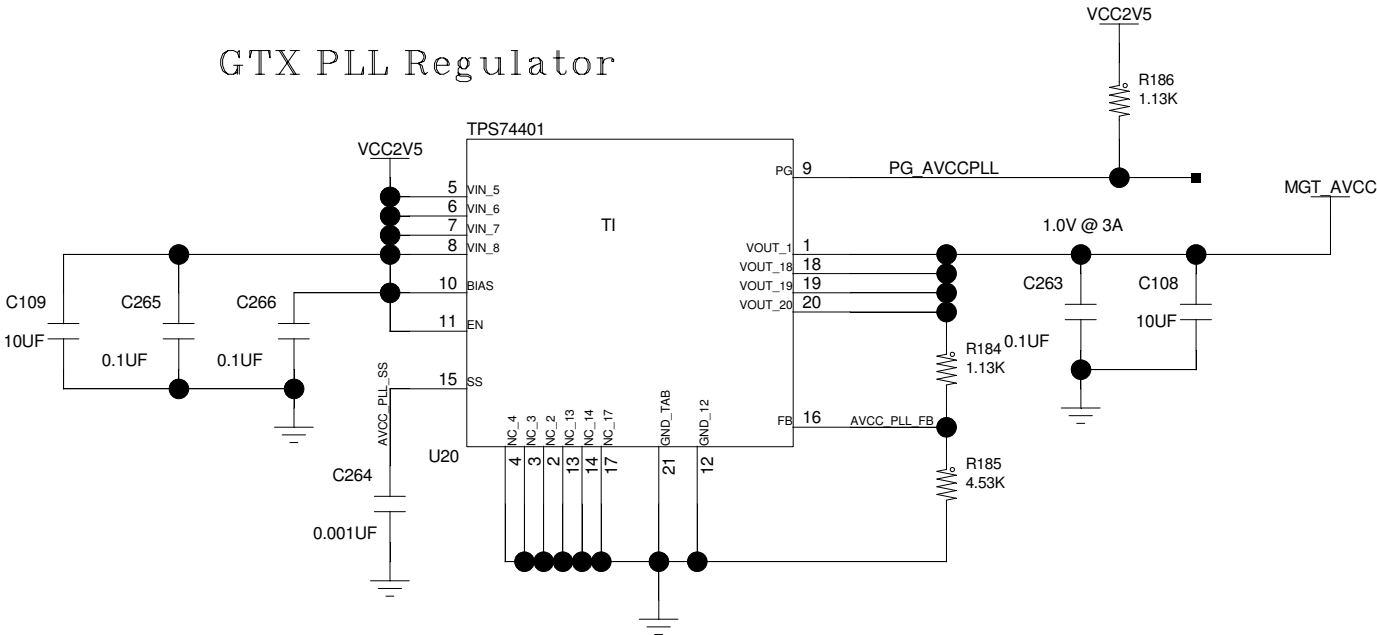
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| B             | BPM DFE                 |  |  | B |
| SHEET SIZE    | REVISION                |  |  |   |
| ESH&Q         | LT-EL-SR-EU-BPM-0101-03 |  |  |   |
| RISK LEVEL A2 | SHEET 28 OF 29          |  |  |   |

GTX Power Supplies

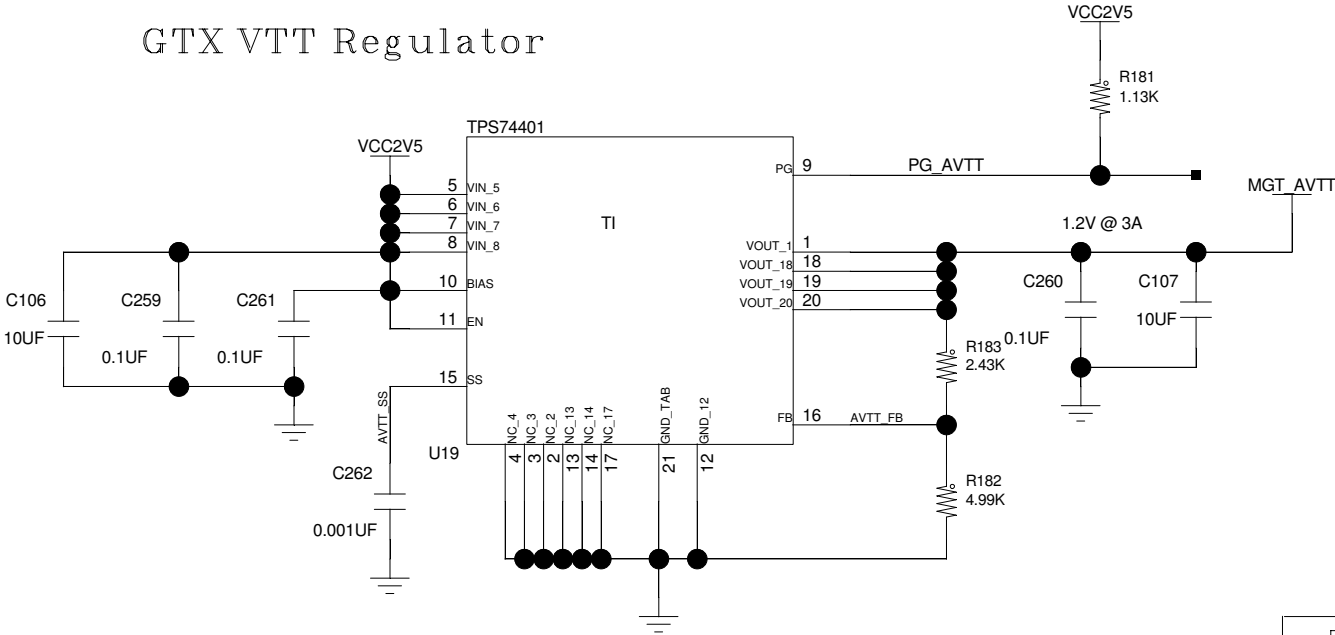
REVISION HISTORY

| REV. | DESCRIPTION     | DATE     | DESIGNER   | CHECKED BY | ENGINEER |
|------|-----------------|----------|------------|------------|----------|
| A    | SEE SHEET 1     | 12/8/11  | K. ACKLEY  | B. BACHA   | J. MEAD  |
| B    | LT-ECN-017-1742 | 2/6/2017 | J. Bohenek | D. Padrazo | J. Mead  |

GTX PLL Regulator



GTX VTT Regulator



LT-EL-SR-EU-BPM-0101-03

|                        |                         |       |       |    |
|------------------------|-------------------------|-------|-------|----|
| B                      | BPM DFE                 |       |       | B  |
| SHEET SIZE             | REVISION                |       |       |    |
| ESH&Q<br>RISK LEVEL A2 | LT-EL-SR-EU-BPM-0101-03 | SHEET | 29 OF | 29 |