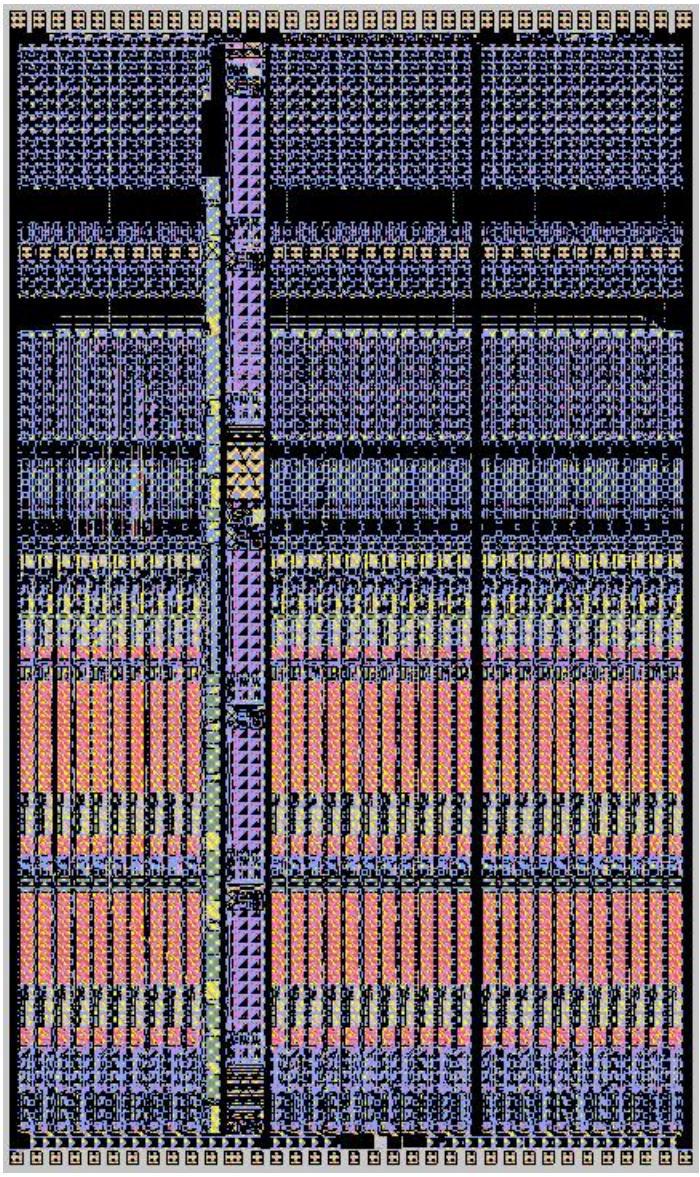
LS ASIC (HERMES4) – Version 4 – IC101



Technology : *CMOS 0.35µm 2-poly, 4-metal*

Channels : *32*

- preamplifier / high order shaper
  - settable gain: *0.75V/fC, 1.5V/fC*
  - settable peaking time: *0.5µs, 1µs, 2µs, 4µs*
- two window-comparators and one threshold comparator
- comparator thresholds controlled by five 10-bit DACs
- comparator thresholds trimmable per channel (6-bit DACs)
- 24-bit counter for each comparator

Power per channel : ≈ *8mW*

Serial interface

LOGIC

Chip select via CS
Chip is selected when CS (chip select) is high.
If SDAC low, WR low sets write mode in standard register, WR high sets read mode.
If SDAC low, transition high to low of CS resets the counters (internal control CRST) and sets ELK and EAN (internal control SAN).
If SDAC high, writing to 10-bit DACs is enabled (independently of WR).

Chip select via token
Chip selection can also be performed via token by connecting TO (token out) to CS of the next chip.

Enabling Counters and data SDI/SDO interface
Counters are enabled/disabled through EN.
Read/write mode is selected through WR.
In write mode (WR=0) SCK and SDI are enabled through internal control WE (write enable).
In read mode (WR=1) SCK and SDO (tristated) are enabled through internal control RE (read enable).
If CS is low, WE and RE are forced to low.

SUPPLIES

Vdd	+3.3V analog
Vddb	+3.3V analog common bias
Vddp	+3.3V analog input MOSFET
Vddd	+3.3V digital
Vss	0V analog
Vssb	0V analog common bias
Vssd	0V digital
Vsubd	0V substrate digital

ANALOG INPUTS

I0-I31	inputs
CAL	calibration input
VL0	low threshold, window 0
VL1	low threshold, window 1
VH1	high threshold, window 1
VL2	low threshold, window 2
VH2	high threshold, window 2

ANALOG OUTPUTS

O0-O31	**analog outputs**
GUARD	**reproduces input voltage for guard biasing, on input side**
OAN	analog output
OLK	leakage current monitor

ANALOG CONTROLS (self biasing)

BLK	internal leakage current control
BLN	output baseline control
BDAC	DAC range control

DIGITAL INPUTS

SCK	clock input	positive edge shifts in write mode negative edge shifts in read mode (latch on positive edge) clock must be idling high

SDI (SDAC low) 904 bit serial input
SDA,SDA0,SDA1,SDA2,EBLK,T1,T2,G,[ECH,ECAL,ELK,EAN,D0-D5/VL1,D0-D5/VH1,D0-D5/VL2,D0-D5/VH2]x32,
first bit of data stream is D5/VH2 of Ch31, last bit of data stream is 0.

SDI (SDAC high)50 bit serial input; first bit written at first clock (positive edge), ending to VL0 DAC
P0:P9(VH2), P0:P9(VL2), P0:P9(VH1), P0:P9(VL1), P0:P9(VL0)
first bit of data stream is P9(VL0), last bit of data stream P0(VH2).

CS	chip select if SDAC low, CS transition 1 to 0 resets the counters and sets EAN and ELK	1 active
EN	counters enable/disable	EN=1 enables the counters EN=0 disables the counters
WR	write/read mode	WR=1 read mode WR=0 write mode
RST	global reset OR-ed to internal power-on reset	0 active
TO	token output, to be connected to CS of the next chip	
TCK	token clock input	positive edge shifts token
SDAC	**enables writing to 10-bit DACs (independent of WR)**	

DIGITAL OUTPUTS (clocked)

SDO	2304 bit counter serial output; first bit available before first clock, starting from Ch31 [C23-C0/W0, C23-C0/W1, C23-C0/W2]x32, first bit of data stream is C23/W0 of Ch31, last bit of data stream is C0/W2 of Ch0.

DIGITAL CONTROLS

EBLK	**internal bias leakage enable**	**0 disable (default)** **1 enable**
T2,T1	**peaking time controls**	**00 1µs (default)** **01 0.5µs** **10 4.0µs** **11 2.0µs**
SDA	**Internal DACs enable**	**0 disabled (default)**
SDA2:SDA0	**10-bit DAC monitors to OAN**	**000 disabled (default)** **001 DAC VL0** **010 DAC VL1** **011 DAC VH1** **100 DAC VL2** **101 DAC VH2**

P9:P0	**10-bit DAC setting**	**0:0 (0)** **1:1 (3FF)**	**~300mV** **~ 2.25V**	**(default)**
G	gain control	0 1500mV/fC 1 750mV/fC		
ECH	channel enable	0 enable 1 disable		
ECAL	calibration input enable	1 enable 0 disable		
ELK	leakage current monitor enable	1 enable 0 disable		
EAN	analog output enable	1 enable 0 disable		
E4T	ch.4 EAN, ECAL, ELK enable	1 enable 0 disable		

also forces T2 high (peaking time to 4µs from 1µs default)

DIE SIZE / PADS

Layout size	**3711 µm x 6287µm**
Requested max die cut size	3850 µm x 6500 µm
Confirmed die cut size	3826 µm x 6432 µm
Pads	35 left + 35 right + **32 midright**, none top or bottom
Pad opening	Input: 60µm x 70µm - **MidOutput 97µm x 70µm** - Output 70µm x 100µm
Pad pitch	Input/Output 106µm, **MidOutput 101µm**
Fabrication	TSMC 0.35µm through MOSIS

Vddp		Vdd
I31	**O31**	Vss
I30	**O30**	CS
I29	**O29**	SDI
I28	**O28**	SCK
I27	**O27**	TCK
I26	**O26**	WR
I25	**O25**	EN
I24	**O24**	**SDAC**
I23	**O23**	RST
I22	**O22**	Vddd
Guard		Vssd
I21	**O21**	Vdd
I20	**O20**	Vss
I19	**O19**	VH2
I18	**O18**	VL2
I17	**O17**	VH1
I16	**O16**	VL1
I15	**O15**	VL0
I14	**O14**	BDAC
I13	**O13**	BLN
I12	**O12**	BLK
I11	**O11**	OAN
I10	**O10**	OLK
I9	**O9**	Vss
I8	**O8**	Vdd
I7	**O7**	CAL
I6	**O6**	Vsubd
I5	**O5**	SDO
I4	**O4**	TO
I3	**O3**	E4T
I2	**O2**	Vddd
I1	**O1**	Vssd
I0	**O0**	Vss
Vddp		Vdd