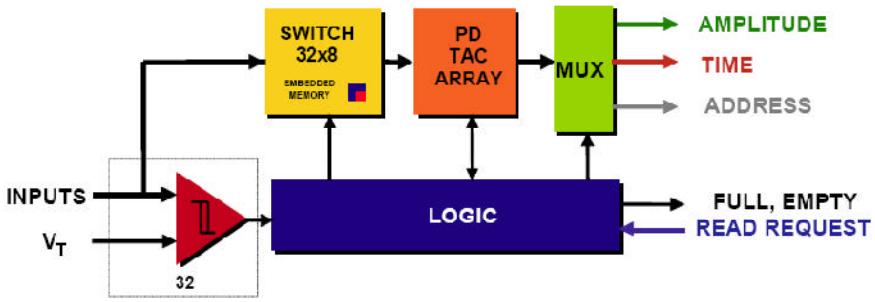
PDD ASIC 7.0 (IC105)

- **Power**: ≈ 110 mW
- **Architecture:** Inputs for 32 shaped, positive unipolar pulses with minimum peaking time 30 ns, input filter option.
  Threshold controlled with one 10-bit DAC and plus 4-bit DAC trimmer per channel.
  Eight offset-free, two-phase peak detectors with 3-bit address.
  32-to-8 cross-point switches that route any input channel to any available peak detector (PD/TD).
  Fast arbitration logic for simultaneous event to control the cross-point switches.



- **Layout size :** 4842 × 3562 µm²
- **Actual die size :** 4956 × 3705 um²
- **Pad pitch :** left and right 100 µm, top and bottom 150 µm
- **Technology :** TSMC CMOS 0.35µm – 3.3V, 1-poly, 4-metal, MiM cap, sil blk resistors
- **Package :** MQFP80A

Core functions

The PDD ASIC is designed to accept independent, randomly occurring analog pulses (events) on 32 input channels. For each event, the ASIC extracts the amplitude (peak height), timing information (4 modes available) and channel address. When a pulse arrives, it is routed to any of the available peak detect (PD) circuits which extracts and stores the peak amplitude and the corresponding timing information on a time to amplitude converter (TAC).
Simultaneous events on different channels are acquired by means of dedicated circuitry which selectively optimize the number free PD/TD in the system. Internal arbitration and derandomizing logic manages the analog and digital memory on the chip. In response to the assertion of read request (RR), the PDD ASIC will present an analog peak sample and timing to the main analog outputs (PDOUT, TDOUT) and the corresponding 5 bit channel address to the outputs PIXADDR 4:0.

Secondary functions

In addition, the PDD ASIC can route a specified input channel to the main analog output for baseline measurement, while at the same time, connect it to the secondary analog output for test of the PD function. The PDD also route seven parallel configurable SPI bits (B6:0) to buffered outputs. These bits can be used to set logic levels on external peripheral devices.

Arbitration logic functions

In response to an input threshold-crossing, the cross-point switch routes the channel to the next available PD. The switching can be completed and ready for the next processing in a few nanoseconds (ns). If two pulses arrive within a few ns of each other, priority is given to the lower-numbered channel. If the catching mode is enabled, both pulses are processed. Once the cross-point switch is set the selected peak detector enters the “tracking” state which lasts until a peak is found or an adjustable time-out occurs. During this time the remaining free peak detectors can simultaneously process other pulses arriving on any other input channel. When the PD detects a peak, it enters the “buffering” state. At this time the address of the channel being processed is stored and the cross-point switch is reset. The peak detector remains “occupied” until it is read out. The arbitration logic maintains a time-ordered list of occupied peak detectors “pending readout”. This list is updated whenever a change in the number of occupied peak detectors occurs, either by a new hit or by a readout operation. “FULL” and “EMPTY” flags are available to indicate when all the peak detectors are occupied and unoccupied, respectively. A read request is initiated by a rising edge of RR. If a valid peak sample is being held in a PD, the amplitude and timing of that PD are routed to the output pins PDOUT and TDOUT of the chip, and the latched channel address becomes available on the PIXADDR outputs while a flag, DATAVAL is asserted to indicate a valid sample. Once the external ADC has completed its conversion, the downstream electronics acknowledges that it acquired the peak height and channel address by lowering RR. At the lowering of RR the arbitration logic resets the appropriate peak detector for subsequent pulses. The PDOUT, TDOUT and PIXADDR lines can be placed in a tri-stated condition with DATAVAL.

Timing relationships

Fig.1 shows the timing relationship for the three phase peak detector. Time t_{arb} is the time for the arbitration logic to complete the setup of the cross-point switch. If a more than one pulse arrives within t_{arb}, the pulse on the lowest-numbered channel is allowed access to the PD array and the other channels are blocked, unless the catching mode is enabled. Time t_{arb} is expected to be few ns. Time t_{track} is the time between the threshold crossing and the peak of the pulse. During this time the peak detector is in WRITE mode. Time t_{buf} is the time starting when the PD acquires the peak and ending when the PD is reset. It includes the time spent waiting for all prior-written PDs to be read out, the waiting time until the next CS rising edge occurs, the ADC converts, and the reset occurs. The peak detector is in READ mode during $\boldsymbol{t_{buf}}$.

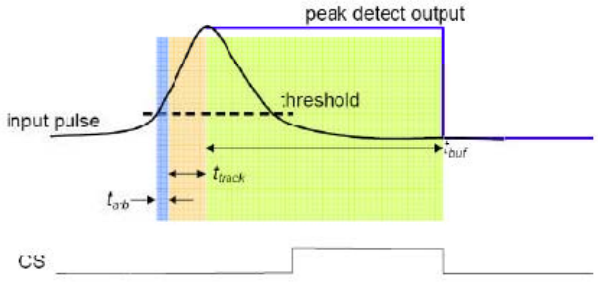


Fig. 1 Profile of the three phase peak detector.

There are four programmable timing measurements as illustrated in Fig. 2. *Rise time* mode measures the time from comparator firing until a peak is detected. *Time of occurrence* mode measures the time from when a peak is detected to when RR arrives, allowing measurement of the peak time relative to a known system clock. *Leading time of occurrence* mode measures from when the comparator crosses the threshold to allowing measurement of the leading edge time relative to a known system clock. *Time over threshold* mode measures the time interval in which the signal is above threshold, allowing also pile-up rejection.

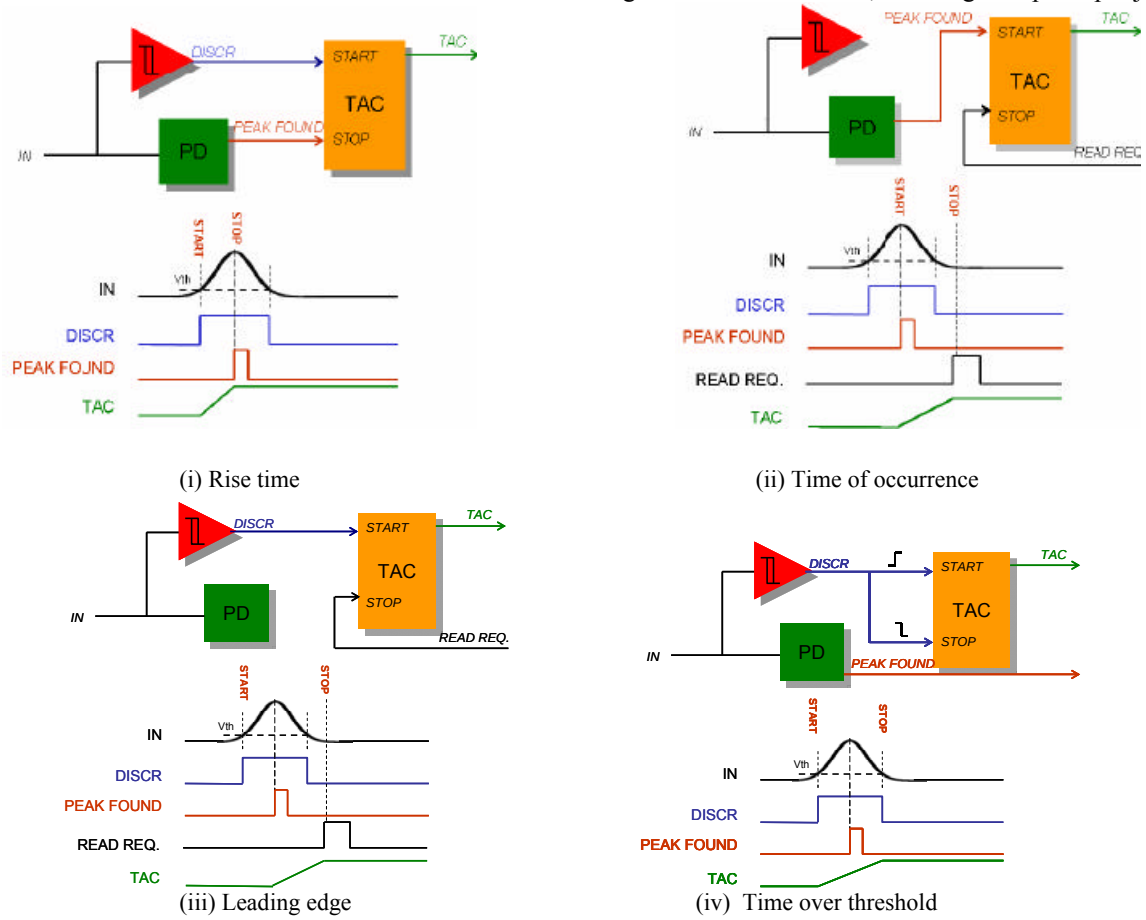


Fig. 2 PDDASIC timing modes; (i) Rise time, (ii) time of occurrence, (iii) leading edge (iv) time over threshold.

BROOKHAVEN NATIONAL LABORATORY
Instrumentation Division

The Serial Peripheral Interface (SPI)

The SPI of the PDDASIC is comprised of one shift register (SR). Data is shifted in MSB first on the rising edge of the clock. There are 11 banks of parallel load data registers (R0-R10) which are addressed by the upper nibbles of the SR.

MSB Shift Register (SR) LSB

A3	A2	A1	A0	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NAME	*FUNCTION*	*RESET VALUE*
A 3:0	Register address	0
D 19:0	Data bits	0

MSB Data Register Map (R0-R7)

SR	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	m3	$da3_3$	$da3_2$	$da3_1$	$da3_0$	m2	$da2_3$	$da2_2$	$da2_1$	$da2_0$	m1	$da1_3$	$da1_2$	$da1_1$	$da1_0$	m0	$da0_3$	$da0_2$	$da0_1$	$da0_0$
R1	m7	$da7_3$	$da7_2$	$da7_1$	$da7_0$	m6	$da6_3$	$da6_2$	$da6_1$	$da6_0$	m5	$da5_3$	$da5_2$	$da5_1$	$da5_0$	m4	$da4_3$	$da4_2$	$da4_1$	$da4_0$
R2	m11	$da11_3$	$da11_2$	$da11_1$	$da11_0$	m10	$da10_3$	$da10_2$	$da10_1$	$da10_0$	m9	$da9_3$	$da9_2$	$da9_1$	$da9_0$	m8	$da8_3$	$da8_2$	$da8_1$	$da8_0$
R3	m15	$da15_3$	$da15_2$	$da15_1$	$da15_0$	m14	$da14_3$	$da14_2$	$da14_1$	$da14_0$	m13	$da13_3$	$da13_2$	$da13_1$	$da13_0$	m12	$da12_3$	$da12_2$	$da12_1$	$da12_0$
R4	m19	$da19_3$	$da19_2$	$da19_1$	$da19_0$	m18	$da18_3$	$da18_2$	$da18_1$	$da18_0$	m17	$da17_3$	$da17_2$	$da17_1$	$da17_0$	m16	$da16_3$	$da16_2$	$da16_1$	$da16_0$
R5	m23	$da23_3$	$da23_2$	$da23_1$	$da23_0$	m22	$da22_3$	$da22_2$	$da22_1$	$da22_0$	m21	$da21_3$	$da21_2$	$da21_1$	$da21_0$	m20	$da20_3$	$da20_2$	$da20_1$	$da20_0$
R6	m27	$da27_3$	$da27_2$	$da27_1$	$da27_0$	m26	$da26_3$	$da26_2$	$da26_1$	$da26_0$	m25	$da25_3$	$da25_2$	$da25_1$	$da25_0$	m24	$da24_3$	$da24_2$	$da24_1$	$da24_0$
R7	m31	$da31_3$	$da31_2$	$da31_1$	$da31_0$	m30	$da30_3$	$da30_2$	$da30_1$	$da30_0$	m29	$da29_3$	$da29_2$	$da29_1$	$da29_0$	m28	$da28_3$	$da28_2$	$da28_1$	$da28_0$

Note: Each channel's mask can be represented as m# and the corresponding trimming DAC bit by $da\#_x$, where the pound sign (#) is used to indicate the channel number and "x" represents the bit position. See the example below for register R0.

MSB Data Register (R0)

R0	m3	$da3_3$	$da3_2$	$da3_1$	$da3_0$	m2	$da2_3$	$da2_2$	$da2_1$	$da2_0$	m1	$da1_3$	$da1_2$	$da1_1$	$da1_0$	m0	$da0_3$	$da0_2$	$da0_1$	$da0_0$

NAME	*FUNCTION*	*RESET VALUE*
m3	Channel 3 mask, 1 = mask	0
$DA3_{3:0}$	Channel 3 threshold trim, [0:0] ≈ -150mV, [1:1] ≈ 0mV, Step ≈ -10mV	0
m2	Channel 2 mask, 1 = mask	0
$DA2_{3:0}$	Channel 2 threshold trim, [0:0] ≈ -150mV, [1:1] ≈ 0mV, Step ≈ -10mV	0
m1	Channel 1 mask, 1 = mask	0
$DA1_{3:0}$	Channel 1 threshold trim, [0:0] ≈ -150mV, [1:1] ≈ 0mV, Step ≈ -10mV	0
m0	Channel 0 mask, 1 = mask,	0
$DA0_{3:0}$	Channel 0 threshold trim, [0:0] ≈ -150mV, [1:1] ≈ 0mV, Step ≈ -10mV	0

MSB

Global Data Register (R8)

R8	tcm1	tcm0	filtena	B6	B5	B4	B3	tos2	tos1	tos0	trke	trk	tds2	tds1	tds0	tdm1	tdm0	tria	tri2	tri1

Operation Control

NAME	*FUNCTION*	*RESET VALUE*
tcm 1:0	Comparator multi-fire suppression, 00 = 0s, 01= 100ns, 10 = 1us, 11 = 2us	0
filtena	1 = enables additional filtering of input signal	0
B6	General purpose SPI data bit	0
B5	General purpose SPI data bit	0
B4	General purpose SPI data bit	0
B3	General purpose SPI data bit	0
tos 2:0	Timeout slope select 000 to 111 = 9.3, 4.6, 2.3, 1.2, 0.6, 0.45, 0.3, 0.15 us	0
trke	Enhanced simultaneous events mode, 1= active	0
trk	Simultaneous events mode, 1= active	0
tds 2:0	Time detect TAC slope select 000 to 111 = 19.4, 9.8, 4.9, 2.5, 1.25, 0.83, 0.63, 0.31 us	0
tdm 1:0	TAC mode (00 = time of occurrence, 01 = rise time, 10 = fall time, 11 = time over threshold)	00 0
tria	PDE/PDF driven on event (1 = driven on event, 0 = always driven (if 1, tri1 must be 0))	0
tri2	Valid tristate control (1 = tristate, 0 = driven)	0
tri1	PDE/PFD driven on RR (1 = trist. on RR, 0 = always driven)	0

MSB

Global Data Register (R9)

R9	-	-	-	-	-	-	-	-	-	B2	B1	B0	-	aux	sth	thpd0	thpd2	thpd1	thpd0	lock

Test Control

NAME	*FUNCTION*	*RESET VALUE*
Bits 19:11	Reserved	0
B 2:0	General purpose SPI data bit	0
aux	Baseline/lock output port, 1 = PDOUT, 0 = AAOUT	0
sth	Disables internal threshold DAC for external bypass	0
thpd 3:0	PD reference trim, [0:0] ≈ -150mV, [1:1] ≈ 0mV, Step ≈ -10mV	0
lock	Baseline/lock mode select, 1 = lock mode **Note: all channels except desired must be masked**	0

MSB

Global Data Register (R10)

R10	-	-	-	-	-	-	-	-	-	-	Vd9	Vd8	Vd7	Vd6	Vd5	Vd4	Bd3	Vd2	Vd1	Vd0

NAME	*FUNCTION*	*RESET VALUE*
Bits 10: 19	Reserved	
Vd 0:9	10-bit Threshold DAC, ~2V full scale, ~1.95 mV step 0mV baseline.	0

Single Chip and Daisy Chain Configurations

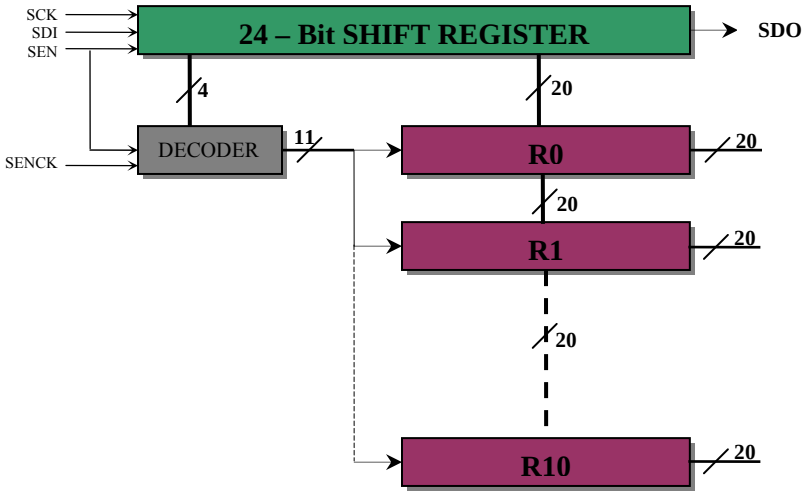


Fig. 3 Simplified block diagram of the Serial Peripheral Interface

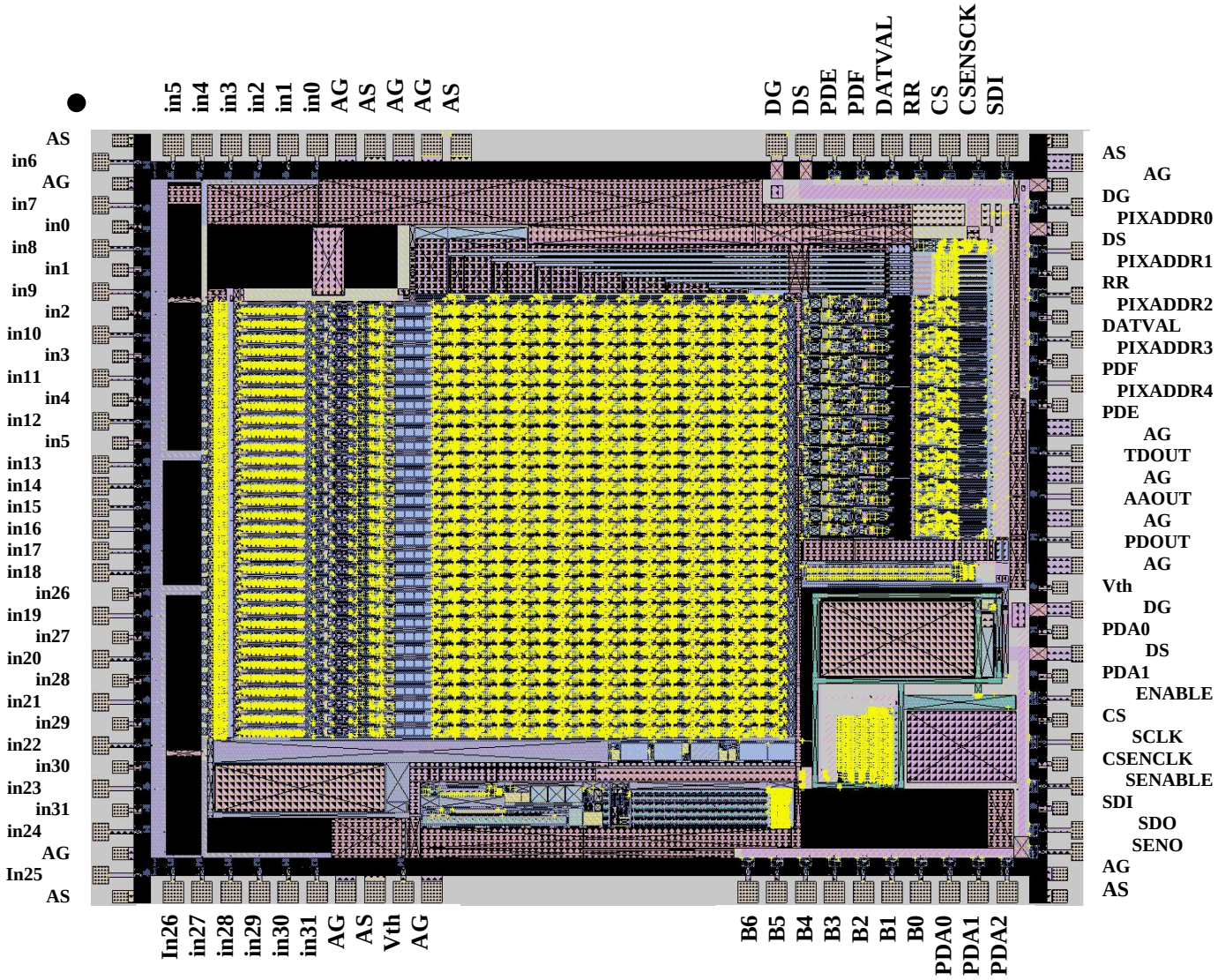
A simplified representation of the SPI is shown in Fig. 3. In single chip mode, with SENABLE high data on SDI is shifted into the 24-bit shift register on the rising edge of SCK. The four register address bits (A3:A0) are loaded MSB first, followed by the 20-bit configuration data word (D19:D0). When the full 20-bit word has been shifted in, SENABLE is pulled low, loading the appropriate register. The buffered serial output of the shift register is available on the SDO pin. Data is shifted out on the rising edge of SCK. All configuration register bits are set to their default value on power-up or whenever the system RESET is asserted.

In daisy chain mode, multiple PDDASICs may be configured by a single host microcontroller in two ways.

(i) The ASICs SENABLE, and SCK pins are tied together and the host writes the configuration data to the first chip in the chain. In this a case, a total of *m* PDASIC chips are configured by connecting each SDO (except the last) to the SDI of the next chip, forming a single *m* x 24-bit shift register. During the write in process, SENABLE is held high while *m* x 24-bit words are clocked in to the SDI of the first chip. SENABLE is then pulled low, loading the addressed register in each ASIC simultaneously.

(ii) In the second configuration, SENABLE is not common to all the ASICS in the chain. Instead, the output SENO from the first chip is fed into the SENABLE input of the second chip etc. At the end of each 24-bit write-in to the shift register, SDI is brought high and a clock CSENCLK (at falling edge) is used to latch the data into the appropriate register. An additional clock CSENCLK with SDI low is used to advance the token by setting SENO high. With this setup, the chips can be configured one by one.

PDD ASIC Pinout



BROOKHAVEN NATIONAL LABORATORY
Instrumentation Division

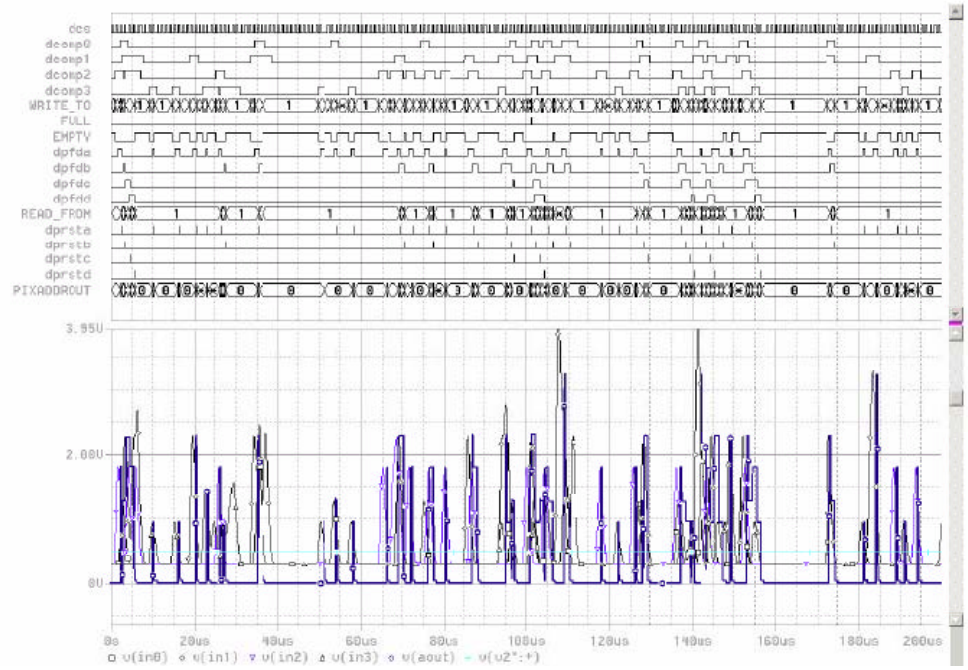
Table 1 ASIC Pin List

Num. Pins	Pin Num.	Signal Name	In/Out	Description
2	5,106	in0	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	7,107	in1	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	\9,108	in2	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	11,109	in3	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	13,110	in4	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	15,111	in5	In	DC or AC coupled charge input from detector. ESD protected (mild).
20	2,4,6,8,10,12,14 16 – 21 23,25,27,29,31,33,35	in6,in7,in8,in9,in10,in11,in12 in13 – in18 in19,in20,in21,in22,in23,in24 in25	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	22,37	in26	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	24,38	in27	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	26,39	in28	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	28,40	in29	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	30,41	in30	In	DC or AC coupled charge input from detector. ESD protected (mild).
2	32,42	in31	In	DC or AC coupled charge input from detector. ESD protected (mild).
7	1,36,44,57,91,101,104	AS		Analog supply: +3.3V.
2	3,34,43,46,58,72,74,76,788 9,102,103,105	AG		Analog ground: 0V.
2	45,71	Vth	In/Out	Threshold input for the comparator trigger level. ESD protected.
1	47	B6	Out	External general purpose SPI data bit.
1	48	B5	Out	External general purpose SPI data bit.
1	49	B4	Out	External general purpose SPI data bit.
1	50	B3	Out	External general purpose SPI data bit.
3	51 - 53	B 2:0	Out	External general purpose SPI data bits.
3	54, 55/67, 56/69	PDA 2:0	Out	Peak detector address. Tristataed with Dataval. ESD protected.
1	59	SENO	Out	Clocked SENABLE output. ESD protected.
1	60	SDO	Out	Output of shift register. Tristated with SENABLE. ESD protected.
2	61, 92	SDI	In	SPI Data input. ESD protected
1	62	SENABLE	In	CMOS level. It allows the clock (SCLK) to acces the chip for Writein operation. On the falling edge, data is latched into the addressed SPI configuration register when SDI is low (single chip mode). ESD protected.
2	63,93	CSENCLK	In	Dual function in daisy chain mode. (i) Used to latch register data when SDI is high. (ii) Clock out SENABLE for daisy chain on Pin SENO when SDI is low. ESD protected.

Num. Pins	Pin Num.	Signal Name	In/Out	Description
1	64	SCLK	In	Clock for Writein.. Clock is enabled with SENABLE. ESD protected.
2	65,94	CHIPSELECT (CS)	In	Enables RR input (active high). ESD protected.
1	66	ENABLE	In	PDD reset. When high, PDD is enabled. Active low reset. ESD protected.
1	73	PDOUT	Out	Analog Peak Detect/Baseline Output. ESD protected.
1	75	AAOUT	Out	Auxiliary Analog Output. ESD protected.
1	77	TDOUT	Out	Analog Time Detector Output. ESD protected.
2	79,98	PDE	Out	Peak Detector Empty Indicators. ESD protected.
2	81,97	PDF	Out	Peak Detector Full Indicators. ESD protected.
2	83,96	DATVAL	Out	Data Valid. ESD protected.
2	85,95	RR	In	Data read request (active high). ESD protected.
5	80,82,84,86,88	PIXADDR 4:0	Out	Pixel Address Signals. Tristataed with Dataval. ESD protected.
3	70,89,100	DG		Digital ground: 0V.
3	68,87,99	DS		Digital supply: +3.3V.
111		**Total Pin**		

Simulation Results

Fig. 4 shows the PSPICE results of a transistor level (BSIM3V3.2 model) simulation of PDD ASIC characterized by four input channels and four peak detectors. The four input channels receive Gaussian pulses of 1.2 μs peaking time with 1, 2, 1.5, and 0.6 V amplitude respectively. The pulse arrival times are Poisson distributed with a mean rate of 100 kHz/channel. The input signals are shown on the bottom panel. The upper trace dcs is RR, which runs at a rate of 1 MHz (slightly faster than twice the average pulse input rate). The next 16 traces are the internal digital signals of the PDD ASIC arbitration logic. The lowest digital trace is the pixel address (PIXADDROUT) corresponding to the hit channel that is currently being read out. If the chip is EMPTY when a read request occurs, it responds by setting PDOUT to 0V and PIXADDROUT to 00. The full simulation covers 200 μs during which 84 input pulses are issued. Because of the high rate per channel there is significant pileup and only 62 pulses can be distinguished by the internal comparators. Of these 62 pulses none are blocked. The second simulation plot shows a detail of a time interval in which 4 pulses arrive within less than 2 μs, more than twice the average arrival rate. Within this group the third and fourth pulses cross threshold within 5.8. Nevertheless, all pulse amplitudes and their corresponding channel addresses are properly processed by the PDASIC. If the CS rate is decreased to 500 kHz, the efficiency drops to 93.5%, i.e. 58 of the 62 pulses are recorded and 4 are blocked by the all-busy condition.



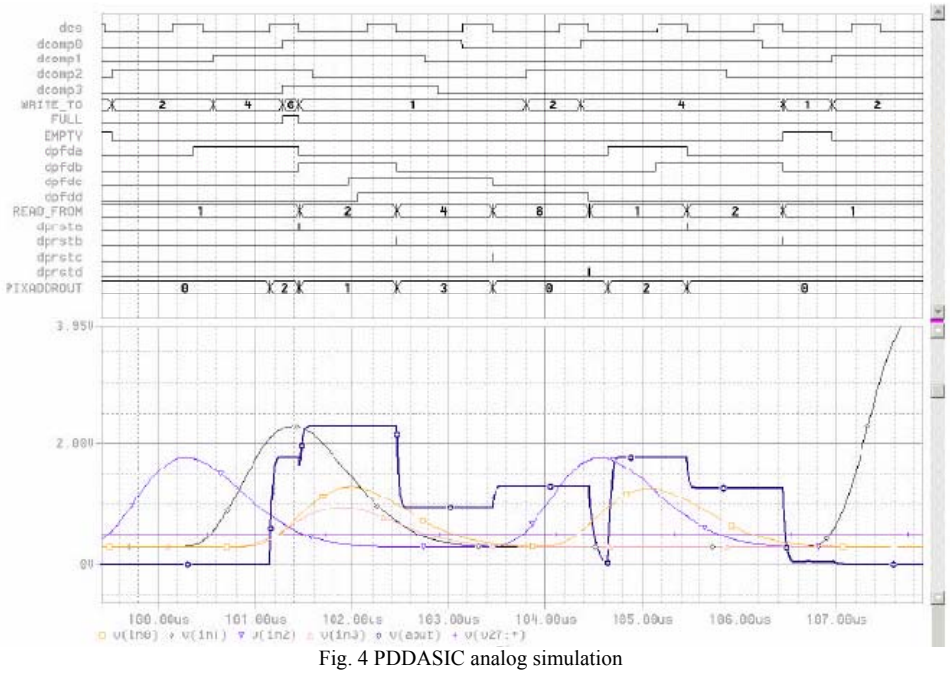


Fig. 4 PDDASIC analog simulation

References

G. De Geronimo, P. O'Connor, J. Grosholz, *A generation of CMOS readout ASICs for CZT detectors*, IEEE Trans. Nucl. Sci., 47 (2000) 1857-1867

G. De Geronimo, P. O'Connor, A. Kandasamy, *Analog CMOS peak detect and hold circuits - Part 1. analysis of the classical configuration*, Nucl. Instrum. & Meth., A484 (2002) 533-543.

G. De Geronimo, P. O'Connor, A. Kandasamy, *Analog CMOS peak detect and hold circuits - Part 2. The two-phase offset-free and derandomizing configuration*, Nucl. Instrum. & Meth., A484 (2002) 544-556.

G. De Geronimo, A. Kandasamy, P. O'Connor, *Analog peak detector and derandomizer for high rate spectroscopy*, Proc. 2001 Nuclear Science Symp., San Diego, CA 2001, IEEE Trans. Nucl. Sci., 49 (2002) 1769-1773.

P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASICs*, Pres. Symposium on Radiation Measurements, Ann Arbor, Michigan, 2002, Nucl. Instrum. & Meth., A505 (2003) 352-357.

P. O'Connor, G. De Geronimo, A. Kandasamy, *Amplitude and time measurement ASIC with analog derandomization: first results*, Proc. 2002 Nuclear Science Symp., Norfolk, VA 2002, IEEE Trans. Nucl. Sci., 50 (2003) 892-897.

P. O'Connor, G. De Geronimo, J. Grosholz, A. Kandasamy, S. Junnarkar, J. Fried, *Multichannel energy and timing measurements with the peak detector/derandomizer ASIC*, Proc. 2004 Nuclear Science Symp., Rome, Italy, 2004.

A. Dragone, G. De Geronimo, J. Fried, A. Kandasamy, P. O'Connor, E. Vernon, *The PDD ASIC: highly efficient energy and timing extraction for high-rate applications*, Proc. 2005 Nuclear Science Symp., Puerto Rico, 2005,