IIIT BANGALORE

VLS 502

Analog CMOS VLSI Design

Project Report

Submitted By:-

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Submitted To:-

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1. Specifications

In this project, we have developed an LDO designed to operate under various conditions. The design includes both externally compensated and internally compensated configurations. We have explored multiple technology nodes for this purpose. Specifically, the figure below showcases the design using the 45nm technology node, with the corresponding technology node file attached. Our objective is to optimize the LDO to handle both maximum and minimum load conditions effectively.

We have the following specifications:-

Table 1: Specifications Table

Parameter	**Value**
V_{in}	1.4 V
V_{out}	1 V
PSRR	60 dB
$I_{load,\ max}$	2 mA
C_{load}	1 F
$I_{quiescent}$	50 u A

2. Purpose of an LDO

An LDO is a type of linear regulator, which can regulate output voltages to values very close to the supplied input voltage. The input to output differential voltage, at which the LDO fails to regulate the output is defined as the dropout voltage.

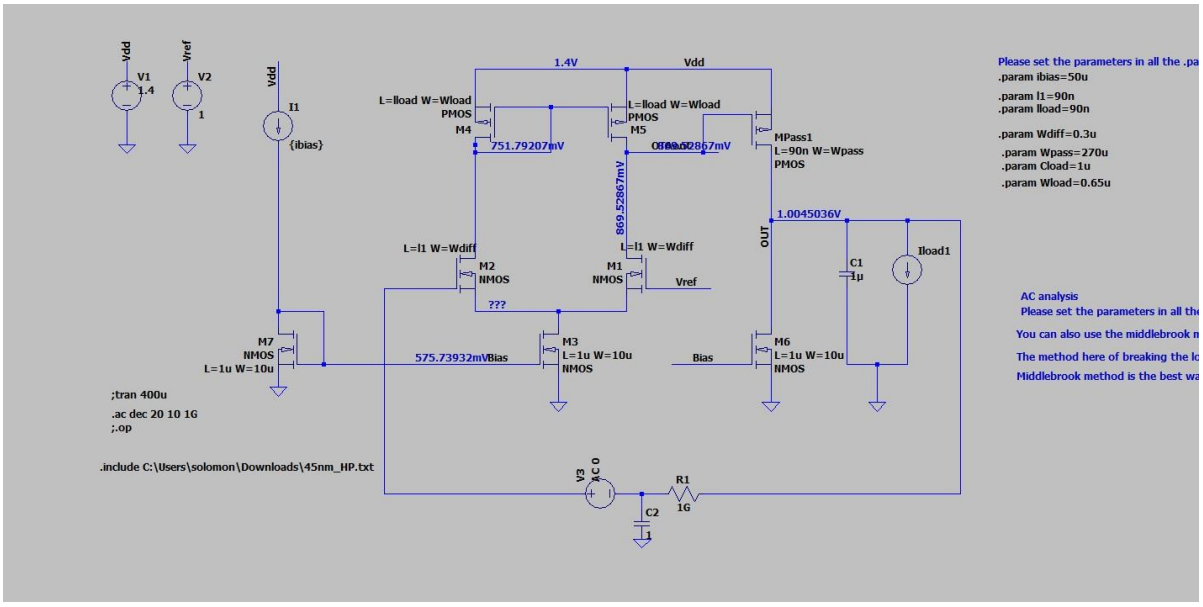
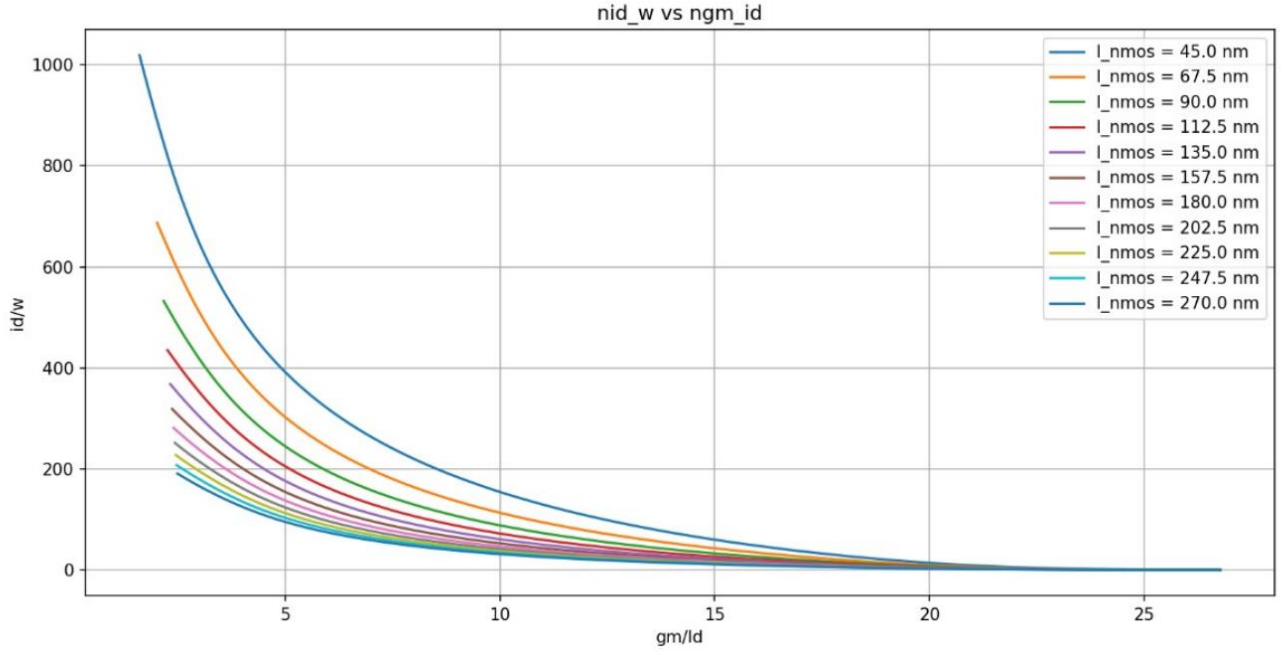
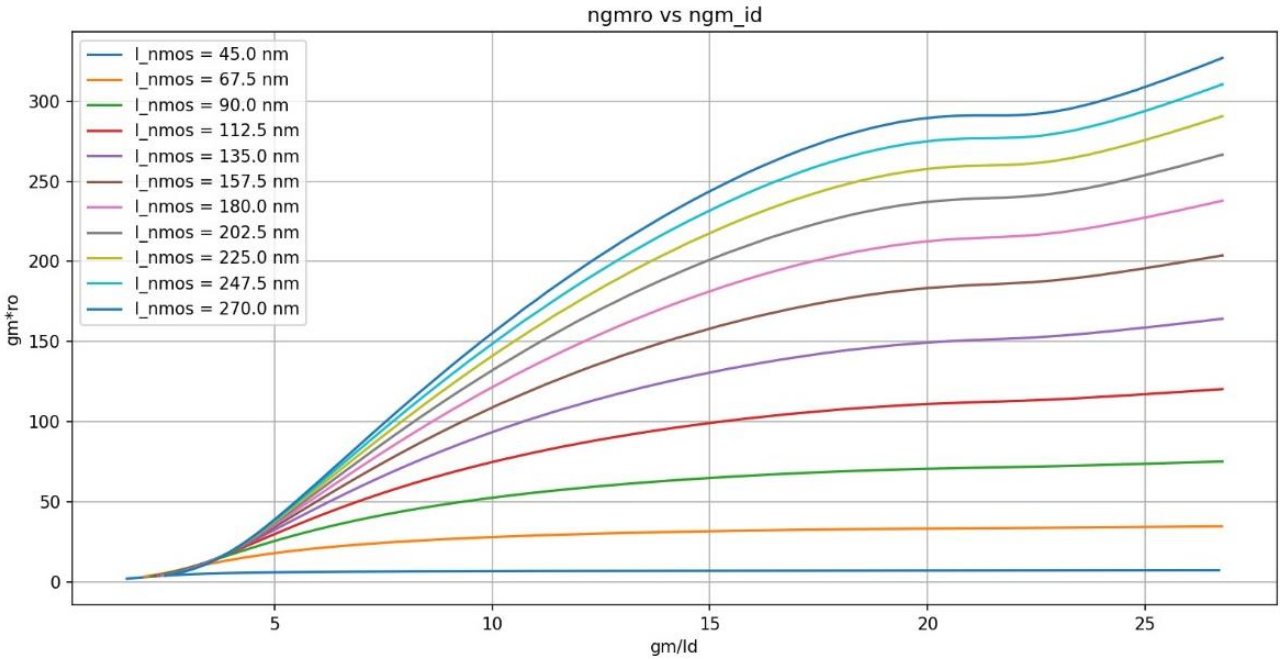


Figure 1: LDO schematic

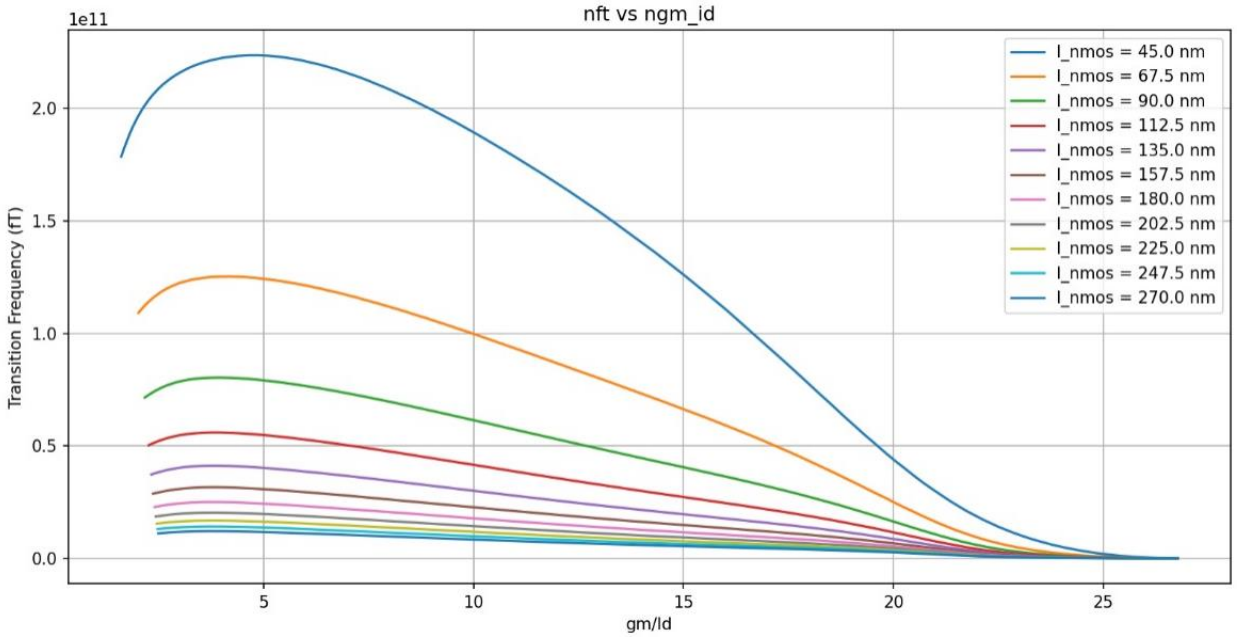
3. Relevance of Techplots (45 nm tech) //Python waveforms



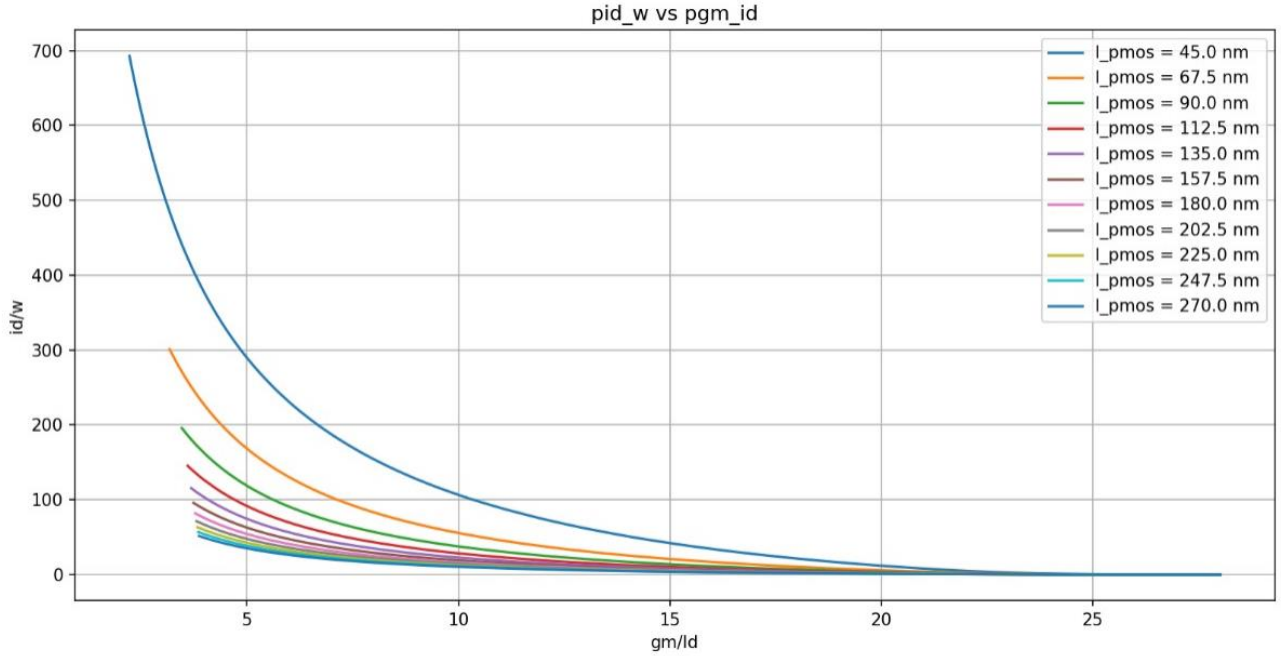
NMOS Techplots - Id/W



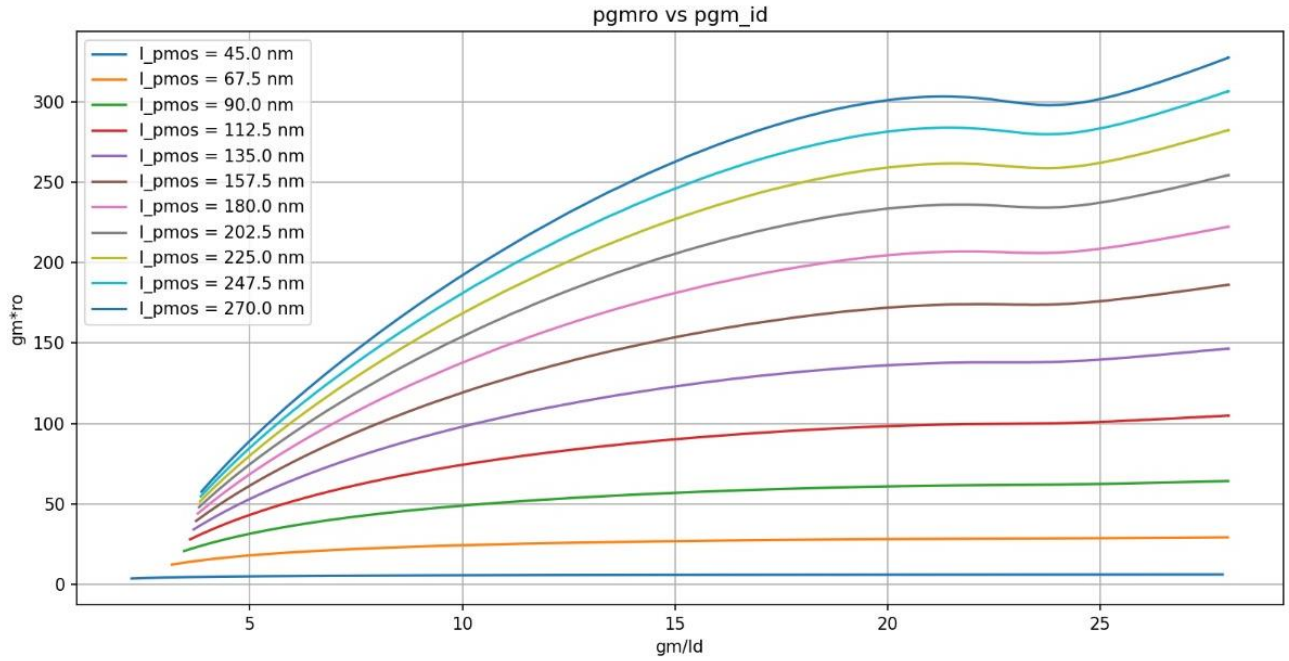
NMOS Techplots- gmro



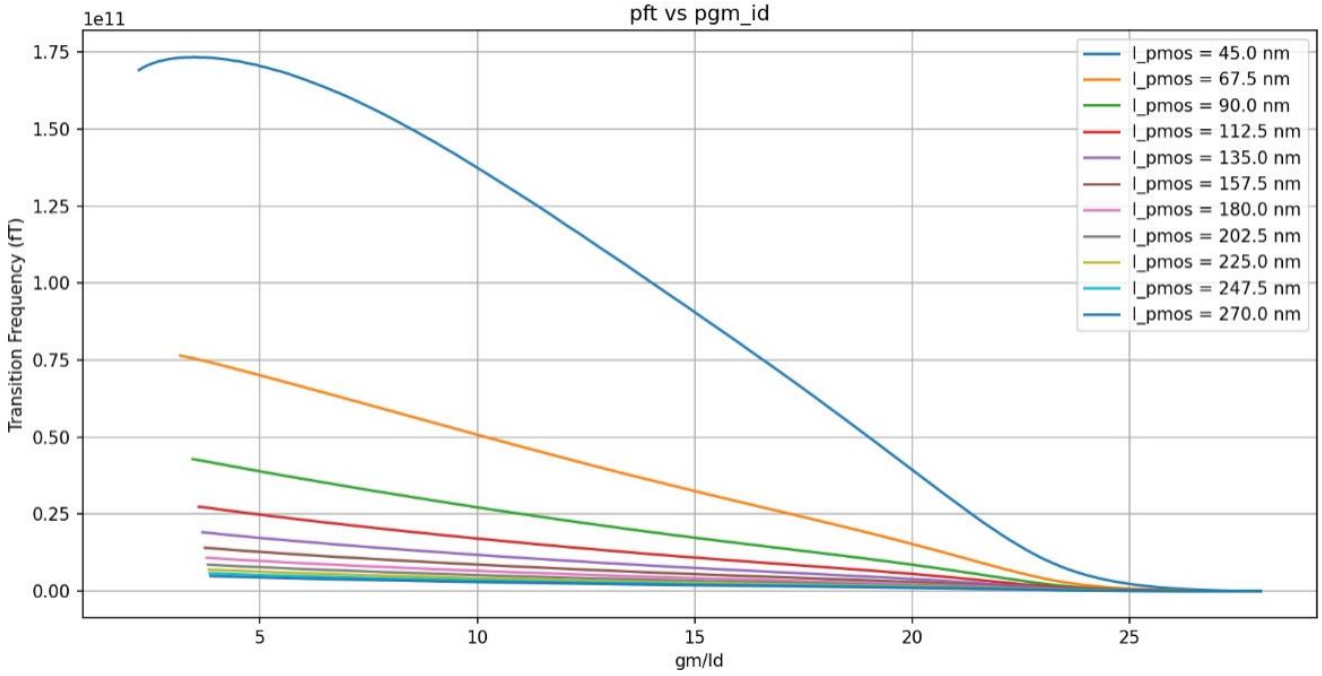
NMOS Techplots - fT



PMOS Techplots-Id/W



PMOS Techplots- gmro



PMOS Techplots-- fT

4. FET Sizes

we Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 3: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	270u/90n	10	50	40	30 GHz
Diff-Amp pmos	0.65u/90n	10	20	40	30 GHz
Diff-Amp nmos	0.3u/90n	10	20	90	60 GHz
Current Mirror nmos	1u/10n	-	-	40	10 GHz

5. Stability Analysis

For Heavy load we get the following curve:

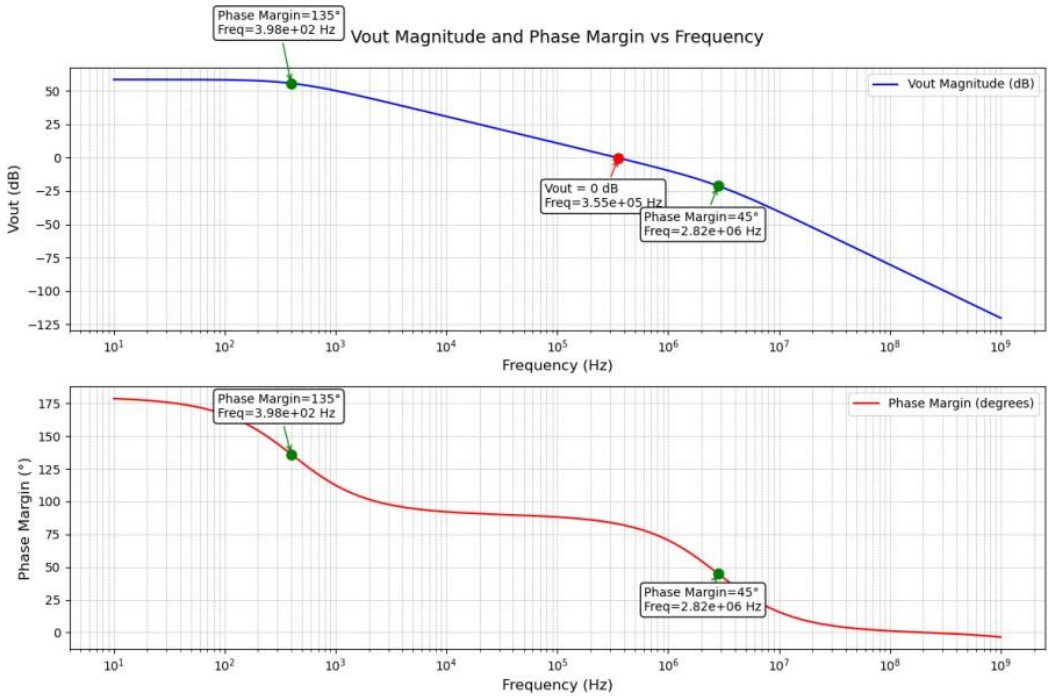


Figure 2: Output on Python

For Light load we get the following curve

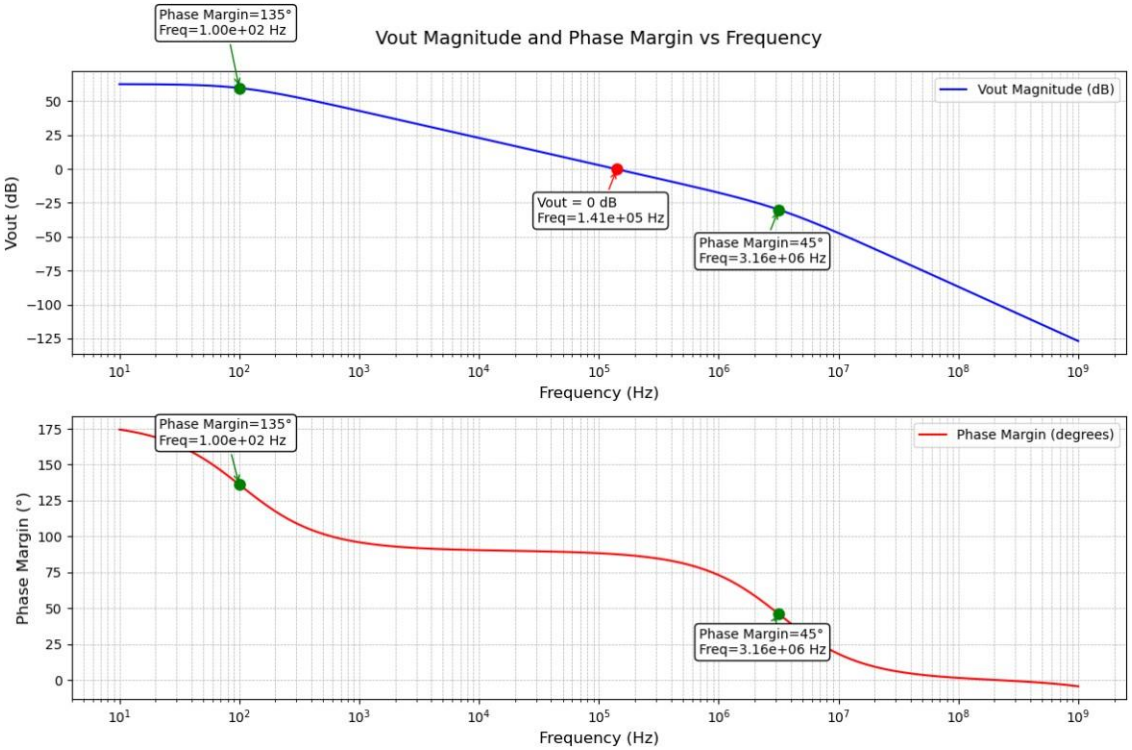


Figure 3: Output on Python

From the above analysis, we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. We can also observe a lesser phase margin of 76 degrees for the heavy load case than that of the light load case. From this analysis, we can say that when we apply light load, we get a more stable system.

Table 4: Key Metrics under Heavy and Light Load Conditions

Parameter	Heavy Load	Light Load
DC Loop Gain (dB)	58.7	62.32
Unity Gain Bandwidth (KHz)	355khz	141khz
Phase Margin (degrees)	82.89	87.58
Pole 1 (Hz)	398	100
Pole 2 (MHz)	2.82	3.16

7. PSRR Simulation Results

We created three schematics in LTSpice to evaluate the three specified conditions. Additionally, we developed a simulation artifact to analyze and visualize the results effectively.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

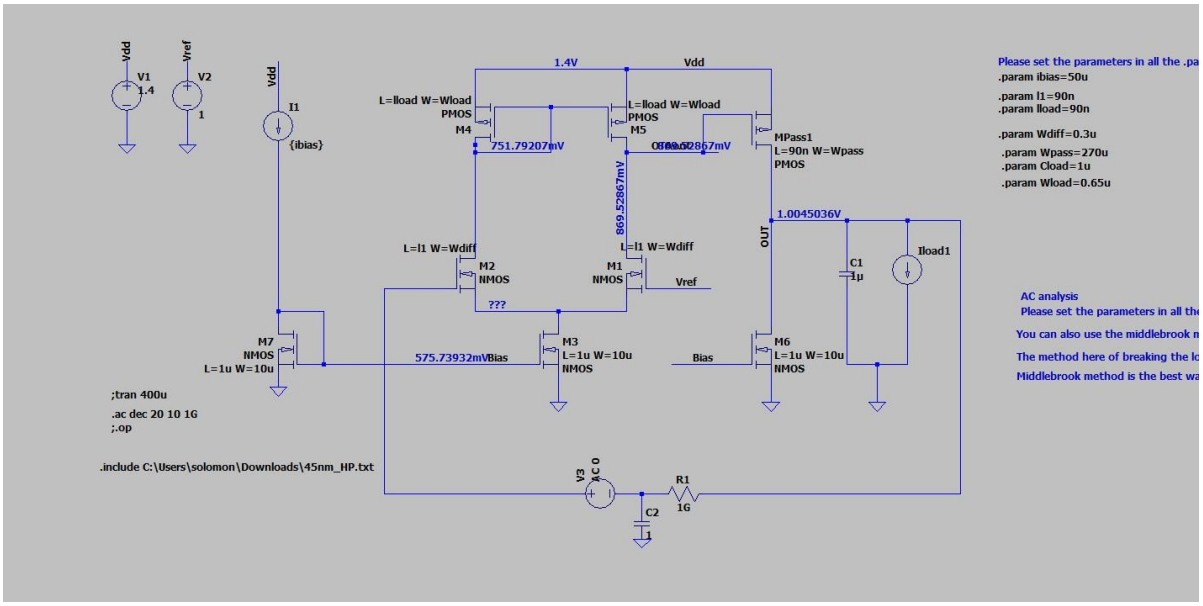


Figure 5: Schematic

Output Log File:-

SPICE Output Log: C:\Users\solomon\Downloads\502_PSRR_Demo.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\solomon\Downloads\502_PSRR_Demo.asc
Start Time: Fri Dec  6 18:25:51 2024
solver = Normal
Maximum thread count: 4
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m7           m8
Model:     nmos         nmos         nmos         nmos         nmos
Id:      2.49e-05     2.48e-05     4.97e-05     5.06e-05     5.00e-05
Vgs:     6.04e-01     6.04e-01     5.76e-01     5.76e-01     5.76e-01
Vds:     3.56e-01     3.53e-01     3.96e-01     1.01e+00     5.76e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.66e-01     4.66e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.45e-01     1.45e-01     1.33e-01     1.33e-01     1.33e-01
Gm:      2.40e-04     2.40e-04     6.24e-04     6.34e-04     6.28e-04
Gds:     5.11e-06     5.13e-06     1.98e-06     1.35e-06     1.54e-06
Gmb      5.55e-05     5.54e-05     1.44e-04     1.46e-04     1.44e-04
Cbd:     1.24e-16     1.24e-16     4.48e-15     3.97e-15     4.30e-15
Cbs:     2.20e-16     2.20e-16     8.00e-15     8.00e-15     8.00e-15

Name:       m4           m5         mpass
Model:     pmos         pmos         pmos
Id:     -2.48e-05    -2.48e-05    -1.01e-02
Vgs:    -6.52e-01    -6.52e-01    -6.49e-01
Vds:    -6.52e-01    -6.49e-01    -3.87e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.84e-01    -4.84e-01    -4.87e-01
Vdsat:  -1.81e-01    -1.81e-01    -1.77e-01
Gm:      2.39e-04     2.39e-04     9.95e-02
Gds:     4.87e-06     4.87e-06     2.52e-03
Gmb      5.07e-05     5.07e-05     2.11e-02
Cbd:     2.63e-16     2.63e-16     1.21e-13
Cbs:     4.96e-16     4.96e-16     2.16e-13

Total elapsed time: 0.189 seconds.
```

Figure 6: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Device Name	Device Type	|Vds|	|Vgs|	|Vt|	|Vgs|-|Vt|	Reason for saturation
Mpass1	pmos	3.87E-01	6.49E-01	4.87E-01	1.62E-01	|Vsd|>|Vgs|-|Vt|
M1	pmos	6.49E-01	6.52E-01	4.84E-01	1.68E-01	|Vsd|>|Vgs|-|Vt|
M2	pmos	6.52E-01	6.52E-01	4.84E-01	1.68E-01	|Vsd|>|Vgs|-|Vt|
M3	nmos	3.96E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M4	pmos	1.01E+00	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M5	pmos	3.53E-01	6.04E-01	4.66E-01	1.38E-01	|Vsd|>|Vgs|-|Vt|
M6	nmos	3.56E-01	6.04E-01	4.66E-01	1.38E-01	|Vsd|>|Vgs|-|Vt|
M7	nmos	5.76E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|

Figure 7: Operating regions

Output on Python:-

Phase margin and Gain

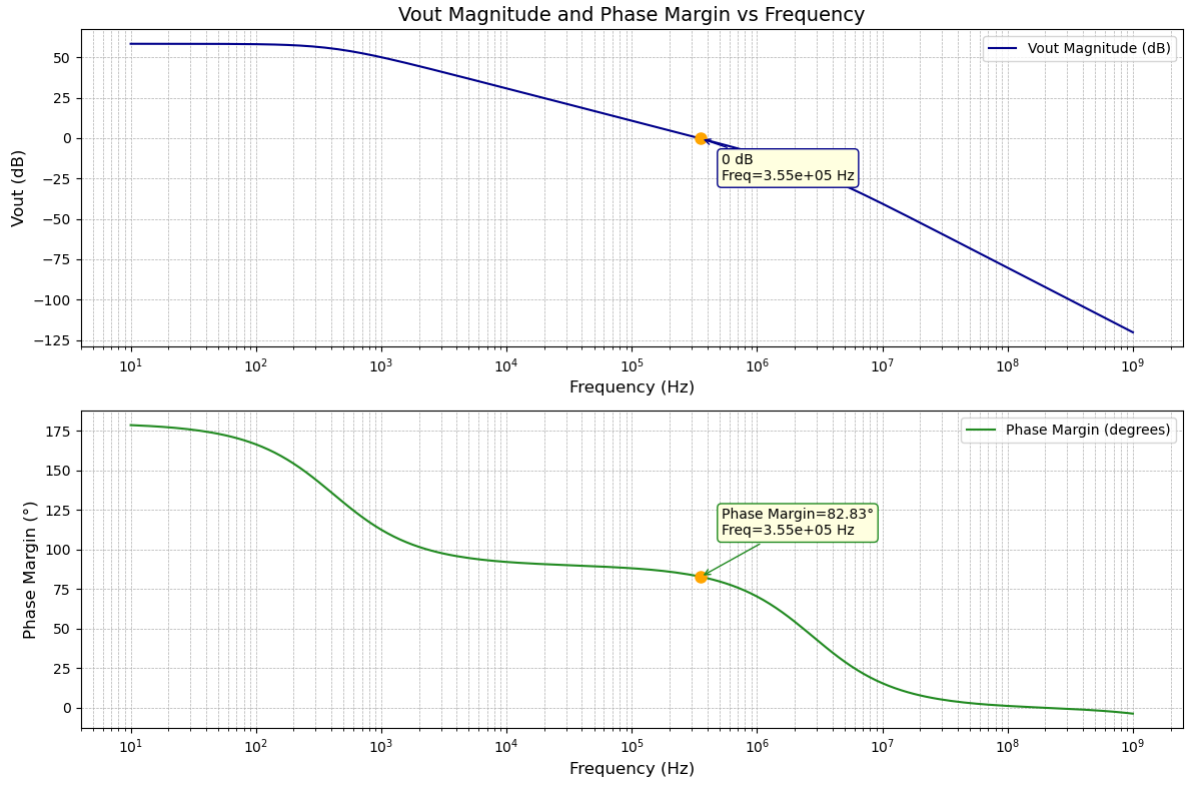


Figure 8: Gain and phase margin

The phase margin is 82.83

The output voltage (Loop gain) comes out to be close to 59.12db . The formula for loop gain is Adiff Apass where Adiff is differential amplifier gain and Apass is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

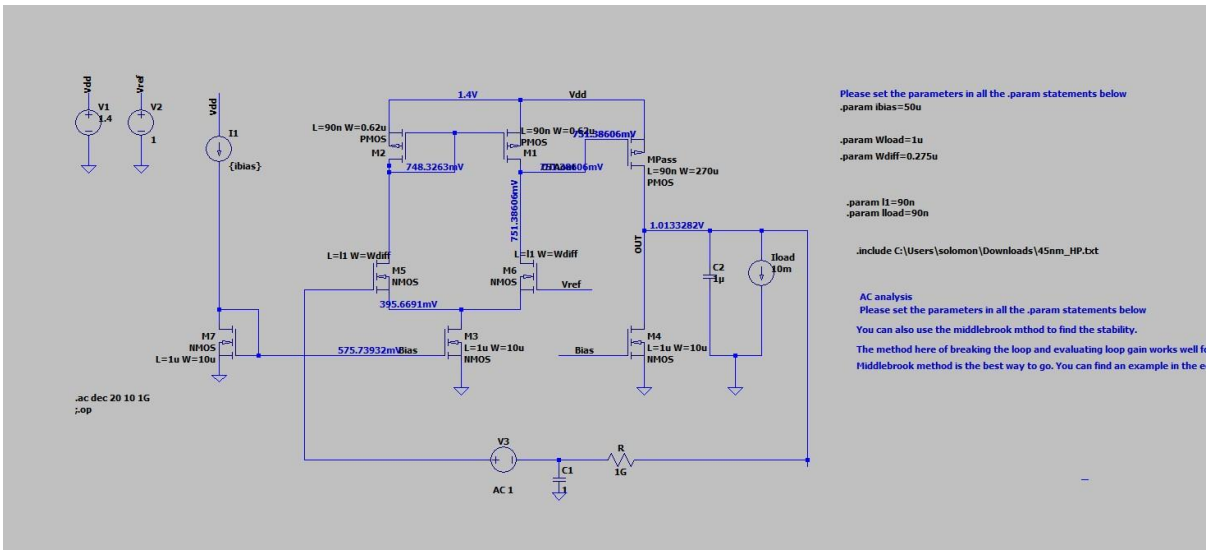
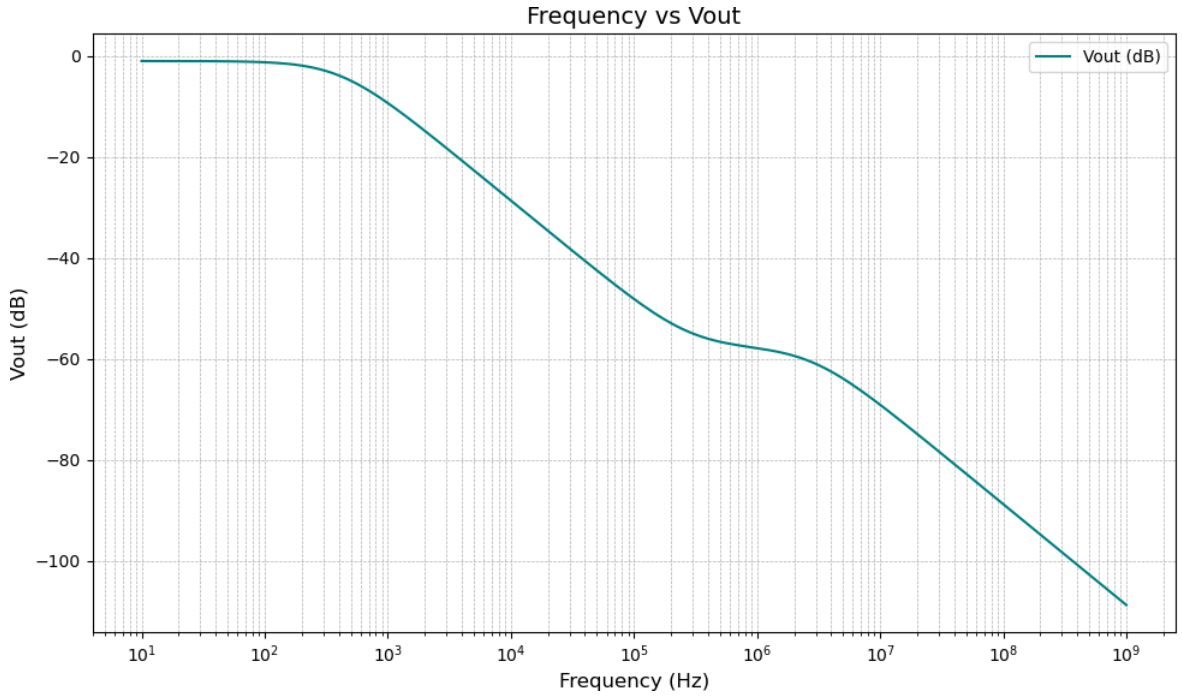


Figure 9: Schematic

Vout vs freq



VoutA vs freq

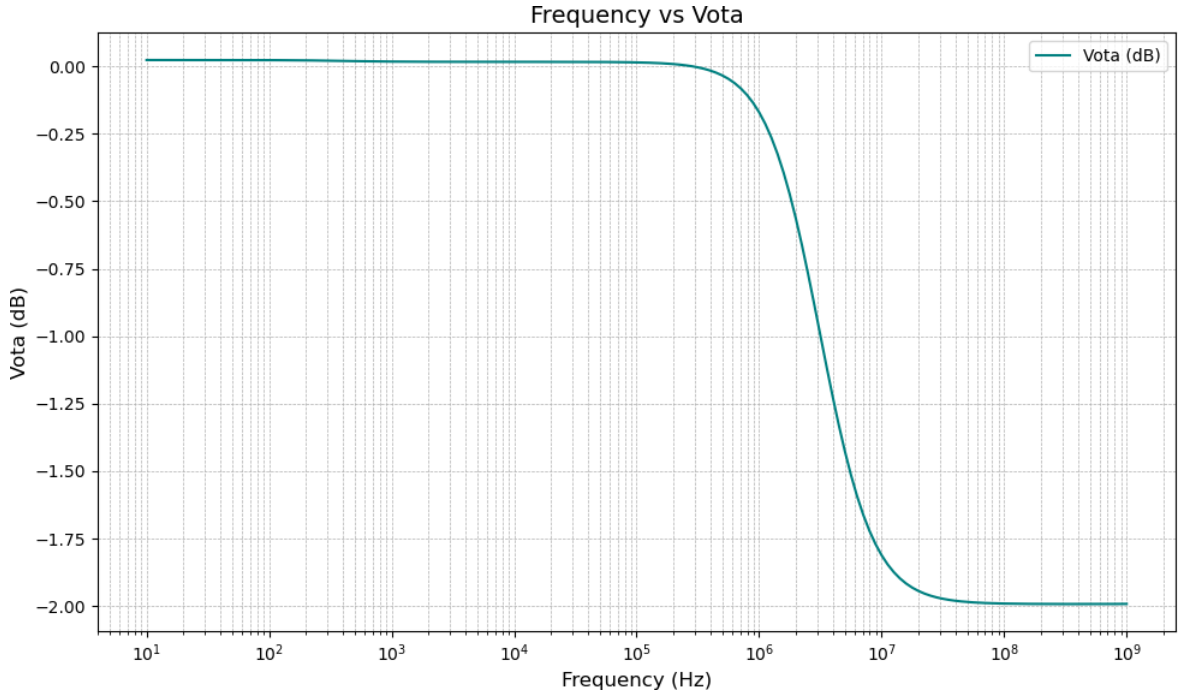


Figure 10: Phase margin

Case 3:- Closed Loop PSRR Calculation

Schematic

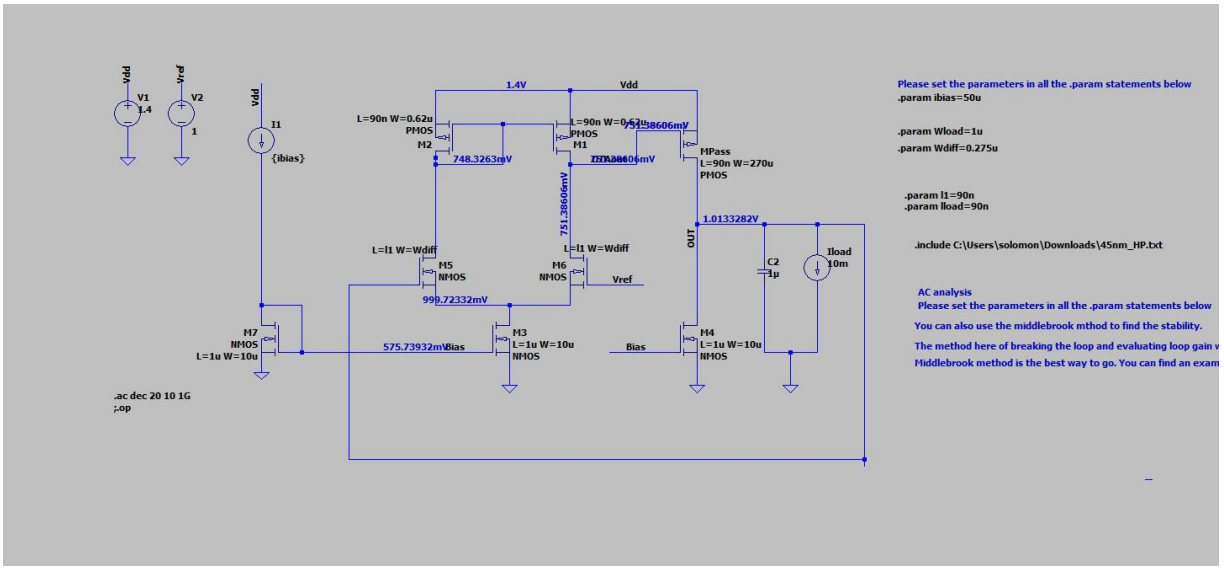


Figure 11: Schematic

Output on Python:-

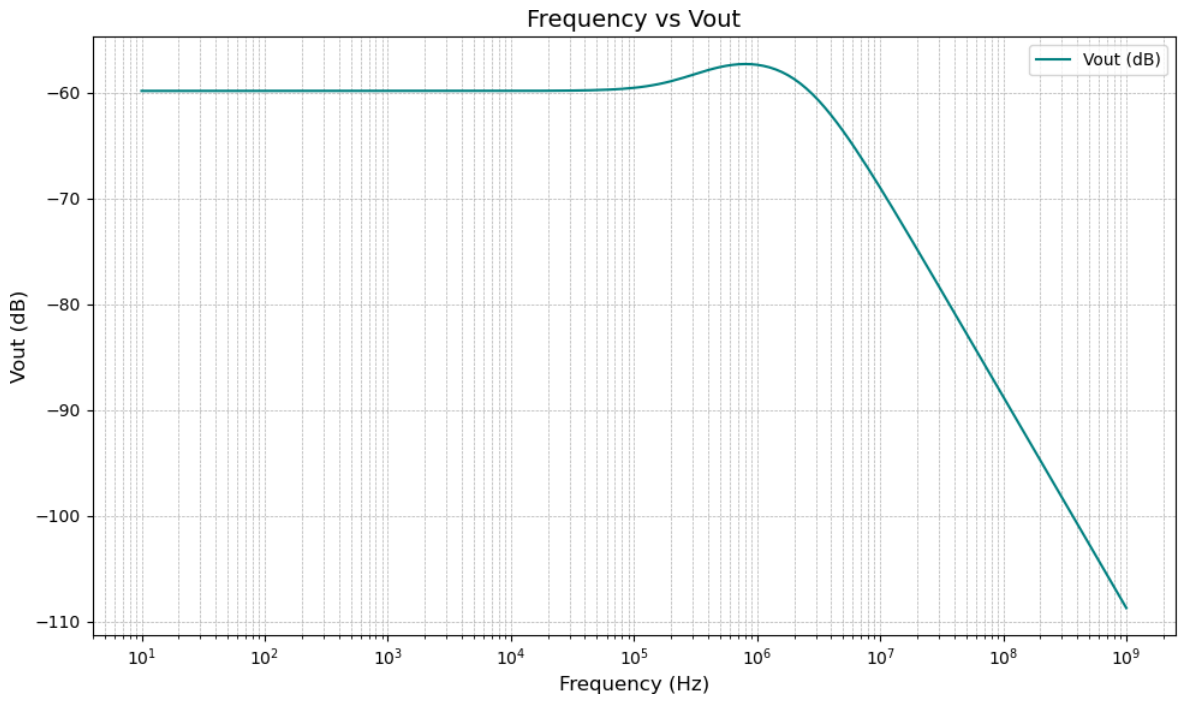


Figure 12: Output on Python

freq vs vouta

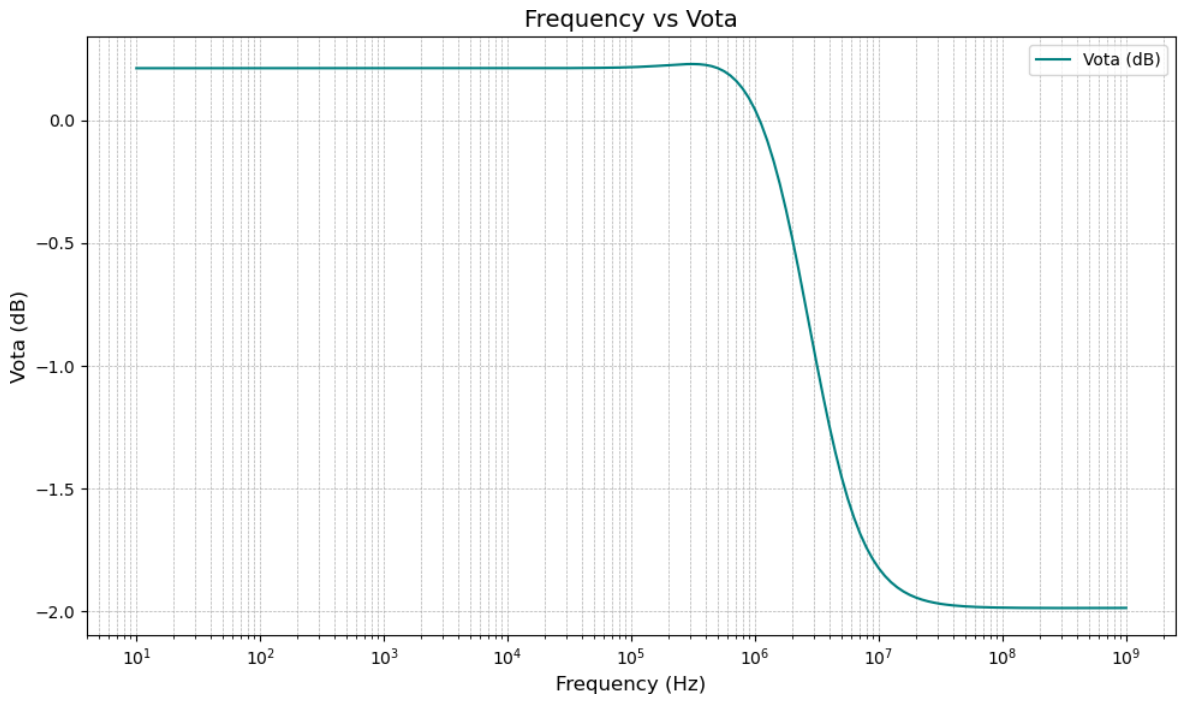


Figure 13: Vouta vs freq

Light Load (2ma)

Case 1:- Loop gain analysis

Schematic

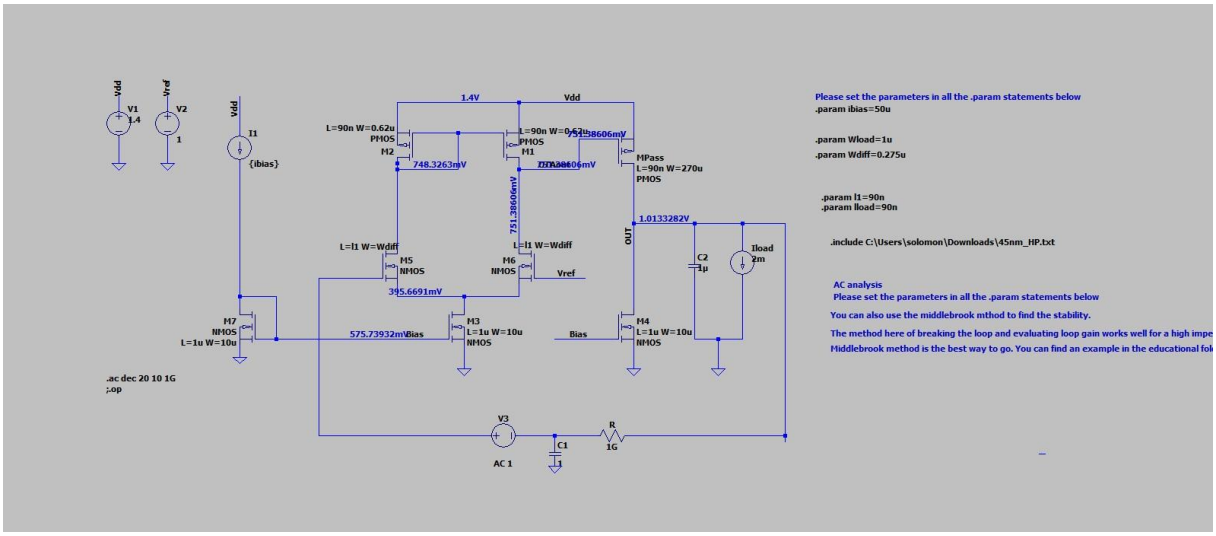


Figure 14: Schematic

Output Log File:-

SPICE Output Log: C:\Users\solomon\Downloads\502_PSRR_Demo.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\solomon\Downloads\502_PSRR_Demo.asc
Start Time: Fri Dec  6 18:25:51 2024
solver = Normal
Maximum thread count: 4
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m7           m8
Model:     nmos         nmos         nmos         nmos         nmos
Id:      2.49e-05     2.48e-05     4.97e-05     5.06e-05     5.00e-05
Vgs:     6.04e-01     6.04e-01     5.76e-01     5.76e-01     5.76e-01
Vds:     3.56e-01     3.53e-01     3.96e-01     1.01e+00     5.76e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.66e-01     4.66e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.45e-01     1.45e-01     1.33e-01     1.33e-01     1.33e-01
Gm:      2.40e-04     2.40e-04     6.24e-04     6.34e-04     6.28e-04
Gds:     5.11e-06     5.13e-06     1.98e-06     1.35e-06     1.54e-06
Gmb      5.55e-05     5.54e-05     1.44e-04     1.46e-04     1.44e-04
Cbd:     1.24e-16     1.24e-16     4.48e-15     3.97e-15     4.30e-15
Cbs:     2.20e-16     2.20e-16     8.00e-15     8.00e-15     8.00e-15

Name:       m4           m5          mpass
Model:     pmos         pmos         pmos
Id:     -2.48e-05    -2.48e-05    -1.01e-02
Vgs:    -6.52e-01    -6.52e-01    -6.49e-01
Vds:    -6.52e-01    -6.49e-01    -3.87e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.84e-01    -4.84e-01    -4.87e-01
Vdsat:  -1.81e-01    -1.81e-01    -1.77e-01
Gm:      2.39e-04     2.39e-04     9.95e-02
Gds:     4.87e-06     4.87e-06     2.52e-03
Gmb      5.07e-05     5.07e-05     2.11e-02
Cbd:     2.63e-16     2.63e-16     1.21e-13
Cbs:     4.96e-16     4.96e-16     2.16e-13


Total elapsed time: 0.189 seconds.
```

Figure 15: Output Log Details

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Device Name	Device Type	|Vds|	|Vgs|	|Vt|	|Vgs|-|Vt|	Reason for saturation
Mpass1	pmos	3.81E-01	5.31E-01	4.87E-01	4.40E-02	|Vsd|>|Vgs|-|Vt|
M1	pmos	5.31E-01	6.52E-01	4.85E-01	1.67E-01	|Vsd|>|Vgs|-|Vt|
M2	pmos	6.53E-01	6.53E-01	4.84E-01	1.69E-01	|Vsd|>|Vgs|-|Vt|
M3	nmos	3.99E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M4	pmos	1.02E+00	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M5	pmos	3.48E-01	6.06E-01	4.66E-01	1.40E-01	|Vsd|>|Vgs|-|Vt|
M6	nmos	4.70E-01	6.01E-01	4.65E-01	1.36E-01	|Vsd|>|Vgs|-|Vt|
M7	nmos	5.76E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|

Figure 16: Operating region

Output on Python:-

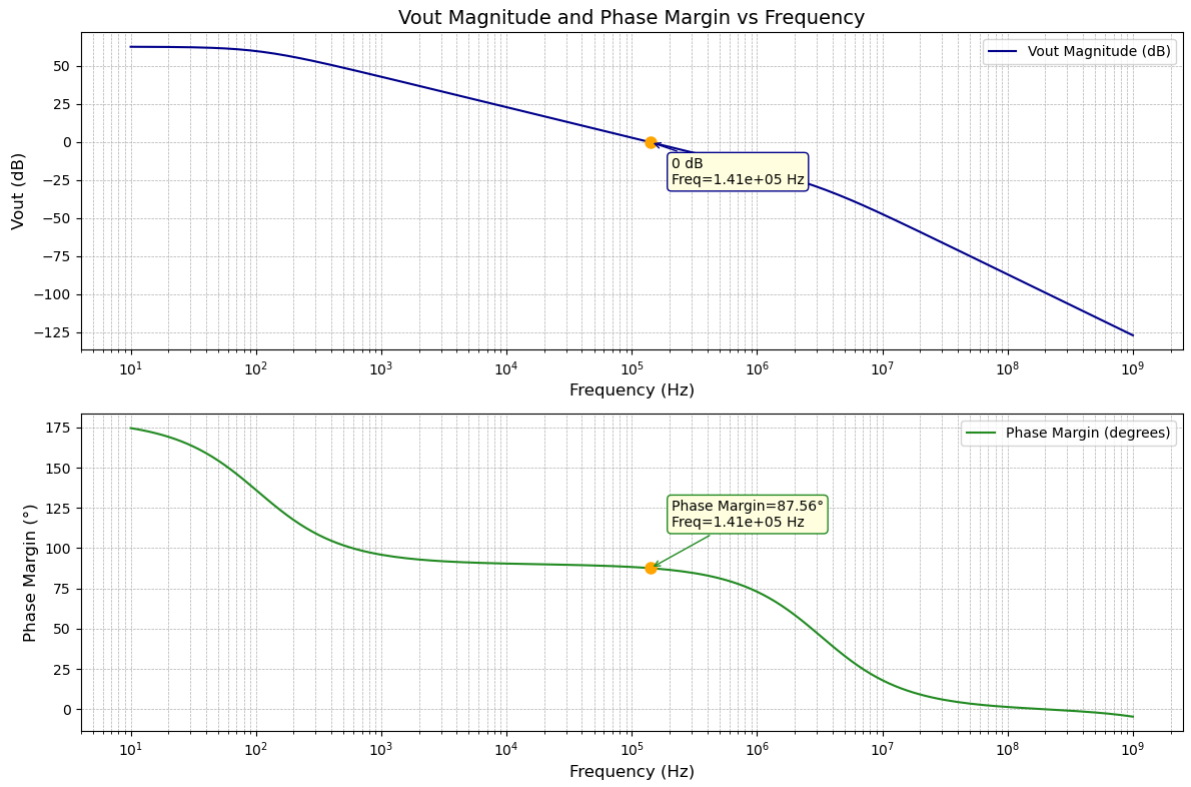


Figure 17: Output on Python

The phase margin obtained is 87.56 degrees. This value is more than that of the value obtained for heavy load. Thus proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR calculation

Schematic

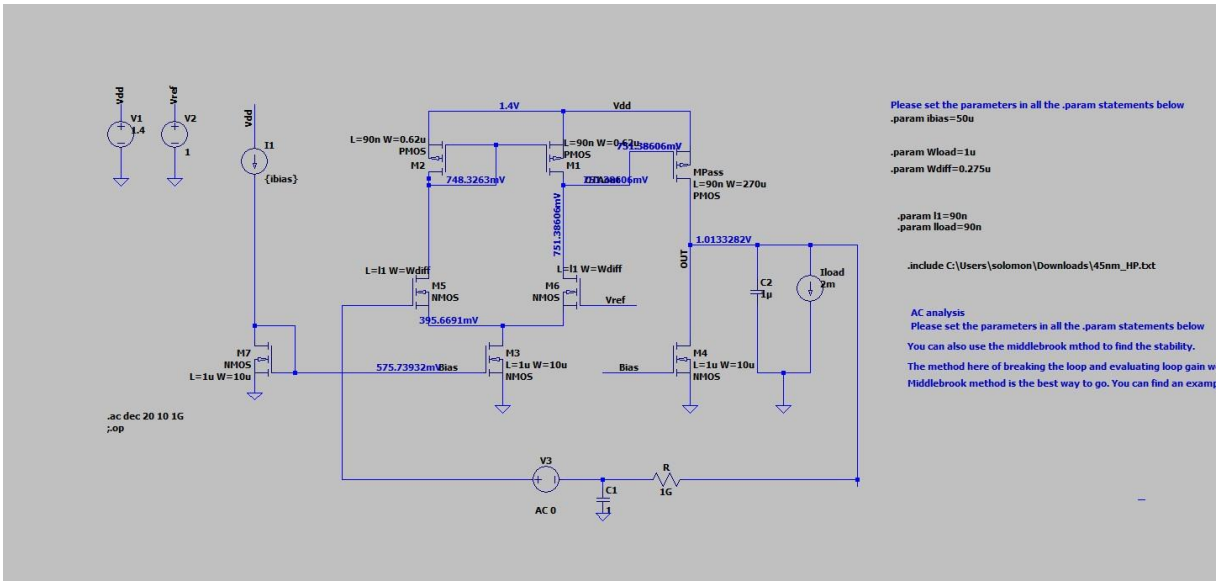


Figure 18: Schematic

Output on Python:-

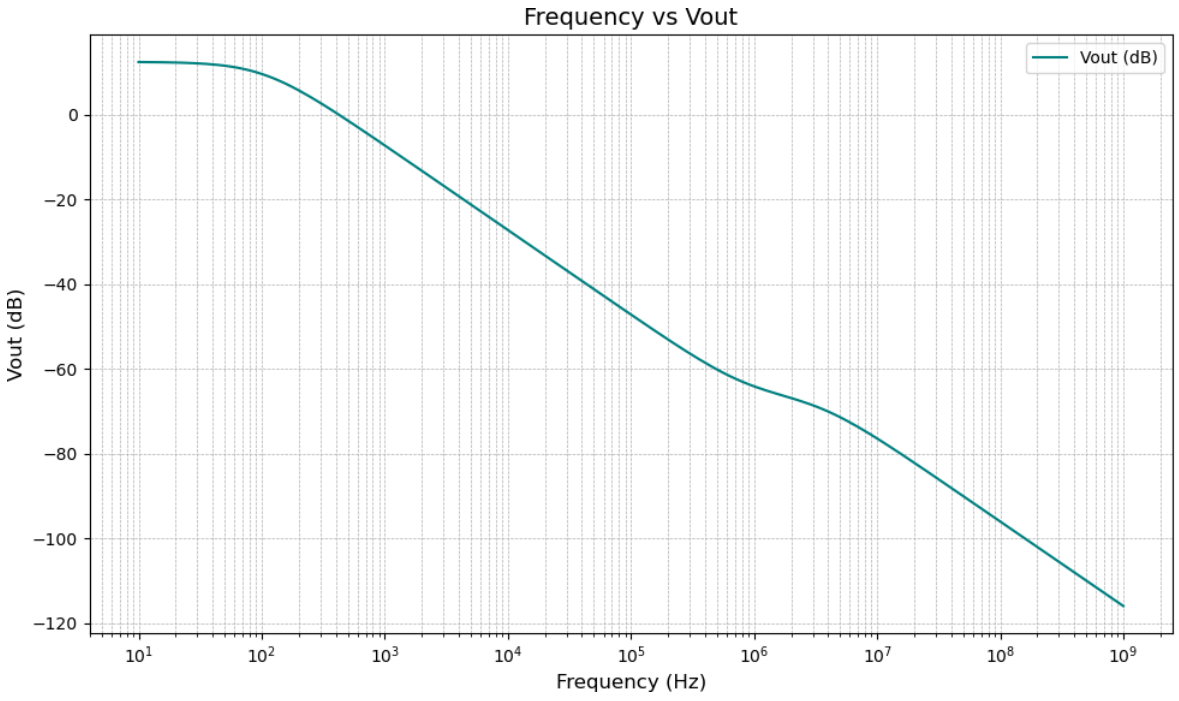


Figure 19: Output on Python

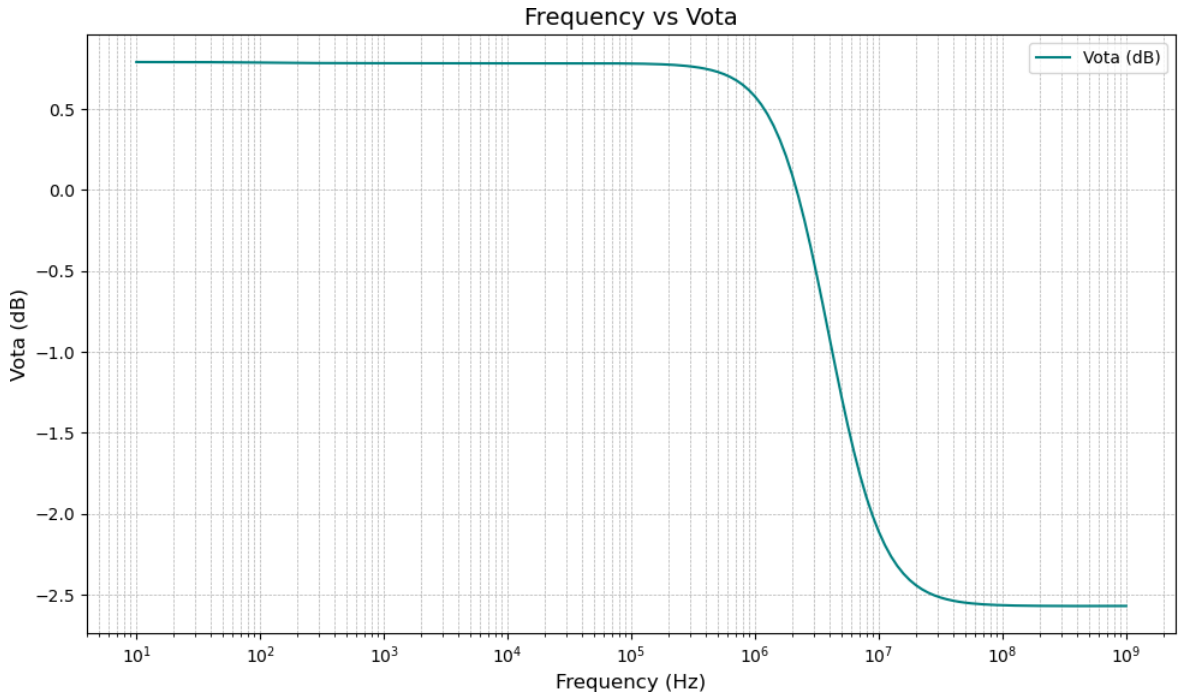


Figure 20: Vouta vs freq

Case 3:- Closed loop PSRR calculation

Schematic

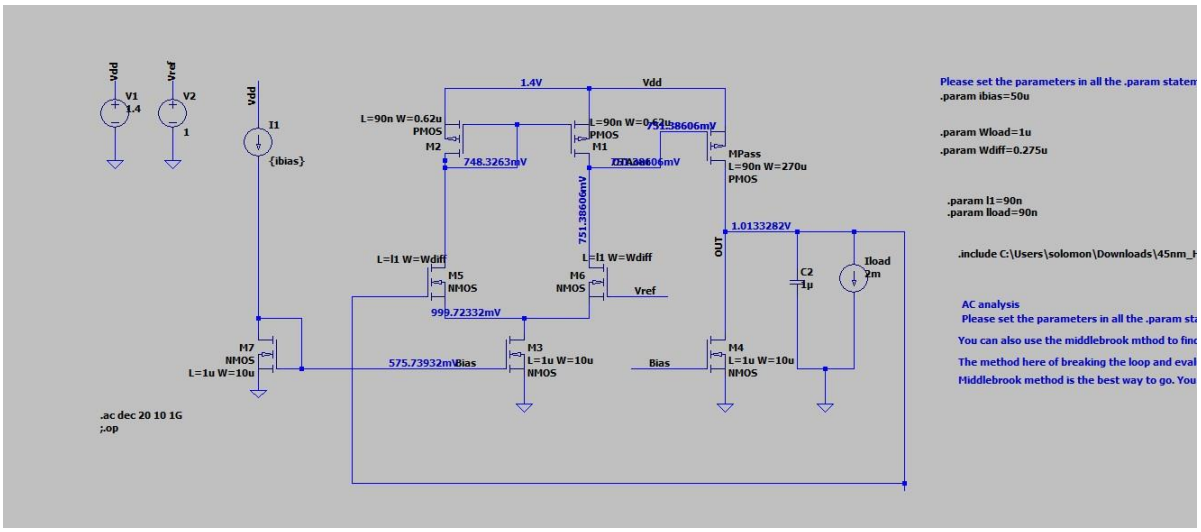


Figure 21: Schematic

Output on Python:-

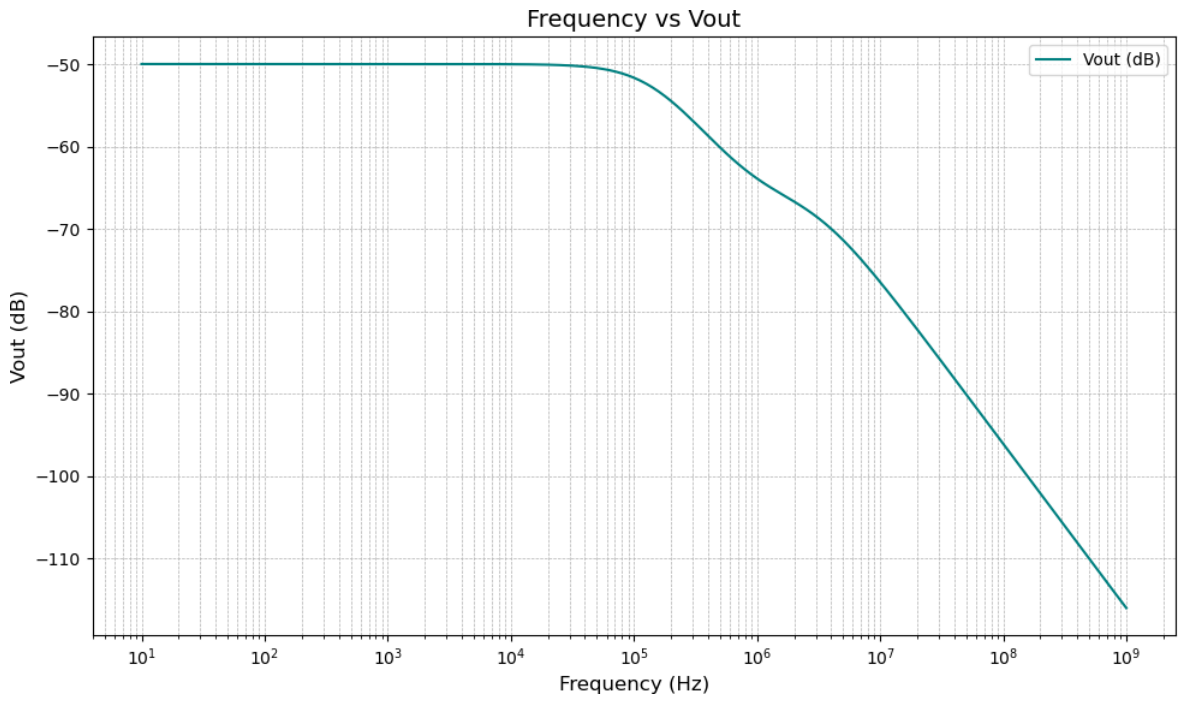


Figure 22: Output on Python

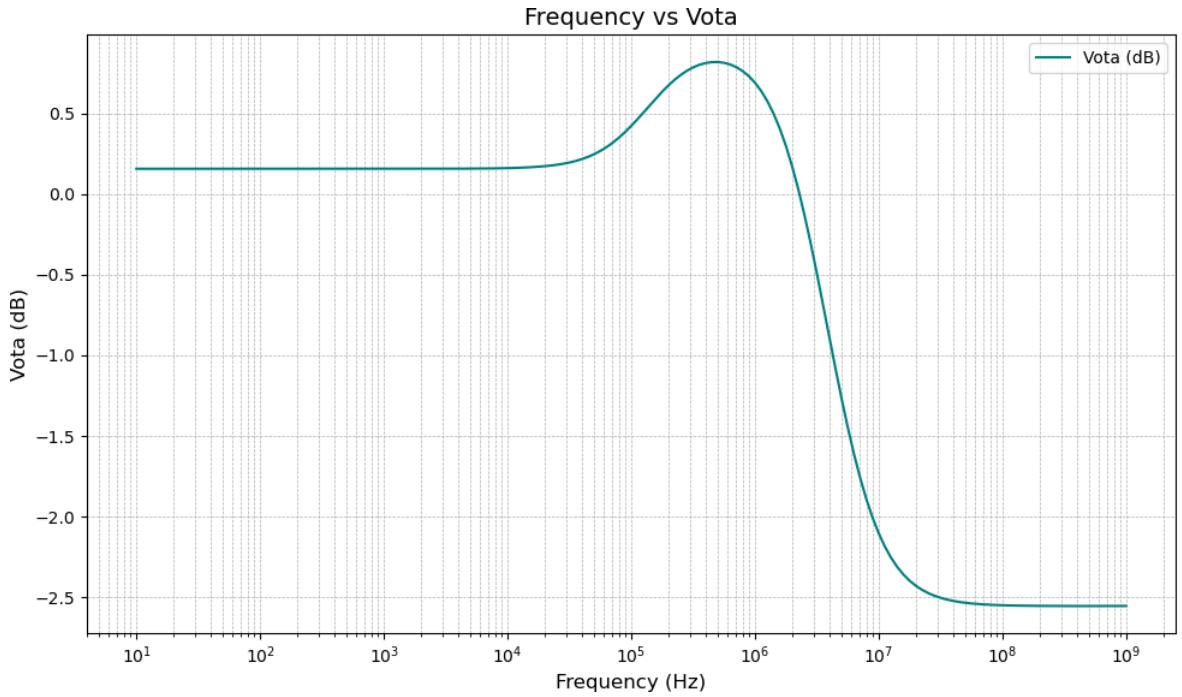


Figure 23: Vouta vs freq

8. Transient Simulation Results

Schematic:-

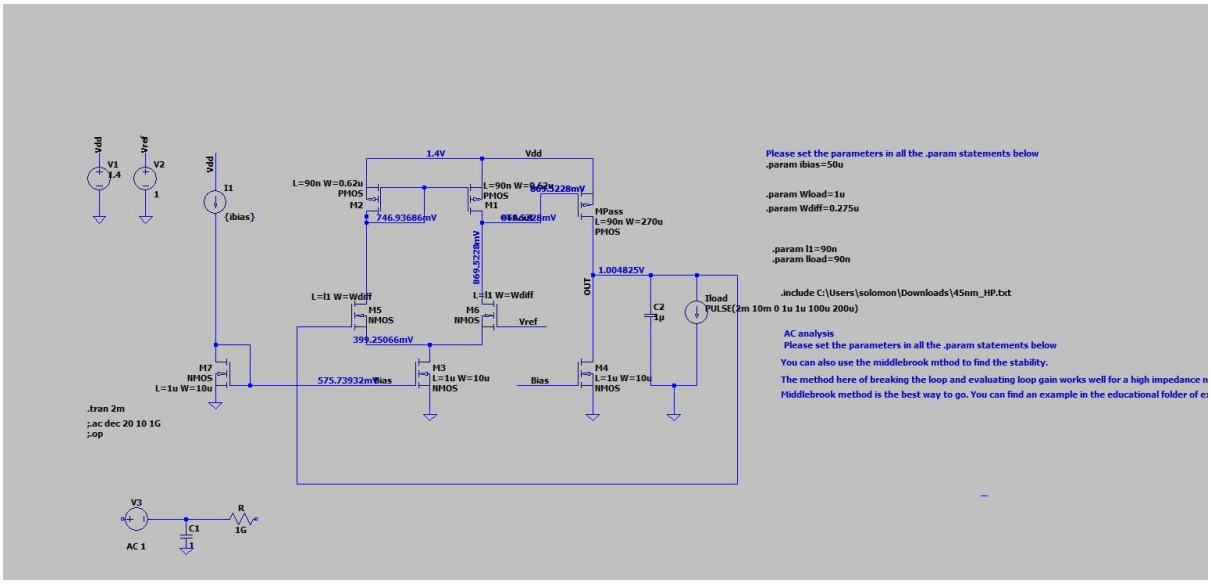


Figure 24: Schematic

Output on Python:-

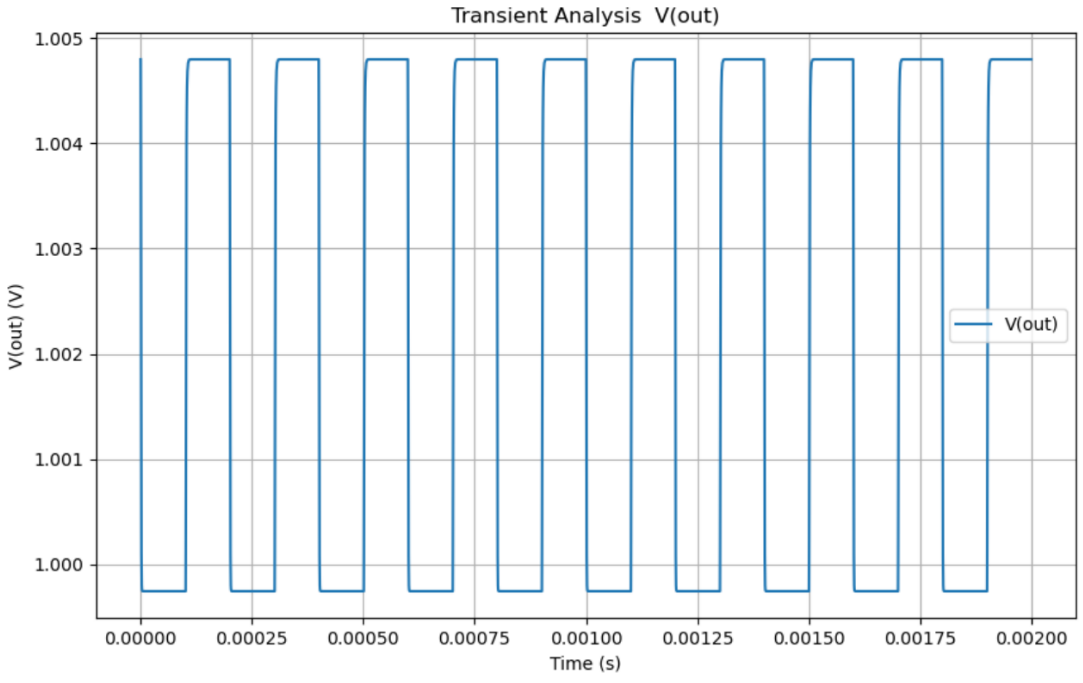


Figure 25: Vout vs time

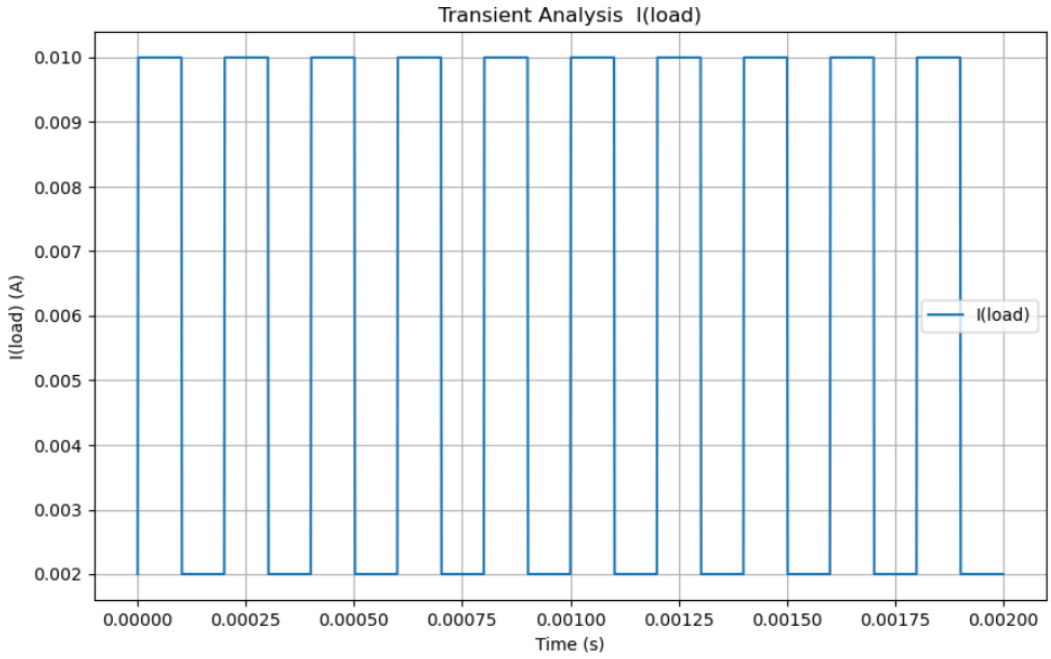


Figure 26: Iout vs time

9. Simulation vs. Hand Calculations

For Passfet

Hand Calculation

- r_o = 500 Ω
- g_m = 0.1 A/V
- W_{p1} (first pole location) = 2k
- $g_m r_o$ = 50

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds}$ = 406.5 Ω
- g_m = 0.0991 A/V
- W_{p1} (first pole location) = 2.46k
- $g_m r_o$ = 40.28

Table 5: Simulation vs. Hand Calculations with Percentage Error

Parameter	Simulation	Hand-Calculation	% Error
ro (Ohm)	406.5	500	18.69%
gm (A/V)	0.0991	0.1000	0.9%
Wp1 (Hz)	2.6k	2k	22.9%
gmro	40.28	50	19.43%

2.Internally Compensated LDO

PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Light Load (2ma)

Schematic

Case 1:- Loop gain analysis:-

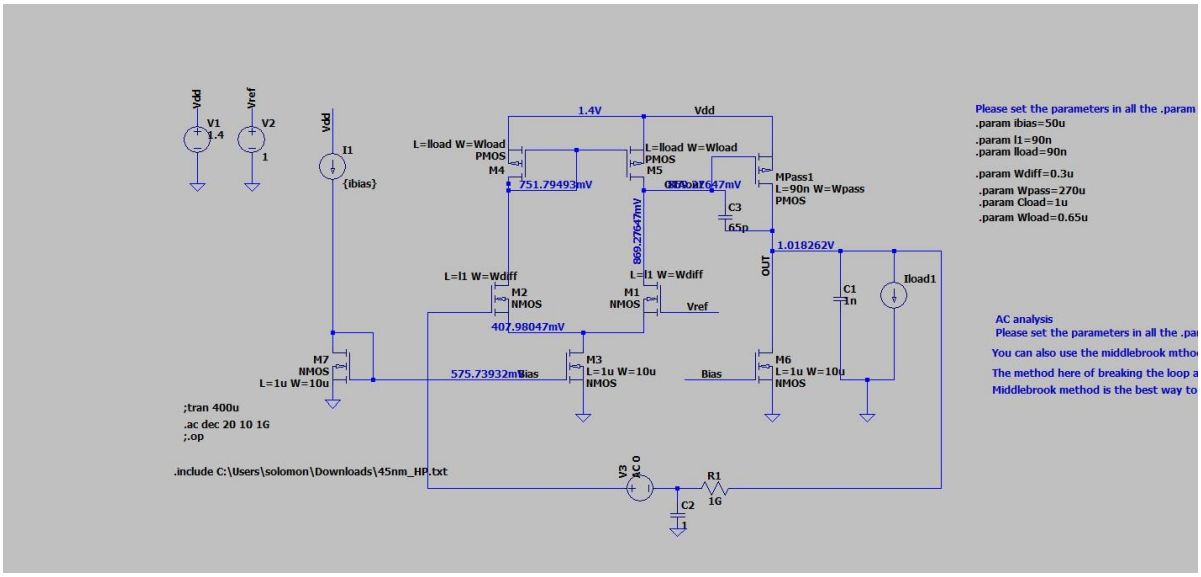


Figure 27: Schematic

Explanation of the artifact used:-

Output Log File:-

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\solomon\Downloads\internal_open.asc
Start Time: Sat Dec  7 01:08:28 2024
solver = Normal
Maximum thread count: 4
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                         --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m6           m7
Model:     nmos         nmos         nmos         nmos         nmos
Id:      2.46e-05     2.51e-05     4.97e-05     5.06e-05     5.00e-05
Vgs:     5.92e-01     5.97e-01     5.76e-01     5.76e-01     5.76e-01
Vds:     4.61e-01     3.44e-01     4.08e-01     1.02e+00     5.76e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.65e-01     4.66e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.38e-01     1.40e-01     1.33e-01     1.33e-01     1.33e-01
Gm:      2.52e-04     2.53e-04     6.25e-04     6.34e-04     6.28e-04
Gds:     4.42e-06     5.34e-06     1.92e-06     1.35e-06     1.54e-06
Gmb      5.79e-05     5.82e-05     1.44e-04     1.46e-04     1.44e-04
Cbd:     1.32e-16     1.36e-16     4.47e-15     3.97e-15     4.30e-15
Cbs:     2.40e-16     2.40e-16     8.00e-15     8.00e-15     8.00e-15

Name:       m4           m5        mpass1
Model:     pmos         pmos         pmos
Id:     -2.51e-05    -2.45e-05    -2.05e-03
Vgs:    -6.48e-01    -6.48e-01    -5.31e-01
Vds:    -6.48e-01    -5.31e-01    -3.82e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.84e-01    -4.85e-01    -4.87e-01
Vdsat:  -1.79e-01    -1.78e-01    -9.46e-02
Gm:      2.46e-04     2.42e-04     3.59e-02
Gds:     4.99e-06     5.19e-06     6.60e-04
Gmb      5.22e-05     5.13e-05     7.41e-03
Cbd:     2.76e-16     2.82e-16     1.21e-13
Cbs:     5.20e-16     5.20e-16     2.16e-13


Total elapsed time: 0.136 seconds.
```

Figure 28: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Device Name	Device Type	|Vds|	|Vgs|	|Vt|	|Vgs|-|Vt|	Reason for saturation
Mpass1	pmos	3.82E-01	5.31E-01	4.87E-01	4.40E-02	|Vsd|>|Vgs|-|Vt|
M1	pmos	4.61E-01	5.92E-01	4.65E-01	1.27E-01	|Vsd|>|Vgs|-|Vt|
M2	pmos	3.44E-01	5.97E-01	4.66E-01	1.31E-01	|Vsd|>|Vgs|-|Vt|
M3	nmos	4.08E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M4	pmos	6.48E-01	6.48E-01	4.84E-01	1.64E-01	|Vsd|>|Vgs|-|Vt|
M5	pmos	5.31E-01	6.48E-01	4.85E-01	1.63E-01	|Vsd|>|Vgs|-|Vt|
M6	nmos	1.02E+00	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M7	nmos	5.76E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|

Output on Python:-

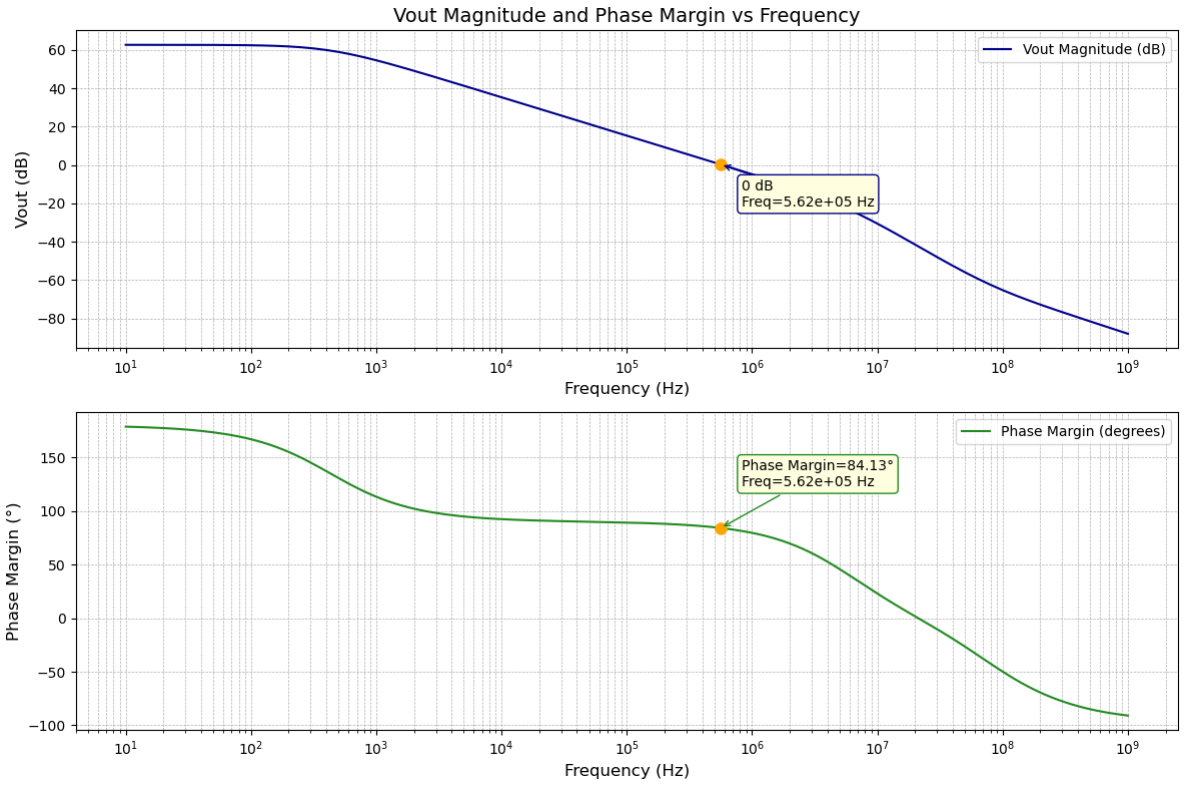


Figure 29: Output on Python

Case 2:- Open Loop PSRR calculation

Schematic

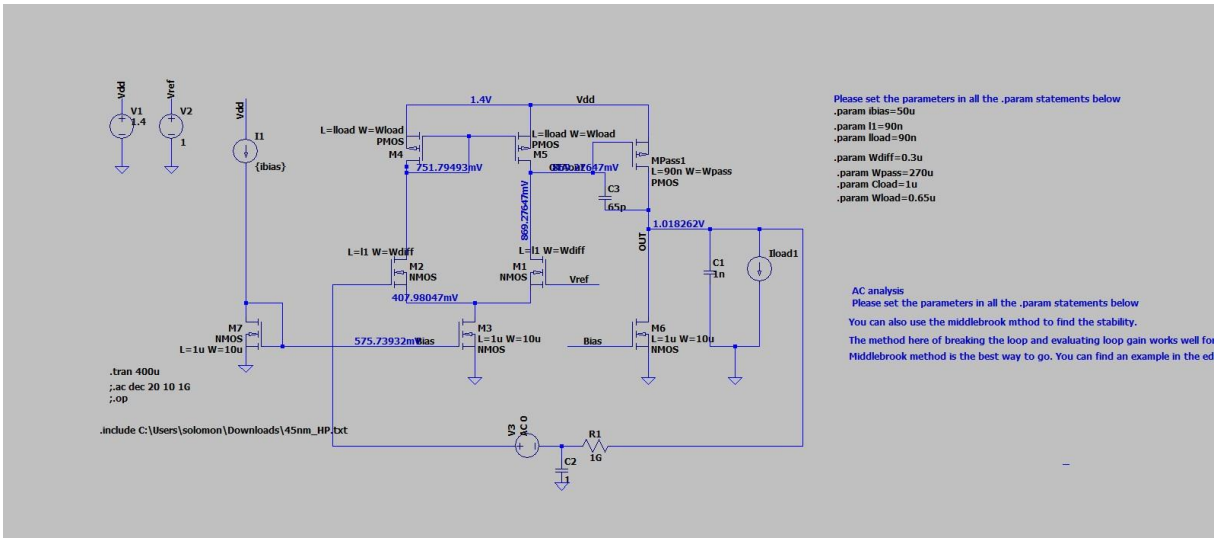


Figure 30: Schematic

Output on Python:-

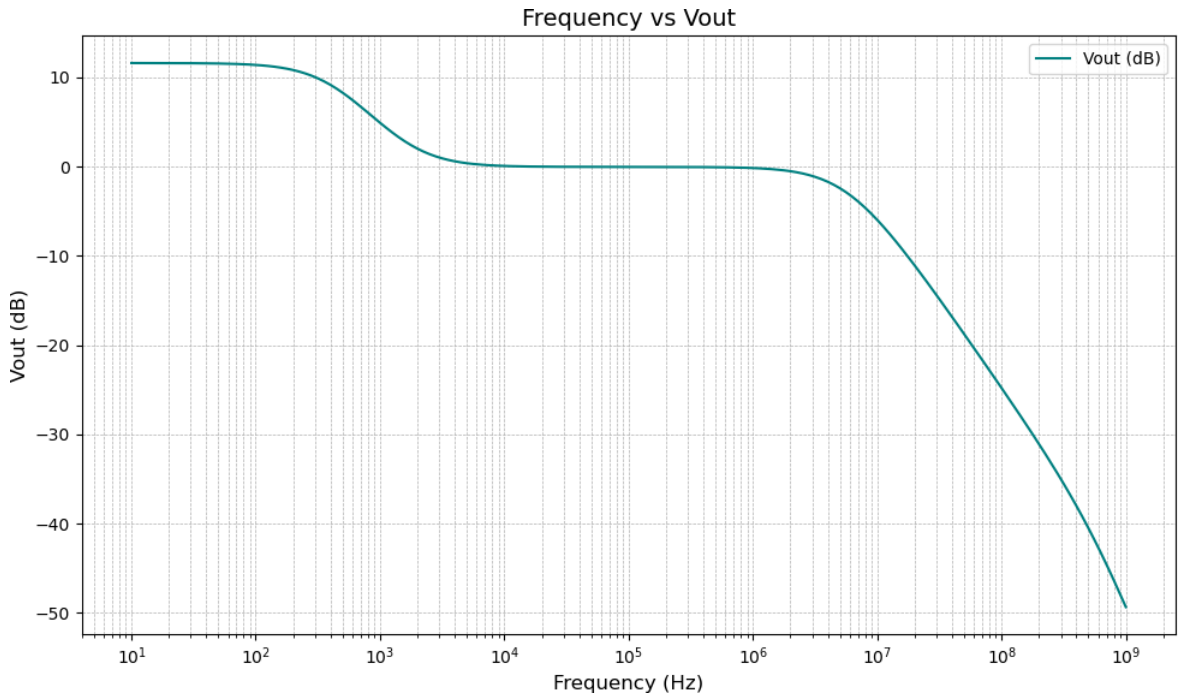


Figure 31: Output on Python

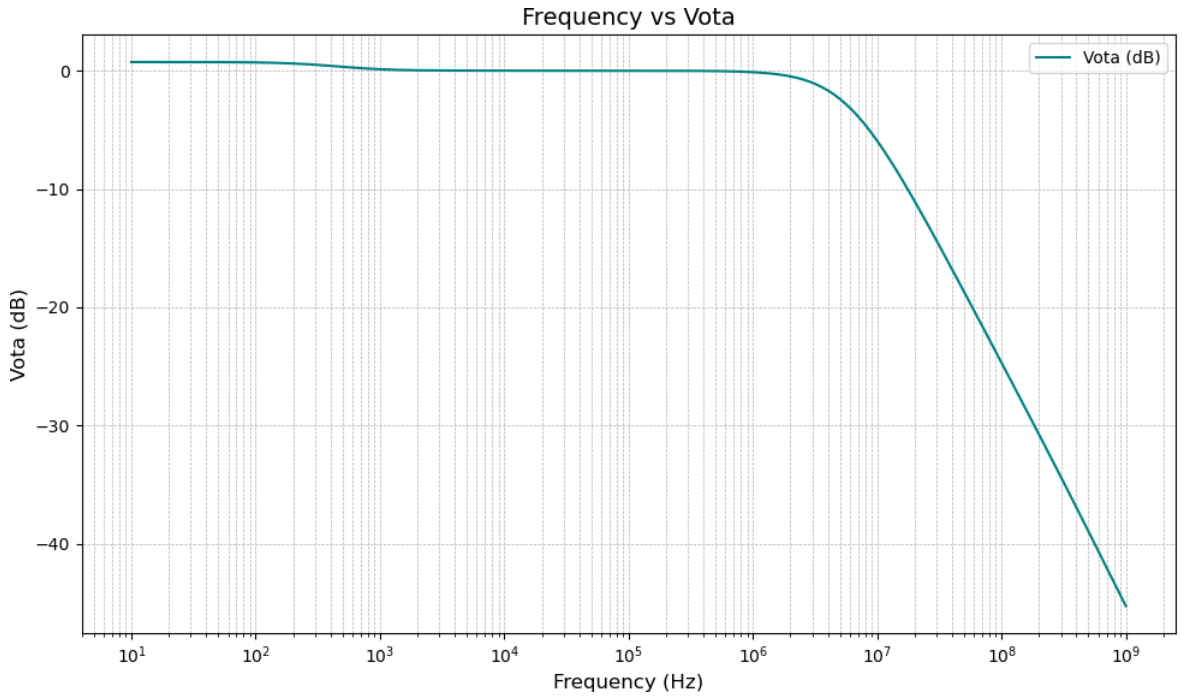


Figure 32: VoutA vs freq

Case 3:- Closed loop PSRR calculation

Schematic

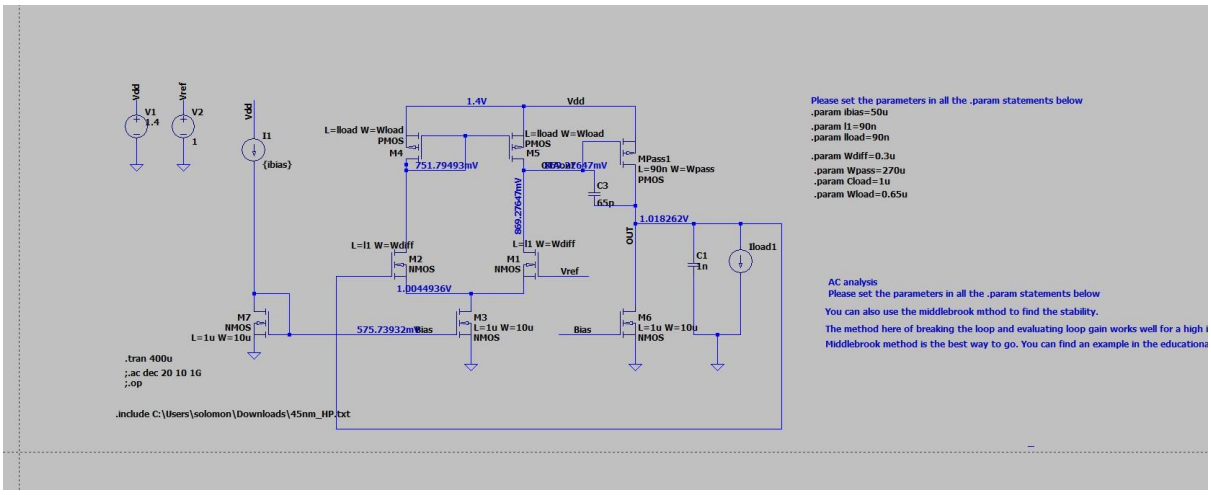


Figure 33: Schematic

Output on Python:-

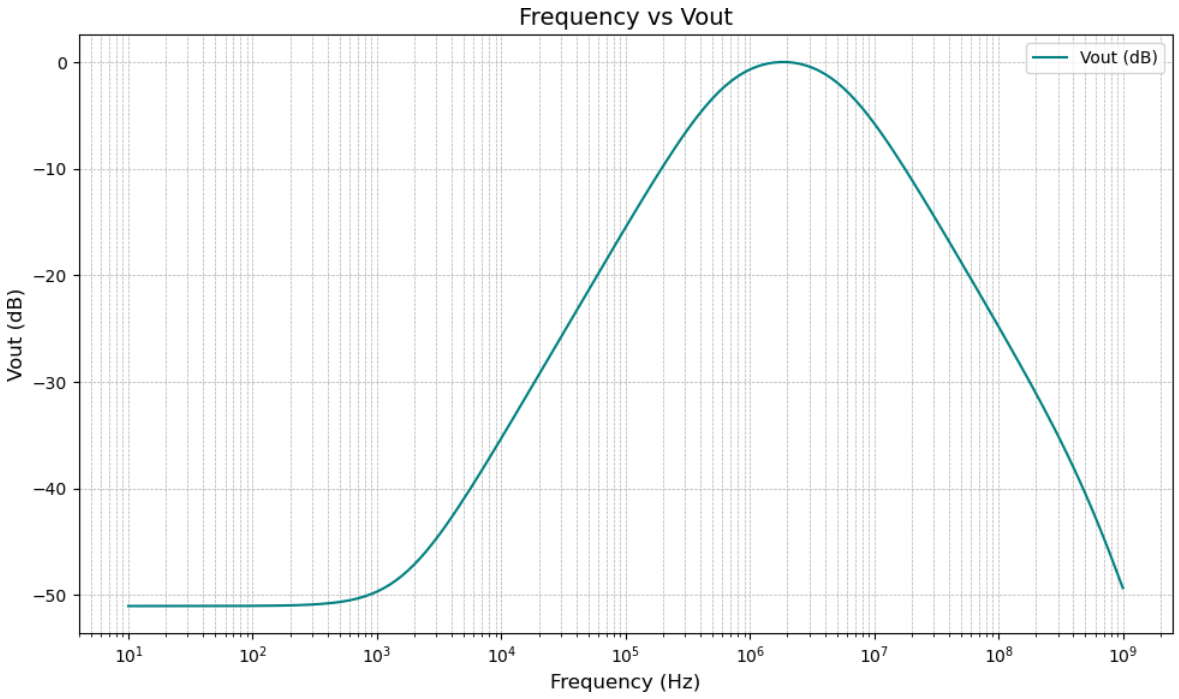


Figure 34: Output on Python

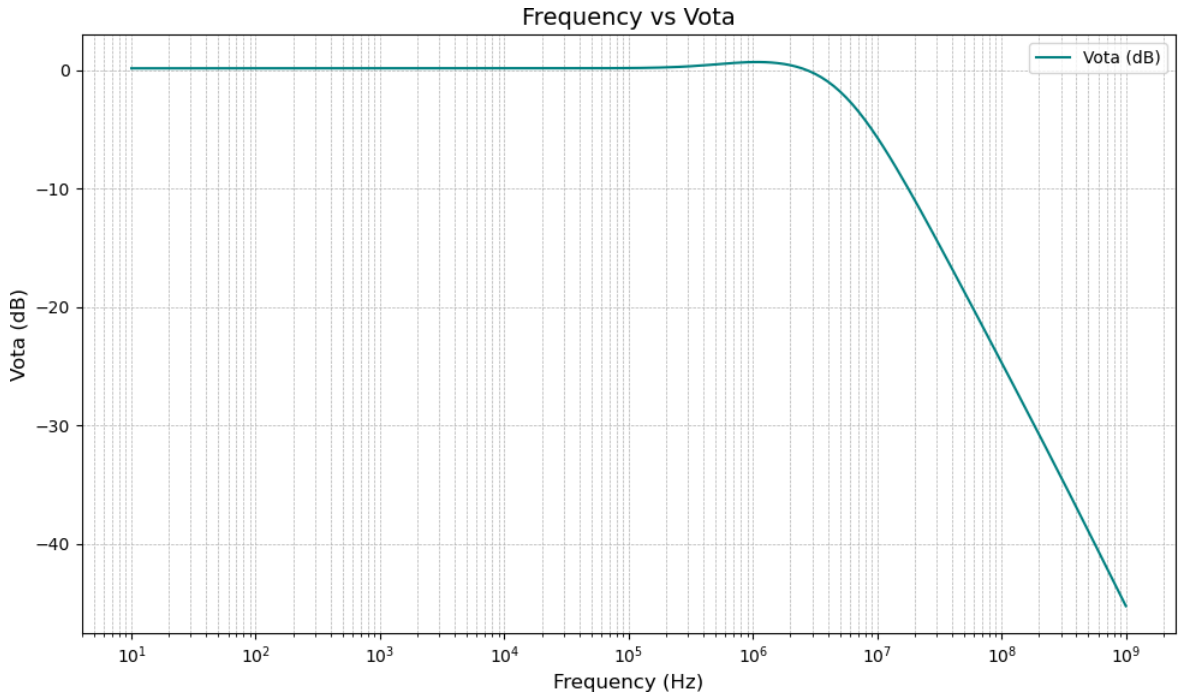


Figure 35: VoutA vs freq

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

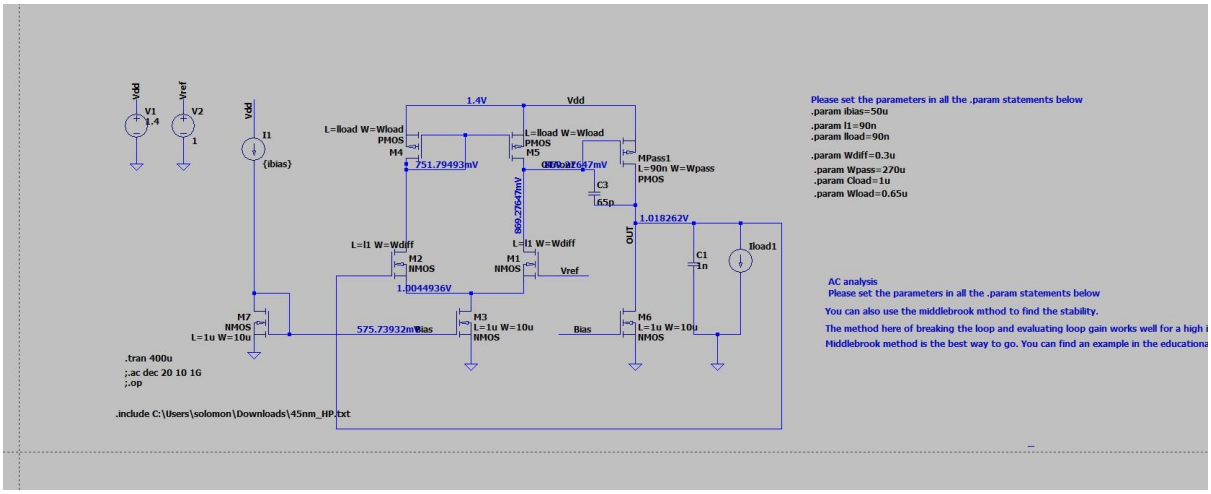


Figure 36: Schematic

Explanation of the artifact used:-

Output Log File:-

SPICE Output Log: C:\Users\solomon\Downloads\internal_open.log

```
LTspice 24.0.12 for Windows
Circuit: * C:\Users\solomon\Downloads\internal_open.asc
Start Time: Sat Dec  7 01:29:01 2024
Solver = Normal
Maximum thread count: 4
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                          --- BSIM4 MOSFETS ---
Name:       m1           m2           m3           m6           m7
Model:     nmos         nmos         nmos         nmos         nmos
Id:      2.49e-05     2.48e-05     4.97e-05     5.06e-05     5.00e-05
Vgs:     5.95e-01     5.95e-01     5.76e-01     5.76e-01     5.76e-01
Vds:     3.47e-01     3.49e-01     4.05e-01     1.00e+00     5.76e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00     0.00e+00     0.00e+00
Vth:     4.66e-01     4.66e-01     4.69e-01     4.69e-01     4.69e-01
Vdsat:   1.39e-01     1.39e-01     1.33e-01     1.33e-01     1.33e-01
Gm:      2.52e-04     2.51e-04     6.25e-04     6.34e-04     6.28e-04
Gds:     5.25e-06     5.21e-06     1.94e-06     1.35e-06     1.54e-06
Gmb      5.80e-05     5.78e-05     1.44e-04     1.46e-04     1.44e-04
Cbd:     1.36e-16     1.36e-16     4.47e-15     3.98e-15     4.30e-15
Cbs:     2.40e-16     2.40e-16     8.00e-15     8.00e-15     8.00e-15

Name:       m4           m5        mpass1
Model:     pmos         pmos         pmos
Id:     -2.48e-05    -2.48e-05    -1.01e-02
Vgs:    -6.47e-01    -6.47e-01    -6.48e-01
Vds:    -6.47e-01    -6.48e-01    -4.00e-01
Vbs:     0.00e+00     0.00e+00     0.00e+00
Vth:    -4.84e-01    -4.84e-01    -4.87e-01
Vdsat:  -1.78e-01    -1.78e-01    -1.77e-01
Gm:      2.45e-04     2.45e-04     9.97e-02
Gds:     4.95e-06     4.95e-06     2.46e-03
Gmb      5.18e-05     5.18e-05     2.11e-02
Cbd:     2.76e-16     2.76e-16     1.21e-13
Cbs:     5.20e-16     5.20e-16     2.16e-13


Total elapsed time: 0.277 seconds.
```

Figure 37: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Device Name	Device Type	|Vds|	|Vgs|	|Vt|	|Vgs|-|Vt|	Reason for saturation
Mpass1	pmos	4.00E-01	6.48E-01	4.87E-01	1.61E-01	|Vsd|>|Vgs|-|Vt|
M1	pmos	3.47E-01	5.95E-01	4.66E-01	1.29E-01	|Vsd|>|Vgs|-|Vt|
M2	pmos	3.49E-01	5.95E-01	4.66E-01	1.29E-01	|Vsd|>|Vgs|-|Vt|
M3	nmos	4.05E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M4	pmos	6.47E-01	6.47E-01	4.84E-01	1.63E-01	|Vsd|>|Vgs|-|Vt|
M5	pmos	6.48E-01	6.47E-01	4.84E-01	1.63E-01	|Vsd|>|Vgs|-|Vt|
M6	nmos	1.00E+00	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|
M7	nmos	5.76E-01	5.76E-01	4.69E-01	1.07E-01	|Vsd|>|Vgs|-|Vt|

Figure 38: Operating region table

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Output on Python:-

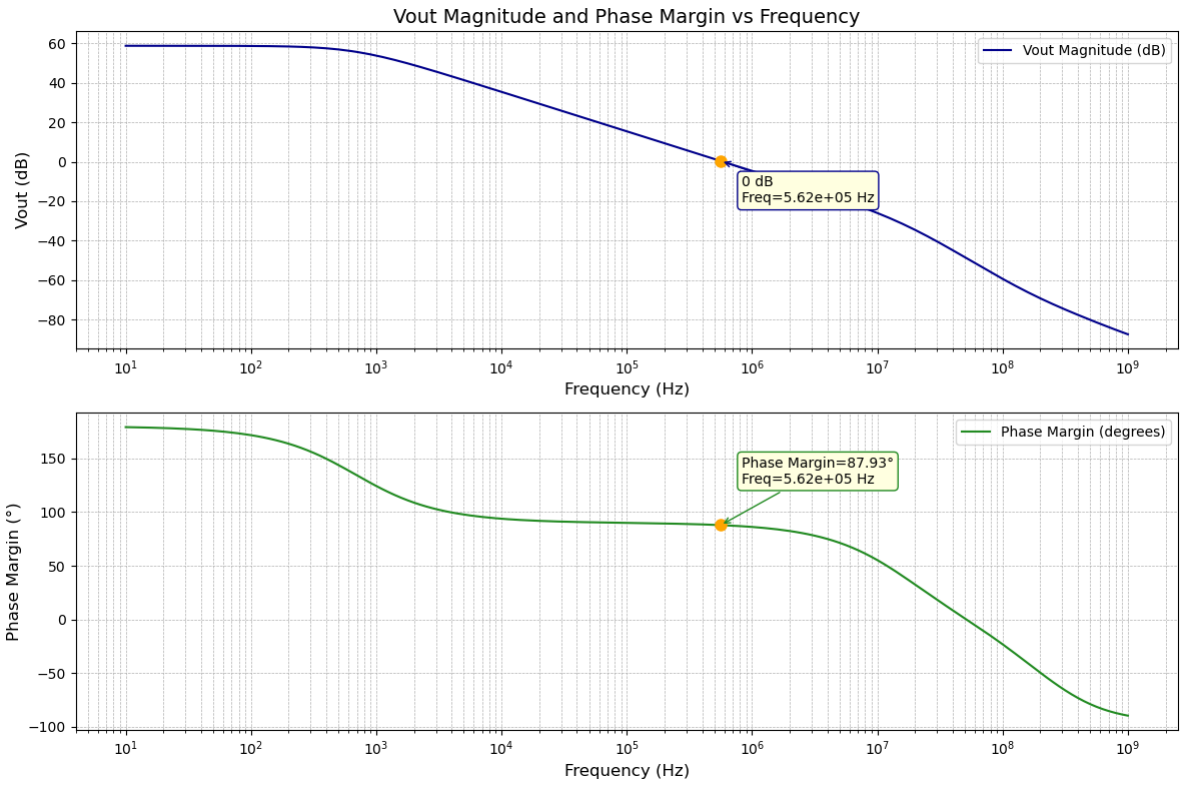


Figure 39: Enter Caption

Figure 40: Output on Python

Case 2:- Open Loop PSRR calculation

Schematic

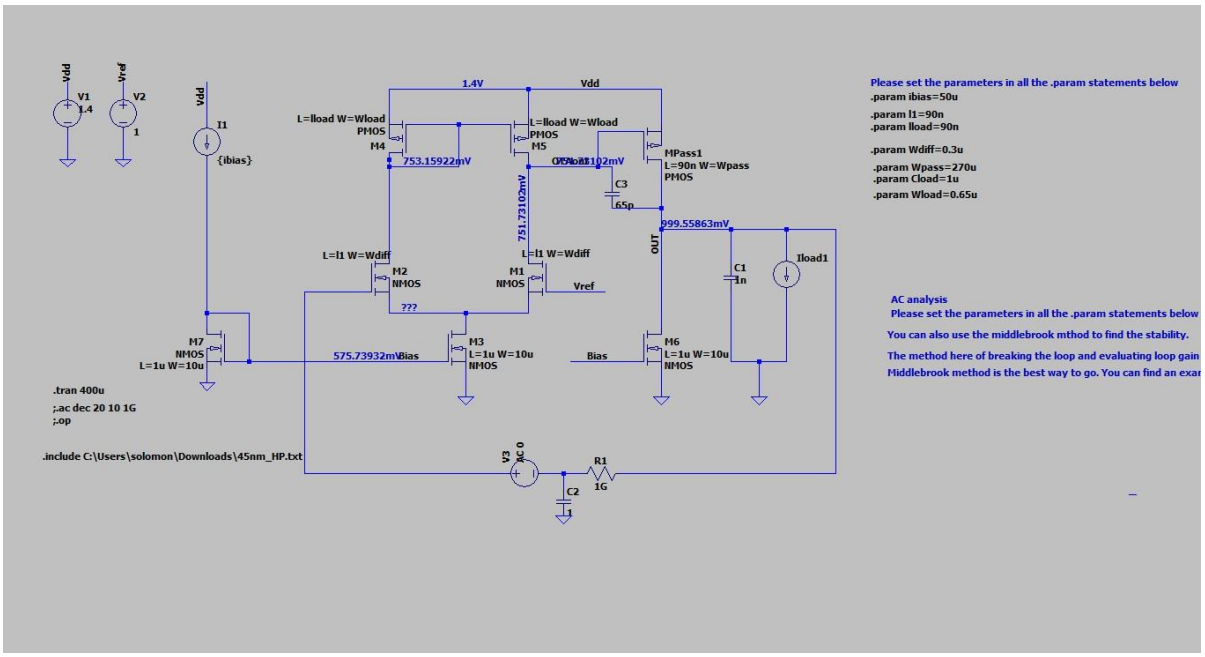


Figure 41: Schematic

Output on Python:-

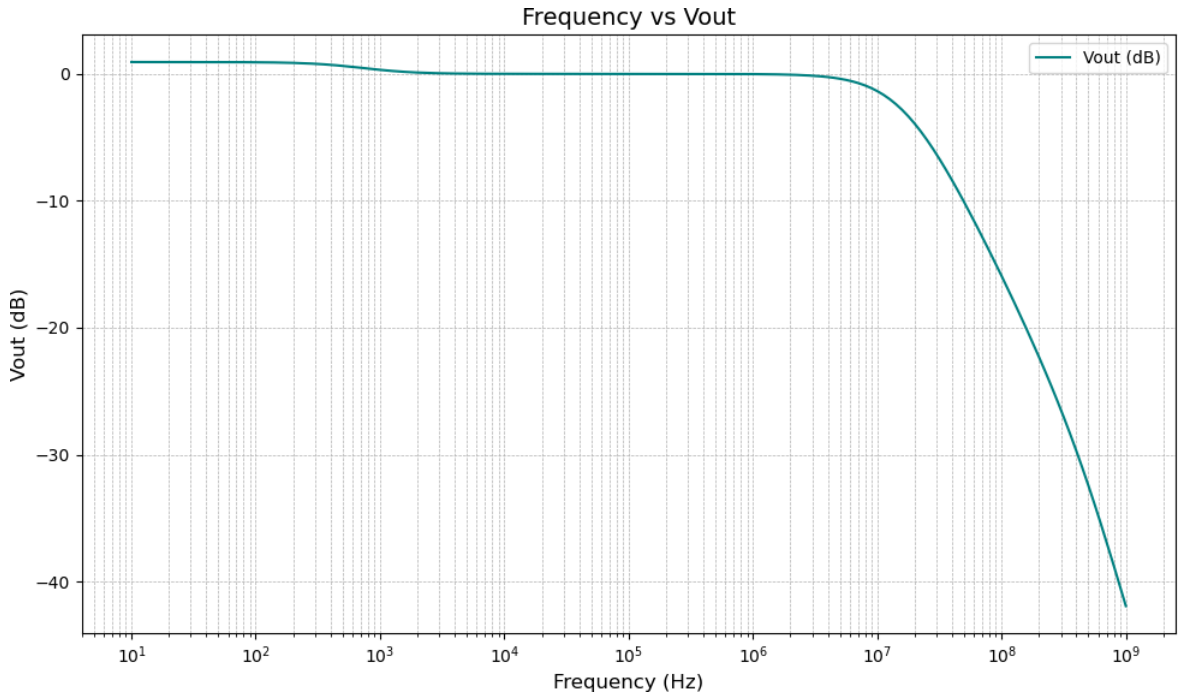


Figure 42: Output on Python

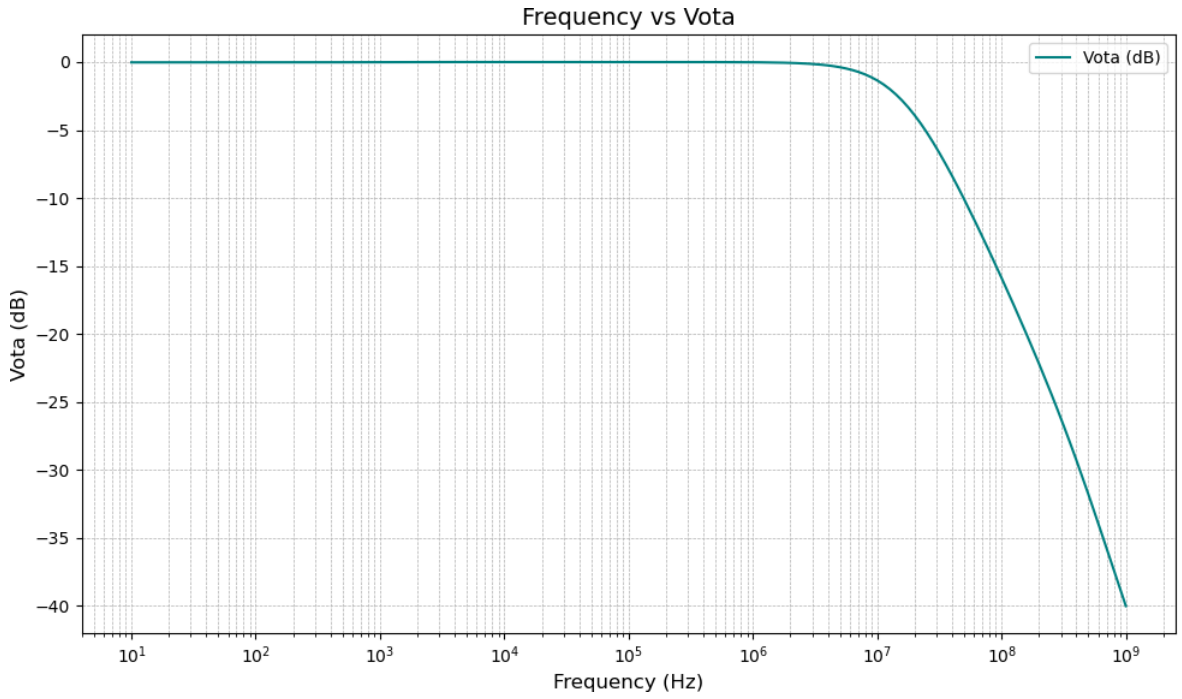


Figure 43: Vouta vs freq

Case 3:- Closed loop PSRR calculation

Schematic

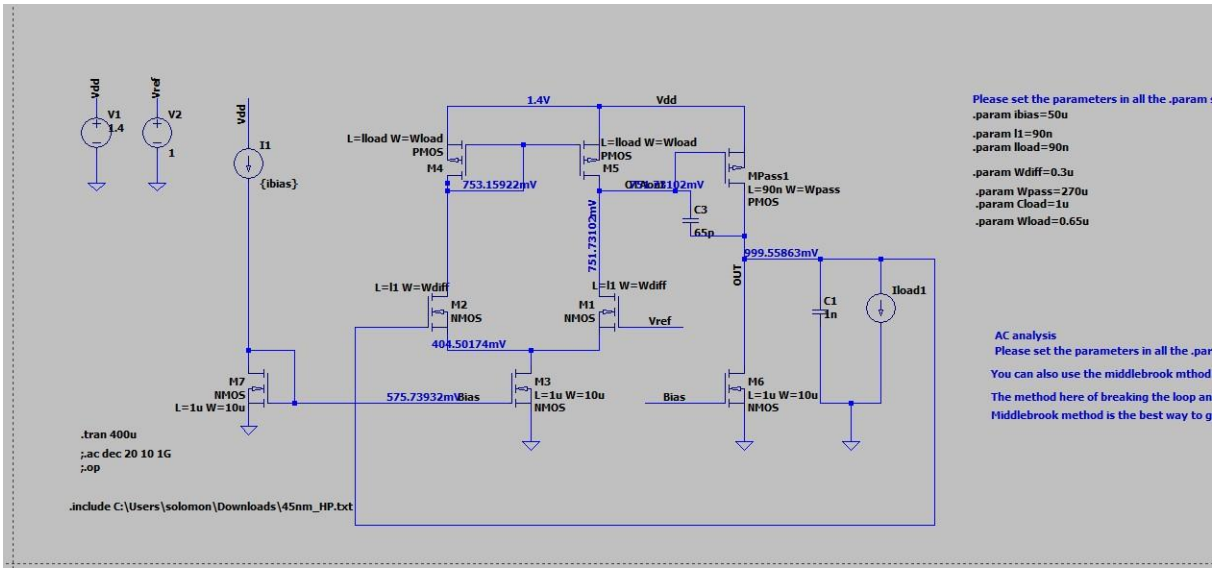


Figure 44: Schematic

Output on Python:-

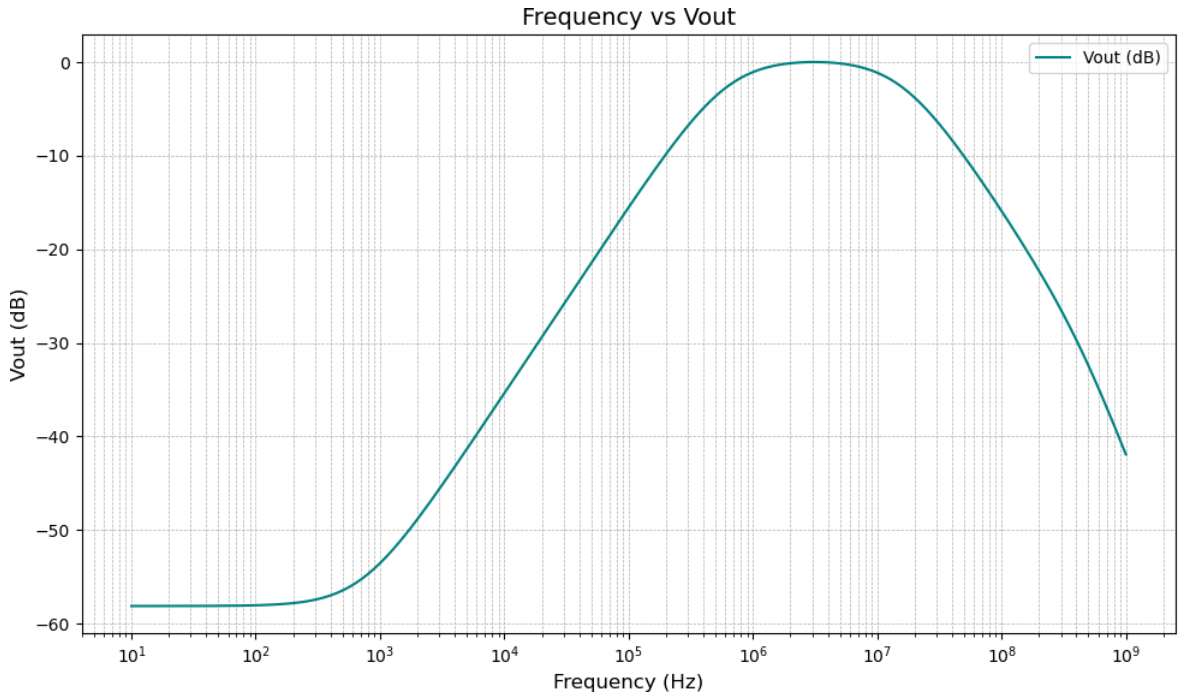


Figure 45: Output on Python

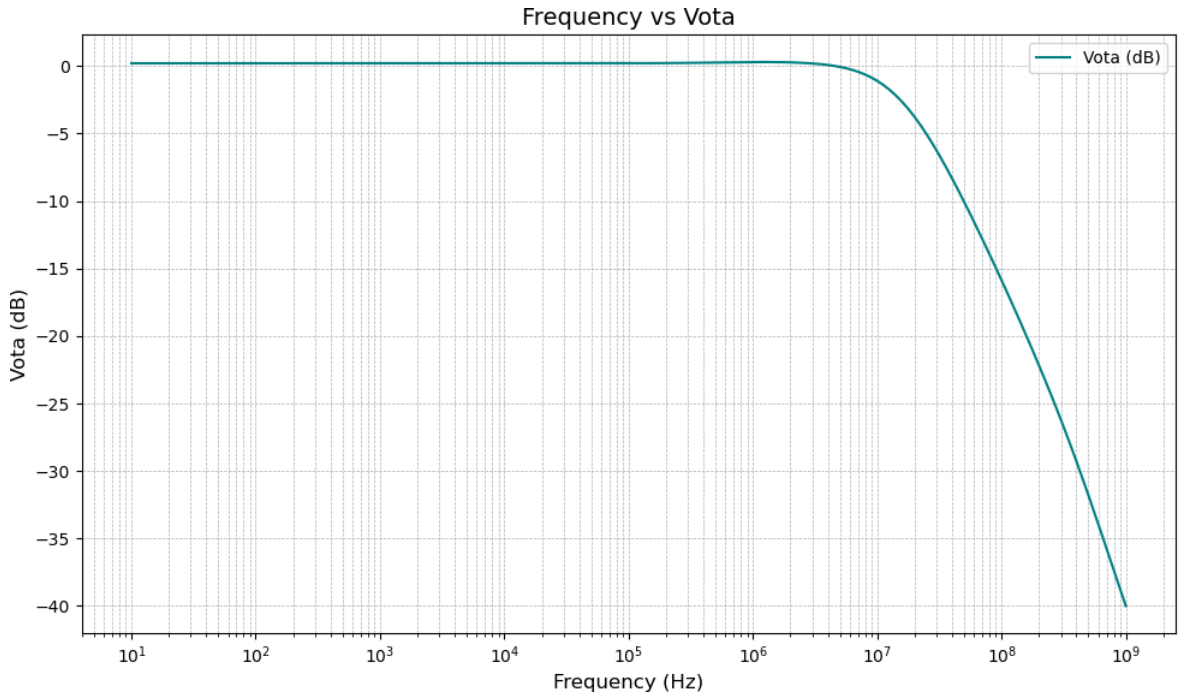


Figure 46: Phase margin

Transient Analysis

Schematic

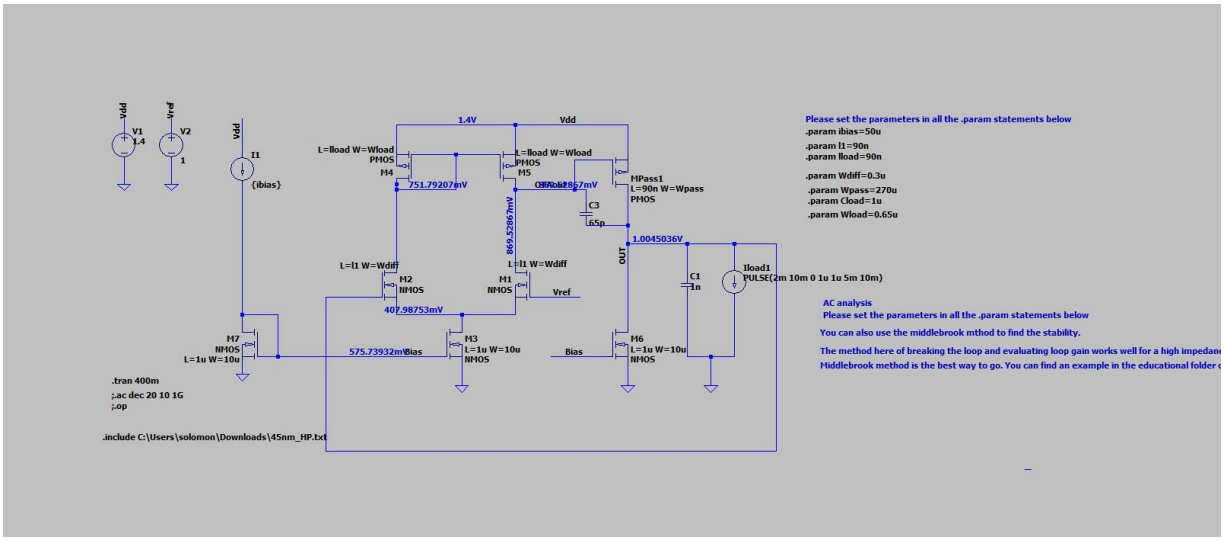


Figure 47: Schematic

Iload Vs Time

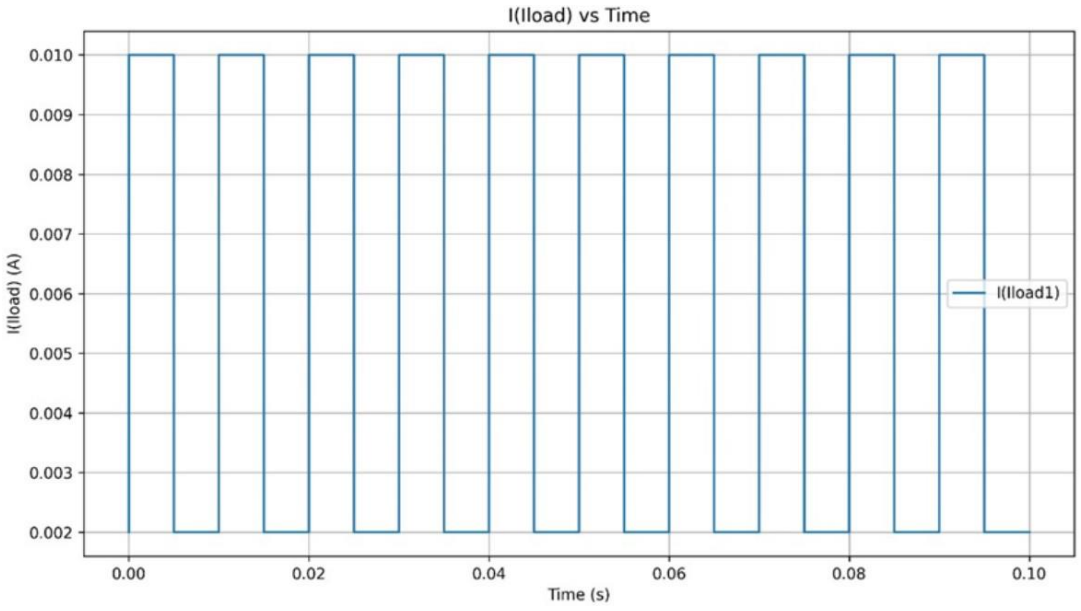


Figure 48: Iload Vs Time

Vout vs Time

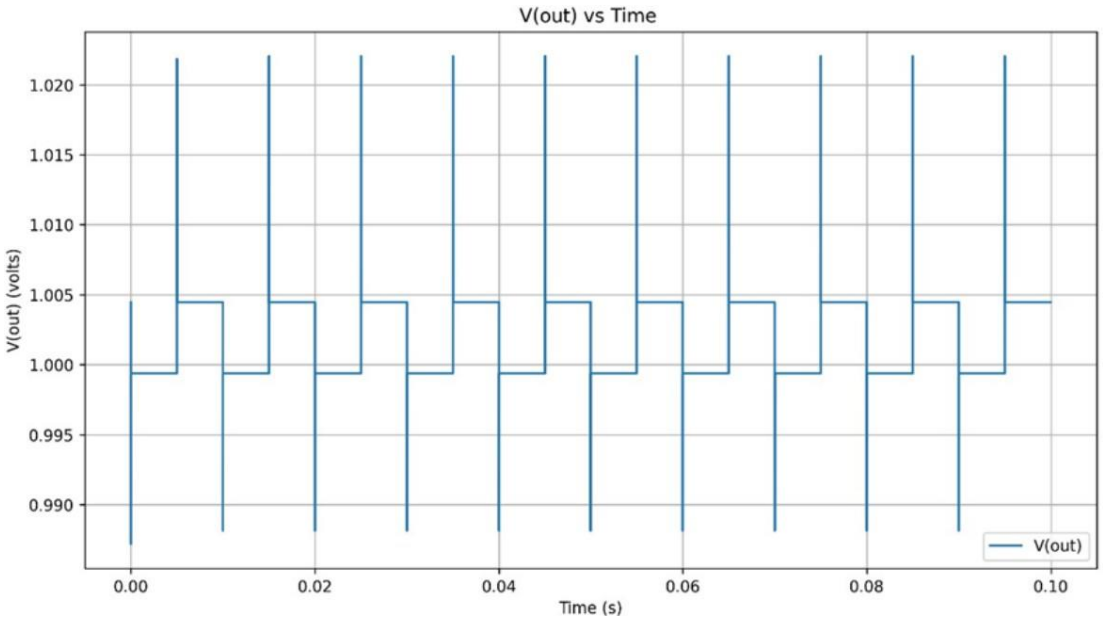


Figure 49: Enter Caption

Figure 50: Vout vs Time

Change this FET Sizes

we Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 6: FET Sizes and Parameters

Transistor	Size (*W/L*)	Gm/id
PassFET pmos	270u/90nn	10
Diff-Amp pmos	65u/90n	10
Diff-Amp nmos	0.3u/90n	10
Current Mirror nmos	10u/1un	10

The value of the capacitance for the internal capcitor is 65pf

Stability Analysis

For Heavy load we get the following curve:

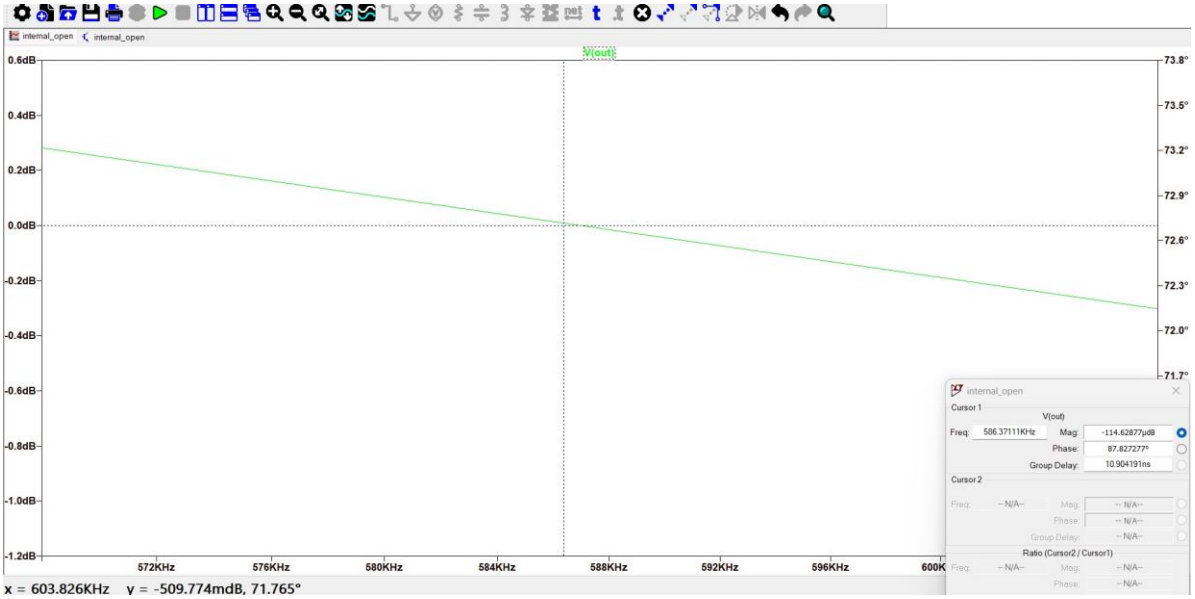


Figure 51: Output on Python

For Light load we get the following curve

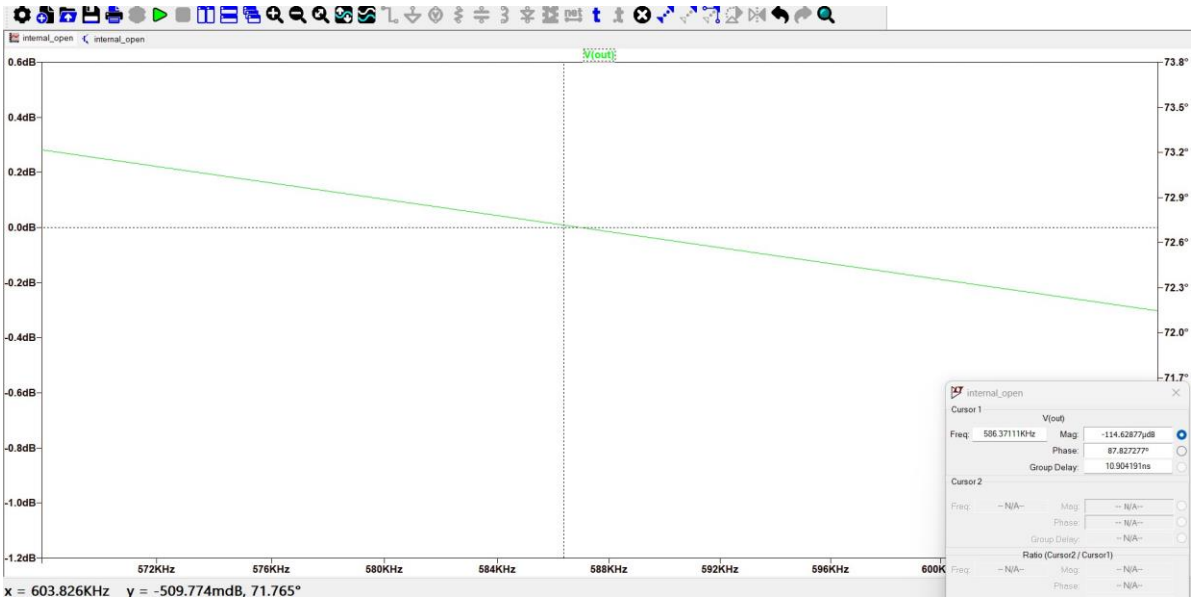


Figure 52: Output on Python

At heavier loads the system is more stable