Project 1: Designing a small standard cell library

(20% of final course grade)

Project Description:

In this project you will work in a team (3 students) to design (schematic and layout) and simulate few CMOS (3.3V) standard cells using Electric VLSI software.

Preparations:

Do not start Project 1 unless you finished Lab 3. For this project use the same design rules and technology files used in Lab 3.

Procedure:

Design (layout and schematic), verify and characterize the following cells:

1. Inverter (sizes: 1, 2, 4 and 8)
2. Tri-state Inverter (sizes: 1, 2, 4 and 8)
3. 3 input NAND gate (sizes: 1, 2 and 4)
4. 3 input NOR gate (sizes: 1, 2 and 4)
5. The complex function: $f(x, y, z, w) = \overline{xy + wz}$ (sizes: 1, 2 and 4)

Rules:

- You need to select the widths of the transistors for each cell to achieve equal rise (t_{pdr}) and fall (t_{pdf}) times (symmetrical cell). *Hint:* You will not be able to design a perfect symmetrical cell.
- Size 1 cell has, in the worst case, the same pull-up and pull-down resistances of the smallest inverter.
- Size n cell transistors have n times the widths of those of Size 1.
- For a standard cell library, every cell should have a width which is multiple of a standard unit, we call this unit "site", in our project the site width is 4λ.
- You need to obtain t_{pdr} and t_{pdf} for each cell using spice simulation. t_{pdr} and t_{pdf} should be obtained for different loads C_{inv}, $2C_{inv}$, $4C_{inv}$ and $8C_{inv}$. Also, you need to use different transition times (Here the transition time is defined as the time needed for the signal to go from 20% to 80% of its final value): 0 ps, 100 ps, 400 ps and 800 ps (In total there will be 32 simulations per cell; 16 for t_{pdr} and 16 for t_{pdf}).

- Derive the Linear delay model for each cell: $delay = k_1 \times C_{load} + k_2 \times Transition + k_3$; k_1, k_2 and k_3 are constants
- The gates layout should follow the standard cell layout guidelines mentioned in the lectures (for example, all the gates should have the same height). Also, the layout should be DRC and LVS clean. The height of the cell should be as minimum as possible. The team that designs the shortest cells will receive a bonus of 10% of the project's grade.

Deliverables:

- Stick diagrams for all cells
- Your estimation for the cell's height
- The layout of at least one size for each function
- Electric VLSI library that contains the schematic and the layout for the gates
- Spice Decks used to obtain t_{pdr} and t_{pdf}
- At least 12 pages (plus the cover) report in **Latex** to outline the design experience and to report the collected data. Also, it should show the derived linear delay models. The report has to show your work to determine the cell height as well as the stick diagrams used for the layout. *Reports written in any software* ***other than Latex will NOT be accepted.***
- All data plots **must** be done in **R or Python**. *Plots done using* ***any other software (e.g. Matlab or Excel) will NOT be accepted.***
- You have to plan your group work carefully and start as early as possible. The report must indicate the work of each group member. All group members will receive **the same** grade, except if some members did **all** the work or **no work at all**.

Requirements for the Report

To be considered complete, the report must contain the following sections:

1. Cover page, containing course number, course title, project number, and name and IDs of all group members.
2. Table of Contents with page numbers
3. Introduction chapter to explain briefly what the purpose of this project is.
4. The report should be organized such that each chapter is about a given circuit. For example, Chapter 1 would contain all work on the inverter, Chapter 2 would include all work on the Tri-state inverter...etc.

5. Each chapter must have sections underneath highlighting the content. Here is an example:
   Under Chapter 1: Inverter, you would have
   (a) Section 1.1: Schematics
   (b) Section 1.2: Stick Diagrams
   (c) Section 1.3: Layouts (where applicable)
   (d) Section 1.4: Calculating input transition times
   (e) Section 1.5: Data Collection (how you collected and measured all required parameters, including data plots)
   (f) Section 1.6: Obtaining the minimum cell height (what methods you used to reach the minimum cell height in your design, and what that minimum height value is)

   This order will have to be followed throughout the report for the rest of the chapters on the other gates.

For technical help, always consult with your graduate and undergraduate TA's. However, they are NOT going to do your project for you!