

The other possible idea is to instead of construct the graph structure around the module, we can construct the graph structure around the instructions. Opposite to the other idea, I think this might make things easier when making inter module optimizations but make writing the internals of the modules a bit more difficult. I think this approach can prove to be more flexible.

```
1  {
2    "instruction": "ADD"
3    "modules": [
4      {
5        "module": "control",
6        "args": [
7          {
8            "type": "input", "length": 5, "name": "op"
9          },
10         {
11           "type": "output reg", "length": 1, "name": "alu_op"
12         },
13         {
14           "type": "output reg", "length": 1, "name": "alu_src"
15         },
16         {
17           "type": "output reg", "length": 1, "name": "mem_to_reg"
18         },
19         {
20           "type": "output reg", "length": 1, "name": "reg_write"
21         }
22       ],
23       "always": {
24         "trigger": "*",
25         "cases": [
26           {
27             "var": "op",
28             "case": {
29               "val": "`OPCODE_Arith_I",
30               "code": "alu_src = 1'b1;
31                 reg_wrtie = 1'b1;
32                 alu_op = 2'b11;"
33             }
34           }
35         ]
36       }
37     ]
38   }
39 }
```

This can allow us to