National Semiconductor

SC14421 DECT Baseband Processor

General description

The SC14421 is a 3.0 Volt CMOS chip optimized to handle all the audio, signal and data processing needed within a DECT basestation. All processing for one external line is performed on chip including echo cancelling, echo suppression and DTMF tone generation. The SC14421 is equipped with a double ADPCM transcoder and provisions are made to connect a phone hook with an external codec. Also burst mode logic, scrambler/de-scrambler, encryptor/decryptor and CRC logic are included. The SC14421 is designed such that it is compatible with many radio interfaces. Flexible interfacing to-wards most common 8 or 16-bit micro computers with either multiplexed buses or separate address data buses is provided.

Features

- Integrated Transceiver according to ETSI ETS 300 175-2, 175-3 & 175-8 DECT specification

Supply

- 3.0 to 5.5 Volt operating voltage

High Integration

- 2 kByte Data Memory with linear addressing modes
- 2 full duplex ADPCM transcoders
- On-chip 14-bit linear CODEC
- 3 or 4 party conferencing
- Echo Cancelling & suppression
- Echo suppression on two ISDN B channels
- (DTMF) tonegenerator
- Software controlled gain on audio input and output
- On-chip Gaussian filter with programmable amplitude
- RSSI peak hold ADC
- synchronisation port
- ISDN interface formats

Flexibility

- On board dedicated instruction processor
- Operating program stored in RAM for instant changes.
- Flexible programmable DRAM allocation for data storage.
- Eleven programmable control signals for radio front end
- Serial interface to control radio front end circuitry.
- Flexible control of onboard DSP with all algorithm parameters stored in RAM

MAC functionality

- Full support of B-field data formats (D80, D32, D08, D00).
- Protected B-field data format (D32).
- Standard DECT encryption with different keys possible for different MAC-connections.
- 6 MAC connections can be handled simultaneously.
- Seamless handover.

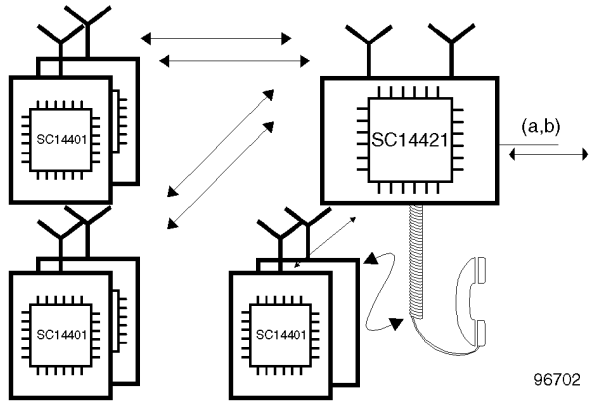


FIGURE 1.

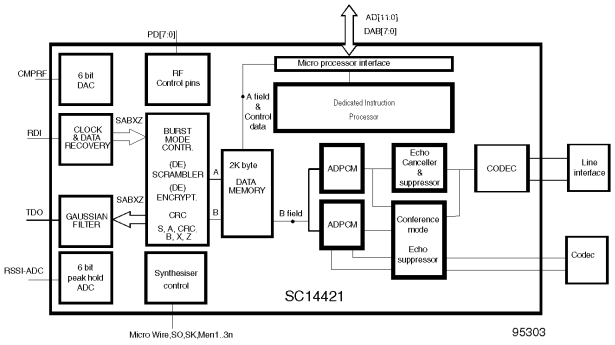


FIGURE 2. Block diagram

Table 1: Pin descriptions

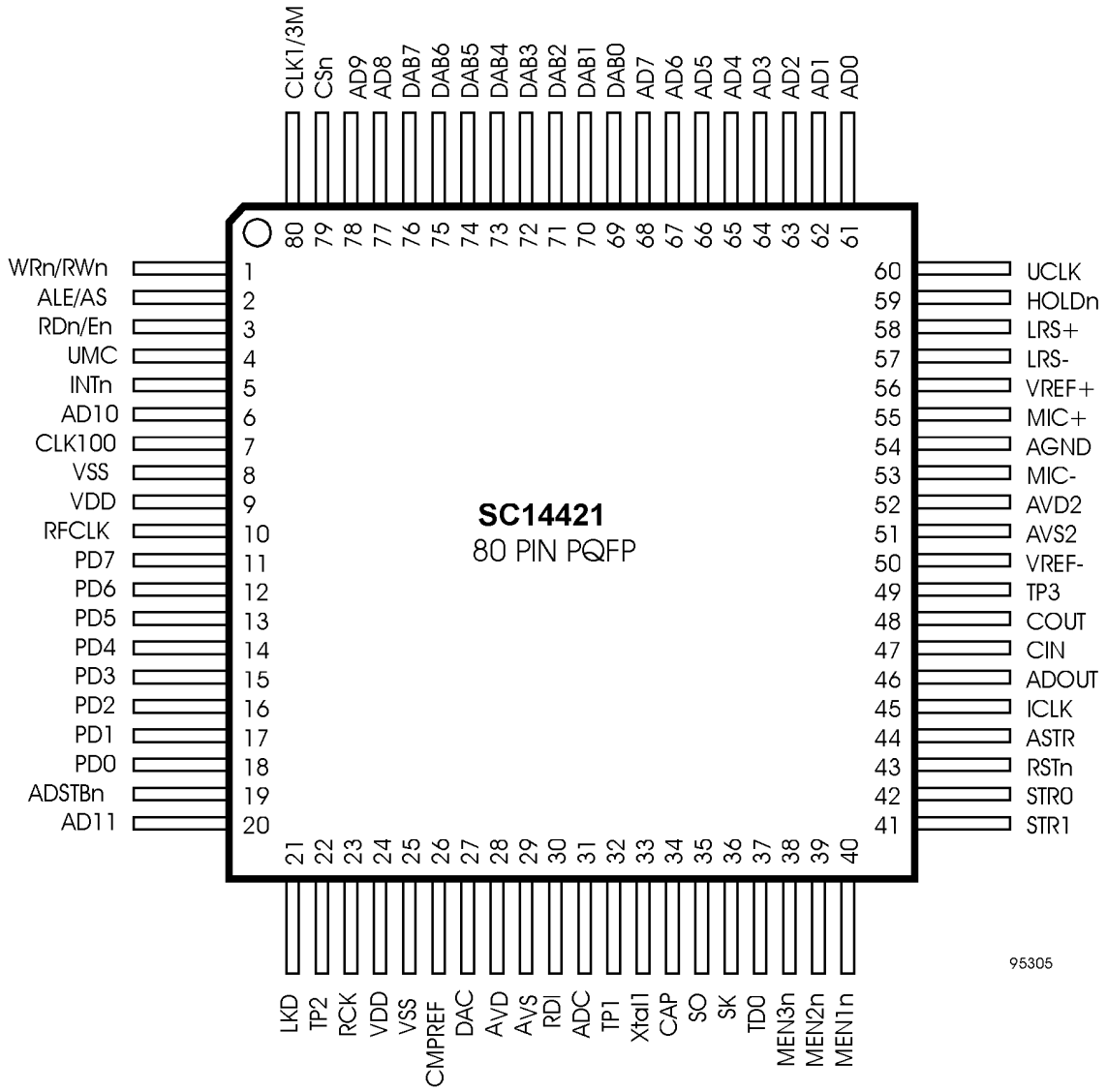
Pin name	Pin number	Description
WRn/RWn	1	INPUT. Active low write signal in case UMC = ‘0’ . Read / Write not in case UMC = ‘1’ .
ALE/AS	2	INPUT. Address Latch Enable in case UMC = ‘0’. Address Strobe in case UMC = ‘1’.
RDn/En	3	INPUT. Active low read in case UMC = ‘0’ . Active low enable when UMC=’1’ .
UMC	4	INPUT. UMC = ‘0’ : Intel style interface, UMC = ‘1’ : Motorola style.
INTn	5	OPEN DRAIN OUTPUT. Interrupt not.
AD[10]	6	INPUT. Address pin 10
CLK100	7	OUTPUT. 100 Hz clock output synchronized with 10 ms Frame.
VSS	8	POWER. 0 Volt connection.
VDD	9	POWER. Positive supply voltage.
RFCLK	10	OUTPUT. 10 MHz clock output. Logic 1 after reset or when disabled.
PD[7:6]	11-12	TRISTATE OUTPUT. Power Down pins with 12 mA output drive. Hi-Z after reset until PD_en is programmed.
PD[5:0]	13-18	TRISTATE OUTPUT. Power Down pins 5-0. Hi-Z after reset until PD_EN is programmed.
ADSTBn	19	INPUT. When low the ADC will measure peak value on the ADC pin.
AD[11]	20	INPUT. Address pin 11
LKD	21	INPUT. LocK Detect input for synchronisation purposes.
TP2	22	INPUT with pull down. Test pin 2. Connect to ground
RCK	23	INPUT/OUTPUT. Receive data clock. Either the internal generated clock can be used or a external clock can be fed to this pin.
VDD	24	POWER. Positive supply voltage connection
VSS	25	POWER. 0 Volt connection.
CMPREF	26	INPUT. Comparator reference level.
DAC	27	OUTPUT. 6-bit DAC output signal.
AVD	28	POWER. Analog positive supply voltage
AVS	29	POWER. Analog ground
RDI	30	INPUT. Received Data. It is programmable to invert this input.
ADC	31	INPUT. 6-bit ADC input with peak hold circuitry.
TP1	32	INPUT with pull down.Testpin1. Connect to ground.
Xtal1	33	INPUT. 10.368MHz crystal connection to V_{SS}.
CAP	34	External capacitor.
SO	35	OUTPUT. Serial data output.
SK	36	OUTPUT. Serial interface clock: 1.152 MHz

Table 1: Pin descriptions (CONTINUED)

Pin name	Pin number	Description
TDO	37	TRISTATE OUTPUT. Transmit Data. Can be programmed to be inverted.
MEN3n	38	OUTPUT. Microwire enable output active low. Can be synchronized to LKD input
MEN2n	39	OUTPUT. Microwire enable output active low. Can be synchronized to LKD input
MEN1n	40	OUTPUT. Microwire enable output active low. Can be synchronized to LKD input
STR1	41	INPUT/OUTPUT. Strobe signal (see format definitions).
STR0	42	INPUT/OUTPUT. Strobe signal (see format definitions).
RSTn	43	INPUT. Active low Reset.
ASTR	44	OUTPUT. 8 kHz strobe signal.
ICLK	45	INPUT/OUTPUT.Interface clock signal. On falling edge data is latched. On rising edge output data is valid.
ADOUT	46	INPUT/ OUTPUT. ADPCM (linear). ECP input.
CIN	47	INPUT/OUTPUT. ECP output connected to input internal/external codec
COUT	48	INPUT/OUTPUT. ECP input connected to output internal/external codec
TP3	49	INPUT. Test pin 3. Connect to ground.
VREF-	50	OUTPUT. Negative microphone reference
AVS2	51	POWER. Analog ground for CODEC
AVD2	52	POWER. Analog supply for CODEC
MIC-	53	INPUT. Microphone negative input
AGND	54	POWER. Signal ground.
MIC+	55	INPUT. Microphone positive input.
VREF+	56	OUTPUT. Positive microphone reference
LRS-	57	OUTPUT. Negative loudspeaker output
LRS+	58	OUTPUT. Positive loudspeaker output
HOLDn	59	OUTPUT. When low, SC14421 is still busy completing a read or write cycle.
UCLK	60	OUTPUT. Microprocessor clock output: 10.368 ÷ (1 or 16) ÷ (1, 2, 4 or 8).
AD[7:0]	68-61	INPUT. Address bits 7-0.
DAB[7:0]	76-69	INPUT/OUTPUT. Databus I/O to microprocessor.
AD[8]	77	INPUT. Address pin 8.
AD[9]	78	INPUT. Address pin 9.
CSn	79	INPUT. Chip Select. Active low.
CLK1/3M	80	OUTPUT. 1.152MHz or 3.456 MHz clock output.

Note 1: PD 3 as well as MEN1n, 2n & 3n rising or falling edge can be synchronised to LocK Detect (LKD pin 21) rising or falling edge. PD1 rising or falling edge can be synchronised either to the end of the complete S pattern or to the end of the bit sync part of the S pattern

Connection diagram



Order Number SC14421VF (6 dB dynamic range Echo canceller)
Order Number SC14421BVF (18 dB dynamic range Echo canceller)
Order Number SC14421CVF (improved clock recovery circuitry)
See NS package Number VJE80A

Background information

The Digital European Cordless Telephone (DECT) System

DECT provides a wireless radio connection at 1.9 GHz between a handset and a radio receiver. This radio receiver will normally be connected to the public or a private telephony network.

One or more handsets or portable parts (PP), can communicate via one radio receiver or fixed part (FP), with each other or to the outside world, either via a PBX or not. The SC14421 is optimized for use in a domestic basestation connected via an analog line interface to the central office. A second codec interface allows for a corded phone to be connected to the base. The SC14421 is equipped with a dedicated Digital Signal Processing unit which handles tone generation, conferencing and echo cancelling and suppression. In case of ISDN for both B channels

echo suppression can be selected. More SC14421's can be connected in parallel to allow for a modular approach with more external lines.
The SC14421 used in a basestation can handle 6 MAC connections, i.e. two sets of two handsets can talk with each other while two other handsets can communicate to the outside lines.
For every MAC connection a different encryption key can be used simultaneously.
The radio communication uses digital technology which permits time division multiplexing with simultaneous signalling information and speech information on the same carrier. Speech is digitally encoded and compressed according to the 32 kbit/s ITU G721/G726 ADPCM recommendation.
The distributed Radio Resource Management determines dynamically who is using, which radio frequency channel at a certain timeslot. The control is done via the handset rather than via the base stations. In this way a flexible and future expandible system is created.

Time Division Multiple Access (TDMA) Timeslots

DECT uses frequency multiplexing (10 frequency bands) and time division multiplexing. The data to be transmitted is compressed into bursts and some additional control information is added. A time frame of 10 milliseconds is divided into 2 x 12 timeslots in a full slot operation. One out of the first 12 timeslots is used to transmit from the fixed part towards the portable part; One out of the second 12 timeslots in a frame is used to transmit from the PP towards the FP. There are always 12 timeslots between transmitting and receiving and all PP synchronize on the received frame from the FP. Time-slot K and timeslot K+12 make up a timeslot pair.

Digitized Speech

Speech is digitized by a CODEC and then ADPCM coded which leads to a bit rate of 32 kbit/s. Thus each 10ms (the burst period) 320 speech data bits are available. To allow for synchronization and MAC control in total 424 bits are transmitted in a burst. The guard period is equivalent to 56 bits. In total 480x12x2 databits have to be transmitted in 10 msec which leads to an overall bitrate of 1152 kbit/s.
In special applications this data bandwidth can be used for pure computer data as the DECT specification includes a transparent mode that bypasses the audio components. The specification allows for multiple timeslots to be used so that the full bandwidth is available for data transfer. The SC14421 is capable of fulfilling half slot, full slot and double slot formats. And is flexible to configure almost any other slot format. Protected B field CRC calculation is only performed in full slot operation.

Access Protocol

The SC14421 assists a microprocessor to access a timeslot. This access protocol is decentralized and controlled by the PP. The DECT access protocol is comparable with the access protocol on a local area network like ethernet (Carrier sense multiple access with collision detection).

Received Signal Strength Detection

The frequency band to be used is determined by the Received Signal Strength Indications (RSSI) of the different frequencies. The one with the lowest RSSI is selected as this indicates a channel with no activity. These RSSIs are continuously monitored. Switching to the frequency with the lowest RSSI can happen during an active connection without interruption of the communication for the purpose of seamless hand over. The microprocessor keeps tables of the RSSI values of the available channels, which are updated during each RSSI scan.
Carrier Sensing leads to the selection of a quiet slot. More PPs could decide to "jump on" the idle channel and a collision occurs. Collisions are detected by the fact that a normal exchange of data messages during a connection establishment phase is disrupted.

Functional description

The SC14421 interfaces to:
- The Radio Front end
- A microprocessor.
- The data interface / ADPCM interface
- Line interface.

The Radio Front-End Interface

The SC14421 can fully comply to any radio interface (including ARi1™*) providing all necessary timing signals and control information.

SYNTHESIZER INTERFACE

A flexible serial interface with three separate enable signals allows the user to control almost any RF synthesizer device. Any number of bits can be transferred, three enables (MEN1..3n, pin # 40..38) are programmable active low or active high. These MEN pins can also be used for any other RF control signal. The serial interface consists of a data output (SO, pin # 35) and a clock (SK, pin # 36). The data rate is 1.152 Mbit /s.
The RFCLK (pin # 10) output pin on the SC14421 is meant to be used as the reference input clock for the synthesizer. This clock is a buffered output of the frequency controlled crystal oscillator of the SC14421 running at 10.368 MHz (9x baud rate). For power saving it is possible to set the RFCLK output to become high.

PROGRAMMABLE CONTROL PINS

The SC14421 provides eight programmable timing signals PD[7:0] (pin # 11.. 18). Each of them can be individually set or reset at any time during a frame. These timing signals can be used to activate or deactivate the front end circuitry. Two timing signals PD6 and PD7 have a 12 mA output drive capability for applications such as driving PIN diode switches.
After reset the PD outputs will be in the Hi-Z mode. Only when enabled the pins will get their programmed value. This allows to control with external resistors these pins to be high or low after reset.

* ARi1™ is a trademark of National Semiconductor Corporation

To prevent activating the power amplifier while the synthesizer is not in lock or to prevent switching off the synthesizer in a VCO driving state: one of the pins PD3 as well as MEN1n, 2n&3n can be programmed to adjust its falling or rising edge to the lock detect output of the synthesizer.

RSSI PEAKHOLD ADC

In order to select the best frequency channel with respect to signal to noise ratio, the so called Received Signal Strength Indication (RSSI) is measured for the different frequency bands.
To define the time period in which the RSSI has to be measured one of the timing signals can be used connected to ASTBn (pin # 19). As long as ASTBn is low, the peak value is measured. The on chip peak hold 6-bit ADC can be used to convert the RSSI peak value on pin ADC (pin # 31). The peak detector can track peaks from zero to maximum scale within 32 microseconds. The ADC data bits are written into the Data memory at different locations for each slot. Whenever ASTBn is high the ADC input pin is connected to ground to discharge the external capacitor.

MODULATED OUTPUT

The modulation method for RF transmissions in DECT is gaussian frequency shift keying with a bandwidth x bit period product, BT=0.5. The SC14421 generates at the Transmit Data Output (pin TDO, pin # 37) the burst data at the baud rate (1152 kbit/s). The TDO output can be programmed to output a gaussian shaped symbol. The shape is spread over three symbols and coded with an eigth bit DAC. The amplitude can be controlled with another 3 bits. The Gaussian output voltage is independent of the supply voltage level. With information loaded in the Data memory this output can be controlled. With control bit "INV_TDO" the TDO output can be inverted. With M[1:0] set to: M[1:0]='00' Digital output is selected. M[1:0] ='10' powers down. M[1:0]='01' activates the gaussian output shape. M[1:0]= '11' set TDO to the mid level. With VOL[2:0] the amplitude of the gaussian shape can be trimmed step wise (see Table 5).

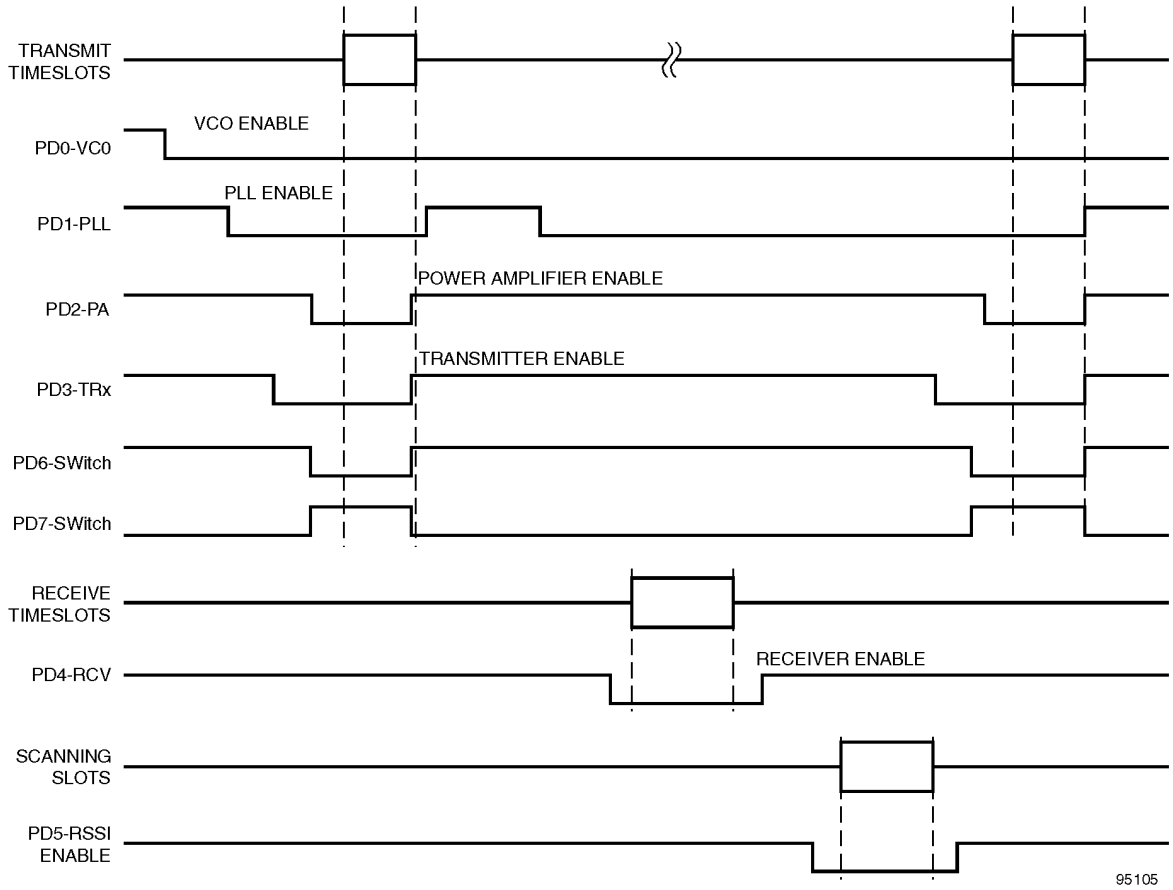


FIGURE 3. Typical timing

DEMODULATED DATA INPUT

The demodulator in the RF front end regenerates the data bits, when activated by one of the timing signals PD[7:0], the data bits. The Received Data In (RDI, pin # 30) is clocked into the SC14421 on the rising edge of the clock signal (RCK, pin # 23). With control bit "INV_RDI" inversion of RDI signal can be selected.

The SC14421 is equipped with a very stable and accurate received symbol timing extraction unit using a nine times over sampled digital phase correlator on the S-field. It is selectable to use either the internal generated clock or an external generated clock. A fast (total delay of less than 30 ns), low power (<500 µA when active) comparator allows for demodulated data to be input on the RDI pin, with input levels typically as low as 100mVpp.

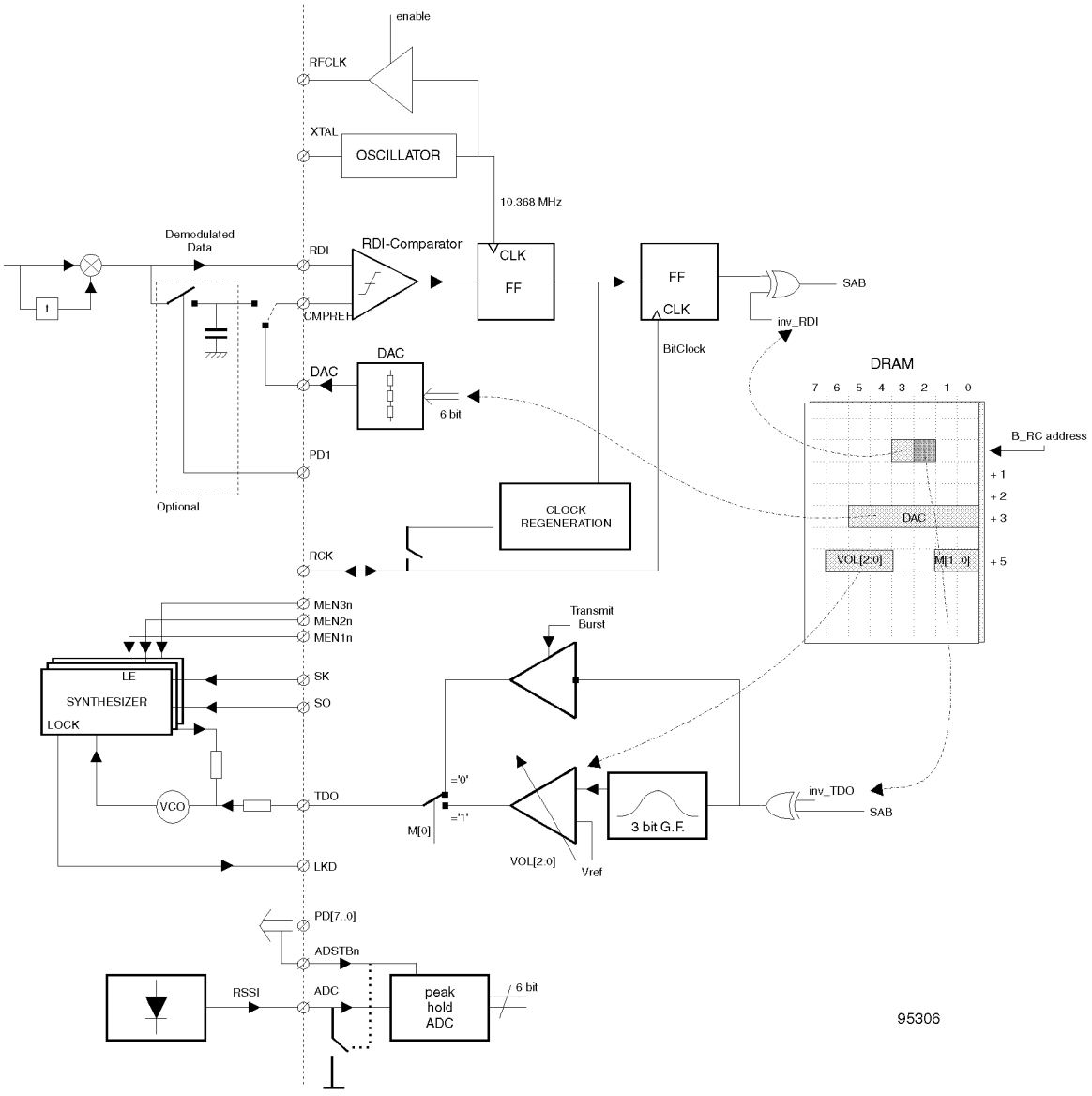


FIGURE 4. SC14421 Radio Front-end interface

DC OFFSET COMPENSATION

To allow for compensation of the DC offset generated in the RF circuitry due to mixer imbalances and/or frequency offsets, the SC14421 offers two solutions. The first solution uses the S-field bit sync pattern to measure the DC-offset by means of measuring the eye opening duty cycle. DC offset can only be measured correctly if the comparator reference level is within the eye opening of the received data input. Four symbols are measured with nine times oversampling. At the end of each received packet the measured offset is stored in the Data RAM status information bytes The microcomputer can control a 6-bit DAC to compensate for the DC-offset. The DC offset value ranges from 0 to 36, binary coded. If the output value equals 18 then there is no DC offset. In case the output is:

0 ≤ output ≤ 17

Then the DC offset of the data signal is positive and the reference level should be adjusted accordingly. If the output is:

19 ≤ output ≤ 36

then the DC offset of the input data signal is negative and the reference level should be lowered accordingly. In the MAC "locked" state (S and Qt detected) the DC offset is reported as zero if the S-field is incorrectly received. In the "unlocked" state the DC offset value is continuously updated and allows for initial DC offset control.
A second DC offset method is implemented to be used in case the offset variation exceeds the received signal eye opening. The SC14421 provides an accurate control pin PD1 in case the DC offset is measured with an external capacitor. One can program the PD1 pin to rise or fall synchronised with the end of the bit sync pattern of the S field or the end of the complete S field.

Microprocessor Interface

A microprocessor is part of the DECT system architecture. The microprocessor takes care of all datalink layer and network layer protocols. The SC14421 Dedicated Instruction co-Processor (DIP) can be programmed to control all baseband MAC and physical layer protocols autonomously. The SC14421 is defined such that the microprocessor is relieved from all time critical tasks. The SC14421 controls all burst mode timing. On slot level typically a 5 ms reaction time is needed. The microprocessor can program, on a frame basis for each timeslot, a number of control and data bytes to control the RF circuitry in a very flexible way. A DECT timeslot is subdivided into the so called A-field and the B-field. The A-field contains signalling and MAC layer control information and the B-field contains speech or data information. The SC14421 takes care of synchronizing to a timeslot, multiplexing and demultiplexing of the A and the B-field respectively. A-field messages are processed by the microprocessor. Several received A-field messages can be stored in sub-banks of the Data RAM. It is programmable which message is to be transmitted in which timeslot and vice versa.

DIP PROGRAM MEMORY

The so called Sequencer RAM of 512 bytes containing the program words for the Dedicated Instruction Processor (DIP) can be accessed as being external RAM to the microcontroller. An instruction is loaded at address N with a word access to address 2N and 2N+1.The SC14421 allows for any kind of word access. An instruction is loaded to address N upon writing consecutively to address 2N[+1] and 2N[+1] where N = 1..254 and [+1] is optional.

2 KBYTE DATA MEMORY

The SC14421 is equipped with 2kbyte random access memory (Data RAM) to be used for data storage by both an external micro controller and the SC14421. An internal arbiter handles the access conflicts. A Holdn active low output pin (pin # 59) holds the microcontroller if internal access is required. The Chip Select pin (CSn pin # 79) must be low to access the SC14421. This CSn pin can be used to differentiate between more SC14421's if used in parallel.

Table 2: SC14421 hardwired address mapping

SC14421 pin	Indirect mode	Linear mode 0	Linear mode 1	Linear mode 2
AD[0] pin # 61	=> A0	=> A0	=> A0	CS0n (A15)
AD[1] pin # 62	=>A1	=> A1	=> A1	CS1n (A12)
AD[2] pin # 63	=>A2	=> A2	=> A2	'1'
AD[3] pin # 64	=>A3	=> A3	=> A3	'1'
AD[4] pin # 65	=>A4	=> A4	=> A4	=> A12
AD[5] pin # 66	=>A5	=> A5	=> A5	=> A13
AD[6] pin # 67	=>A6	=> A6	=> A6	=> A14
AD[7] pin # 68	=>A7	=> A7	=> A7	=> A15
AD[8] pin # 77	=>A8	=> A8	=> A8	=> A8
AD[9] pin # 78	CS1= '1'	=> A9	=> A9	=> A9
AD[10] pin # 6	CS2= '1'	=> A10	=> A10	=> A10
AD[11] pin # 20	CS3= '1'	=> A11	=> A11	=> A11
DAB[0] pin # 69	=>DB0	=> A16	=> A16	=> A0
DAB[1] pin # 70	=>DB1	=> A17	=> A17	=> A1
DAB[2] pin # 71	=>DB2	=> A18	=> A18	=> A2
DAB[3] pin # 72	=>DB3	=> A19	=> A19	=> A3
DAB[4] pin # 73	=>DB4	=> A20	=> A20	=> A4
DAB[5] pin # 74	=>DB5	=> A21	=> A21	=> A5
DAB[6] pin # 75	=>DB6	=> A22	=> A22	=> A6
DAB[7] pin # 76	=>DB7	=> A23	=> A23	=> A7

ADDRESS PINS

The SC14421 is equipped with 12 address pins and 8 data/address multiplexed pins. Depending on the selected mode the address pins will be used differently (see Table 2).

INDIRECT RAM ACCESS

The SC14421 is backwards compatible with the SC14401/420 family and is equipped with an indirect addressing mode to address both the data and the Dedicated Instruction Processor program memory. (Be aware that writing to Sequencer RAM address N uses a word access to address 2N and 2N+1 as oposed to writing consecutively twice to address N as in the SC14401). Instead of two banks of Data RAM eight banks of Data RAM can be accessed. In Table 2 an overview is given. In the indirect mode address pins AD[11:9] must be ‘1’ to access the chip. The control register is located at address FFF

After power on reset (RSTn pin # 43 low) the SC14421 is initiated in the indirect mode. By setting the correct data bits in the control byte the different modes can be selected. A software reset will not affect the settings (see Table 3).

DIRECT RAM ACCESS

In addition to this indirect mode three different direct addressing modes are implemented for optimal use with eg the mitsubishi 16 bit micro controller family or 8051 type controllers. Mode 0 and 1 are optimized for use with a M377xx family and Mode 2 is optimized for an 8051 controller type. The direct addressing modes allow connecting the SC14421 without additional decoding logic.
In all direct addressing modes the databus is used as a multiplexed data address bus. In mode 0 and 1 pins DAB[7:0] are used as AD23..AD16 at Address Strobe (AS, pin # 2) signal going low. In mode 2 pins DAB[7:0] are used as AD7..0 at Address Latch Enable (ALE, pin #2) going low. In Table 2 an overview is given of proposed ad-

dress line connections between the controller and the SC14421. In Figure 5 a memory map for mode 0 and 1 is depicted using these proposed connections.
In mode 0 the SC14421 Data RAM address locations are such that the M37702 can use a total memory ranging from address 00.00.80 up to 00.xF.FE without restrictions. 128 bytes ranging from address 00.x8.00 upto 00.x87F overlap in the SC14421 with the memory in the micro controller. These SC14421 addresses can not be read resp. written by the controller. However the SC14421 may use these addresses internally. On address 00.xF.FF the control register is located. Be aware that the SC14421 internally uses the Data RAM memory in banks of 256 bytes. Therefore A- and B-field data can not cross a bank border.
In mode 1 the Data RAM is located at 80.x8.00 upto 80.xF.FE and address 80.xF.FF is the control register. In both modes 0 and 1 the Dedicated Instruction Processor program sequencer memory (SRAM) is located at address 80.x0.00 upto 80.x1.FF
Mode 2 is optimized for micro controllers with 16 address lines only. Next to CSn two additional select pins are provided on pins AD[0] and AD[1] With the proposed connections (see Table 2) the SRAM is located at address 10.00 upto 11.FF with AD[0]= '0' and AD[1]= '1'. The data ram is mapped at 08.00 to 0F.FF with AD[1]='0' and AD[0] can be either '0' or '1'.

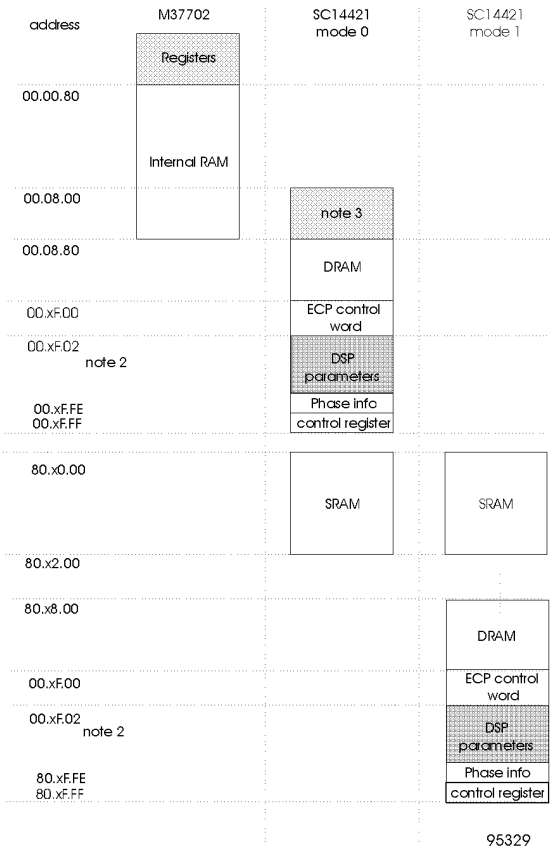


FIGURE 5. Memory map

Note 2: x = 0..F since A12..A15 are not used in the SC14421. The SC14421 is only selected if CSn = '0'
Note 3: Can not be addressed by the controller but may be used by the SC14421 internally.

INTERRUPT VECTOR

The DIP can set an interrupt vector and controls an open drain interrupt pin (INTn pin # 5). Upon reading the interrupt vector the INTn pin is reset to logic 1.

MICROPROCESSOR CLOCK

The SC14421 provides a clock to the microprocessor (UCLK, pin # 60). This clock is derived from the main clock of 10.368 MHz via a prescaler followed by a divider. The microprocessor can program the division ratios. The ratios are 1 (no division) 2, 4, 8. In case of no division 40 to 60 % duty cycle can occur. After reset, divide by 8 is selected and the prescaler is switched off. A fixed prescaler division by 16 can be programmed to switch the microprocessor into low power mode if enabled with bit 6 in the control register. When this bit is cleared the prescalar will be switched off. On interrupt generated by the SC14421 this prescaler will be switched off. A continuous clock of 100 Hz (CLK100 pin) coupled to the 10 ms frame can be used to update multiframe and frame counters, or to synchronise different basestations.

INTEL OR MOTOROLA MODE

With the microprocessor mode pin (UMC) one can select between mode I type processors (INTEL) and mode II type processors (MOTOROLA). The functions of the microprocessor control pins depend on the selected mode. In both modes a separate twelve bit wide address bus (AD[11:0]) and an eight bit wide data I/O bus (DAB[7:0]) exist. For a microprocessor with address/data bus multiplexed the address (AD[7:0]) and data bus (DAB[7:0]) have to be connected.
In mode I Address Latch Enable (ALE, pin # 2) and separate read (RDn, pin # 3) and write (WRn, pin # 1) signals are available. In mode II Address Select (AS, pin # 2), Enable not (En, pin # 3) and Read/Write-not (RWn, pin # 1) signals are selected. These modes allow connection to almost any microprocessor.

Table 3: Write to control register

7	6	5	4	3	2	1	0	Remarks	
		1	x	x	x		0	indirect mode	sequencer memory addressed
		0	0	0	0			indirect mode data RAM selected	bank 0
			0	0	1				bank 1
			0	1	0				bank 2
			0	1	1				bank 3
			1	0	0				bank 4
			1	0	1				bank 5
			1	1	0				bank 6
			1	1	1				bank 7
				0	0		1	linear mode	mode 0
				0	1				mode 1
				1	x				mode 2
1								Force sequencer program to stop. Address is put to 1. Reset BMC/ADPCM to its initial states	
0								start sequencer program at address 1	
	1							prescalar enabled	
						1		timer interrupt enabled	

Table 4: Read from control register

bit 7	6	5	4	[3:0]
RST	Prescalar	'0'	Timer interrupt	interrupt vector

Note 4: The control register is located at address xx.xF.FF, where xx.x = don't care in the indirect mode, xx.x = 00.d in mode 0 (d=don't care), xx.x = 80.d in mode 1 (d=don't care), or xx.x = xx.F in mode 2.

ADPCM

The SC14421 integrates two full duplex ADPCM transcoders respectively channel 0 and 1. Both channels can be independently configured.
The SC14421 encodes/decodes linear coded voice samples down to 32 kbit/s. The prescribed ADPCM technique used is fully complying to G721/G726.

MUTE

If enabled by the microprocessor, by means of the SENSE_A = '1' control bit, the SC14421 will only write the received B-field in the case A-field CRC is correctly received. In this way the last frame is repeated and erroneously received frames will not disturb the ADPCM. The microprocessor can also decide to mute either channel 0 or 1: in that case the ADPCM input is forced to zero.

VOLUME CONTROL

(CHANNEL 0 ONLY)

ADPCM channel 0 receiver has a coarse level control of 3 dB/step from 0 to -36 dB. The sidetone level programmable to be either -6 or -12dB, is independent of the coarse receive level selection and can be switched off.

Line interface

The SC14421 is equipped with a CODEC and a fully differential Analog Front End, to directly connect to lineinterface circuits.

Table 5: Overview of Control Information

Bit Name	Type	Function (set with logic 1 unless stated)
S_err[3..0]	Binary	maximum number of errors allowed in non-masked bits of S-field pattern S[8..31]
Inv_RDI		Inversion of received data input
Inv_TDO		Inversion of transmit data output
SENSE_A		B field data is not written in the case when the A-field CRC is incorrect
PP/FPn		PP mode selected
MASK[15..8]		S field bit[i] is ignored in case MASK[i] = '0' for i in 15..8 in the S pattern detection phase
SLIDE[15..8]		S field bit[i] is ignored in case SLIDE[i] = '0' for i in 15..8 for the sliding error calculation.
DAC[5..0]	Binary	DAC output value to control DAC pin 27
ADP		Upon A-field CRC error, no phase adjustment will be made
WIN[3..0]	Binary	Defines maximum phase shift. If phase shift is between ±WIN symbols, the IN_SYNC bit will be set
VOL[2..0]	Binary	TDO gaussian output volume control. 1dB per step. Default '100' mid value after reset.
SCoff	Binary	0 = scrambling on 1 = scrambling off
DOFr	Binary	0 = PD1 sync on bit pattern of S_field 1 = PD1 sync on complete S_field
M[1..0]	Code	Defines the output mode on TDO pin; 00=digital output 01=Gaussian output 10=power down 11=mid level
FR_nr[3..0]	Binary	Frame number 0..15
MFR[23..0]	Binary	Multi frame number
IV[28..63]	Code	Encryption unit initialisation vector
CK[0..63]	Code	Encryption unit cypher key

Dedicated Instruction Processor

The SC14421 contains a Dedicated Instruction Processor (DIP). All instructions are backwards compatible with the National DECT family SC14420/401. The instructions are stored in the so called Sequencer Random Access Memory (SRAM). This permits connection to different RF-frontends without the need to change ROM codes in the SC14421. For more detailed information see the SC144XX DECT Family Commands Manual.
Once correctly programmed the SC14421 takes care of all the slot and frame timing without microprocessor interruption. All necessary data and control information can be stored in advance to control a complete 10 ms frame without microprocessor interruptions even if more slots with different data areas are used. Consecutive instructions are performed at the symbol clock rate. Eight programmable timing signals (PD(7..0)) are provided to control, activate or deactivate the RF front end. These timing signals can be set or reset by instructions loaded into the sequencer memory. Every symbol period a new instruction is fetched. There for these signals can be set/reset with a resolution of 1 symbol period. As an example Figure 3 shows the timing of the ARi1 interface
The Sequencer RAM program allows for jumps to subroutines and unconditional branches. A wait N symbols opcode puts the Sequencer RAM in a mode where it waits N symbol periods before the next instruction is performed. The Wait for next slot opcode waits to process the next instruction line until the active slot is finished.
If enabled (e.g. in the PP mode) the next slot counter is synchronized to the received frame structure. In paging mode, both normal and slow scan, the programming is such that only once every 16 or 64 frames the Sequencer

RAM program is looped through. Specific instructions in the sequencer memory control the location of the data storage in the data RAM.
At initialization the microprocessor has to take care that the appropriate data is stored in the Sequencer RAM. With bit 7 set to '1' in the control register, the chip will reset to its initial state. Data is retained in the memories during this reset. When bit 7 is set to '0' the actions in the sequencer memory will be performed starting from address '1'.
With this implementation one has the possibility, with a resolution equal to the symbol clock (870ns) to:

1) Set or reset at any moment the PD(7:0) signals.
2) Receive and or transmit in any (or all) timeslot(s).
3) Preprogram different A-field data messages
4) Program different synthesizer control programs for any slot without mC interruption
5) Program normal and low speed paging
6) Program interrupts at any time in the frame
7) Program receive levels
8) Control the ADPCM mute for both channels and sidetone and receive levels for channel 0 only.
9) Program test loops
10) Program Power Down modes.
11) Handle encryption on all slots
12) Program protected B-field formats
13) Format half, full and double slots
14) To build any other user defined format.

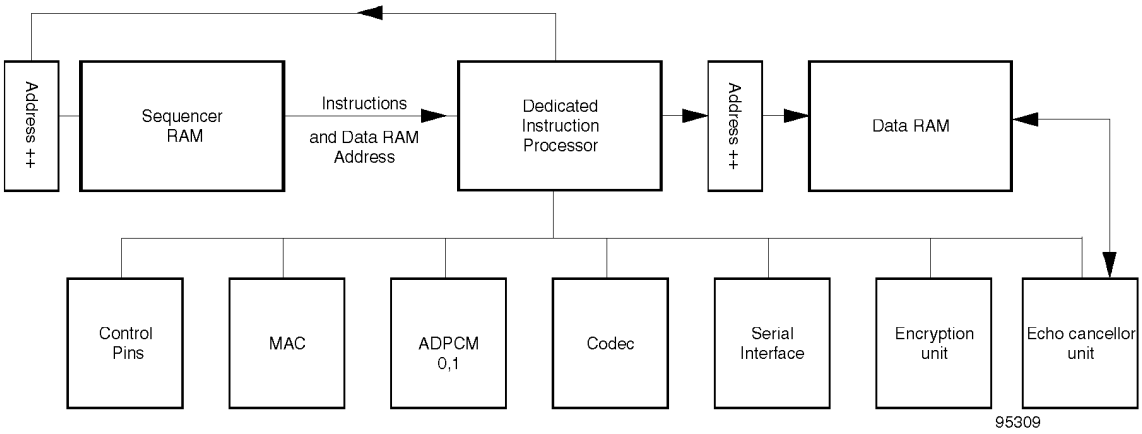


FIGURE 6. SC14421 Dedicated instruction processor

Dedicated Signal Processor unit (ECP)

In the SC14421 a dedicated hard coded echo canceller/ echo suppressor, according to ETS300-175-8, and tone generator is implemented. One analog subscriber line can be supported with echo cancelling and suppression. In case of ISDN echo suppression can be performed on both B channels. The dedicated signal processor includes also a conferencing function. Conferencing can be set up between two handsets, the external line and the eventually connected basestation phone (four party conference). All functions are implemented in ROM. All used parameters, timing constants, decision levels and coefficients are stored in the Data RAM. This permits to program and monitor this device to its full extend.

The Echo canceller/suppressor.

The EC algorithm uses a 32 tap FIR filter with the commonly used Least Mean Square (LMS) update algorithm. The coefficient update constants (μ_n) and the coefficients (Ci) are stored in the Data RAM and can be initialized and monitored during operation. A Voice Activity Detection(VAD) algorithm is implemented to perform Echo suppression with a programmable attenuation and a smoothly switching on/off characteristic. The implemented algorithm incorporates all necessary means to allow for fast convergence, prevents incorrect update of the coefficients and switches on and off the echo canceller/suppressor in case the receive level has a certain ratio over the transmit level. The EC on/off control has programmable time constants. Two different time constants for switching on and off exists. In Figure 8. an overview of the different areas and modes is depicted. The areas are defined with the ratio between the incoming data signals and the signals send on the line.

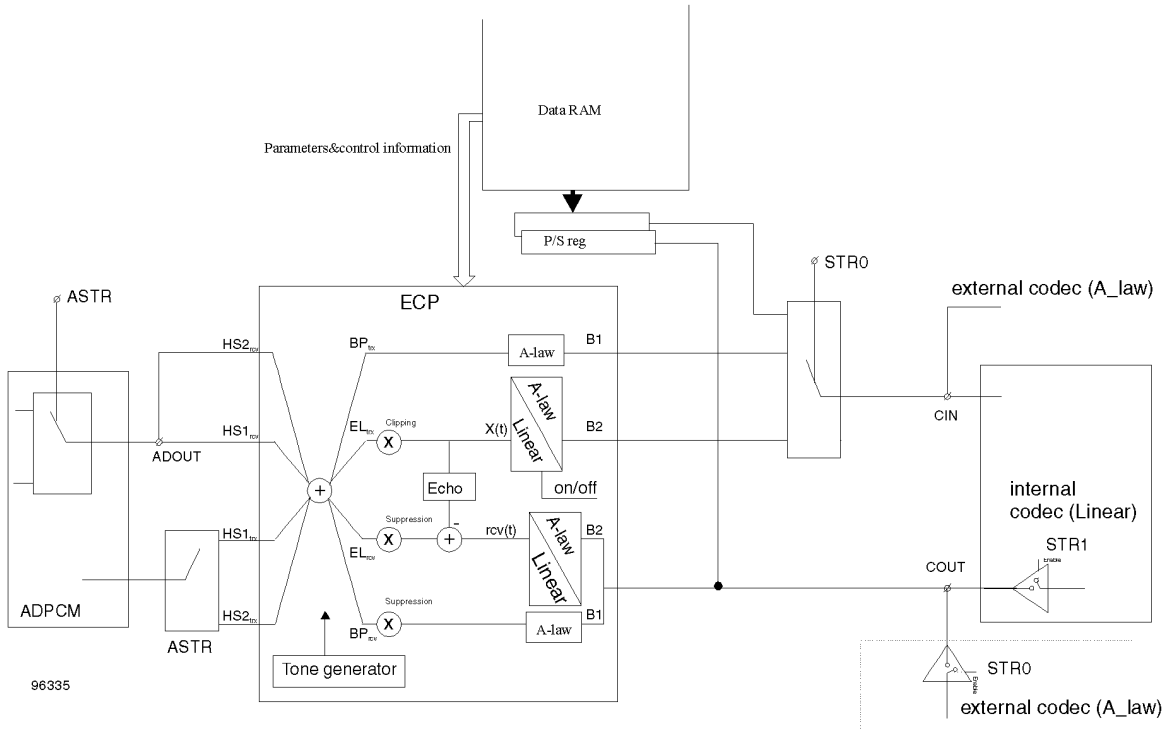


FIGURE 7. Dedicated Signal Procesing Unit (ECP)

Note 5: codec is only active in FORMAT 1 interface mode

Algorithm

Reconstructed echo signal:

$$) = 2\alpha \cdot \sum_{i=0}^{31} C_i(t-T) \cdot X(t-iT-4T)$$

$$t) = C_i(t-T) + \mu_n \cdot [rcv(t) - \varepsilon(t)] \cdot X(t-iT-4T)$$

$$= \frac{1}{8kHz}$$

$$) = echo \cdot path \cdot reconstruction$$

$$\cdot - iT - 4T) = transmitted \cdot data$$

$$'(t) = received \cdot data$$

$$= update \cdot constant \sim \frac{1}{(P_{TRX})^2}$$

$$= Filter \cdot coefficient$$

Echo canceller coefficient-update-constant (μ_n) and transmit and receive levels time-constants depend on the mode. All parameters can be programmed between 0..1-2_{-14} in the data RAM. All C_i and X_i must be initialized to "0".

The echo suppression (Sup) is smoothly switched on and off. Both switching on and off have programmable time constants.

$$EL_{RCV}(t) = [rcv(t) - \varepsilon(t)] \cdot Sup(t)$$

$$Sup(t) = (1 - S\beta_m) \cdot Sup(t-T) + Sup_{ON/OFF} S\beta_m$$

A delay for the suppressor can be programmed by loading a decrement counter with a preset value. Also a centerclip function (noise suppression) is implemented. When the RCV level is below a programmed threshold the suppressor will be active and the RCV signal will be attenuated with 12 dB.Different modes are selected depending on the ratio between receive and transmit levels. The levels are calculated as follows:

Rise time and hold time of the level calculation is determined by programmable update constants $P\beta_m$ ($P\beta_m$. can be $P\beta_r$ or $P\beta_f$)

If $P_{TRX}/P_{RCV} \leq Ratio0$ then the echo canceller is off. The update constant μ_n is set to "0".

If $P_{TRX}/P_{RCV} \leq Ratio1$ echo suppressor is switched off.

$$_{RX}(t-T) < (\beta_L \cdot |X(t)|)$$

$$\cdot \left(P_{TRX}(t) = \frac{|X(t)|}{2}\right)$$

$$\cdot P_{TRX}(t) = (1 - P\beta_m) \cdot P_{TRX}(t-T) + P\beta_m \cdot |X(t)|$$

$$_{V}(t) = (1 - P\beta_m) \cdot P_{RCV}(t-T) + P\beta_m \cdot |rcv(t) - \varepsilon(t)|$$

If $P_{TRX}/P_{RCV} \leq 1/Ratio2$ *AND* $P_{TRX} \geq LvL1$*:* the echo canceller&suppressor are switched on. The Echo canceller update constant μ_n is given a value dependent on the transmit level. If $P_{TRX} \geq LvL1$ then μ_1 is selected. If $P_{TRX} \geq LvL2$ then μ_2 is selected and if $P_{TRX} \geq LVL3$ then μ_3 is selected. If $P_{TRX} \geq LVL4$ then soft limiting is performed on the X(t) signals. Limiting off time constant is equal to the echo suppression off time constant. The limiting value is equal to LVL4 in case the level is exceeded otherwise Limit_off is taken.
In all other cases:(double speech mode) the echo canceller&suppressor are switched on. The update constant is μ_0 .

$$= Limit(t) \cdot EL_{TRX}$$

$$_{t}) = (1 - S\beta_{off})Limit(t-T) + (S\beta_{off} \cdot Loff)$$

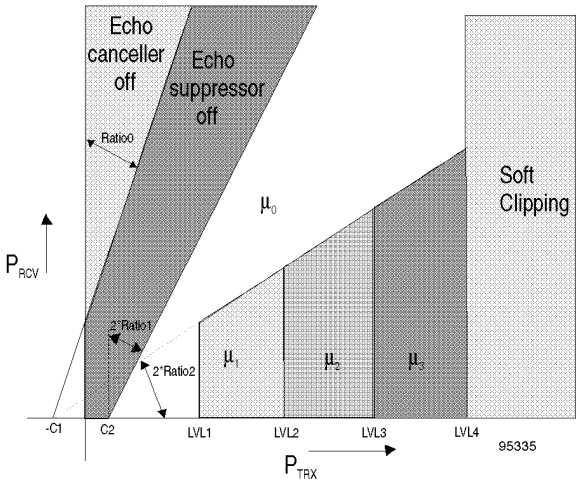


FIGURE 8. Mode definitions

DTMF tone generator

The dedicated signal processing unit calculates sine waves using standard mathematical techniques.

$$y_1(t) = N_1 \cdot y_1(t-T) - y_1(t-2T)$$

$$y_2(t) = N_2 \cdot y_2(t-T) - y_2(t-2T)$$

$$DTMF(t) = y_1(t) + y_2(t)$$

Initialization, i=1,2

$$N_i = 2 \cdot cos(2\pi T \cdot f_i)$$

$$y_i(-T) = Amp \cdot sin(2\pi T \cdot f_i)$$

$$y_i(-2T) = 0$$

$$T = \frac{1}{8kHz}$$

Any single or dual tone can be generated with correct initialisation data written in the Data memory. It can be controlled whether the tone is transferred towards the internal codec (line interface), the external codec(basestation phone), handset_1 or handset_2 or any combination.
A programmable timer is implemented which defines the active and idle times for the DTMF tones. Two preset values PRST1 and PRST2 can be set. At the end of active time defined by the PRST1 value, an Interrupt will be set. Bit 4 in the control register will be set and the INTn (pin#5) will be activated when enabled with bit 4 set to 1 in the control register (see page 11).

Conference function

It is possible to implement a four party conference between two handsets, the external line (EL) and the "base station corded phone (BP)".

$$HS1_{TRX} = \alpha_{HS2} \cdot HS2_{RCV} + \alpha_{EL} \cdot EL_{RCV} + \alpha_{BP} \cdot BP_{RCV}$$
$$HS2_{TRX} = \alpha_{HS1} \cdot HS1_{RCV} + \alpha_{EL} \cdot EL_{RCV} + \alpha_{BP} \cdot BP_{RCV}$$
$$BP_{TRX} = \alpha_{HS1} \cdot HS1_{RCV} + \alpha_{HS2} \cdot HS2_{RCV} + \alpha_{EL} \cdot EL_{RCV}$$
$$EL_{TRX} = \alpha_{HS1} \cdot HS1_{RCV} + \alpha_{HS2} \cdot HS2_{RCV} + \alpha_{BP} \cdot BP_{RCV}$$

Second line interface

It is possible to perform echo suppression only on the second line interface. Ie in case of ISDN this mode allows full use of 2B channels.

$$r_{RX}(t) = HS2_{RCV}$$
$$2_{TRX}(t) = BP_{RCV} \cdot Sup2(t)$$
$$\text{›}2(t) = (1 - S\beta_m) \cdot Sup2(t-T) + S\beta_m \cdot Sup2_{ONOFF}$$

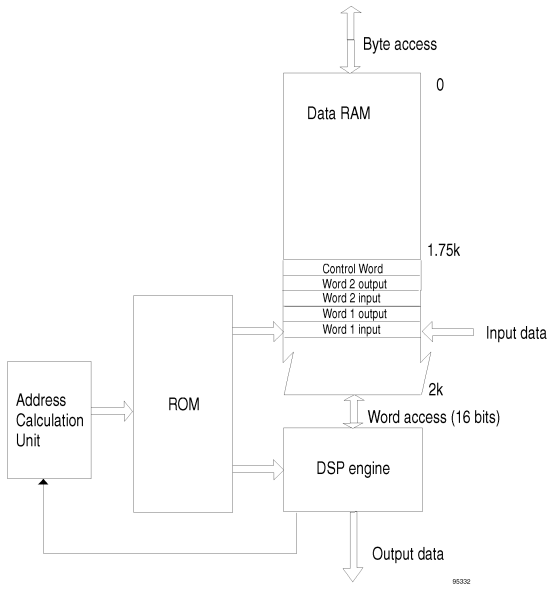


FIGURE 9. Programming in DRAM

Programming

All parameters can be programmed in the Data RAM. The last 256 bytes are used for the DSP engine. The micro computer can access this RAM as normal external RAM at any time. The DSP engine will use the RAM word oriented.

ECP/Codec interface

A very flexible interface to many different external codecs and ISDN interface circuits has been implemented on the SC14421.
With control information in the first byte of the RAM for the ECP block between many options can be chosen.
Four formats are implemented. Only in format 1 the internal codec is activated, so in format1 the B2 data is transmitted to/received from the internal CODEC.

FORMAT 0 (DEFAULT AFTER RESET)

STR0, STR1 are input signals. Both B1 and B2 data are coded according to A_law and on both channels echo suppression is performed.

FORMAT 1

STR0, STR1 are output signals.. B1 is coded according the A-law and B2 is coded linear: 14 bit two's complement sign extended to 16 bit. On channel B1 echo suppression is performed and on channel B2 echo cancelling and suppression is performed.

FORMAT 2:

STR0, STR1 are input signals. Both B1 and B2 data are coded according to A_law and on both channels echo suppression is performed.

FORMAT 3:

STR0, STR1 are input signals. The ECP block is bypassed and two RAM words are transported towards the interface. This can be used for data transfer.

GENERAL

ICLK may be divided by two and can be provided externally or generated internally. A 2.304 MHz or 1.152 MHz clock is output on ICLK if generated internally .
The maximum external clock allowed is 2048kHz or 4096 kHz in case div 2 option is selected. The repetition rate of STR0,1 must be 8 kHz. To prevent data from being lost frequency synchronisation must be performed.

Table 6: Interface control word

Value	15	14	13	12	11	10	9	8
	Conference	DTMF				VADPrcv	Format	
0	off	HS1 off	HS2 off	EL off	BP off	after EC	00= format 0,2	
1	on	HS1 on	HS2 on	EL on	BP on	before EC	01 =format 3	
							10 = format 1	
							11 = format 1	

Value	7	6	5	4	3	2	1	0
	rcv leve	Echo canceller replica gain			Format		ICLK	
0	divide by 1	00= disable ec			00= format 0		external	div 1
1	divide by 2	01 =normal			01 = format 1		internal	div 2
		10 = *2			10 = format 2			
		11 = *4			11 = format 3			

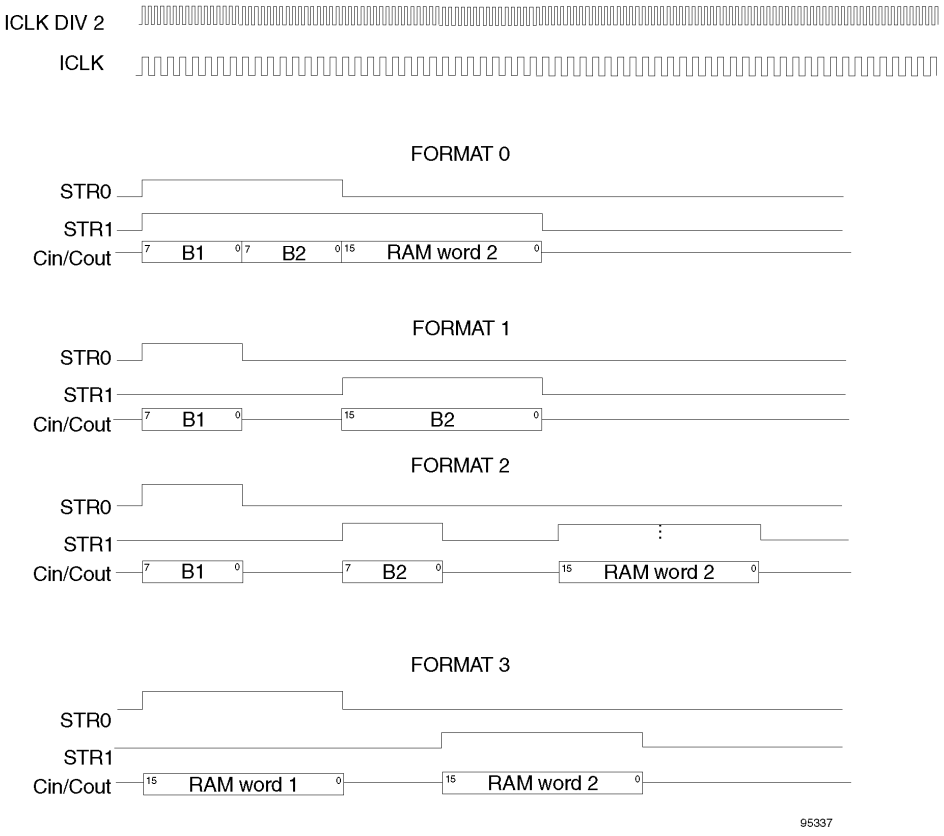


FIGURE 10. Different IO formats on the CODEC interface

Synchronisation Port

The SC14421 enables synchronisation to the incoming 8 kHz in all formats except format 1. Both the crystal frequency and the DECT frame phase can be tuned. After (soft) reset the internally generated 8 kHz is triggered by STR0 input pin. The time difference between the STR0 and the internally 8 kHz signal is measured in units of the bit clock (870ns) and the result is stored in RAM location $0F.FE_{16}$ .Initially 52_{16} is stored. If the value increases the crystal frequency should be decreased and vice versa. A new DiP command <WSC> halts the TDMA co-processor until the first rising edge of the STR0 input signal. This allows to synchronise the 10ms DECT frame to an incoming 8 kHz signal at any bit position.

MAC Functions

Receive and transmit burst timing information is controlled by the DIP. All MAC-CSF functions as depicted in see Figure 11 apart from the T-MUX and E/U-MUX are handled. By programming the data memory control bytes, specific settings can be initialized by the microprocessor. Control information is read before every received and transmitted slot. MAC status information on received slots is written into the Data RAM of the SC14421 (Table 3). At the end of every received timeslot an interrupt instruction can be set in the Sequencer RAM to enable the microprocessor to read out the appropriate status data.

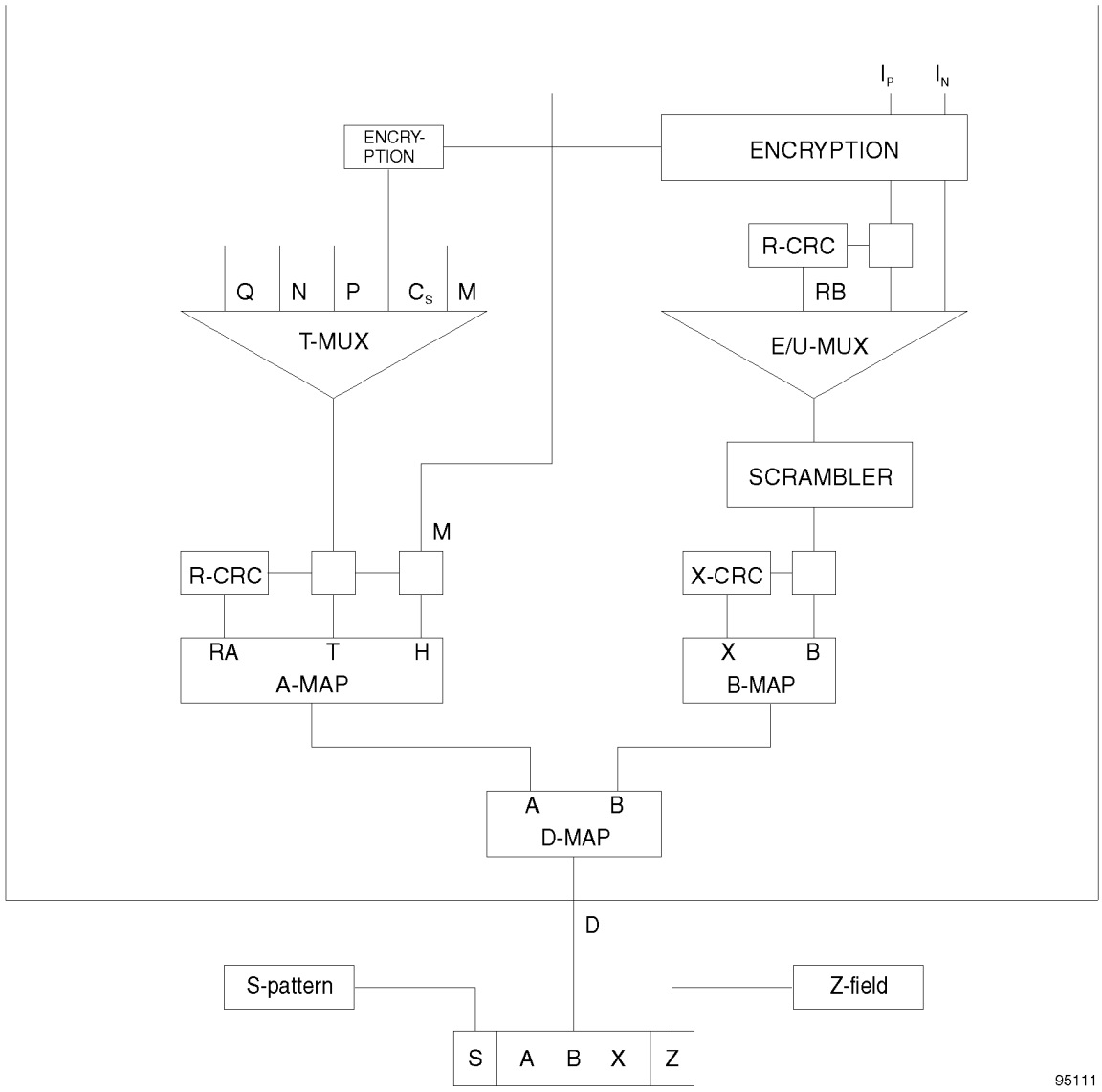


FIGURE 11. SC14421 Mac functionality

SLOT SYNCHRONISATION

The SC14421 is capable of detecting the S-field pattern. To be able to lock to the received frame in the PP mode the microprocessor enables the slot counter to be preset at S-field detection. If the preset of the slot counter occurred once, the preset is disabled. The microprocessor can enable this preset again. If disabled the SC14421 will only search for the S-field pattern in a predefined window repeated every 10ms after the first S-field pattern has been detected. In lock the SC14421 can accept a packet phase shift up to a programmed maximum window size. This window is programmable with control nibble WIN[3:0] from 0-15 symbol periods. This phase shift information is stored in PHASE[7:0] in two's complement notation in the MAC status bytes. If the phase shift is more than the programmed window the "in_sync" bit will be reset. Once enabled by the microprocessor the SC14421 will automatically adjust the frame timing. If the ADP bit is set '1' then the automatic phase adjustment will only be done if the A-field CRC is correct. If ADP is '0' the phase adjustment will be made regardless of the A-field result. Choosing to write the B-field data depending on the A-field CRC result is selectable using the control bit SENSE_A.

Table 7: Overview of MAC return information

Name	Type	Function
ADC[5..0]	Binary	Maximum peak value measured during ADSTBn
IN_SYNC		Set to '1' when the S-Field pattern lies within the defined window size
A_CRC		Set to '1' when the A-field CRC is correct
X_CRC		Set to '1' when the X-field CRC is correct
ZACK		Set to '1' when the Z-field = X-field
Bn-CRC		Set to '1' when protected B field R-CRC of block n is correctly received. Where n =1..4
SL-err[3..0]	Binary	Sliding errors in the unmasked S-field pattern[15..8]
Phase[7..0]	2's Comp	S-field pattern phase error
DC[5..0]	Binary	DC offset information

If the phase shift between the internally generated frame and received frame is less than 2 symbol periods frame timing is adjusted with 1 symbol period at the end of the frame. The update will be maximum 2 symbols if the phase shift is 2 or more symbols. However the microprocessor can take over control and program phase jumps of 1 symbol period instructions for the next frame if appropriate and disable the automatic phase jumps.
The microprocessor programs a jump instruction to the right slot address in the timing RAM once Qt message is received and decoded and thus presets the slot-counter.

S-PATTERN CORRELATOR

With the control bytes it is possible to define the criterion for the S-field to be detected. The first eight bits of the S-field [7:0] bit sync pattern are ignored. On the next eight bits a mask register (S-field bit[i] is don't care in case MASK[i] = '0' for i = 15..8), stored in the data RAM, determines which bits are masked. If the total number of errors in the non masked bits from bit 8 through 31 is less than a number programmed in the Data RAM (S_err[3:0]), the S-field is received correctly and the phase shift can be calculated. S-field bits 15 through 8 are also used to check for sliding errors. These are reported in the MAC unit status bytes: SL_err[3:0]. In the calculation S-field bits[i] are ignored in case slide[i] = '0' for i = 15..8. A sliding error occurs when a neighbouring un-synchronized station sends out a packet that slides into the received packet.

ENCRYPTION

The Key Stream Generator (KSG), used to encrypt A and B-field information, can be switched on or off by the microcontroller via instructions in the Sequencer RAM. The KSG initial state is stored in the internal data memory. CK[63:0] is the cypher key information. The MAC unit recognizes Cs type messages in the A-field data and encrypts or decrypts only these messages.

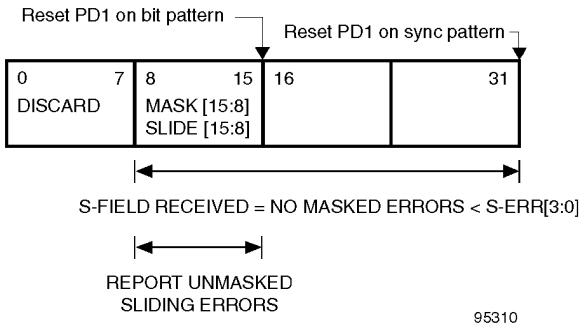


FIGURE 12. S-Field Pattern

SCRAMBLER

Scrambling and descrambling, using the frame counter bits FR_nr[2:0] for initialisation, is performed on the B-field. Scrambling can be disabled on a per slot basis with control bit SCoff in the MAC control information bytes.

R-CRC, X-CRC AND Z FIELD

Generation and checking of the 16-bit CRC is performed on the A-field data (A_CRC will be set if CRC is correct). For the B-field, X-CRC and Z-field are generated and checked for transmission and reception respectively. A, X and Z field results are stored in the internal data memory (A_CRC, X_CRC and ZACK bit). Full slot protected B-field format is supported and 16 bit CRC is calculated for every 64 bits of data.

DATA STORAGE

At the end of every received slot the status is updated in the Data RAM. A-field data and B-field data are fetched and stored in the internal data memory. The user can define as many memory locations and subbanks for different slots and / or A-field messages as needed. See overview of MAC return information (Table 7).

Crystal Oscillator

The SC14421 contains an amplitude controlled oscillator. This oscillator is designed for power saving. The SC14421 runs at a frequency of 10.368 MHz.

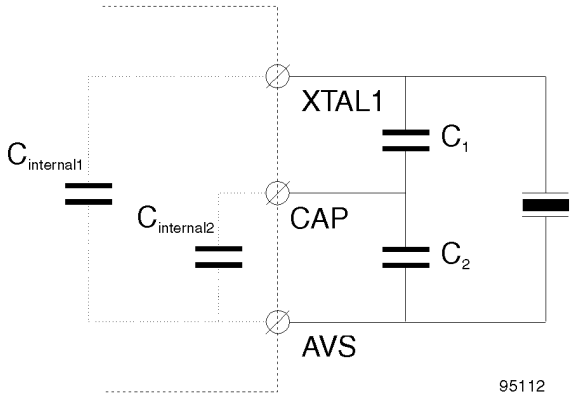


FIGURE 13. Crystal application

$$C_{internal} < 3\ pF$$

$$C_{load} = \left(\frac{C_1 \times (C_2 + C_{internal2})}{C_1 + (C_2 + C_{internal2})}\right) + C_{internal1}$$

Table 8: Crystal specification

Parameter	Max
C Load	41 pF
Rt	75 Ω
CShunt	7 pF

Specifications

Table 9: Absolute maximum ratings (Note 6)

Parameter	Min	Max	Units
Power supply voltage (VDD-VSS / AVD-AVS)		6	V
Voltage on any pin	VSS-0.3	VDD+0.3	V
Storage temperature	-65	+150	°C
Package power dissipation @ 25 °C		500	mW

Note 6: Absolute maximum ratings are those values beyond which damage to the device may occur.

Table 10: Operating Conditions

Parameter	Description	Min	Typ	Max	Units
TA	Ambient temperature (Note 7)	-10		60	°C
VDD,AVD,AVD2	Positive supply voltage (Notes 8,9)	3.0	3.3	5.5	V
Xclk	Crystal frequency		10.368		MHz

Note 7: Within this temperature range full operation is guaranteed.
Note 8: Functional operation is guaranteed with VDD AVD up to 5.5V.
Note 9: The differences between AVD, VDD may never be more than 300mV; during a short period of time e.g. during power up more than 300mV difference is allowed.

DC electrical characteristics

AVD, AVD2, VDD = 3.3 Volt all signals are related to Vss, TA = -10°C - +60°C, crystal frequency = 10.368 MHz

Table 11: Supplies

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{VDD}	Digital supply current (pin 9 + pin 24)	• Duplex voice connection, ADPCM channel 0, codec and encryption on. • RF-clock disabled • UCLK = 81 kHz • Crystal connected • Active ECP block		6	8.5	mA
I_{AVD}	Analog supply current (pin 28)			400	700	µA
I_{AVD2}	Analog supply current (pin 52)			1.6	2.5	mA
ΔI_{VDD}	Increase of digital supply current (pin 9 + pin 24)	Second ADPCM channel active		2.0	3.0	mA
I_{VDD}		Paging mode • One active receive channel every 16 frames (Paging mode) • RF-clock disabled • UCLK = 81 kHz • Crystal connected		1.7	2.2	mA
I_{AVD}				350	450	µA
I_{AVD2}				0	10	µA
ΔI_{VDD}	Increase of digital supply current	One additional active slot (with encryption)		200	250	µA
ΔI_{AVD}	Increase of analog supply current			20	30	µA
ΔI_{AVD2}	Increase of analog supply current 2			0	0	µA

Table 12: DAC

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution			6		bits
V_{out}	Low level on DAC-pin	DAC[5:0]=00(hex)	0.39*AVD	0.4169*AVD	0.44*AVD	V
	High level on DAC-pin	DAC[5:0]=3F(hex)	0.56*AVD	0.586*AVD	0.61*AVD	V
Non-linearity	Differential				±0.5	LSB

Table 13: Peak Hold ADC (pin 31)

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution			6		bits
V_{in}	Low level on ADC-pin	ADC[5:0]=00(hex)	0.06*AVD	0.086*AVD	0.11*AVD	V
	High level on ADC-pin	ADC[5:0]=3F(hex)	0.48*AVD	0.5*AVD	0.52*AVD	V
Non-linearity	Differential				±0.5	LSB
	Integral				±1	LSB
Rin	Input impendance	ADSTBn = low	1			MΩ
		ADSTBn = high			5	kΩ

Table 14: RDI - Comparator

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{offset}	input offset voltage	Between RDI and CMPREF	-10		10	mV
I_{in}	input current	V_{IN} = 2.5 V on both RDI and CMPREF	-100	1	100	nA

Table 15: Digital Inputs (WRn/RWn, ALE/AS, RDn/En, UMC, TP1, ADSTBn, TP2, LKD, RCK, RSTn, AD[11:0], TP3, CIN, CSn, DAB[7:0], ICLK, STR0, STR1, COUT)

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IL}	Logic 0 input level				0.2*Vdd	V
V_{IH}	Logic 1 input level		0.7*Vdd			V
I_{in}	Input current	all inputs , except for TP1, TP2: Vin=0 Vin=1			10 10 125	µA µA µA

Table 16: Digital Outputs (INTn, CLK100, RFCLK, PD(7:0), MEN (3..1)n, SO,SK, ASTR, ICLK, ADOUT, COUT, STRO, STR1, CIN, HOLDn, UCLK, CLK1/3M, DAB[7:0])

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OL}	Logic 0 output level	I_{OUT} as specified below			0.5	V
V_{OH}	Logic 1 output level	I_{OUT} as specified below	VDD-0.5			V
I_{out}	Output current	PD6,7, TDO, INTn All other outputs	12 2			mA mA

AC electrical characteristics

AC characteristics VDD,AVD,AVD2 = 3.3 Volts, TA = -10°C - +60 °C, crystal frequency = 10.368 MHz

Table 17: External clock on XTAL1 pin

Parameter	Description	Conditions	Min	Typ	Max	Units
f	Input signal frequency				10.4	MHz
t_{LOW}	Duty cycle		40		60	%
V_{IL}	Logic 0 input Level				0.2*AVD	V
V_{IH}	Logic 1 input level		0.7*AVD			V
		Minimum current consumption	0.9*AVD			V

Table 18: RSTn pin

Pin name	Parameter	Conditions	Min	Typ	Max	Units
RSTn	t_{LOW}	Minimum low time to reset the device after power up	10			ms
		Minimum low time to reset the device in active mode (Note 10)	100			ns

Note 10: spikes down to 5 ns may reset the device but no proper operation is guaranteed

Table 19: ADPCM transcoder signal level control, channel 0 only

Parameter	Description	Conditions	Min	Typ	Max	Units
Gain adj.	ADPCM receiver output level	adjustment in steps of 3 dB	-36		0	dB
Sidetone	ADin0 to ADout0	independent of gain adjustment, sidetone on.		-12		dB

Table 20: ECP/CODEC interface (max 50 pF load on all outputs), see timing diagrams on page page 36

Pin name	Parameter	Conditions	Min	Typ	Max	Units
COUT, CIN	t_{SETUP}	Relative to falling edge of ICLK	25			ns
	t_{HOLD}	Relative to falling edge of ICLK	25			ns
CIN, COUT	t_{RF}	Relative to rising edge of ICLK	-25		25	ns
ICLK	1/tperiod	format 0,2,3				
		- div1	256		2048	kHz
		- div2	512		4096	kHz
		format1				
		- div1	2304		2304	kHz
		- div2	1152		1152	kHz
STR0	t_{RF0}	format1	-25		+25	ns
	t_{HIGH0}	div1 (Note 11)				
		-format 0			16	Iclk cycles
		-format 1	8		8	Iclk cycles
		-format 2		8		Iclk cycles
		-format 3		16		Iclk cycles
	$t_{PERIOD0}$		8		8	kHz
STR1	t_{RF1}	format1	-25		+25	ns
	t_{HIGH1}	div1 (Note 11)				
		format 0		32		Iclk cycles
		format 1	8		8	Iclk cycles
		format 2		8		Iclk cycles
		format 3		16		Iclk cycles
	$t_{PERIOD1}$	format 0, 2, 3	0		8	kHz
		format 1	8		8	kHz
STR0, STR1	t_{GAP}	div1 (Note 11)				
		format 1	8		8	Iclk cycles
		format 2, 3	2			Iclk cycles

Note 11: If div2 is selected the given number of Iclk cycles must be multiplied by 2.

Table 21: RFCLK pin (Note 12)

Pin name	Parameter	Conditions	Min	Typ	Max	Units
RFCLK	1 / t_{PERIOD}			10368		kHz
	t_{LOW}	duty cycle	40		60	%

Note 12: See timing diagrams on page 30 for detailed description

Table 22: RDI-comparator (see Figure 22 and 24)

Pin name	Parameter	Conditions	Min	Typ	Max	Units
RDI	t_{HOLD}	relative to rising edge RCK CMPREF level as specified (V_{in}) 50mV overdrive. (VIL,VIH)	0			ns
	t_{SETUP}		40			ns
CMPREF	V_{in}		1.25		AVD - 0.5	V

Table 23: Serial interface signals (max 50 pF load on all outputs), see timing diagram on page 32)

Pin name	Parameter	Conditions	Min	Typ	Max	Units
MEN(3..1)n	t_{LOW}	fully programmable		24 /1.152		µs
SK	1 / t_{PERIOD}			1152		kHz
	t_{HIGH}		300			ns
SO	t_{RF}	relative to falling edge SK	-25		25	ns

Table 24: Power down signals

Pin name	Parameter	Conditions	Min	Typ	Max	Units
PD(7...0)	Switching accuracy			1/1.152		µs

Table 25: TDO pin, digital mode M[1:0] = '00'

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{out}	Output current		12			mA
VOL	Logic 0 output level				0.5	V
VOH	Logic 1 output level		VDD-0.5			V

Table 26: TDO pin, Gaussian mode M[1:0] = ‘01’

Parameter	Description	Conditions	Min	Typ	Max	Units
R_{load}	Load resistance	see Figure 14	5			kΩ
$C_{parasitic}$	Load capacitance	see Figure 14			20	pF
V_{out}	Output level (Note 13)	at 0dB level (VOL[2:0]=4), 0101010....-pattern	0.81	0.911	1.02	V_{pp}
$V_{out-max}$	Maximum output level	at 0dB level (VOL[2:0]=4), 111000111000....-pattern	0.92	1.035	1.17	V_{pp}
$V_{out-adj}$	Output level adjustment		-3		+3	dB

Note 13: V_{out} is independent of supply voltage

$$R_{load} = R_1 + R_2$$

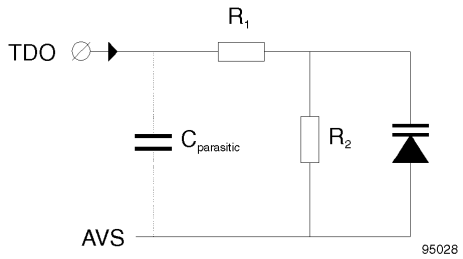


FIGURE 14. Typical application diagram

Table 27: TDO pin, Mid level mode M[1:0] = ‘11’

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{out}	Output level			1.25		V

Micro processor interface (max 30 pF load on all outputs)

Table 28: Read cycle (see timing diagram on page 37, page 38 and page 40)

Pin name	Parameter	Conditions	Min	Typ	Max	Units
AD[11:0], CSn	$t_{setup/hold}$	if ALE =1 and UMC = 0 relative to falling edge of RDn/En else relative to falling edge of ALE/AS	25			ns
ALE/AS	T_{AfRf}		0			ns
RDn/En	T_{RrRf}		110			ns
WRn/RWn	T_{WrRf}	UMC = 1	10			ns
	T_{RrWf}	UMC = 1	10			ns
HOLDn (Note 14)	T_{RfHf}				35	ns
	T_{RfHr}		190		410	ns
	T_{HrEr}		0			ns
DAB[7:0]	T_{RfD}		180		420	ns
	T_{HrD}				10	ns
	T_{DRr}		15		25	ns

Micro processor interface (max 30 pF load on all outputs)

Table 29: Write cycle (see timing diagram on page 37, page 38 and page 40)

Pin name	Parameter	Conditions	Min	Typ	Max	Units
AD[11:0], CSn	t_{setup} t_{hold} t_{setup} t_{hold}	relative to falling edge of ALE/AS	25			ns
		relative to falling edge of WRn/ RWn when ALE=1 and UMC=0	25			ns
DAB[7:0]	$t_{setup/hold}$	relative to rising edge of : • WRn/RWn if UMC=0 and RDn/En=1 • RDn/En if UMC=1 and WRn/RWn=0	20			ns
ALE/AS	T_{AfWf} T_{HrAf}		0 0			ns ns
RDn/En	T_{RfRr}	UMC = 1, WRn/RWn = 0	110			ns
	T_{RrRf}	UMC = 1	110			

Table 29: Write cycle (CONTINUED) (see timing diagram on page 37, page 38 and page

Pin name	Parameter	Conditions	Min	Typ	Max	Units
WRn/RWn	T_{WfWr}	UMC = 0, RDn/En = 1	110			ns
	T_{WrWf}	UMC = 0	110			ns
	T_{WfRf}	UMC = 1	10			ns
	T_{RrWr}	UMC = 1	10			ns
HOLDn (Note 14)	T_{WrHr}		210		410	ns
	T_{WrHf}	relative to rising edge of • WRn / RWn if UMC = 0 • RDn/En if UMC = 1			35	ns

Note 14: HOLDn pin can be used to extend read / write cycle in the case of a faster microprocessor. In case the write cycle is not completed and the chip is addressed again the HOLDn is pulled low. The read cycle will be extended till after this write cycle is completed.

Table 30: Microphone amplifier

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{in_0dB}	Differential input voltage between MIC+ and MIC-	0dBm0 on COUT (Note 15) MIC-gain[3:0] = 0, @ 1020 Hz	225	300	375	mVrms
A	Gain	N * 2dB steps (N=1..15)	(N*2)-0.7	(N*2)	(N*2)+0.3	dB
R_{in}	Differential input impedance between MIC+ and MIC-	MIC GAIN[3:0] = 0..10 MIC GAIN[3:0] = 11 MIC GAIN[3:0] = 12 MIC GAIN[3:0] = 13 MIC GAIN[3:0] = 14 MIC GAIN[3:0] = 15	16.0 13.0 10.2 8.0 6.5 5.0			kΩ kΩ kΩ kΩ kΩ kΩ

Note 15: 0 dBm0 on COUT = -3.14 dB of max. PCM value

Table 31: Loudspeaker amplifier

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{out_0dB}	Differential output voltage between LRS+ and LRS-	0dBm0 on CIN (Note 16) LRS[3:0] = 0, @ 1020 Hz Load circuit A with $R_{L1}=\infty$, C_{P1} as specified below	0.85	1.15	1.45	Vrms
V_{out_-6dB}	Single ended output voltage between LRS+ and AVS	-6dBm0 on CIN (Note 16) LRS[3:0] = 0, @ 1020 Hz Load circuit C with $R_{L3}=\infty$	0.425	0.575	0.725	
A	Attenuation	N * 1dB steps (N=1..15)	N - 0.5	N	N + 0.5	dB
R_{out}	Differential output impedance between LRS- and LRS+			50	tbd	Ω
CP_1	Load capacitance	see Figure 15 • $R_{L1} > 1$ kΩ • 600Ω < $R_{L1} \leq 1$ kΩ			30 100	pF pF
R_{L1}	Load resistance		600			Ω
C_{P2}	Parallel load capacitance	see Figure 17			30	pF
C_{S2}	Serial load capacitance		10		100	nF
R_{L2}	Load resistance		600			Ω
R_L3	Load resistance		10K			Ω

Note 16: 0 dBm0 on CIN = -3.14 dB of max PCM value

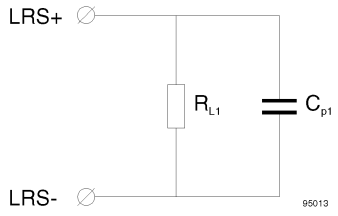


FIGURE 15. Load circuit A (dynamic loudspeaker

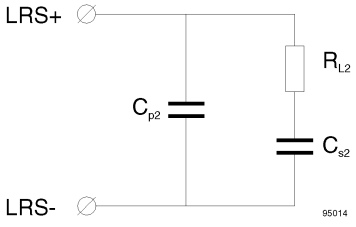


FIGURE 16. Load circuit B (Piezo loudspeaker)

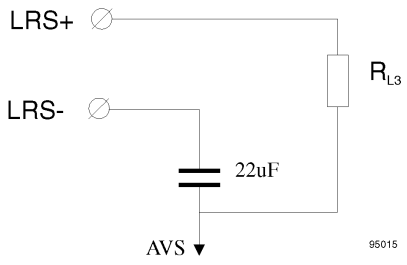


FIGURE 17. Load circuit C (single ended)

Table 32:Reference circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
$\Delta(V_{REF+} - V_{REF-})$		I_{LOAD} = 0 mA	2.2	2.5	2.8	V
C_{load}	Load capacitance	see Figure 18	2.0			µF
R_{out}	Differential output resistance between VREF+ and VREF-			20	tbd	Ω
I_{load}	Differential output current				2	mA
	Vref noise	• differential measured between Vref+/Vref- • CCITT weighted		-90	-80	dBVp

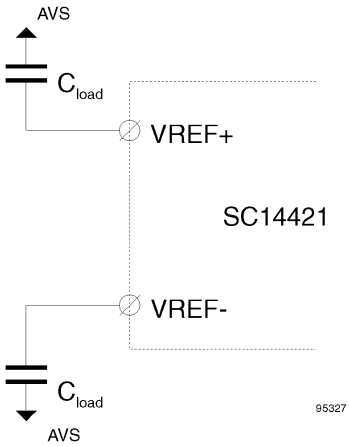


FIGURE 18. Reference circuit decoupling

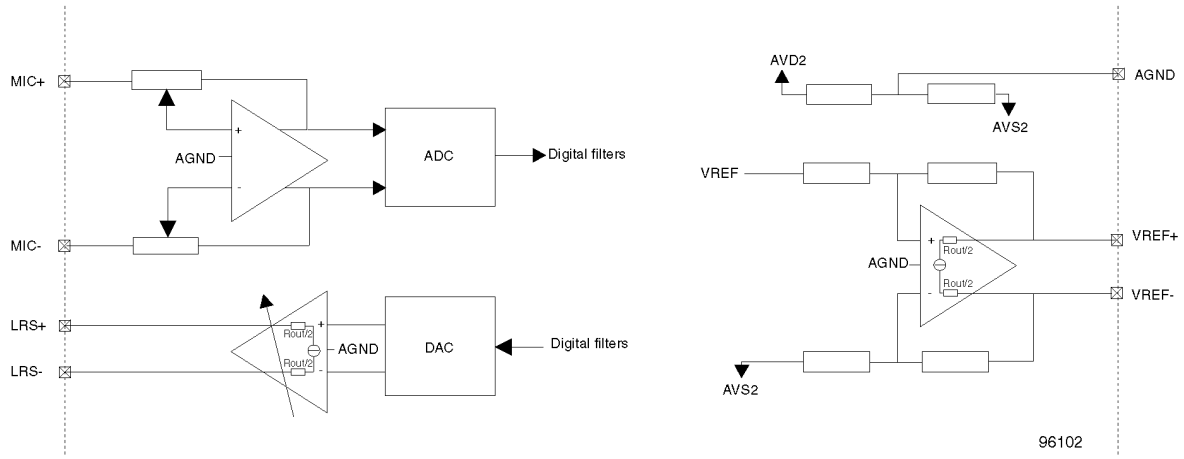


FIGURE 19. Analog frontend block diagram

Table 33:CODEC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
S/D_{AD}	Signal to total distortion ratio Analog/ Digital	• see measurement diagram (Figure 20), R_{ab}= ∞ • CCITT weighted • differential input signal between MIC+ and MIC- with f=1020Hz • ADPCM transcoder active • MICGAIN[3:0] = 0 • ECP in transparent mode 1) 0 dBm0 on COUT (see note 17) 2) -40 dBm0 3) -45 dBm0	 40 35 30	 45		 dB dB dB
S/D_{DA}	Signal to total distortion ratio Digital/ Analog	• see measurement diagram (Figure 21) • CCITT weighted • differential input signal between MIC+ and MIC- with f=1020Hz • ADPCM transcoder active • LRSGAIN[3:0] = 0 • ECP in transparent mode 1) 0 dBm0 on ADIN (see note 17) 2) -40 dBm0 3) -45 dBm0	 40 35 30	 50		 dB dB dB
$NOISE_{AD}$	Idle channel noise Analog/ Digital	• see measurement diagram (Figure 20, R_{ab} = 0 Ohm) • CCITT weighted • Relative to 0 dBm0 (see note 17) • MICGAIN[3:0] = F • ECP in transparent mode		-80	-72	dBmp
$NOISE_{DA}$	Idle channel noise Digital/ Analog	• see measurement diagram (Figure 21) • CCITT weighted • Relative to 0 dBm0 (see note 17) • LRSGAIN[7:4] = 0 • ECP in transparent mode		-83	-80	dBmp
FREQ. RESP. AD	frequency responce Analog/ Digital	• see measurement diagram (Figure 20), R_{ab} = ∞ • relative to 1020 Hz • ECP in transparent mode	see frequency response diagram (Figure 22)			
FREQ. RESP. DA	frequency responce Digital/ Analog	• see measurement diagram (Figure 21), R_{ab} = 1 kOhm • relative to 1020 Hz • ECP in transparent mode	see frequency response diagram (Figure 23)			

Note 17: 0 dBm0 on COUT = -3.14 db of max. PCM value

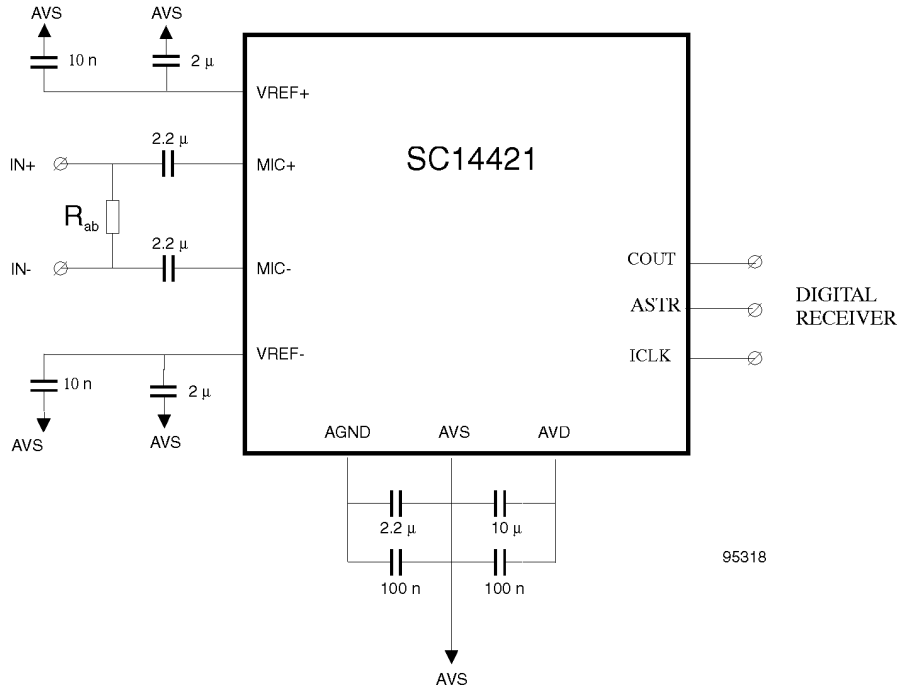


FIGURE 20. CODEC Measurement Diagram, analog to digital

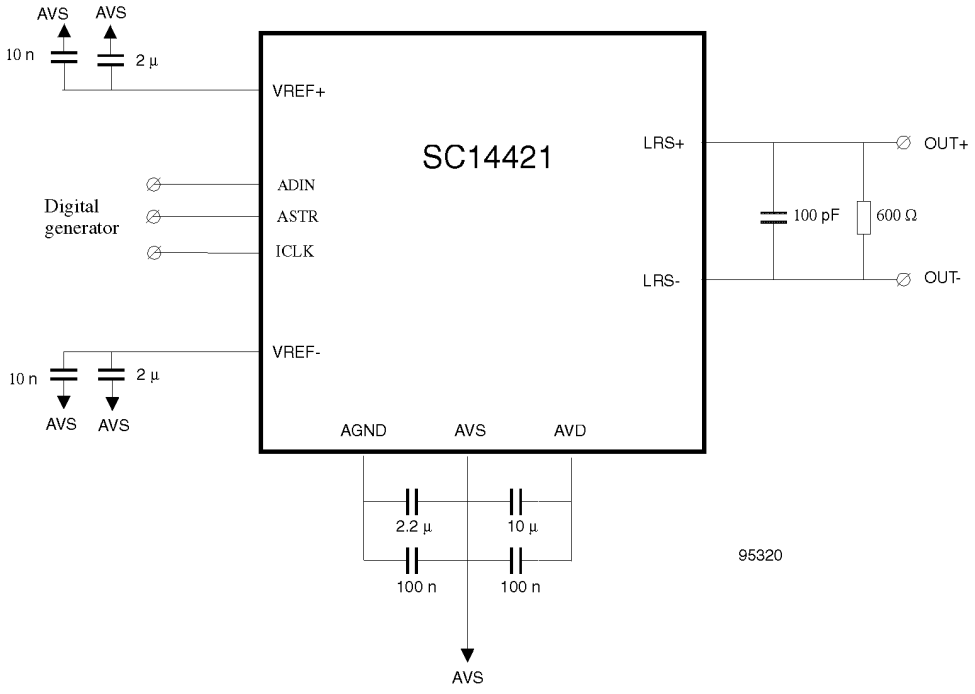


FIGURE 21. CODEC Measurement Diagram, digital to analog

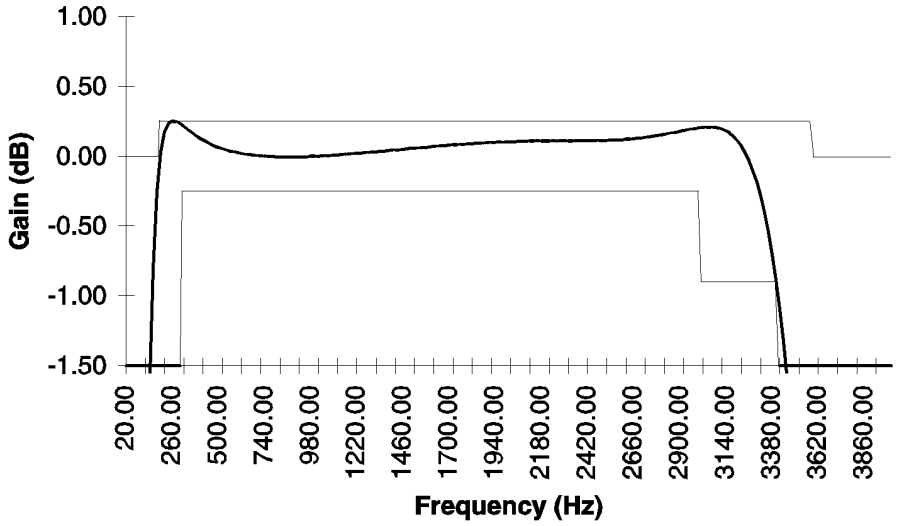


FIGURE 22. CODEC Frequency Response, analog to digital

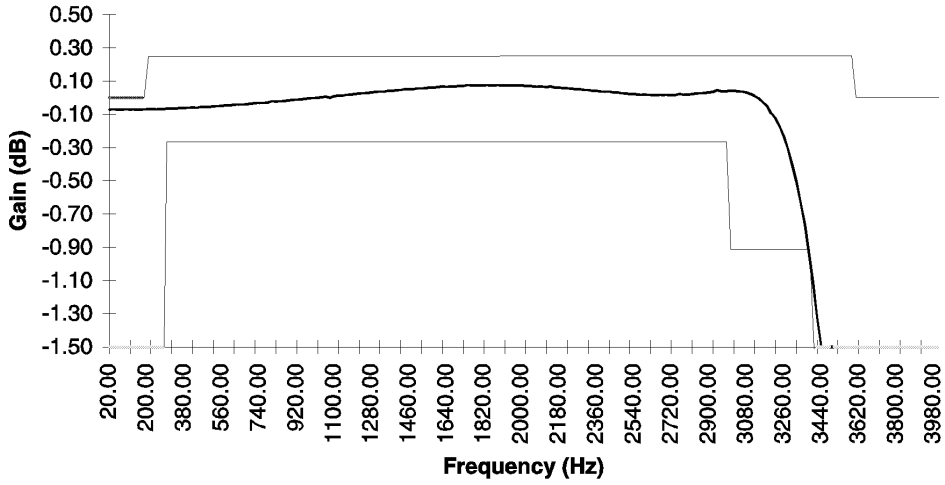


FIGURE 23. CODEC Frequency Response, digital to analog

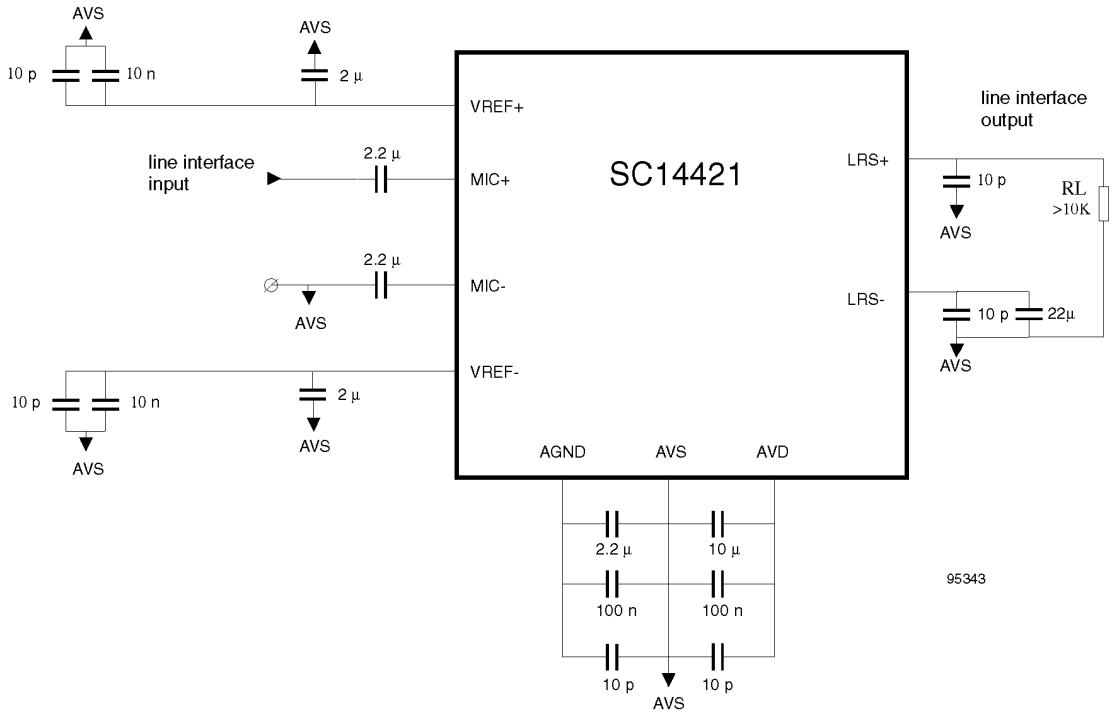


FIGURE 24. Line Interface Application Diagram

RCK_int software instruction the internal clock is selected.

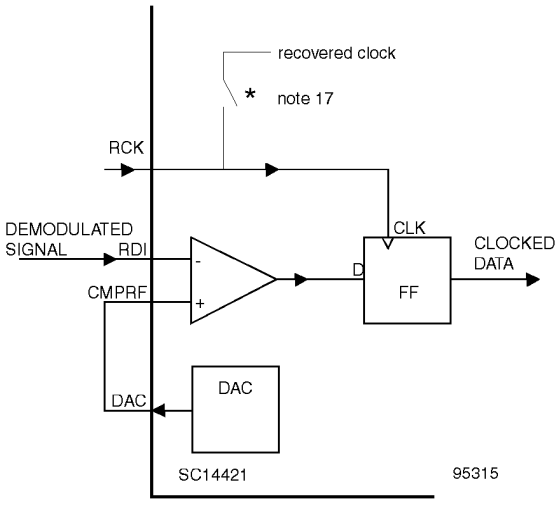


FIGURE 25. RDI Input circuitry

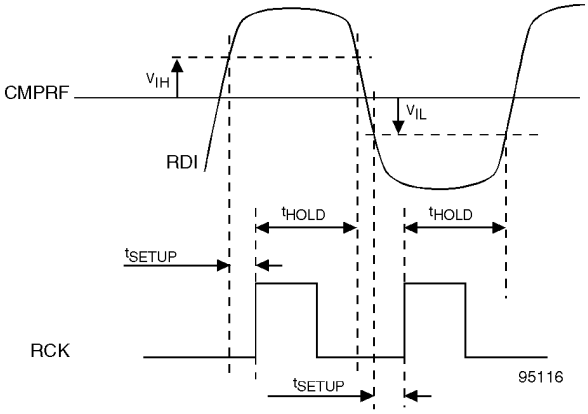


FIGURE 26. RDI Timing diagram

Note 18: It is recommended to use to internal recovered clock. With the

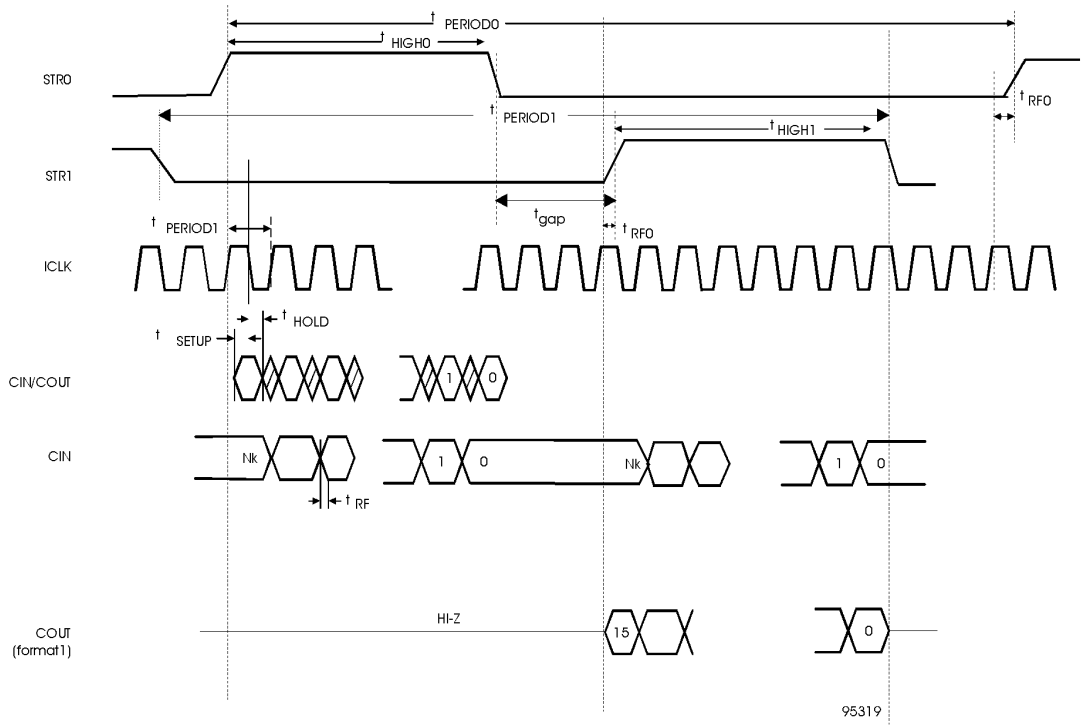


FIGURE 27. ECP / CODEC interface

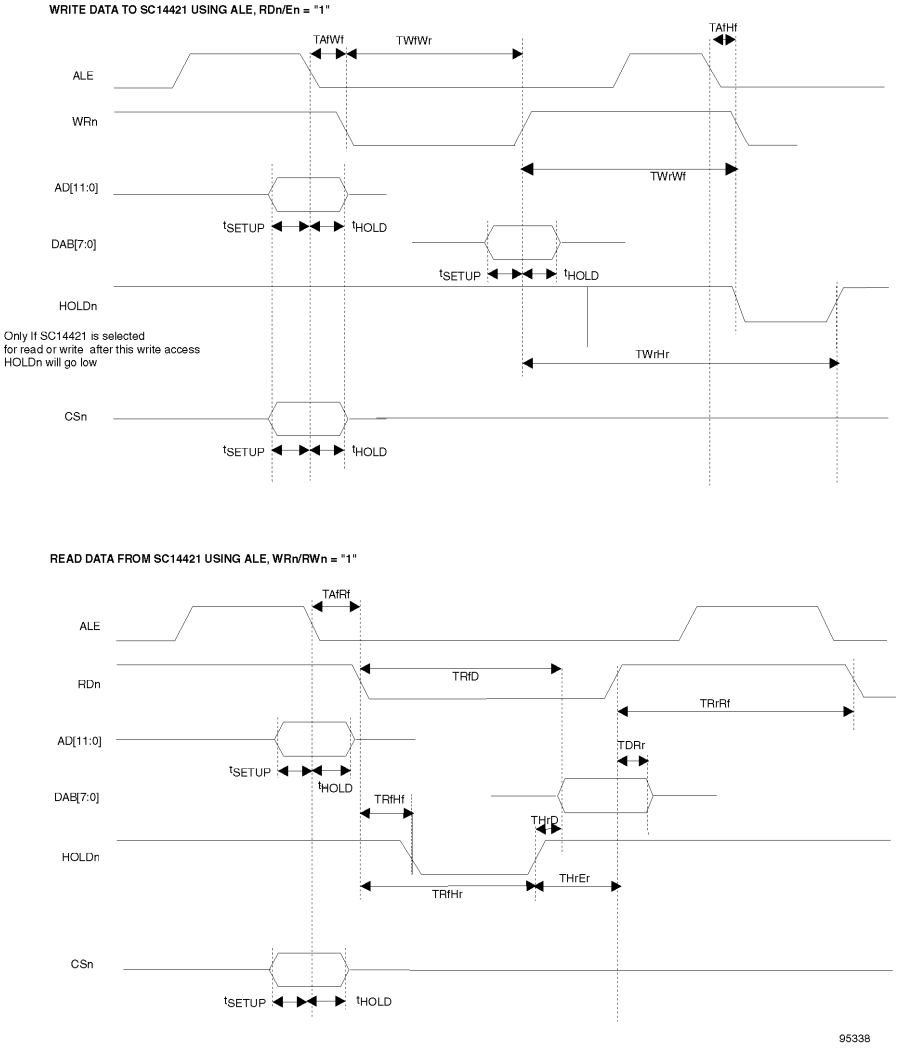


FIGURE 28. Processor Interface - Mode I (UMC = 0)

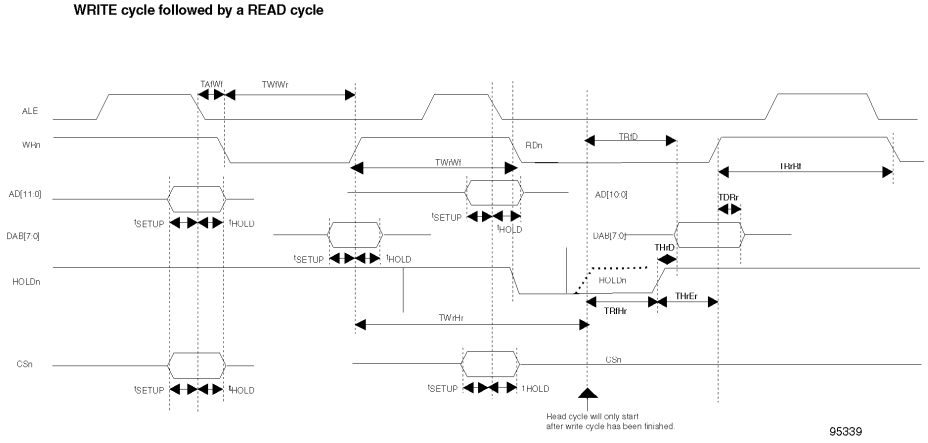


FIGURE 29. WRITE cycle followed by a READ cycle

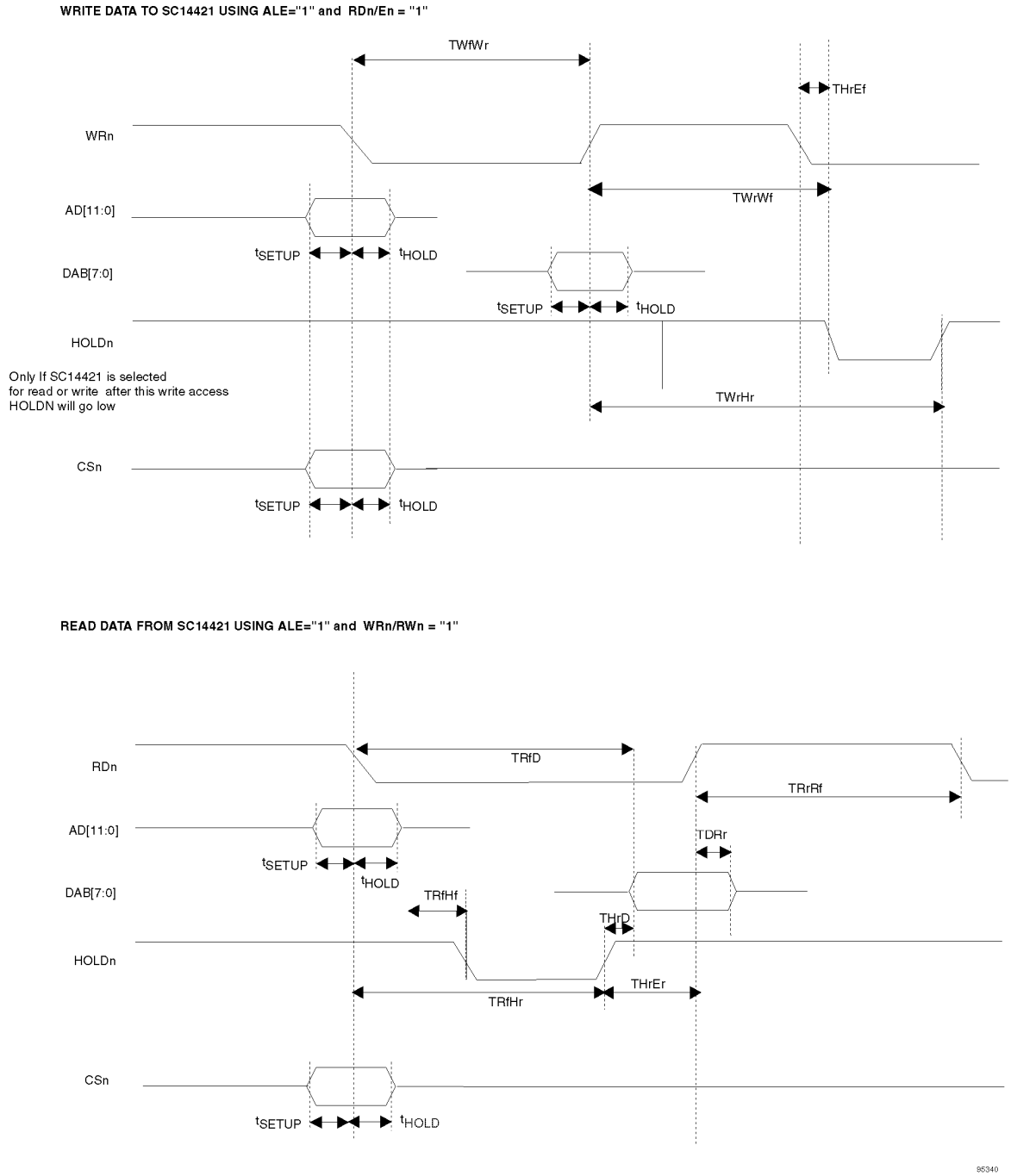


FIGURE 30. Processor Interface - Mode I (UMC = 0)

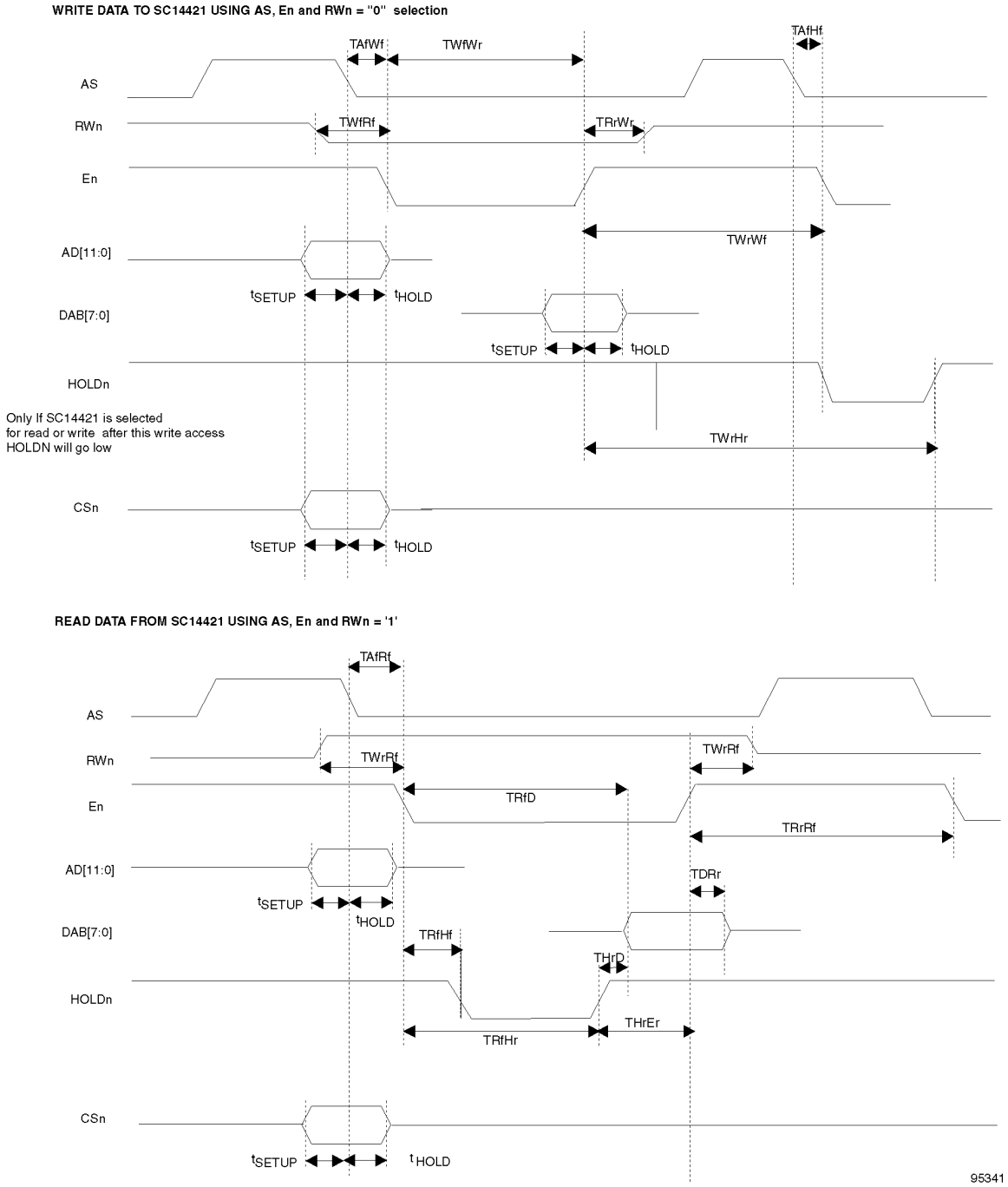


FIGURE 31. Processor Interface - Mode II (UMC = '1')

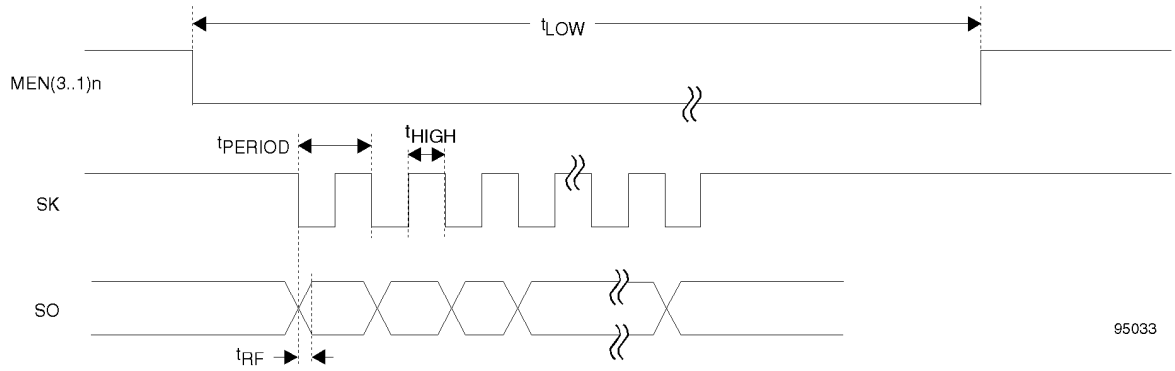


FIGURE 32. Serial Interface

Physical dimensions - INCHES (Millimeters)

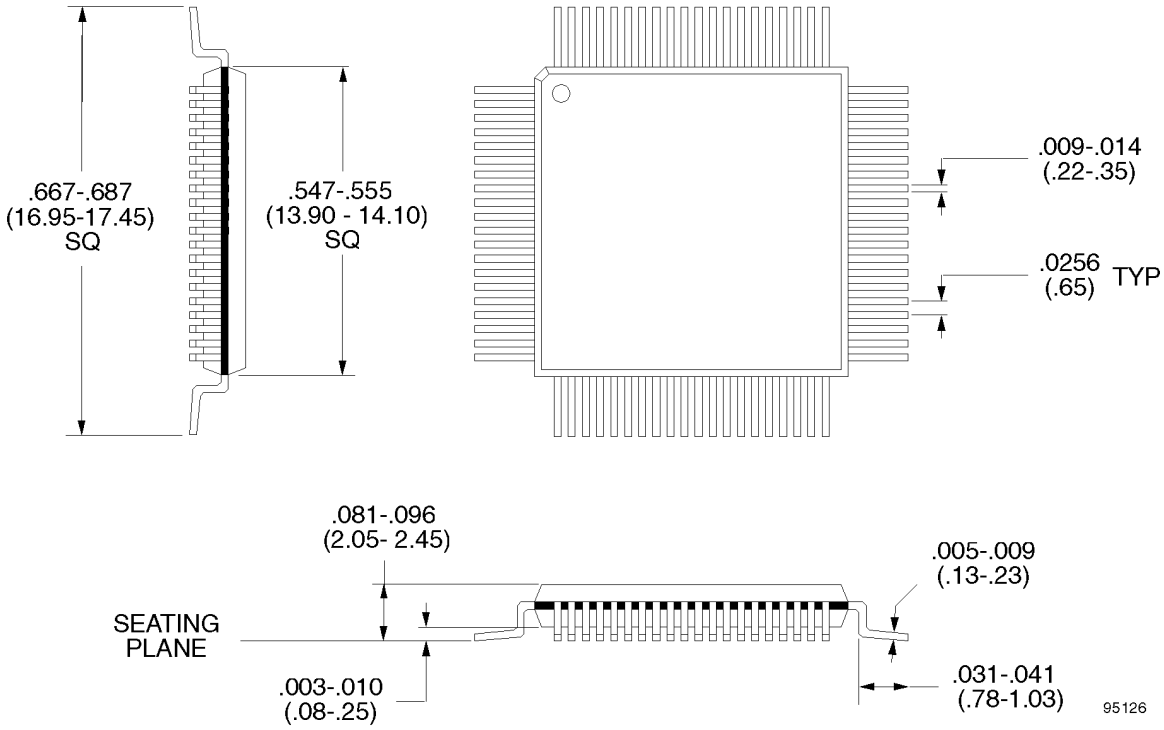


FIGURE 33. Package 80-Pin Quad Flat Pack

Product status definitions

Definition of Terms

Data sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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