LMX4181
Radio Transceiver with integrated PA for DECT

The LMX4181 is a radio transceiver including an RF power amplifier integrated circuit optimized for the Digital Enhanced Cordless Telecommunications (DECT) system. The transceiver, when combined with a a Tx/Rx switch, implements a complete radio transceiver compliant for DECT & DECT 6.0 CAT-iq and Korean DECT handsets and basestations. The LMX4181 interfaces to SiTel Semiconductor's SC144xx DECT family of baseband processors.

The LMX4181 includes a complete transmitter, consisting of a phase locked loop with fully integrated VCO and RF PA. The receiver contains LNA, quadrature downconverter, polyphase IF filter/combiner, automatic gain control, and digital demodulator.

Features

- Complies with DECT ETS 300 175-2,3 & 8 and DECT 6.0 and Korean DECT (1.7 GHz)
- 1.9 - 3.45 V battery operation range
- Easy decoupling of only 2 supply pins
- On-chip timing control
- Microwire™ interface to baseband processor. (Slave transmit and receive).
- Radio transceiver
  - Integrated 1.9 GHz/1.7 GHz CMOS transceiver
  - <70 µs RF PLL lock time
  - Four digital output ports (including two for fast antenna diversity switching)
  - -96 dBm receiver sensitivity
- Integrated 1.9 GHz PA for DECT and Korean DECT
  - High Power Mode EU (HPM): 25.5 dBm
    High Power Mode USA (HPM/U): 23.5 dBm
    Low Power Mode (LPM) 12 dBm
    'Green' Mode (GPM): 4 dBm
    Low Radiation Mode (LRM): -35 dBm
  - Output power ramp and flatness control
- Small 32 pin lead less package (VQFN)

Note 1: Microwire™, is trademark of National Semiconductor.

System Diagram

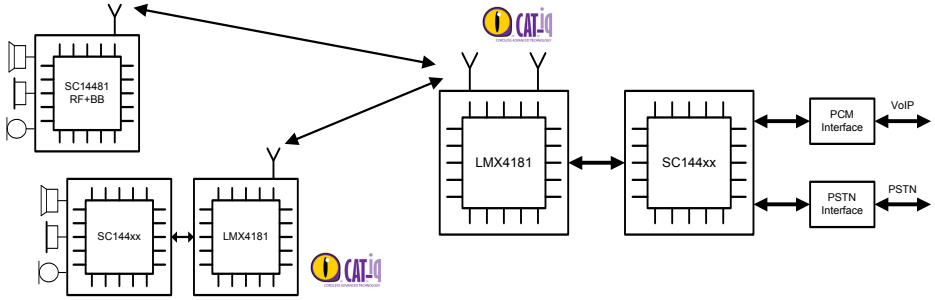
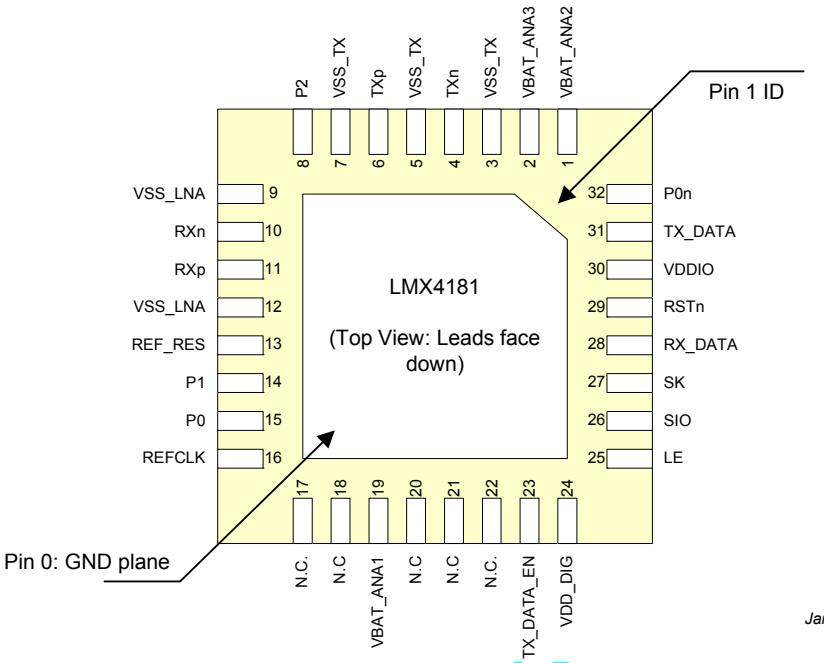


Table of Contents

1.0 Connection Diagram



Order Number: LMX4181AQXN
Package Number VQFN-P 32L (5.0×5.0 mm) (see page 44)

Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 1)	DESCRIPTION
GND plane	-	-	I-PU	Ground
Radio transceiver				
RXp RXn	A9	-	I	INPUT. RF Receiver inputs.
VSS_LNA	A9	-	I	LNA Ground
TXp TXn	A10	-	O	OUTPUT. RF PA outputs. Must be connected to PA_SUPPLY by external matching circuit. SPoB Prematching with capacitors under discussion.
VSS_TX	A9	-	I	PA Ground
REF_RES	A7	-	O	Connection for bias resistor to ground (56kΩ). For stability the maximum parasitic load on this pin may not exceed 10 pF.
P0	D2	8	Hi-Z	Digital outputs supplied with internal RF LDOs. (1.7V) If the RF LDOs are not enabled, the output of these port can not be used. Refer to Table 62 on page 39
P0n	D2	8	Hi-Z	
P1	D2	8	Hi-Z	
P2	D2	8	Hi-Z	
Microwire and digital interface				
LE	DI	-	-	INPUT. Microwire latch enable
SK	DI	-	-	INPUT. Microwire clock
SIO	DIO	2	I	INPUT/OUTPUT. Microwire data

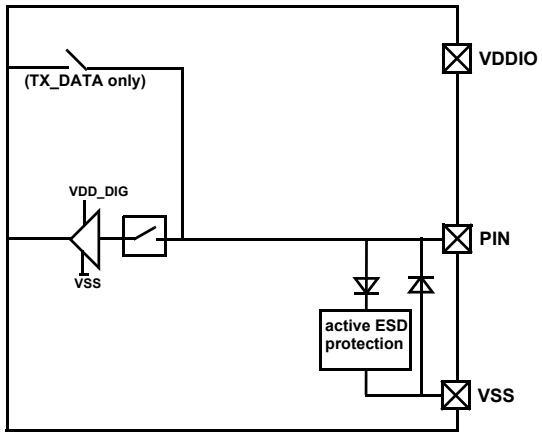
Table 1: Pin Description

PIN NAME	TYPE	Drive (mA)	Reset state (Note 1)	DESCRIPTION
TX_DATA	DI/AI	-	AI	INPUT. Transmit Data.
TX_DATA_EN	DI	-	I	INPUT. Transmit Data Enable. TX_DATA_EN is only used when TX_DATA_MODE = 2. For all other values of TX_DATA_MORE, TX_DATA_EN shall be connected to ground.
RX_DATA	DO	2	O-1	OUTPUT. Receive Data
REFCLK	DI	-	I	INPUT. Digital reference clock.
Power and supply				
RSTn	DI	-	I	INPUT/OUTPUT. Active low Reset input with Schmitt trigger input.
VBAT_ANA1 VBAT_ANA2, VBAT_ANA3	A7			INPUT RF transceiver supply voltage 1.9V-3.45V. Connected to VBAT if <3.45V. VBAT_ANA1, VBAT_ANA2 must be connected together (preferably directly to the 2-cell battery). In case 3.45V<VBAT<5.5V (E.g. Li-Ion) these pins to the external LDO_RF NPN transistor. VBAT_ANA 2 (top) supplies LDOs for image reject mixer, RF port P0n, RF port 2, LNA, VCO, Phase frequency detector VBAT_ANA 1 (left) supplies LDOs for IF filter, RX ADC, RF ports 0 and 1, frequency divider, MMC, LDO Xtal. VBAT_ANA 3 (top) supplies LDO for the PA
VDD_DIG				INPUT Supply voltage for the digital core (1.8V typical)
VDDIO				INPUT Supply voltage (1.8 to 3.45 V) for digital IOs RSTn, REFCLK, RX_DATA, SIO,LE, SK, TX_DATA and TX_DATA_EN.

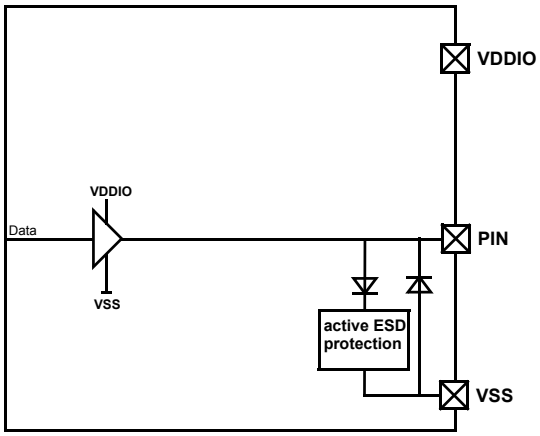
Note 1: All digital inputs have Schmitt trigger inputs. After reset all I/Os are set to input.
I = input, O=output, Hi-Z= high impedance, 1= logic HIGH level, 0= logic LOW level

1.1 PIN TYPE DEFINITIONS

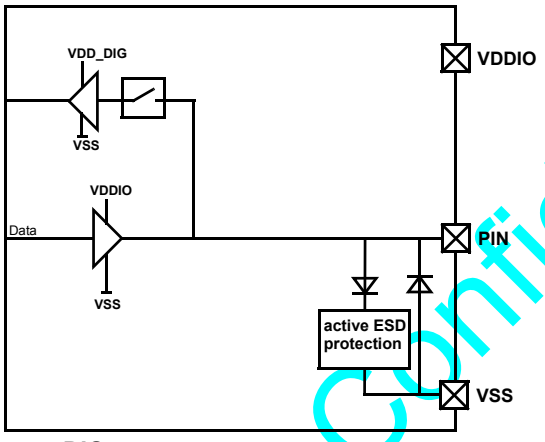
Table 2: PIn type definitions



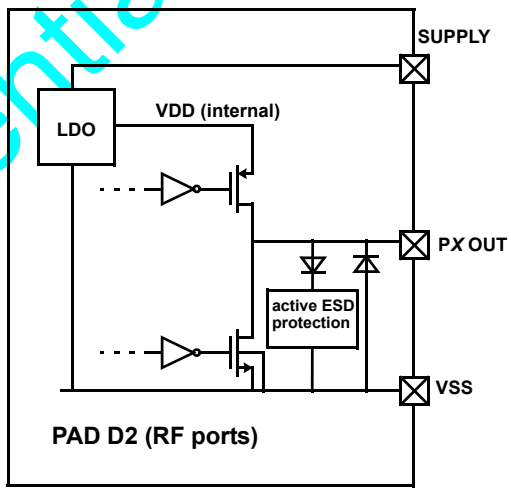
PAD DI/AI



DO

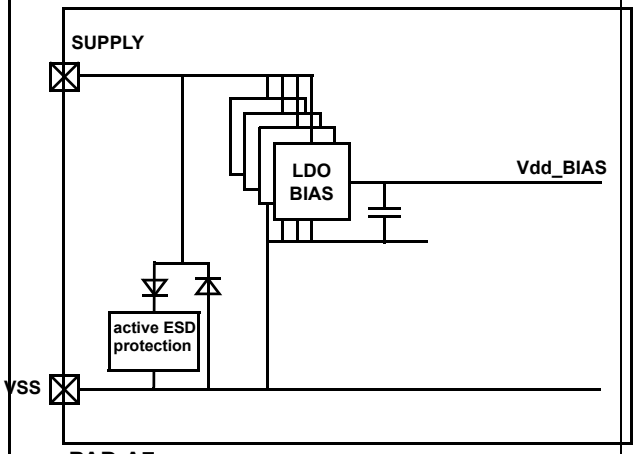


DIO

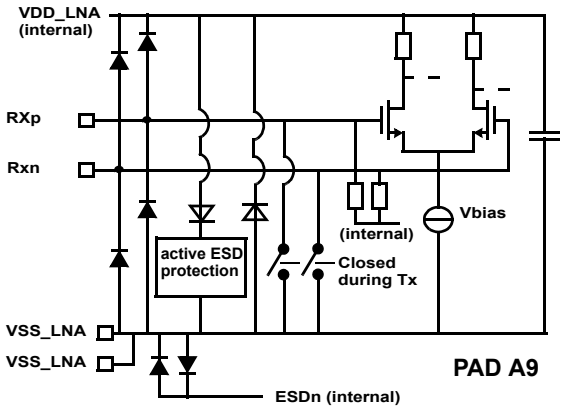


PAD D2 (RF ports)

Table 2: PIn type definitions



PAD A7



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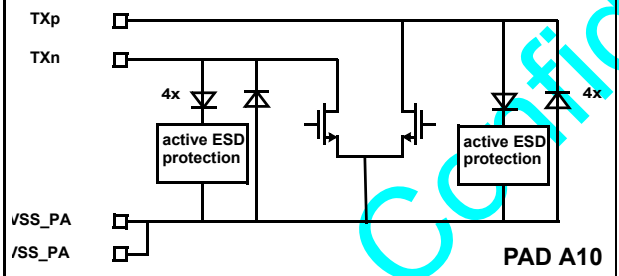

PAD A10

2.0 Functional overview

The LMX4181 is a complete DECT radio transceiver integrated, designed to perform the complete receive function without an external SAW filter at IF. For transmit, an RF Power Amplifier (PA) has been integrated. Furthermore, the device includes a fully integrated fractional-N PLL used for both transmit and receive functions. The device is designed to operate the frequency synthesizer in a closed loop fashion in both transmit and receive mode.

The operation of the radio transceiver can be divided into three distinct tasks:

- Set-up of the desired functionality,
- Locking the frequency synthesizer, and
- Performing the desired transmit or receive function.

All functions are controlled by programming the MICROWIRE™ interface of the device.

Before transmission or reception of a data slot, the frequency synthesizer is locked to the desired frequency. When locked, the transmit or receive functions are switched on automatically at a predefined (user-configured) time.

During transmit mode, a data signal is provided by a baseband processor IC to the TX_DATA pin. The PA provides the RF signals to an off-chip matching circuit.

During receive mode, the signal at the Rx input is downconverted to an intermediate frequency (IF = f_{REFCLK}/12) of 864kHz. At IF, blocking signals and noise are attenuated and the wanted signal is amplified to a sufficient level using an AGC amplifier. Thereafter the signal is demodulated, and the data signal is recreated, along with a received signal strength indication (RSSI) signal

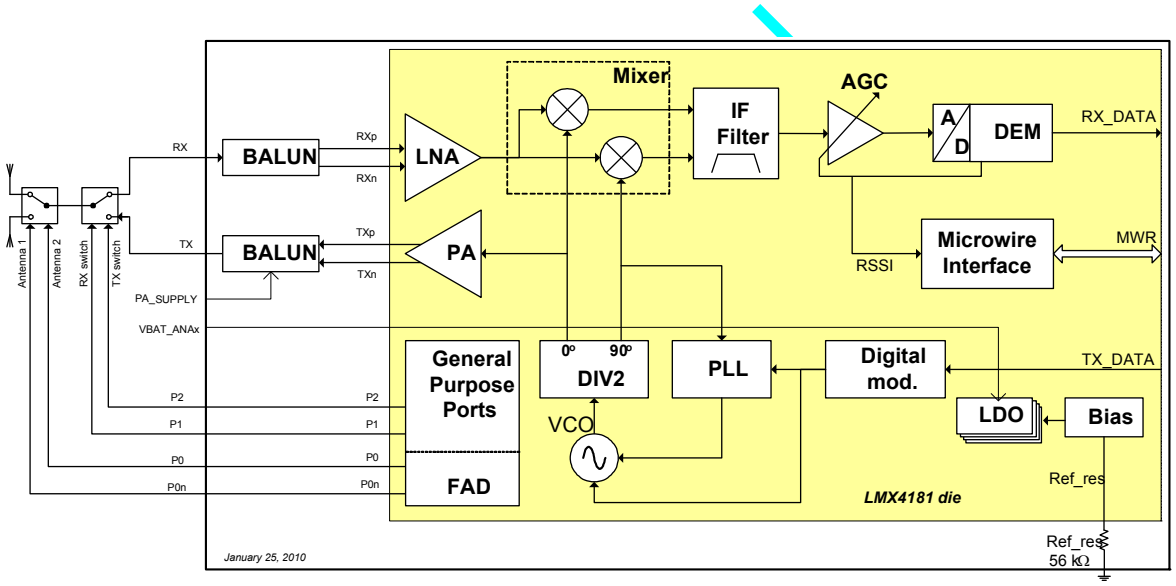

Figure 1 Radio Transceiver Block Diagram

2.1 FREQUENCY SYNTHESIZER

The fractional-*N* frequency synthesizer embodies an automatic VCO calibration, tuning and modulation mechanism. The VCO Calibration can be performed on a slot to slot basis, preceding phase lock. It is also possible to perform VCO calibration beforehand and providing the calibration information along with the desired channel. The reference frequency is the crystal oscillator frequency, which can be either 10.368 MHz or 20.736 MHz. The divide ratios (*N*) that set the output frequency to a transmit channel or a receive LO frequency value (which combined form a 864 kHz grid) may therefore be fractional. Furthermore, the modulation is injected while the synthesizer is in closed-loop using two-point modulation. The two modulation points are the VCO and the frequency divider.

2.1.1 PLL

The fractional-*N* synthesizer is implemented using a multi-modulus counter (frequency divider), a tri-state phase-frequency detector a high performance active loop filter and digital control circuitry. For convenience (refer to Figure 1) these blocks are indicated with the term *PLL*. The complete loop including the VCO and frequency divider is indicated with the term *synthesizer*. The multi-modulus counter divides the LO frequency by an integer value *N* (in the range of 180 when the reference frequency is 10.368 MHz), which is provided by a ΣΔ-modulator. The ΣΔ-modulator generates a sequence of *N* values such that the average

$$N_{avg} = (f_{LO} + f_{mod,dig}) / f_{REFCLK} \quad , \qquad (1)$$

where f_{LO} is the local oscillator as defined by equation (2) in section 4.1, $f_{MOD,DIG}$ is digital modulation from the Gaussian pulse shaper (which is non-zero in TX mode) and f_{REFCLK} is the reference clock frequency.

Through its 3rd order MASH design the ΣΔ-modulator shifts the quantisation noise primarily to higher frequencies, which is subsequently filtered out of the VCO control signal by the fully integrated loop-filter.

The Gaussian shaped TX data is added to the input of the ΣΔ-modulator and to the second VCO input. These 2 points provide the lower and higher frequency ranges of the TX spectrum, respectively and their crossover point is given by the bandwidth of the PLL. Both paths of the two-point modulation must have equal gain which is automatically optimized by the modulation gain calibration algorithm.

2.1.2 VCO

The VCO is fully integrated and operates at twice the required frequency. An automatic calibration mechanism is implemented to compensate fabrication tolerances. The VCO is powered by an internally regulated supply.

2.1.3 Frequency Divider

A frequency divider (DIV2) is implemented to allow the VCO to run at a different frequency than the incoming/outgoing RF signal frequency and hence prevent load pulling due to activation of the internal PA. In receive mode it provides the I/Q generation of the LO signal that is used in the quadrature down converter.

2.2 RADIO TRANSMITTER

Transmission is accomplished by closed-loop modulation. The digital modulator oversamples and filters the data bits and provides a digital version of the data to the ΣΔ-modulator and an analog version to the VCO. The frequency deviation can be programmed in software. The modulated output frequency of the VCO is divided by 2 in order to down convert to the required transmit frequency. The integrated Power Amplifier (PA) is enabled just before the transmit slot becomes active, providing the necessary isolation for a good transmit mask.

2.3 INTEGRATED POWER AMPLIFIER

The integrated Power Amplifier (PA) consists of a 2 stage power amplifier and a variable attenuator stage. The PA, when combined with a proper output matching network and a Tx/Rx switch, is compliant with the ETSI EN 301406 standard.

PA features

- High Power Mode EU (HPM): 25.5 dBm
  High Power Mode USA (HPM/U): 23.5 dBm
  Low Power Mode (LPM) 12 dBm
  'Green' Power Mode (GPM): 4 dBm
  Low Radiation Mode (LRM): -35 dBm
- Power flatness, ramping and gain control
- Differential Output
- 1.9 - 3.45V operation range (PA_SUPPLY)

The PA output is differential. By means of a balun the output can be made single-ended. This balun also performs the required output matching of the PA (See Figure 2).

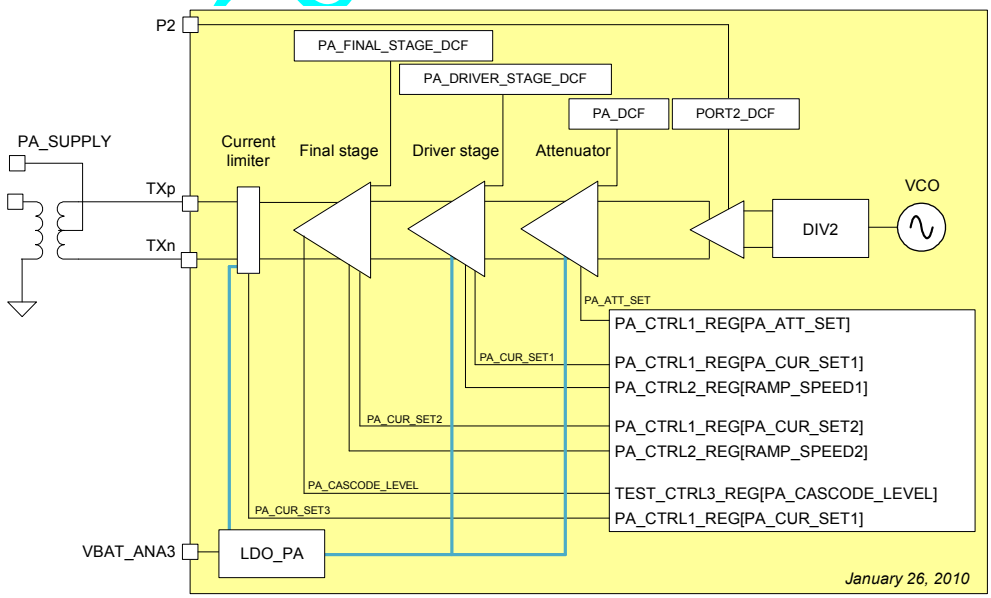

Figure 2 PA block diagram

The PA has two voltage supplies:

- VBAT_ANA3 to supply the LDO_PA. This pin is common for all transceiver blocks.
- PA_SUPPLY which supplies the TXp and TXn open drains via the matching network.
  The voltage range is 1.9 to 3.45 V. In case of a two cell battery supply this pin is directly connected to VBAT_ANA2. In case of a Li-Ion battery supply, an external LDO supplies this pin.

2.3.1 PA power mode settings

The PA gain and PA stage biasing is controlled through the PA_CTRL1_REG register. It is recommended to store/update the registers on a slot by slot basis during the settling time of the radio synthesizer.

A list of preferred register settings for each power mode is given in Table 3. This table is based on typical measurements performed on the SiTel evaluation board with the recommended output matching network. The customer is free to choose a different output power mode level for each power mode by changing the content of the registers. Note that changing the PA_CUR_SET1 or PA_CUR_SET2 settings might influence the PA specifications as given in Table 68.

2.3.2 PA power ramping and DCF timing

The DCF timing for the PA is provided through the following DCF registers (See Figure 3):

- PA_DCF_REG enables the PA.
- PORT2_DCF_REG enables the Divider buffer towards the PA and the external TX switch via P2. Note that both signals are 'active high'.
- PA_DRIVER_STAGE_DCF_REG enables the ramp start and stop of the PA **first** stage.
- PA_FINAL_STAGE_DCF_REG enables the ramp start and stop of the PA **final** stage.

The speed, at which the power ramps up or ramps down, is controlled through the PA_CTRL2_REG register. The ramp speed of the first stage and final stage is controlled separately for maximum flexibility. Note that when the ramp speed of one or both stages is changed, the RESET_OFFSET of the modified PA stage(s) should be adjusted to fit the power template (See Figure 3).

2.3.3 Output Power flatness control

Figure 4 shows a typical output power characteristic as a function of PA_SUPPLY (VBAT) and PA_ATT_SET setting value 0 (minimum attenuation) to 15 (max attenuation) without any power flatness control. When an even flatter output power level versus PA_SUPPLY behaviour is required, the PA can be provided with a software controlled output power flatness. The software should measure and average the battery voltage VBAT during an active Tx slot using an external ADC. When VBAT exceeds a certain predefined limit, a different attenuation setting should be programmed for the next slot to achieve the required power flatness. For more information refer to *AN-D-169 "SC14481 RFPA Output Power control"*.

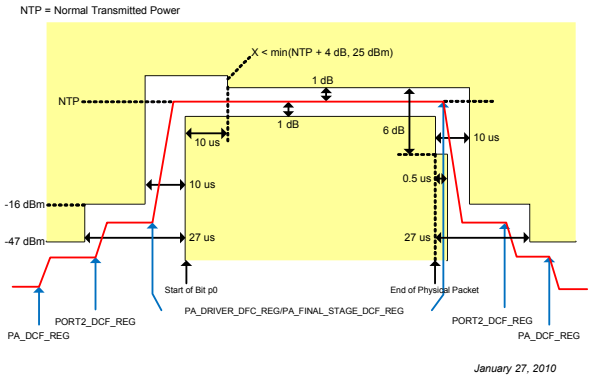

Figure 3 PA power ramping and DCF timing

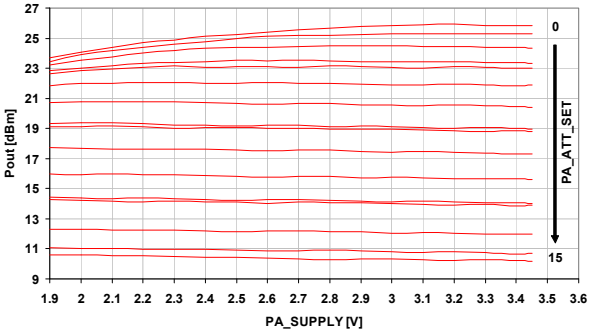

Figure 4 PA output power level versus VBAT and PA_ATT_SET setting (for reference only)

Table 3: PA preferred register settings for various power modes.

Power mode	HPM	HPM	HPM/U	LPM	GPM	LRM
Pout (dBm)	25.5 (VBAT<=3V)	25.5 (VBAT>3V)	23.5	12	4	-35
PA_CTRL1_REG	0x0F80		0x4840	0x9720	0xD630	0x7410
TEST_MODE2_REG	0x005F	0x005F	0x0068	0x0068	0x0068	0x0068
TEST_CTRL3_REG	0x0380	0x0380	0x0380	0x0390	0x0390	0x03A0

2.4 TX_DATA INTERFACE

The TX_DATA input on a LMX4181 can either be an analogue input containing a PAM modulated signal or a digital bit stream.The analogue input can be the TDO output from a SiTel baseband controller or any other device that generates a PAM modulated signal with a mid-level of typical 900 mV. This mode is typically used for applications where the LMX4181 replaces a LMX4180 device and the interface is required to be backwards compatible. The digital bit stream can be used in conjunction with an enable signal, an internal DCF (see Section 3.3) or with a start embedded in the digital bit stream. These modes are typically used for applications where the baseband controller only has a digital interface or the analogue interface is switched off which leads to a lower power consumption.

The mode is selected with the field TX_DATA_MODE in the register TX_DATA_CTRL_REG.

Analogue TX_DATA (TX_DATA_MODE = 0)

The TX_DATA interface detects the bits to be transmitted on the analogue TX_DATA signal with the use of two comparators that compare the analogue signal level with two threshold that are place just below and above the mid-level. TX_DATA is sampled with the symbol rate after the first bit on TX_DATA has been detected, i.e., one of the two comparator outputs is high. The end of packet is detected by that both comparator outputs are low.

DCF (TX_DATA_MODE = 1)

The first bit to be transmitted and last bit to be transmitted on TX_DATA are detected by the rising and falling edges of the TX_DATA_DCF DCF, respectively. The length of the active period for TX_DATA_DCF must equal the number of symbols in the packet.

TX_DATA_EN (TX_DATA_MODE = 2)

The first bit to be transmitted and last bit to be transmitted on TX_DATA are detected by the rising and falling edges of the input signal TX_DATA_EN, respectively. The period where TX_DATA_EN is asserted must equal the number of symbols in the packet.

Start bit detection (TX_DATA_MODE = 3)

It is for this mode required that the baseband controller inserts a bit before the first bit to be transmitted with the inverse value of the first bit. The first bit to be transmitted is detected by a rising or falling edge on the digital TX_DATA signal. The edge detection is gated with the DCF TX_DATA_DCF. The length of the active period for TX_DATA_DCF must equal the number of symbols in the packet.

The time between the detected of the first bit and the sample moment at symbol rate is programmable with the field TX_DATA_DELAY in the register TX_DATA_CTRL_REG.

2.5 RADIO RECEIVER

The receiver consists of an LNA and a quadrature downconversion mixer converting the desired channel to IF. At IF the signal is filtered and an automatic gain control (AGC) circuit adjusts the gain to allow the full dynamic range of the receiver to be utilized. After the amplification, the signal is converted to the digital domain and is demodulated.

2.5.1 LNA

The on board LNA is a fully differential structure integrated with the mixer providing low noise performance and good immunity from blocking signals.

2.5.2 Mixer

The quadrature down converter is an image reject type mixer. The quadrature down-converter is implemented as a passive FET mixer including low-pass filtering, DC blocking at its output and part of the gain controlled IF amplifier.

2.5.3 Polyphase Filter

The polyphase filter provides the required channel selectivity and recombines the quadrature signal to a single differential output. It also serves as an anti-aliasing filter for the ADC which is part of the demodulator.

2.5.4 IF Amplifier

The gain controlled IF amplifier automatically adapts the wanted signal to the maximum input range of the demodulator.

2.5.5 AGC

A digitally realized automatic gain control is imple-

mented as part of the demodulator to adjust the gain of the IF amplifiers.

2.5.6 Demodulator

The demodulator consists of an ADC and digital circuitry. Digital signal processing is used to extract the phase from the IF signal. The derivative of the phase over one symbol results in the demodulated data symbol. Automatic Frequency Control (AFC) is used to maintain good sensitivity for IF frequency offsets up to ±100kHz. Two methods of AFC are available in this device: AFC + Active Slice (classic solution, refer to tables 31 through 33) and Fast-AFC (FAFC refer tables 34 and 35). The FAFC achieves the same accuracy as the classic solution but uses fewer preamble bits. This is now the preferred method as represented by the recommended settings of sections 5.1 and 5.2 which are used during characterisation. FAFC must be disabled during search mode which is done by setting RF_FAFC_CTRL_REG[FAFC_EN] = 0.

2.6 DIGITAL CONTROLLER

A digital controller is provided to operate the chip by timed control sequences, so called dynamic control functions (DCFs, see Section 3.3). The set and reset times of DCFs will be defined by programming register banks. Two groups of control sequences can be defined. One for the receive mode and one for the transmit mode of the chip. By use of a control word, the chip is brought into either the receive or the transmit mode. Dependent on the selected mode of operation, one of the two groups of control sequences is started.

2.7 DIGITAL OUTPUT PORTS

Four logic output ports are available for general switching purposes. The signals provided at the ports can be used to control a Tx/Rx switch. The logic level and the relative timing of the logic signals at the ports can be programmed. Two additional ports (P0 and P0n) are meant for fast antenna diversity (FAD) switching. The FAD functionality is implemented on-chip.

2.8 MICROWIRE™ INTERFACE

The LMX4181 register set can be accessed through the MICROWIRE™ interface. The interface allows read/write operations from/to the IC (see Section 3.1). To program the device, a data word is clocked into the shift register of this interface. Digital RSSI information is accessible by reading from this interface.

2.9 SUPPLY STRATEGY

Digital blocks are supplied from an externally regulated voltage source (VDD_DIG). This voltage source is always active, such that the programming in the MICROWIRE™ registers is sustained.

Analog blocks and digital output ports are supplied from several on-chip low-drop-out regulators (LDOs). These regulators are all supplied from the VBAT_ANAx pins. The analog supply voltages (e.g. VBAT_ANA1) are regulated to 1.7V, using a switched capacitor circuit. The regulators are refreshed on a slot to slot basis, using the signal on LE (refer to Section 3.6).

3.0 MICROWIRE™ interface

3.1 MICROWIRE FUNCTIONALITY

The LMX4181 register set can be accessed through the MICROWIRE™ interface.

MICROWIRE™ is a three-wire serial interface to transfer data and control words from the baseband IC to the LMX4181 (by means of a *write* operation) and back (by means of a *read* operation).

A Microwire transaction consists of 24 bits (or 8 bits, see Section 4.1):

- The first bit (RW) discriminates between a read (RW = 1) and a write (RW = 0) operation.
- The next 7 bits (A6 to A0) are the address bits A[6:0].
- The final 16 bits (D15 to D0) are the data bits D[15:0].
- The three wires of the interface are:
- LE: latch enable. This is an input to the LMX4181. All serial communication with the device is enabled only when this pin is high. When writing, the transferred information is decoded and stored into one of the on-chip registers on the falling edge of LE (no other clock is necessary to be active).
- SK: serial clock. This input controls the bit transfer rate. On the rising edge of SK, incoming serial data is clocked into the Microwire shift register. This signal has only effect when LE is high.
- SIO: data in/data out. This signal carries the bits transferred.

The timing of a write operation is shown in Figure 5 while the diagram for a read operation is given in Figure 6. Note that the read operation has half a clock cycle shift for the data bits.

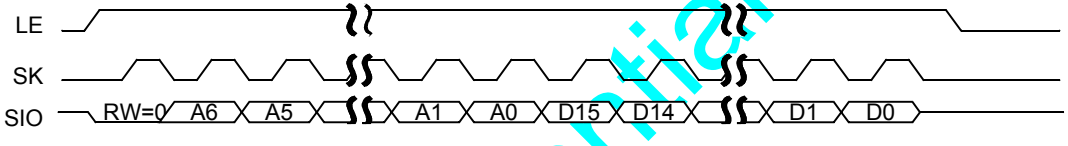

Figure 5 Microwire write timing.

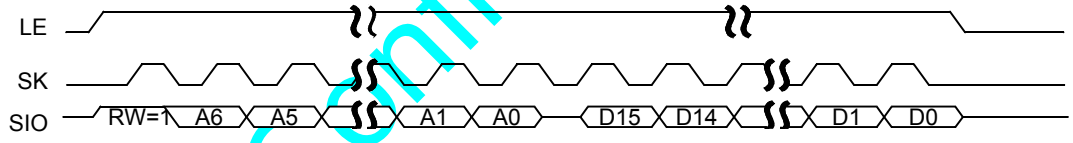

Figure 6 Microwire read timing.

Information on the interface of the LMX4181 with the baseband IC SC144xx can be found in a separate document: *SiTel Semiconductor Application Note AN-D-xxx: "*Interfacing the LMX4181 with ...".

3.2 BURST-MODE CONTROL WORD

Writing to the special 18-bit register BURST_MODE_CTRL_REG initiates most of the activities related to processing a TX or RX slot. In particular, the dynamic control functions (DCFs), the behavior of which can be configured in advance by static register settings (see Section 3.3) are activated by means of a single transceiver control interface transaction.

BURST_MODE_CTRL_REG is also called burst-mode control word (BMCW) for historical reasons.

For the BMCW, the information in A[1:0] should be interpreted as the data symbol RX_TX:

- RX_TX = 1: 'transmit'; the transceiver will initiate the processing of a "TX slot" and activate those blocks associated with transmitting according to a programmable sequence.
- RX_TX = 2: 'receive'; the transceiver will initiate the processing of an "RX slot" and activate those blocks associated with receiving according to a programmable sequence.
- RX_TX = 3: 'general calibration'; an autonomous calibration procedure is executed in the hardware (see Section 4.2).
- RX_TX = 0, the radio timers (see Section 3.4) are not updated until the reception of the following BMCW with RX_TX = 0. This is known as the pause word.

A BMCW transfer may consist of 8 bits only (M_RST is executed after 8 bits are transferred rather than 24 bits). If 24 bits are sent, the data bits contain various settings that are likely to change from slot to slot (See BURST_MODE_CTRL_REG).

3.3 DYNAMIC CONTROL FUNCTIONS

The processing of a burst, i.e. a receive (RX) or trans-

mit (TX) slot, is characterized by a sequence of activations and deactivations of transceiver blocks that obey a specific timing at the resolution of one DECT symbol. The waveform that indicates the moment of activation and deactivation for one block, is called that block's *dynamic control function* (DCF).

A collection of counters have been implemented to realize the DCFs. These counters are called the *radio timers*. The mechanism is explained in detail in the next section.

3.4 DCF GENERATION WITH RADIO TIMERS

When the transceiver needs to process a transmit or receive slot, various blocks on the LMX4181 will be activated in some specific order according to programmable timing settings. The settings related to one block define the block's dynamic control function (DCF).

A DCF is characterized by a time instant when activation starts and an instant when activation terminates. These instants are specified relative to seven so-called switch instants (SIs). They are listed in Table 4. Each of them, except SO_SLOT which is fixed to time 0, can be programmed with a value between 0 and 1984 DECT bit periods, in multiples of 8. The values are programmed in the registers PORT_RSSI_SI_REG, TX_SI_REG and RX_SI_REG. The values are programmed as the actual switch instant in DECT bit periods divided by 8 (= 8 most significant bits). The offsets from the SIs can be specified using a granularity of a single DECT bit period within a range of 0 to 63.

Table 4: List of switch instants

switch instant	description
SO_SLOT	start of slot (fixed at time 0)
SO_PORT	start of port (programmable)

Table 4: List of switch instants

switch instant	description
EO_RSSI	end of RSSI measurement (programmable)
SO_TX	start of transmit (programmable)
SO_RX	start of receive (programmable)
EO_TX	end of transmit (programmable)
EO_RX	end of receive (programmable)

The SIs with respect to which the programmable set and reset times are specified, are hard wired. In addition, the control of activation by either TX, RX or either of the two is hard wired as well. For each DCF <B>, there is a register <B>_DCF_REG. The DCFs and their associated SIs are listed in Table 3. The registers have the following fields (port DCFs are slightly different and are discussed later on):

- SET_OFFSET: limited-range offset in DECT bit periods for the start time of the DCF measured from start SI.
- RESET_OFFSET: limited-range offset in DECT bit periods for the stop time of the DCF measured from stop SI.
- DIS: disable block activation.

In addition, a bit called ALW_EN is associated with each block controlled by a DCF. Setting this bit to '1' activates the block irrespective of any other condition that causes the activation or deactivation of the DCF. All ALW_EN bits of the LMX4181 have been collected in a single register called ALW_EN_REG such that any combination of blocks or ports can be turned on or off with a single transceiver control interface transaction. The timing of DCFs is illustrated in Figure 7.

Table 5: List of DCFs

DCF	description	controlled by	start SI	stop SI
PA	integrated power-amplifier (PA)	TX or TRX[2)3)]	SO_TRX[4)], SO_PORT[5)] or SO_SLOT[6)]	EO_TRX[8)]
PA_DRIVER_STAGE PA_FINAL_STAGE	power ramping of the PA	TX, RX or TRX[13)]	SO_TRX, SO_PORT[14)]or SO_SLOT[14)]	EO_TRX
LNAMIX	low-noise amplifier and mixer	RX	SO_RX or SO_SLOT[7)]	EO_RX
IF	intermediate-frequency filter	RX	SO_RX or SO_SLOT[7)]	EO_RX
ADC	analog-to-digital converter	RX	SO_RX or SO_SLOT[7)]	EO_RX
DEM	demodulator	RX	SO_RX or SO_SLOT[7)]	EO_RX

Table 5: List of DCFs

DCF	description	controlled by	start SI	stop SI
RSSIPH	RSSI peak-hold computation[9)]	RX	SO_DEM[10)]	EO_RSSI or EO_RX[12)]
BIAS	bias circuit	TRX	SO_SLOT	EO_TRX
SYNTH	synthesizer	TRX	SO_SLOT	EO_TRX
PLLCLOSED	PLL closed loop	TRX	SO_SLOT	EO_TRX or SO_TRX[7)]
PORT1 PORT2	general-purpose output ports	TX, RX or TRX[13)]	SO_TRX, SO_PORT[14)]	EO_TRX
FAD_WINDOW	fast antenna diversity window	RX	SO_DEM	SO_DEM

Note 2: TRX is the Boolean OR of TX and RX.
Note 3: PA is sensitive to both TX and RX when BURST_MODE_CTRL_REG[RX_SENSITIVE] = '1'.
Note 4: SO_TRX means SO_TX when in a TX slot and SO_RX when in an RX slot.
Note 5: The start SI becomes SO_PORT when PA_DCF_REG[PA_SSI] = '1'.
Note 6: The start SI becomes SO_SLOT when PA_DCF_REG[PA_SSI] = '2' or '3'
Note 7: The start SI becomes SO_SLOT when *xxx*_DCF_REG[SSI] = '1'
Note 8: EO_TRX means EO_TX when in a TX slot and EO_RX when in an RX slot.
Note 9: While the RSSIPH_DCF and the DEM_DCF are active, reading the RSSI_REG[RSSI_VAL] resets peak-hold computation.
Note 10: SO_DEM is the absolute time instant where the demodulator is started: SO_RX + DEM_DCF_REG[SET_OFFSET].
Note 11: The stop SI becomes SO_TRX when PLLCLOSED_DCF_REG[SSI] = '1'.
Note 12: The stop SI becomes EO_RX when BURST_MODE_CTRL_REG[RSSI_MODE] = '1'.
Note 13: The sensitivity of the ports for either TX, RX or both is programmable with PORTx_DCF_REG[EN_BY_TX | EN_BY_RX].
Note 14: The start SI becomes SO_PORT when PORT_CTRL_REG[SSI] = '1'.

All times (in DECT symbol periods) are counted with respect to a moment $T_{start} + \Delta T_{start}$, where T_{start} is the moment when a TX or RX setting in the BMCW was received and ΔT_{start} is a delay related to the processing of the BMCW. There exists also a delay ΔT_{alw_en} from the moment of receiving ALW_EN_REG until it results in activation or deactivation of a block (not shown in the figure).

Port DCFs

Port DCFs have four control bits instead of the DIS bit:

- EN_BY_TX: 'enable by transmit'; when '1', the port is activated in a TX slot'; the offsets are taken with respect to a programmable Start SI and EO_TX.
- EN_BY_RX: 'enable by receive'; when '1', the port is activated in an RX slot; the offsets are taken with respect to a programmable Start SI and EO_RX.
- SSI: 'select the Start SI'; when '0', the port is activated relative to SO_TRX, when '1', relative to SO_PORT
- The polarity of the ports can be programmed with the symbols PORT*x*_INV in PORT_CTRL_REG

The dynamic control of the PA is identical to any other block, with the exception of 2 extra control bits. The function of PA_SSI is similar to that of the port DCF's, giving more freedom of the absolute time at which the PA switches on. Furthermore, the PA driver can also be activated during a receive slot (for test purposes only).

Note that the combination of SIs and offsets allows to control block activation within a range of 0 to 2047 DECT symbol periods at a single symbol resolution.

Controlling the blocks by programming ALW_EN_REG allows block activation with an arbitrary duration at a single symbol resolution but with the restriction that two consecutive changes are at least three symbols apart. The two mechanisms can be mixed at wish leading to a very flexible control of block activation.

3.5 RE-TRIGGERING

When an 8-bit BMCW is programmed with RX_TX='1' or '2', the transceiver will process TX or RX slots without activating the synthesizer. This mode is useful if relatively short slots are to be transmitted or received on the same RF channel with a small guard space in between.

All DCFs that have a start SI = SO_SLOT will retain their values. All DCFs that have a start SI = SO_TRX, will be started relative to SO_SLOT and stopped relative to their own stop SI - SO_TRX.

Effectively, this re-triggers the FAD, active slice and RSSI peak-hold computation for the next receive slot. Otherwise it allows the PA to be temporarily switched off during the guard space between two transmit slots, while leaving the PLL tuned to the desired frequency. Note that the 8-bit BMCW must be programmed before the end of the initial slot, such that the synthesizer blocks are in the correct setting for endured operation.

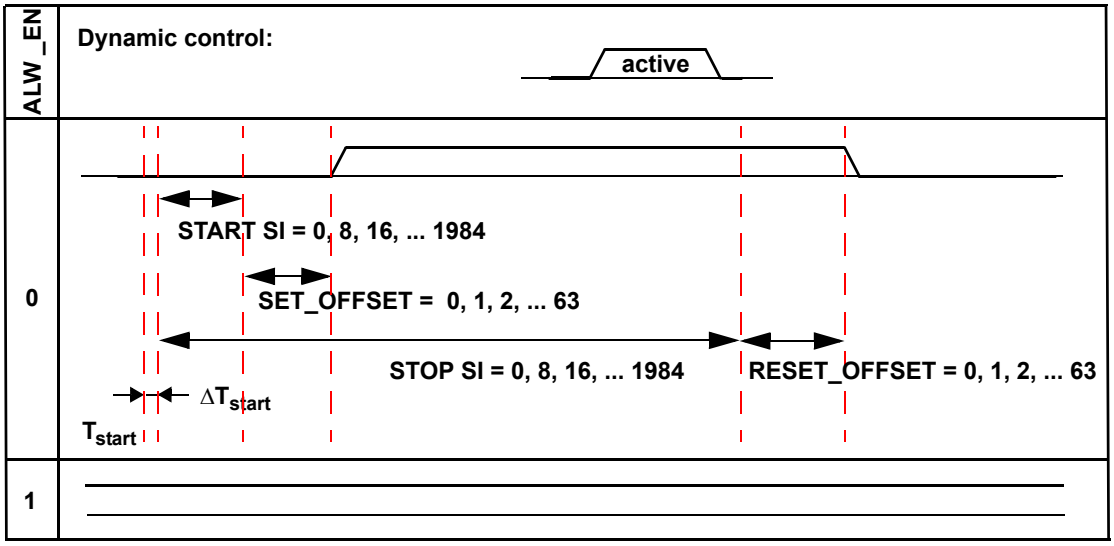

Figure 7 DCF timing

3.6 LDO REFRESH

The LDOs that control the power supplies need to be refreshed regularly, from slot to slot. This is done automatically by activity on the MICROWIRE™ interface as described in Section 3.1. Typically, writing a BMCW when the LMX4181is idle will refresh the LDOs prior to activating the DCFs to process the new slot.

The minimum refresh time is 4 symbols. It is therefore recommended, when using the MICROWIRE™ interface at the maximum speed, to use some overlap around the activity of SK and SIO, such that the LE is active for more than 4 symbols.

Note that the BIAS_DCF must be inactive while LE is active for an LDO refresh to take place (Refresh is the logical AND of NOT(BIAS_DCF) and LE.) This condition prevents accidentally refreshing the LDOs during an active slot by e.g. reading the RSSI information. It is necessary to allow the BIAS_DCF to reset (by waiting for the DCF to terminate) before the next MICROWIRE™ action is capable to refresh the LDOs.

3.7 VOLTAGE HANDLING OF THE DIGITAL INTERFACE

The LMX4181 is optimized for 2 battery operation without the need for a DC-DC converter on the base band processor. The optimum application features a baseband processor that uses 1.8-3.3 V for its digital interface.

Some baseband processors (e.g. SiTel Semiconductor's SC14434) uses a digital supply voltage of more than 2.0 V. In order to withstand these relatively high voltages, the pins on the LMX4181 digital interface are supplied by a dedicated IO supply (VDDIO) that can be up to 3.3 V. The IO supply voltages must be supplied by the baseband processor. The specifications for the digital interface pins can be found in Table 60 and Table 61.

It is possible to put the digital output RX_DATA pin in tri-state mode when the LMX4181 is not in receive mode. More specifically, the digital output RX_DATA pin is only enabled when the DEM_DCF is active (refer to the register DEM_CTRL_REG). This can be used for application where two LMX4181 are connected to a single baseband processor.

The reset pin RSTn is standard digital input. In power-on reset mode, the RSTn pin should be connected to VDDIO by a suitable pull-up resistor and to ground by a suitable capacitor (refer to Table 65). When the RSTn pin is connected to a digital port on the baseband processor, no external components are needed.

Because the TX_DATA input pin can operate in an analogue mode (see Section 2.4), it is recommend that the input pin TX_DATA is kept low until the supply signals VDD_DIG and VDDIO are present.

4.0 Programming description

4.1 BURST MODE PROGRAMMING

Programming the BMCW will bring the LMX4181 in/out receive or transmit mode. It causes the relevant circuit blocks to switch on and off using the predefined DCFs (refer to Section 3.3).

This register contains 5 symbols using a total of 18 data bits (at the expense of 2 address bits).

The symbol RX_TX sets the transceiver in RX or TX mode. When the value RX_TX = '3' a general calibration is performed (refer to Section 4.2).

The symbol FAD sets the behavior of the *fast antenna diversity* algorithm (refer to Section 4.5).

The function of RSSI_MODE depends on the mode of operation.

When in RX mode, it defines the behavior of the RSSI computation. The RSSI value is computed constantly during a complete RX slot. Its maximum is available for read after the slot is processed. In some cases it is desirable to measure the maximum of the RSSI during only the first part of a slot. RSSI_MODE = '1' enables the STOP_SI of RSSIPH_DCF to be changed to EO_RSSI instead of EO_RX.

The symbols RFCAL and CN specify the functionality of the synthesizer.

The symbol RFCAL is used for VCO calibration. There are 3 ways in which the synthesizer can start up. The choice is programmed in the symbol RFCAL_MODE in the RFCAL_CTRL_REG. Refer to Section 4.4 for a description of the algorithms.

The desired local oscillator frequency can be programmed with a 7 bit channel number (*CN*) and is given by

$$f_{LO} = [CH0 + SGN(CS \times CN) + RX]f_{IF} \quad (2)$$

In this equation, f_{IF} means the intermediate frequency of 864kHz or more general, f_{IF} is fixed at $f_{REFCLK}/12$. All local oscillator frequencies are therefore given as multiples of f_{IF}. The parameters *CH0*, *SGN* and *CS* are multipliers that are constant in a given application. The variables *CN* and *RX* are programmed on a slot to slot basis.

CH0 defines the frequency of channel 0. In the DECT system that is 1897.344 MHz, so *CH0* = 2196. The channels in the DECT system count from high to low frequency, so the sign of the additional term is negative (*SGN* = -1). The DECT channel spacing is 1728 kHz, so *CS* = 2.

The channel numbers (*CN*) can now simply be programmed between 0 and 9 as defined in the DECT specification. The additional parameter *RX*, the MSB of the RX_TX symbol in the BMCW, is either 1 (in RX mode) or 0 (in TX mode) indicating that the local oscillator frequency is higher than the wanted channel frequency in receive mode.

For the EU-DECT system, the parameters *CH0*, *SGN*, *CS* are given by the reset values, thus need not be programmed. For other applications in or around the EU-DECT, these parameters can be redefined at wish. The value of *CN* can vary between 0 and 127 enabling all kinds of applications with up to 128 channels. The channel spacing parameter *CS* can vary from 1 to 4 and the sign can be either positive or negative (*SGN* = -1 or +1).

The parameter *CS* should be changed from 2 (CS_MO=1) for full-rate applications to 1 (CS_MO=0) for half-rate applications.

Due to the limited frequency range of the integrated VCO, not all possible programming combinations yield valid local oscillator frequencies.

In TX mode the output power mode is set by transmitting the PA_CTRL1_REG, PA_CTRL2_REG, TEST_MODE_REG and TEST_CTRL3_REG to the PA via the microwire on a slot by slot base.

4.2 GENERAL CALIBRATION PROGRAMMING

Calibration of all fabrication tolerances is performed automatically by programming the BMCW symbol RX_TX = '3'. The IF filter center frequency and bandwidth, the IF amplifier DC offset voltage, the start value for the VCO calibration and the bandwidth of the internal loop filter are all calibrated sequentially.

The modulation gain can optionally be calibrated in parallel or sequentially with the calibration of the IF filter and IF amplifier. The following options are available (see GENCAL_MODE in RFCAL_CTRL_REG):

- Only the VCO, IF filter and IF amplifier are calibrated
- Only the VCO and modulation gain are calibrated
- The VCO, IF filter, IF amplifier and modulation gain are calibrated. The modulation gain is calibrated in parallel with the IF filter and IF amplifier.
- The VCO, modulation gain IF filter and IF amplifier are calibrated. The modulation gain is calibrated before the IF filter and IF amplifier.

The start value for the VCO calibration depends on the selected channel number (CN). The base band IC may perform multiple calibrations sequentially to build a table of start values, or simply choose CN in the center of the frequency band and calibrate only once. Note that although the RX-bit from RX_TX is '1' when RX_TX='3', that during general calibration only the TX channel frequency can be programmed (*RX* = 0 in Eq. (2)).

The length of the VCO calibration is 74 symbols, the combined length of the IF filter and IF amplifier calibrations is 248 symbols, and the length of the modulation gain calibration is 8 + 8•MODCAL_PERIOD symbols.

This general calibration has to be performed only once after initial programming of the LMX4181. Afterwards the settings are kept in on-chip registers.

Note that during calibration the reference clock must be present.

4.3 MODULATION GAIN CALIBRATION PROGRAMMING

The LMX4181 features a novel synthesizer architecture enabling closed loop modulation. This has the advantage that the base band TDO output level no longer needs to be trimmed in production. This trimming is replaced by an automatic alignment. This Modulation Gain Calibration is recommended to be performed once per telephone call. The modulation gain calibration can either be done as a part of the general calibration or be triggered separately by setting the MODCAL_TRIG in the PLL_CTRL4_REG register.

4.4 RF CALIBRATION PROGRAMMING

The synthesizer tunes the local oscillator to the desired frequency. It consists of a coarse tuning (RFCAL) and a fine tuning (PLL in closed loop) action. The coarse tuning action is needed to optimize the amount of fixed capacitance in the VCO tank circuit, by means of a binary scaled calibration capacitance (C_{cal} = C_{LSB}×RFCAL_CAP). The coarse tuning range is large to cover all fabrication tolerances. During operation, however, the coarse tuning only uses a limited range around its preset value.

For this reason, the VCO calibration is split up into 2 parts. Initially, during general calibration (Section 4.2), the process tolerances are eliminated and a start value for RFCAL_CAP (CC_{start}) is established.

During normal operation a linear search algorithm optimizes the limited range (CC_δ) to suit the given channel. In the given slot the value for RFCAL_CAP = CC_{start} + CC_δ.

Depending on the application the range of CC_δ can be chosen by varying the number of measurements (RFCAL_STEPS in RFCAL_CTRL_REG) that are performed by the algorithm. For DECT the variation is small and thus 3 steps is default.

Each measurement step can have one of 3 results: correct, too high or too low. The resulting range of CC_δ is thus $[-2^{RFCAL\_STEPS}+1, 2^{RFCAL\_STEPS}-1]$, which turns out as $CC_\delta \in [-7, 7]$ for RFCAL_STEPS = '3', as shown in Figure 8.

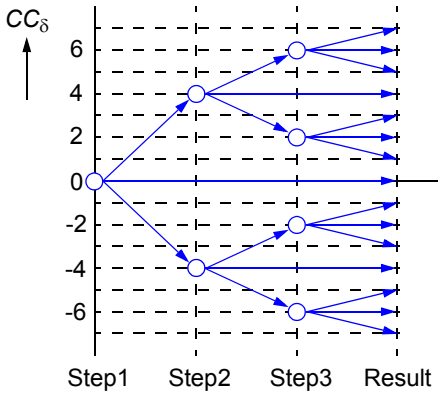

Figure 8 RF Calibration range for 3 steps

Calibrating only in 3 steps rather than 6 (1 step for every bit in RFCAL_CAP) saves half the time needed for calibration. This allows the PLL to operate in closed loop condition longer and hence more accurate tuning. There are 3 ways in which the calibration can be initiated. This is programed in the symbol RFCAL_MODE in RFCAL_CTRL_REG.

RFCAL_MODE = '0': VCO calibration is omitted altogether, enabling the synthesizer to operate in closed loop for the maximum amount of time. In this case the value of RFCAL from the BMCW is used to preset the VCO. For this mode to work, the base band must keep record of the proper values per channel. These values can be obtained by using one of the other calibration modes first and reading the final value of RFCAL_CAP at the end of the slot from RSSI_REG.

RFCAL_MODE = '1': VCO calibration is performed. The value of CC_{start} is provided by RFCAL in the BMCW. When the base band provides the previous value that was used for the given channel, the number of measurements may be restricted to RFCAL_STEPS = '1'.

RFCAL_MODE = '2': VCO calibration is performed. The previous value of RFCAL_CAP is used for CC_{start}. This value may be derived at a different channel frequency, but only moments earlier. Aging and operating temperature effects are already represented by CC_{start}, and the number of measurements may therefore be restricted to RFCAL_STEPS = '2'.

4.5 FAST ANTENNA DIVERSITY

The LMX4181 allows *fast antenna diversity* (FAD), the possibility to select the best of two available antennas. This choice is determined in an RX slot, based on the RSSI information during the (prolonged) preamble. It is described in this section in conjunction with the behavior of the ports P0 and P0n that are dedicated for switching antennas.

When FAD is to be used, and two antennas are therefore present, the following port connections need to be

used:

- P1 controls the RX switch
- P2 controls the TX switch
- P0 controls Antenna 1
- P0n controls Antenna 2

There is a special DCF for FAD called FAD_WINDOW (See FAD_WINDOW_DCF_REG). Note that the set and reset offsets are relative to the start instant of the demodulator, rather than SO_RX.

The FAD algorithm is activated when the symbol FAD = '3' and RX_TX = '2' in the BMCW. Initially, Antenna 1 is selected and the RSSI starts to settle. At the switch instant FAD_SWAP, Antenna 2 is selected and a new value for the RSSI becomes available. At the switch instant FAD_DECIDE, the antenna that gave the highest RSSI_VAL is selected and can be read from RSSI_REG as the symbol FAD_CHOICE.

The symbol FAD_CHOICE remains valid, until the next RX slot evaluates it again. When the first slot after evaluation is a TX slot, as is generally true in a hand set, the symbol FAD in the BMCW can be left at '3', and the same antenna is used for this TX slot.

In a base station, the RX slot is usually succeeded by another RX slot, since in DECT all hand sets transmit one after the other in the first half frame and receive one after the other in the second half frame. In this case, each hand set can be identified by its channel number *CN*. In order to use the best antenna for transmitting to a given hand set, the base band IC must record the value of FAD_CHOICE per channel and use it in a TX slot on the same channel ($FAD_{TX,CN}$ = $FAD\_CHOICE_{RX,CN}$). Note that FAD is a 2-bit symbol and FAD_CHOICE is 1-bit.

The combination of control settings leads to the behavior of P0 and P0n as given in Table 6.

Table 6: FAD and P0/P0n switching

FAD	P0/P0n behavior
0	P0 follows P1 in RX slot and P2 in TX slot; P0n = ANT_INACTIVE_VAL.
1	P0 = ANT_INACTIVE_VAL P0n follows P1 in RX slot and P2 in TX slot.
2	Do not use FAD, P0/P0n inactive P0 = ANT_INACTIVE_VAL; P0n = ANT_INACTIVE_VAL.
3	If FAD_CHOICE = '0': P0 follows P1 in RX slot and P2 in TX slot; P0n = ANT_INACTIVE_VAL. If FAD_CHOICE = '1': P0 = ANT_INACTIVE_VAL P0n follows P1 in RX slot and P2 in TX slot. Note that FAD_CHOICE dynamically changes during an RX slot, resulting in the wanted FAD behavior.

A typical example of the behavior of P0 and P0n during an RX slot is shown in the timing diagram of Figure 9(a). For all signals, it is assumed that a DCF is high when active (ANT_INACTIVE_VAL = '0' in PORT_CTRL_REG). As can be seen in the figure, the timing of P0 and P0n is derived from the DCFs of P1 and DEM and the preamble delay. Figure 9(b) shows typical behavior in a TX slot where P0 and P0n only depend on the DCF of P2.

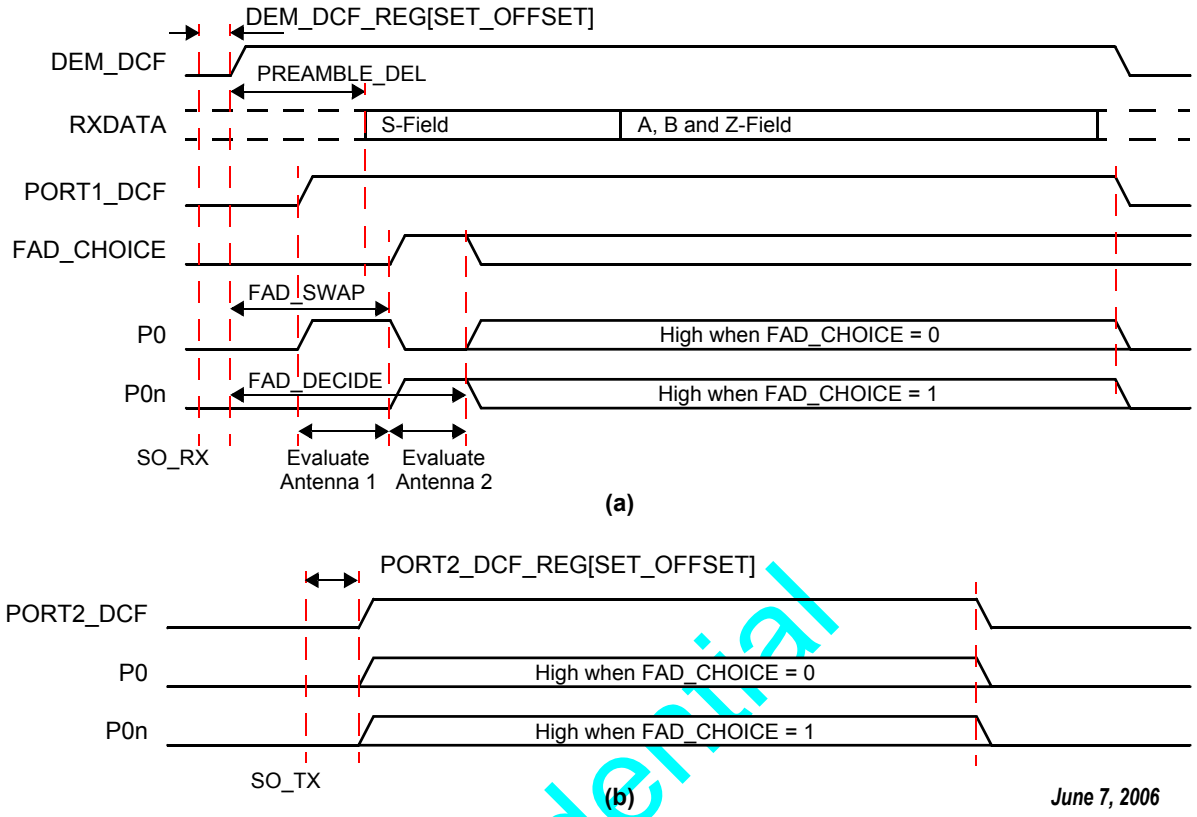

Figure 9 Example of typical timing of P0 and P0n when performing FAD in an RX slot (a) and a TX slot (b)

5.0 Memory map Detailed

Table 7: Detailed memory Map

Note 15: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
0x00	BURST_MODE_CTRL_REG	BMCW
0x04	ALW_EN_REG	always-enable bits for block activation
0x05	PORT_RSSI_SI_REG	SO_PORT/EO_RSSI switch instant settings
0x06	TX_SI_REG	TX switch instant settings
0x07	RX_SI_REG	RX switch instant settings
0x08	PORT1_DCF_REG	Port 1 dynamic control function settings
0x09	PORT2_DCF_REG	Port 2 dynamic control function settings
0x0A	PA_DRIVER_STAGE_DCF_REG	PA driver stage dynamic control function settings
0x0B	PA_FINAL_STAGE_DCF_REG	PA final stage dynamic control function settings
0x0C	PLLCLOSED_DCF_REG	PLL closed loop dynamic control function
0x0D	SYNTH_DCF_REG	voltage-controlled oscillator dynamic control function
0x0E	BIAS_DCF_REG	bias circuit dynamic control function
0x0F	RSSIPH_DCF_REG	RSSI peak-hold computation dynamic control function
0x10	DEM_DCF_REG	demodulator dynamic control function
0x11	ADC_DCF_REG	analog-to-digital converter dynamic control function
0x12	IF_DCF_REG	intermediate-frequency filter dynamic control function
0x13	LNAMIX_DCF_REG	low-noise amplifier and mixer dynamic control function
0x14	PA_DCF_REG	PA dynamic control function
0x15	FAD_WINDOW_DCF_REG	FAD timing control function
0x16	TX_DATA_DCF_REG	TX_DATA interface timing control function
0x20	RFCAL_CTRL_REG	RF calibration control settings
0x21		reserved
0x22	DEM_CTRL_REG	demodulator control settings
0x23	PREAMBLE_REG	preamble-processing control settings
0x24	RSSI_REG	received-signal strength indication value, FAD choice and RF calibration result
0x25	PORT_CTRL_REG	port control settings
0x26	PAD_IO_REG	disable digital input/output on PORTs
0x27	BANDGAP_REG	Bandgap register
0x28	PLL_CTRL1_REG	PLL control settings for frequency calculation
0x29	PLL_CTRL2_REG	PLL control settings for frequency calculation
0x2A	PLL_CTRL3_REG	PLL control settings for frequency calculation
0x2B	PLL_CTRL4_REG	PLL control settings for frequency calculation
0x2C	SLICER_REG	RX active slicer settings
0x2D	SLICER_RESULT_REG	Results computed by RX active slicer
0x2E	GAUSS_GAIN_RESULT_REG	Result of modulation-gain calibration
0x2F	TX_DATA_CTRL_REG	TX_DATA control settings
~~0xFF7070~~	~~BURST_MODE_SHADOW1_REG~~	~~BMCW shadow register~~

Table 7: Detailed memory Map

Note 15: Test registers are not defined here. Write access to undefined addresses might result in undefined behaviour.

Address	Port	Description
~~0xFF7072~~	~~BURST_MODE_SHADOW2_REG~~	~~BMCW shadow register~~
~~0xFF7074~~	~~DCF_MONITOR_REG~~	~~To monitor DCF strobes to GPIO pins~~
0x40	SYNTH_CTRL1_REG	These registers shall not be modified unless instructed by SiTel Semiconductor. Recommended settings are given in Table 8
0x41	SYNTH_CTRL2_REG	
0x42	AGC_REG	
0x43	AGC12_TH_REG	
0x44	AGC12_ALPHA_REG	
0x45	POSITIONING_REG	
0x46	DC_OFFSET_REG	
0x47	DC_OFFSET34_REG	
0x48	IQ_DC_OFFSET_REG	
0x49	IF_CTRL_REG	
0x4A	REF_OSC_REG	
0x4B	ADC_CTRL_REG	
0x4C	RFIO_CTRL_REG	
0x4D	BIAS_CTRL_REG	
0x4E	DRIFT_TEST_REG	
0x4F	TEST_MODE_REG	
0x50	LDO_TEST_REG	
0x56	PLL_CTRL5_REG	
0x57	PLL_CTRL6_REG	
0x58	TEST_CTRL3_REG	
0x59	PA_CTRL1_REG	RF PA control registers
0x5A	PA_CTRL2_REG	
0x5B	IFCAL_RESULT_REG	These registers shall not be modified unless instructed by SiTel Semiconductor. Recommended settings are given in Table 8
0x5C	DC_OFFSET12_REG	
0x5D	AGC_RESULT_REG	
~~0x5E~~	~~GAUSS_GAIN_MSB_REG~~	
0x5F	RXFE_CTRL_REG	
0x60	FAFC_CTRL_REG	
0x61	FAFC_RESULT_REG	
0x62	TEST_MODE2_REG	
0x70	MODCAL_RESULT1_REG	
0x71	MODCAL_RESULT2_REG	
0x7A	CHIP_TEST_REG	Chip test register 1
0x7B	CHIP_ID1_REG	Chip identification register 1
0x7C	CHIP_ID2_REG	Chip identification register 3
0x7D	CHIP_REVISION_REG	Chip revision register
0x7E	CHIP_CONFIG1_REG	Chip configuration register 1
0x7F	CHIP_CONFIG2_REG	Chip configuration register 2

5.1 RECOMMENDED SETTINGS FOR RF APPLICATION REGISTERS

All RF application registers can have arbitrary values, but the recommendations from Table 8 may serve as a starting point, compatible with an application of SiTel Semiconductor's LMX4180.

These settings are used as a standard burst definition for the radio performance measurements as specified in sections 7.2, 7.3 and 7.4 starting on page 42.

They represent the setup for receiving or transmitting a P32 packet with a 16 bit preamble in the DECT application in blind slot operation. This means that the slot consists of 424 symbols in the physical packet (S-field 32 bits, D-field 388 bits and Z-field 4 bits) and the guard space is 56 symbols long.

The falling edge of LE when writing the BMCW is synchronized at 200 symbols before bit p0 of the physical packet. Note that the synchronization of the MICROWIRE™ interface takes only 3/9 to 4/9 symbol periods (= tLE_start, refer to Table 64).

Registers BURST_MODE_CTRL_REG and ALW_EN_REG change on a slot to slot basis, based on what type of function the LMX4181 is supposed to perform (refer to Tables 10), so no recommendations are given.

Registers RSSI_REG, SLICER_RESULT_REG and GAUSS_GAIN_RESULT_REG are read only (R), so no recommendations are given. With varying slot length the registers with the addresses 0x05 through 0x07 are the only ones that need to change.

Table 8: Recommended and reset values of application registers

Address	Port	Recommended value	Reset value
0x00	BURST_MODE_CTRL_REG	-	0x0000
0x04	ALW_EN_REG	-	0x0000
0x05	PORT_RSSI_SI_REG	No Change	0x1C00
0x06	TX_SI_REG	No Change	0x4E12
0x07	RX_SI_REG	No Change	0x4E13
0x08	PORT1_DCF_REG	No Change	0x2346
0x09	PORT2_DCF_REG	No Change	0x145E
0x0A	PA_DRIVER_STAGE_DCF_REG	No Change	0x102D
0x0B	PA_FINAL_STAGE_DCF_REG	No Change	0x102D
0x0C	PLLCLOSED_DCF_REG	No Change	0x4720
0x0D	SYNTH_DCF_REG	No Change	0x0754
0x0E	BIAS_DCF_REG	No Change	0x0780
0x0F	RSSIPH_DCF_REG	No Change	0x006A
0x10	DEM_DCF_REG	No Change	0x42CF
0x11	ADC_DCF_REG	No Change	0x44C0
0x12	IF_DCF_REG	No Change	0x4442
0x13	LNAMIX_DCF_REG	0x43C4	0x43C2
0x14	PA_DCF_REG	No Change	0x0719
0x15	FAD_WINDOW_DCF_REG	No Change	0x0A23
0x20	RFCAL_CTRL_REG	No Change	0x0033
0x22	DEM_CTRL_REG	No Change	0x0001
0x23	PREAMBLE_REG	No Change	0x042A
0x24	RSSI_REG	R	0x0030
0x25	PORT_CTRL_REG	No Change	0x0000
0x26	PAD_IO_REG	No Change	0x003F
0x27	BANDGAP_REG	0x0009	0x000F
0x28	PLL_CTRL1_REG	R	0x6894
0x29	PLL_CTRL2_REG	**(Note 16)** No Change	0x2036
0x2A	PLL_CTRL3_REG	No Change	0x0800

Table 8: Recommended and reset values of application registers

Address	Port	Recommended value	Reset value
0x2B	PLL_CTRL4_REG	No Change	0xB824
0x2C	SLICER_REG	No Change	0x00E0
0x2D	SLICER_RESULT_REG	R	0x0000
0x60	FAFC_CTRL_REG	(normal operation) 0x0005 (search mode) 0x0004	0x0005
0x61	FAFC_RESULT_REG	R	0

Note 16: A recommended value for GAUSS_GAIN is given as starting point for RF evaluation. In the application this value should be (automatically) calibrated as described in Section 4.3.

5.2 RF TEST REGISTER VALUES

Test registers are used during production. They set several blocks in alternative operational modes. These modes are subject to change until this datasheet reaches V1.0

The recommended values are used for characterization and production tests and are the only settings that guarantee the performance specification as given in sections 7.2, 7.3 and 7.4 starting on page 42.

Registers of which the Recommended Value is indicated by R are read only registers and need never be written.

Table 9: RF Test register values

Address	Port	Recommended Values	Reset Value
0x40	SYNTH_CTRL1_REG	No Change	0x0C08
0x41	SYNTH_CTRL2_REG	0x6781	0x6791
0x42	AGC_REG	No Change	0x0248
0x43	AGC12_TH_REG	No Change	0x399A
0x44	AGC12_ALPHA_REG	No Change	0x0038
0x45	POSITIONING_REG	No Change	0x0000
0x46	DC_OFFSET_REG	No Change	0x0000
0x47	DC_OFFSET34_REG	R	0x0000
0x48	IQ_DC_OFFSET_REG	No Change	0x4000
0x49	IF_CTRL_REG	No Change	0x059C
0x4A	REF_OSC_REG	No Change	0x3868
0x4B	ADC_CTRL_REG	No Change	0x000F
0x4C	RFIO_CTRL_REG	No Change	0x1000
0x4D	BIAS_CTRL_REG	No Change	0x0007
0x4E	DRIFT_TEST_REG	R	0x0000
0x4F	TEST_MODE_REG	No Change	0x0001
0x50	LDO_TEST_REG	No Change	0x0000
0x56	PLL_CTRL5_REG	No Change	0x0000
0x57	PLL_CTRL6_REG	No Change	0x0800
0x58	TEST_CTRL3_REG	See Table 3 for details.	0x03A8
0x59	PA_CTRL1_REG	See Table 3 for details.	0x0A50
0x5A	PA_CTRL2_REG	No Change	0x7700
0x5B	IFCAL_RESULT_REG	R	0x0020
0x5C	DC_OFFSET12_REG	R	0x0000
0x5D	AGC_RESULT_REG	R	0x0110

Table 9: RF Test register values

Address	Port	Recommended Values	Reset Value
0x5E	GAUSS_GAIN_MSB_REG	R	0x0000
0x5F	RXFE_CTRL_REG	No Change	0x011C
0x62	TEST_MODE2_REG	See Table 3 for details.	0x068

6.0 Registers description detailed

Table 10: BURST_MODE_CTRL_REG (0x00) (Note 17)

Note 17: This register takes the address bits A[1:0] as extra data.

Bit	Mode	Symbol	Description	Reset
17-16	W	RX_TX	0 = Toggle the enabling of the radio timer. If no DCFs are active, bits 15-0 can be programmed without starting DCFs. 1 = Initiate a new transmit slot 2 = Initiate a new receive slot 3 = Initiate a general calibration slot (ref. Section 4.2)	0
15-14	R/W	FAD	0 = use antenna1 (connected to P0) 1 = use antenna 2 (connected to P0n) 2 = Do not use antenna switching (P0, P0n inactive) 3 = Use the best antenna (in RX mode), use the best antenna from the previous RX-slot (in TX mode)	0
13	R/W	RSSI_MODE	In RX Mode: Set the behavior of the RSSI measurement 0 = use EO_RSSI as the Stop SI for RSSIPH 1 = use EO_RX as the Stop SI for RSSIPH In TX Mode this bit has no function	0
12-7	R/W	RFCAL	RF calibration setting (ref. RFCAL_CTRL_REG)	0
6-0	R/W	CN	RF channel number (ref. PLL_CTRL_REG)	0

Table 11: ALW_EN_REG (0x04)

Bit	Mode	Symbol	Description	Reset
13	R/W	TX_DATA_ALW_EN	TX_DATA interface always enable	0
12	R/W	PA_ALW_EN	RF power-amplifier driver always enable	0
11	R/W	LNAMIX_ALW_EN	low-noise amplifier and mixer always enable	0
10	R/W	IF_ALW_EN	intermediate-frequency filter always enable	0
9	R/W	ADC_ALW_EN	analog-to-digital converter always enable	0
8	R/W	DEM_ALW_EN	demodulator always enable	0
7	R/W	RSSIPH_ALW_EN	RSSI peak-hold computation always enable	0
6	R/W	BIAS_ALW_EN	bias circuit always enable	0
5	R/W	SYNTH_ALW_EN	voltage-controlled oscillator always enable	0
4	R/W	PLLCLOSED_ALW_EN	PLL closed loop always enable	0
3	R/W	PORT1_ALW_EN	PORT1 always enable	0
2	R/W	PORT2_ALW_EN	PORT2 always enable	0
1	R/W	PA_DRIVER_STAGE_ALW_EN	PA driver stage always enable	0
0	R/W	PA_FINAL_STAGE_ALW_EN	PA final stage always enable	0

Table 12: PORT_RSSI_SI_REG (0x05)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_RSSI_VAL	End-of-RSSI switch instant activation value	0x1C
7-0	R/W	SO_PORT_VAL	Start-of-PORT switch instant activation value	0x00

Table 13: TX_SI_REG (0x06)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_TX_VAL	End-of-TX switch instant activation value	0x4E
7-0	R/W	SO_TX_VAL	Start-of-TX switch instant activation value	0x12

Table 14: RX_SI_REG (0x07)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	EO_RX_VAL	End-of-RX switch instant activation value	0x4E
7-0	R/W	SO_RX_VAL	Start-of-RX switch instant activation value	0x13

Table 15: PORT1_DCF_REG (0x08)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, MUST be set to 0.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	1
12	R/W	EN_BY_TX	enable DCF in TX slot	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x0D
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX or SO_PORT)	0x06

Table 16: PORT2_DCF_REG (0x09)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, MUST be set to 0.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x11
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX or SO_PORT)	0x1E

Table 17: PA_DRIVER_STAGE_DCF_REG (0x0A)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, MUST be set to 0.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot (for test purposes only)	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x00
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX or SO_PORT)	0x2D

Table 18: PA_FINAL_STAGE_DCF_REG (0x0B)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, MUST be set to 0.	0
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot (for test purposes only)	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x00
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX or SO_PORT)	0x2D

Table 19: PLLCLOSED_DCF_REG (0x0C)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_TRX as the Stop SI; 1 = use EO_TRX as the Stop SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (SO_TRX or SO_TX/EO_RX)	0x1C
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x20

Table 20: SYNTH_DCF_REG (0x0D)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop EO_TRX	0x1D
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x14

Table 21: BIAS_DCF_REG (0x0E)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x1E
5-0	R/W	SET_OFFSET	offset w.r.t. SO_SLOT	0x00

Table 22: RSSIPH_DCF_REG (0x0F)

Bit	Mode	Symbol	Description	Reset
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (EO_RSSI or EO_RX)	0x01
5-0	R/W	SET_OFFSET	offset w.r.t. start instant of the demodulator	0x2A

Table 23: DEM_DCF_REG (0x10)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x0B
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x0F

Table 24: ADC_DCF_REG (0x11)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x13
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x00

Table 25: IF_DCF_REG (0x12)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x11
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x02

Table 26: LNAMIX_DCF_REG (0x13)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_SLOT as the Start SI; 1 = use SO_RX as the Start SI.	1
13	-			0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_RX	0x0F
5-0	R/W	SET_OFFSET	offset w.r.t. SO_RX	0x02

Table 27: PA_DCF_REG (0x14)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	PADR_SSI	Select the PA start switch instance: 0x0 = SO_TRX 0x1 = SO_PORT 0x2, 0x3 = SO_SLOT	0x0
13	R/W	RX_SENSITIVE	enable PA also in RX mode (for test purposes only)	0
12	R/W	DIS	disable DCF irrespective of the switch instants	0
11-6	R/W	RESET_OFFSET	offset w.r.t. stop switch instant (EO_TX or EO_TRX)	0x1C
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (depending on PA_SSI)	0x19

Table 28: FAD_WINDOW_DCF_REG (0x15)

Bit	Mode	Symbol	Description	Reset
11-6	R/W	FAD_DECIDE	moment when FAD algorithm makes a choice between either of the two antennas. (offset w.r.t. start instant of the demodulator)	0x28
5-0	R/W	FAD_SWAP	moment when the FAD algorithm starts measuring from the second antenna. (offset w.r.t. start instant of the demodulator)	0x23

Table 29: TX_DATA_DCF_REG (0x16)

Bit	Mode	Symbol	Description	Reset
14	R/W	SSI	0 = use SO_TRX as the Start SI; 1 = use SO_PORT as the Start SI.	0
13	R/W	EN_BY_RX	enable DCF in RX slot (for test purposes only)	0
12	R/W	EN_BY_TX	enable DCF in TX slot	1
11-6	R/W	RESET_OFFSET	offset w.r.t. EO_TRX	0x1C
5-0	R/W	SET_OFFSET	offset w.r.t. start switch instant (SO_TRX or SO_PORT)	0x14

Table 30: RFCAL_CTRL_REG (0x20)

Bit	Mode	Symbol	Description	Reset
8-7	R/W	GENCAL_MODE	The general calibration mode 0: Only the VCO, IF filter and IF amplifier are calibrated 1: Only the VCO and modulation gain are calibrated 2: The VCO, IF filter, IF amplifier and modulation gain are calibrated. The modulation gain is calibrated in parallel with the IF filter and IF amplifier. 3: The VCO, IF filter, IF amplifier and modulation gain are calibrated. The modulation gain is calibrated after the IF filter and IF amplifier.	0
6-5	R/W	RFCAL_PERIOD	Length of a (single) RF calibration step 0 = 1.36µs 1 = 2.51µs 2 = 3.67µs 3 = 4.83µs	0x1
4-3	R/W	RFCAL_MODE	0 = No RF calibration, use the value in RFCAL field 1 = RF calibration using BMCW[RFCAL] as CC_{start} 2, 3 = RF calibration using RSSI_REG[RFCAL_CAP] as CC_{start}	0x2
2-0	R/W	RFCAL_STEPS	Number of measurement steps used for RF calibration (0-6) 0 = No updates, use CC_{start} as defined by RFCAL_MODE 1 = Perform 1 update, ... 6 = Perform 6 updates, 7 = Perform 7 updates in a special sequence such that the VCO frequency is minimized during calibration. (This is the setting, used during general calibration)	0x3

Table 31: DEM_CTRL_REG (0x22)

Bit	Mode	Symbol	Description	Reset
15-8	R/W	SLICE_VAL	Slice or threshold value in 2's complement (-1 to 127/128) write: fixed-slice value when SLICE_EN = 0; threshold value for enabling positive frequency offset compensation when SLICE_EN = 1 & AFC_EN = 1. (recommended 0x0A in FBR, 0x14 in HBR);	0x00
7	R/W	SLICE_EARLY	compute slice level by averaging 0 = the post-demodulation filter output 1 = the post-demodulation filter input	0
6-3	-			0
2	R/W	RX_DATA_OE	Enable the RX_DATA output when DEM_DCF is active 0: Always enabled 1: Enabled when DEM_DCF = 1. The RX_DATA output is otherwise in tri-state mode.	0
1	R/W	SLICE_EN	0 = use slice value given by SLICE_VAL **(value 0 must be used in search mode)** 1 = use measured slice value	0
0	R/W	DEM_INVERT	0 = normal demodulator output 1 = inverted demodulator output	1

Table 32: PREAMBLE_REG (0x23)

Bit	Mode	Symbol	Description	Reset
15	R/W	SYNC_RX_DATA	0 = output raw slicer output on RX_DATA 1 = output synchronized slicer output on RX_DATA	0
14	R/W	HALF_BIT_RATE	0 = normal operation 1 = set the DEM clock frequency to REFCLK/2, operate at half bit rate.	0
13	R/W	GATE_DATA	0 = output demodulator permanently active 1 = output demodulator equal to 0 until 4 symbols after PREAMBLE_DEL	0
12-11	R/W	PREAMBLE_SYM	Compute final slice level by 0 = averaging 4 symbols 1 = averaging 8 symbols 2 = averaging 12 symbols 3 = averaging 14 symbols	0x0
10-9	R/W	AFC_SETTLE_DEL	Delay in symbols (0, 1, 2, or 3) between switching LO and start of final slice-level computation	0x2
8	R/W	AFC_EN	0 = use digital LO as given by AFC_VAL (see above) **(value 0 must be used in search mode)** 1 = enable automatic frequency compensation	0
7-6	R/W	AFC_VAL	Value supplied (write) or computed (read) for LO: 0 = 864 kHz 1 = 943 kHz 2, 3 = 798 kHz	0x0
5-0	R/W	PREAMBLE_DEL	Delay in symbols of start moment for frequency compensation, measured from enabling time of demodulator	0x2A

Table 33: SLICER_RESULT_REG (0x2D)

Bit	Mode	Symbol	Description	Reset
15-8	R	SLICE_VAL	Slice value computed by active slicer (not the written value)	0x00
7-6	R	AFC_VAL	Computed result for LO after AFC: 0 = 864 kHz 1 = 943 kHz 2, 3 = 798 kHz	0x0
5-0	-		Reserved	0

Table 34: FAFC_CTRL_REG (0x60)

Bit	Mode	Symbol	Description	Reset
15-11	-		-	-
10-3	R/W	FAST_VAL	Frequency offset compensation value Frequency offset = FAST_VAL × 81/16 kHz	0x0
2	R/W	FAST_AFC_EN	Enable the Fast Automatic Frequency Control (FAFC) '0': Disable the FAFC '1': Start the FAFC after PREAMBLE_DEL symbols	1
1	R/W	FAFC_MEAN	Set the number of preamble symbols for the frequency offset estimation '0': Two preamble symbols '1': Four preamble symbols	0
0	R/W	FAFC_EN	Enable the Fast Automatic Frequency Control (FAFC) '0': Use FAFC_CTRL_REG[FAST_VAL] for the frequency offset compensation '1': Use the estimated frequency offset for the frequency offset compensation FAFC_RESULT_REG[FAST_VAL] **(value 0 must be used in search mode)**	1

Table 35: FAFC_RESULT_REG (0x61)

Bit	Mode	Symbol	Description	Reset
15-8	-		-	0
7-0	R	FAST_VAL	Estimated frequency offset Frequency offset = FAST_VAL × 81/16 kHz	0x0

Table 36: RSSI_REG (0x24)

Bit	Mode	Symbol	Description	Reset
14	R	FAD_CHOICE	The antenna chosen by the FAD algorithm 0 = Antenna 1 (connected to P0) 1 = Antenna 2 (connected to P0n)	0
13-8	R	RSSI_VAL	Received Signal Strength Indication. Reading this register resets the RSSI peak-hold circuit, allowing a very simple search mode. (Reset via MWR programming only)	0x00
7-6	-			
5-0	R	RFCAL_CAP	Return value of the RF calibration algorithm	0x30

Table 37: PORT_CTRL_REG (0x25)

Bit	Mode	Symbol	Description	Reset
4	R/W	ANT_INACTIVE_VAL	output value when P0/P0n inactive.	0
3	-	-	Reserved, Must be kept 0	0
2	-	-	Reserved, Must be kept 0	0
1	-		Reserved, Must be kept 0	0
0	R/W	PORT1_INV	0 = PORT1 DCF on P1 pin; 1 = inverted PORT1 DCF on P1 pin.	0

Table 38: PAD_IO_REG (0x26) (Note 18)

Note 18: All ports and test pads are supplied by an internal LDO. Their inputs and outputs can only be enabled when BIAS_DCF is active. When BIAS_DCF is inactive, the ports and test pads are in tri-state.

Bit	Mode	Symbol	Description	Reset
5-0	R/W	PAD_OE	enable digital output on pads (MSB-LSB order is: P2, P1, P0n, P0).	0x3F
6	R/W	P0_IE	enable digital input on pad P0	0
5	-	-	Reserved, May be kept to 1	1
4	-	-	Reserved, May be kept to 1	1
3	R/W	P2_OE	enable digital output on pad P2	1
2	R/W	P1_OE	enable digital output on pad P1	1
1	R/W	P0N_OE	enable digital output on pad P0n	1
0	R/W	P0_OE	enable digital output on pad P0	1

Table 39: BANDGAP_REG (0x27)

Bit	Mode	Symbol	Description	Reset
15-6	-		Reserved, must be kept 0	0
5-4	R/W	BANDGAP_VIT	00 = <- default value may not be changed 10 = Voltage and current -5.6% <- for test purposes only! 01 = Voltage and current +5.6% <- for test purposes only.!	00
3-0	R/W	BANDGAP_VI	Bandgap reference voltage and current adjust to trim AVD. 0000 = -5.6% 0001 = -4.9% 0010 = -4.2% 0011 = -3.5% 0100 = -2.8% 0101 = -2.1% 0110 = -1.4% 0111 = -0.7% 1000 = midlevel <- default value. 1001 = +0.7% 1010 = +1.4% 1011 = +2.1% 1100 = +2.8% 1101 = +3.5% 1110 = +4.2% 1111 = +4.9% <- Reset Value	0xF

Table 40: PLL_CTRL1_REG (0x28)

Bit	Mode	Symbol	Description	Reset
15-14	R/W	CS_MO	Channel spacing in multiples of f_{IF} 0 = CS = 1 1 = CS = 2 2 = CS = 3 3 = CS = 4.	0x1
13	R/W	SGN_NEG	0 = SGN = +1, Channels numbers count up 1 = SGN = -1, Channel numbers count down	1
12-0	R/W	CH_ZERO	Base channel number (CH0) in multiples of f_{IF}	0x894

Table 41: PLL_CTRL2_REG (0x29)

Bit	Mode	Symbol	Description	Reset
15	-		Reserved, must be kept 0	0
14	R/W	MODE20M	0 = 10.368 MHz XTAL 1 = 20.736 MHz XTAL	0
13-8	R/W	MODINDEX	Modulation index *h* = MODINDEX/64	0x20
7-0	R/W	GAUSS_GAIN	Externally supplied Gaussian DAC volume,	0x36

Table 42: PLL_CTRL3_REG (0x2A)

Bit	Mode	Symbol	Description	Reset
12-11	R/W	LOCK_TIME	Lock time of the PLL 0 = 55µs 1 = 70µs (recommended with best residual FM) 2, 3 = not allowed, can give synchronisation errors in extreme cases.	0x1
10	R/W		Reserved	0
9-0	R/W		Reserved	0x000

Table 43: PLL_CTRL4_REG (0x2B)

Bit	Mode	Symbol	Description	Reset
15-13	R/W	KMOD_ALPHA	Kmod channel dependent trimming constant. The modulation gain in the direct path is modified with a factor: 1-SGN×KMOD_ALPHA×CN/2048 0 = no scaling 1 = ~~Preferred for ISM5G8, half rate,~~ Reserved 2 = ~~Preferred for ISM5G8, full rate,~~ Reserved 5 = Preferred for US-DECT 5 = Preferred for EU-DECT	0x5
12-11	R/W	SD2_ORDER	Sigma-Delta order after FASTLOCK_PERIOD	3
10-9	-			0
8	R/W	MODCAL_TRIG	Trigger modulation gain calibration by a single rising edge.	0
7-0	R/W	MODCAL_PERIOD	Length of the modulation gain calibration step time = MODCAL_PERIOD/288kHz	0x24

Table 44: SLICER_REG (0x2C)

Bit	Mode	Symbol	Description	Reset
7-2	R/W	SLICE_LOW	threshold slicer value in 2s complement (-32/128 to 31/128) for enabling negative frequency-offset compensation (recommended 0x38 in FBR, 0x30 in HBR)	0x38
1	R/W	DECIDE_ON_AVG	when SYNC_RX_DATA enabled: 0 = decide on central sample of symbol 1 = decide on sample average	0
0	R/W	TRACK_SLICE	0 = slice-level computation enabled during preamble only 1 = slice-level computation enabled in entire slot	0

Table 45: GAUSS_GAIN_RESULT_REG (0x2E)

Bit	Mode	Symbol	Description	Reset
15-8	R	-	Reserved	0
7-0	R	GAUSS_GAIN	Corrected Gaussian DAC volume after modulation gain calibration.	0

Table 46: TX_DATA_CTRL_REG (0x2F)

Bit	Mode	Symbol	Description	Reset
7-6	R/W	TX_DATA_MIDLEVEL	Threshold values for the analogue interface 00: Vhigh = 1000 mV, Vlow = 800 mV 01: Vhigh = 900 mV, Vlow = 700 mV 10: Vhigh = 950 mV, Vlow = 750 mV 11: Vhigh = 1050 mV, Vlow = 850 mV	0
5-4	R/W	TX_DATA_MODE	TX_DATA interface mode 00: Analogue interface 01: Interface enabled with TX_DATA_DCF 10: Interface enabled with TX_DATA_EN 11: Start bit detection	0
3-0	R/W	TX_DATA_DELAY	Delay added to the detection of the first bit.	2

Table 47: PA_CTRL1_REG (0x59)

Bit	Mode	Symbol	Description	Reset
15-12	R/W	PA_ATT_SET	PA pre-stage attenuator setting in steps of 0.5 dB. 0 is lowest, 0xF is highest attenuation	0x0
11-8	R/W	PA_CUR_SET2	PA final stage bias current	0xA
7-4	R/W	PA_CUR_SET1	PA first stage bias current	0x5
3-0	-			

Table 48: PA_CTRL2_REG (0x5A)

Bit	Mode	Symbol	Description	Reset
15-12	R/W	RAMP_SPEED2	PA final stage ramp speed	0x7
11-8	R/W	RAMP_SPEED1	PA first stage ramp speed	0x7
7-0	-			0

Table 49: MODCAL_RESULT1_REG (0x70)

Bit	Mode	Symbol	Description	Reset
15-0	R	MODCAL_N0	Reserved	0

Table 50: MODCAL_RESULT2_REG (0x71)

Bit	Mode	Symbol	Description	Reset
15-0	R	MODCAL_N1N2	Reserved	0

Table 51: CHIP_TEST_REG (0x7A)

Bit	Mode	Symbol	Description	Reset
15-8	R	CHIP_TEST1	Reserved for test purposes, device dependent value	0
7-0	R	CHIP_TEST2	Reserved for test purposes, device dependent value	0x20

Table 52: CHIP_ID1_REG (0x7B)

Bit	Mode	Symbol	Description	Reset
15-8	R	CHIP_ID1	First character of device type “4181” in ASCII.	0x34
7-0	R	CHIP_ID2	Second character of device type “4181” in ASCII.	0x31

Table 53: CHIP_ID2_REG (0x7C)

Bit	Mode	Symbol	Description	Reset
15-8	R	CHIP_ID3	Third character of device type “4181” in ASCII.	0x38
7-0	R	CHIP_ID4	Third character of device type “4181” in ASCII.	0x31

Table 54: CHIP_REVISION_REG (0x7D)

Bit	Mode	Symbol	Description	Reset
15-8	R	CHIP_SWC	Integer (default = 0) which is incremented if a silicon change has impact on the baseband processor Firmware. Can be used by software developers to write silicon revision dependent code.	0x00
7-0	R	REVISION_ID	Chip version, corresponds with type number in ASCII 0x41 = ‘A’, 0x42 = ‘B’	0x41

Table 55: CHIP_CONFIG1_REG (0x7E)

Bit	Mode	Symbol	Description	Reset
15-8	R	CHIP_CONFIG1	Reserved	0x20
7-0	R	CHIP_CONFIG2	Reserved	0x20

Table 56: CHIP_CONFIG2_REG (0x7F)

Bit	Mode	Symbol	Description	Reset
7-0	R	CHIP_CONFIG3	Reserved	0x20

7.0 Specifications

All MIN/MAX specification limits are guaranteed by design, or production test, or statistical methods unless note 19 is added to the parameter description. Typical values are informative.

Note 19: This parameter will not be tested in production. The MIN/MAX values are guaranteed by design and verified by characterization.

Table 57: ABSOLUTE MAXIMUM RATINGS (Note 20)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNITS
VBAT_ANA_max	Max voltage on VBAT_ANA1,VBAT_ANA2 and VBAT_ANA3			**3.6**	**V**
Vpa_max	Max voltage on TXp, TXn pins			**3.6**	**V**
Vdd_max	Max Core supply voltage (VDD_DIG-VSS)			**2.0**	**V**
Vddio_max	Max IO supply voltage (VDDIO-VSS)			**3.6**	**V**
Vesd_hbm	ESD voltage according to human body model			**2000**	**V**
Vesd_mm	ESD voltage according to machine model			**100**	**V**

Note 20: Absolute maximum ratings are those values that may be applied for maximum 50 hours. Beyond these values, damage to the device may occur.

Table 58: OPERATING CONDITIONS (Note 21)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
VBAT_ANA	Supply voltage VBAT_ANAx-VSS		**1.9**		**3.45**	**V**
VDD_DIG	Supply voltages VDD_DIG-VSS, Digital operation guaranteed down-to reset level		**1.60**	**1.8**	**1.98**	**V**
VDDIO	IO supply voltages VDDIO-VSS,		**1.60**	**1.8**	**3.45**	**V**
Vdig	Voltage on all digital pin without backdrive protection				**VDDIO + 0.3**	**V**
Vana	Voltage on analogue pins				**VBAT_ANA+ 0.3**	**V**
Vpa	Voltage on TXp, TXn pins				**3.45**	**V**
Vpin_neg	Minimum voltage on any pin		**VSS-0.3**			**V**
Ppackage	Package power dissipation @ 25 °C				**1**	**W**
R_ref	Reference resistor (2% accuracy)		**54.9**	**56**	**57.1**	**kΩ**
f_REFCLK	Refer to CMOS digital input (see Table 60)			**10.368**		**MHz**
Tstorage	Refer to SiTel Portal document “Floor and shelf life advisory”					
TA	Ambient temperature with all specifications guaranteed	**(Note 22)**	**-20**		**+60**	**°C**
TA_70	Ambient temperature with limited specifications and mentioned conditions: RF Rx Sensitivity reduces 0.5 dB above 60°C		**-20**		**+70**	**°C**

Note 21: Within the specified limits, a life time of 10 years is guaranteed.

Note 22: Within this temperature range full operation is guaranteed

7.1 ELECTRICAL CHARACTERISTICS

VDD_DIG = 1.8 Volt and VDDIO =1.8 Volt. All signals are related to VSS. Typical values are at +25 °C. MAX and MIN values are over the full temperature range TA. Crystal frequency = 10.368 MHz unless specified otherwise.

Table 59: RF Supply currents

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Idd_PDN_1a	Total supply current without the reference clock **(Note 23)**	ALW_EN_REG = 0x0000, (VBAT_ANA = 2.0 V)	-	-	**20**	µA
Idd_PDN_1b	Total supply current without the reference clock **(Note 23)**	ALW_EN_REG = 0x0000, (VBAT_ANA = 3.2 V)	-	-	**20**	µA
Idd_PDN_1a_T	Total supply current without the reference clock (full temperature range)	ALW_EN_REG = 0x0000, (VBAT_ANA = 2.0 V)	-	-	**30**	µA
Idd_PDN_1b_T	Total supply current without the reference clock (full temperature range)	ALW_EN_REG = 0x0000, (VBAT_ANA = 3.2 V)	-	-	**40**	µA
Idd_PDN_2	Total supply current with digital reference clock applied	ALW_EN_REG = 0x0000	-	**0.3**	**1**	**mA**
Isupply_RX	Total supply current in receive mode	ALW_EN_REG = 0x0FE0	-	**68**	**96**	**mA**
Isupply_TX	Total supply current in transmit mode	ALW_EN_REG = 0x1060	-	**78**	**134**	**mA**
Isupply_TUNE	Total supply current in tuning mode	ALW_EN_REG = 0x0070	-	**24**	**34**	**mA**
Isupply_CAL	Average supply current during General Calibration	BURSTMODE_CTRL_REG[RX_TX] = 0x3	-	**10**		**mA**

Note 23: Idd_PDN_1a and Idd_PDN_1b are only valid for TA = 25°C. Use Idd_PDN_1a_T or Idd_PDN_1b_T for the full termperature range specification.

Table 60: Digital and analogue switching inputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vil_dig	Logic 0 input level all digital pads	VDDIO = 1.6-3.45 V			**0.3*VDDIO**	**V**
Vih_dig	Logic 1 input level all digital pads	VDDIO = 1.6-3.45 V	**0.7*VDDIO**			**V**
Ileak_hi	Input current of all inputs with (programmable) pull-down resistors disabled.	VDD_DIG = 1.8V			**10**	**uA**
Ileak_lo	Input current of all inputs with (programmable) pull-up resistors disabled.	Vin = VSS			**10**	**uA**

Table 61: Digital outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vol_2ma	Logic 0 output level	Iout = 2 mA VDDIO = 1.6 V			**0.2*VDDIO**	**V**
Vol_8ma	Logic 0 output level	Iout = 8 mA VDDIO = 3.3 V			**0.2*VDDIO**	**V**
Voh_2ma	Logic 1 output level	Iout = 2 mA VDDIO = 1.6 V	**0.8*VDDIO**			**V**
Voh_8ma	Logic 1 output level	Iout = 8 mA VDDIO = 3.3 V	**0.8*VDDIO**			**V**

Note 24: Output must stay below Vil or above Vih to avoid switching cross currents in the input stage.

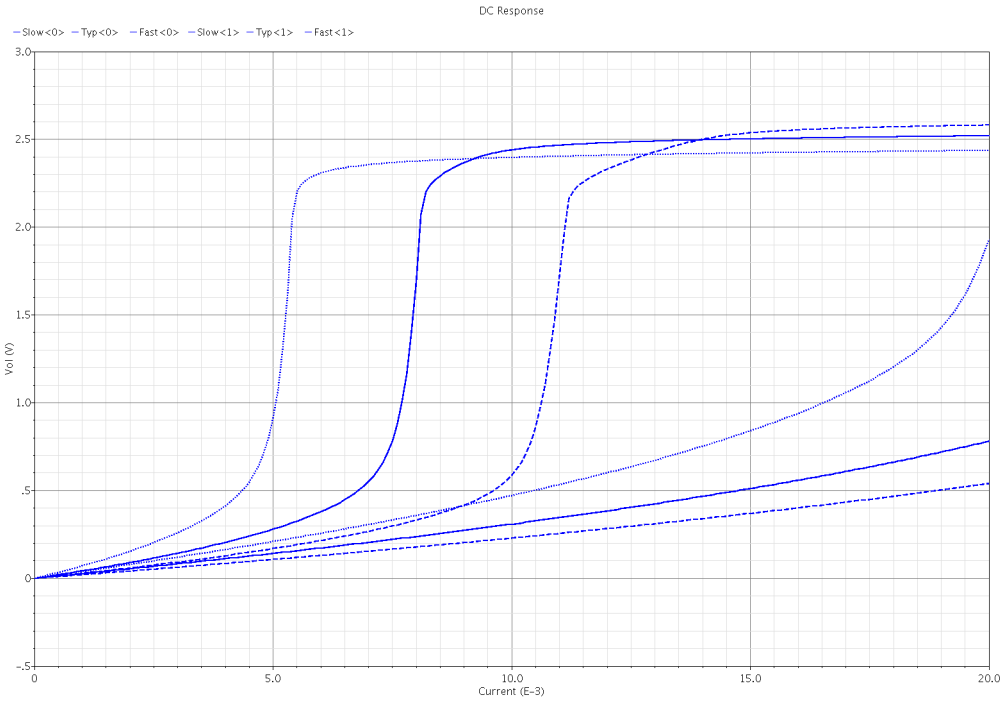

Figure 10 Digital pads output characteristics, VDDIO = 1.8 V and VDDIO = 3.3 V

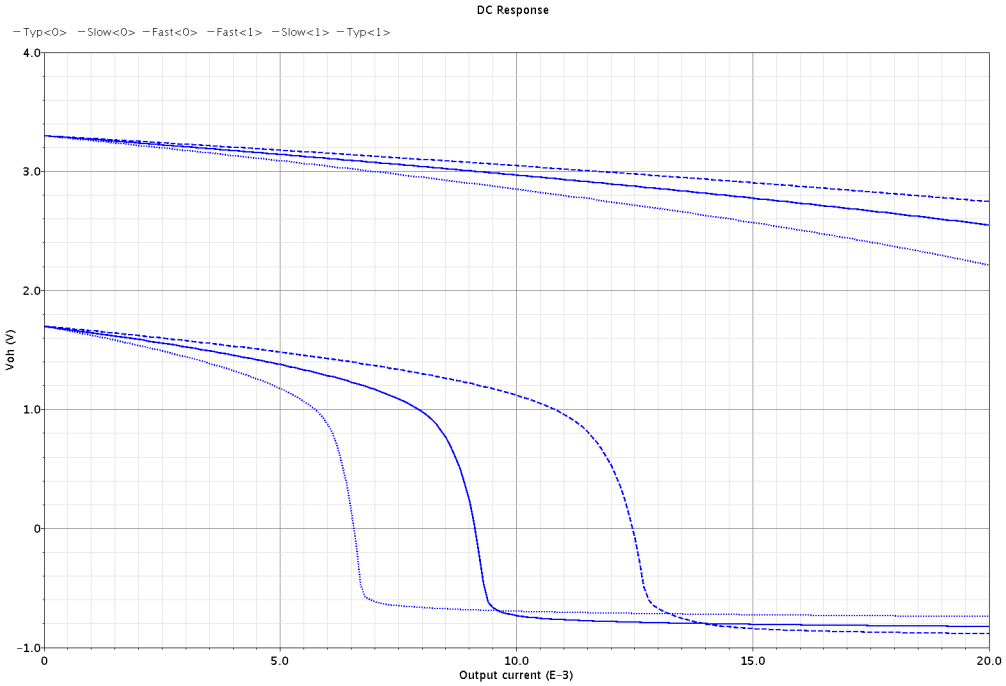

Figure 10 Digital pads output characteristics, VDDIO = 1.8 V and VDDIO = 3.3 V

Table 62: Regulated digital RF outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Voh_s	High level output voltage for RF 'switch' ports, as used for e.g. PIN diode switches. (measured on P0, P0n, P1 and P2 simulta-neously)	Iout = -5 mA Internal core supply = 1.7V **(Note 25)**	**1.7-0.25**			**V**
Vol_r	Low level output voltage for RF 'switch' ports, as used for e.g. PIN diode switches. (measured on P0, P0n, P1 and P2 simulta-neously)	Iout = 2 mA Internal core supply = 1.7V			**0.34**	**V**

Note 25: The RF ports can provide 8 mA@0.2x1.7V, but they are tested with 2 resp 5 mA

Table 63: MICROWIRE™ timing

Parameter	Description	Condition	Min	Typ	Max	Units
tSK_setup	SIO to rising edge SK setup time in write mode		15	-	-	ns
tSK_hold	SIO to rising edge SK hold time in write mode		15	-	-	ns
tSIO_rd_valid	SIO valid after rising edge SK in read mode.		35	-	-	ns
tSK2LE	Rising edge SK to falling edge LE separation		15	-	-	ns
tLE_high	LE high phase (LDO refresh)	BIAS DCF = '0'	3	5	-	µs
tLE_low	LE low phase		20	-	-	ns
fSK	SK frequency		-	-	10.368	MHz

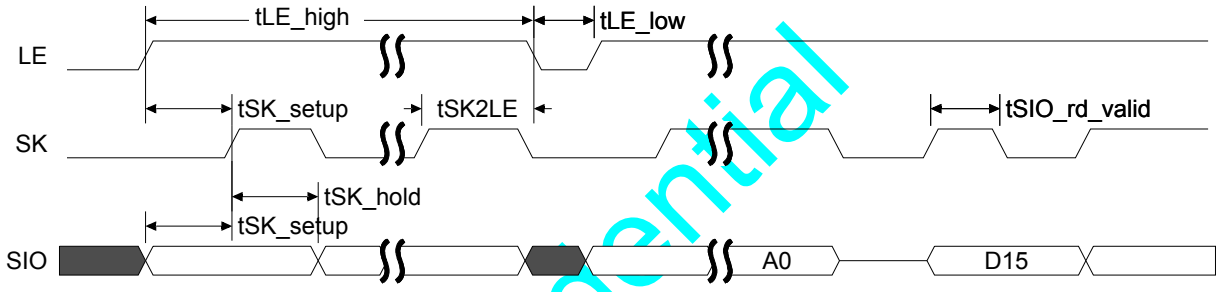

Figure 11 MICROWIRE™ signal-edge pairs used for timing specification.

Table 64: Digital Control

Parameter	Description	Condition	Min	Typ	Max	Units
tLE_start	Falling edge LE to active dynamic control function	LE for BMCW indicating start of burst **(Note 26)**	2.60	-	3.47	µs
tLE_ALW_EN	Falling edge LE to DCF activation/ deactivation through ALW_EN	LE for ALW_EN_REG **(Note 26)**	0.00	-	0.87	µs

Note 26: Guaranteed by design when f_REFCLK=10.368MHz.

Table 65: RSTn Pin

Parameter	Description	Condition	Min	Typ	Max	Units
t_low	Low time to reset device	Capacitance minimally 470pF	10	-	-	µs

7.2 RADIO RECEIVER SPECIFICATION

For s-parameters of the input RXp, RXn and design guidelines for an RX matching network, please refer to SiTel Semiconductor Application Note AN-D-177. All measurements are done in burst mode, using the preferred settings given in sections 5.1 and 5.2.

Table 66: Receiver (Note 27), (Note 28), (Note 29)

Note 27: R_ref = 56kΩ., Fxtal = 10.368 MHz, BANDGAP_REG[BANDGAP_VI] trimmed.

Note 28: All Rx powers specified at input of SiTel proposed matching network which is optimized at channel 5.

Note 29: Tests performed on DECT channel 0, 5, 9 (EU-DECT), 23 and 27 (DECT6.0), using frequency deviation Δf = 288kHz, unless specified otherwise.

Note 30: Korean DECT band (1785-1805MHz) is supported. Characterisation results are available upon request.

Note 31: Due to the low IF architecture, the selectivity of the receiver is better for interferers that are at lower frequencies than the wanted channel. The worst case results (i.e. for interferers at higher frequencies than the wanted channel) are noted here. For interferers at lower frequencies than the wanted channel, the IPL results are typically -34dBm.

Note 32: Guaranteed by design. All deviations from the ideal slope are taken into account in RSSI_acc.

Parameter	Description	Condition	Min	Typ	Max	Units
f_in	Receiver input frequency range **(Note 30)**		**1880**	**-**	**1950**	**MHz**
P_Rx	Receiver sensitivity at standard frequency deviation	TA = 25°C	**-**	**-96**	**-93**	**dBm**
P_Rx_350	Receiver sensitivity at practical frequency deviation	TA = 25°C; Δf = 350kHz	**-**	**-98**	**-95**	**dBm**
P_Rx_T	Receiver sensitivity, full temperature range	0°C ≤ TA ≤ +55°C	**-**	**-**	**-92**	**dBm**
P_Rx_f	Receiver sensitivity, degraded by frequency offset f_os	−100 kHz ≤ f_os ≤ +100 kHz; TA = 25°C	**-**	**-**	**-90**	**dBm**
P_in	Receiver input power range	TA = 25°C BER ≤ 1E-5	**-**	**-**	**+13**	**dBm**
IPL	Intermodulation performance level (EN 301 406 section 4.5.7.6) **(Note 31)**	TA = 25°C	**-38.5**	**-37**	**-**	**dBm**
CI_0	Interferer performance (EN 301 406 section 4.5.7.3)	Y = M; TA=25°C	**-**	**9**	**10**	**dB**
CI_1		Y = M±1; TA = 25°C	**-**	**-18**	**-13**	**dB**
CI_2		Y = M±2; TA = 25°C	**-**	**-48**	**-34**	**dB**
CI_3		Y = any other DECT channel in range [0, 9]∪[23, 27]; TA=25°C	**-**	**-56**	**-40**	**dB**
P_Rx_RSSI_min	lower limit of RSSI monotonous range	TA = 25°C	**-**	**-100**	**-95**	**dBm**
P_Rx_RSSI_max	upper limit of RSSI monotonous range	TA = 25°C	**-31**	**-28**	**-**	**dBm**
RSSI_acc	RSSI accuracy. Tolerance of P_Rx when RSSI_VAL = *X* on a slot to slot basis.	Measured in burst mode; RSSI_VAL is a 4 sample average; 25 < *X* < 45, TA = 25°C	**-3**	**-**	**3**	**dB**
RSSI_res	RSSI resolution **(Note 32)**	Guaranteed by design	**-**	**2**	**-**	**dB/step**

7.3 RADIO SYNTHESIZER SPECIFICATION

All measurements are done in burst mode, using the preferred settings given in sections 5.1 and 5.2.

Table 67: Synthesizer (Note 33)

Note 33: R_ref = 56kΩ, Fxtal = 10.368MHz, BANDGAP_REG[BANDGAP_VI] trimmed.

Note 34: Korean DECT band (1785-1805MHz) is supported. Characterisation results are available upon request.

Note 35: This is the difference between SET_OFFSETs of PLLCLOSED_DCF and SYNTH_DCF. This time serves to settle the DC biassing of the analogue synthesizer blocks after the LDO's and reference bias currents have already reached their steady state. Preferred settings are given in section 5.1 as 32 - 20 = 12 DECT symbol periods (= 10.4 µs).

Note 36: Guaranteed by design. Values are defined by digital state machine and provided for reference only.

Note 37: Tests performed on DECT channel 0, 5, 9 (EU-DECT), 23 and 27 (DECT6.0), after modulation gain calibration is performed and with setting PLL_CTRL2_REG[MODINDEX] = 0x20 (h = 0.5 i.e. Δf = 288kHz). ACP6 systematically suffers from spurious components due to the reference frequency. EN 301 406 allows 1 exception for EU-DECT channels at -33 dBm rather than -44 dBm. For any channel M in the EU-DECT band either Y = M - 6 or Y = M + 6 is situated in the EU-DECT band. Typically both ACP6 results adhere to the more severe spec of -44 dBm.

Note 38: Residual FM depends on the measurement bandwidth. The most appropriate bandwidth is the IF bandwidth of the receiver (1.2 MHz centered at 864 kHz). Due to equipment constraints the measurement bandwidth is set to 1.3 MHz (single sideband from 200 kHz to 1.5 MHz).

Note 39: The minimum fine tuning time is usually larger than 10 µs, but is not a part of the radio synthesizer specification.

Parameter	Description	Condition	Min	Typ	Max	Units
f_lo	Local oscillator frequency range **(Note 34)**		**1880**	**-**	**1950**	**MHz**
t_settle	Settling time of synthesizer blocks before coarse calibration may be started **(Note 35)**		**10**			**µs**
t_cc_0	Time needed for coarse calibration (fastest), **(Note 36)**	RFCAL_PERIOD = 0	**-**	**1.36**	**-**	**µs/step**
t_cc_1	Time needed for coarse calibration, **(Note 36)**	RFCAL_PERIOD = 1	**-**	**2.51**	**-**	**µs/step**
t_cc_2	Time needed for coarse calibration, **(Note 36)**	RFCAL_PERIOD = 2	**-**	**3.67**	**-**	**µs/step**
t_cc_3	Time needed for coarse calibration (most accurate), **(Note 36)**	RFCAL_PERIOD = 3	**-**	**4.83**	**-**	**µs/step**
t_lock_1	Time needed for fine tuning, **(Note 39)**	LOCK_TIME = 1	**-**	**25**	**40**	**µs**
ACP1	Adjacent channel power ratio (EN 301 406 section 4.5.6.2) **(Note 37)**	Y=M±1	**-**	**-20**	**-8**	**dBm**
ACP2		Y=M±2	**-**	**-45**	**-30**	**dBm**
ACP3		Y=M±3	**-**	**-50**	**-41**	**dBm**
ACP4		Y=M±4	**-**	**-50**	**-44**	**dBm**
ACP5		Y=M±5	**-**	**-50**	**-44**	**dBm**
ACP6		Y=M±6	**-**	**-45**	**-33**	**dBm**
ACP7		Y=M±7	**-**	**-50**	**-44**	**dBm**
FMres	Residual FM on LO signal, measured in RX mode, **(Note 38)**			**3**	**5**	**kHz**

7.4 RADIO PA SPECIFICATION

For s-parameters of the input RF_TXp, RF_TXn and design guidelines for a TX matching network, please refer to SiTel Semiconductor Application Note AN-D-177. All measurements are done in burst mode, on SiTel Semiconductors characterization board using the preferred settings given in sections 5.1 and 5.2. Different TX matching and deviating from the settings provided in sections 5.1 and 5.2 will yield alternative results.

Table 68: AC characteristics (Note 40), (Note 41), (Note 42)

Note 40: Vrfpa = 2.4V; R_ref = 56 kΩ, Fxtal = 10.368MHz, BANDGAP_REG[BANDGAP_VI] trimmed.

Note 41: All Tx powers levels are specified at output of SiTel proposed matching network, which is optimized in HPM at channel 5.

Note 42: Tests performed on DECT channel 0, 5, 9 (EU-DECT), 23 and 27 (DECT6.0).

Note 43: Korean DECT band (1785-1805MHz) is supported. Characterisation results are available upon request.

Note 44: A software algorithm for power variation reduction is available in AN-D-169.

Note 45: Attack and release times are evaluated according to EN 301 406 sections 4.5.3.1.4 and 4.5.3.1.5. The higher power level is defined as P_{NTP}-1dB and the lower power level is 25µW (-16dBm). Values are given according to preferred settings from section 5.2.

Parameter	Description	Condition	Min	Typ	Max	Units
Frfpa_op	PA operating range **(Note 43)**		**1880**		**1930**	**MHz**
Prfpa_hpm	PA output power (see Table 3)	HPM; TA = 25°C	**24.0**	**25.2**	**26.5**	**dBm**
Prfpa_hpmu		HPM (DECT6.0); TA = 25°C		**23.5**		**dBm**
Prfpa_lpm		LPM; TA = 25°C		**12**		**dBm**
Prfpa_gpm		GPM; TA = 25°C		**4**		**dBm**
Prfpa_lrm		LRM; TA = 25°C		**-35**		**dBm**
dPrfpa_T	PA Power Variation across the whole temperature range	HPM; 0°C ≤ TA ≤ +55°C		**2**	**3**	**dB**
dPrfpa_f	PA Power Variation across the band (worst case EU-, DECT6.0)	HPM; TA = 25°C		**0**	**1**	**dB**
dPrfpa_sup1	PA Power Variation across standard supply range **(Note 44)**	HPM; 2.0V ≤ Vrfpa ≤ 3.6V		**2**	**2.5**	**dB**
dPrfpa_sup2	PA Power Variation across full supply range **(Note 44)**	HPM; 1.9V ≤ Vrfpa ≤ 3.6V		**2.5**	**3.0**	**dB**
Prfpa_h2	PA Harmonic Output Power @2×Frfpa_op	HPM; TA = 25°C		**-40**	**-30**	**dBm**
Prfpa_h3	PA Harmonic Output Power @3×Frfpa_op	HPM; TA = 25°C		**-40**	**-30**	**dBm**
Prfpa_h4	PA Harmonic Output Power @4×Frfpa_op	HPM; TA = 25°C		**-33**	**-30**	**dBm**
Prfpa_h5	PA Harmonic Output Power @5×Frfpa_op	HPM; TA = 25°C		**-45**	**-30**	**dBm**
Prfpa_h6	PA Harmonic Output Power @6×Frfpa_op	HPM; TA = 25°C		**-45**	**-30**	**dBm**
Nrfpa	PA enable duty cycle				**50**	%
Trfpa_atk	PA attack time **(Note 45)**	TA = 25°C	**0.8**	**1.25**	**1.5**	**µs**
Trfpa_rls	PA release time **(Note 45)**	TA = 25°C	**1**	**1.25**	**1.5**	**µs**
Irfpa_hpm	PA total current consumption (all stages, incl. LDO_PA)	HPM; TA = 25°C	**450**	**500**	**550**	**mA**
Irfpa_hpmu		HPM (DECT6.0); TA = 25°C		**350**		**mA**
Irfpa_lpm		LPM; TA = 25°C		**150**		**mA**
Irfpa_gpm		GPM; TA = 25°C		**100**		**mA**
Irfpa_lrm		LRM; TA = 25°C		**55**		**mA**
Irfpa_standby	PA standby current	PA off; TA = 25°C			**10**	**µA**

8.0 Package information

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8.1 MOISTURE SENSITIVITY LEVEL (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH. before the solder reflow process.

LMX4181 is qualified to MSL 3.

MSL Level	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30°C/85%RH

8.2 SOLDERING INFORMATION

Refer to the JEDEC standard J-STD-020 for relevant soldering information.
This document can be downloaded from http://www.jedec.org

8.3 PACKAGE OUTLINES

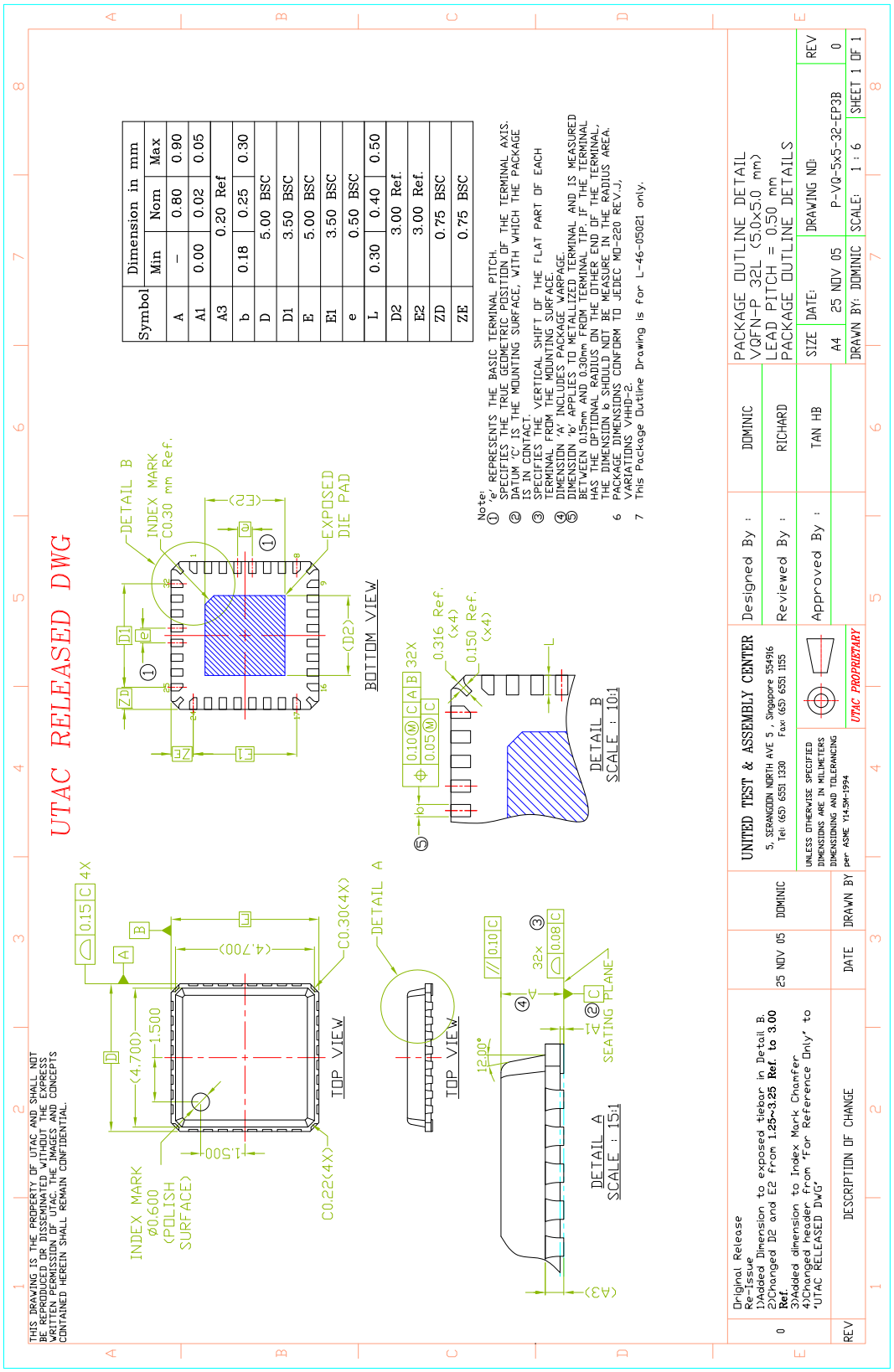

Figure 12 32 pins Very Thin Quad Flat No-lead (VQFN) package

Product Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
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