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The Belle II Silicon Vertex Detector

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Abstract

The KEKB factory (Tsukuba, Japan) has been shut down in mid-2010 after reaching a total integrated luminosity of $1\,\mathrm{ab}^{-1}$. Recently, the work on an upgrade of the collider (SuperKEKB), aiming at an ultimate luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, has started. This is 40 times the peak value of the previous system and thus also requires a redesign of the Belle detector (leading to Belle II), especially its Silicon Vertex Detector (SVD), which surrounds the beam pipe.

Similar to its predecessor, the future Belle II SVD will again consist of four layers of double-sided silicon strip sensors (DSSD), but at higher radii. Moreover, a double-layer PiXel Detector (PXD) will complement the SVD as the innermost sensing device. All DSSDs will be made from 6” silicon wafers and read out by APV25 chips, which were originally developed for the CMS experiment. That system was proven to meet the requirements for Belle II in matters of occupancy and dead time. Since the KEKB factory operates at relatively low energy, material inside the active volume has to be minimized in order to reduce multiple scattering. This can be achieved by the Origami chip-on-sensor concept, including a very light-weight mechanical support structure made from carbon fiber reinforced Airex foam. Moreover, CO_2 cooling for the front-end chips will ensure high efficiency at minimum material budget.

Keywords: Belle II, SVD, APV25, Silicon Detector, DSSD, Chip-on-Sensor, Origami, CO2 cooling
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1. Introduction

The second version of the Silicon Vertex Detector (SVD) of the Belle experiment [1] at KEK (Tsukuba, Japan) was in operation from 2003 until 2010, when the KEKB factory was shut down. Now, the machine undergoes a major upgrade until 2014 in order to eventually deliver a luminosity of $8 \times 10^{35}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, 40 times higher than previously achieved. It is obvious that such an increased intensity also requires massive changes in the Belle experiment and its innermost system, the SVD, in particular, leading to the largely renewed Belle II experiment [2, 3].

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As the old SVD already operated close to its limits in terms of occupancy and readout speed, a completely new readout scheme must be implemented, which also implies a redesign of the detector front-end. In order to improve the robustness of vertexing, the future Silicon Vertex Detector will be shifted towards higher radii and complemented by a two-layer PiXel Detector (PXD) built in DEPFET technology [4].

The Belle II pixel detector apparently features a very fine spatial granularity, but it has a long integration time. On the other hand, the future Silicon Vertex Detector will deliver very precise timing, but also present spatial ambiguities due to ghost hits. Obviously, the full power of the two silicon detector subsystems unfolds with the proper combination of their data, leading to high accuracy in both space and time domains.

2. Detector Layout

The future Silicon Vertex Detector will have four layers of double-sided silicon sensors which are all made from 6” wafers. Compared to the predecessor, the radii will be shifted outside to $r = 38/80/115/140$ mm in order to make room for the pixel detector located at $r = 14/22$ mm.

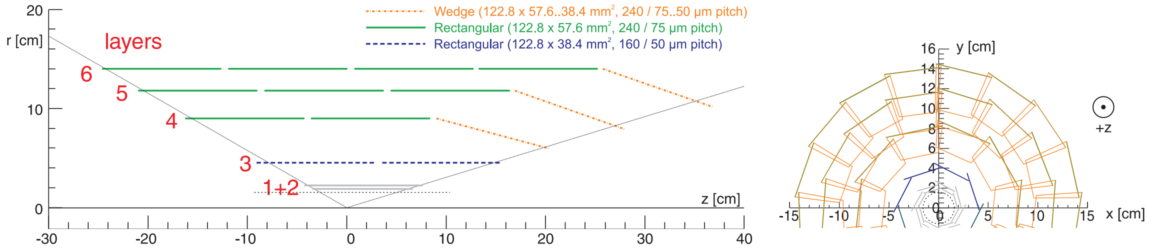

Fig. 1. Layout of the Belle II Silicon Vertex Detector (SVD) including the two innermost pixel layers (gray). The dimensions given refer to the active areas of the sensors.

Fig. 1 shows the arrangement of silicon sensors in Belle II, which have a polar angle coverage of $17° \ldots 150°$. This asymmetry reflects the forward boost arising from the different energies of the colliding electron and positron beams. In order to improve the performance of the SVD sensors in the very forward region, a slant angle was introduced for the outer three layers, which not only results in better spatial resolution but also implies less sensors and readout channels compared to the all-straight option. Obviously, these benefits come at the cost of a more complicated mechanical structure.

3. Double-Sided Silicon Sensors

As shown in fig. 1, only three different sensor types are required for the Belle II SVD, which all have the same length of 12.3 cm. The large rectangular sensor is 5.8 cm wide and thus fully uses up the available space on a 6” silicon wafer. In the innermost layer, a smaller sensor width of 3.8 cm was chosen in order to arrange the sensors in a circular fashion around the PXD. The width of the trapezoidal sensors in the slanted forward part varies between 5.8 and 3.8 cm.

Full-size prototype sensors for the large rectangular as well as the trapezoidal sensors were delivered by Hamamatsu Photonics (Japan) and Micron Semiconductor (UK), respectively, and both were tested successfully on the sensor level as well as with readout electronics in the laboratory and in a beam (see section 8 for results).

In case of the trapezoidal sensor, the full wafer was designed by ourselves, so we filled the areas around the large sensor with baby sensors and test structures. Different types of p-stop patterns were implemented on the n-sides of the baby sensors and compared in a beam test before and after irradiation with 700 kGy of ^{60}Co gammas. As reported in detail in [5], the atoll type p-stop with a certain geometry was found to be the best option, because its signal-to-noise was superior to all other designs both before and after irradiation.

4. Front-End Readout

In order to cope with the high particle rates expected in Belle II, the sensors need a short integration (shaping) time and fast readout. Moreover, in order to avoid dead time, a pipeline is mandatory to enable data taking and transfer in parallel. Finally, radiation tolerance up to 100 kGy is also desirable. The APV25 front-end chip [6], originally developed for the CMS experiment at the LHC, was chosen as it fulfills all those requirements. It has a shaping time of 50 ns, a pipeline depth of 192 cells and a nominal clock speed of 40 MHz. In Belle II, it will be operated at 31.8 MHz, which is 1/16 of the SuperKEKB RF.

The built-in "deconvolution" function [7], which is used in CMS to narrow down the hit pulse to a single bunch crossing, is not applicable to SuperKEKB because of its quasi-continuous collisions. Nonetheless, the APV25 can also read out several consecutive samples of the shaped waveform without applying the deconvolution, and thus the precise particle timing can be obtained by data processing in the back-end electronics (see section 8). Together with precise trigger timing, this helps to identify and discard off-time background and thus reduce the effective occupancy significantly.

Due to its fast shaping, the noise figure of the APV25 is inevitably higher than that of amplifiers with a long integration time. Consequently, the input capacitance of the amplifier must be minimized in order to maintain a good signal-to-noise ratio. This also means that the concatenation of several sensors (as it was done in the old SVD) or long fan-out connections are prohibitive – the chips must be placed as close as possible to the sensor strips, which leads to the "Origami" chip-on-sensor concept described in section 5.

One APV25 dissipates about 350 mW of power. As the Belle II SVD will contain 1902 chips in a confined space, active cooling is mandatory and will be described in section 6.

5. Ladder Design

The SuperKEKB is a B factory which mostly operates at a collision energy of 10.58 GeV, the $\Upsilon(4S)$ resonance, three orders of magnitude lower than the LHC. Consequently, multiple scattering is a serious concern which requires the lowest achievable mass especially for the vertexing detectors, i.e. PXD and SVD.

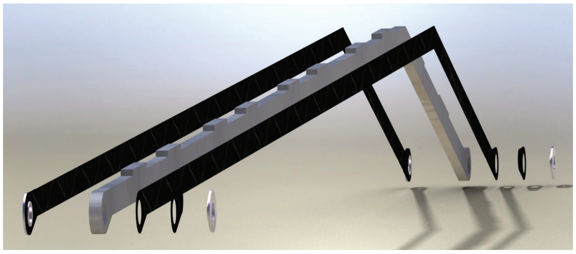

Fig. 2. Exploded view of a sandwich composite rib. Each Belle II SVD ladder is supported by two such ribs.

The sensor size is deliberately made as large as commercially available in order to reduce the overall amount of structural material. Depending on the layer, up to five sensors are arranged in a ladder, as shown in fig. 1. Each ladder is supported by two ribs made of a composite of a light-weight styrofoam (Airex [8]) with 65 μm thin plies of carbon fiber laminated onto the sides (fig. 2). The resulting structure is very light, but extremely stiff. Tiny pillars on the top side of the Airex core ensure that wire bonds on the bottom side of the sensor are not damaged and the conductive carbon fiber does not touch the sensors.

A thin (1 mm) layer of Airex is glued on top of the sensors in order to provide a thermal and electrical barrier. Then, a three-layer flex printed circuit (hybrid), which carries the APV25 chips, is placed onto the Airex sheet. The hybrid also includes a fan-out that allows to connect the chips to the strips on the top side of the sensor. Moreover, two additional flex pitch adapters are bent around the edge of the sensor in order to establish a contact to the bottom side strips – hence the name "Origami" [9].

An Origami ladder is shown in fig. 3. The big advantage of this concept is that all APV25 chips can be placed on the same flex hybrid and thus no duplicate infrastructure is needed despite of double-sided

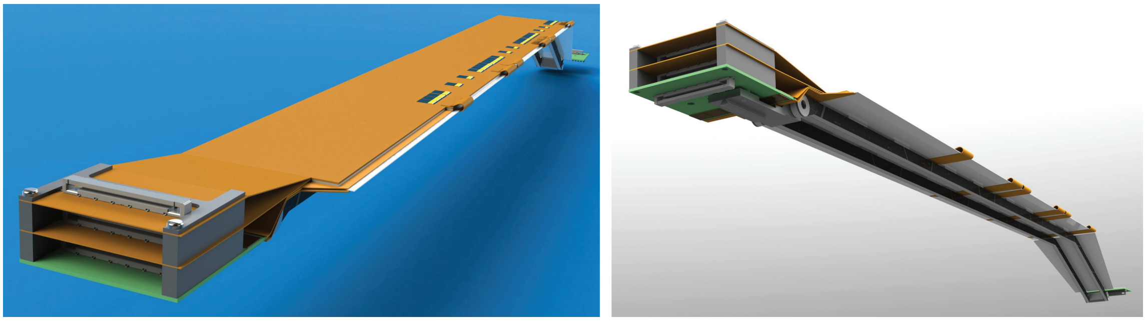

Fig. 3. Top and bottom sides of a fully assembled ladder (except for the cooling pipe).

readout. Moreover, the chips are thinned to 100 μm in order to reduce dead material. The Origami chip-on-sensor concept is only adopted for the inner sensors of a ladder. The first and last detectors, however, are read out with conventional PCB hybrids (shown in green) from the sides using proper flex pitch adapters to connect the strips. For the inner detectors, however, such pitch adapters would be much longer and thus result in prohibitive capacitance.

As the Origami chips are all aligned on the top side of the ladder, a single, thin cooling pipe is sufficient to remove the dissipated power, using CO_2 as a highly efficient coolant (see section 6). Despite the operational pressure of approximately 20 bar, tiny stainless steel tubes with an inner diameter of 1.4 mm and a wall thickness of just 50 μm easily withstand those conditions and ensure good heat transfer. The overall averaged material budget for a single ladder is calculated to be 0.55% X_0 including ribs, sensors, electronics and cooling. Static FEA simulation shows that the gravitational sag of the fully equipped longest (=outermost) ladder is less than 50 μm when the ladder is tilted to the side and around 100 μm when gravity acts from top.

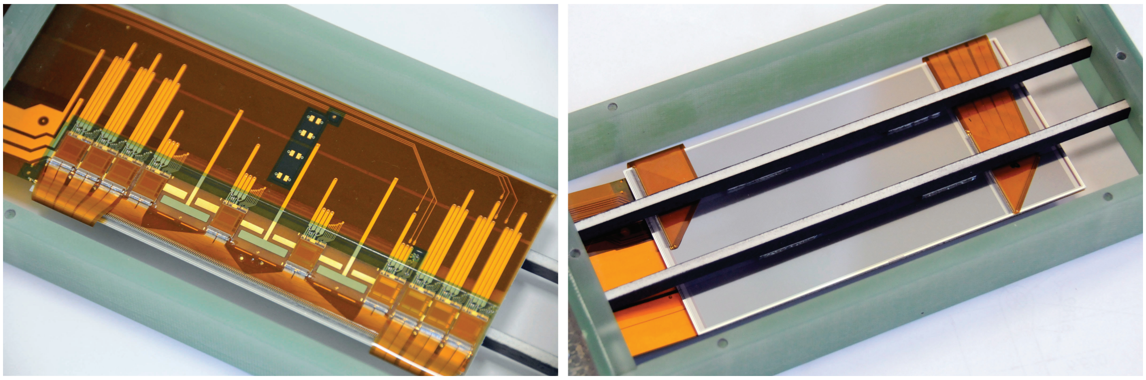

Fig. 4. Top and bottom sides of a prototype Origami module (before mounting the cooling pipe).

Two full-size prototype modules (fig. 4) using a single silicon sensor were assembled and successfully tested in the lab and in a beam. Further modules with a slightly revised flex hybrid are being assembled now and after that, the assembly process will be extended to a full ladder.

6. CO_2 Cooling

Both SVD and PXD of the Belle II experiment will be cooled with CO_2, an emerging technology in high energy physics which has several advantages compared to conventional systems. Thanks to the evaporation enthalpy of 282 kJ/kg at −20° C, two-phase (evaporative) CO_2 cooling is highly efficient and allows to use very thin pipes that maintain an almost constant temperature over the full length in case of a distributed heat load. Moreover, the coolant is cheap, nontoxic and gaseous at room temperature, thus potential leakage is not a serious concern. The main challenge of a CO_2 cooling system is its relatively high operating pressure, which scales with the coolant temperature. In case of the Belle II SVD, a rather low operating temperature is actually desirable from the viewpoint of thermal noise reduction. At approximately $-20°$ C, the operating pressure in the cooling system is in the order of 20 bar. It is obvious that such an operating temperature requires a dry environment in order to avoid condensation and ice.

Belle II will make use of closed-loop cooling systems, which are presently being designed. In parallel, we have developed an open (blow) system for lab tests which will soon be used to cool Origami modules in a beam test. This setup is a table-top box (fig. 5) connected to a CO_2 gas bottle and the device under test.

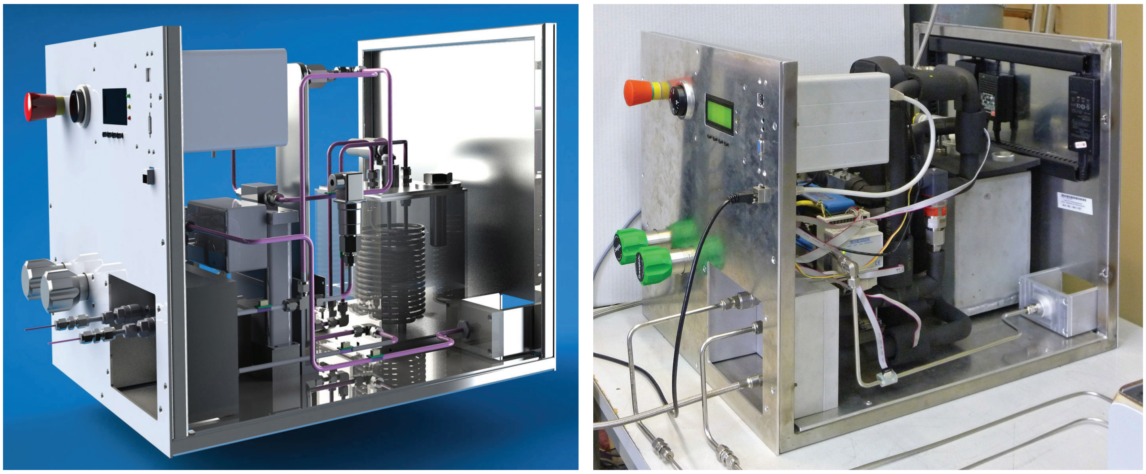

Fig. 5. Drawing and photograph of the CO_2 blow system used for evaporative cooling tests.

7. Readout System

The active front-end electronics of the Belle II SVD merely consists of the APV25 chips, which are connected by cables to junction boxes approximately 2 m away. These units are located in a moderately radiative area and thus contain only passive components as well as radiation-hard voltage regulators to supply the front-end chips. Control and data lines are fed through to the VME system in a distance of roughly 10 m. Tests with up to 14 m cables confirmed the driving capabilities of the APV25.

The core components of the back-end are 9U VME boards called "FADC+PROC" [2], which perform digitization of the incoming data as well as real-time data processing in FPGAs. The data treatment involves several steps performed in a pipeline style: first of all, a FIR filter compensates the frequency-dependent transfer function of the long cable, followed by the extraction of strip data, pedestal subtraction, a two-pass common mode correction and zero suppression. Finally, hit time finding will be applied using lookup tables.

Eventually, the processed data will be handed over to transmitter boards located in the rear of the crate, which send them to the common DAQ platform and to the pixel detector data reduction unit in parallel by optical fibers. The latter system will use the SVD information to perform online tracking in order to find regions of interest in the pixel detector and significantly reduce the amount of data in that system.

8. Beam Test Results

In October 2010, two Origami modules were tested in a 120 GeV hadron beam at CERN. At that time, the CO_2 cooling plant was not yet available, so liquid cooling with a commercial chiller was used, which required a thicker cooling pipe to ensure sufficient mass flow. In this configuration, $-10°$ C was the lowest temperature that could be achieved.

The Origami modules were fully functional and cluster signal-to-noise ratios of 14.4 and 22.9 were obtained for p- and n-sides, respectively, at cold temperature. The difference stems from the fact that the sensor is rectangular with strip lengths of 12.3 and 5.8 cm for p- and n-sides (see section 3) which also feature different strip pitches. Operation without cooling results in signal-to-noise values which are approximately 20% lower than those at cold temperature, which comes from thermal noise sources in the sensor and, more prominently, in the preamplifier of the APV25. Thus, we aim for a coolant temperature of −20° C for best performance in Belle II.

Hit time reconstruction was applied using offline numerical fitting for each event (see fig. 6, left side) and comparing the resulting peak time values to measurements of a reference TDC [10]. The difference (error) follows a normal distribution with RMS figures of approximately 4.4 and 2.3 ns for p- and n-sides. These values nicely fit into a scatter plot (fig. 6, rigth side) collected from several beam tests using sensors of various sizes and thus covering a wide range of signal-to-noise ratios. A clear double-logarithmic correlation between signal-to-noise and timing precision can be seen.

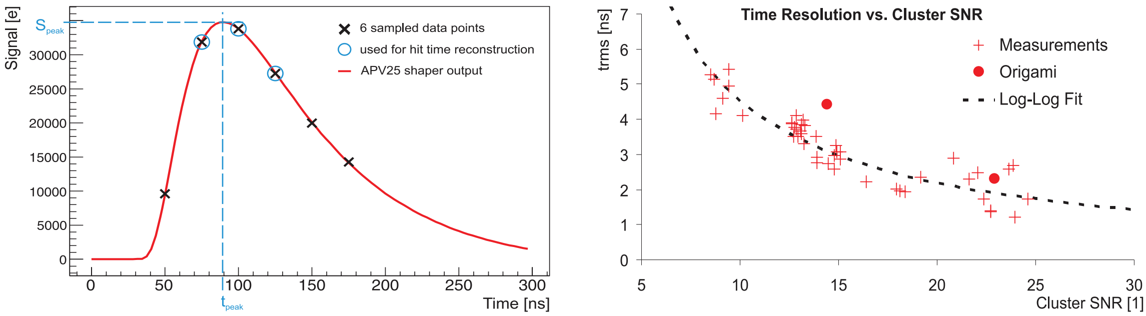

Fig. 6. Left: Measured event with fitted waveform obtained from an averaged calibration pulse scan. Right: Measured time resolution (RMS) vs. cluster signal-to-noise ratio. The values obtained with the Origami modules are represented by red dots.

9. Summary

Vertexing in the Belle II experiment will be performed with a two-layer PiXel Detector (PXD) close to the interaction point, surrounded by four strip detector layers in the Silicon Vertex Detector (SVD). The two subsystems complement each other in the sense that high precision in both space and time can be achieved by proper combination of their data.

The SVD is composed of 187 sensors featuring three different designs, two of rectangular and one of trapezoidal shape. All sensors are double-sided and made as large as possible from 6” wafers. Several sensors are combined in ladders, which utilize the Origami chip-on-sensor concept for the central sensors in order to achieve good signal-to-noise ratio with a total material budget of only 0.55% X_0, including structure, sensors, electronics and CO_2 cooling.

APV25 front-end chips will deliver multiple consecutive samples of the shaper output for each event. Those data points will be used in the back-end VME system to determine the exact hit timing, such that off-time background hits can be discarded. Cluster signal-to-noise ratios of 14.4 (p-side) and 22.9 (n-side) were achieved in a beam test with a full-size Origami module together with a corresponding timing precision of 4.4 and 2.3 ns, respectively.

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