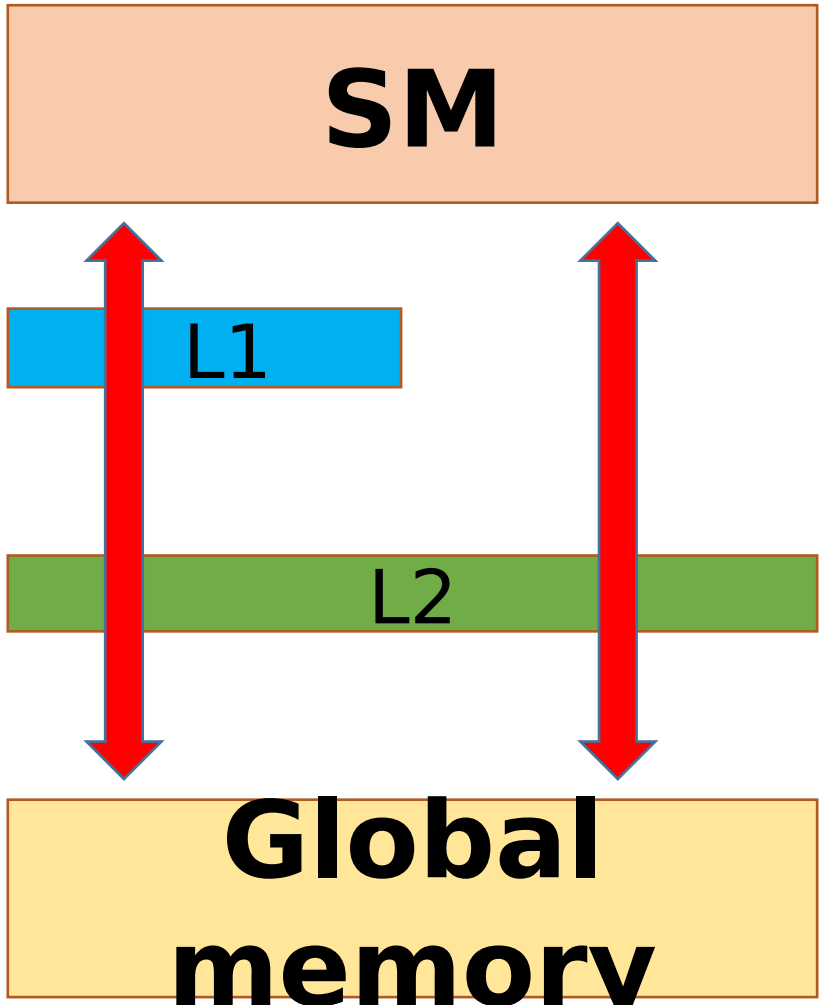
Memory access patterns

128 Btyes tansactio ns



32 Btyes tansactio ns

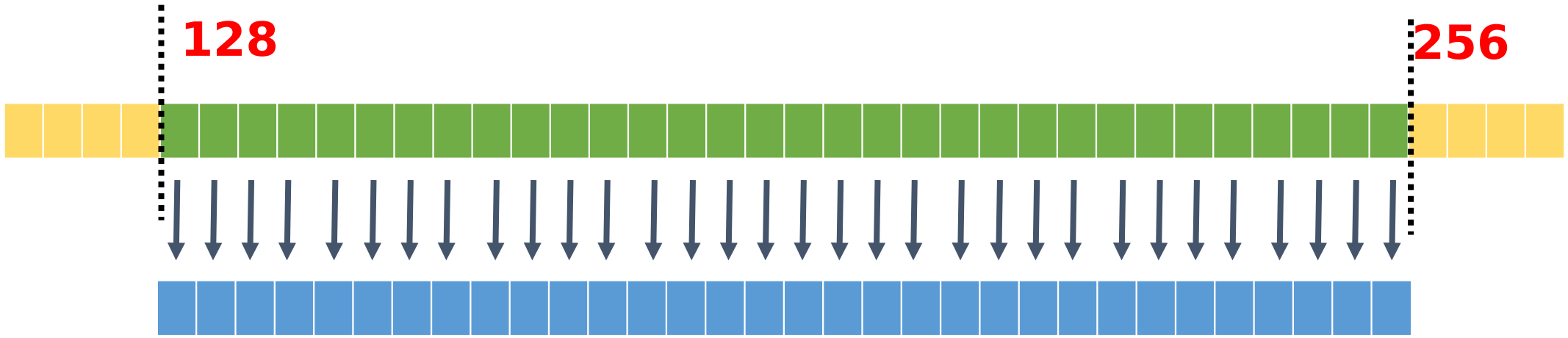
Characteristics of memory access

- **Aligned memory accesses**

First address is an even multiple of the cache granularity

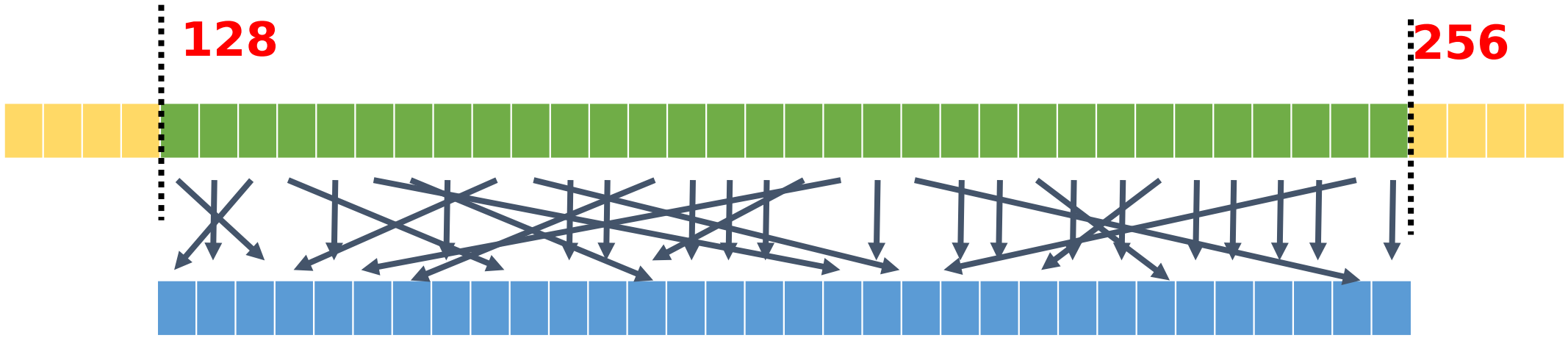
- **Coalesced memory accesses**

32 threads in a warp access a continuous chunk of memory



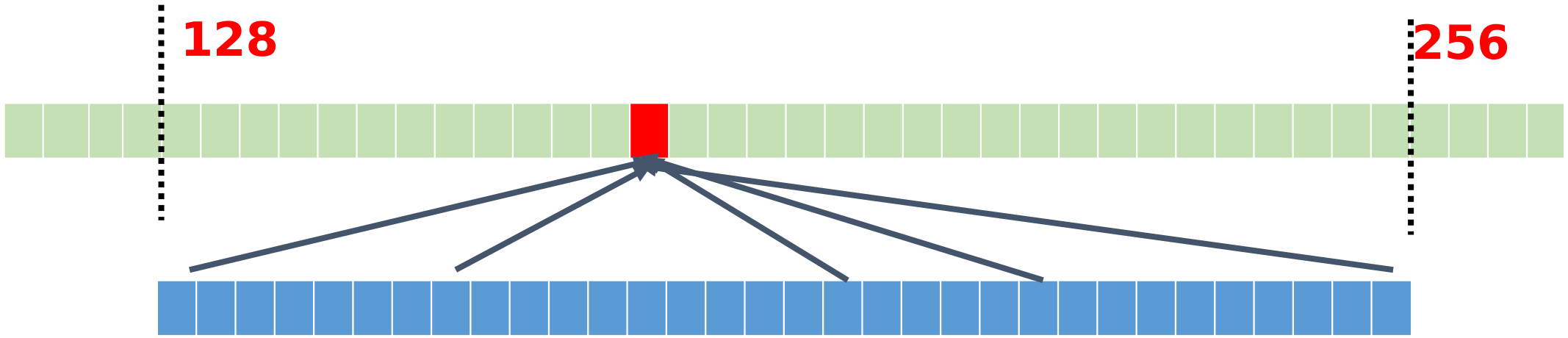
ThreadId 0 **3**

x **1**



ThreadId 0 **3**

x **1**

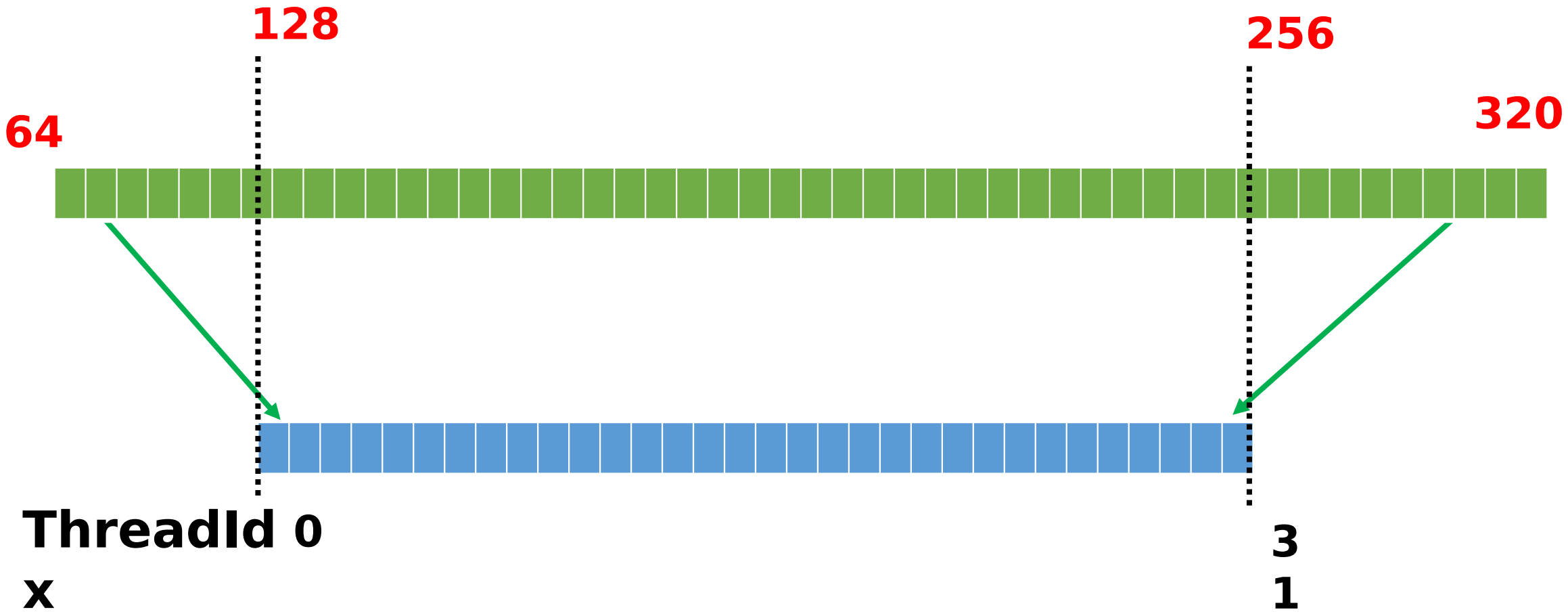


ThreadId 0

3

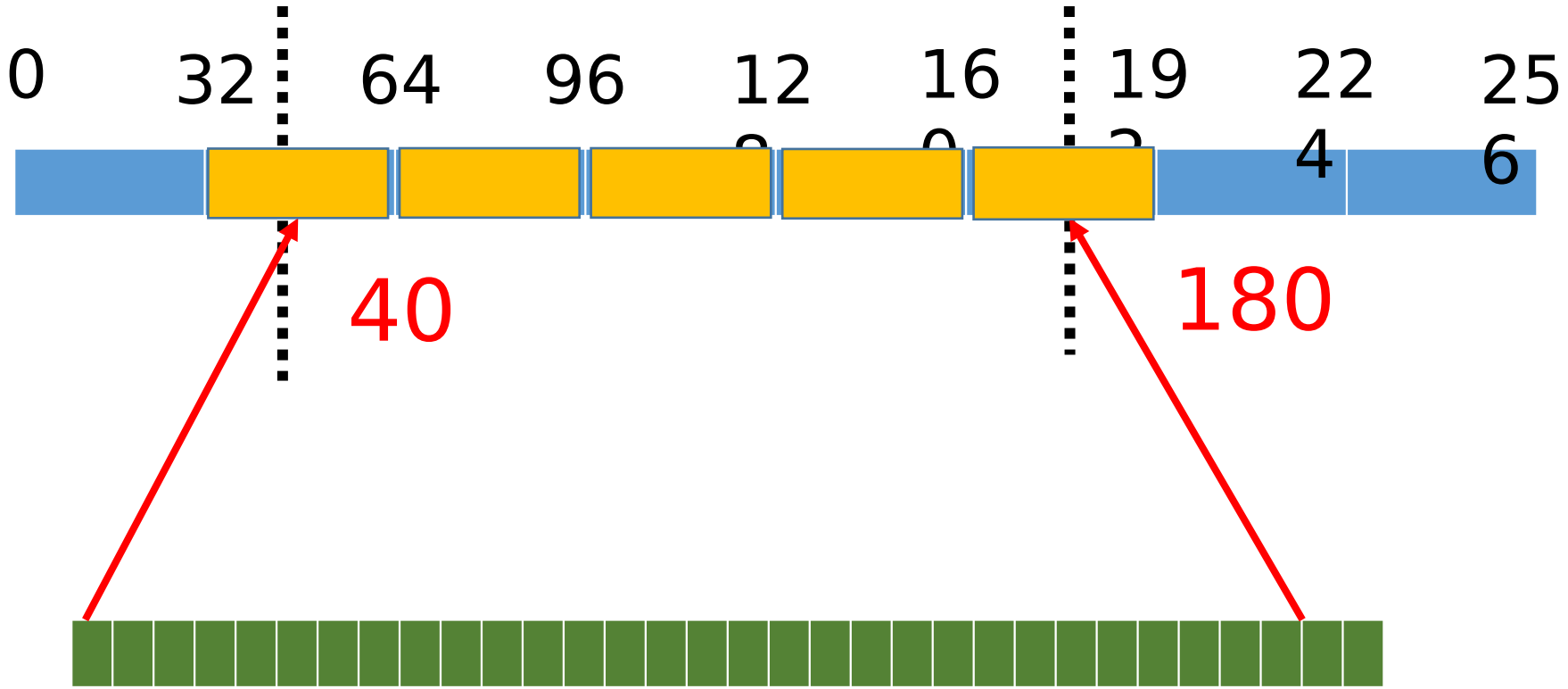
x

1

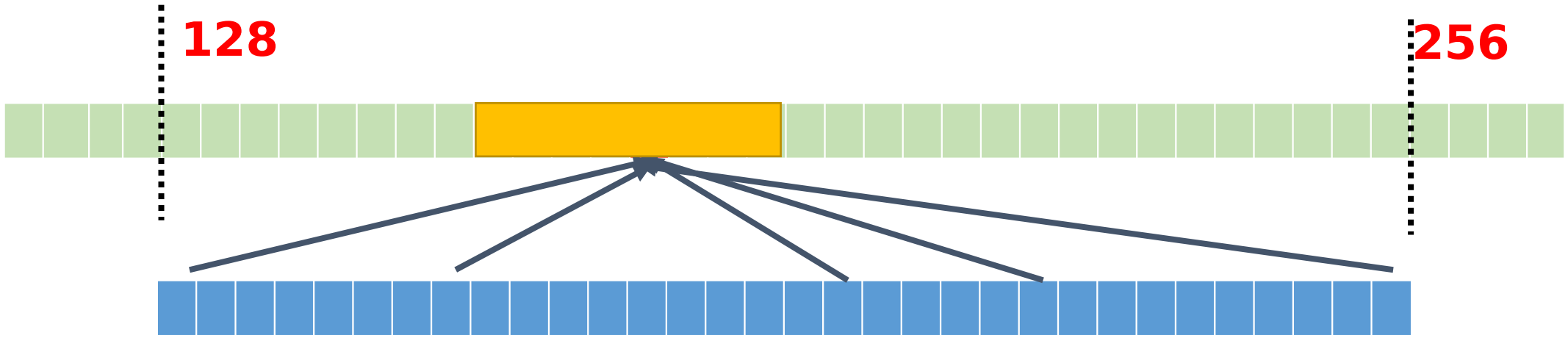

128
256
64
320
ThreadId 0
x
3
1

Un cached memory reads

- Memory loads does not utilized L1 cache refer as un cache loads
- Uncashed memory servings are more fi ne-grained, and can lead to better bus utilization for misaligned or un-coalesced memory accesses



(128 /160) * 100% = 80%



ThreadId 0 **3**

x **1**