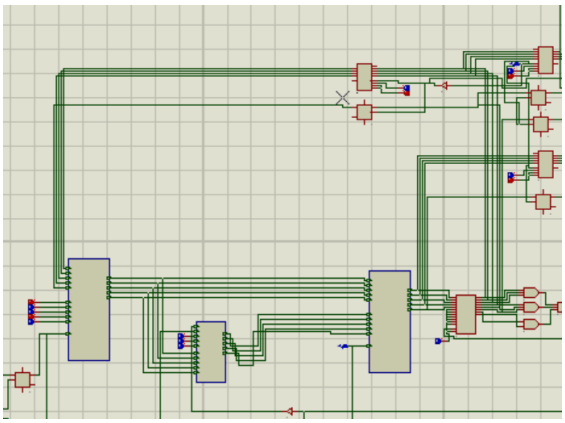
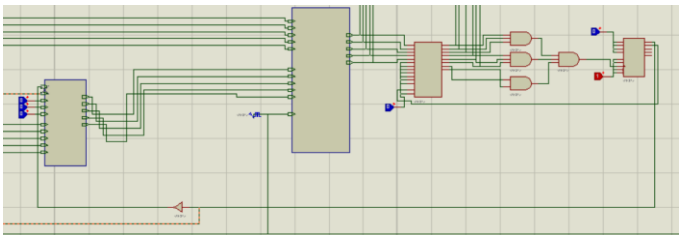
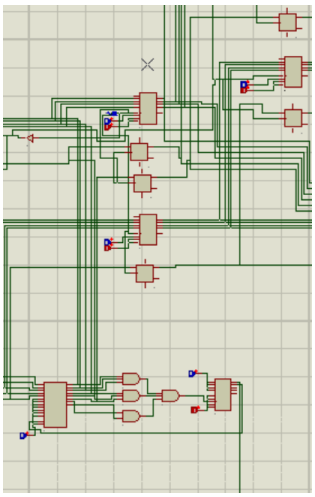
Approach: I first gave input to rom then the output from rom gets stored in a register in one half cycle then in next cycle , rom receives the input as previous input +1.



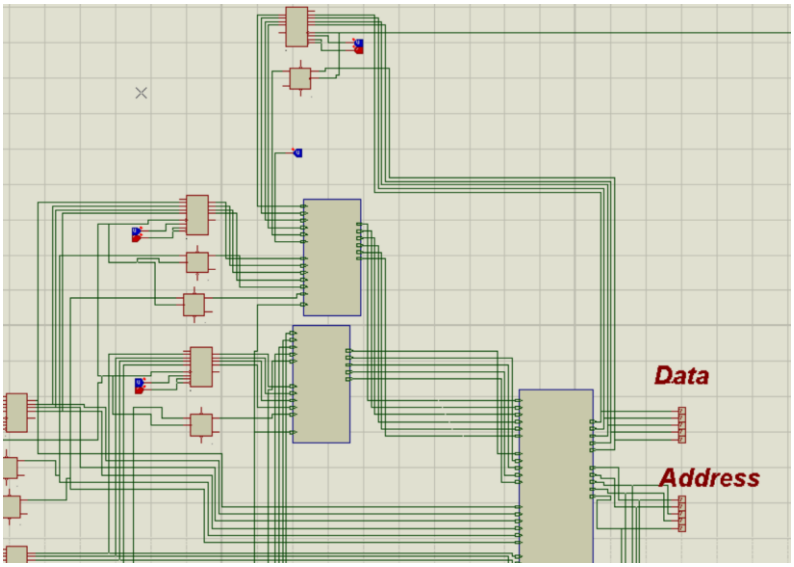
After travelling in forward direction, once we get 255, the number in adder is changed from 1 to 2 and we traverse in backward direction in list.



The data and address is strored in registers.



After storing in the register, Comparator is used to determine the minimum address and corresponding to that data , address is also given as output. If data is same, minimum address is given as output.



Components		Quantity	
ROM		1	75
74179		7	14
74161		1	2
7474		10	10
Comparator		4	8
clock		2	80
Logic Gates(2 i/p)			
	subadder	18	
	selector1	16	
	selector2	16	
	And8_4	1	
	not	4	
	MIN	47	
	Selectline	35	
		118	11.8
Logic Gates(3 i/p)			
	MIN	5	
	AND8	3	
		8	1.6
		COST	**202.4**