EXPERIMENT 4

PART 1

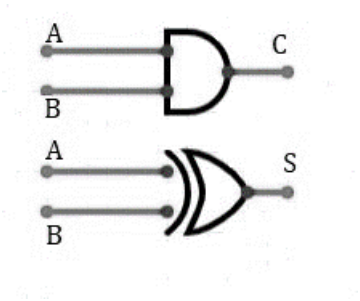
RIPPLE CARRY ADDER

AIM OF THE EXPERIMENT: To design a ripple carry adder using combinational circuit.

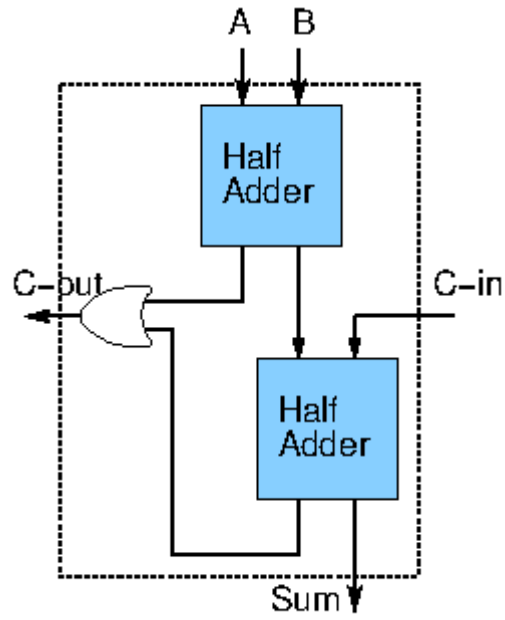
APPARATUS REQUIRED:

Sl.No.	APPARATUS	QUANTITY
1	74LS08	2
2	74LS32	1
3	74LS86	2

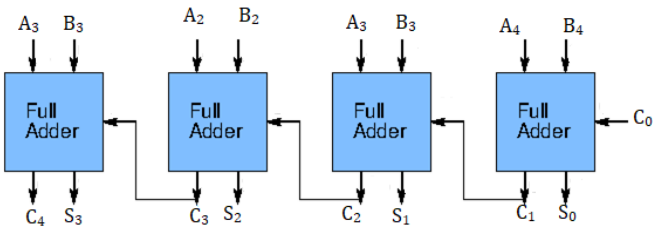
CIRCUIT DIAGRAM:



Half Adder Circuit



Full Adder using two Half Adders



4-bit Ripple carry Adder

THEORY

1 bit Full Adder circuit

1 bit Full Adder circuit can be built from two half adder circuits.

1 bit half adder:

It consists of two input bits to add (A & B) and give output the resultant sum and carry of addition of these two bits.

The logic of half adder is given below:

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Hence S= A⊕B and C=A & B

Full adder consists of two addend bits A and B, and an input carry bit C_{in}. It gives output as S, the sum and C_{out} as the output carry.

The logic of Full Adder is given below:

A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1

Hence,

$S=A \oplus B \oplus C_{in}$

$C_{out}=A.B+(A \oplus B)C_{in}$

4 bit Ripple Carry Adder:

A 4-bit ripple carry adder consists of 4 bit inputs A and B, an input carry C_{in} . Its output are a 4 bit sum S and an output carry C_{out}. It works on the principle of ripple carry, i.e. the carry from previous bit addition is fed into the current full adder to compute its sum and output carry. Thus, to get the C_{out} one needs to wait for all the carries to be computed chronologically. Hence, ripple carry adders are generally slow.

Computation of delay

To compute the delay between the feeding input to the 4 bit ripple carry adder and getting the output carry, we give the following inputs

A=1111

B=0000

First we set C_{in}=0, and record both the input and output waves (C_{in} & C_{out}) . Then we change C_{in} to 1.

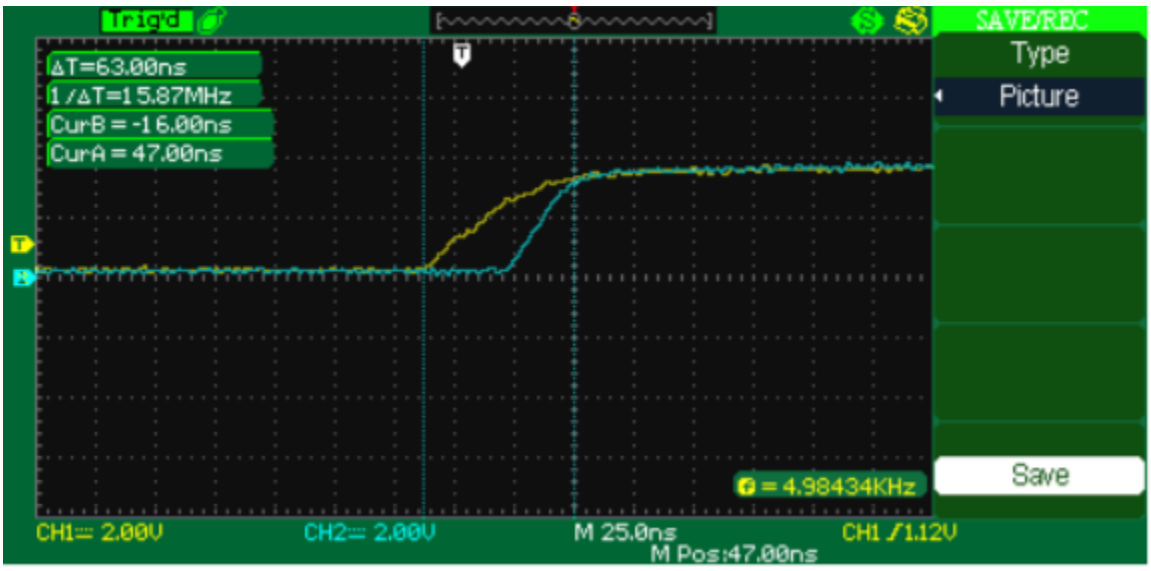
So initially C_{out}=0

Then C_{out}=1

We measure the difference between the times when C_{in} and C_{out} become 1.

RESULTS

The 4-bit ripple carry adder circuit was implemented and tested to be working correctly. The delay was measured to be approximately 100ns.



DISCUSSION:

- The ripple carry adder is slow as it introduces delay between input and output carry.
- The circuit for ripple carry adder is comparatively simpler hence less cost in terms of circuit.
- The logic for C_{out} for 1 bit full adder can be replaced by $C_{out} = A.B + (A+B)C$ where the xor is replaced by an or.
- The delay time can be reduced by using a carry lookahead adder.