Q1 Accumulator

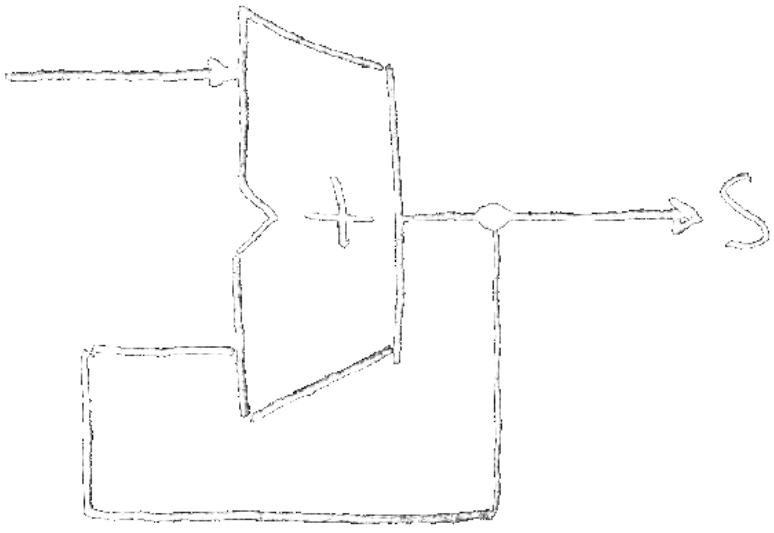
4 Points

You can find the lecture slides for todays lecture here!

You can access the YouTube playlist here!

Q1.1 Which of the following are true?

4 Points



One reason our naïve attempt at an accumulator (shown above) didn't work because we had no way to initialize S to 0

- [x] True
- [ ] False

One reason our naïve attempt at an accumulator (shown above) didn't work because we had no way to control the next iteration of the for loop

- [x] True
- [ ] False

One reason our naïve attempt at an accumulator (shown above) didn't work because we had no way to send different values of X_i in

- [ ] True
- [x] False

We fixed our naïve attempt at an accumulator by using a register to hold the current value of S

- [x] True
- [ ] False

Q2 Register Details Flip-flops

4 Points

Q2.1 Which of the following are true?

4 Points

A n-bit-wide flip-flop is made up of n 1-bit-wide registers

- ○ True
- ◉ False

They call them flip-flops because they were invented in San Diego

- ○ True
- ◉ False

We'll mostly only consider rising edge flip-flops in this course

- ◉ True
- ○ False

The three values that are part of the spec of a flip-flop are the "clock-to-q" delay, the "stable" time, and the "unstable" time.

- ○ True
- ◉ False

Q3 Accumulator revisited

4 Points

Q3.1 Which of the following are true?
4 Points

S_{i-1} holds the results of the $i^{th} - 1$ iteration

- (•) True
- ( ) False

It's ok that S_i is temporarily wrong for a brief time

- (•) True
- ( ) False

It's ok that S_{i-1} is temporarily wrong for a brief time

- ( ) True
- (•) False

X_i can vary at any time within the window of a clock signal as long as its frequency is identical to the clock rate

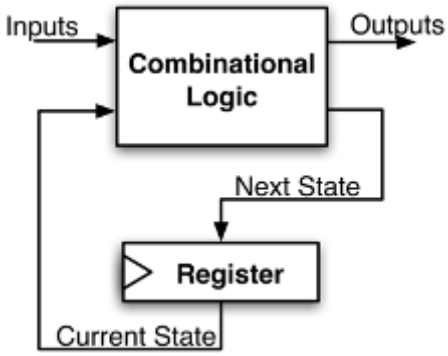
- ( ) True
- (•) False

Q4 Pipelining for Performance

4 Points

Q4.1 Which of the following are true?

4 Points



The Max delay of the circuit above is a function of $t_{clock-to-q}$

- (●) True
- ( ) False

The Max delay of the circuit above is a function of t_{setup}

- (●) True
- ( ) False

The Max delay of the circuit above is a function of t_{hold}

- ○ True
- ◉ False

We often pipeline circuits with a large t_{CL} delay to allow us to increase the clock frequency

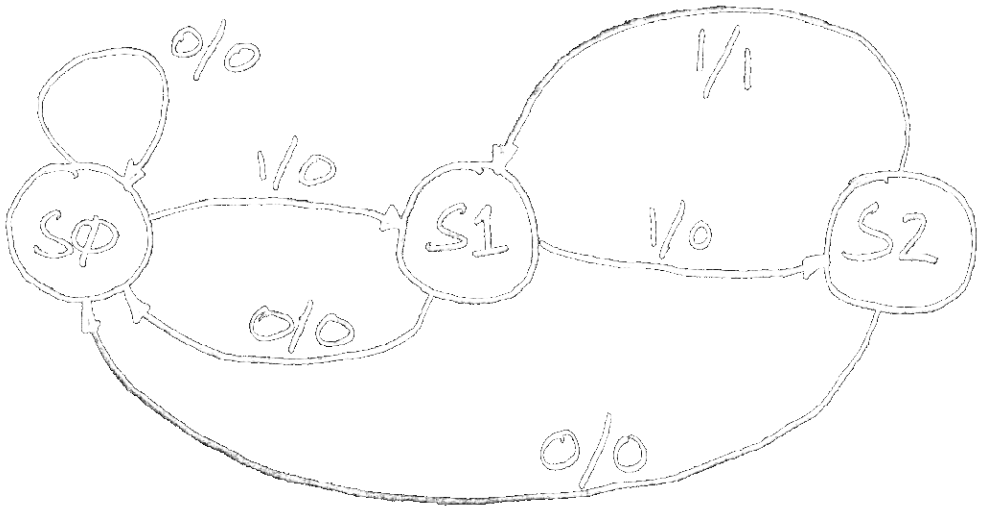
- ◉ True
- ○ False

Q5 Finite State Machines

4 Points

Q5.1 Assuming we start at S0, the circuit below detects

4 Points



- ○ The occurrence of 2 consecutive ones (and after that repeatedly 2 consecutive ones)
- ○ The occurrence of 2 consecutive ones (and after that repeatedly 3 consecutive ones)
- ◉ The occurrence of 3 consecutive ones (and after that repeatedly 2 consecutive ones)
- ○ The occurrence of 3 consecutive ones (and after that repeatedly 3 consecutive ones)

Lecture 15 - State, State Machines

● GRADED

STUDENT
Somya Mohindra

TOTAL POINTS
20 / 20 pts

QUESTION 1

Accumulator **4** / 4 pts

1.1 Which of the following are true? **4** / 4 pts

QUESTION 2

Register Details Flip-flops **4** / 4 pts

2.1 Which of the following are true? **4** / 4 pts

QUESTION 3

Accumulator revisited **4** / 4 pts

3.1 Which of the following are true? **4** / 4 pts

QUESTION 4

Pipelining for Performance **4** / 4 pts

4.1 Which of the following are true? **4** / 4 pts

QUESTION 5

Finite State Machines **4** / 4 pts

5.1 Assuming we start at S0, the circuit below detects **4** / 4 pts