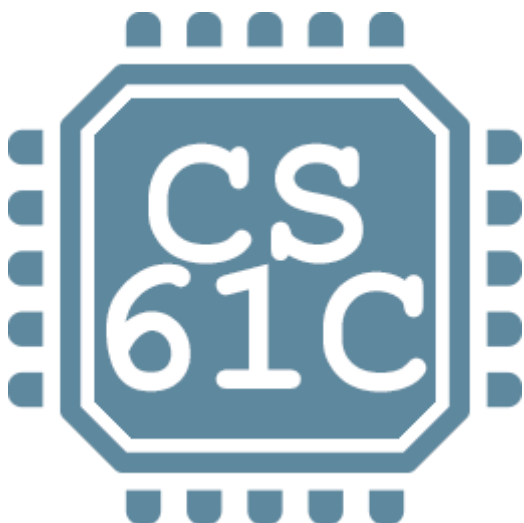


Q1 RISC-V Processor Design

4 Points

You can find the lecture slides for today's lecture [here!](#)

You can access the YouTube playlist [here!](#)



Q1.1 Which of the following are true?

4 Points

The CPU consists of a datapath and a controller which tells the datapath what to do.

☒ True

☐ False

The datapath will determine what to do based on the instruction.

☐ True

☒ False

The CPU consists of 6 separate datapaths, one for each instruction format.

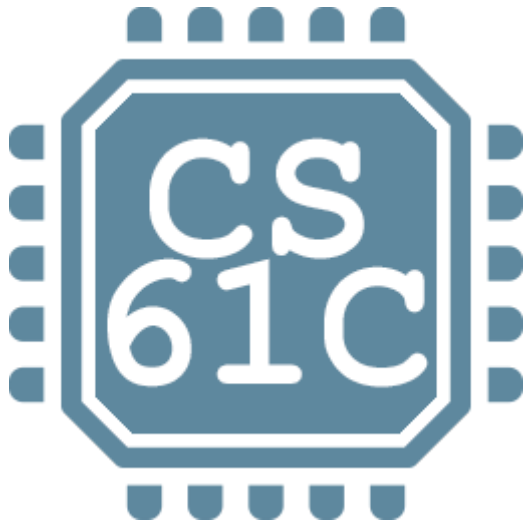
- ☐ True
- ☒ False

There is only one correct implementation of RISC-V ISA.

- ☐ True
- ☒ False

Q2 Building a RISC-V Processor

7 Points



Q2.1 Which of the following are true?

4 Points

When implementing an R-Type instruction, there are 6 steps to evaluating an instruction.

- ☐ True
- ☒ False

The circuit for the PC is just a wire incrementing the PC by 4 every time the clock ticks.

☒ True

☐ False

The PC exists in the Register File.

☐ True

☒ False

The RegFile has 5 inputs of varying width and 2 outputs of 32 bit width.

☐ True

☒ False

Q2.2 Which of the following are true?

3 Points

The RegFile contains 32 registers.

☐ True

☒ False

For R-type instructions, we do not need the Write Enable bit of the Regfile.

☒ True

☐ False

The ALU is the Addition Logical Unit. It is used to only perform addition in our processor.

☐ True

☒ False

Q3 R-Type Add Datapath

3 Points

**Q3.1** Which of the following are true?

3 Points

IMEM and DMEM are two physically separate DRAM chips.

- ☐ True
- ☒ False

Instruction decoding is performed in IMEM block

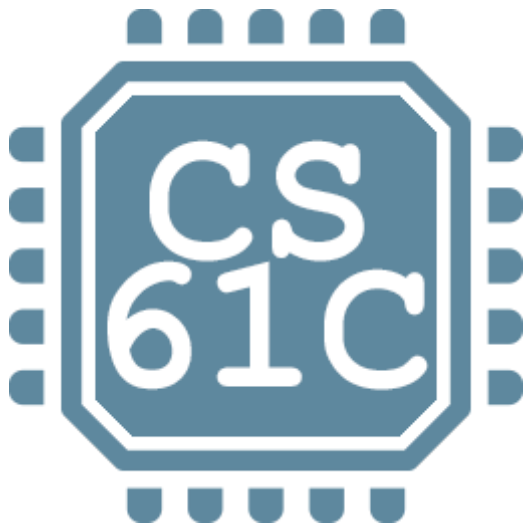
- ☐ True
- ☒ False

PC is updated at the same time as the value in the destination register rd, during add

- ☒ True
- ☐ False

Q4 Sub Datapath

1 Point

**Q4.1**

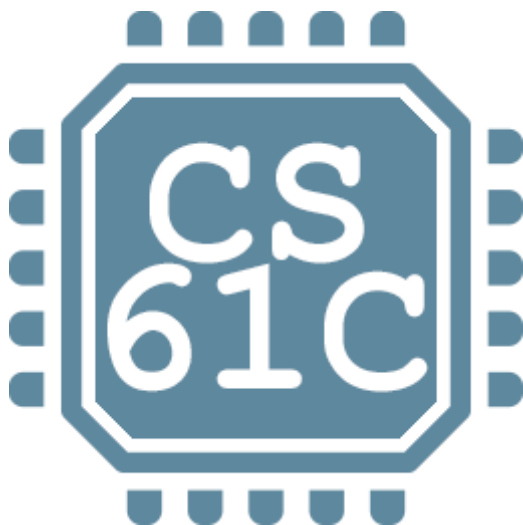
1 Point

I swear that I have watched this video and that if I have not and say that I have watched it, I will receive an F in the class.

- ☒ I have watched the video.
- ☐ I have not watched the video.

Q5 Datapath with Immediates

3 Points

**Q5.1**

3 Points

The Immediate Generator is an abstraction which will generate an immediate and perform whatever operation the instruction told it to do.

- ☐ True
- ☒ False

We will always sign extend the I-Type immediate.

- ☒ True
- ☐ False

To add an I-Type instruction, we had to change the ALU B input to the immediates' output.

- ☐ True
- ☒ False

Lecture 18 - Single-Cycle CPU Datapath I

● GRADED

STUDENT

Sauna Hannani

TOTAL POINTS

18 / 18 pts

QUESTION 1

RISC-V Processor Design

4 / 4 pts

1.1 Which of the following are true?

4 / 4 pts

QUESTION 2

Building a RISC-V Processor

7 / 7 pts

2.1 Which of the following are true? **4 / 4 pts**

2.2 Which of the following are true? **3 / 3 pts**

QUESTION 3

R-Type Add Datapath **3 / 3 pts**

3.1 Which of the following are true? **3 / 3 pts**

QUESTION 4

Sub Datapath **1 / 1 pt**

4.1 (no title) **1 / 1 pt**

QUESTION 5

Datapath with Immediates **3 / 3 pts**

5.1 (no title) **3 / 3 pts**