Computer Architecture
2. Central Processing Unit

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2. CPU – Main topics

- CPU general block diagram
- CPU instruction processing cycle
- Registers
- Control Unit – CU
- Arithmetic and Logic Unit – ALU
- CPU internal bus
- Some CPU block diagrams

CPU general block diagram

CU: Control Unit

IR: Instruction Register

PC: Program Counter

MAR: Memory Address Register

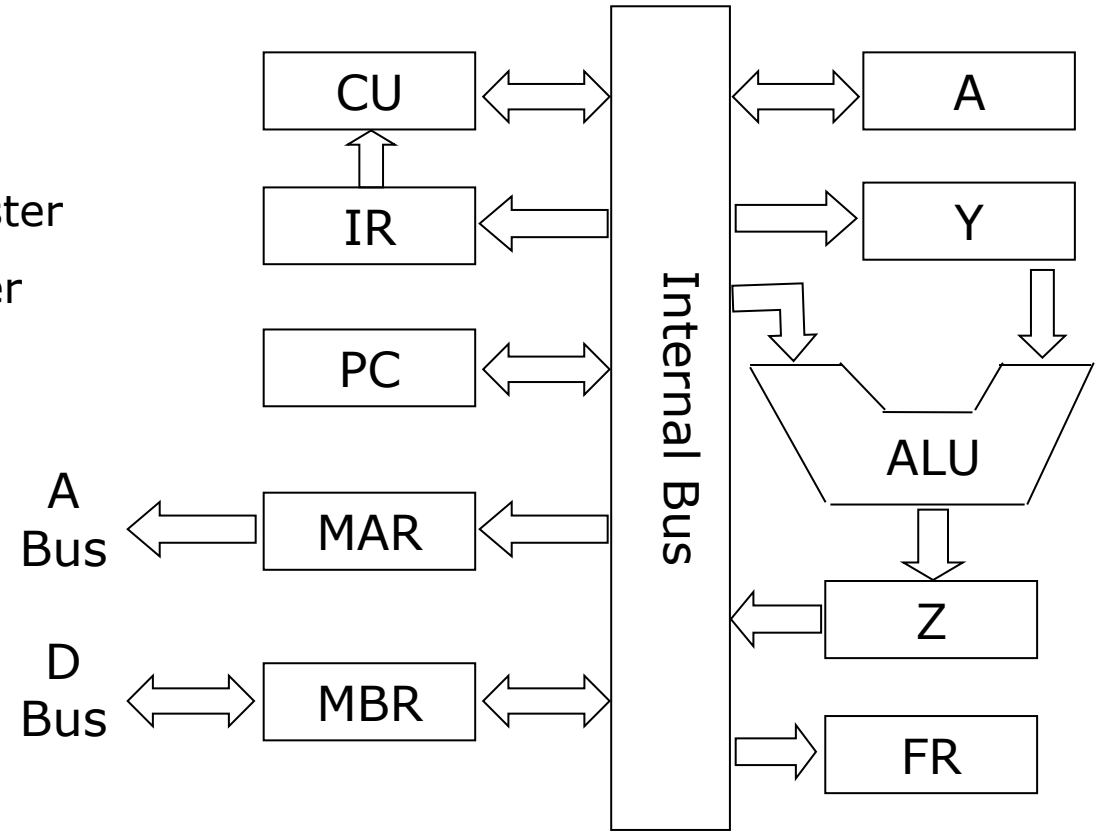
MBR: Memory Buffer Register

A: Accumulator Register

Y, Z: Temporary Register

FR: Flag Register

ALU: Arithmetic and Logic Unit



CPU instruction processing cycle

1. When a program is executed, the Operating System loads the program code into internal memory.
2. The address of the first instruction of the program is set onto PC register.
3. The address of memory cell that contains the instruction is transferred to A bus via MAR register.
4. In turn, A bus forwards the address to the Memory Management Unit (MMU).
5. MMU selects the memory cell and carries out the CPU READ signal.

CPU instruction processing cycle

6. Instruction from memory cell is transferred to MBR register via D bus.
7. MBR forwards the instruction to IR register. IR in turn forwards the instruction to CU.
8. CU decodes the instruction and generates execution signal for other units, such as ALU to execute the instruction.
9. Address in PC is increased to point to next instruction of the program.
10. Repeat Step 2 to 9 for all program's instructions.

CPU Registers

- Registers are temporary storage cells inside CPU:
  - Store instructions and data to be processed;
  - Small in number and size;
  - Very fast and run at CPU clock speed.
- Old CPUs (8086, 80x86) have 16-32 registers; modern CPUs (Intel Pentium 4, Core 2 Duo) have hundreds of registers.
- Register sizes depend on CPU design: 8, 16, 32, 64, 128 and 256 bits.

CPU Registers - Accumulator

- Accumulator or A register is one the most important CPU registers.
  - A is used to store the input operand
  - A is used to store the output result
- Size of A is equivalent to the CPU Data Word Length: 8, 16, 32, 64 bits.
- A is also used in data exchange with input and output devices.

CPU Registers - Accumulator

- Example: compute x + y → s
  - Load x operand into A
  - Load y operand into register Y
  - ALU carries out the addition A + Y and the result is stored in Z
  - Then the result is moved to A.

CPU Registers - PC

- PC – Program Counter or Instruction Pointer stores the memory address of next instruction.
- PC stores the memory address of the first instruction when a program is loaded into the memory.
- After CPU executes one instruction, the memory address of next instruction is loaded into PC.
- The size of PC depends on CPU design: 16, 32, 64 bits.

CPU Registers - FR

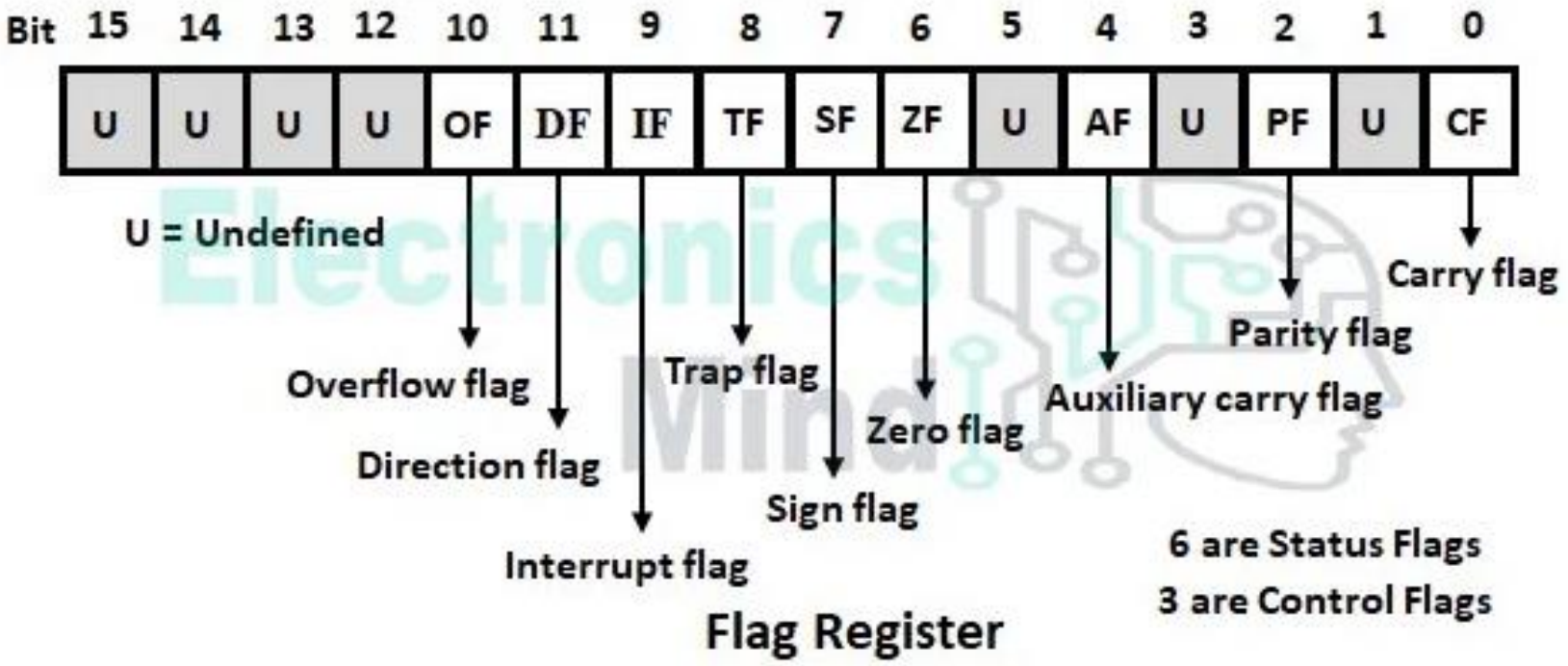
- FR – Flag or Status Register: Each FR bit stores the status of the result of the operation executed by ALU.
- There are two types of flags:
  - Status flags: CF, OF, AF, ZF, PF, SF
  - Control flags: IF, TF, DF
- Flag bits are usually used as the conditions in branching instructions to create program logics.
- FR size depends on CPU design.

CPU Registers - FR

Flag	ZF	SF	CF	AF	IF	OF	PF	1
Bit No	7	6	5	4	3	2	1	0

- ZF: Zero Flag, ZF=1 if the result=0 and ZF=0 if result<>0.
- SF: Sign Flag, SF=1 if result is negative and SF=0 if result is positive.
- CF: Carry Flag, CF=1 if there is carry/borrow of left most bit.
- AF: Auxiliary Flag, AF=1 if there is carry/borrow of left most bit of nibble.
- OF: Overflow Flag, OF=1 there is overflow, OF=0 if otherwise.
- PF: Parity Flag, PF=1 if total number of 1 bits in the result is odd and PF=0 if total number of 1 bits in the result is even.
- IF: Interrupt Flag, IF=1: Interrupt enabled, IF=0: Interrupt disabled

CPU Registers – FR flag position



CPU Registers – SP – Stack Pointer

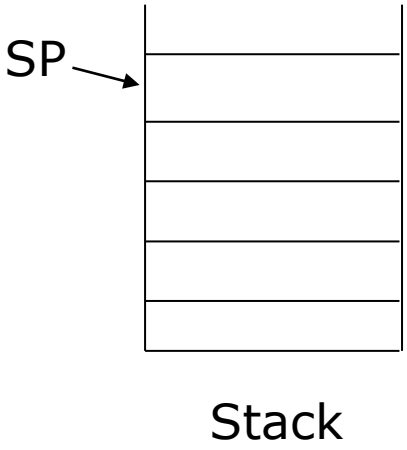
- Stack is a special memory segment which works on the Last In First Out (LIFO) principle.
- SP – Stack Point is the register that always points to the top of the stack.
- Two stack operations:
  - Push: put data into stack

    SP ← SP + 1

    {SP} ← Data
  - Pop: get data out of stack

    Register ← {SP}

    SP ← SP - 1



General Purpose Registers

- General Purpose Registers can be used for many purposes:
  - To store input operands
  - To store output results
- Example: CPU Intel 8086 has 4 general purpose registers:
  - AX: Accumulator
  - BX: Base Register
  - CX: Counter Register
  - DX: Data Register

CPU Registers - IR

- IR – Instruction register is used to store the current executed instruction.
- IR gets instruction from MBR and forwards it to CU for decoding.

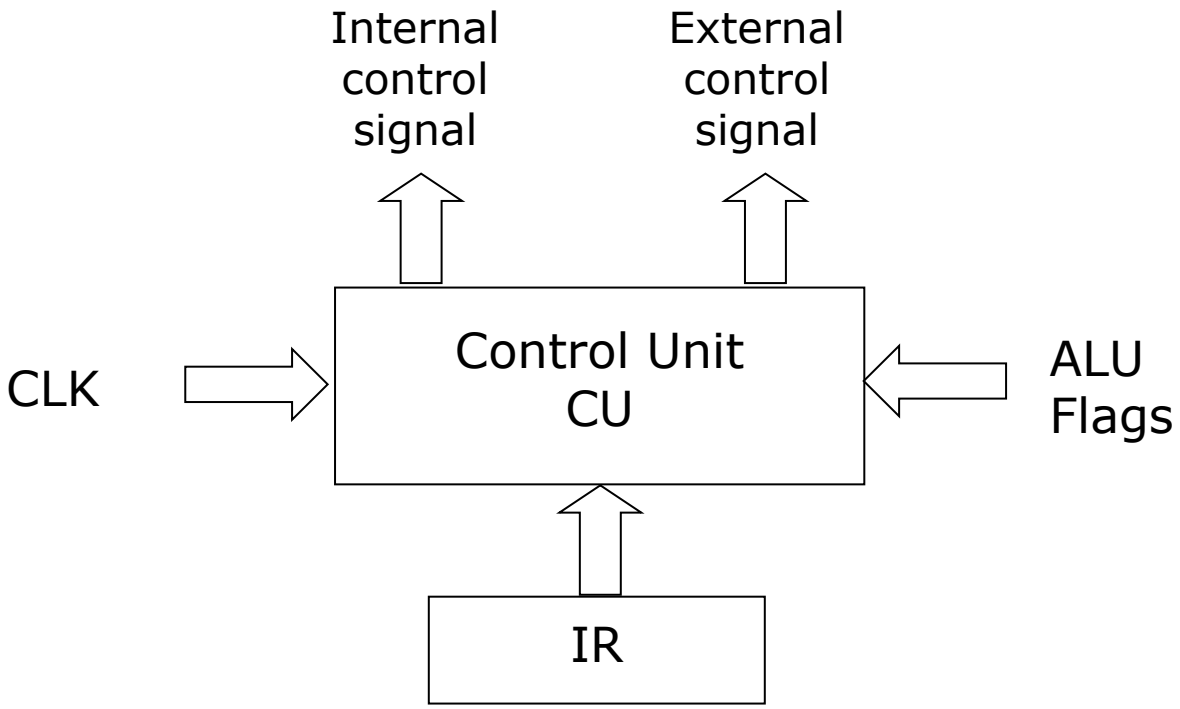
CPU Registers – MAR/MBR

- MAR – memory address register
  - is the interface between the CPU and the address bus.
  - gets memory address of next instruction from PC and forwards it to address bus.
- MBR - memory buffer register
  - is the interface between the CPU and the data bus.
  - gets instruction from data bus and forwards it to IR.

CPU Registers– Temporary Registers

- CPU usually use a number of temporary registers to:
  - To store input operands
  - To store output results
  - To support parallel processing (run more than one instruction at a time)
  - To support advanced execution engine, such as OOO – Out Of Order execution.

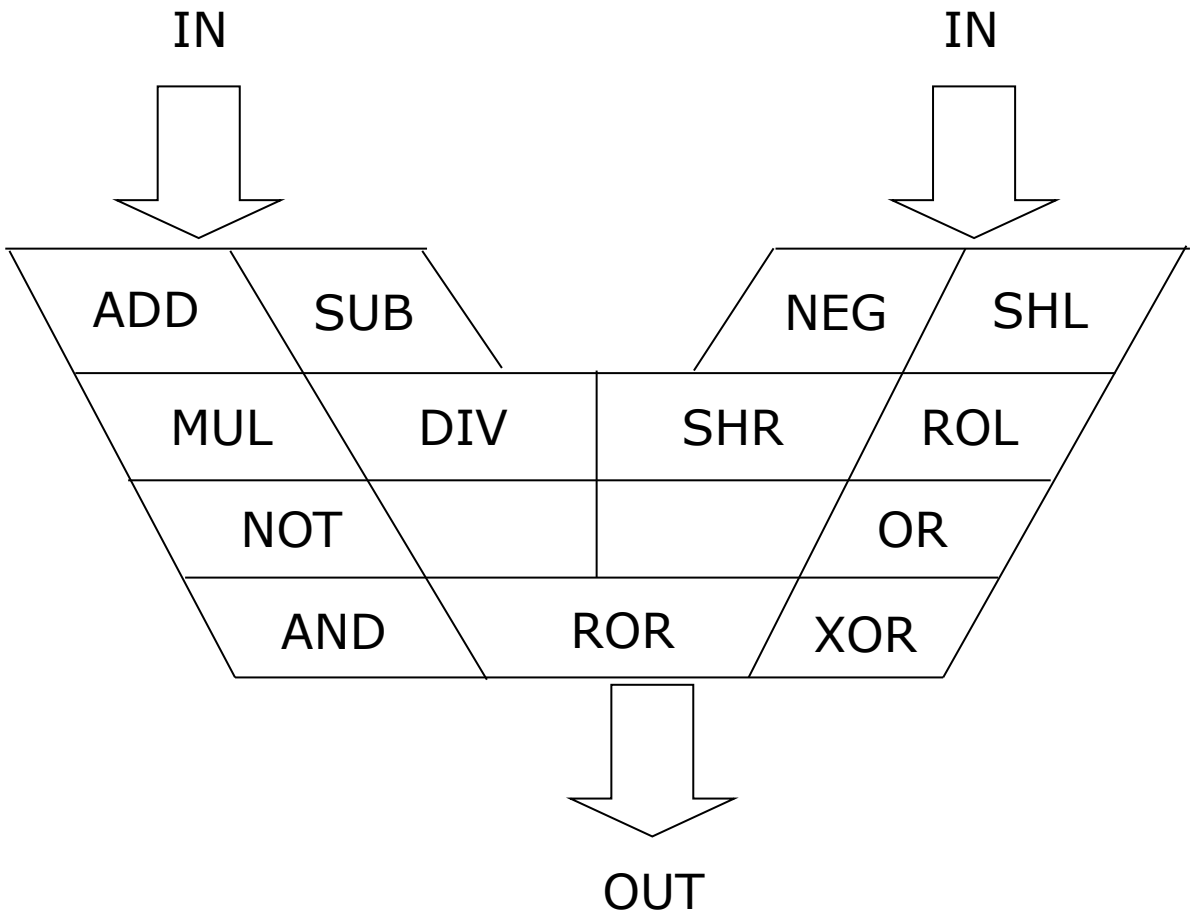
CU – Control Unit



CU – Control Unit

- Controls all CPU's activities based on system clock;
- Gets instruction from IP, decodes and generates control signals;
- Uses clock to synchronize activities of functional units inside CPU and between CPU and external components.

ALU – Arithmetic and Logic Unit



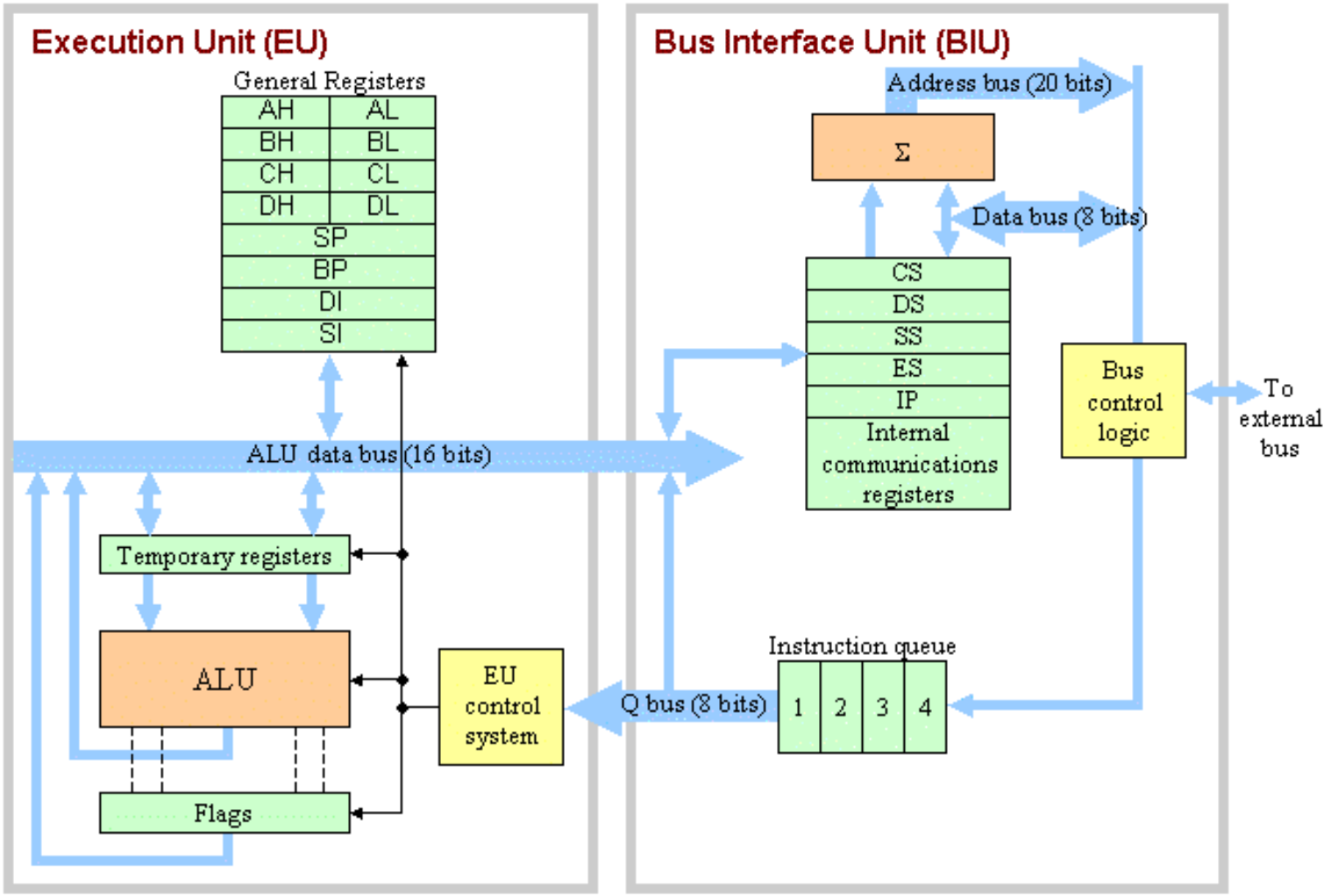
ALU – Arithmetic and Logic Unit

- ALU consists of multiple units for arithmetic and logic operations, such as add, subtract, multiply, divide, NOT, AND, OR.
- ALU has
  - two IN ports to get inputs from registers, and
  - one OUT port which is connected to internal bus to send result to registers.

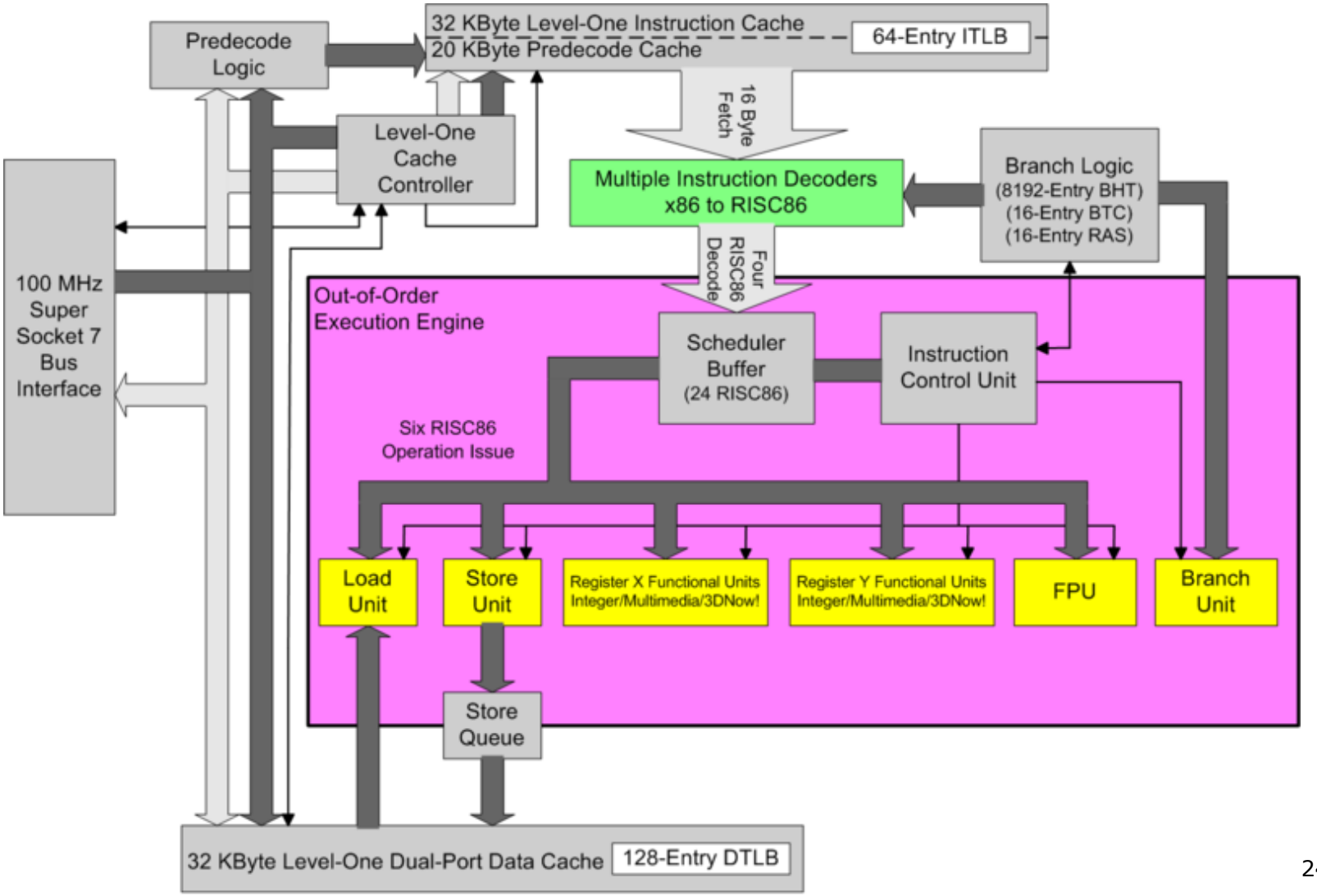
CPU- Internal Bus

- Internal Bus is the communication channel of all CPU components;
- Internal Bus supports full duplex (two ways) communication;
- Internal Bus has interfaces to exchange information with external buses (system buses).
- Internal Bus usually has large bandwidth and much faster than external buses.

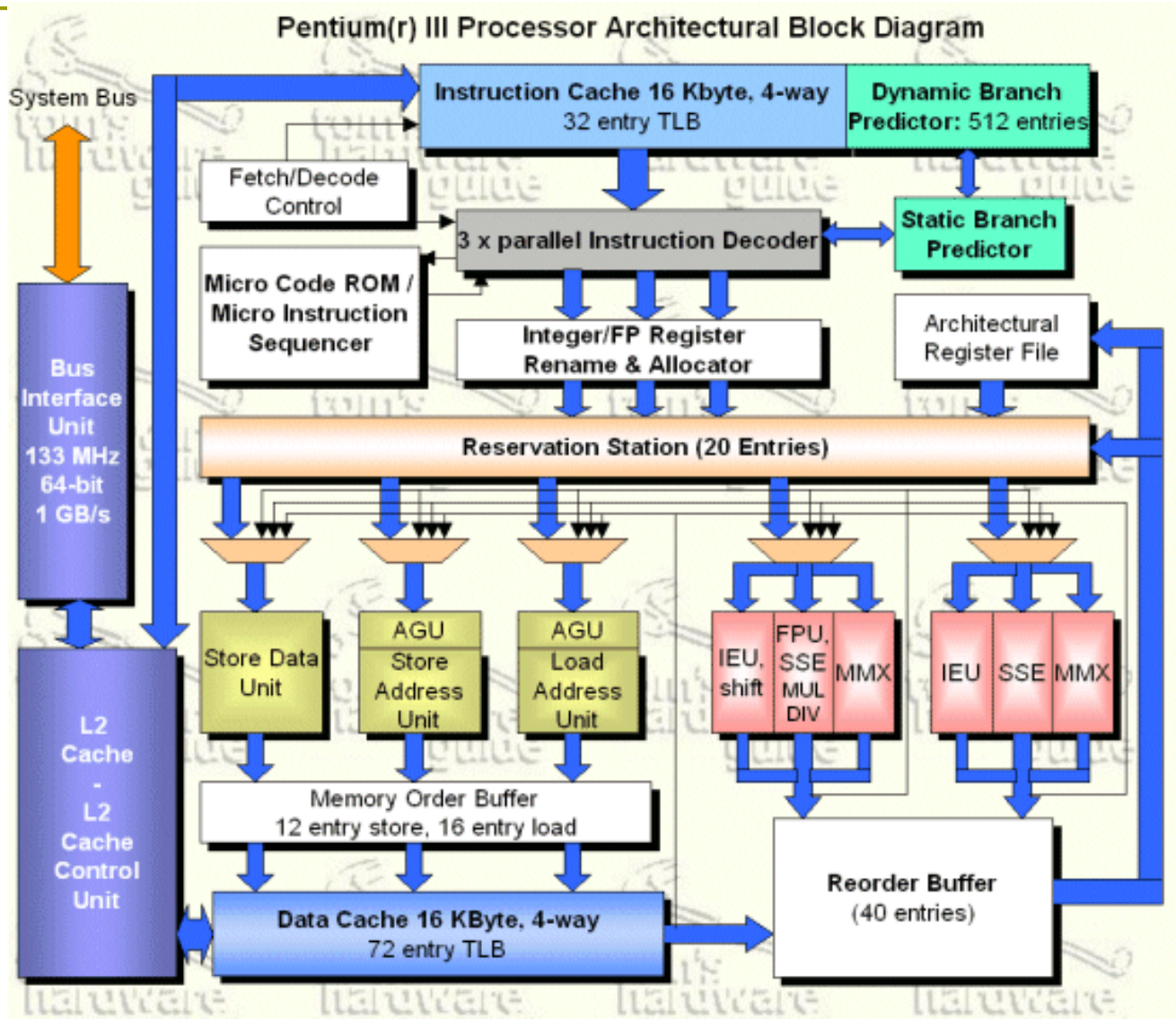
CPU block diagrams – Intel 8086



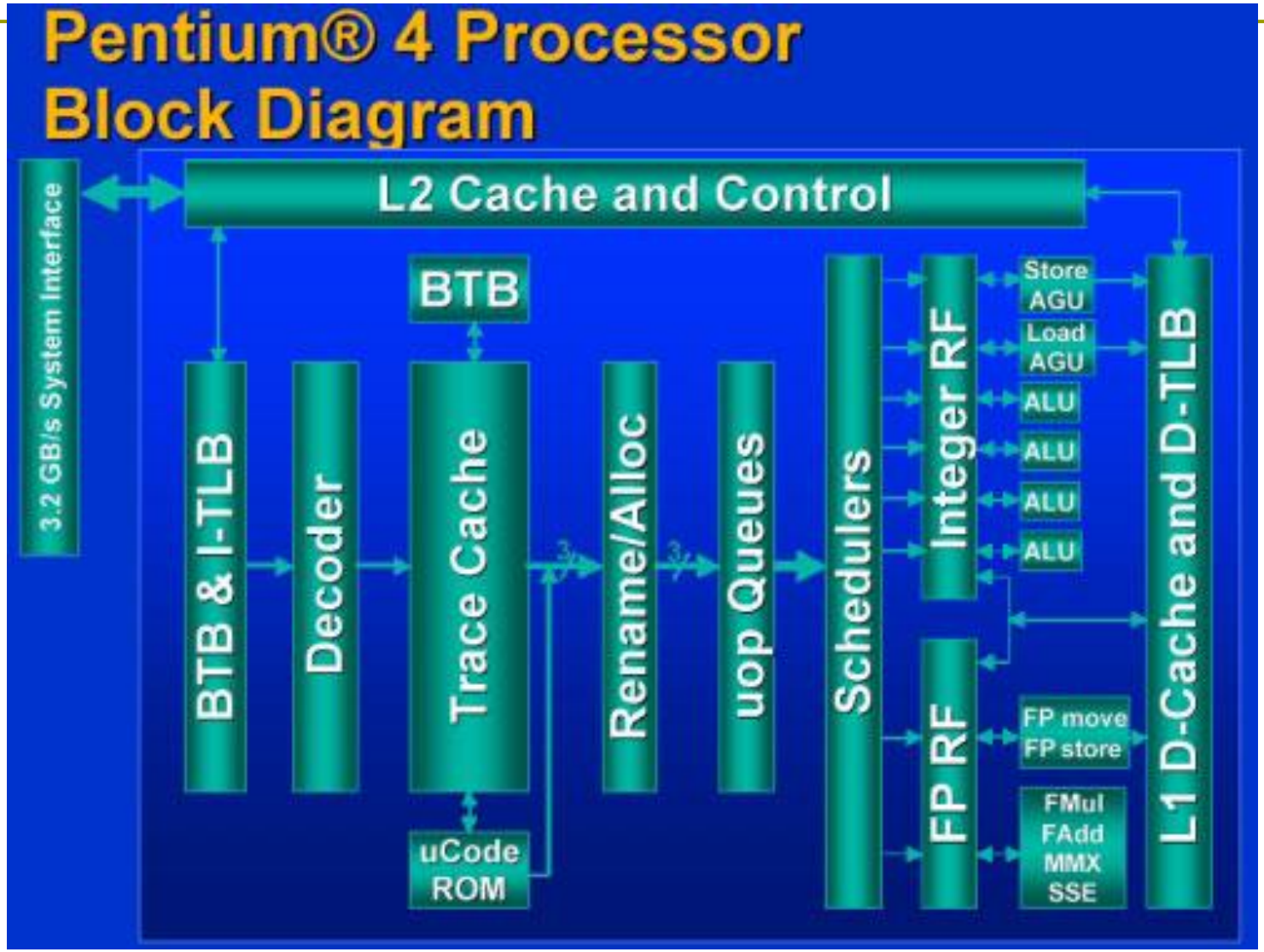
CPU block diagrams – AMD K62



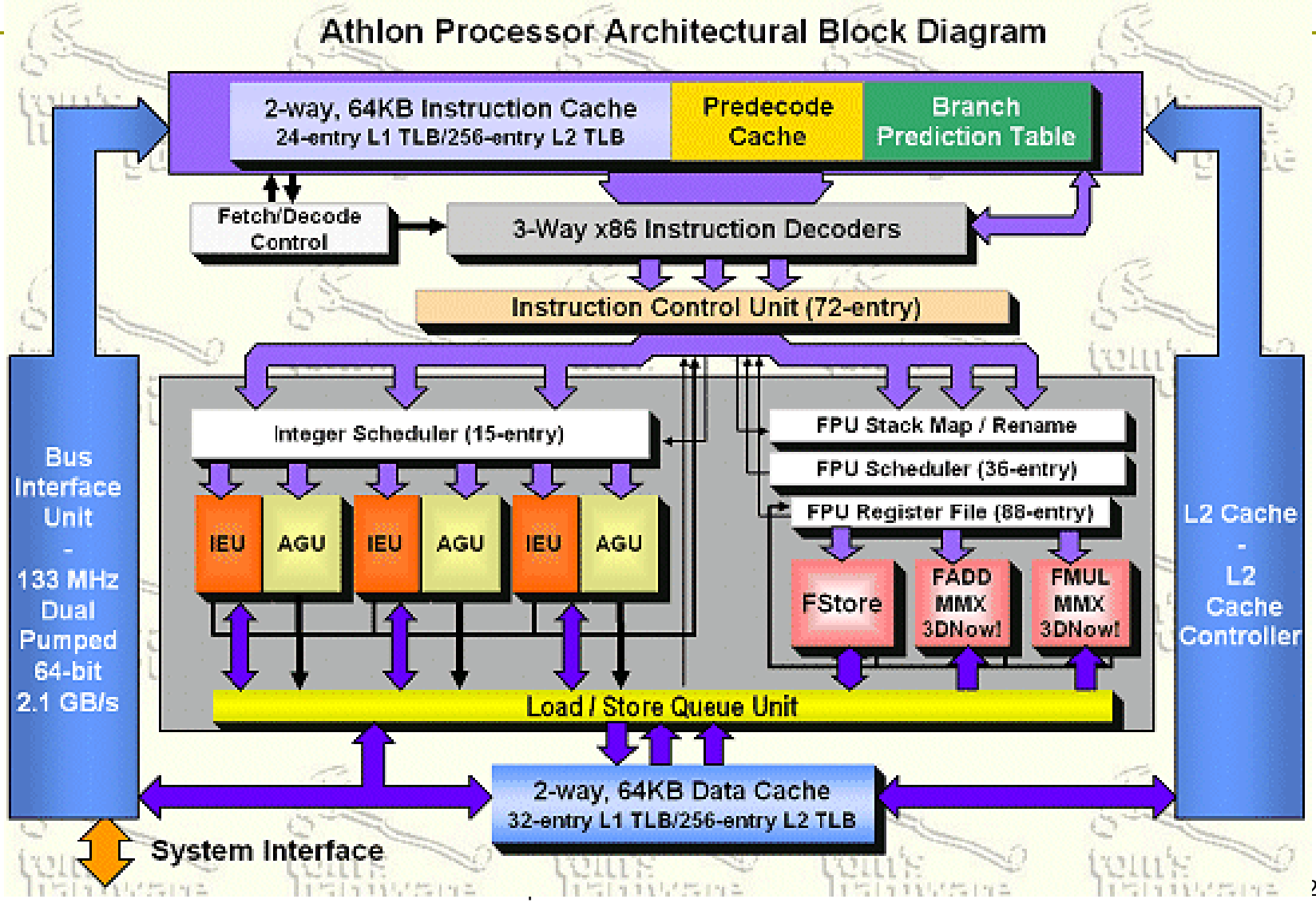
CPU block diagrams – Intel Pen III



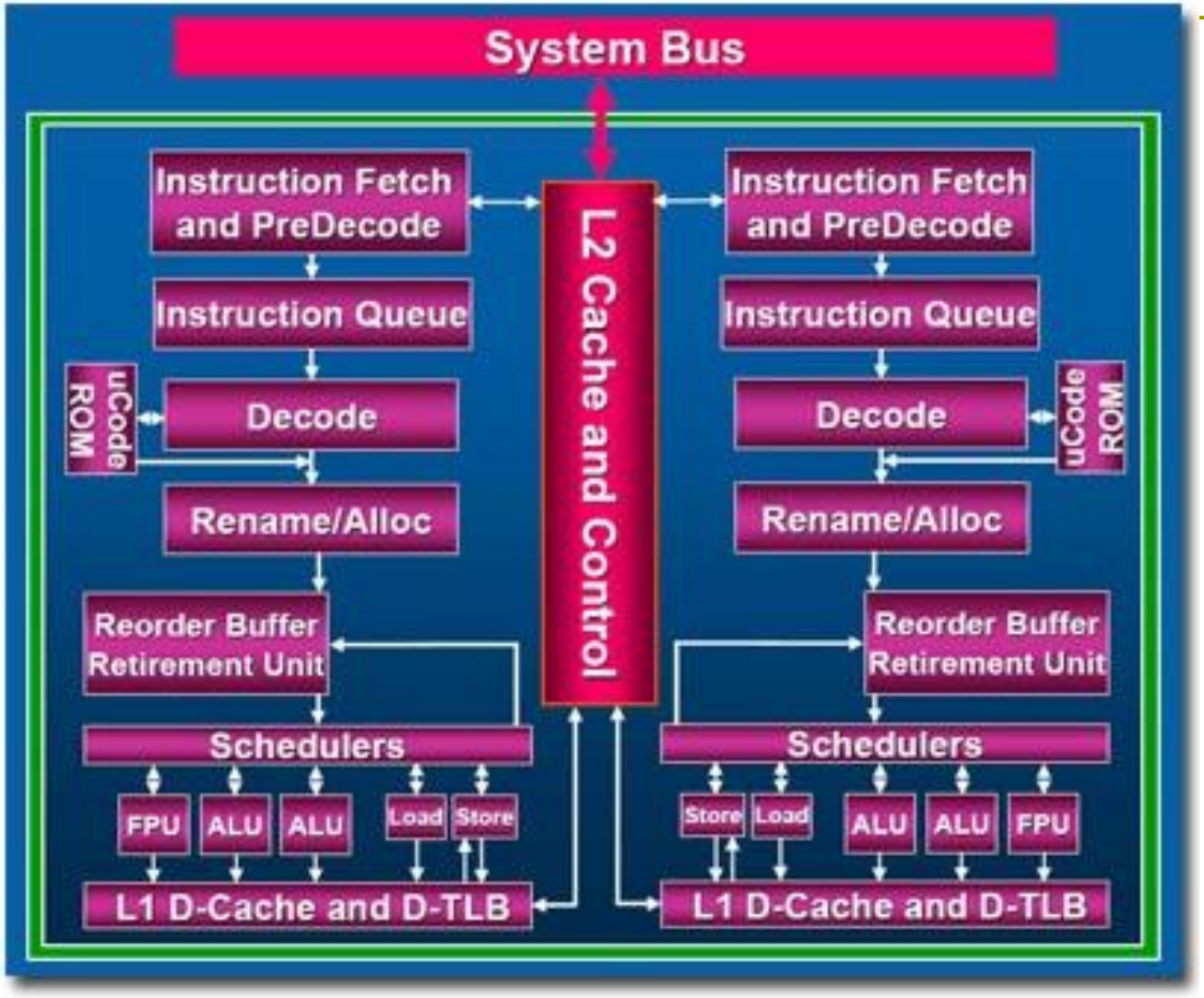
CPU block diagrams - Intel Pen IV



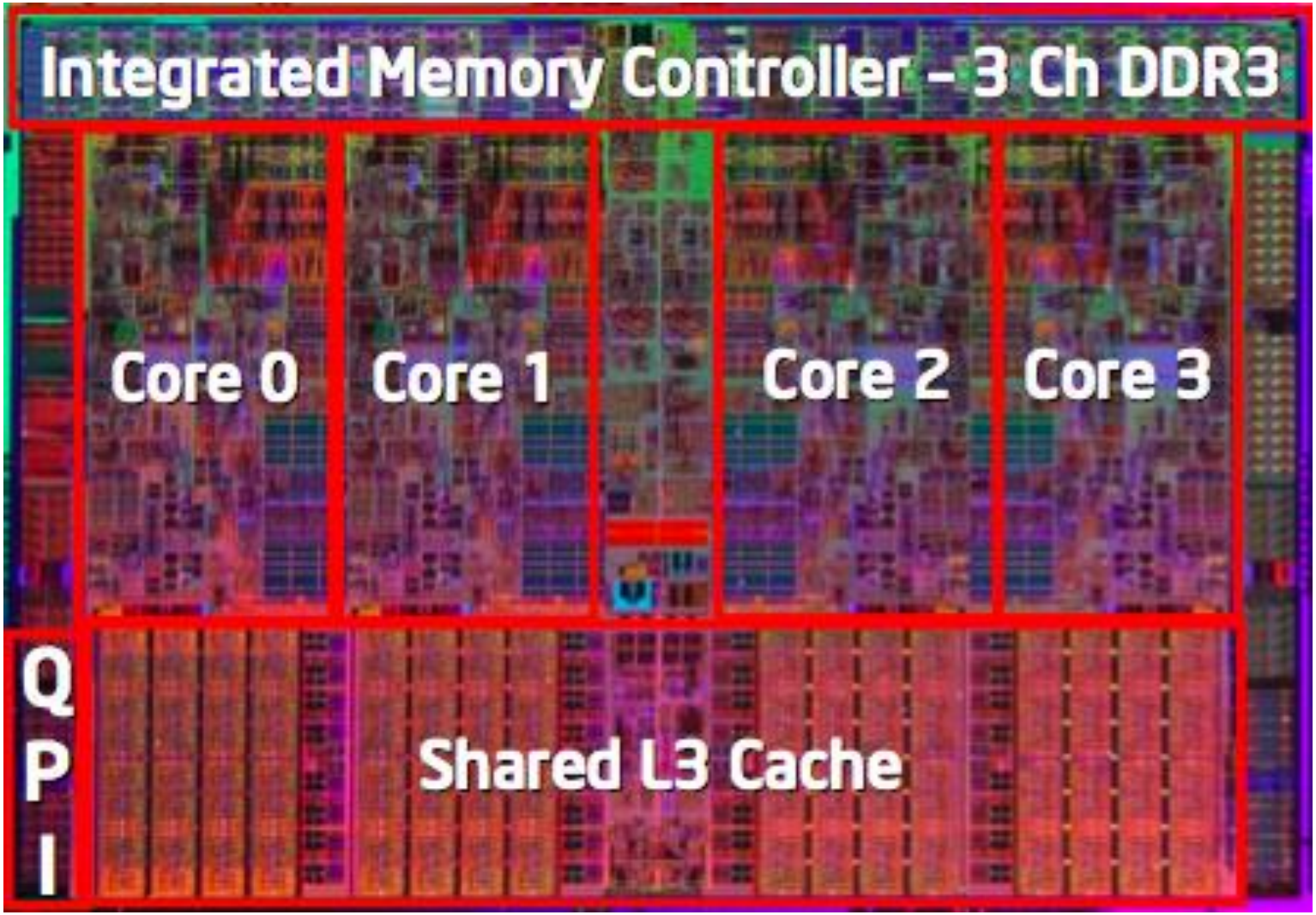
CPU block diagrams-AMD Athlon XP



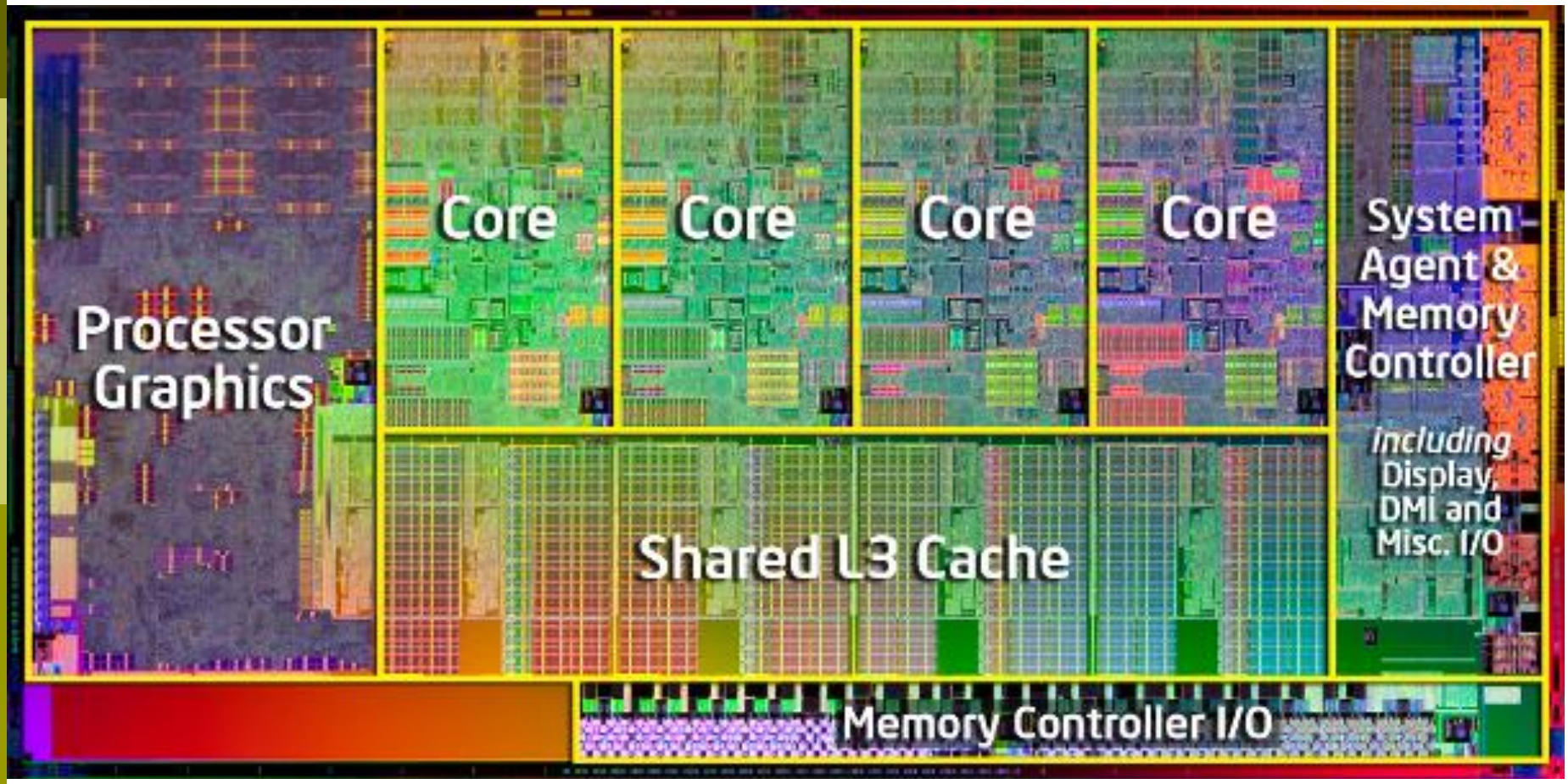
CPU block diagrams-Intel Core 2 Duo



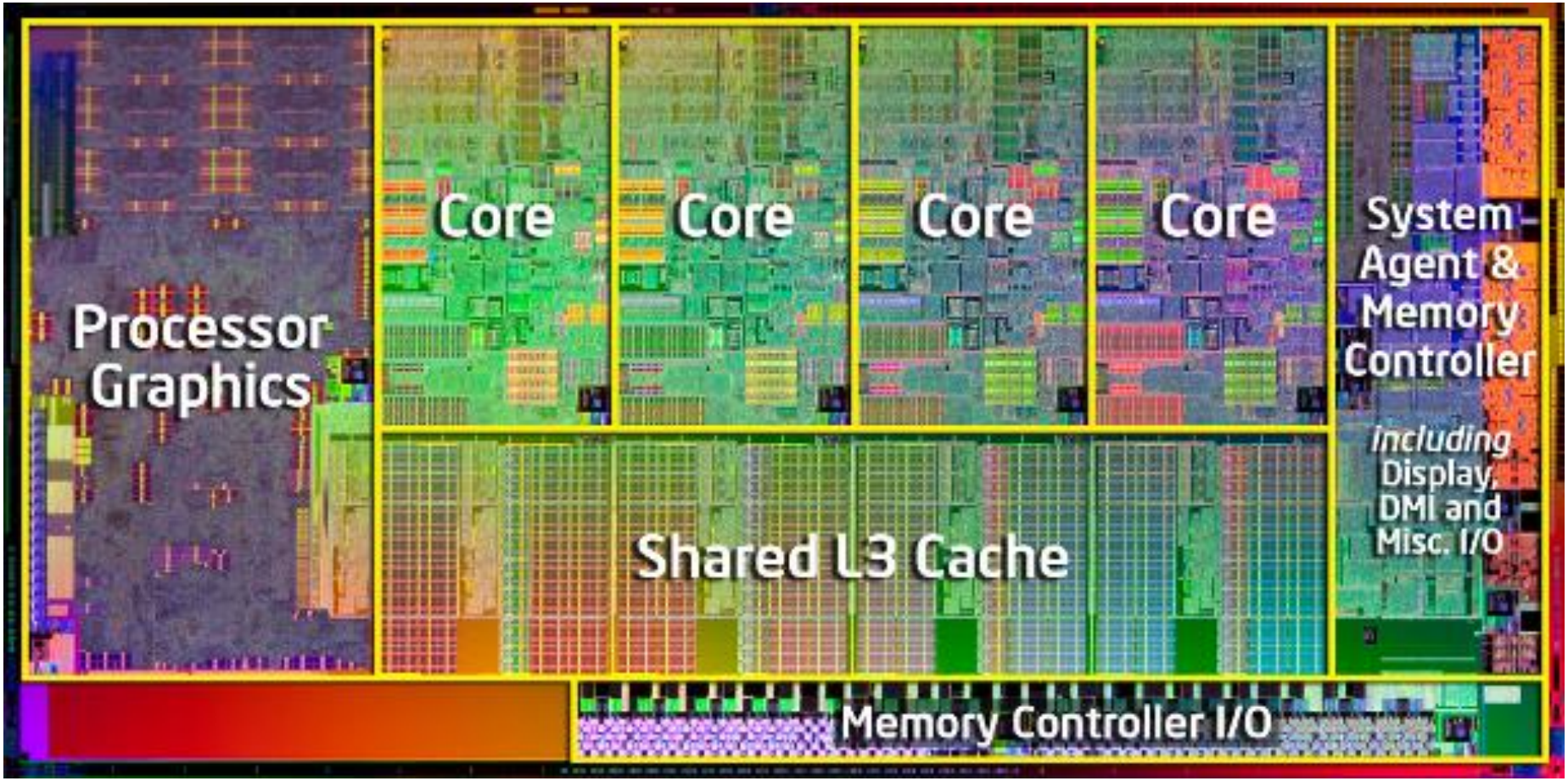
CPU block diagrams – Intel Nehalem Core i5/i7 (2008)



CPU block diagrams - Intel Sandy Bridge Core i5/i7 (2010)



CPU block diagrams - Intel Kaby Lake Core i5/i7 (2016)



CPU block diagrams - Intel Alder Lake Core i5/i7 (2021)