Computer Architecture
7. Computer Buses

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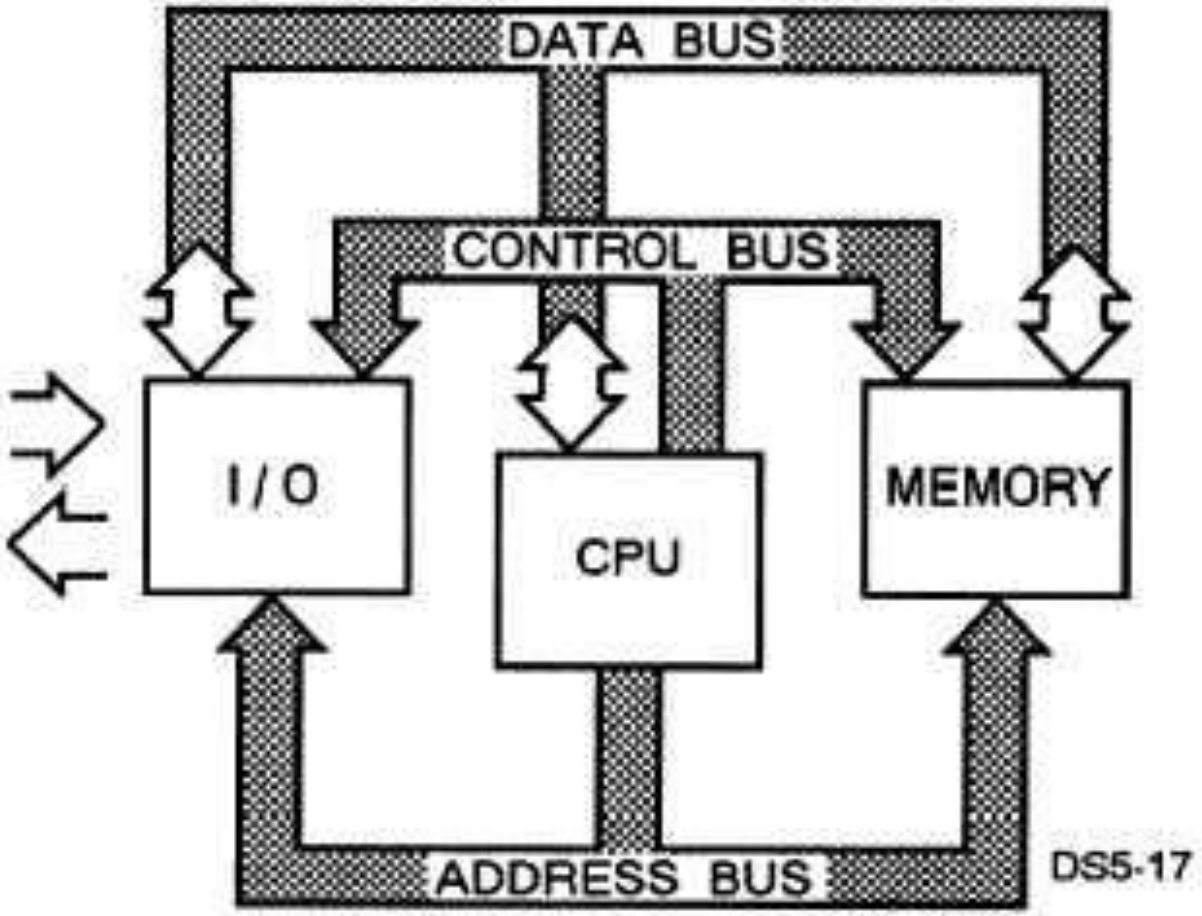
Main topics

- Introduction to computer buses
- ISA, EISA buses
- PCI buses
- AGP buses
- PCI Express bus

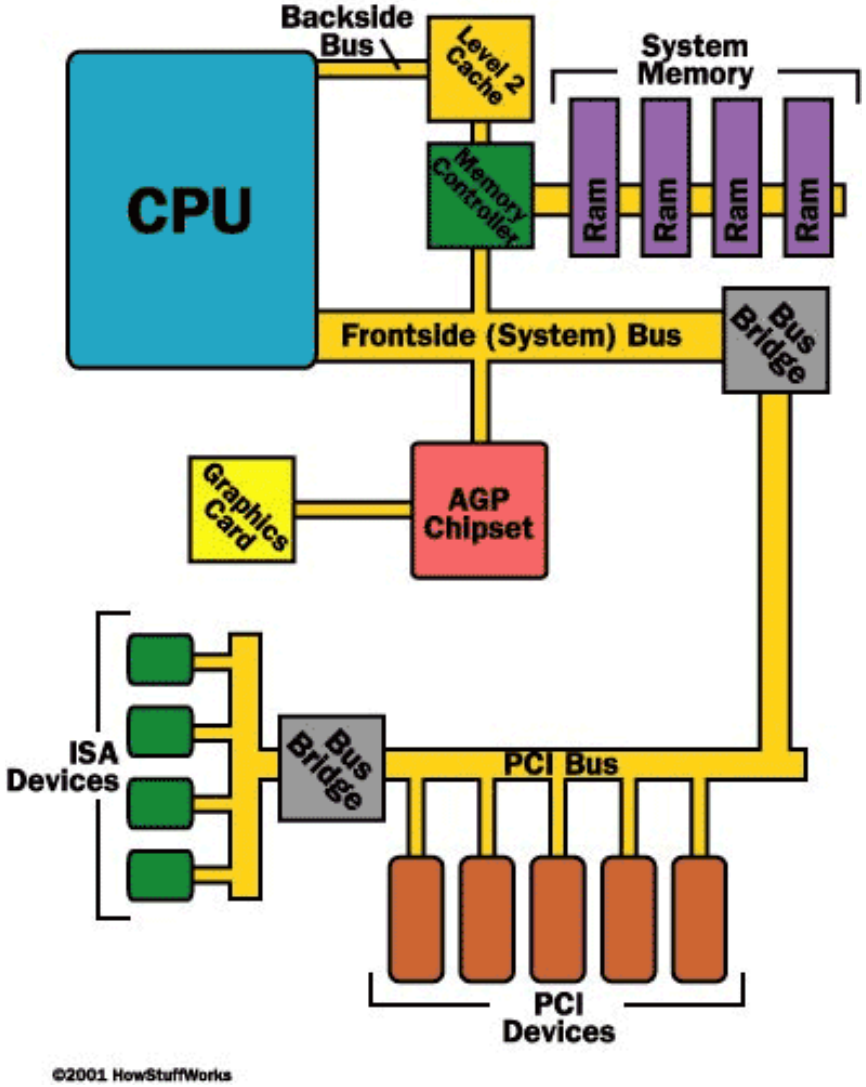
Introduction to Computer Buses

- Computer bus is a subsystem that transfers data between components inside a computer.
- Computer bus usually consists of 3 sub-buses:
  - Address bus (A Bus)
  - Data bus (D Bus)
  - Control bus (C Bus)
- Common computer buses: ISA, EISA, PCI, AGP, PCI Express (or PCIe), USB bus, etc.

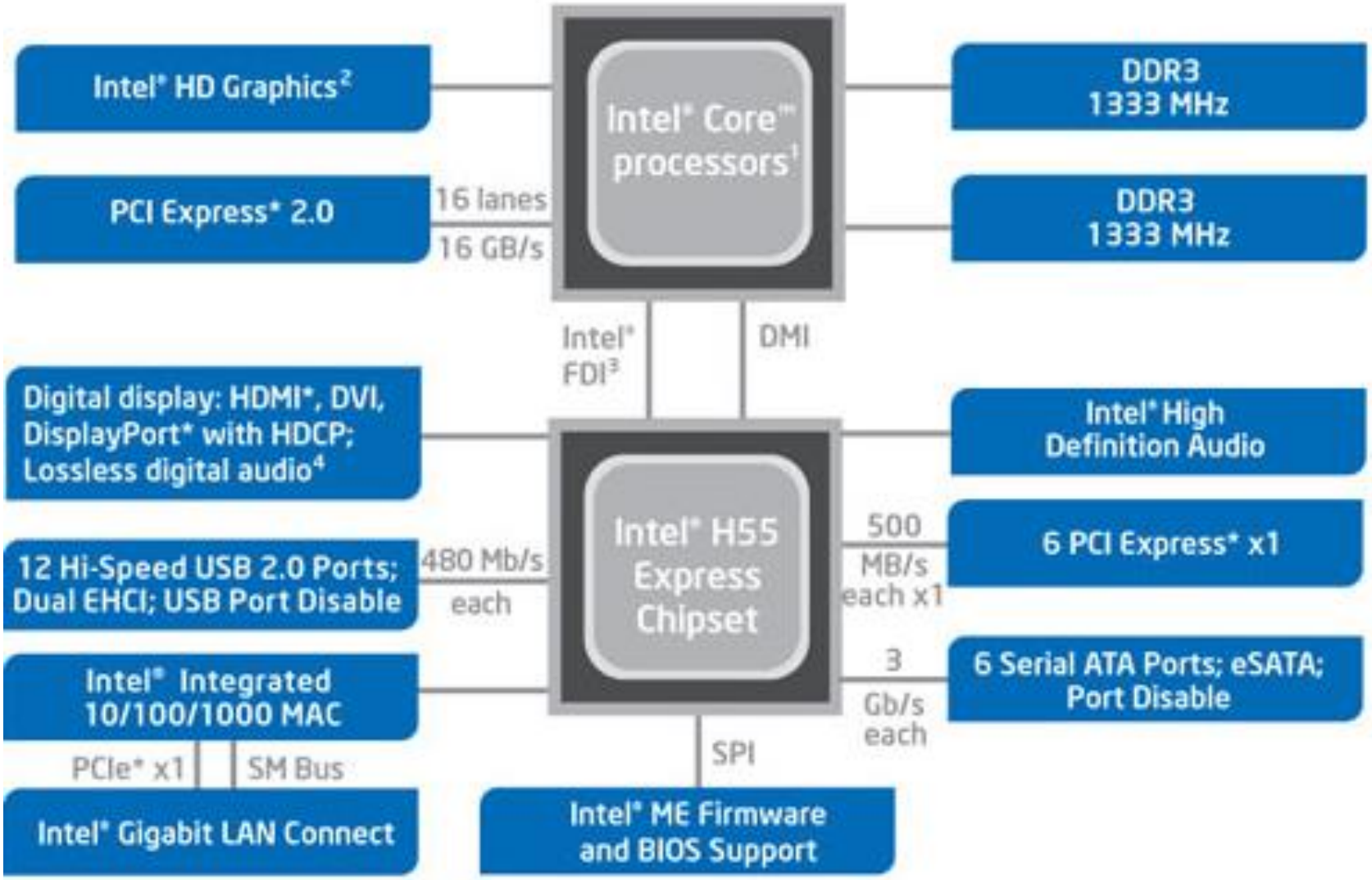
Computer Buses – Principle Diagram



Computer Buses – Modern Systems

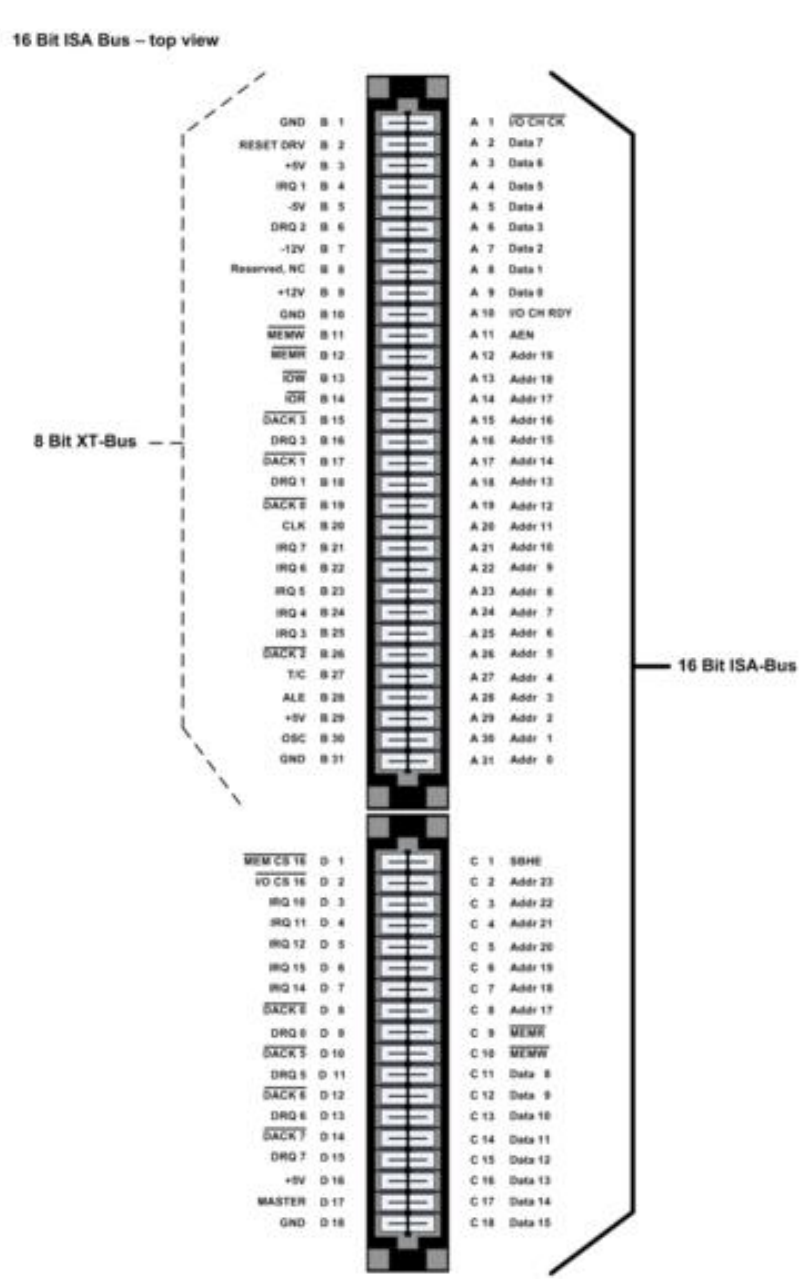


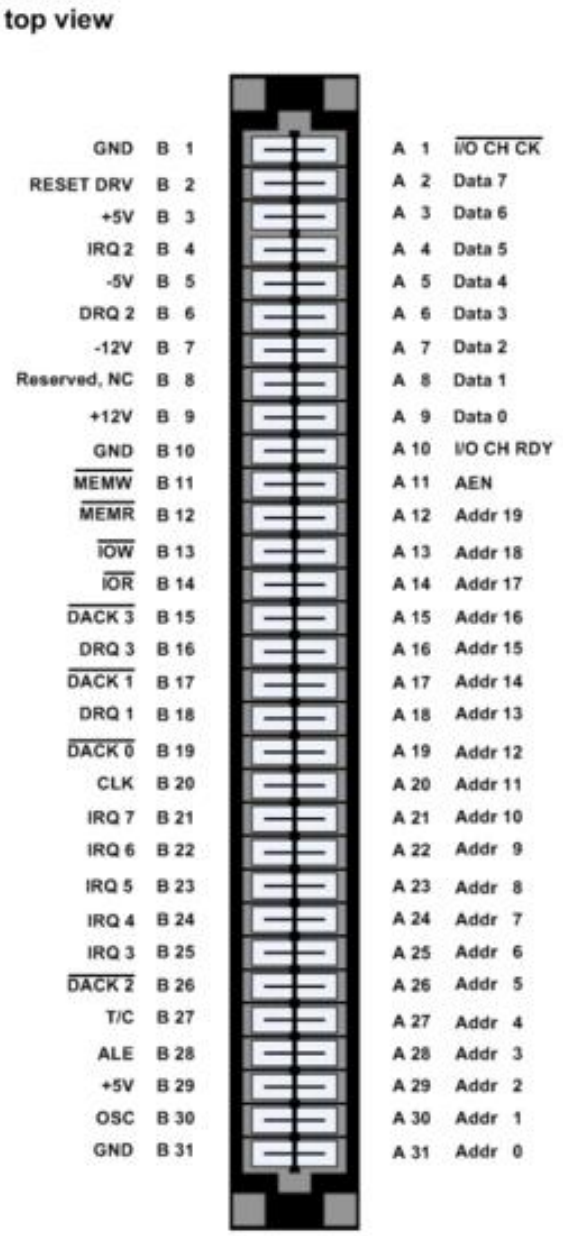
Computer Buses – Modern Systems



ISA - Industrial Standard Architecture

- ISA was developed by IBM in 1981
- Bit width: 8 (XT) or 16 (AT) bits
- Number of max devices: 6
- Clock speed: 4, 6, 8MHz


16 Bit ISA Bus – top view
8 Bit XT-Bus
16 Bit ISA-Bus
GND B 1
RESET DRV B 2
+5V B 3
IRQ 1 B 4
-5V B 5
DRQ 2 B 6
-12V B 7
Reserved, NC B 8
+12V B 9
GND B 10
MEMW B 11
MEMR B 12
IOW B 13
IOR B 14
DACK 3 B 15
DRQ 3 B 16
DACK 1 B 17
DRQ 1 B 18
DACK 0 B 19
CLK B 20
IRQ 7 B 21
IRQ 6 B 22
IRQ 5 B 23
IRQ 4 B 24
IRQ 3 B 25
DACK 2 B 26
T/C B 27
ALE B 28
+5V B 29
OSC B 30
GND B 31
A 1 I/O CH CK
A 2 Data 7
A 3 Data 6
A 4 Data 5
A 5 Data 4
A 6 Data 3
A 7 Data 2
A 8 Data 1
A 9 Data 0
A 10 I/O CH RDY
A 11 AEN
A 12 Addr 19
A 13 Addr 18
A 14 Addr 17
A 15 Addr 16
A 16 Addr 15
A 17 Addr 14
A 18 Addr 13
A 19 Addr 12
A 20 Addr 11
A 21 Addr 10
A 22 Addr 9
A 23 Addr 8
A 24 Addr 7
A 25 Addr 6
A 26 Addr 5
A 27 Addr 4
A 28 Addr 3
A 29 Addr 2
A 30 Addr 1
A 31 Addr 0
MEM CS 16 D 1
I/O CS 16 D 2
IRQ 10 D 3
IRQ 11 D 4
IRQ 12 D 5
IRQ 15 D 6
IRQ 14 D 7
DACK 0 D 8
DRQ 0 D 9
DACK 5 D 10
DRQ 5 D 11
DACK 6 D 12
DRQ 6 D 13
DACK 7 D 14
DRQ 7 D 15
+5V D 16
MASTER D 17
GND D 18
C 1 SBHE
C 2 Addr 23
C 3 Addr 22
C 4 Addr 21
C 5 Addr 20
C 6 Addr 19
C 7 Addr 18
C 8 Addr 17
C 9 MEMR
C 10 MEMW
C 11 Data 8
C 12 Data 9
C 13 Data 10
C 14 Data 11
C 15 Data 12
C 16 Data 13
C 17 Data 14
C 18 Data 15


8 Bit XT Bus – top view
GND B 1
RESET DRV B 2
+5V B 3
IRQ 2 B 4
-5V B 5
DRQ 2 B 6
-12V B 7
Reserved, NC B 8
+12V B 9
GND B 10
MEMW B 11
MEMR B 12
IOW B 13
IOR B 14
DACK 3 B 15
DRQ 3 B 16
DACK 1 B 17
DRQ 1 B 18
DACK 0 B 19
CLK B 20
IRQ 7 B 21
IRQ 6 B 22
IRQ 5 B 23
IRQ 4 B 24
IRQ 3 B 25
DACK 2 B 26
T/C B 27
ALE B 28
+5V B 29
OSC B 30
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A 1 I/O CH CK
A 2 Data 7
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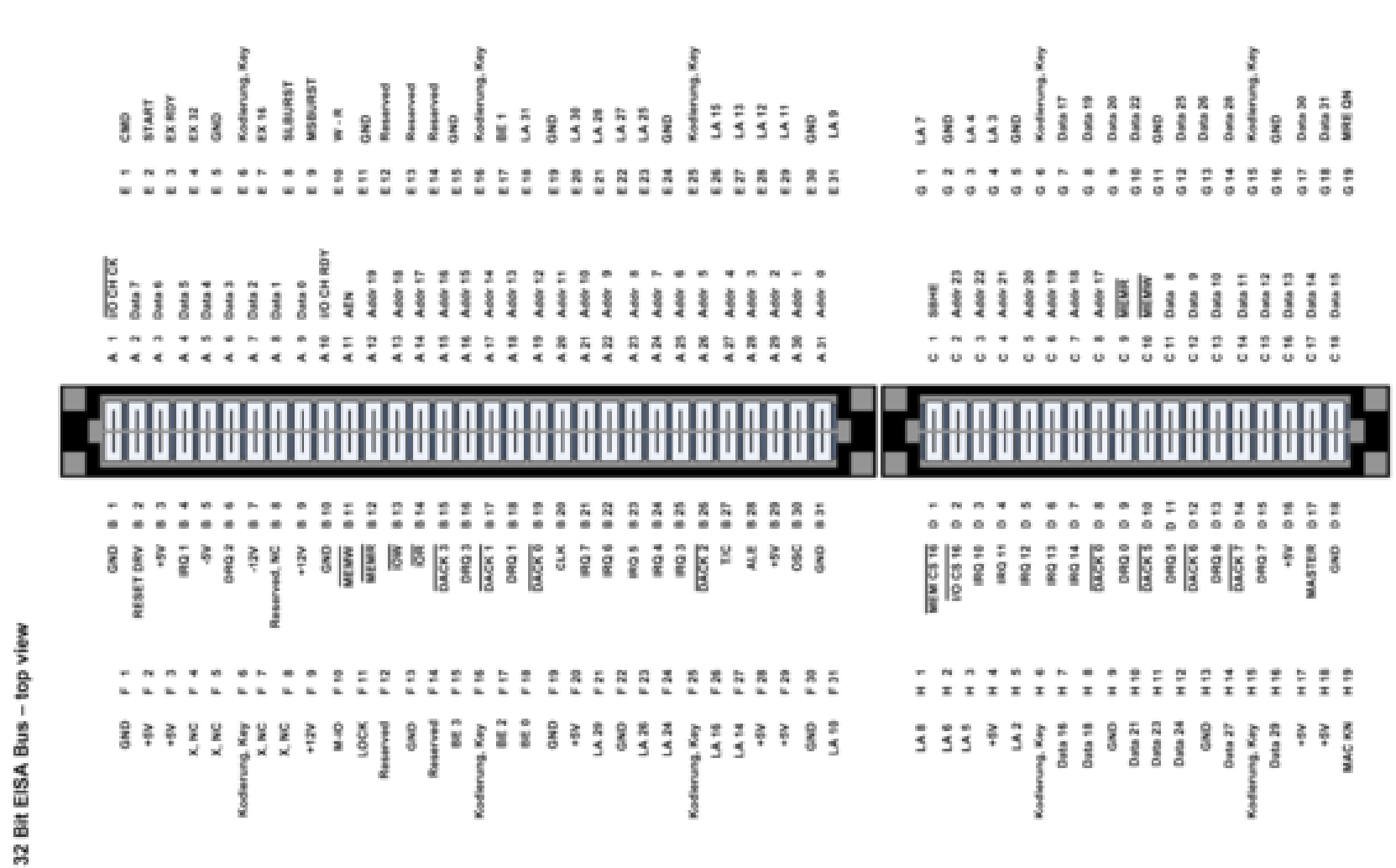
A 15 Addr 16
A 16 Addr 15
A 17 Addr 14
A 18 Addr 13
A 19 Addr 12
A 20 Addr 11
A 21 Addr 10
A 22 Addr 9
A 23 Addr 8
A 24 Addr 7
A 25 Addr 6
A 26 Addr 5
A 27 Addr 4
A 28 Addr 3
A 29 Addr 2
A 30 Addr 1
A 31 Addr 0

EISA buses

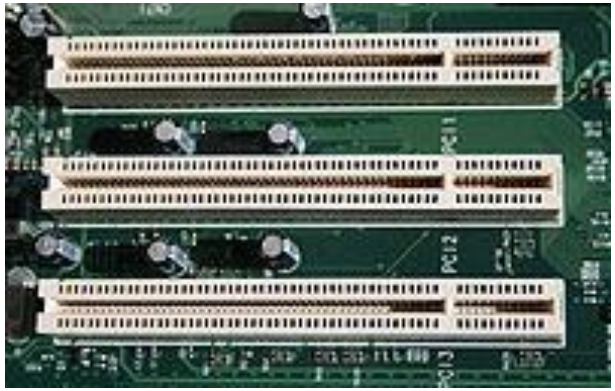
- EISA is an ISA extension released in 1988.
- Bit width: 32 bits
- EISA is compatible with 8 and 16 bit ISA devices
- Number of devices: 1 per slot
- Clock speed: 8.33MHz
- Data transfer rate: 33MB/s.

EISA buses

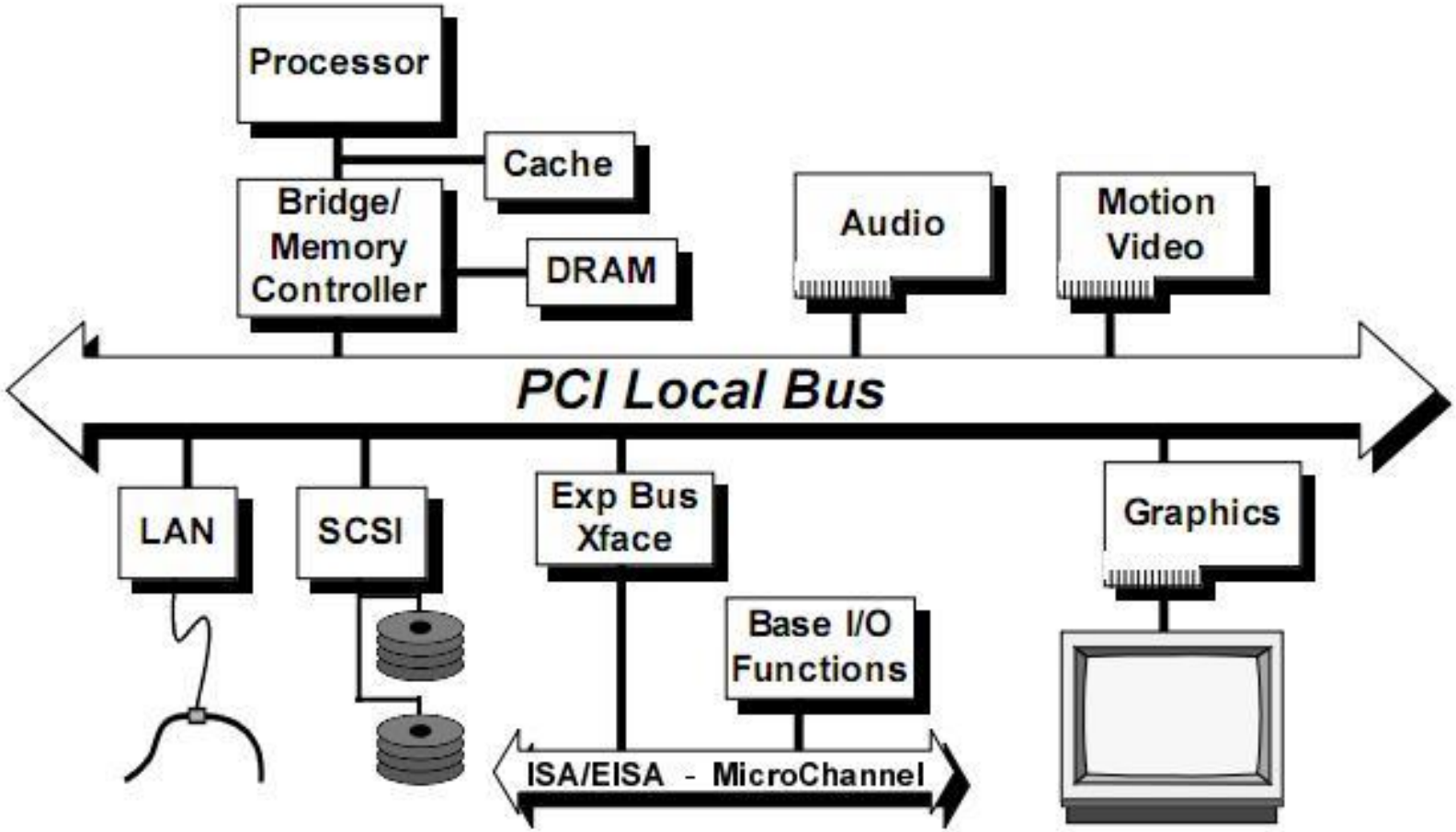


PCI Buses

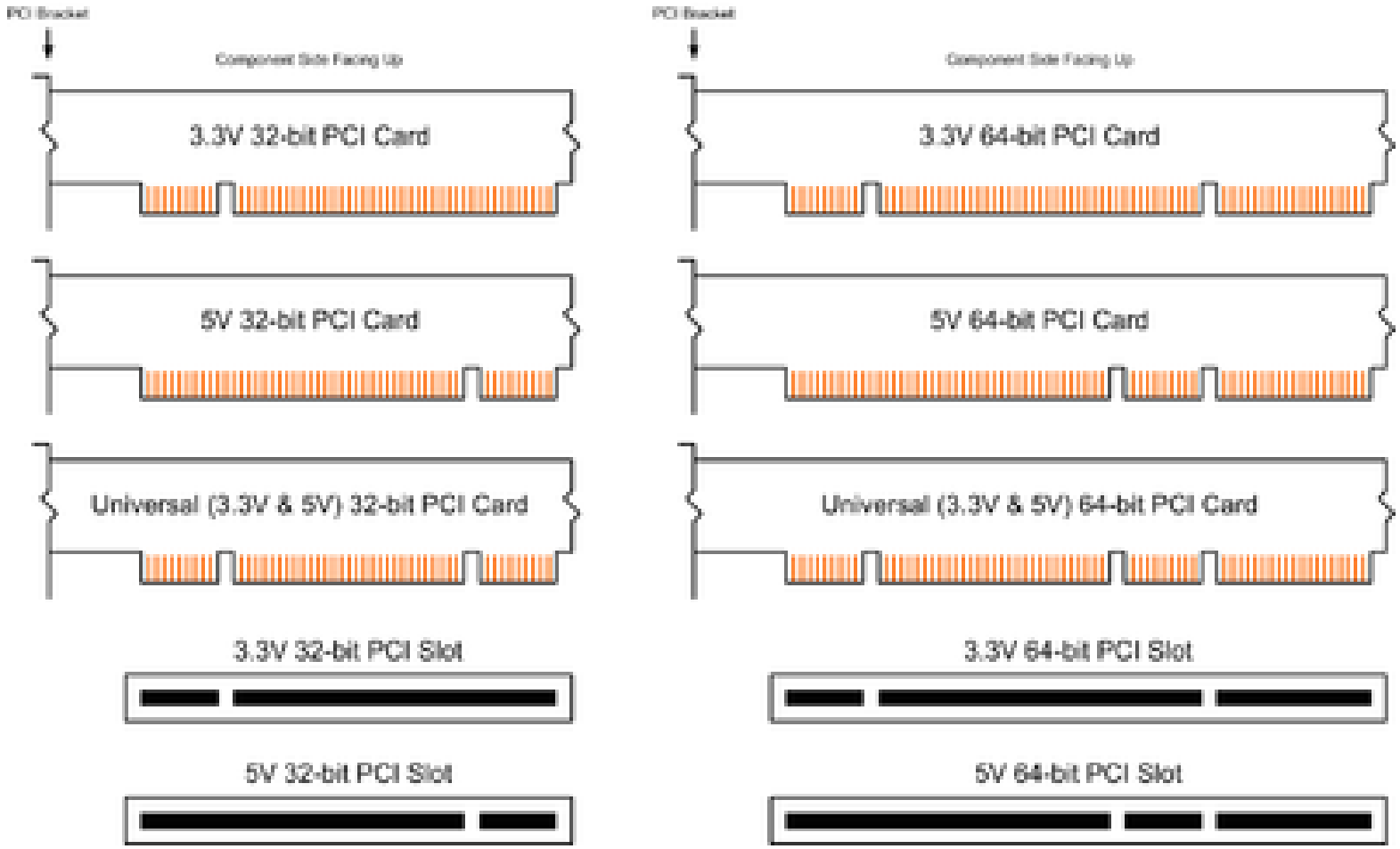
- PCI (Peripheral Component Interconnect) bus was developed by Intel in 1993.
- Bit width: 32 or 64 bits
- Capacity:
  - 133 MB/s (32bit at 33MHz)
  - 266 MB/s (32bit at 66MHz or 64bit at 33MHz)
  - 533 MB/s (64bit at 66MHz)



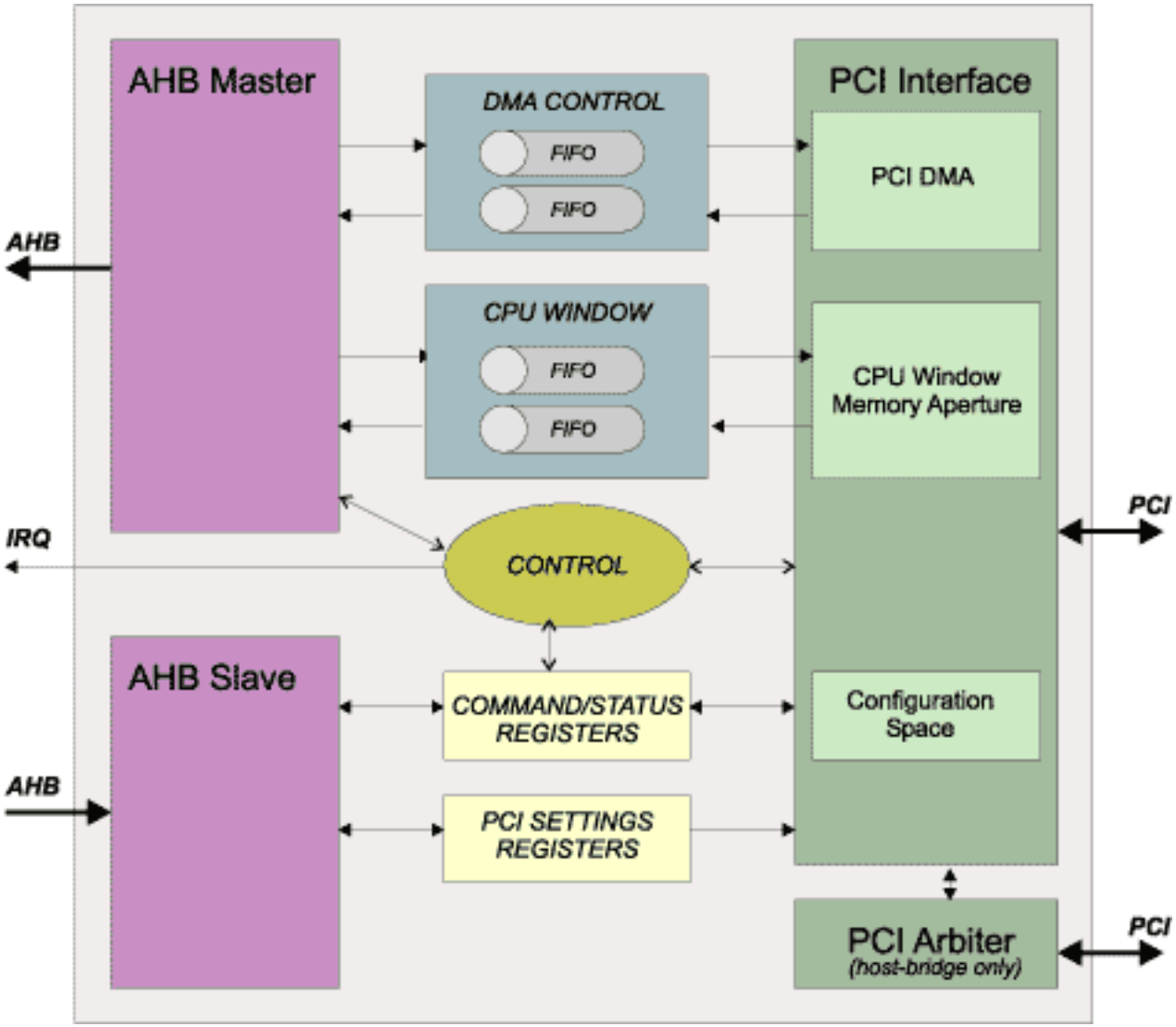
PCI Local Buses



32 bit vs 64 bit PCI buses



PCI Block Diagram



PCI Bus Signals

- Signals to initiate a transaction:
  - REQ#: bus request signal sent by initiator
  - GNT#: bus grant signal given by Arbiter
- Signals to control a transaction:
  - FRAME#: Start a bus cycle
  - IRDY#: Initiator is ready
  - DEVSEL#: Target confirms transaction begin
  - TRDY#: Target is ready
  - STOP#: Stop a transaction.

PCI Bus Transaction Phases

- A PCI transaction (a session of data transmission on PCI bus) usually consists of 3 phases:
  - Arbitration: Initialize a transaction
  - Address: Determine address of parties participated in a transaction
  - Data: Transfer data.

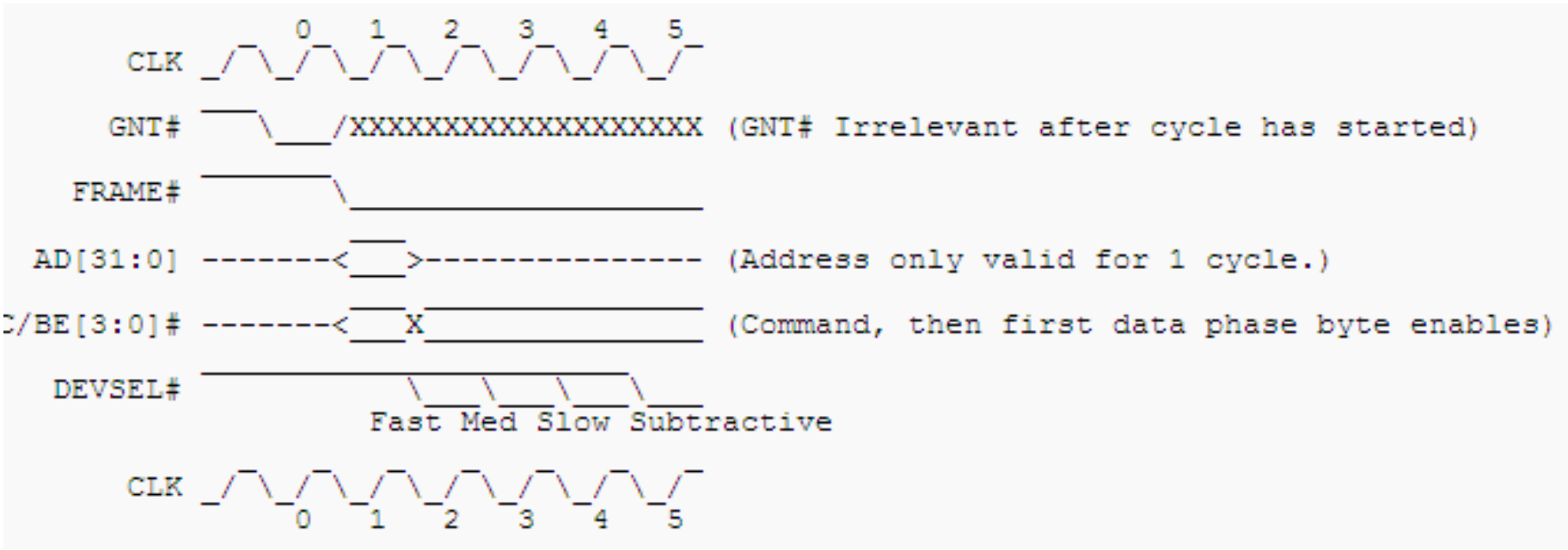
PCI Bus Transaction Phases

- Arbitration
  - A PCI device (initiator) sends REQ# signal to Arbiter to use bus
  - If bus is free, Arbiter sends GNT# to initiator
  - If bus is busy, the request is added into a queue
  - GNT# signals may be removed by Arbiter at any time
  - A PCI device with granted GNT# can start a PCI transaction if bus is idle.

PCI Bus Transaction Phases

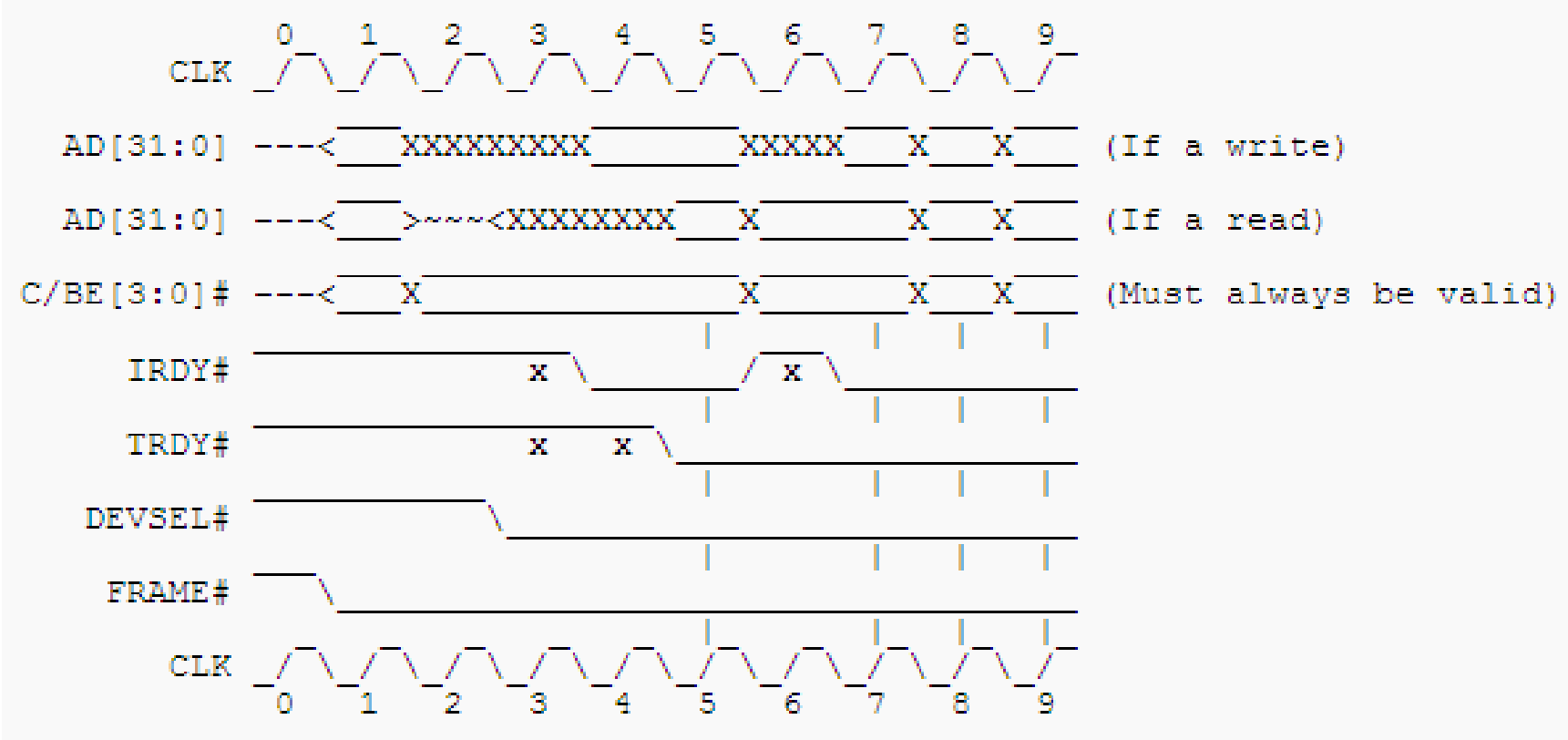
- Address phase
  - PCI device with GNT# can start a PCI transaction by sending FRAME# signal and send the target address and associated command (Read/Write)
  - Each other device examines the address and command and decides whether to respond as the target by asserting DEVSEL#.
  - A device must respond by asserting DEVSEL# within 3 cycles.

PCI Bus- Address phase timing



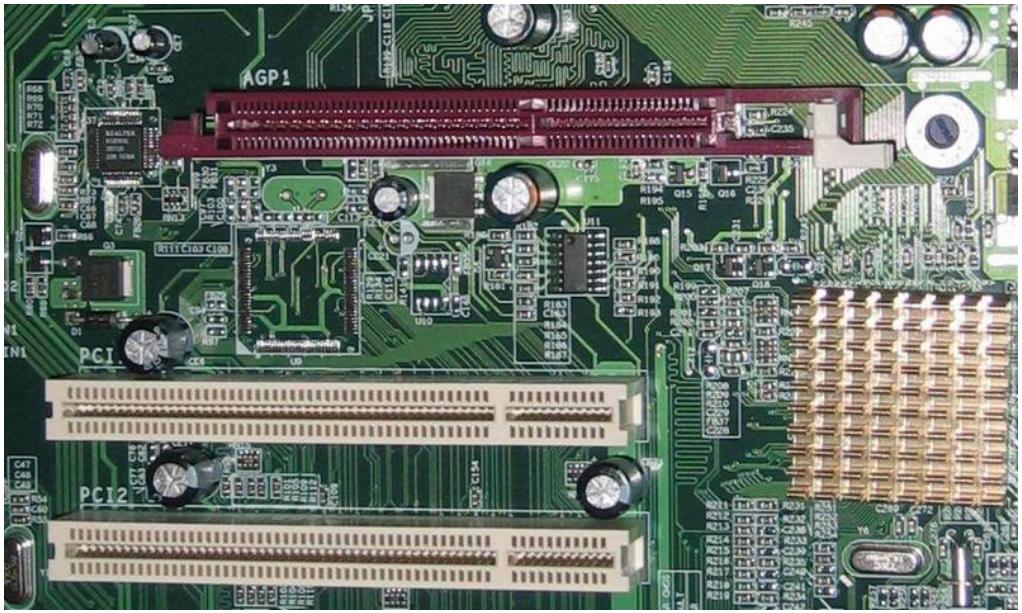
PCI Bus – Data Phase

- After the address phase (when DEVSEL# goes low) comes a burst of one or more data phases

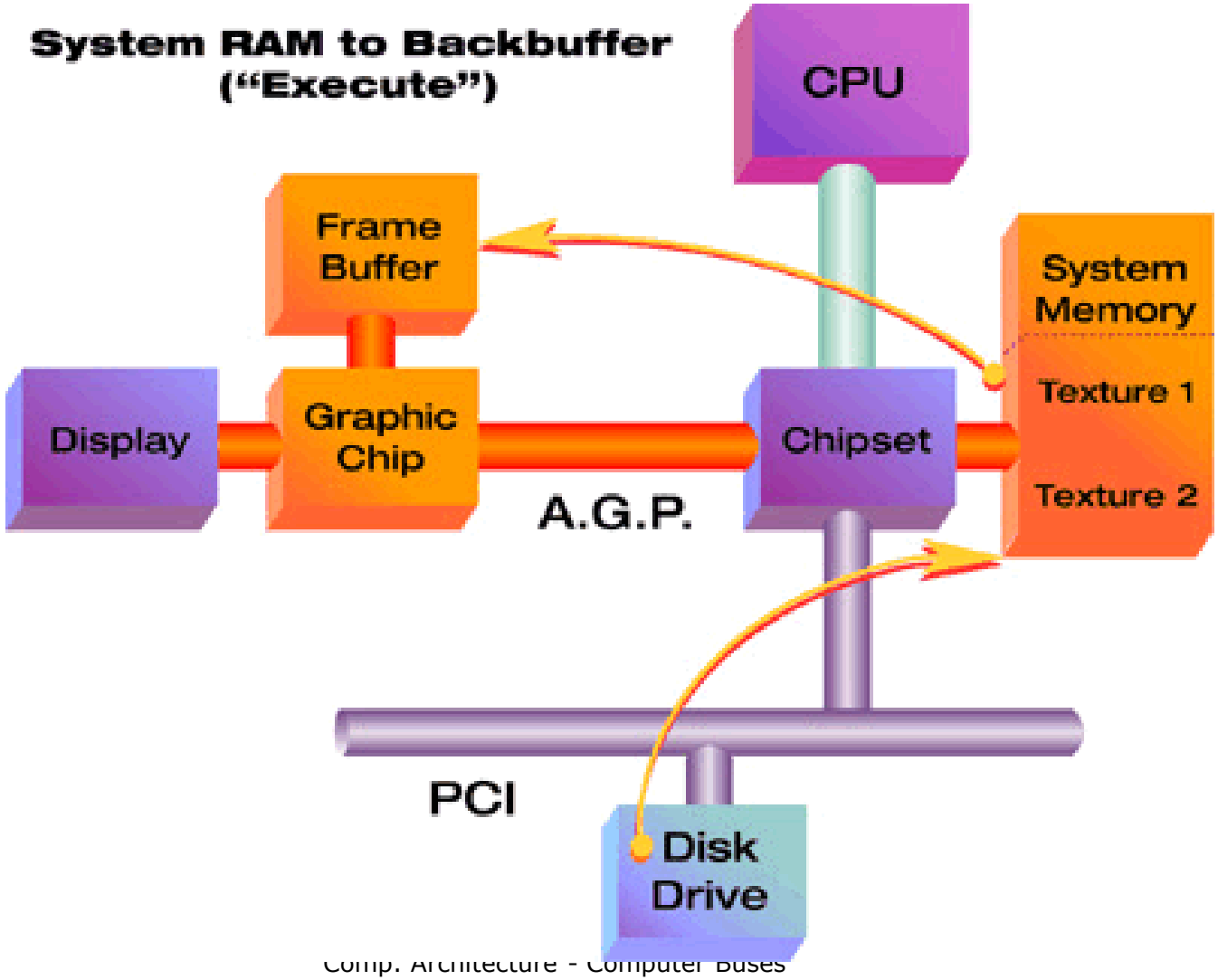


AGP - Accelerated Graphics Port

- AGP was developed by Intel in 1993
- Bit width: 32
- Data transfer rate
  - 1x: 66MHz, 266MB/s
  - 2x: 133MHz, 533MB/s
  - 4x: 266MHz, 1066MB/s
  - 8x: 533MHz, 2133MB/s



AGP - Accelerated Graphics Port

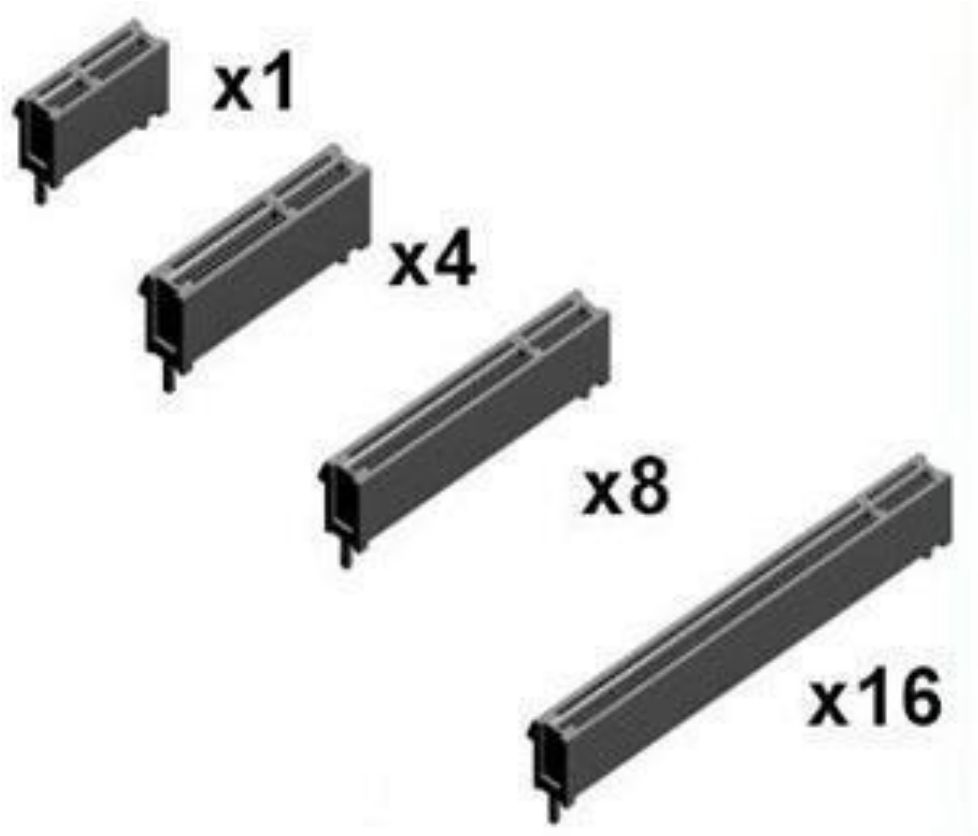


AGP Card

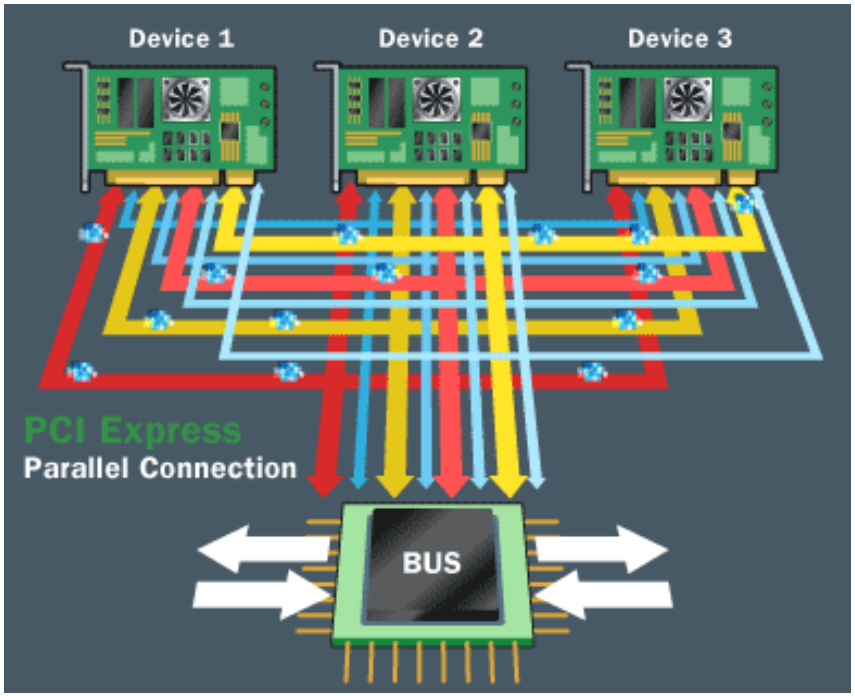
PCI Express

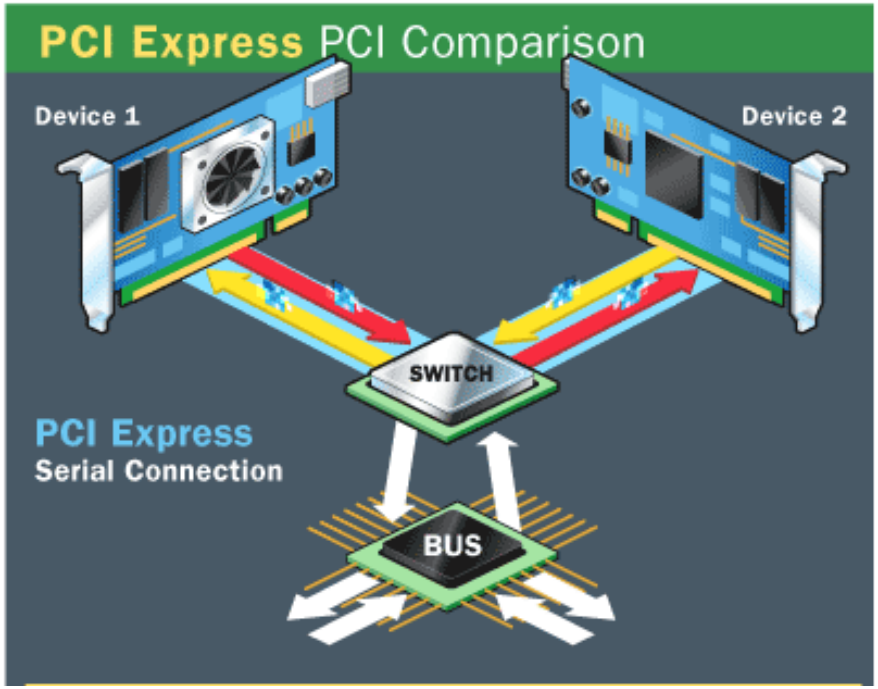
- PCI Express (PCIe) was developed by Intel in 2004.
- Width in bits: 1-32
- Communication type: serial (point to point)
- Capacity:
  - Per lane:
    - v1.x: 250 MB/s
    - v2.0: 500 MB/s
    - v3.0: 1 GB/s
    - v4.0: 1,969 GB/s
    - v5.0: 3,938 GB/s
  - 16 lane slot:
    - v1.x: 4 GB/s
    - v2.0: 8 GB/s
    - v3.0: 16 GB/s
    - v4.0: 31,51 GB/s
    - v5.0: 63 GB/s

PCI Express Slots



PCI Express vs PCI





Devices using PCI share a common bus, but each device using PCI Express has its own dedicated connection to the switch

PCIe Architecture

- PCIe is structured around point-to-point serial links.
- A pair of 2 serial links (one in each direction) is a lane.
- Lanes are routed by a hub on the main-board acting as a crossbar switch.
- Physical PCIe slots may contain from 1 to 32 lanes.

PCIe Architecture – Serial Bus

- PCIe is a type of serial bus:
  - Parallel buses (ISA, PCI, AGP) require all bits of a transferred data unit to come to destination at the same time;
  - Due to the timing skew issue, bits of a transferred data unit may fail come to destination at the same time, which makes it difficult to recover the final data word;
  - There is no timing issue in serial buses because they don't require all bits of a transferred data unit to come to destination at the same time.