

**Preliminary
BIOS and Kernel
Developer's Guide
(BKDG)
for AMD Family 16h
Models 00h-0Fh
(Kabini) Processors**

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Revision History

KB BKDG Revision 3.00 initial release.

1 Overview

This document defines AMD Family 16h Models 00h-0Fh Processors, henceforth referred to as the processor.

- The processor overview is located at [2.1 \[Processor Overview\]](#).
- The processor is distinguished by the combined ExtFamily and BaseFamily fields of the CPUID instruction (see [CPUID Fn8000_0001_EAX](#) in [3.18 \[CPUID Instruction Registers\]](#)).

1.1 Intended Audience

This document provides the processor behavioral definition and associated design notes. It is intended for platform designers and for programmers involved in the development of low-level BIOS (basic input/output system) functions, drivers, and operating system kernel modules. It assumes prior experience in personal computer platform design, microprocessor programming, and legacy x86 and AMD64 microprocessor architecture. The reader should also have familiarity with various platform technologies, such as DDR DRAM.

1.2 Reference Documents

- Advanced Configuration and Power Interface (ACPI) Specification. www.acpi.info.
- AMD64 Architecture Programmer's Manual Volume 1: Application Programming, #24592.
- AMD64 Architecture Programmer's Manual Volume 2: System Programming, #24593.
- AMD64 Architecture Programmer's Manual Volume 3: Instruction-Set Reference, #24594.
- AMD64 Architecture Programmer's Manual Volume 4: 128-Bit and 256-Bit Media Instructions, #26568.
- AMD64 Architecture Programmer's Manual Volume 5: 64-Bit Media and x87 Floating-Point Instructions, #26569.
- Software Optimization Guide for AMD Family 16h Processors, #52128.
- Revision Guide for AMD Family 16h Models 00h-0Fh Processors, #51810
- JEDEC standards. www.jedec.org.
- PCI local bus specification. (www.pcisig.org).
- PCI Express® specification. (www.pcisig.org).
- Universal Serial Bus Specification (<http://www.usb.org>)
- Serial ATA Specification (<http://www.sata-io.org>)
- AT Attachment with Packet Interface (<http://www.t13.org>)
- SD Host Controller Standard Specification (<https://www.sdcard.org>)
- Alert Standard Format Specification (<http://dmtf.org/standards/asf>)

1.3 Conventions

1.3.1 Numbering

- **Binary numbers.** Binary numbers are indicated by appending a “b” at the end, e.g., 0110b.
- **Decimal numbers.** Unless specified otherwise, all numbers are decimal. This rule does not apply to the register mnemonics described in [3.1 \[Register Descriptions and Mnemonics\]](#); register mnemonics all utilize hexadecimal numbering.
- **Hexadecimal numbers.** hexadecimal numbers are indicated by appending an “h” to the end, e.g., 45f8h.
- **Underscores in numbers.** Underscores are used to break up numbers to make them more readable. They do not imply any operation. E.g., 0110_1100b.

1.3.2 Arithmetic And Logical Operators

In this document, formulas generally follow Verilog conventions for logic equations.

Table 1: Arithmetic and Logical Operators

Operator	Definition
{}	Concatenation. Curly brackets are used to indicate a group of bits that are concatenated together. Each set of bits is separated by a comma. E.g., {Addr[3:2], Xlate[3:0]} represents a 6-bit value; the two MSBs are Addr[3:2] and the four LSB's are Xlate[3:0].
	Bitwise OR. E.g. (01b 10b == 11b).
	Logical OR. E.g. (01b 10b == 1b); treats multibit operand as 1 if ≥ 1 and produces a 1-bit result.
&	Bitwise AND. E.g. (01b & 10b == 00b).
&&	Logical AND. E.g. (01b && 10b == 1b); logical treats multibit operand as 1 if ≥ 1 and produces a 1-bit result.
^	Bitwise exclusive-OR. E.g. (01b ^ 10b == 11b). Sometimes used as “raised to the power of” as well, as indicated by the context in which it is used. E.g. (2^2 == 4).
~	Bitwise NOT. (also known as one’s complement). E.g. (~10b == 01b).
!	Logical NOT. E.g. (!10b == 0b); treats multibit operand as 1 if ≥ 1 and produces a 1-bit result.
<, <=, >, >=, ==, !=	Relational. Less than, Less than or equal, greater, greater than or equal, equal, and not equal.
+, -, *, /, %	Arithmetic. Addition, subtraction, multiplication, division, and modulus.
<<	Bitwise left shift. Shift left first operand by the number of bits specified by the 2nd operand. E.g. (01b << 01b == 10b).
>>	Bitwise right shift. Shift right first operand by the number of bits specified by the 2nd operand. E.g. (10b >> 01b == 01b).
?:	Ternary conditional. E.g. condition ? value if true : value if false. Equivalent to IF condition THEN value if true ELSE value if false.

Table 2: Functions

Function	Definition
ABS	ABS(integer-expression): Remove sign from signed value.
FLOOR	FLOOR(integer-expression): Rounds real number down to nearest integer.
CEIL	CEIL(real-expression): Rounds real number up to nearest integer.
MIN	MIN(integer-expression-list): Picks minimum integer or real value of comma separated list.
MAX	MAX(integer-expression-list): Picks maximum integer or real value of comma separated list.
COUNT	COUNT(integer-expression): Returns the number of binary 1's in the integer.

Table 2: Functions

Function	Definition
ROUND	ROUND(real-expression): Rounds to the nearest integer; halfway rounds away from zero.
UNIT	UNIT(fieldName UnitOfMeasure): Input operand is a register field name that defines all values with the same unit of measure. Returns the value expressed in the unit of measure for the current value of the register field.
POW	POW(base, exponent): POW(x,y) returns the value x to the power of y.

1.3.3 Operator Precedence and Associativity

This document follows C operator precedence and associativity. The following table lists operator precedence (highest to lowest). Their associativity indicates in what order operators of equal precedence in an expression are applied. Parentheses are also used to group sub-expressions to force a different precedence; such parenthetical expressions can be nested and are evaluated from inner to outer. E.g. “X = A | ~B & C” is the same as “X= A | ((~B) & C)”.

Table 3: Operator Precedence and Associativity

Operator	Description	Associativity
!, ~	Logical negation/bitwise complement	right-to-left
*, /, %	Multiplication/division/modulus	left-to-right
+, -	Addition/subtraction	left-to-right
<<, >>	Bitwise shift left, Bitwise shift right	left-to-right
<, <=, >, >=, ==, !=	Relational operators	left-to-right
&	Bitwise AND	left-to-right
^	Bitwise exclusive OR	left-to-right
	Bitwise inclusive OR	left-to-right
&&	Logical AND	left-to-right
	Logical OR	left-to-right
:?	Ternary conditional	right-to-left

1.4 Definitions

Table 4: Definitions

Term	Definition
AP	Application processor. See 2.3 [Processor Initialization] .
BAPM	Bidirectional Application Power Management. See 2.5.9.3 [Bidirectional Application Power Management (BAPM)] .
Battery-Power	The system is running from a battery power source or otherwise undocked from a continuous power supply. Setting using this definition may be required to change during runtime.
BCS	Base configuration space. See 2.7 [Configuration Space] .

Table 4: Definitions

Term	Definition
BERT	Bit error rate tester. A piece of test equipment that generates arbitrary test patterns and checks that a device under test returns them without errors.
BIST	Built-in self-test. Hardware within the processor that generates test patterns and verifies that they are stored correctly (in the case of memories) or received without error (in the case of links).
Boot VID	Boot voltage ID. This is the VDD and VDDNB voltage level that the processor requests from the external voltage regulator during the initial phase of the cold boot sequence. See 2.5.1.2 [Internal VID Registers and Encodings] .
BCD	Binary coded decimal number format.
BSC	Boot strap core. Core 0 of the BSP . Specified by MSR0000_001B[BSC] .
BSP	Boot strap processor. See 2.3 [Processor Initialization] .
CAR	Use of the L2 cache as RAM during boot. See 2.3.3 [Using L2 Cache as General Storage During Boot] .
C-states	These are ACPI-defined core power states. C0 is operational. All other C-states are low-power states in which the processor is not executing code. See 2.5.3.2 [Core C-states] .
Canonical address	An address in which the state of the most-significant implemented bit is duplicated in all the remaining higher-order bits, up to bit 63.
Channel	See DRAM channel.
CMP	Chip multi-processing. Refers to processors that include multiple cores. See 2.1 [Processor Overview] .
COF	Current operating frequency of a given clock domain. See 2.5.3 [CPU Power Management] .
Cold reset	PWROK is deasserted and RESET_L is asserted. See 2.3 [Processor Initialization] .
Core Cluster	Four JG Cores that share L2 resources. See L2 complex .
L2 complex	Four Cores that share L2 resources. See 2.1 [Processor Overview] .
Core	The instruction execution unit of the processor. See 2.1 [Processor Overview] .
CPB	Core performance boost. See 2.5.9.1 [Core Performance Boost (CPB)] .
CpuCore-Num	Specifies the core number. See 2.4.4 [Processor Cores and Downcoreing] .
CPUID function X	Refers to the CPUID instruction when EAX is preloaded with X. See 3.18 [CPUID Instruction Registers] .
CS	Chip select. See D18F2x[5C:40]_dct[0] [DRAM CS Base Address] .
DCT	DRAM controller. See 2.9 [DRAM Controllers (DCTs)] .
DCQ	DRAM controller queue.
DDR3	DDR3 memory technology. See 2.9 [DRAM Controllers (DCTs)] .
DID	Divisor identifier. Specifies the post-PLL divisor used to reduce the COF. See 2.5.3 [CPU Power Management] .
Doubleword	A 32-bit value.
Downcoreing	Removal of cores. See 2.4.4 [Processor Cores and Downcoreing] .
DRAM channel	The part of the DRAM interface that connects to a DIMM. See 2.9 [DRAM Controllers (DCTs)] .

Table 4: Definitions

Term	Definition
Dual-Plane	Refers to a processor or systemboard where VDD and VDDNB are separate and may operate at independent voltage levels. Refer to 2.5.1 [Processor Power Planes And Voltage Control] .
DW	Doubleword. A 32-bit value.
ECS	Extended configuration space. See 2.7 [Configuration Space] .
EDS	Electrical data sheet. See 1.2 [Reference Documents] .
FCH	Fusion Controller Hub. The integrated platform device that contains the IO subsystem and the bridge to system BIOS. See 2.15 [Fusion Controller Hub] .
FDS	Functional data sheet; there is one FDS for each package type.
FID	Frequency identifier. Specifies the PLL frequency multiplier for a given clock domain. See 2.5.3 [CPU Power Management] .
FreeR-unSample-Timer	An internal free running timer used by many power management features. The timer increments at the rate specified by D18F4x110[CSampleTimer] .
GB	Gbyte or Gigabyte; 1,073,741,824 bytes.
#GP	A general-protection exception.
#GP(0)	Notation indicating a general-protection exception (#GP) with error code of 0.
GpuEnabled	GpuEnabled = (D1F0x00!=FFFF_FFFh).
GT/s	Giga-transfers per second.
HCD	Host Controller Driver. A software component.
HTC	Hardware thermal control. See 2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)] .
HTC-active state	Hardware-controlled lower-power, lower-performance state used to reduce temperature. See 2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)] .
IBS	Instruction based sampling. See 2.6.2 [Instruction Based Sampling (IBS)] .
IFCM	Isochronous flow-control mode, as defined in the link specification.
ILM	Internal loopback mode. Mode in which the link receive lanes are connected directly to the transmit lanes of the same link for testing and characterization. See D18F0x[18C:170] [Link Extended Control] .
IO configuration	Access to configuration space through IO ports CF8h and CFCh. See 2.7 [Configuration Space] .
IORR	IO range register. See MSRC001_00[18,16] [IO Range Base (IORR_BASE[1:0])] .
KB	Kbyte or Kilobyte; 1024 bytes.
L1 cache	The level 1 caches (instruction cache and the data cache) and the level 2 caches. See 2.1 [Processor Overview] .
L2 cache	
L2I	The L2 Interface complex common to a set of cores.
L2BC	L2I Base Core. The lowest numbered core for a L2I instance.
Linear (virtual) address	The address generated by a core after the segment is applied.
Link	Generic term that refers to a refer to PCIe® link.
LINT	Local interrupt.

Table 4: Definitions

Term	Definition
Logical address	The address generated by a core before the segment is applied.
LVT	Local vector table. A collection of APIC registers that define interrupts for local events. E.g., APIC[530:500] [Extended Interrupt [3:0] Local Vector Table] .
Master abort	This is a PCI-defined term that is applied to transactions on other than PCI buses. It indicates that the transaction is terminated without affecting the intended target; reads return all 1's; writes are discarded; the master abort error code is returned in the response, if applicable; master abort error bits are set if applicable.
MB	Megabyte; 1024 KB.
MCT	Memory controller. See 2.8 [Northbridge (NB)] .
MCQ	Memory controller queue. See 2.8 [Northbridge (NB)] .
Micro-op	Micro-op. Instructions have variable-length encoding and many perform multiple primitive operations. The processor does not execute these complex instructions directly, but, instead, decodes them internally into simpler fixed-length instructions called macro-ops. Processor schedulers subsequently break down macro-ops into sequences of even simpler instructions called micro-ops, each of which specifies a single primitive operation. See <i>Software Optimization Guide for AMD Family 16h Processors</i> .
MEMCLK	Refers to the clock signals, M[B, A][3:0]_CLK, that are driven from the processor to DDR DIMMs.
MMIO	Memory-mapped input-output range. This is physical address space that is mapped to the IO functions such as the IO links or MMIO configuration. The IO link MMIO ranges are specified by D18F1x[2CC:2A0,1CC:180,BC:80] [MMIO Base/Limit] .
MMIO configuration	Access to configuration space through memory space. See 2.7 [Configuration Space] .
MSR	Model-specific register. The core includes several MSRs for general configuration and control. See 3.19 [MSRs - MSR0000_xxxx] for the beginning of the MSR register definitions.
MTRR	Memory-type range register. The MTRRs specify the type of memory associated with various memory ranges. See MSR0000_00FE , MSR0000_020[F:0] , MSR0000_02[6F:68,59:58,50] , and MSR0000_02FF .
NB	Northbridge. The transaction routing block of the node. See 2.1 [Processor Overview] .
NBC	NBC = (CPUID Fn0000_0001_EBX[LocalApicId[3:0]]==0). Node Base Core. The lowest numbered core in the node.
NBPMC	Performance monitor counter. See 2.6.1.3 [NB Performance Monitor Counters] .
NCLK	The main northbridge clock. The NCLK frequency is the NB COF.
Node	See 2.1 [Processor Overview] .
Normalized address	Addresses used by DCTs. See 2.8 [Northbridge (NB)] .
OW	Octword. An 128-bit value.
ODM	On-DIMM mirroring. See D18F2x[5C:40]_dct[0][OnDimmMirror] .
ODT	On-die termination, which is applied DRAM interface signals.
ODTS	DRAM On-die thermal sensor.
Operational frequency	The frequency at which the processor operates. See 2.5 [Power Management] .

Table 4: Definitions

Term	Definition
PCIe®	PCI Express®.
PDS	Product data sheet.
Physical address	Addresses used by cores in transactions sent to the NB.
PMC	Performance monitor counter. See 2.6.1.1 [Core Performance Monitor Counters] .
PRBS	Pseudo-random bit sequence.
Processor	See 2.1 [Processor Overview] .
PSI	Power Status Indicator. See 2.5.1.3.1 [PSIx_L Bit] .
P-state	Performance state. See 2.5 [Power Management] .
PTE	Page table entry.
QW	Quadword. A 64-bit value.
RAS	Reliability, availability and serviceability (industry term). See 2.14.1 [Machine Check Architecture] .
RDQ	Read data queue.
REFCLK	Reference Clock, refers to the clock frequency (100 MHz) or the clock period (10 ns) depending on the context used.
RX	Receiver.
RevA0	RevA0 = ((D18F3xFC[BaseModel] == 0h) && (D18F3xFC[Stepping] == 0h))
RevA1	RevA1 = ((D18F3xFC[BaseModel] == 0h) && (D18F3xFC[Stepping] == 1h)).
Scrubber	Background memory checking logic. See 2.8.3 [Memory Scrubbers] .
Shutdown	A state in which the affected core waits for either INIT, RESET, or NMI. When shutdown state is entered, a shutdown special cycle is sent on the IO links.
Single-Plane	Refers to a processor or systemboard where VDD and VDDNB are tied together and operate at the same voltage level. Refer to 2.5.1 [Processor Power Planes And Voltage Control] .
Slam	Refers to changing the voltage to a new value in one step (as opposed to stepping). See 2.5.1.4.1 [Hardware-Initiated Voltage Transitions] .
SMAF	System management action field. This is the code passed from the SMC to the processors in STPCLK assertion messages. The action taken by the processors in response to this message is specified by D18F3x[84:80] [ACPI Power State Control] .
SMBus	System management bus. Refers to the protocol on which the serial VID interface (SVI) commands are based. See 2.5.1 [Processor Power Planes And Voltage Control] , and 1.2 [Reference Documents] .
SMC	System management controller. This is the platform device that communicates system management state information to the processor through an IO link, typically the system IO hub.
SMI	System management interrupt. See 2.4.8.2.1 [SMM Overview] .
SMM	System management mode. See 2.4.8.2 [System Management Mode (SMM)] .
Speculative event	A performance monitor event counter that counts all occurrences of the event even if the event occurs during speculative code execution.
SVI2	Serial VID 2.0 interface. See 2.5.1.1 [Serial VID Interface]
SVM	Secure virtual machine. See 2.4.9 [Secure Virtual Machine Mode (SVM)] .

Table 4: Definitions

Term	Definition
Sync flood	The propagation of continuous sync packets to all links. This is used to quickly stop the transmission of potentially bad data when there are no other means to do so. See the link specification for additional information.
TCC	Temperature calculation circuit. See 2.10 [Thermal Functions] .
Tctl	Processor temperature control value. See 2.10.3 [Temperature-Driven Logic] .
TDC	Thermal design current. See the AMD Infrastructure Roadmap, #41482.
TDP	Thermal design power. A power consumption parameter that is used in conjunction with thermal specifications to design appropriate cooling solutions for the processor. See 2.5.9.2 [TDP Limiting] .
Token	A scheduler entry used in various northbridge queues to track outstanding requests. See D18F3x140 [SRI to XCS Token Count] on Page 461.
TX	Transmitter.
UI	Unit interval. This is the amount of time equal to one half of a clock cycle.
UMI	Unified Media Interface. The link between the processor and the FCH.
VDD	Main power supply to the processor core logic.
VDDNB	Main power supply to the processor NB logic.
VID	Voltage level identifier. See 2.5.1 [Processor Power Planes And Voltage Control] .
Virtual CAS	The clock in which CAS is asserted for the burst, N, plus the burst length (in MEMCLKs), minus 1; so the last clock of virtual CAS = N + (BL/2) - 1.
VRM	Voltage regulator module.
W	Word. A 16-bit value.
Warm reset	RESET_L is asserted only (while PWROK stays high). See 2.3 [Processor Initialization] .
WDT	Watchdog timer. A timer that detects activity and triggers an error if a specified period of time expires without the activity. For example, see MSRC001_0074 [CPU Watchdog Timer (Cpu-WdtCfg)] or the NB watchdog timer in D18F3x40 [MCA NB Control] .
WDQ	Write data queue.
XBAR	Cross bar; command packet switch. See 2.8 [Northbridge (NB)] .

1.5 Changes Between Revisions and Product Variations

1.5.1 Revision Conventions

The processor revision is specified by [CPUID Fn0000_0001_EAX \[Family, Model, Stepping Identifiers\]](#) or [CPUID Fn8000_0001_EAX \[Family, Model, Stepping Identifiers\]](#). This document uses a revision letter instead of specific model numbers. The following table contains the definitions based on model and stepping used in this document. Where applicable, the processor stepping is indicated after the revision letter. All behavior marked with a revision letter apply to future revisions unless they are superseded by a change in a later revision. See the revision guide for additional information about revision determination. See [1.2 \[Reference Documents\]](#).

Table 5: Processor revision conventions

Term	Definition
PROC	Processor. PROC = {CPUID Fn0000_0001_EAX[ExtFamily], {CPUID Fn0000_0001_EAX[ExtModel], CPUID Fn0000_0001_EAX[BaseModel]}, CPUID Fn0000_0001_EAX[Stepping]}.
KB_A1	KB_A1 = {07h,00h,1h}.

1.5.2 Major Changes

This section describes the major changes relative to Family 14h Models 00h-0Fh (ON) Processors.

- CPU core (JG) changes, with respect to BT:
 - Architectural changes:
 - Shared L2 Cache.
 - MSRC001_023[6,4,2,0], MSRC001_023[7,5,3,1] L2I Performance counters indicated by CPUID Fn8000_0001(ECX[PerfCtrExtL2I].
 - MSRC001_024[6,4,2,0], MSRC001_024[7,5,3,1]: NB Performance counters indicated by CPUID Fn8000_0001(ECX[PerfCtrExtNB].
 - CPUID Fn8000_0008_EAX[PhysAddrSize]: Physical Address Extended to 40 bits.
 - CPUID Fn8000_0001(ECX[DataBreakpointExtension]: Debug Breakpoint Extension.
 - Instruction set changes:
 - CPUID Fn0000_0001(ECX[AVX]: Added AVX instruction support.
 - CPUID Fn0000_0001(ECX[XSAVE,OSXSAVE]: CPUID Fn0000_000D: Added XSAVE support.
 - CPUID Fn0000_0001(ECX[AES]: Added AES instruction support.
 - CPUID Fn0000_0001(ECX[SSE41, SSE42]: Added SSE4.1 and SSE4.2 instruction support.
 - CPUID Fn0000_0001(ECX[PCLMULQDQ]: Added PCLMULQDQ instruction support.
 - CPUID Fn0000_000D_EAX_x0-CPUID Fn0000_000D_EDX_x2: Added XSAVE/XRSTOR.
 - CPUID Fn0000_0001(ECX[MOVBE]: Added MOVBE instruction support.
 - CPUID Fn0000_0001(ECX[F16C]: Added F16C instruction support.
 - CPUID Fn0000_0007_EBX_x0[BMI1]: Added BMI1 instruction support.
 - Virtualization Support
 - CPUID Fn8000_000A_EDX[TscRateMsr]: Added TSC Scaling.
 - CPUID Fn8000_000A_EDX[FlushByAsid]: Added Flush by ASID.
 - CPUID Fn8000_000A_EDX[DecodeAssists]: Added Decode Assist.
 - CPUID Fn8000_000A_EDX[PauseFilterThreshold]: Added Enhanced Pause Filter.

1.5.2.1 Major Changes to Core/NB Performance Counters

Major Changes to Core/NB Performance Counters:

PerfMon Changes: Added L2I PerfMon group. See MSRC001_023[6,4,2,0] and MSRC001_023[7,5,3,1].

2 Functional Description

2.1 Processor Overview

The *processor* is defined as follows:

- The processor is a package that contains one node.
- Supports x86-based instruction sets.
- Packages:

- FT3: Notebook BGA Package.
- FS1b: Desktop uPGA Package.
- See [CPUID Fn8000_0001_EBX\[PkgType\]](#).
- L2 complex

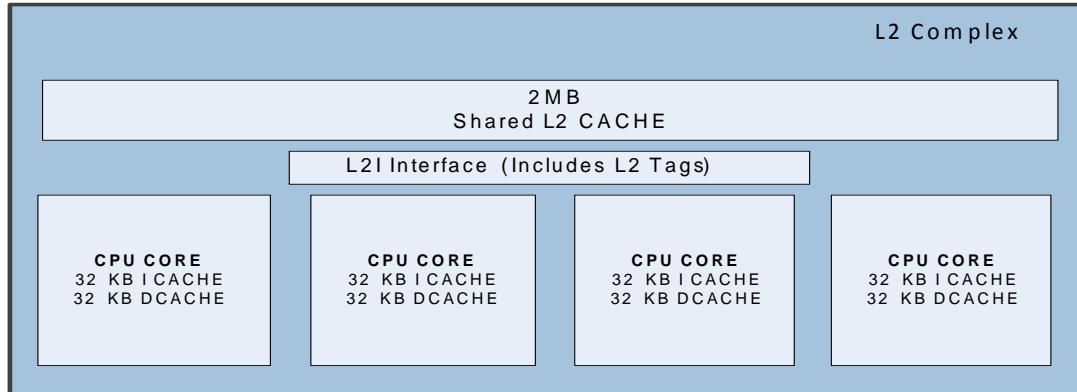


Figure 1: A L2 Complex

- 1 L2 complex (4 cores)
- 2 MB L2
- See [2.4.1 \[L2 complex\]](#).
- DRAM:
 - One 64-bit DDR3 memory channel (A). See [Figure 16 \[System Diagram\]](#).
- Northbridge (UNB):
 - One communication packet routing block referred to as the northbridge (NB). The NB routes transactions between the cores, the link, and the DRAM interfaces. It includes the configuration register space for the device.
- Graphics northbridge/GNB:
 - Link:
 - PCIe® Gen2
 - One x4 Gfx link, four x1 GPP links.
 - See [2.11.3 \[Links\]](#).
- Power Management:
 - See [2.5 \[Power Management\]](#).
- RAS:
 - See [2.14 \[RAS Features\]](#).

2.2 System Overview

2.3 Processor Initialization

This section describes the initialization sequence after a cold reset ([2.6.1 \[Cold Boot Sequence \(S4/S5 to S0\)\]](#)).

Core 0 of the processor, the bootstrap core (BSC), begins executing code from the reset vector. The remaining cores do not fetch code until their enable bits are set ([D18F0x1DC\[CpuEn\]](#)).

2.3.1 BSC Initialization

The BSC must perform the following tasks as part of boot.

- Store BIST information from the EAX register into an unused processor register.
- D18F0x6C[InitDet] may be used by BIOS to differentiate between INIT and cold/warm reset.
- Determine type of startup using D18F0x6C[ColdRstDet].
 - If this is a warm reset then BIOS may check for valid MCA errors and if present save the status for later use. See 2.14.1.6 [Handling Machine Check Exceptions].
- Enable the cache, program the MTRRs for CAR and initialize CAR. See 2.3.3 [Using L2 Cache as General Storage During Boot].
- Setup the SMU.
- Setup of APIC (2.4.8.1.3 [ApicId Enumeration Requirements]).
- Setup the link configuration 2.11.3.2 [Link Configurations].
- Setup the root complex and initialize the I/O links 2.11.4.3 [Link Configuration and Initialization].
- If required, reallocate data and flow control buffers of the links (see D18F0x[F0,D0,B0,90] [Link Base Channel Buffer Count] and D18F0x[F4,D4,B4,94] [Link Isochronous Channel Buffer Count]).
- Issue system warm reset. See 2.6.2 [Warm Reset Sequence].
- Configure the DRAM controllers.
- Configure processor power management. See 2.5 [Power Management].
- Allow other cores to begin fetching instructions by setting D18F0x1DC[CpuEn] in the PCI configuration space of all nodes. See 2.4.4 [Processor Cores and Downcoring].

2.3.2 AP Initialization

All other processor cores other than core 0 begin executing code from the reset vector. They must perform the following tasks as part of boot.

- Store BIST information from the eax register into an unused processor register.
- D18F0x6C[InitDet] may be used by BIOS to differentiate between INIT and cold/warm reset.
- Determine the history of this reset using the D18F0x6C [Link Initialization Control] [ColdRstDet] bit:
 - If this is a warm reset then BIOS may check for valid MCA errors and if present save the status for use later. See 2.14.1.6 [Handling Machine Check Exceptions].
- Set up the local APIC. See 2.4.8.1.3 [ApicId Enumeration Requirements].
- Configure processor power management. See 2.4 [Core].

2.3.3 Using L2 Cache as General Storage During Boot

Prior to initializing the DRAM controller for system memory, BIOS may use the L2 cache as general storage. If BIOS is not using L2 cache as general storage during boot, program MSRC001_102A[CLILinesToL2Dis]=0.

The L2 cache as general storage is described as follows:

- Each L2 complex has its own L2 cache.
- BIOS manages the mapping of the L2 storage such that cacheable accesses do not cause L2 victims.
- The L2 size, L2 associativity, and L2 line size is determined by reading CPUID Fn8000_0006(ECX)[L2Size, L2Assoc, L2LineSize]. L2WayNum is defined to be the number of ways indicated by the L2Assoc code.
 - The L2 cache is viewed as (L2Size/L2LineSize) cache lines of storage, organized as L2WayNum ways, each way being (L2Size/L2WayNum) in size.
 - E.g. L2Assoc=8 so L2WayNum=16 (there are 16 ways). If (L2Size=2MB) then there are 16 blocks of cache, each 2MB/16 in size, or 128KB each.

- For each of the following values of L2Size, the following values are defined:
 - L2Size=1 MB: L2Tag=PhysAddr[39:16], L2WayIndex=PhysAddr[15:6].
 - L2Size=2 MB: L2Tag=PhysAddr[39:17], L2WayIndex=PhysAddr[16:6].
- PhysAddr[5:0] addresses the L2LineSize number of bytes of storage associated with the cache line.
- The L2 cache, when allocating a line at L2WayIndex:
 - Picks an invalid way before picking a valid way.
 - Prioritizes the picking of invalid ways such that way 0 is the highest priority and L2WayNum-1 is the lowest priority.
- It is recommended that BIOS assume a simpler allocation of L2 cache memory, being L2WayNum size-aligned blocks of memory, each being L2Size/L2WayNum bytes.
- BIOS can rely on a minimum L2Size of 1 MB and can rely on being able to use all 16 ways for general storage. See [CPUID Fn8000_0006_ECX\[L2Size\]](#).

The following memory types are supported:

- WP-IO: BIOS ROM may be assigned the write-protect IO memory type and may be accessed read-only as data and fetched as instructions.
 - WP-IO accesses, both read and write, do not get allocated into the L2 and therefore do not need to be considered for allocation into the L2.
- WB-DRAM: General storage may be assigned the write-back DRAM memory type and may be accessed as read-write data, but not accessed by instruction fetch.
 - BIOS initializes an L2LineSize sized and aligned location in the L2 cache, mapped as write-back DRAM, with 1 read to at least 1 byte of the L2LineSize sized and aligned WB-DRAM address. BIOS may store to a line only after it has been allocated by a load.
 - Fills, sent to the disabled memory controller, return undefined data.
- All of memory space that is not accessed as WP-IO or WB-DRAM space must be marked as UC memory type.
- In order to prevent victimizing L2 data, no more than L2WayNum cache lines accessed as WB-DRAM may have the same L2WayIndex.
 - Software does not need to know which ways the L2WayNum lines are allocated to for any given value of L2WayIndex, only that invalid ways will be selected for allocation before valid ways will be selected for allocation.
 - Software is not allowed to deallocate a line in the L2 by using CLFLUSH.

Performance monitor event [L2IPMCx060](#)[3:2], titled “write victim block”, can be used to indicate whether L2 dirty data was lost by being victimized and sent to the disabled memory controller.

The following requirements must be satisfied prior to using the cache as general storage:

- Paging must be disabled. Reason: The caching of TLB entries will displace L2 cache entries.
- [MSRC001_0015](#)[INVDBINVD]=0. Reason: INVD's must be prevented from pushing dirty data to uninitialized DRAM.
- [MSRC001_1021](#)[DisSpecTlbRld]=1. Disable speculative ITLB reloads. Reason: Prevent misinterpreted speculative IFetch from accessing WB-DRAM dirty lines as code and evicting them from the L2.
- [MSRC001_1022](#)[DisSpecTlbWalk]=1. Disable speculative DTLB reloads. Reason: BIOS has been known to map more memory as WB-DRAM than the size of the L2. Setting this bit will prevent mispredicted speculative data accesses from accessing a region outside of the [CAR](#) region that may be mapped as WB-DRAM and cause an L2 eviction.
- [MSRC001_1022](#)[DisHwPf]=1.
- [MSRC001_10A0](#)[L2RinserDis]=1. Reason: Disable background removal of stored data.
- [MSRC001_10A0](#)[PrefetcherDis]=1. Disable L2 hardware prefetcher.
- [MSRC001_10A0](#)[CacheIcAttrDis]=1. Reason: If there is data access to an instruction line whose attri-

butes were written into that the L2 cache, we would get an L2 eviction so the line could be reloaded from the NB with ECC.

- CLFLUSH, INVD, and WBINVD must not be used during **CAR** but may be used when tearing down **CAR** for all compute units on a node. Reason: In order to ensure that data L2 data for a compute unit is not evicted when another compute unit completes use of **CAR**.
- The BIOS must not use SSE, or MMX™ instructions, with the exception of the following list: MOVD, MOVQ, MOVDQA, MOVQ2DQ, MOVDQ2Q.
- The BIOS must not enable exceptions, page-faults, and other interrupts.
- BIOS must not use software prefetches.
- UC-DRAM: All of DRAM that is not accessed as WB-DRAM space must be marked as UC memory type. Reason: This prevents speculative accesses that fall outside of the **CAR** region from getting to the caches and DRAM controller.

When BIOS has completed using the cache for general storage the following steps are followed:

1. Prior to issuing an INVD instruction, BIOS must ensure that no other source of coherent traffic, such as a DMA engine, is operating in the system. This condition must hold true until the INVD instruction for tear-down has been executed on all CPUs.
2. An INVD instruction is executed on each core that used cache as general storage; an INVD is issued when all cores on all nodes have completed using the cache for general storage.
3. If DRAM is initialized and there is data in the cache that needs to get moved to main memory, CLFLUSH or WBINVD may be used instead of INVD, but software must ensure that needed data in main memory is not overwritten.
4. Program the following configuration state (Order is unimportant):
 - **MSRC001_0015**[INVDBINVD]=1.
 - **MSRC001_1021**[DisSpecTlbRld]=0.
 - **MSRC001_1022**[DisSpecTlbWalk]=0.
 - **MSRC001_1022**[DisHwPf]=0.
 - **MSRC001_10A0**[PrefetcherDis]=0.
 - **MSRC001_10A0**[CacheIcAttrDis]=0.
 - **MSRC001_102A**[CLILinesToL2Dis]=0.

2.3.4 Instruction Cache Configuration Register Usage Requirements

Modification of **MSRC001_1021** [Instruction Cache Configuration (IC_CFG)] requires the following steps for all cores within the L2 complex:

- Synchronize all cores.
- Modify **MSRC001_1021** observing the **Same-for-all** requirement.
- Flush all caches using WBINVD for all cores within the L2 complex.
- Resume all cores.

2.4 Core

The majority of the behavioral definition of the core is specified in the AMD64 Architecture Programmer's Manual. See [1.2 \[Reference Documents\]](#).

2.4.1 L2 complex

Each *L2 complex* or cluster includes 4 cores each having an x86 instruction execution logic and first-level (L1) data cache and first-level (L1) instruction cache. The second level (L2) general-purpose cache is shared between all cores of the L2 complex.

There is a set of MSRs and APIC registers associated with each core. Processors that include multiple cores are

said to incorporate *chip multi-processing* or CMP. Unless otherwise specified the processor configuration interface hides the L2 complex implementation and presents software with homogenous cores, each independent of the other.

Software may use [D18F5x80](#)[Enabled, DualCore, TripleCore, QuadCore] in order to associate a core with a L2 complex. This information can be useful because some configuration settings are determined based on active L2 complexes and core performance may vary based on resource sharing within a L2 complex.

2.4.2 Caches and TLBs

Cache and TLB storage available to a core is reported by:

- CPUID Fn8000_0005_EAX-CPUID Fn8000_0006_EDX.
- CPUID Fn8000_0019_EAX-CPUID Fn8000_0019_E[D,C]X.
- CPUID Fn8000_001D_EAX_x0-CPUID Fn8000_001E_EDX.

Cache and TLB storage available to a core is summarized as follows:

- L1 and L2 Caches:
 - DC: 32 KB, 8-way, write-back, per-core.
 - IC: 32 KB, 2-way, per-core.
 - L2: 1 MB or 2 MB (Product-specific), 16-way associative, shared between all cores of a L2 complex.
- TLBs:
 - D, L1TLB:
 - 4 KB: 40 entries, fully associative.
 - 2 MB: 8 entries, fully associative.
 - D, L2TLB:
 - 4 KB: 512 entries, 4 way associative
 - 2 MB: 256 entries, hashed 2 way associative.
 - I, L1TLB:
 - 4 KB: 32 entries, fully associative.
 - 2 MB, 8 entries, fully associative.
 - I, L2TLB:
 - 4 KB: 512 entries, 4-way associative.

2.4.2.1 Registers Shared by Cores in a L2 complex

Some registers are implemented one instance per L2 complex instead of per core; these registers are designated as [Per-L2](#). The absence of [Per-L2](#) implies the normal per-core instance programming model.

Programming rules for [Per-L2](#) registers:

- Software must ensure that a shared MSR written by one core on a L2 complex will not cause a problem for software that is running on the other core of the L2 complex.
- [Per-L2](#): A write to a [Per-L2](#) MSR does not have to be written to the other cores of the L2 complex in order for the other cores to see the updated value.
- A read-modify-write of a shared MSR register is not atomic. Software must ensure atomicity between the cores that could simultaneously read-modify-write the shared register.

2.4.3 Virtual Address Space

The processor supports 48 address bits of virtual memory space (256 TB) as indicated by [CPUID Fn8000_0008_EAX](#).

2.4.4 Processor Cores and Downcoring

Each L2 Complex supports downcoring as follows:

- The number of fuse enabled cores supported is specified by D18F5x84[CmpCap].
- The cores of a L2 complex may be software downcored by D18F3x190[DisCore]. See 2.4.4.1 [Software Downcoring using D18F3x190[DisCore]].
 - Clocks are turned off and power is gated to software or fuse downcored L2 complexes. The power savings is the same as CC6.
 - There must be at least 1 L2 complex enabled.
 - D18F3x190[DisCore] affects the value of CPUID Fn0000_0001_EBX[LogicalProcessorCount], CPUID Fn0000_0001_EDX[HTT], CPUID Fn8000_0001_ECX[CmpLegacy], CPUID Fn8000_0008_ECX[NC], D18F3x12C[CpuNum], D18F5x80[Enabled, DualCore, TripleCore, QuadCore]. D18F3x190[DisCore] does not affect the value of D18F5x84[CmpCap].
- An implemented (physical) core that is downcored is not visible to software. Cores that are not downcored are numbered logically in a contiguous manner. The physical to logical mapping is described as follows:
- D18F5x80 [Compute Unit Status 1] reports core topology information to software.
- The number of cores specified in CPUID Fn8000_0008_ECX[NC] must be the same as the number of cores enabled in D18F0x1DC[CpuEn].
- The core number, CpuCoreNum, is provided to SW running on each core through CPUID Fn0000_0001_EBX[LocalApicId] and APIC20[ApicId]; CpuCoreNum also affects D18F0x1DC[CpuEn]. CpuCoreNum, varies as the lowest integers from 0 to D18F5x84[CmpCap], based on the number of enabled cores; e.g., a 4-core node with 1 core disabled results in cores reporting CpuCoreNum values of 0, 1, and 2 regardless of which core is disabled. The boot core is always the core reporting CpuCoreNum=0.

Some legacy operating systems do not support processors with a non-power-of-2 number of cores. The BIOS is recommended to support a user configurable option to disable cores down to a power-of-2 number of cores for legacy operating system support.

2.4.4.1 Software Downcoring using D18F3x190[DisCore]

Cores may be downcored by D18F3x190[DisCore].

Software is required to use D18F3x190[DisCore] as follows:

- Setting bits corresponding to cores that are not present results in undefined behavior.
- Once a core has been removed by D18F3x190[DisCore]=1, it cannot be added back without a cold reset. E.g. Software may only set DisCore bits, never clear them.
- For enabled L2 complexes where (L2 complex>=1) software may not disable logical Core 0 of the L2 complex.
- The most significant bit N, affected by Fuse[CoreDis], is (the number of cores)-1 at cold reset; the number of cores at cold reset is (CPUID Fn8000_0008_ECX[NC]+1).
- The most significant bit N and the logical core ID significance of DisCore is not affected by the value of DisCore followed by a warm-reset.
 - E.g. If logical core 2 is disabled by DisCore[3:0]=0100b followed by a warm reset, then the new logical core 2 is the old logical core 3. If the new logical core 2 needs to then be disabled then DisCore[3:0]=1100b followed by a warm reset.
- All bits greater than bit N are reserved. Bits greater than N associated with a fuse disabled core are read-write. Bits greater than N associated with a non-existent core are read-only.
- If D18F3x190[DisCore] is changed, then the following need to be updated:
 - D18F0x60[CpuCnt[4:0]].
 - D18F5x170[NbPstateThreshold]

2.4.5 Physical Address Space

The processor supports a 40 bit physical address space, as indicated by [CPUID Fn8000_0008_EAX \[Long Mode Address Size Identifiers\]](#).

The processor master aborts the following upper-address transactions (to address PhysAddr):

- Link or core requests with non-zero PhysAddr[63:40].

2.4.6 System Address Map

The processor defines a reserved memory address region starting at 0000_00FD_0000_0000h and extending up to 0000_0100_0000_0000h. System software must not map memory into this region. Downstream host accesses to the reserved address region results in a page fault. Upstream system device accesses to the reserved address region results in an undefined operation.

2.4.6.1 Memory Access to the Physical Address Space

All memory accesses to the physical address space from a core are sent to its associated northbridge (NB). All memory accesses from a link are routed through the NB. An IO link access to physical address space indicates to the NB the cache attribute (Coherent or Non-coherent, based on bit[0] of the Sized Read and Write commands).

A core access to physical address space has two important attributes that must be determined before issuing the access to the NB: the memory type (e.g., WB, WC, UC; as described in the MTRRs) and the access destination (DRAM or MMIO).

This mechanism is managed by the BIOS and does not require any setup or changes by system software.

2.4.6.1.1 Determining Memory Type

The memory type for a core access is determined by the highest priority of the following ranges that the access falls in: 1==Lowest priority.

1. The memory type as determined by architectural mechanisms.
 - See the APM2 chapter titled “Memory System”, sections “Memory-Type Range Registers” and “Page-Attribute Table Mechanism”.
 - See the APM2 chapter titled “Nested Paging”, section “Combining Memory Types, MTRRs”.
 - See [MSR0000_02FF \[MTRR Default Memory Type \(MTRRdefType\)\]](#), [MSR0000_020\[F:0\] \[Variable-Size MTRRs Base/Mask\]](#), [MSR0000_02\[6F:68,59:58,50\] \[Fixed-Size MTRRs\]](#).
2. TSeg & ASeg SMM mechanism. (see [MSRC001_0112](#) and [MSRC001_0113](#))
3. CR0[CD]: If (CR0[CD]==1) then MemType=CD.
4. MMIO config space, APIC space.
 - MMIO APIC space and MMIO config space must not overlap.
 - MemType=UC.
 - See [2.4.8.1.2 \[APIC Register Space\]](#) and [2.7 \[Configuration Space\]](#).
5. SmmATValNoMchFrcCD: If (“In SMM Mode” && ([MSRC001_102A\[SmmATValNoMchFrcCD-Dis\]==0](#)) && ~(([MSRC001_0113\[AValid\]](#) && “The address falls within the ASeg region”) || ([MSRC001_0113\[TValid\]](#) && “The address falls within the TSeg region”))) then MemType=CD.

2.4.6.1.2 Determining The Access Destination for Core Accesses

The access destination, DRAM or MMIO, is based on the highest priority of the following ranges that the access falls in: 1==Lowest priority.

1. RdDram/WrDram as determined by [MSRC001_001A \[Top Of Memory \(TOP_MEM\)\]](#) and [MSRC001_001D \[Top Of Memory 2 \(TOM2\)\]](#).
2. The IORRs. (see [MSRC001_00\[18,16\]](#) and [MSRC001_00\[19,17\]](#)).
3. The fixed MTRRs. (see [MSR0000_02\[6F:68,59:58,50\] \[Fixed-Size MTRRs\]](#))
4. TSeg & ASeg SMM mechanism. (see [MSRC001_0112](#) and [MSRC001_0113](#))
5. MMIO config space, APIC space.
 - MMIO APIC space and MMIO config space must not overlap.
 - RdDram=IO, WrDram=IO.
 - See [2.4.8.1.2 \[APIC Register Space\]](#) and [2.7 \[Configuration Space\]](#).
6. NB address space routing. See [2.8.2.1.1 \[DRAM and MMIO Memory Space\]](#).

2.4.7 Timers

Each core includes the following timers. These timers do not vary in frequency regardless of the current P-state or C-state.

- [MSR0000_0010 \[Time Stamp Counter \(TSC\)\]](#); the TSC increments at the rate specified by the P0 P-state.
 - See [2.5.3.1.1.1 \[Software P-state Numbering\]](#).
 - See [MSRC001_00\[6B:64\] \[P-state \[7:0\]\]](#).
- The APIC timer (APIC380 and [APIC390](#)), which increments at the rate of 2xCLKIN; the APIC timer may increment in units of between 1 and 8.

2.4.8 Interrupts

2.4.8.1 Local APIC

The local APIC contains logic to receive interrupts from a variety of sources and to send interrupts to other local APICs, as well as registers to control its behavior and report status. Interrupts can be received from:

- IO devices including the IO hub (IO APICs)
- Other local APICs (inter-processor interrupts)
- APIC timer
- Thermal events
- Performance counters
- Legacy local interrupts from the IO hub (INTR and NMI)
- APIC internal errors

The APIC timer, thermal events, performance counters, local interrupts, and internal errors are all considered local interrupt sources, and their routing is controlled by local vector table entries. These entries assign a message type and vector to each interrupt, allow them to be masked, and track the status of the interrupt.

IO and inter-processor interrupts have their message type and vector assigned at the source and are unaltered by the local APIC. They carry a destination field and a mode bit that together determine which local APIC(s) accepts them. The destination mode (DM) bit specifies if the interrupt request packet should be handled in physical or logical destination mode. If the destination field matches the broadcast value specified by [D18F0x68\[ApicExtBrdCst\]](#), then the interrupt is a broadcast interrupt and is accepted by all local APICs regardless of destination mode.

2.4.8.1.1 Detecting and Enabling

APIC is detected and enabled via [CPUID Fn0000_0001_EDX\[APIC\]](#).

The local APIC is enabled via [MSR0000_001B\[ApicEn\]](#). Reset forces APIC disabled.

2.4.8.1.2 APIC Register Space

MMIO APIC space:

- Memory mapped to a 4 KB range. The memory type of this space is the UC memory type; also, hardware forces the 4 KB page mapped by ApicBar to UC. The base address of this range is specified by [{MSR0000_001B\[ApicBar\[47:12\]\], 000h}](#).
- The mnemonic is defined to be APICXX; XX is the byte address offset from the base address.
- MMIO APIC registers in xAPIC mode is defined by the register from [APIC20](#) to [APIC\[530:500\]](#).
- Treated as normal memory space when APIC is disabled, as specified by [MSR0000_001B\[ApicEn\]](#).

2.4.8.1.3 ApicId Enumeration Requirements

System hardware and BIOS must ensure that the number of cores per processor (NC) exposed to the operating system by all tables, registers, and instructions across all cores in the processor is identical. See [2.4.10.1 \[Multi-Core Support\]](#) to derive NC.

Operating systems are expected to use [CPUID Fn8000_0008_ECX\[ApicIdCoreIdSize\]](#), the number of least significant bits in the Initial APIC ID that indicate core ID within a processor, in constructing per-core CPUID masks. (ApicIdCoreIdSize[3:0] determines the maximum number of cores (MNC) that the processor could theoretically support, not the actual number of cores that are actually implemented or enabled on the processor, as indicated by CPUID Fn8000_0008_ECX[NC].) MNC = $(2^{\text{ApicIdCoreIdSize}})$. BIOS must use the ApicId MNC rule when assigning [APIC20\[ApicId\]](#) values as described below.

ApicId MNC rule: The ApicId of core j on processor i must be enumerated/assigned as:

- $\text{ApicId}[\text{proc}=i, \text{core}=j] = (\text{OFFSET_IDX} + i) * \text{MNC} + j$
- Where OFFSET_IDX is an integer offset (0 to N) used to shift up the core ApicId values to allow room for IOAPIC devices.

It is recommended that BIOS use the following APIC ID assignments for the broadest operating system support. Given N = (Number_Of_Processors * MNC) and M = Number_Of_IOAPICS:

- If $(N+M) < 16$, then assign the local (core) ApicIds first from 0 to N-1, and the IOAPIC IDs from N to N+(M-1). APIC ID 15 is reserved for broadcast when [APIC410\[ExtApicIdEn\]==0](#).
- If $(N+M) \geq 16$, then assign the IOAPIC IDs first from 0 to M-1, and the local (core) ApicIds from K to K+(N-1), where K is an integer multiple of MNC greater than M-1.

2.4.8.1.4 Physical Destination Mode

The interrupt is only accepted by the local APIC whose [APIC20\[ApicId\]](#) matches the destination field of the interrupt. Physical mode allows up to 255 APICs to be addressed individually.

2.4.8.1.5 Logical Destination Mode

A local APIC accepts interrupts selected by [APICD0 \[Logical Destination \(LDR\)\]](#) and the destination field of the interrupt using either cluster or flat format as configured by [APICE0\[Format\]](#).

If flat destinations are in use, bits 7-0 of [APICD0\[Destination\]](#) are checked against bits 7-0 of the arriving interrupt's destination field. If any bit position is set in both fields, the local APIC is a valid destination. Flat format allows up to 8 APICs to be addressed individually.

If cluster destinations are in use, bits 7-4 of [APICD0\[Destination\]](#) are checked against bits 7-4 of the arriving

interrupt's destination field to identify the cluster. If all of bits 7-4 match, then bits 3-0 of [APICD0\[Destination\]](#) and the interrupt destination are checked for any bit positions that are set in both fields to identify processors within the cluster. If both conditions are met, the local APIC is a valid destination. Cluster format allows 15 clusters of 4 APICs each to be addressed.

2.4.8.1.6 Interrupt Delivery

SMI, NMI, INIT, Startup, and External interrupts are classified as non-vectored interrupts.

When an APIC accepts a non-vectored interrupt, it is handled directly by the processor instead of being queued in the APIC. When an APIC accepts a fixed or lowest-priority interrupt, it sets the bit in [APIC\[270:200\] \[Interrupt Request \(IRR\)\]](#) corresponding to the vector in the interrupt. For local interrupt sources, this comes from the vector field in that interrupt's local vector table entry. The corresponding bit in [APIC\[1F0:180\] \[Trigger Mode \(TMR\)\]](#) is set if the interrupt is level-triggered and cleared if edge-triggered. If a subsequent interrupt with the same vector arrives when the corresponding bit in [APIC\[270:200\]\[RequestBits\]](#) is already set, the two interrupts are collapsed into one. Vectors 15-0 are reserved.

2.4.8.1.7 Vectored Interrupt Handling

[APIC80 \[Task Priority \(TPR\)\]](#) and [APICA0 \[Processor Priority \(PPR\)\]](#) each contain an 8-bit priority divided into a main priority (bits 7-4) and a priority sub-class (bits 3-0). The task priority is assigned by software to set a threshold priority at which the processor is interrupted.

The processor priority is calculated by comparing the main priority (bits 7-4) of [APIC80\[Priority\]](#) to bits 7-4 of the 8-bit encoded value of the highest bit set in [APIC\[170:100\] \[In-Service \(ISR\)\]](#). The processor priority is the higher of the two main priorities.

The processor priority is used to determine if any accepted interrupts (indicated by [APIC\[270:200\]\[RequestBits\]](#)) are high enough priority to be serviced by the processor. When the processor is ready to service an interrupt, the highest bit in [APIC\[270:200\]\[RequestBits\]](#) is cleared, and the corresponding bit is set in [APIC\[170:100\]\[InServiceBits\]](#).

When the processor has completed service for an interrupt, it performs a write to [APICB0 \[End of Interrupt\]](#), clearing the highest bit in [APIC\[170:100\]\[InServiceBits\]](#) and causing the next-highest interrupt to be serviced. If the corresponding bit in [APIC\[1F0:180\]\[TriggerModeBits\]](#) is set, a write to [APICB0](#) is performed on all APICs to complete service of the interrupt at the source.

2.4.8.1.8 Interrupt Masking

Interrupt masking is controlled by the [APIC410 \[Extended APIC Control\]](#). If [APIC410\[IerEn\]](#) is set, [APIC\[4F0:480\] \[Interrupt Enable\]](#) are used to mask interrupts. Any bit in [APIC\[4F0:480\]\[InterruptEnableBits\]](#) that is clear indicates the corresponding interrupt is masked. A masked interrupt is not serviced and the corresponding bit in [APIC\[270:200\]\[RequestBits\]](#) remains set.

2.4.8.1.9 Spurious Interrupts

In the event that the task priority is set to or above the level of the interrupt to be serviced, the local APIC delivers a spurious interrupt vector to the processor, as specified by [APICF0 \[Spurious-Interrupt Vector \(SVR\)\]](#). [APIC\[170:100\]](#) is not changed and no write to [APICB0](#) occurs.

2.4.8.1.10 Spurious Interrupts Caused by Timer Tick Interrupt

A typical interrupt is asserted until it is serviced. An interrupt is deasserted when software clears the interrupt status bit within the interrupt service routine. Timer tick interrupt is an exception, since it is deasserted regardless of whether it is serviced or not.

The processor is not always able to service interrupts immediately (i.e. when interrupts are masked by clearing EFLAGS.IM or when the processor is in PDM).

If the processor is not able to service the timer tick interrupt for an extended period of time, the INTR caused by the first timer tick interrupt asserted during that time is delivered to the local APIC in ExtInt mode and latched, and the subsequent timer tick interrupts are lost. The following cases are possible when the processor is ready to service interrupts:

- An ExtInt interrupt is pending, and INTR is asserted. This results in timer tick interrupt servicing. This occurs 50 percent of the time.
- An ExtInt interrupt is pending, and INTR is deasserted. The processor sends the interrupt acknowledge cycle, but when the PIC receives it, INTR is deasserted, and the PIC sends a spurious interrupt vector. This occurs 50 percent of the time.

There is a 50 percent probability of spurious interrupts to the processor.

2.4.8.1.11 Lowest-Priority Interrupt Arbitration

Fixed, remote read, and non-vectored interrupts are accepted by their destination APICs without arbitration.

Delivery of lowest-priority interrupts requires all APICs to arbitrate to determine which one accepts the interrupt. If [APICF0](#)[FocusDisable] is clear, then the focus processor for an interrupt always accepts the interrupt. A processor is the focus of an interrupt if it is already servicing that interrupt (corresponding bit in [APIC\[170:100\]](#)[InServiceBits] is set) or if it already has a pending request for that interrupt (corresponding bit in [APIC\[270:200\]](#)[RequestBits] is set). If [APIC410](#)[IerEn] is set the interrupt must also be enabled in [APIC\[4F0:480\]](#)[InterruptEnableBits] for a processor to be the focus processor. If there is no focus processor for an interrupt, or focus processor checking is disabled, then each APIC calculates an arbitration priority value, stored in [APIC90](#) [[Arbitration Priority \(APR\)](#)], and the one with the lowest result accepts the interrupt.

The arbitration priority value is calculated by comparing [APIC80](#)[Priority] with the 8-bit encoded value of the highest bit set in [APIC\[270:200\]](#)[RequestBits] (IRRVec) and the 8-bit encoded value of the highest bit set [APIC\[170:100\]](#)[InServiceBits] (ISRVVec). If [APIC410](#)[IerEn] is set the IRRVec and ISRVVec are based off the highest enabled interrupt. The main priority bits 7-4 are compared as follows:

```

IF ((APIC80[Priority[7:4]] >= IRRVec[7:4]) && (APIC80[Priority[7:4]] > ISRVVec[7:4])) THEN
    APIC90[Priority] = APIC80[Priority]
ELSEIF (IRRVec[7:4] > ISRVVec[7:4]) THEN
    APIC90[Priority] = {IRRVec[7:4],0h}
ELSE
    APIC90[Priority] = {ISRVect[7:4],0h}
ENDIF.

```

2.4.8.1.12 Inter-Processor Interrupts

[APIC300](#) [[Interrupt Command Low \(ICR Low\)](#)] and [APIC310](#) [[Interrupt Command High \(ICR High\)](#)] provide a mechanism for generating interrupts in order to redirect an interrupt to another processor, originate an interrupt to another processor, or allow a processor to interrupt itself. A write to register [APIC300](#) causes an inter-

rupt to be generated with the properties specified by the [APIC300](#) and [APIC310](#) fields.

2.4.8.1.13 APIC Timer Operation

The local APIC contains a 32-bit timer, controlled by [APIC320 \[LVT Timer\]](#), [APIC380 \[Timer Initial Count\]](#), and [APIC3E0 \[Timer Divide Configuration\]](#). The processor bus clock is divided by the value in [APIC3E0\[Div\]](#) to obtain a time base for the timer. When [APIC380\[Count\]](#) is written, the value is copied into [APIC390 \[Timer Current Count\]](#). [APIC390\[Count\]](#) is decremented at the rate of the divided clock. When the count reaches 0, a timer interrupt is generated with the vector specified in [APIC320\[Vector\]](#). If [APIC320\[Mode\]](#) specifies periodic operation, [APIC390\[Count\]](#) is reloaded with the [APIC380\[Count\]](#) value, and it continues to decrement at the rate of the divided clock. If [APIC320\[Mask\]](#) is set, timer interrupts are not generated.

2.4.8.1.14 Generalized Local Vector Table

All LVTs ([APIC330](#) to [APIC3\[60:50\]](#), and [APIC\[530:500\]](#)) support a generalized message type as follows:

- 000b=Fixed
- 010b=SMI
- 100b=NMI
- 111b=ExtINT
- All other messages types are reserved.

2.4.8.1.15 State at Reset

At power-up or reset, the APIC is hardware disabled ([MSR0000_001B\[ApicEn\]=0](#)) so only SMI, NMI, INIT, and ExtInt interrupts may be accepted.

The APIC can be software disabled through [APICF0\[APICSWEn\]](#). The software disable has no effect when the APIC is hardware disabled.

When a processor accepts an INIT interrupt, the APIC is reset as at power-up, with the exception that:

- [APIC20\[ApicId\]](#) is unaffected.
- Pending APIC register writes complete.

2.4.8.2 System Management Mode (SMM)

System management mode (SMM) is typically used for system control activities such as power management. These activities are typically transparent to the operating system.

2.4.8.2.1 SMM Overview

SMM is entered by a core on the next instruction boundary after a system management interrupt (SMI) is received and recognized. A core may be programmed to broadcast a special cycle to the system, indicating that it is entering SMM mode. The core then saves its state into the SMM memory state save area and jumps to the SMI service routine (or SMI handler). The pointer to the SMI handler is specified by MSRs. The code and data for the SMI handler are stored in the SMM memory area, which may be isolated from the main memory accesses.

The core returns from SMM by executing the RSM instruction from the SMI handler. The core restores its state from the SMM state save area and resumes execution of the instruction following the point where it entered SMM. The core may be programmed to broadcast a special bus cycle to the system, indicating that it is exiting SMM mode.

2.4.8.2.2 Operating Mode and Default Register Values

The software environment after entering SMM has the following characteristics:

- Addressing and operation is in Real mode.
- A far jump, call or return in the SMI handler can only address the lower 1M of memory, unless the SMI handler first switches to protected mode.
- If [\(MSRC001_0111\[SmmBase\]>=0010_0000h\)](#) then:
 - The value of the CS selector is undefined upon SMM entry.
 - The undefined CS selector value should not be used as the target of a far jump, call, or return.
- 4-Gbyte segment limits.
- Default 16-bit operand, address, and stack sizes (instruction prefixes can override these defaults).
- Control transfers that do not override the default operand size truncate the EIP to 16 bits.
- Far jumps or calls cannot transfer control to a segment with a base address requiring more than 20 bits, as in Real mode segment-base addressing, unless a change is made into protected mode.
- A20M# is disabled. A20M# assertion or deassertion have no affect during SMM.
- Interrupt vectors use the Real mode interrupt vector table.
- The IF flag in EFLAGS is cleared (INTR is not recognized).
- The TF flag in EFLAGS is cleared.
- The NMI and INIT interrupts are masked.
- Debug register DR7 is cleared (debug traps are disabled).

The SMM base address is specified by [MSRC001_0111\[SmmBase\]](#). Important offsets to the base address pointer are:

- [MSRC001_0111\[SmmBase\] + 8000h](#): SMI handler entry point.
- [MSRC001_0111\[SmmBase\] + FE00h - FFFFh](#): SMM state save area.

2.4.8.2.3 SMI Sources And Delivery

The processor accepts SMIs as link-defined interrupt messages only. The core/node destination of these SMIs is a function of the destination field of these messages. However, the expectation is that all such SMI messages are specified to be delivered globally (to all cores of all nodes).

There are also several local events that can trigger SMIs. However, these local events do not generate SMIs directly. Each of them triggers a programmable IO cycle that is expected to target the SMI command port in the IO hub and trigger a global SMI interrupt message back to the coherent fabric.

Local sources of SMI events that generate the IO cycle specified in [MSRC001_0056 \[SMI Trigger IO Cycle\]](#) are:

- In the core, as specified by:
 - [MSRC001_0022 \[Machine Check Exception Redirection\]](#).
 - [MSRC001_00\[53:50\] \[IO Trap \(SMI_ON_IO_TRAP_\[3:0\]\)\]](#).
- All local APIC LVT registers programmed to generate SMIs.

The status for these is stored in [SMMFEC4](#).

2.4.8.2.4 SMM Initial State

After storing the save state, execution starts at [MSRC001_0111\[SmmBase\] + 08000h](#). The SMM initial state is specified in the following table.

Table 6: SMM Initial State

Register	SMM Initial State
CS	SmmBase[19:4]
DS	0000h
ES	0000h
FS	0000h
GS	0000h
SS	0000h
General-Purpose Registers	Unmodified (including CR2, CR3, CR8)
EFLAGS	0000_0002h
RIP	0000_0000_0000_8000h
CR0	Bits 0, 2, 3, and 31 cleared (PE, EM, TS, and PG); remainder is unmodified
CR4	0000_0000_0000_0000h
GDTR	Unmodified
LDTR	Unmodified
IDTR	Unmodified
TR	Unmodified
DR6	Unmodified
DR7	0000_0000_0000_0400h
EFER	All bits are cleared except bit 12 (SVME) which is unmodified.

2.4.8.2.5 SMM Save State

In the following table, the offset field provides the offset from the SMM base address specified by [MSRC001_0111 \[SMM Base Address \(SMM_BASE\)\]](#).

Table 7: SMM Save State

Offset	Size	Contents			Access
FE00h	Word	ES	Selector		Read-only
FE02h	6 Bytes		Reserved		
FE08h	Quadword		Descriptor in memory format		
FE10h	Word	CS	Selector		Read-only
FE12h	6 Bytes		Reserved		
FE18h	Quadword		Descriptor in memory format		
FE20h	Word	SS	Selector		Read-only
FE22h	6 Bytes		Reserved		
FE28h	Quadword		Descriptor in memory format		
FE30h	Word	DS	Selector		Read-only
FE32h	6 Bytes		Reserved		
FE38h	Quadword		Descriptor in memory format		

Table 7: SMM Save State

Offset	Size	Contents	Access
FE40h	Word	FS Selector Reserved FS Base {16'b[47], 47:32} ¹	Read-only
FE42h	2 Bytes		
FE44h	Doubleword		
FE48h	Quadword	Descriptor in memory format	
FE50h	Word	GS Selector Reserved GS Base {16'b[47], 47:32} ¹	Read-only
FE52h	2 Bytes		
FE54h	Doubleword		
FE58h	Quadword	Descriptor in memory format	
FE60h	4 Bytes	GDTR Reserved Limit Reserved	Read-only
FE64h	Word		
FE66h	2 Bytes		
FE68h	Quadword	Descriptor in memory format	
FE70h	Word	LDTR Selector Attributes Limit	Read-only
FE72h	Word		
FE74h	Doubleword		
FE78h	Quadword	Base	
FE80h	4 Bytes	IDTR Reserved Limit Reserved	Read-only
FE84h	Word		
FEB6h	2 Bytes		
FE88h	Quadword	Base	
FE90h	Word	TR Selector Attributes Limit	Read-only
FE92h	Word		
FE94h	Doubleword		
FE98h	Quadword	Base	
FEA0h	Quadword	IO_RESTART_RIP	Read-only
FEA8h	Quadword	IO_RESTART_RCX	
FEB0h	Quadword	IO_RESTART_RSI	
FEB8h	Quadword	IO_RESTART_RDI	
FEC0h	Doubleword	SMMFEC0 [SMM IO Trap Offset]	Read-only
FEC4	Doubleword	SMMFEC4 [Local SMI Status]	Read-only
FEC8h	Byte	SMMFEC8 [SMM IO Restart Byte] (no if zero; yes if non-zero)	Read-write
FEC9h	Byte	SMMFEC9 [Auto Halt Restart Offset] (no if zero; yes if non-zero)	Read-write
FECAh	Byte	SMMFECA [NMI Mask]	Read-write
FECCh	4 Bytes	Reserved	
FED0h	Quadword	EFER	Read-only
FED8h	Quadword	SMMFED8 [SMM SVM State]	Read-only
FEE0h	Quadword	Guest VMCB physical address	Read-only

Table 7: SMM Save State

Offset	Size	Contents	Access
FEE8h	Quadword	SVM Virtual Interrupt Control	Read-only
FEF0h	8 Bytes	Reserved	
FEFCh	Doubleword	SMMFEFC [SMM-Revision Identifier]	Read-only
FF00h	Quadword	SMMFF00 [SMM Base Address (SMM_BASE)]	Read-write
FF20h	Quadword	Guest PAT	Read-only
FF28h	Quadword	Host EFER ²	
FF30h	Quadword	Host CR4 ²	
FF38h	Quadword	Nested CR3 ²	
FF40h	Quadword	Host Cr0 ²	
FF48h	Quadword	CR4	
FF50h	Quadword	CR3	
FF58h	Quadword	CR0	
FF60h	Quadword	DR7	Read-only
FF68h	Quadword	DR6	
FF70h	Quadword	RFLAGS	
FF78h	Quadword	RIP	Read-write
FF80h	Quadword	R15	
FF88h	Quadword	R14	
FF90h	Quadword	R13	
FF98h	Quadword	R12	
FFA0h	Quadword	R11	
FFA8h	Quadword	R10	Read-write
FFB0h	Quadword	R9	
FFB8h	Quadword	R8	
FFC0h	Quadword	RDI	
FFC8h	Quadword	RSI	
FFD0h	Quadword	RBP	
FFD8h	Quadword	RSP	
FFE0h	Quadword	RBX	
FFE8h	Quadword	RDX	
FFF0h	Quadword	RCX	
FFF8h	Quadword	RAX	

Notes:

1. This notation specifies that bit[47] is replicated in each of the 16 MSBs of the DW (sometimes called *sign extended*). The 16 LSB's contain bits[47:32].
2. Only used for an SMI in guest mode with nested paging enabled. Used to control the table walker.

The SMI save state includes most of the integer execution unit. Not included in the save state are: the floating point state, MSRs, and CR2. In order to be used by the SMI handler, these must be saved and restored. The save state is the same, regardless of the operating mode (32-bit or 64-bit).

The following are some offsets in the SMM save state area. The mnemonic for each offset is in the form SMMxxxx, where xxxx is the offset in the save state.

SMMFEC0 SMM IO Trap Offset

If the assertion of SMI is recognized on the boundary of an IO instruction, [SMMFEC0 \[SMM IO Trap Offset\]](#) contains information about that IO instruction. For example, if an IO access targets an unavailable device, the system can assert SMI and trap the IO instruction. [SMMFEC0](#) then provides the SMI handler with information about the IO instruction that caused the trap. After the SMI handler takes the appropriate action, it can reconstruct and then re-execute the IO instruction from SMM. Or, more likely, it can use [SMMFEC8 \[SMM IO Restart Byte\]](#), to cause the core to re-execute the IO instruction immediately after resuming from SMM.

Bits	Description
31:16	Port: trapped IO port address. Read-only. This provides the address of the IO instruction.
15:12	BPR: IO breakpoint match. Read-only.
11	TF: EFLAGS TF value. Read-only.
10:7	Reserved.
6	SZ32: size 32 bits. Read-only. 1=Port access was 32 bits.
5	SZ16: size 16 bits. Read-only. 1= Port access was 16 bits.
4	SZ8: size 8 bits. Read-only. 1=Port access was 8 bits.
3	REP: repeated port access. Read-only.
2	STR: string-based port access. Read-only.
1	V: IO trap word valid. Read-only. 1=The core entered SMM on an IO instruction boundary; all information in this offset is valid. 0=The other fields of this offset are not valid.
0	RW: port access type. Read-only. 0=IO write (OUT instruction). 1=IO read (IN instruction).

SMMFEC4 Local SMI Status

This offset stores status bits associated with SMI sources local to the core. For each of these bits, 1=The associated mechanism generated an SMI.

Bits	Description
17	SmiSrcLvtExt: SMI source LVT extended entry. Read-only. This bit is associated with the SMI sources specified in APIC[530:500] [Extended Interrupt [3:0] Local Vector Table] .
16	SmiSrcLvtLcy: SMI source LVT legacy entry. Read-only. This bit is associated with the SMI sources specified by the non-extended LVT entries of the APIC.
15:9	Reserved.
8	MceRedirSts: machine check exception redirection status. Read-only. This bit is associated with the SMI source specified in MSRC001_0022[RedirSmiEn] .
3:0	IoTrapSts: IO trap status. Read-only. Each of these bits is associated with each of the respective SMI sources specified in MSRC001_00[53:50] [IO Trap (SMI_ON_IO_TRAP_[3:0])] .

SMMFEC8 SMM IO Restart Byte

00h on entry into SMM.

If the core entered SMM on an IO instruction boundary, the SMI handler may write this to FFh. This causes the core to re-execute the trapped IO instruction immediately after resuming from SMM. The SMI handler should only write to this byte if **SMMFEC0** field V==1; otherwise, the behavior is undefined.

If a second SMI is asserted while a valid IO instruction is trapped by the first SMI handler, the core services the second SMI prior to re-executing the trapped IO instruction. **SMMFEC0** field V==0 during the second entry into SMM, and the second SMI handler must not rewrite this byte.

If there is a simultaneous SMI IO instruction trap and debug breakpoint trap, the processor first responds to the SMI and postpones recognizing the debug exception until after resuming from SMM. If debug registers other than DR6 and DR7 are used while in SMM, they must be saved and restored by the SMI handler. If **SMMFEC8 [SMM IO Restart Byte]**, is set to FFh when the RSM instruction is executed, the debug trap does not occur until after the IO instruction is re-executed.

Bits	Description
7:0	RST: SMM IO Restart Byte. Read-write.

SMMFEC9 Auto Halt Restart Offset

Bits	Description
7:1	Reserved.
0	HLT: halt restart. Read-write. Upon SMM entry, this bit indicates whether SMM was entered from the Halt state. 0=Entered SMM on a normal x86 instruction boundary. 1=Entered SMM from the Halt state. Before returning from SMM, this bit can be written by the SMI handler to specify whether the return from SMM should take the processor back to the Halt state or to the instruction-execution state specified by the SMM state save area (normally, the instruction after the halt). 0=Return to the instruction specified in the SMM save state. 1=Return to the halt state. If the return from SMM takes the processor back to the Halt state, the HLT instruction is not refetched and re-executed. However, the Halt special bus cycle is broadcast and the processor enters the Halt state.

SMMFECA NMI Mask

Bits	Description
7:1	Reserved.
0	NmiMask. Read-write. Specifies whether NMI was masked upon entry to SMM. 0=NMI not masked. 1=NMI masked.

SMMFED8 SMM SVM State

Read-only. This offset stores the SVM state of the processor upon entry into SMM.

Bits	Description
63:4	Reserved.

3	HostEflagsIf: host Eflags IF.														
2:0	SvmState. <table> <tr> <td><u>Bits</u></td> <td><u>Definition</u></td> </tr> <tr> <td>000b</td> <td>SMM entered from a non-guest state.</td> </tr> <tr> <td>001b</td> <td>Reserved.</td> </tr> <tr> <td>010b</td> <td>SMM entered from a guest state.</td> </tr> <tr> <td>101b-011b</td> <td>Reserved.</td> </tr> <tr> <td>110b</td> <td>SMM entered from a guest state with nested paging enabled.</td> </tr> <tr> <td>111b</td> <td>Reserved.</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	000b	SMM entered from a non-guest state.	001b	Reserved.	010b	SMM entered from a guest state.	101b-011b	Reserved.	110b	SMM entered from a guest state with nested paging enabled.	111b	Reserved.
<u>Bits</u>	<u>Definition</u>														
000b	SMM entered from a non-guest state.														
001b	Reserved.														
010b	SMM entered from a guest state.														
101b-011b	Reserved.														
110b	SMM entered from a guest state with nested paging enabled.														
111b	Reserved.														

SMMFEFC SMM-Revision Identifier

SMM entry state: 0003_0064h

Bits	Description
31:18	Reserved.
17	BRL. Read-only. Base relocation supported.
16	IOTrap. Read-only. IO trap supported.
15:0	Revision. Read-only.

SMMFF00 SMM Base Address (SMM_BASE)

Bits	Description
31:0	See: MSRC001_0111 [SmmBase].

2.4.8.2.6 Exceptions and Interrupts in SMM

When SMM is entered, the core masks INTR, NMI, SMI, INIT, and A20M interrupts. The core clears the IF flag to disable INTR interrupts. To enable INTR interrupts within SMM, the SMM handler must set the IF flag to 1. A20M is disabled so that address bit 20 is never masked when in SMM.

Generating an INTR interrupt can be used for unmasking NMI interrupts in SMM. The core recognizes the assertion of NMI within SMM immediately after the completion of an IRET instruction. Once NMI is recognized within SMM, NMI recognition remains enabled until SMM is exited, at which point NMI masking is restored to the state it was in before entering SMM.

While in SMM, the core responds to the DBREQ and STPCLK interrupts, as well as to all exceptions that may be caused by the SMI handler.

2.4.8.2.7 The Protected ASeg and TSeg Areas

These ranges are controlled by [MSRC001_0112](#) and [MSRC001_0113](#); see those registers for details.

2.4.8.2.8 SMM Special Cycles

Special cycles can be initiated on entry and exit from SMM to acknowledge to the system that these transitions are occurring. These are controlled by [MSRC001_0015](#)[RsmSpCycDis, SmiSpCycDis].

2.4.8.2.9 Locking SMM

The SMM registers ([MSRC001_0112](#) and [MSRC001_0113](#)) can be locked from being altered by setting [MSRC001_0015](#)[SmmLock]. SBIOS must lock the SMM registers after initialization to prevent unexpected changes to these registers.

2.4.8.2.10 Synchronizing SMM Entry (Spring-Boarding)

The BIOS must take special care to ensure that all cores have entered SMM prior to accessing shared IO resources and all core SMI interrupt status bits are synchronized. This generally requires that BIOS waits for all cores to enter SMM.

The following conditions can cause one or more cores to enter SMM without all cores entering SMM:

- More than one IO device in the system is enabled to signal an SMI without hardware synchronization (e.g. using an end of SMI gate).
- A single device may signal multiple SMI messages without hardware synchronization (e.g. using an end of SMI gate).
- An SMI is received while one or more AP cores are in the INIT state. This may occur either during BIOS or secure boot.
- A hardware error prevents a core from entering SMM.

The act of synchronizing cores into SMM is called spring-boarding. Because not all of the above conditions can be avoided, it is recommended that all systems support spring-boarding.

An ACPI-compliant IO hub is required for spring-boarding. Depending on the IO hub design, BIOS may have to set additional end-of-SMI bits to trigger an SMI from within SMM.

The software requirements for the suggested spring-boarding implementation are listed as follows.

- A binary semaphore located in SMRAM, accessible by all cores. For the purpose of this discussion, the semaphore is called CheckSpringBoard. CheckSpringBoard is initialized to zero.
- Two semaphores located in SMRAM, accessible by all cores. For the purpose of this discussion, the semaphores are called NotInSMM and WaitInSMM. NotInSMM and WaitInSMM are initialized to a value equal to the number of cores in the system (NumCPUs).

The following BIOS algorithm describes spring-boarding and is optimized to reduce unnecessary SMI activity. This algorithm must be made part of the SMM instruction sequence for each core in the system.

1. Attempt to obtain ownership of the CheckSpringBoard semaphore with a read-modify-write instruction. If ownership was obtained then do the following, else proceed to step 2:

- Check all enabled SMI status bits in the IO hub.
Let Status=enable1&status1 | enable2&status2 | enable3&status3 ... enable n & status n.
- If (Status==0) then perform the following sub-actions.
 - Trigger an SMI broadcast assertion from the IO hub by writing to the software SMI command port.
 - Resume from SMM with the RSM instruction.

//Example:

```
InLineASM{
    BTS CheckSpringBoard,0; Try to obtain ownership of semaphore
    JC Step_2:
    CALL CheckIOHUB_SMIEVT; proc returns ZF=1 for no events
    JNZ Step_2:
    CALL Do_SpringBoard;Trigger SMI and then RSM
```

```
Step_2:
}
```

2. Decrement the NotInSMM variable. Wait for (NotInSMM==0). See Note 1.
3. Execute the core-local event SMI handler. Using a third semaphore (not described here), synchronize core execution at the end of the task. After all cores have executed, proceed to step 4. The following is a brief description of the task for each core:
 - Check all enabled core-local SMI status bits in the core's private or MSR address space. Handle the event if possible, or pass information necessary to handle the event to a mailbox for the BSC to handle.
 - An exclusive mailbox must exist for each core for each core local event.
 - Wait for all cores to complete this task at least once.
4. If the current core executing instructions is not the BSC then jump to step 5. If the core executing instructions is the BSC then jump to the modified main SMI handler task, described below.
 - Check all enabled SMI status bits in the IO hub. Check mailboxes for event status.
 - For each event, handle the event and clear the corresponding status bit.
 - Repeat until all enabled SMI status bits are clear and no mailbox events remain.
 - Set NotInSMM=NumCPUs. (Jump to step 5.)
5. Decrement the WaitInSMM variable. Wait for WaitInSMM=0. See Note 2.
6. Increment the WaitInSMM variable. Wait for WaitInSMM=NumCPUs.
7. If the current processor core executing instructions is the BSC then reset CheckSpringBoard to zero.
8. Resume from SMM with the RSM instruction.

Notes:

1. To support a secure startup by the secure loader the BIOS must provide a timeout escape from the otherwise endless loop. The timeout value should be large enough to account for the latency of all cores entering SMM. The maximum SMM entrance latency is defined by the platform's IO sub-system, not the processor. A value of twice the watchdog timer count is recommended. See [D18F3x44 \[MCA NB Configuration\]](#) for more information on the watchdog time-out value. If a time-out occurs in the wait loop, the BIOS (the last core to decrement NotInSMM) should record the number of cores that have not entered SMM and all cores must fall out of the loop.
2. If a time-out occurs in the wait loop in step 2, the BIOS must not wait for WaitInSMM=0. Instead it must wait for WaitInSMM=(the number of cores recorded in step 2).
3. If BIOS places APs in the INIT state during any part of the boot process when SMIs may be generated, or may generate SMIs before taking all APs out of their initial microcode reset loop (i.e., before [D18F0x1DC\[CpuEn\]](#) is set), then it is recommended that BIOS keep a record of how many APs are in these two states and exclude these cores from the wait loops. SMIs are not recognized by a processor in these states. AMD does not recommend enabling SMI sources prior to bringing all APs out of these states.

2.4.9 Secure Virtual Machine Mode (SVM)

Support for SVM mode is indicated by [CPUID Fn8000_0001_ECX\[SVM\]](#).

2.4.9.1 BIOS support for SVM Disable

The BIOS should include the following user setup options to enable and disable AMD Virtualization™ technology.

- Enable AMD Virtualization™.
 - [MSRC001_0114\[SvmeDisable\]](#) = 0.
 - [MSRC001_0114\[Lock\]](#) = 1.
 - [MSRC001_0118\[SvmLockKey\]](#) = 0000_0000_0000_0000h.
- Disable AMD Virtualization™.

- [MSRC001_0114](#)[SvmeDisable]=1.
- [MSRC001_0114](#)[Lock]=1.
- [MSRC001_0118](#)[SvmLockKey] = 0000_0000_0000_0000h.

The BIOS may also include the following user setup options to disable AMD Virtualization™ technology.

- Disable AMD Virtualization™, with a user supplied key.
 - [MSRC001_0114](#)[SvmeDisable]=1.
 - [MSRC001_0114](#)[Lock]=1.
 - [MSRC001_0118](#)[SvmLockKey] programmed with value supplied by user. This value should be stored in NVRAM.

2.4.10 CPUID Instruction

The CPUID instruction provides data about the features supported by the processor. See [3.18 \[CPUID Instruction Registers\]](#).

2.4.10.1 Multi-Core Support

There are two methods for determining multi-core support. A recommended mechanism is provided and a legacy method is also available for existing operating systems. System software should use the correct architectural mechanism to detect the number of physical cores by observing [CPUID Fn8000_0008_ECX\[NC\]](#). The legacy method utilizes the [CPUID Fn0000_0001_EBX\[LogicalProcessorCount\]](#).

2.5 Power Management

The processor supports many power management features in a variety of systems. [Table 8](#) provides a summary of ACPI states and power management features and indicates whether they are supported.

Table 8: Power Management Support

ACPI/Power Management State	Supported	Description
G0/S0/C0: Working	Yes	
G0/S0/C0: Core P-state transitions	Yes	2.5.3.1 [Core P-states]
G0/S0/C0: NB P-state transitions	Yes	2.5.4.1 [NB P-states]
G0/S0/C0: Hardware thermal control (HTC)	Yes	2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)]
G0/S0/Per-core IO-based C-states	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/C1: Halt	Yes	
G0/S0/CC6: Per-core Power gating	Yes	2.5.3.2 [Core C-states]
G0/S0/XC6: CPC-L2 power gating	Yes	2.5.3.2 [Core C-states] and 2.5.5.2.3.5 [XC6 State]
G0/S0/PC6: 0V support (VDD power plane).	Yes	2.5.3.2 [Core C-states] and 2.5.1.3.2 [Low Power Voltages]
G0/S0/Cx: Cache flushing support	Yes	2.5.3.2.3.1 [C-state Probes and Cache Flushing]
G0/S0: Northbridge C-states (DRAM self-refresh, NB clock-gating)	Yes	2.5.4.2 [NB C-states]
G1/S1: Stand By (Powered On Suspend)	No	
G1/S3: Stand By (Suspend to RAM)	Yes	2.5.8.1 [S-states]
G1/S4: Hibernate (Suspend to Disk)	Yes	
G1/S5: Shut Down (Soft Off)	Yes	
G3 Mechanical Off	Yes	
Parallel VID Interface	No	
Serial VID Interface 1	Yes	
Serial VID Interface 2	Yes	
Single-plane systems	No	
Number of voltage planes	2	2.5.1 [Processor Power Planes And Voltage Control]
APM: Application Power Management	Yes	2.5.9 [Application Power Management (APM)]

2.5.1 Processor Power Planes And Voltage Control

Refer to the *Electrical Data Sheet* and the *AMD Infrastructure Roadmap* for power plane definitions. See [1.2 \[Reference Documents\]](#).

2.5.1.1 Serial VID Interface

The processor includes an interface to control external voltage regulators, called the serial VID interface (SVI). Both SVI1 and SVI2 are supported. On PWROK assertion, the SVT pin is sampled by the processor to determine the SVI mode supported by the voltage regulator. If SVT is high the processor uses SVI2 mode, otherwise the processor uses SVI1 mode. The default frequency for SVI1 is 3.4MHz. The frequency of SVC for SVI2 is controlled by [D18F3xA0\[Svi2HighFreqSel\]](#). See the *AMD Voltage Regulator Specification* and the *AMD Serial VID Interface 2.0 (SVI2) Specification* for additional details.

2.5.1.1.1 SVI2 Features

The processor supports the following SVI2 features:

- Voltage offsets:
 - VDD: [D18F5x12C](#)[CoreOffsetTrim], [D0F0xBC_x3F9F8](#)[SviLoadLineOffsetVdd]. Changes to either register must be reflected in both locations.
 - VDDNB: [D18F5x188](#)[NbOffsetTrim], [D0F0xBC_x3F9F8](#)[SviLoadLineOffsetVddNB]. Changes to either register must be reflected in both locations.
- Load line trim:
 - VDD: [D18F5x12C](#)[CoreLoadLineTrim], [D0F0xBC_x3F9F4](#)[SviTrimValueVdd]. Changes to either register must be reflected in both locations.
 - VDDNB: [D18F5x188](#)[NbLoadLineTrim], [D0F0xBC_x3F9F4](#)[SviTrimValueVddNB]. Changes to either register must be reflected in both locations.

2.5.1.2 Internal VID Registers and Encodings

All VID register fields within the processor are 8-bits wide. When using SVI1, VID encodings are 7-bits wide and the least significant bit is ignored. In SVI2 all 8 bits are used. The VID encodings to voltage translation for all VID codes are defined by the SVI mode. See the *AMD Voltage Regulator Specification* and the *AMD Serial VID Interface 2.0 (SVI2) Specification* for additional details.

The boot VID is 1.0 volts.

2.5.1.2.1 MinVid and MaxVid Check

Hardware limits the minimum and maximum VID code that is sent to the voltage regulator. The allowed limits are specified in [D18F5x17C](#)[MinVid, MaxVid]. Prior to generating VID-change commands to SVI, the processor filters the InputVid value to the OutputVid as follows (higher VID codes correspond to lower voltages and lower VID codes correspond to higher voltages):

- If InputVid < MaxVid, OutputVid=MaxVid.
- Else if (InputVid > MinVid) & (MinVid!=00h), OutputVid=MinVid.
- Else OutputVid=InputVid.

This filtering is applied regardless of the source of the VID-change command, except for THERMTRIP which applies Fuse[ThermVid] irrespective of MinVid.

2.5.1.3 Low Power Features

2.5.1.3.1 PSIx_L Bit

The processor can indicate whether or not it's in a low-voltage state via the PSIx_L bit. This indicator may be used by the voltage regulator to place itself into a more power efficient mode. PSIx_L is controlled independently for VDD and VDDNB. Support for PSIx_L varies with the SVI mode as follows:

- SVI2: The processor supports the PSI0_L and the PSI1_L bits in the data fields of the SVI2 command.
 - PSI0_L: PSI0_L for VDD and VDDNB is enabled using [D18F3xA0](#)[PsiVidEn] and [D18F5x17C](#)[NbPsi0VidEn], respectively. Once enabled, the state of PSI0_L is controlled by [D18F3xA0](#)[PsiVid[7:0]] and [D18F5x17C](#)[NbPsi0Vid]. Changes to the state of PSI0_L can only occur on VID changes.

- PSI1_L: The PSI1_L bit for VDD and VDDNB is specified by D18F5x12C[CorePsi1En] and D0F0xBC_x3F9EC[EnableNbPsi1], respectively. See also D18F5x188[NbPsi1]. Changes to the state of PSI1_L can occur at any time.

2.5.1.3.1.1 BIOS Requirements for PSI0_L

Enabling PSI0_L for the VDD and VDDNB planes depends on support from the voltage regulator and is therefore system specific. The voltage regulator must be able to supply the current required for the processor to operate at the VID code specified in D18F3xA0[PsiVid[7:0]] and D18F5x17C[NbPsi0Vid[7:0]]. Depending on the regulator used, AMD recommends one of the following methods:

- PSI0_L disabled:
 - VDD: To set PSI0_L for the VDD plane, program D18F3xA0[PsiVidEn]=0.
 - VDDNB: To set PSI0_L for the VDDNB plane, program D18F5x17C[NbPsi0VidEn]=0.
- PSI0_L set/clear based on current requirements:
 - VDD: The following algorithm describes how to program PSI0_L on VDD:

PSI_vrm_current = current at which the regulator allows PSI0_L. Refer to parameter BLDCFG_VRM_LOW_POWER_THRESHOLD in AMD Generic Encapsulated Software Architecture (AGESA) Interface Specification, order #44065.

```
previous_voltage = FFh

for (each P-state from P0 to D18F3xDC[HwPstateMaxVal]) {
    pstate_current = ProcIddMax for the current P-state,
                    see 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check];
    pstate_voltage = MSRC001_00[6B:64][CpuVid] of the current P-state;

    if (current P-state == D18F3xDC[HwPstateMaxVal]) {
        next_pstate_current = 0;
    } else {
        next_pstate_current = ProcIddMax for the next P-state,
                            see 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check];
    }

    if ((pstate_current <= PSI_vrm_current) &&
        (next_pstate_current <= PSI_vrm_current) &&
        (pstate_voltage != previous_voltage)) {
        Program D18F3xA0[PsiVid] = pstate_voltage;
        Program D18F3xA0[PsiVidEn] = 1;
        break;
    }
    previous_voltage = pstate_voltage;
}
```

- VDDNB: The following algorithm describes how to program PSI0_L on VDDNB:

NbIddMax = D18F5x16[C:0][NbIddDiv] current.

PSI_vrm_current = current at which the VDDNB regulator allows PSI0_L. Refer to parameter BLDCFG_VRM_NB_LOW_POWER_THRESHOLD in AMD Generic Encapsulated Software Architecture (AGESA) Interface Specification, order #44065.

```
previous_voltage = FFh

for (each valid NB P-state starting with NBP0) {
    pstate_current = NbIddMax of the current NB P-state;
    pstate_voltage = D18F5x16[C:0][NbVid] of the current NB P-state;
```

```

if (current P-state is the last valid P-state) {
    next_pstate_current = 0;
} else {
    next_pstate_current = NbIddMax for the next P-state;
}

if ((pstate_current <= PSI_vrm_current) &&
    (next_pstate_current <= PSI_vrm_current) &&
    (pstate_voltage != previous_voltage)) {
    Program D18F5x17C[NbPsi0Vid] = pstate_voltage;
    Program D18F5x17C[NbPsi0VidEn] = 1;
    break;
}
previous_voltage = pstate_voltage;
}

```

2.5.1.3.2 Low Power Voltages

In order to save power, voltages lower than those normally needed for operation may be applied to the VDD power plane while the processor is in a C-state or S-state. The lower voltages are defined as follows:

- PC6Vid: [D18F5x128\[PC6Vid\]](#) specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores. See [2.5.3.2.3.4 \[Package C6 \(PC6\) State\]](#).

2.5.1.4 Voltage Transitions

The processor supports dynamic voltage transitions on the VDD and VDDNB planes. These transitions are requested by either hardware or software during state changes such as reset, P-state changes, and C-state changes. In all cases the VID code passed to the voltage regulator changes from the old value to the new value without stepping through intermediate values. The voltage regulator ramps the voltage directly from the starting voltage to the final voltage, no stepping occurs. See the *AMD Voltage Regulator Specification* and the *AMD Serial VID Interface 2.0 (SVI2) Specification* for additional details.

- If a voltage increase is requested in SVI2, the processor waits the amount of time specified by [D18F5x12C\[WaitVidCompDis\]](#) before sending any additional voltage change requests to the voltage regulator or before beginning a frequency transition.
- If a voltage decrease is requested, the processor waits the amount of time specified by [D18F5x128\[FastSlamTimeDown\]](#) before sending any additional voltage change requests to the voltage regulator. For voltage decreases, the processor does not wait any time before beginning frequency changes.

The processor continues code execution during voltage changes when in the C0 state.

2.5.1.4.1 Hardware-Initiated Voltage Transitions

When software requests any of the following state changes, or hardware determines that any of the following state changes are necessary, hardware coordinates the necessary voltage changes:

- VDD:
 - Core P-state transition. See [2.5.3.1 \[Core P-states\]](#).
 - Package C-state transition. [D18F5x128\[PC6Vid\]](#) specifies a voltage that does not retain the CPU caches or the core microarchitectural state. PC6Vid does not allow execution and is only applied to the cores.

See [2.5.3.2.3.4 \[Package C6 \(PC6\) State\]](#).

- S-state transition. See [2.5.8.1 \[S-states\]](#).
- VDDNB:
 - NB P-state transition. See [2.5.4.1 \[NB P-states\]](#).
 - S-state transition. See [2.5.8.1 \[S-states\]](#).

2.5.1.4.2 Software-Initiated Voltage Transitions

2.5.1.4.2.1 Software-Initiated NB Voltage Transitions

Software can request voltage changes on the VDDNB power plane using the BIOSSMC_MSG_VDDNB_REQUEST software interrupt. To make a voltage change request, software uses the sequence described in [2.12.1 \[Software Interrupts\]](#) with Service Index 3Ah. This request is evaluated with other VDDNB requests within GNB as mentioned below.

Software voltage requests are considered by hardware when taking voltage plane dependencies into account (see [2.5.2.2 \[Dependencies Between Subcomponents on VDDNB\]](#)).

2.5.2 Frequency and Voltage Domain Dependencies

2.5.2.1 Dependencies Between Cores

Whenever a P-state or C-state is requested on a core (see [2.5.3.1 \[Core P-states\]](#) and [2.5.3.2 \[Core C-states\]](#)), hardware must take the following frequency and voltage domain dependencies into account when deciding whether to make the requested change:

- Cores within a compute unit share a common frequency and voltage domain.
- Compute units within a processor share a common voltage domain, but have independent frequency domains. The voltage is determined by the highest-performance P-state requested on any core.

As a result, the P-state and C-state change requests have the following results:

- If different compute units request different voltages, the VDD voltage is determined by the highest voltage (lowest VID) requested.
- If the cores within a compute unit request different P-states while in C0, frequency and voltage are determined by the highest-performance P-state requested.
- If both cores request non-C0 states, the behavior is specified by [D18F4x128\[CoreCstatePolicy\]](#).
- If one core within a compute unit requests a CC6 while the other core is in C0, the frequency and voltage of the compute unit is determined by the core in C0.
- If one core within a compute unit requests a CC6 while the other core is in C0, the core could independently enter CC6.

2.5.2.2 Dependencies Between Subcomponents on VDDNB

Many subcomponents of the processor reside on the VDDNB power plane. Hardware must take voltage domain dependencies into account when determining whether to make a voltage change requested by one of the subcomponents. Whenever a state transition occurs that causes a voltage change request (see [2.5.1.4.2 \[Hardware-Initiated Voltage Transitions\]](#)), or software makes a voltage change request (see [2.5.1.4.2 \[Software-Initiated Voltage Transitions\]](#)), the VDDNB voltage requested by the processor is determined by the highest voltage (lowest VID) request made by any of the subcomponents or by software. GNB voltage requests can be ignored by NB voltage controller via [D18F5x178\[GnbVidReqDis\]](#).

2.5.2.3 BIOS Requirements for Power Plane Initialization

- Ensure the following fields are configured to their BIOS recommendations:
 - [D18F3xA0\[Svi2HighFreqSel, SviHighFreqSel\]](#).
 - [D18F3xD8\[VS Ramp Slam Time\]](#).
- Optionally configure [PSIx_L](#). Refer to [2.5.1.3.1 \[PSIx_L Bit\]](#) for additional details.

2.5.3 CPU Power Management

2.5.3.1 Core P-states

Core P-states are operational performance states characterized by a unique combination of core frequency and voltage. The processor supports up to 8 core P-states (P0 through P7), specified in [MSRC001_00\[6B:64\]](#). Out of cold reset, the voltage and frequency of the compute units is specified by [MSRC001_0071\[StartupPstate\]](#) and [D18F3xA0\[CofVidProg\]](#).

Support for dynamic core P-state changes is indicated by more than one enabled selection in [MSRC001_00\[6B:64\]\[PstateEn\]](#). At least one enabled P-state (P0) is specified for all processors.

Software requests core P-state changes for each core independently using the hardware P-state control mechanism (a.k.a. fire and forget). Support for hardware P-state control is indicated by [CPUID Fn8000_0007_EDX\[HwPstate\]=1b](#). Software may not request any P-state transitions using the hardware P-state control mechanism until the P-state initialization requirements defined in [2.5.3.1.6 \[BIOS Requirements for Core P-state Initialization and Transitions\]](#) are complete.

The processor supports independently-controllable frequency planes for each compute unit and the NB; and independently-controllable voltage planes. See [2.5.1 \[Processor Power Planes And Voltage Control\]](#) for voltage plane definitions and [1.5.4 \[Supported Feature Variations\]](#) for package/socket-specific information on voltage plane compatibility.

The following terms may be applied to each of these planes:

- FID: frequency ID. Specifies the PLL frequency multiplier, relative to the reference clock, for a given domain.
- DID: divisor ID. Specifies the post-PLL power-of-two divisor that can be used to reduce the operating frequency.
- COF: current operating frequency. Specifies the operating frequency as a function of the FID and DID. Refer to [CoreCOF](#) for the CPU COF formula and [NBCOF](#) for the NB COF formula.
- VID: voltage ID. Specifies the voltage level for a given domain. Refer to [2.5.1.2.1 \[MinVid and MaxVid Check\]](#) for encodings.

All FID and DID parameters for software P-states must be programmed to equivalent values for all cores and NBs in the coherent fabric. See [2.5.3.1.1.1 \[Software P-state Numbering\]](#). Refer to [MSRC001_00\[6B:64\]](#) and [D18F5x16\[C:0\]](#) for further details on programming requirements.

2.5.3.1.1 Core P-state Naming and Numbering

Since the number of boosted P-states may vary from product to product, the mapping between [MSRC001_00\[6B:64\]](#) and the indices used to request P-state changes or status also varies. In order to clarify this, two different numbering schemes are used.

2.5.3.1.1.1 Software P-state Numbering

When referring to software P-state numbering, the following naming convention is used:

- Non-boosted P-states are referred to as P0, P1, etc.
 - P0 is the highest power, highest performance, non-boosted P-state.
 - Each ascending P-state number represents a lower-power, lower performance non-boosted P-state than the prior P-state number.
- Boosted P-states are referred to as Pb0, Pb1, etc.
 - Pb0 is the highest-performance, highest-power boosted P-state.
 - Each higher numbered boosted P-state represents a lower-power, lower-performance boosted P-state.

For example, if [D18F4x15C\[NumBoostStates\]](#) contains the values shown below, then the P-states would be named as follows:

Table 9: Software P-state Naming

D18F4x15C[NumBoost-States]=1		D18F4x15C[NumBoost-States]=3	
P-state Name	Corresponding MSR Address	P-state Name	Corresponding MSR Address
Pb0	MSRC001_0064	Pb0	MSRC001_0064
P0	MSRC001_0065	Pb1	MSRC001_0065
P1	MSRC001_0066	Pb2	MSRC001_0066
P2	MSRC001_0067	P0	MSRC001_0067
P3	MSRC001_0068	P1	MSRC001_0068
P4	MSRC001_0069	P2	MSRC001_0069
P5	MSRC001_006A	P3	MSRC001_006A
P6	MSRC001_006B	P4	MSRC001_006B

All sections and register definitions use software P-state numbering unless otherwise specified.

2.5.3.1.1.2 Hardware P-state Numbering

When referring to hardware P-state numbering, the following naming convention is used:

- All P-states are referred to as P0, P1, etc.
 - P0 is the highest power, highest-performance P-state, regardless of whether it is a boosted P-state or a non-boosted P-state.
 - Each ascending P-state number represents a lower-power, lower-performance P-state, regardless of whether it is a boosted P-state or not.

2.5.3.1.2 Core P-state Control

Core P-states are dynamically controlled by software and are exposed through ACPI objects (refer to [2.5.3.1.8.3 \[ACPI Processor P-state Objects\]](#)). Software requests a core P-state change by writing a 3 bit index corresponding to the desired P-state number to [MSRC001_0062\[PstateCmd\]](#) of the appropriate core. For example, to request P3 for core 0 software would write 011b to core 0's [MSRC001_0062\[PstateCmd\]](#).

Boosted P-states may not be directly requested by software. Whenever software requests the P0 state on a processor that supports APM (i.e. writes 000b to [MSRC001_0062\[PstateCmd\]](#)), hardware dynamically places the core into the highest-performance P-state possible as determined by APM. See [2.5.9 \[Application Power Management \(APM\)\]](#).

Hardware sequences the frequency and voltage changes necessary to complete a P-state transition as specified by [2.5.3.1.5 \[Core P-state Transition Behavior\]](#) with no additional software interaction required. Hardware also coordinates frequency and voltage changes when differing P-state requests are made on cores that share a frequency or voltage plane. See [2.5.2 \[Frequency and Voltage Domain Dependencies\]](#) for details about hardware coordination.

Table 10: Software P-state Control

D18F4x15C[NumBoostStates]=1			D18F4x15C[NumBoostStates]=3		
P-state Name	Index Used for Requests/Status	Corresponding MSR Address	P-state Name	Index Used for Requests/Status	Corresponding MSR Address
Pb0	n/a	MSRC001_0064	Pb0	n/a	MSRC001_0064
P0	0	MSRC001_0065	Pb1	n/a	MSRC001_0065
P1	1	MSRC001_0066	Pb2	n/a	MSRC001_0066
P2	2	MSRC001_0067	P0	0	MSRC001_0067
P3	3	MSRC001_0068	P1	1	MSRC001_0068
P4	4	MSRC001_0069	P2	2	MSRC001_0069
P5	5	MSRC001_006A	P3	3	MSRC001_006A
P6	6	MSRC001_006B	P4	4	MSRC001_006B

Hardware controls the VID for each voltage domain according to the highest requirement of the frequency domain(s) on each plane. For example, the VID for a 4 compute unit dual-plane system must be maintained at the highest level required for all 4 frequency domains. The number of frequency domains in a voltage domain is package/platform specific. Refer to [2.5.3.1.5 \[Core P-state Transition Behavior\]](#) for details on hardware P-state voltage control. [2.5.2.3 \[BIOS Requirements for Power Plane Initialization\]](#) specifies the processor initialization requirements for voltage plane control.

2.5.3.1.3 Core P-state Visibility

[MSRC001_0063\[CurPstate\]](#) reflects the current non-boosted P-state number for each compute unit. For example, if [MSRC001_0063\[CurPstate\]](#)=010b on compute unit 1, then compute unit 1 is in the P2 state. If a compute unit is in a boosted P-state, [MSRC001_0063\[CurPstate\]](#) reads back as 0.

The voltage on a compute unit may not correspond to the VID code specified by the current P-state of the compute unit due to voltage plane dependencies. See [2.5.2 \[Frequency and Voltage Domain Dependencies\]](#). If a compute unit is in the P0 state (i.e. if [MSRC001_0063\[CurPstate\]](#)=0), the frequency of the compute unit could be the frequency specified by P0 or any boosted P-state. To determine the frequency of a compute unit, see [2.5.3.3 \[Effective Frequency\]](#).

2.5.3.1.4 Core P-state Limits

Core P-states may be limited to lower-performance values under certain conditions, including:

- HTC. See [D18F3x64\[HtcPstateLimit\]](#).
- Software. See [D18F3x68\[SwPstateLimit\]](#).
- Core Performance Boost. See [2.5.9 \[Application Power Management \(APM\)\]](#).

- PROCHOT_L assertion. See [2.10.3.1 \[PROCHOT_L and Hardware Thermal Control \(HTC\)\]](#).
- SMU. See [D18F4x13C\[SmuPstateLimit\]](#).

P-state limits are applied to all cores on the processor. The current P-state limit is provided in [MSRC001_0061\[CurPstateLimit\]](#). Changes to the [MSRC001_0061\[CurPstateLimit\]](#) can be programmed to trigger interrupts through [D18F3x64\[PslApicLoEn, PslApicHiEn\]](#). In addition, the maximum P-state value, regardless of the source, is limited as specified in [MSRC001_0061\[PstateMaxVal\]](#).

2.5.3.1.5 Core P-state Transition Behavior

The following rules specify how P-states changes function and interact with other system or processor states:

- If the P-state number is increasing (the compute unit is moving to a lower-performance state), then the COF is changed first, followed by the VID change. If the P-state number is decreasing, then the VID is changed first followed by the COF.
- When the processor initiates a VID change that increases voltage for a voltage domain, no new voltage or frequency changes occur until [D18F3xD8\[VRampSlamTime\]](#) has expired, regardless of whether any new requests are received. When the processor initiates a VID change that decreases voltage for a voltage domain, new voltage or frequency changes are allowed to occur immediately.
 - This is true regardless of whether the frequency or voltages changes occur as a result of P-state or C-state changes.
- If multiple commands are issued that affect the P-state of a domain prior to when the processor initiates the change of the P-state of that domain, then the processor operates on the last one issued.
- Once a P-state change starts, the P-state state machine (PSSM) continues through completion unless interrupted by a PWROK deassertion. If multiple P-state changes are requested concurrently, the PSSM may group the associated VID changes separately from the associated COF changes.
- Behavior during RESET_L assertions:
 - All cores are transitioned to C0.
 - VDD VID is transitioned to HWP0 VID. See [MSRC001_0064\[CpuVid\]](#).
 - If there is no P-state transition activity, then the compute units and NB remain in the current P-state. If there is an altvid applied:
 - If a RESET_L assertion interrupts a P-state transition, then the COF remains in it's current state at the time RESET_L is asserted (either the value of the old or the new P-state). BIOS is required to transition to valid COF and VID settings after a warm reset according to the sequence defined in [2.5.3.1.8 \[BIOS COF and VID Requirements After Warm Reset\]](#).
 - After a warm reset [MSRC001_0063 \[P-state Status\]](#) is consistent with [MSRC001_0071\[CurPstate\]](#). [MSRC001_0062 \[P-state Control\]](#) may not be consistent with [MSRC001_0071\[CurPstate\]](#).
- The OS controls the P-state through [MSRC001_0062 \[P-state Control\]](#), independent of P-state limits described in [D18F3x64\[HtcPstateLimit\]](#), [D18F3x68\[SwPstateLimit\]](#), and [D18F3xC4 \[SBI P-state Limit\]](#). P-state limits interact with OS-directed P-state transitions as follows:
 - Of all the active P-state limits, the one that represents the lowest-performance P-state number, at any given time, is treated as an upper limit on performance.
 - As the limit becomes active or inactive, or if it changes, the P-state for each compute unit is placed in either the last OS-requested P-state or the new limit P-state, whichever is a lower performance P-state number.
 - If the resulting P-state number exceeds [MSRC001_0061\[PstateMaxVal\]](#), regardless of whether it is a limit or OS-requested, then the PstateMaxVal is used instead.

2.5.3.1.6 BIOS Requirements for Core P-state Initialization and Transitions

1. Check that [CPUID Fn8000_0007_EDX\[HwPstate\]=1](#). If not, P-states are not supported, no P-state related

- ACPI objects should be generated, and BIOS must skip the rest of these steps.
2. Complete the [2.5.2.3 \[BIOS Requirements for Power Plane Initialization\]](#).
 3. Ensure the following fields are configured to their BIOS recommendations:
 - [D18F3xA0\[PllLockTime\]](#).
 - [D18F3xD4\[PowerStepUp, PowerStepDown\]](#).
 4. Transition all cores to the minimum performance P-state using the algorithm detailed in [2.5.3.1.8.2 \[Core Minimum P-state Transition Sequence After Warm Reset\]](#).
 5. Complete the [2.5.4.1.2.1 \[NB P-state COF and VID Synchronization After Warm Reset\]](#). All cores on a processor must be in the minimum performance P-state prior to executing this sequence.
 6. Complete the [2.5.3.1.7 \[Processor-Systemboard Power Delivery Compatibility Check\]](#).
 7. Perform the following steps in any order:
 - A. Enable [2.5.9 \[Application Power Management \(APM\)\]](#) as follows:
 - Ensure the following fields are configured to their BIOS recommendations:
 - [D18F4x110\[CSampleTimer\]](#).
 - [D18F4x15C\[ApmMasterEn\]](#).
 - [D18F5xE0\[RunAvgRange\]](#).
 - If [D18F4x15C\[NumBoostStates\]!=0](#), program [D18F4x15C\[BoostSrc\]=1](#).
 - B. Transition all cores to the maximum performance P-state by writing 0 to [MSRC001_0062\[PstateCmd\]](#). This is done to enable faster boot times.
 - C. Create ACPI objects if necessary:
 - Determine the valid set of P-states as indicated by [MSRC001_00\[6B:64\]\[PstateEn\]](#).
 - If P-states are not supported, as indicated by only one enabled selection in [MSRC001_00\[6B:64\]\[PstateEn\]](#), then BIOS must not generate ACPI-defined P-state objects described in [2.5.3.1.8.3 \[ACPI Processor P-state Objects\]](#). Otherwise, the ACPI objects should be generated to enable P-state support.
 - D. Configure the COF and VID for each processor appropriately based on the sequence described in [2.5.4.1.2 \[BIOS NB P-state Configuration\]](#).
 8. Configure PSIx_L. Refer to [2.5.1.3.1 \[PSIx_L Bit\]](#) for additional details.

2.5.3.1.7 Processor-Systemboard Power Delivery Compatibility Check

BIOS must disable processor P-states that require higher power delivery than the systemboard can support. This power delivery compatibility check is designed to prevent system failures caused by exceeding the power delivery capability of the systemboard for the power plane(s) that contain the core(s). Refer to [2.5.1 \[Processor Power Planes And Voltage Control\]](#) for power plane definitions and configuration information. BIOS can optionally notify the user if P-states are detected that exceed the systemboard power delivery capability. Modifications to [MSRC001_00\[6B:64\] \[P-state \[7:0\]\]](#) must be applied equally to all cores on the same node. This check does not ensure functionality for all package/socket compatible processor/systemboard combinations.

[MSRC001_00\[6B:64\]\[PstateEn\]](#) must be set to 0 for any P-state MSR where PstateEn=1 and the processor current requirement (ProcIddMax), defined by the following equation, is greater than the systemboard current delivery capability. ProcIddMax is reported in amps per core power plane.

$$\text{ProcIddMax} = \text{MSRC001_00[6B:64][IddValue]} \text{ current} * 1/10^{\text{MSRC001_00[6B:64][IddDiv]}} * \\ (\text{D18F5x84[CmpCap]} + 1) * 1/2^{\text{D18F3xD8[PwrPlanes]}}$$

The power delivery check should be applied starting with hardware P0 and continue with increasing P-state indexes (1, 2, 3, and 4) for all enabled P-states. Once a compatible P-state is found using the ProcIddMax equation the check is complete. All processor P-states with higher indexes are defined to be lower power and performance, and are therefore compatible with the systemboard.

Example:

- MSRC001_0065[IddValue] = 32d
- MSRC001_0065[IddDiv] = 0d
- D18F5x84[CmpCap] = 1d
- ProcIddMax = $32 * 1 * 2 * 1 = 64A$ per plane

The systemboard must be able to supply $\geq 64A$ for the unified core power plane in order to support P1 for this processor. If the systemboard current delivery capability is $< 64A$ per plane then BIOS must set MSRC001_0065[PstateEn]=0 for all cores on this node, and continue by checking P2 in the same fashion.

If no P-states are disabled while performing the power delivery compatibility check then BIOS does not need to take any action.

If at least one P-state is disabled by performing the power delivery compatibility check and at least one P-state remains enabled, then BIOS must perform the following steps:

1. If the P-state pointed to by [MSRC001_0063\[CurPstate\]](#) is disabled by the power delivery compatibility check, then BIOS must request a transition to an enabled P-state using [MSRC001_0062\[PstateCmd\]](#) and wait for [MSRC001_0063\[CurPstate\]](#) to reflect the new value.
2. Copy the contents of the enabled P-state MSRs ([MSRC001_00\[6B:64\]](#)) to the highest performance P-state locations. E.g. if P0 and P1 are disabled by the power delivery compatibility check and P2 - P4 remain enabled, then the contents of P2 - P4 should be copied to P0 - P2 and P3 and P4 should be disabled (PstateEn=0). This step uses software P-state numbering. See [2.5.3.1.1.1 \[Software P-state Numbering\]](#).
3. Request a P-state transition to the P-state MSR containing the COF/VID values currently applied. E.g. If [MSRC001_0063\[CurPstate\]](#)=100b and P4 P-state MSR information is copied to P2 in step 2, then BIOS should write 010b to [MSRC001_0062\[PstateCmd\]](#) and wait for [MSRC001_0063\[CurPstate\]](#) to reflect the new value.
4. If a subset of boosted P-states are disabled, then copy the contents of the P-state MSR pointed to by the highest performance boosted P-state that is enabled to the P-state MSRs pointed to by the boosted P-states that are disabled.
5. If all boosted P-states are disabled, then program [D18F4x15C\[BoostSrc\]](#)=0.
6. Adjust the following P-state parameters affected by the P-state MSR copy by subtracting the number of software P-states that are disabled by the power delivery compatibility check. This calculation should not wrap, but saturate at 0. E.g. if P0 and P1 are disabled, then each of the following register fields should have 2 subtracted from them:
 - [D18F3x64\[HtcPstateLimit\]](#)
 - [D18F3x68\[SwPstateLimit\]](#)
 - [D18F3xDC\[HwPstateMaxVal\]](#)

If any node has all P-states disabled after performing the power delivery compatibility check, then BIOS must perform the following steps. This does not ensure operation and BIOS should notify the user of the incompatibility between the processor and systemboard if possible.

1. If [MSRC001_0063\[CurPstate\]](#) \neq [MSRC001_0061\[PstateMaxVal\]](#), then write [MSRC001_0061\[PstateMaxVal\]](#) to [MSRC001_0062\[PstateCmd\]](#) and wait for [MSRC001_0063\[CurPstate\]](#) to reflect the new value.
2. If [MSRC001_0061\[PstateMaxVal\]](#) \neq 000b copy the contents of the P-state MSR pointed to by [MSRC001_0061\[PstateMaxVal\]](#) to [MSRC001_0064](#) and set [MSRC001_0064\[PstateEn\]](#); Write 000b to [MSRC001_0062\[PstateCmd\]](#) and wait for [MSRC001_0063\[CurPstate\]](#) to reflect the new value. This step uses software P-state numbering. See [2.5.3.1.1.1 \[Software P-state Numbering\]](#).
3. Adjust the following fields to 000b.
 - [D18F3x64\[HtcPstateLimit\]](#)
 - [D18F3x68\[SwPstateLimit\]](#)

- D18F3xDC[HwPstateMaxVal]
4. Program D18F4x15C[BoostSrc]=0.

2.5.3.1.8 BIOS COF and VID Requirements After Warm Reset

Warm reset is asynchronous and can interrupt P-state transitions leaving the processor in a VID state that does not correspond to MSRC001_0063[CurPstate] on any core. The processor frequency after warm reset corresponds to MSRC001_0063[CurPstate]. See 2.5.3.1.5 [Core P-state Transition Behavior] for P-state transition behavior when RESET_L is asserted. BIOS is required to transition the processor to valid COF and VID settings corresponding to an enabled P-state following warm reset. The cores may be transitioned to either the maximum or minimum P-state COF and VID settings using the sequences defined in 2.5.3.1.8.1 [Core Maximum P-state Transition Sequence After Warm Reset] and 2.5.3.1.8.2 [Core Minimum P-state Transition Sequence After Warm Reset]. Transitioning to the minimum P-state after warm reset is recommended to prevent undesired system behavior if a warm reset occurs before the 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check] is complete. BIOS must also transition NB COF and VID settings after warm reset for processors that support NB P-states (as indicated by NbDid=1 in any of MSRC001_00[6B:64] [P-state [7:0]]) using the sequence defined in 2.5.4.1.2.1 [NB P-state COF and VID Synchronization After Warm Reset]. BIOS is not required to manipulate NB COF and VID settings following warm reset if the warm reset was issued by BIOS to update D18F5x16[C:0][NbFid].

2.5.3.1.8.1 Core Maximum P-state Transition Sequence After Warm Reset

1. If MSRC001_0071[CurPstate] = D18F3xDC[HwPstateMaxVal], then skip step 3 for that core.
2. Write MSRC001_0061[PstateMaxVal] to MSRC001_0062[PstateCmd] on all cores in the processor. This step is required to ensure VDD is set to a non-boosted P-state voltage level since no cores should be in boost at this point. This step is not required for 2.5.3.1.8.2 [Core Minimum P-state Transition Sequence After Warm Reset] since P-state down transitions are not gated by a boost voltage on VDD. See 2.5.3.1.5 [Core P-state Transition Behavior].
3. Wait for MSRC001_0071[CurCpuFid, CurCpuDid] = [CpuFid, CpuDid] from MSRC001_00[6B:64] indexed by D18F3xDC[HwPstateMaxVal].
4. Wait for MSRC001_0071[CurCpuVid] = [CurCpuVid] from MSRC001_00[6B:64] indexed by D18F3xDC[HwPstateMaxVal].
5. All previous steps must be completed on all cores prior to continuing the sequence since a compute unit transitions to the highest performance P-state requested on either core.
6. Write 0 to MSRC001_0062[PstateCmd] on all cores in the processor.
7. Wait for MSRC001_0071[CurCpuFid, CurCpuDid] = [CpuFid, CpuDid] from MSRC001_00[6B:64] indexed by MSRC001_0071[CurPstateLimit]. The check against MSRC001_0071[CurPstateLimit] is required since MSRC001_0071[CurPstateLimit] affects the resultant P-state.
8. If MSRC001_0071[CurPstateLimit] != D18F3xDC[HwPstateMaxVal], wait for MSRC001_0071[CurCpuVid] = [CpuVid] from MSRC001_00[6B:64] indexed by MSRC001_0071[CurPstateLimit]. See 2.5.3.1.8.2 [Core Minimum P-state Transition Sequence After Warm Reset].
9. Wait for MSRC001_0063[CurPstate] = MSRC001_0061[CurPstateLimit].

2.5.3.1.8.2 Core Minimum P-state Transition Sequence After Warm Reset

1. If MSRC001_0071[CurPstate] = MSRC001_0071[CurPstateLimit], then skip step 3 for that core.
2. Write 0 to MSRC001_0062[PstateCmd] on all cores in the processor.
3. Wait for MSRC001_0071[CurCpuFid, CurCpuDid] = [CpuFid, CpuDid] from MSRC001_00[6B:64] indexed by MSRC001_0071[CurPstateLimit].
4. Write MSRC001_0061[PstateMaxVal] to MSRC001_0062[PstateCmd] on all cores in the processor.

5. Wait for [MSRC001_0071](#)[CurCpuFid, CurCpuDid] = [CpuFid, CpuDid] from [MSRC001_00](#)[6B:64] indexed by [D18F3xDC](#)[HwPstateMaxVal].
6. If [MSRC001_0071](#)[CurPstateLimit] != [MSRC001_0071](#)[CurPstate], wait for [MSRC001_0071](#)[CurCpuVid] = [CpuVid] from [MSRC001_00](#)[6B:64] indexed by [D18F3xDC](#)[HwPstateMaxVal]. If [MSRC001_0071](#)[CurPstateLimit] = [MSRC001_0071](#)[CurPstate], do not perform a voltage check. On multi-node processors, there is a corner case where all core frequencies are in PstateMaxVal, but the voltage may not be.
7. Wait for [MSRC001_0063](#)[CurPstate] = [MSRC001_0062](#)[PstateCmd].

2.5.3.1.8.3 ACPI Processor P-state Objects

Processor performance control is implemented through the _PCT, _PSS and _PSD objects in ACPI 2.0 and later revisions. The presence of these objects indicates to the OS that the platform and processor are capable of supporting multiple performance states. Processor performance states are not supported with ACPI 1.0b. BIOS must provide the _PCT, _PSS, and _PSD objects, and define other ACPI parameters to support operating systems that provide native support for processor P-state transitions.

The following rules apply to BIOS generated ACPI objects in multi-core systems. Refer to the appropriate ACPI specification for additional details:

- All cores must expose the same number of performance states to the OS.
- The respective performance states displayed to the OS for each core must have identical performance and power-consumption parameters (e.g. P0 on core 0 must have the same performance and power-consumptions parameters as P0 on core 1, P1 on core 0 must have the same parameters as P1 on core 1, however P0 can be different than P1).
- Performance state objects must be present under each processor object in the system.

2.5.3.1.8.3.1 _PCT (Performance Control)

BIOS must declare the performance control object parameters as functional fixed hardware. This definition indicates the processor driver understands the architectural definition of the P-state interface associated with [CPUID Fn8000_0007_EDX](#)[HwPstate]=1.

- Perf_Ctrl_Register = Functional Fixed Hardware
- Perf_Status_Register = Functional Fixed Hardware

2.5.3.1.8.3.2 _PSS (Performance Supported States)

A unique _PSS entry is created for each non-boosted P-state. The value contained in the _PSS Control field is written to [MSRC001_0062](#) [P-state Control] to request a P-state change to the CoreFreq of the associated _PSS object. The value contained in [MSRC001_0063](#) [P-state Status] can be used to identify the _PSS object of the current P-state request by equating [MSRC001_0063](#)[CurPstate] to the value of the Status field. See [2.5.3.1 \[Core P-states\]](#).

BIOS loops through each of [MSRC001_00](#)[6B:64] applying the following formulas to create the fields for the _PSS object for each valid P-state (see [MSRC001_00](#)[6B:64][PstateEn]). BIOS skips over any P-state MSRs that specify boost P-states (see [D18F4x15C](#)[NumBoostStates]).

- CoreFreq (MHz) = Calculated using the formula for [CoreCOF](#).
- Power (mW) = [MSRC001_00](#)[6B:64][CpuVid] voltage * [MSRC001_00](#)[6B:64][IddValue] current * 1000.
- TransitionLatency (us) and BusMasterLatency (us):

- If [MSRC001_00\[6B:64\]\[CpuFid\]](#) is the same for all enabled P-states (see [MSRC001_00\[6B:64\]\[PstateEn\]](#)) and all boosted P-states:
 - TransitionLatency = BusMasterLatency = (15 steps * [D18F3xD4\[PowerStepDown\]](#) time * 1000 us/ns) + (15 steps * [D18F3xD4\[PowerStepUp\]](#) time * 1000 us/ns)
- Else if [MSRC001_00\[6B:64\]\[CpuFid\]](#) is different for any enabled (see [MSRC001_00\[6B:64\]\[PstateEn\]](#)) or boost P-states:
 - TransitionLatency = BusMasterLatency = (15 steps * [D18F3xD4\[PowerStepDown\]](#) time * 1000 us/ns) + [D18F3xA0\[PllLockTime\]](#) time + (15 steps * [D18F3xD4\[PowerStepUp\]](#) time * 1000 us/ns)
- Example:
 - [MSRC001_00\[6B:64\]\[CpuFid\]](#) is not the same for all P-states
 - [D18F3xD4\[PowerStepDown\]](#) = [D18F3xD4\[PowerStepUp\]](#) = 8h (50 ns/step)
 - [D18F3xA0\[PllLockTime\]](#) = 001b (2 us)
 - TransitionLatency = BusMasterLatency = (15 steps * 50 ns/step / 1000 us/ns) + 2us + (15 steps * 50 ns/step / 1000 us/ns) = 3.5 us (round up to 4 us)
- Control/Status:
 - The highest performance non-boosted P-state must have the _PSS control and status fields programmed to 0.
 - Any lower performance non-boosted P-states must have the _PSS control and status fields programmed in ascending order.

2.5.3.1.8.3.3 _PPC (Performance Present Capabilities)

The _PPC object is optional. Refer to the ACPI specification for details on use and content.

2.5.3.1.8.3.4 _PSD (P-state Dependency)

AMD recommends the ACPI 3.0 _PSD object be generated for each core as follows to cause the cores to transition between P-states independently:

- NumberOfEntries = 5.
- Revision = 0.
- Domain = CPUID Fn0000_0001_EBX[LocalApicId[7:2]].
- CoordType = FEh. (HW_ALL)
- NumProcessors = 4. Indicates the P-state dependency for the number of cores within a compute unit.

2.5.3.1.8.4 Fixed ACPI Description Table (FADT) Entries

Declare the following FADT entries:

- PSTATE_CNT = 00h.
- DUTY_WIDTH = 00h.

2.5.3.1.8.5 XPSS (Microsoft® Extended PSS) Object

Some Microsoft® operating systems require an XPSS object to make P-state changes function properly. A BIOS that implements an XPSS object has special requirements for the _PCT object. See the Microsoft *Extended PSS ACPI Method Specification* for the detailed requirements to implement these objects.

2.5.3.2 Core C-states

C-states are processor power states. C0 is the operational state in which instructions are executed. All other C-states are low-power states in which instructions are not executed. When coming out of warm and cold reset,

the processor is transitioned to the C0 state.

2.5.3.2.1 C-state Names and Numbers

C-states are often referred to by an alphanumeric naming convention, C1, C2, C3, etc. The mapping between ACPI defined C-states and AMD specified C-states is not direct. AMD specified C-states are referred to as IO-based C-states. Up to three IO-based C-states are supported, IO-based C-state 0, 1, and 2. The IO-based C-state index corresponds to the offset added to [MSRC001_0073\[CstateAddr\]](#) to initiate a C-state request. See [2.5.3.2.2 \[C-state Request Interface\]](#). The actions taken by the processor when entering a low-power C-state are configured by software. See [2.5.3.2.3 \[C-state Actions\]](#) for information about AMD specific actions.

2.5.3.2.2 C-state Request Interface

C-states are dynamically requested by software and are exposed through ACPI objects (see [2.5.3.2.6 \[ACPI Processor C-state Objects\]](#)). C-states can be requested on a per-core basis. Software requests a C-state change in one of two ways:

- Reading from an IO address: The IO address must be the address specified by [MSRC001_0073\[CstateAddr\]](#) plus an offset of 0 through 7. The processor always returns 0 for this IO read. Offsets 2 through 7 result in an offset of 2. The IO read is trapped by core microcode and does not leave the processor.
- Executing the HLT instruction. This is equivalent to reading from the IO address specified by [D18F4x128\[HaltCstateIndex\]](#).

Microcode communicates the C-state request to the NB by writing to [D18F4x114\[CstateIndex\]](#). When software requests a C-state transition, hardware evaluates any frequency and voltage domain dependencies and determines which C-state actions to execute. See [2.5.2 \[Frequency and Voltage Domain Dependencies\]](#) and [2.5.3.2.3 \[C-state Actions\]](#).

2.5.3.2.3 C-state Actions

A core takes one of several different possible actions based upon a C-state change request from software. The C-state action fields are defined in [D18F4x11\[C:8\]](#).

2.5.3.2.3.1 C-state Probes and Cache Flushing

If probes occur after a core enters a non-C0 state, and the caches are not flushed by hardware, the core clock may be ramped back up to the C0 frequency to service the probes, as specified by [D18F4x118/D18F4x11C\[CpuPrbEn\]](#).

If a core enters a non-C0 state and cache flush is enabled (see [D18F3xDC\[CacheFlushOnHaltCtl\]](#) and [D18F4x118/D18F4x11C\[CacheFlushEn\]](#)), a timer counts down for a programmable period of time as specified by [D18F3xDC\[CacheFlushOnHaltTmr\]](#) or [D18F4x118/D18F4x11C\[CacheFlushTmrSel\]](#). When the timer expires, the core flushes its L1 cache to L2 cache and the core clocks are ramped down to a divisor specified by [D18F3xDC\[CacheFlushOnHaltCtl\]](#). If the core is the last core within a CPC to enter CC6 (see [2.5.5.2.3.5 \[XC6 State\]](#)), then L2 cache is flushed to DRAM. The core checks for interrupts after each sector of the cache is flushed and exits the C-state if an interrupt occurs. The timer is reset if the core exits the C-state for any reason. See [2.5.3.2.4.2 \[Cache Flush On Halt Saturation Counter\]](#).

As a core enters a non-C0 state, probes are blocked on all cores within a CPC until all probes to the CPC are drained. When all responses are returned from L2 cache, the core may enter non-C0 state. Once a core flushes its caches and performs the stpclk handshake with the L2I, probes are no longer sent to that core. This improves probing performance for cores that are in C0.

2.5.3.2.3.2 Core C1 (CC1) State

When a core enters the CC1 state, its clock ramps down to the frequency specified by [D18F4x118/D18F4x11C\[ClkDivisorCstAct\]](#).

2.5.3.2.3.3 Core C6 (CC6) State

A core can gate off power to its internal logic when it enters any non-C0 state. This power gated state is known as CC6. In order to enter CC6, hardware first enters CC1 then checks [D18F4x118/D18F4x11C\[PwrGateEnCstAct\]](#). Power gating reduces the amount of power consumed by the core. VDD voltage is not reduced when a core is in CC6. The following sequence occurs when a core enters the CC6 state:

8. If [MSRC001_10A0\[CacheC6StateDis\]](#)=0, Internal core state is saved to L1 cache (microcode). Else, internal core state is saved to DRAM.
9. L1 cache is flushed to L2 cache (microcode). See [2.5.3.2.3.1 \[C-state Probes and Cache Flushing\]](#).
10. Power is removed from the core and the core PLL/voltage regulator is powered down as specified by [D18F5x128\[CC6PwrDwnRegEn and CC6PwrDwnVcoEn\]](#).

All of the following must be true in order for a core to be placed into CC6:

- [D18F4x118/D18F4x11C\[CacheFlushEn\]](#)=1 for the corresponding C-state action field.
- [D18F4x118/D18F4x11C\[CacheFlushTmrSel\]](#) != 11b for the corresponding C-state action field.
- [D18F4x118/D18F4x11C\[PwrGateEnCstAct\]](#)=1 for the corresponding C-state action field.
- [D18F2x118\[CC6SaveEn\]](#)=1.
- [D18F2x118\[LockDramCfg\]](#)=1 or [D18F3x12C\[OverrideLockDramCfg\]](#)=1.
- The CC6 storage area in DRAM is configured. See [2.9.11 \[DRAM CC6/PC6 Storage\]](#).

The events which cause a core to exit the CC6 state are specified in [2.5.3.2.5 \[Exiting C-states\]](#). When a core exits the CC6 state, it executes the following sequence:

If a warm reset occurs while a core is in CC6, all MCA registers in the core shown in [Table 65](#) are cleared to 0. See [2.14.1 \[Machine Check Architecture\]](#). Since the core was in CC6, the core was not the cause of the warm reset. As a result, no information pertinent to the reset is lost. Correctable error information logged prior to CC6 entry may be lost, but this is not critical to system operation.

The time required to enter and exit CC6 is directly proportional to the core P-state frequency. Slower core frequencies require longer entry and exit times. Latency issues may occur with core P-state frequencies less than 800MHz.

2.5.3.2.3.4 Package C6 (PC6) State

When all cores enter a non-C0 state, VDD can be reduced to a non-operational voltage that does not retain core state. This state is known as PC6 and reduces the amount of static and dynamic power consumed by all cores.

The following actions are taken by hardware prior to PC6 entry:

1. If [D18F3xA8\[CC6PopDownEn\]](#)=1 and [MSRC001_0071\[CurPstate\] < D18F3xA8\[PopDownPstate\]](#), transition the core P-state to [D18F3xA8\[PopDownPstate\]](#).
2. If [MSRC001_10A0\[CacheC6StateDis\]](#)=0, For all cores not in CC6, internal core state is saved to L1 cache (microcode). Else, internal core state is saved to DRAM.
3. For all cores not in CC6, L1 cache is flushed to L2 cache (microcode). See [2.5.3.2.3.1 \[C-state Probes and Cache Flushing\]](#).
4. VDD is transitioned to the VID specified by [D18F5x128\[PC6Vid\]](#).

5. If the core PLLs are not powered down during CC6 entry (see [2.5.3.2.3.3 \[Core C6 \(CC6\) State\]](#)), then they are powered down as specified by [D18F5x128\[PC6PwrDwnRegEn\]](#).

All of the following must be true on all cores in order for a package to be placed into PC6:

- [D18F4x118/D18F4x11C\[CacheFlushEn\]](#)=1 for the corresponding C-state action field
- [D18F4x118/D18F4x11C\[CacheFlushTmrSel\]](#) != 11b for the corresponding C-state action field.
- [D18F4x118/D18F4x11C\[PwrOffEnCstAct\]](#)=1 for the corresponding C-state action field.
- [D18F2x118\[CC6SaveEn\]](#)=1.
- [D18F2x118\[LockDramCfg\]](#)=1 or [D18F3x12C\[OverrideLockDramCfg\]](#)=1.

2.5.3.2.4 C-state Request Monitors

Deeper C-states have higher entry and exit latencies but provide greater power savings than shallower C-states. To help balance the performance and power needs of the system, the processor can limit access to specific C-states in certain scenarios.

2.5.3.2.4.1 FCH Messaging

The FCH can be notified when the processor transitions package C-states. See the following:

- [D18F4x128\[CstateMsgDis\]](#).
- [D18F5x178\[CstateFusionDis\]](#).

2.5.3.2.4.2 Cache Flush On Halt Saturation Counter

A cache flush success monitor tracks the success rate of cache flush timer expirations relative to the core exiting a C-state. Based on the success rate, caches may be flushed immediately without waiting for the cache flush timer to expire. See [D18F4x130\[CacheFlushSuccessMonitor\]](#) and [D18F4x128\[CacheFlushSucMonThreshold\]](#). When the core resumes normal execution, the caches refill as normal.

2.5.3.2.5 Exiting C-states

The following events may cause the processor to exit a non-C0 C-state and return to C0:

- INTR
- NMI
- SMI
- INIT
- RESET_L assertion

If an INTR is received while a core is in a non-C0 C-state, the state of EFLAGS[IF] and the mechanism used to enter the non-C0 C-state determine the actions taken by the processor.

- Entry via HLT, EFLAGS[IF]==0: The interrupt does not wake up the core.
- Entry via HLT, EFLAGS[IF]==1: The interrupt wakes the core and the core begins execution at the interrupt service routine.
- Entry via IO read, EFLAGS[IF]==0: The interrupt wakes the core and the core begins execution at the instruction after the IN instruction that was used to enter the non-C0 C-state.
- Entry via IO read, EFLAGS[IF]==1: The interrupt wakes the core and the core begins execution at the interrupt service routine.

2.5.3.2.6 ACPI Processor C-state Objects

Processor power control is implemented through the _CST object in ACPI 2.0 and later revisions. The presence of the _CST object indicates to the OS that the platform and processor are capable of supporting multiple power states. BIOS must provide the _CST object and define other ACPI parameters to support operating systems that provide native support for processor C-state transitions. See [2.5.3.2.6.1 \[_CST\]](#).

The _CST object is not supported with ACPI 1.0b. BIOS should provide FADT entries to support operating systems that are not compatible with ACPI 2.0 and later revisions. See [2.5.3.2.6.2 \[_CRS\]](#).

2.5.3.2.6.1 _CST

The _CST object should be generated for each core as follows:

- Count = 1.
- Register = [MSRC001_0073](#)[CstateAddr] + 1.
- Type = 2.
- Latency = 400. From CC6 Latency Calculations.
- Power = 0. This field is set to 0 since it's not used by Linux, Win7, or Vista.

2.5.3.2.6.2 _CRS

BIOS must declare in the root host bridge _CRS object that the IO address range from [MSRC001_0073](#)[CstateAddr] to [MSRC001_0073](#)[CstateAddr]+7 is consumed by the host bridge.

2.5.3.2.6.3 Fixed ACPI Description Table (FADT) Entries

Declare the following FADT entries:

- P_LVL2_LAT = 100.
- P_LVL3_LAT = 1001.
- FLAGS.PROC_C1 = 1.
- FLAGS.P_LVL2_UP = 1.

Declare the following P_BLK entries:

- P_LVL2 = [MSRC001_0073](#)[CstateAddr] + 1.
- P_LVL3 = 0.

BIOS must declare the PSTATE_CNT entry as 00h.

2.5.3.2.7 BIOS Requirements for Initialization

1. Initialize [MSRC001_0073](#)[CstateAddr] with an available IO address. See [2.5.3.2.6.2 \[_CRS\]](#).
2. Initialize [D18F4x11](#)[C:8].
3. Generate ACPI objects as described in [2.5.3.2.6 \[ACPI Processor C-state Objects\]](#).

2.5.3.3 Effective Frequency

The effective frequency interface allows software to discern the average, or effective, frequency of a given core over a configurable window of time. This provides software a measure of actual performance rather than forcing software to assume the current frequency of the core is the frequency of the last P-state requested. This can be useful when the P-state is limited by:

- HTC
- [D18F3x68](#)[SwPstateLimit]

- SBI
- CPB

The following procedure calculates effective frequency using [MSR0000_00E7](#) [Max Performance Frequency Clock Count (MPERF)] and [MSR0000_00E8](#) [Actual Performance Frequency Clock Count (APERF)]:

1. At some point in time, write 0 to both MSRs.
2. At some later point in time, read both MSRs.
3. Effective frequency = (value read from [MSR0000_00E8](#) / value read from [MSR0000_00E7](#)) * P0 frequency using software P-state numbering.

Additional notes:

- The amount of time that elapses between steps 1 and 2 is determined by software.
- It is software's responsibility to disable interrupts or any other events that may occur in between the write of [MSR0000_00E7](#) and the write of [MSR0000_00E8](#) in step 1 or between the read of [MSR0000_00E7](#) and the read of [MSR0000_00E8](#) in step 2.
- The behavior of [MSR0000_00E7](#) and [MSR0000_00E8](#) may be modified by [MSRC001_0015](#)[EffFreqCntM-wait].
- The effective frequency interface provides +/- 50MHz accuracy if the following constraints are met:
- Effective frequency is read at most one time per millisecond.
- When reading or writing [MSR0000_00E7](#) and [MSR0000_00E8](#) software executes only MOV instructions, and no more than 3 MOV instructions, between the two RDMSR or WRMSR instructions.
- [MSR0000_00E7](#) and [MSR0000_00E8](#) are invalid if an overflow occurs. Intel defines each counter to reset to 0 on overflow. AMD counters simply wrap.

2.5.4 NB Power Management

2.5.4.1 NB P-states

The processor supports up to four NB P-states (NBP0 through NBP3), specified in [D18F5x16\[C:0\]](#). Each NB P-state consists of the following:

- Enable: [D18F5x16\[C:0\]\[NbPstateEn\]](#).
- NCLK frequency: [D18F5x16\[C:0\]\[NbFid, NbDid\]](#).
- VDDNB voltage: [D18F5x16\[C:0\]\[NbVid\]](#).
- Memory P-state: [D18F5x16\[C:0\]\[MemPstate\]](#). See [2.5.7.1 \[Memory P-states\]](#).

Out of cold reset, the NB P-state is specified by [D18F5x174\[StartupNbPstate\]](#) and [D18F3xA0\[CofVidProg\]](#). The current NB P-state is specified by [D18F5x174\[CurNbFid, CurNbDid, CurNbVid\]](#).

Although four NB P-states are defined, only two NB P-states are used at any given time, specified by [D18F5x170\[NbPstateHi, NbPstateLo\]](#). See [2.5.6.1.5.2 \[NB P-state Pointer Configuration\]](#).

2.5.4.1.1 NB P-state Transitions

Hardware selects whether to use the high or low NB P-state based on several criteria as follows:

- Core P-state:
 - [MSRC001_00\[6B:64\]\[NbPstate\]](#).
 - [D18F5x170\[NbPstateThreshold\]](#).
- GPU activity (current SCLK DPM state):

- The GPU driver selects levels of GPU activity that force the NB P-state to either the high or low state or allow either NB P-state.
- Hysteresis timer:
 - [D18F5x170\[NbPstateHiRes, NbPstateLoRes\]](#).
- The following configuration registers:
 - [D18F5x170\[SwNbPstateLoDis, NbPstateDisOnP0, NbPstateGnbSlowDis\]](#).
 - [MSRC001_0071\[NbPstateDis\]](#).

Once the UNB determines that an NB P-state transition is necessary, the UNB executes the following sequence:

1. If transitioning from the low NB P-state to the high NB P-state, transition VDDNB voltage.
2. If the GPU is enabled as specified by [D18F5x178\[SwGfxDis\]](#), wait for display buffer to fill.
3. Quiesce all active cores.
4. If the internal GPU is enabled as specified by [D18F5x178\[SwGfxDis\]](#), wait for display buffer to fill (see [D18F5x178\[Dis2ndGnbAllowPsWait\]](#)).
5. Stop memory traffic and place DRAM into self-refresh.
6. Transition NCLK frequency.
7. Update NB P-state specific DRAM settings within hardware, see [D18F2x210_dct\[0\]_nbp\[3:0\]](#).
8. Take DRAM out of self-refresh and allow memory traffic.
9. Wake up cores.
10. If transitioning from the high NB P-state to the low NB P-state, transition VDDNB voltage.

2.5.4.1.2 BIOS NB P-state Configuration

2.5.4.1.2.1 NB P-state COF and VID Synchronization After Warm Reset

BIOS performs the following sequence on one core. This is done after any warm reset and before [2.9.7 \[DCT/DRAM Initialization and Resume\]](#). The sequence must always be performed to ensure the NB VID request matches the NB P-state request.

1. Temp1=[D18F5x170\[SwNbPstateLoDis\]](#).
2. Temp2=[D18F5x170\[NbPstateDisOnP0\]](#).
3. Temp3=[D18F5x170\[NbPstateThreshold\]](#).
4. Temp4=[D18F5x170\[NbPstateGnbSlowDis\]](#).
5. If [MSRC001_0070\[NbPstate\]](#)=0, go to step 6. If [MSRC001_0070\[NbPstate\]](#)=1, go to step 11.
6. Write 1 to [D18F5x170\[NbPstateGnbSlowDis\]](#).
7. Write 0 to [D18F5x170\[SwNbPstateLoDis, NbPstateDisOnP0, NbPstateThreshold\]](#).
8. Wait for [D18F5x174\[CurNbPstate\]](#) = [D18F5x170\[NbPstateLo\]](#) and [D18F5x174\[CurNbFid, CurNbDid\]](#)=[NbFid, NbDid] from [D18F5x16\[C:0\]](#) indexed by [D18F5x170\[NbPstateLo\]](#).
9. Set [D18F5x170\[SwNbPstateLoDis\]](#)=1.
10. Wait for [D18F5x174\[CurNbPstate\]](#) = [D18F5x170\[NbPstateHi\]](#) and [D18F5x174\[CurNbFid, CurNbDid\]](#)=[NbFid, NbDid] from [D18F5x16\[C:0\]](#) indexed by [D18F5x170\[NbPstateHi\]](#). Go to step 15.
11. Write 1 to [D18F5x170\[SwNbPstateLoDis\]](#).
12. Wait for [D18F5x174\[CurNbPstate\]](#) = [D18F5x170\[NbPstateHi\]](#) and [D18F5x174\[CurNbFid, CurNbDid\]](#)=[NbFid, NbDid] from [D18F5x16\[C:0\]](#) indexed by [D18F5x170\[NbPstateHi\]](#).
13. Write 0 to [D18F5x170\[SwNbPstateLoDis, NbPstateDisOnP0, NbPstateThreshold\]](#).
14. Wait for [D18F5x174\[CurNbPstate\]](#) = [D18F5x170\[NbPstateLo\]](#) and [D18F5x174\[CurNbFid, CurNbDid\]](#)=[NbFid, NbDid] from [D18F5x16\[C:0\]](#) indexed by [D18F5x170\[NbPstateLo\]](#).
15. Set [D18F5x170\[SwNbPstateLoDis\]](#)=Temp1, [D18F5x170\[NbPstateDisOnP0\]](#)=Temp2, and [D18F5x170\[NbPstateThreshold\]](#)=Temp3, and [D18F5x170\[NbPstateGnbSlowDis\]](#)=Temp4.

2.5.4.1.2.2 NB P-state Transitions

During boot when [D18F5x174\[NbPstateDis\]](#)=0, BIOS forces the processor to the desired NB P-states using the following steps:

1. Save the values in [D18F5x170](#) for later restoration to unforce the NB P-state.
2. Set the desired NB P-state pointers, [D18F5x170\[NbPstateHi, NbPstateLo\]](#). See [2.5.6.1.5.2 \[NB P-state Pointer Configuration\]](#).
3. Transition to the desired state as follows:
 - In order to transition to [D18F5x170\[NbPstateHi\]](#), program [D18F5x170](#) as follows:
 - SwNbPstateLoDis = 1.
 - Wait for [D18F5x174\[CurNbPstate\]](#) to equal NbPstateHi.
 - In order to transition to [D18F5x170\[NbPstateLo\]](#), program [D18F5x170](#) as follows:
 - SwNbPstateLoDis = NbPstateDisOnP0 = NbPstateThreshold = 0.
 - Wait for [D18F5x174\[CurNbPstate\]](#) to equal NbPstateLo.

BIOS performs the following to release the NB P-state force:

4. Release the NB P-state force by restoring initial [D18F5x170](#) values.
 - Restore the initial [D18F5x170\[SwNbPstateLoDis, NbPstateDisOnP0, NbPstateLo\]](#) values.
 - Restore the initial [D18F5x170\[NbPstateThreshold, NbPstateHi\]](#) values.

2.5.4.1.2.3 NB P-state Configuration for Runtime

Please see the SMU programming guide (see [1.2 \[Reference Documents\]](#)) for details.

2.5.4.2 NB C-states

NB C-states are package-level actions that occur only when all cores enter a non-C0 state (see [2.5.3.2 \[Core C-states\]](#)). See also [2.20.5.1 \[Trace Mode Active/Inactive\]](#). The NB C-state actions are:

- DRAM self-refresh (see [2.5.7.2 \[DRAM Self-Refresh\]](#)):
 - Enable bits: [D18F4x118/D18F4x11C\[SelfRefr\]](#) and [D18F5x128\[SelfRefrDis\]](#).
 - Entry requirements (all of the following must be true):
 - No outstanding GPU traffic or traffic from a link. (GPU->UNB traffic)
 - Exit conditions (any of the following must be true):
 - The local APIC timer expires. See [2.4.8.1 \[Local APIC\]](#).
 - New GPU traffic or traffic from a link. (GPU->UNB traffic)
 - A P-state limit update (see [2.5.3.1.4 \[Core P-state Limits\]](#)) causes the most restrictive P-state limit to become a higher number than the current P-state for any core in CC1.
- NB clock gating:
 - Enable bits: [D18F4x118/D18F4x11C\[NbClkGate\]](#) and [D18F5x128\[ClkGateDis\]](#).
 - Entry requirements:
 - No outstanding GPU traffic or traffic from a link.
 - Exit conditions (any of the following must be true):
 - The local APIC timer expires. See [2.4.8.1 \[Local APIC\]](#).
 - New GPU traffic or traffic from a link.
 - A P-state limit update (see [2.5.3.1.4 \[Core P-state Limits\]](#)) causes the most restrictive P-state limit to become a higher number than the current P-state for any core in CC1.

When entering NB C-states, the actions are taken in the following order:

1. DRAM self-refresh.
2. NB clock gating.

When exiting NB C-states, the actions are taken in the following order:

1. NB clock gating.
2. DRAM self-refresh.

2.5.5 Bandwidth Requirements

- The frequency relationship of (core COF / NB COF) $\leq 6 \ \&\& \ (\text{core COF} / \text{NB COF}) \geq 1$ must be maintained for all supported P-state combinations. E.g., a core P0 COF of 4.0 GHz could not be combined with a NB P0 COF of 0.6 GHz; the NB P0 COF would have to be 0.8 GHz or greater; if the NB P0 COF is 1.2 GHz, then the NB P1 COF of 0.6 GHz may only be supported if the corresponding core P-state specify a COF of 3.0 GHz or less. This limit is only a bound for verification.
- All core P-states are required to be defined such that $(\text{NB COF}/\text{core COF}) \leq 32$, for all NB/core P-state combinations. E.g., if the NB COF is 4.8 GHz then the core COF must be no less than 150 MHz; support for an NB P-state that brings the NB COF down to 2.4 GHz would not change the core COF requirement, since all NB/core P-state combinations must meet this requirement.
- All core P-states must be defined such that **CoreCOF** ≥ 600 MHz.
- **NBCOF** \geq MEMCLK frequency.
- 400MHz \leq **NBCOF** \leq 1600MHz.
- **NBCOF** $\leq 2 * \text{MEMCLK}$ frequency.

2.5.6 GPU and Root Complex Power Management

2.5.6.1 Dynamic Power Management (DPM)

The processor supports dynamic GPU frequency changes along with VDDNB voltage change requests, known as Dynamic Power Management (DPM). Once initialized, hardware dynamically monitors processor utilization and adjusts the frequencies and voltage based on that utilization. For DPM, higher numbered states represent higher performance and lower numbered states represent lower performance.

2.5.6.1.1 Activity Monitors

The processor contains activity monitors which track the usage level of different processor subcomponents. A binary signal from each subcomponent is used to determine whether that subcomponent is busy. On each clock cycle, the activity monitor samples the signal from each unmasked subcomponent. If any given subcomponent reports that it is busy, an accumulator is incremented.

See [D0F0xBC_xC020_0110](#) and [D0F0xBC_xC0200118](#) for LCLK DPM activity monitor.

The output of the activity monitor is then used to determine whether the DPM state should be changed.

2.5.6.1.2 SCLK DPM

SCLK DPM consists of up to 8 states. Any number of states up through 8 may be used and there is no requirement that the states be contiguous.

During runtime, SCLK DPM parameters are programmed by the graphics driver. To support the driver, BIOS creates a data structure in memory containing information about the processor. Please see your AMD

representative for more information.

2.5.6.1.3 LCLK DPM

LCLK DPM consists of up to 8 states. Any number of states up through 8 may be used and there is no requirement that the states be contiguous. Each state is made up of the following parameters.

- Valid bit: [D0F0xBC_x3FD\[8C:00:step14\]\[StateValid\]](#).
- Voltage change hysteresis threshold: [D0F0xBC_x3FD\[8C:00:step14\]\[LowVoltageReqThreshold\]](#).
- Divisor: [D0F0xBC_x3FD\[8C:00:step14\]\[LclkDivider\]](#).
- VID: [D0F0xBC_x3FD\[8C:00:step14\]\[VID\]](#).
 - See [2.5.2.2 \[Dependencies Between Subcomponents on VDDNB\]](#).
- State change hysteresis thresholds: [D0F0xBC_x3FD\[94:08:step14\]\[HysteresisUp, HysteresisDown\]](#).
- Activity thresholds: [D0F0xBC_x3FD\[9C:10:step14\]\[ActivityThreshold\]](#).
- Residency counter: See [D0F0xBC_x3FD\[94:08:step14\]\[ResidencyCounter\]](#).

LCLK DPM is enabled by setting [D0F0xBC_x3FDC8\[LclkDpmEn\]](#) to 1 and interrupting the SMU with Service Index 1Eh (see [2.12.1 \[Software Interrupts\]](#)). LCLK DPM voltage changes are enabled using [D0F0xBC_x3FDC8\[VoltageChgEn\]](#). When LCLK DPM is first enabled, the DPM state is transitioned to [D0F0xBC_x3FDC8\[LclkDpmBootState\]](#).

2.5.6.2 GPU and Root Complex Power Gating

Several subcomponents of the GPU and root complex can be power gated when not in use.

- **GPU:** GPU power gating is initialized and enabled by software (see [GpuEnabled](#) and [D0F0x7C\[ForceIntGfxDisable\]](#)). Once initialized and enabled, the GPU is power gated by hardware when inactive and is un gated by hardware when needed. When internal GPU is disabled by BIOS, BIOS is responsible for power gating the GPU. When internal GPU is disable via fusing, hardware power gates the GPU.
- **UVD:** UVD is power gated by software when not in use and is un gated by software when needed. UVD's internal state is not saved and UVD goes through an internal reset when power is restored.
- **GMC:** GMC power gating is initialized and enabled by software. Once initialized and enabled, GMC is power gated by hardware when inactive and is un gated by hardware when needed. GMC's state is saved internally. If the internal GPU is disabled, either by hardware (fusing) or by software, software is responsible for power gating GMC.
- **VCE:** VCE is power gated by software when not in use and is un gated by software when needed. VCE's internal state is not saved and VCE goes through an internal reset when power is restored.
- **DCE:** DCE is power gated by software when there is no display connected. DCE's internal state is not saved and DCE goes through an internal reset when power is restored.
- **PCIe:** The Gfx link core can be power gated when it is not in use. In addition, the individual phys on the TX and RX sides of each link can be power gated when the links are not connected. During POST and runtime, several software components inform the SMU whether the Gfx link core or the link phys are in use. Hardware dynamically power gates or un gates the Gfx link core and the link phys as needed.

2.5.7 DRAM Power Management

2.5.7.1 Memory P-states

The processor supports up to 2 memory P-states, M0 and M1. Each memory P-state consists of the following:

- MEMCLK frequency
- A set of frequency dependent DRAM timing and configuration registers

See [2.9 \[DRAM Controllers \(DCTs\)\]](#) for DRAM technology specific information and requirements.

All valid memory P-states are associated with a specific NB P-state, as specified by [D18F5x16\[C:0\]\[MemPstate\]](#). When hardware transitions to a new NB P-state, the memory P-state is transitioned to that specified by the new NB P-state.

Out of cold reset the current memory P-state is M0. The P-state value specified by [D18F5x16\[C:0\]\[MemPstate\]](#) of the NB P-state indexed by [D18F5x174\[StartupNbPstate\]](#) is invalid. Support for dynamic memory P-state changes is indicated by [D18F3xE8\[MemPstateCap\]=1](#) and one or more [D18F5x16\[C:0\]\[MemPstate\]=1](#); otherwise M0 is used by hardware for configuration purposes.

During boot, and if [D18F5x170\[MemPstateDis\]=0](#), the BIOS can disable memory P-states using the following steps:

1. Program [D18F5x170\[MemPstateDis\]=1](#).
2. Program [D18F5x16\[C:0\]\[MemPstate\]=0](#).

2.5.7.2 DRAM Self-Refresh

DRAM is placed into self-refresh on S3 entry (see [2.5.8.1.1 \[ACPI Suspend to RAM State \(S3\)\]](#)). [D18F5x178\[AllowSelfRefrS3Dis\]](#) controls whether the NB waits for the GPU to assert an internal AllowSelfRefresh signal before transitioning into self-refresh. [D18F5x178\[InbWakeS3Dis\]](#) controls whether the NB to GPU interface must be idle before this transition is started.

In addition to S3, DRAM is placed into self-refresh in S0 in the following two scenarios:

- NB P-state transitions (see [2.5.4.1 \[NB P-states\]](#)).
- NB C-states (see [2.5.4.2 \[NB C-states\]](#)).

The following requirements must be met before hardware places DRAM into self-refresh:

- No pending traffic.
- One of the following is true:
 - The GPU is idle and the internal display buffer is full as specified by [GMMx63C\[McAllowStop\]](#).
 - The internal GPU is disabled.

Once the above requirements are met, the NB asserts an internal signal called PreSelfRefresh. In response, the GNB asserts an internal signal called AllowSelfRefresh when the DMIF region representing its own display is full or exceeds the high watermark (see [2.5.9.3 \[Stutter Mode\]](#)), and hardware places DRAM into self-refresh.

Early self-refresh occurs when DRAMs are placed in self-refresh before expiration of the cache flush timer. See [D18F4x118/D18F4x11C\[SelfRefrEarly\]](#) and [D18F5x128\[SelfRefrEarlyDis\]](#). If early self-refresh is

enabled, the DRAMs are taken out of self-refresh to perform the flush operation when the cache flush timer expires and then placed back into self-refresh.

The following are events that cause DRAM to transition out of self-refresh:

- Core transitioning to C0.
- Incoming request from any link or the GMC as indicated by the assertion of the internal signal InbWake.
- P-state limit update, only in the case when all cores are not in the power gated (CC6) state.

To save additional power, hardware always tristates MEMCLK when entering self-refresh.

2.5.7.3 Stutter Mode

DRAM is most commonly placed in self-refresh due to stutter mode when the internal GPU is in use. The display buffer in the GPU is a combination of a large buffer known as the DMIF (Display Memory Interface FIFO) and a smaller line buffer. The DMIF takes data originating from DRAM and sends it to the line buffer to draw to the screen. When the data level in the DMIF is full, DRAM is placed in self-refresh, and incoming DRAM requests are queued. As the DMIF drains, it eventually falls below a predefined watermark level, at which point hardware pulls DRAM out of self-refresh and services all the requests in the queue. Once all the requests are complete and the DMIF is full again, a transition back into self-refresh occurs if the stutter mode conditions are still met.

2.5.7.3.1 System BIOS Requirements for Stutter Mode Operation During POST

BIOS creates a data structure in memory containing information about the processor for use by the driver. Please see your AMD representative for more information.

2.5.7.4 EVENT_L

EVENT_L is a level sensitive input to the processor. When asserted, the actions specified by [D18F2xA4](#) are taken. EVENT_L is generally asserted to indicate that a DRAM high temperature condition exists. The minimum assertion time for EVENT_L is 15 ns. The minimum deassertion time for EVENT_L is 15 ns.

- EVENT_L is pulled to VDDIO on the motherboard.
- EVENT_L is ignored while:
 - PWROK is de-asserted.
 - RESET_L is asserted.
- BIOS must ensure that throttling is disabled (see [D18F2xA4\[CmdThrottleMode\]](#)) until DRAM training is complete.

See [2.9.12 \[DRAM On DIMM Thermal Management and Power Capping\]](#).

2.5.8 System Power Management

2.5.8.1 S-states

S-states are ACPI defined sleep states. S0 is the operational state. All other S-states are low-power states in which various voltage rails in the system may or may not be powered. See the ACPI specification for descriptions of each S-state. The only other S-state supported is S5.

2.5.8.1.1 ACPI Suspend to RAM State (S3)

The processor supports the ACPI-defined S3 state. Software is responsible for restoring the state of the processor's registers when resuming from S3. All registers in the processor that BIOS initialized during the

initial boot must be restored. The method used to restore the registers is system specific.

During S3 entry, software is responsible for transitioning the processor to Memory Pstate0. See [2.5.7.1 \[Memory P-states\]](#).

During S3 entry, system memory enters self-refresh mode (see [2.5.7.2 \[DRAM Self-Refresh\]](#)). Software is responsible for bringing memory out of self-refresh mode when resuming from S3. To bring memory out of self-refresh mode. See [2.9.7 \[DCT/DRAM Initialization and Resume\]](#).

Many of the systemboard power planes for the processor are powered down during S3. Refer to the Electrical Data Sheet and the AMD Infrastructure Roadmap for the following:

- Power plane electrical requirements during S3.
- Power plane sequencing requirements on S3 entry and exit.
- System signal states for both inputs (e.g. PWROK and RESET_L) and outputs (e.g. VID[*], PSI_L bit, THERMTRIP_L, etc.) during S3.
- System signal sequencing requirements on S3 entry and exit.
- System management message sequencing on S3 entry and exit.

2.5.9 Application Power Management (APM)

Application Power Management (APM) allows the processor to deterministically provide maximum performance while remaining within the specified power delivery and removal envelope. APM dynamically monitors processor activity and generates an approximation of power consumption. If power consumption exceeds a defined power limit, a P-state limit is applied by APM hardware to reduce power consumption. APM ensures that average power consumption over a thermally significant time period remains at or below the defined power limit. This allows P-states to be defined with higher frequencies and voltages than could be used without APM.

2.5.9.1 Core Performance Boost (CPB)

These P-states are referred to as boosted P-states.

- Support for APM is specified by [CPUID Fn8000_0007_EDX\[CPB\]](#).
- APM is enabled if all of the following conditions are true:
 - [MSRC001_0015\[CpbDis\]](#) = 0 for all cores.
 - [D18F4x15C\[ApmMasterEn\]](#) = 1.
 - [D18F4x15C\[BoostSrc\]](#) = 01b.
 - [D18F4x15C\[NumBoostStates\]](#) != 0.
- APM can be dynamically enabled and disabled through [MSRC001_0015\[CpbDis\]](#). If core performance boost (CPB) is disabled on any core, a P-state limit is applied to all cores. The P-state limit restricts all cores to the highest performance non-boosted P-state. See [2.5.5.1.6 \[Modification of P-state Requests and Visibility\]](#).
- All P-states, both boosted and non-boosted, are specified in [MSRC001_00\[6B:64\]](#).
- The number of boosted P-states is specified by [D18F4x15C\[NumBoostStates\]](#).
 - The number of boosted P-states may vary from product to product.
- Two levels of boosted P-states are supported. Compute units can be placed in the first level of boosted P-states if the processor power consumption remains within the TDP limit. The second level of boosted P-states is C-state Boost. See [2.5.9.1.1 \[C-state Boost\]](#).
- All boosted P-states are always higher performance than non-boosted P-states.
- To ensure proper operation, boosted P-states should be hidden from the operating system. BIOS should not

- provide ACPI _PSS entries for boosted P-states. See [2.5.3.1.8.3.2 \[_PSS \(Performance Supported States\)\]](#).
- The lowest-performance P-state CPB limits the processor to is the highest-performance non-boosted P-state.

2.5.9.1.1 C-state Boost

C-state Boost can only be achieved if a subset of compute units are in CC6 and the processor power consumption remains within the TDP limit. See [D18F4x16C\[CstateCnt, CstateBoost\]](#).

2.5.9.2 TDP Limiting

TDP limiting is a mechanism for capping the power consumption of the processor through a TDP limit.

2.5.9.3 Bidirectional Application Power Management (BAPM)

Bidirectional Application Power Management (BAPM) is an algorithm to enable fine grained power transfers between the core and GPU. This algorithm tracks either power or temperature across the processor which enables maximum performance within a defined limit.

2.6 Performance Monitoring

The processor includes support for two methods of monitoring processor performance:

- 2.6.1 [Performance Monitor Counters].
- 2.6.2 [Instruction Based Sampling (IBS)].

2.6.1 Performance Monitor Counters

The following types of performance counters are supported:

- 2.6.1.1 [Core Performance Monitor Counters], consisting of one set located in each core of each compute unit.
- 2.6.1.2 [L2I Performance Monitor Counters], consisting of one set located in each compute unit.
- 2.6.1.3 [NB Performance Monitor Counters], consisting of one set located in each node.

The accuracy of the performance counters is not ensured. The performance counters are not assured of producing identical measurements each time they are used to measure a particular instruction sequence, and they should not be used to take measurements of very small instruction sequences. The RDPMC instruction is not serializing, and it can be executed out-of-order with respect to other instructions around it. Even when bound by serializing instructions, the system environment at the time the instruction is executed can cause events to be counted before the counter value is loaded into EDX:EAX.

To accurately start counting with the write that enables the counter, disable the counter when changing the event and then enable the counter with a second MSR write.

Writing the performance counters can be useful if there is an intention for software to count a specific number of events, and then trigger an interrupt when that count is reached. An interrupt can be triggered when a performance counter overflows. Software should use the WRMSR instruction to load the count as a two's-complement negative number into the performance counter. This causes the counter to overflow after counting the appropriate number of times.

In addition to the RDMSR instruction, the performance counter registers can be read using a special read performance-monitoring counter instruction, RDPMC. The RDPMC instruction loads the contents of the performance counter register specified by the ECX register, into the EDX register and the EAX register. See [Table 36 \[RDPMC ECX Definition\]](#).

2.6.1.1 Core Performance Monitor Counters

The core performance monitor counters are used by software to count specific non L2 events that occur in a core of the compute unit. Each core of each compute unit provides four 48-bit performance counters. Unless otherwise specified, the events count only the activity of the core, not activity caused by the other core of the compute unit.

[MSRC001_00\[03:00\]](#) specify the events to be monitored and how they are monitored. All of the events are specified in [3.23 \[Core Performance Counter Events\]](#). [MSRC001_00\[07:04\]](#) are the counters.

All of the events are specified in [3.23 \[Core Performance Counter Events\]](#).

2.6.1.2 L2I Performance Monitor Counters

The L2I performance monitor counters are used by software to count specific L2 events that occur in a core of the compute unit. Unless otherwise specified using the thread masks, the events count the activity of all cores. Each compute unit provides four 48-bit performance counters.

[MSRC001_023\[6,4,2,0\]](#) [L2I Performance Event Select (L2I_PERF_CTL[3:0])] specify the events to be monitored and how they are monitored. [MSRC001_023\[7,5,3,1\]](#) [L2I Performance Event Counter (L2I_PERF_CTR[3:0])] are the counters. Support for MSRC001_023[7:0] is indicated by CPUID Fn8000_0001_ECX[PerfCtrExtL2I].

All of the events are specified in [3.24 \[L2I Performance Counter Events\]](#).

All L2I performance monitor events can be counted on all counters.

All L2I performance events are one event per clock.

2.6.1.3 NB Performance Monitor Counters

The NB performance monitor counters are used by software to count specific events that occur in the NB. Each node provides four 48-bit performance counters. Since the northbridge performance counter register are shared by all cores on a node, monitoring of northbridge events should only be performed by one core on a node.

[MSRC001_024\[6,4,2,0\]](#) [Northbridge Performance Event Select (NB_PERF_CTL[3:0])] and [MSRC001_024\[7,5,3,1\]](#) [Northbridge Performance Event Counter (NB_PERF_CTR[3:0])] specify the events to be monitored and how they are monitored. Support for MSRC001_024[7:0] is indicated by CPUID Fn8000_0001_ECX[PerfCtrExtNB].

All of the events are specified in [3.25 \[NB Performance Counter Events\]](#).

All NB performance monitor events can be counted on all counters.

All NB performance events are one event per clock.

NB performance counters do not support APIC interrupt capability.

2.6.2 Instruction Based Sampling (IBS)

IBS is a code profiling mechanism that enables the processor to select a random instruction fetch or micro-op after a programmed time interval has expired and record specific performance information about the operation. An interrupt is generated when the operation is complete as specified by [MSRC001_103A](#) [IBS Control]. An interrupt handler can then read the performance information that was logged for the operation.

The IBS mechanism is split into two parts: instruction fetch performance controlled by [MSRC001_1030](#) [IBS Fetch Control (IbsFetchCtl)]; and instruction execution performance controlled by [MSRC001_1033](#) [IBS Execution Control (IbsOpCtl)]. Instruction fetch sampling provides information about instruction TLB and instruction cache behavior for fetched instructions. Instruction execution sampling provides information about micro-op execution behavior. The data collected for instruction fetch performance is independent from the data collected for instruction execution performance. Support for the IBS feature is indicated by the CPUID Fn8000_0001_ECX[IBS].

Instruction fetch performance is profiled by recording the following performance information for the tagged instruction fetch:

- If the instruction fetch completed or was aborted. See [MSRC001_1030](#).
- The number of clock cycles spent on the instruction fetch. See [MSRC001_1030](#).
- If the instruction fetch hit or missed the IC, hit/missed in the L1 and L2 TLBs, and page size. See [MSRC001_1030](#).

- The linear address, physical address associated with the fetch. See [MSRC001_1031](#), [MSRC001_1032](#).

Instruction execution performance is profiled by tagging one micro-op associated with an instruction. Instructions that decode to more than one micro-op return different performance data depending upon which micro-op associated with the instruction is tagged. These micro-ops are associated with the RIP of the next instruction to retire. The following performance information is returned for the tagged micro-op:

- Branch and execution status for micro-ops. See [MSRC001_1035](#).
- Branch target address for branch micro-ops. See [MSRC001_103B](#).
- The logical address associated with the micro-op. See [MSRC001_1034](#).
- The linear and physical address associated with a load or store micro-op. See [MSRC001_1038](#), [MSRC001_1039](#).
- The data cache access status associated with the micro-op: DC hit/miss, DC miss latency, TLB hit/miss, TLB page size. See [MSRC001_1037](#).
- The number clocks from when the micro-op was tagged until the micro-op retires. See [MSRC001_1035](#).
- The number clocks from when the micro-op completes execution until the micro-op retires. See [MSRC001_1035](#).
- Source information for DRAM and MMIO. See [MSRC001_1036](#).

2.7 Configuration Space

PCI-defined configuration space was originally defined to allow up to 256 bytes of register space for each function of each device; these first 256 bytes are called base configuration space (BCS). It was expanded to support up to 4096 bytes per function; bytes 256 through 4095 are called extended configuration space (ECS). The processor includes configuration space registers located in both BCS and ECS. Processor configuration space is accessed through bus 0, devices 18h to 1Fh, where device 18h corresponds to node 0 and device 1Fh corresponds to node 7. See [2.7.3 \[Processor Configuration Space\]](#).

Configuration space is accessed by the processor through two methods:

- IO-space configuration: IO instructions to addresses CF8h and CFCh.
 - Enabled through [IOCF8\[ConfigEn\]](#), which allows access to BCS.
 - Access to ECS enabled through [MSRC001_001F\[EnableCf8ExtCfg\]](#).
 - Use of IO-space configuration can be programmed to generate GP faults through [MSRC001_0015\[IoCf8GpFault\]](#).
 - SMI trapping for these accesses is specified by [MSRC001_0054 \[IO Trap Control \(SMI_ON_IO_TRAP_CTL_STS\)\]](#) and [MSRC001_00\[53:50\] \[IO Trap \(SMI_ON_IO_TRAP_\[3:0\]\)\]](#).
- MMIO configuration: configuration space is a region of memory space.
 - The base address and size of this range is specified by [MSRC001_0058 \[MMIO Configuration Base Address\]](#). The size is controlled by the number of configuration-space bus numbers supported by the system. Accesses to this range are converted configuration space as follows:
 - Address[31:0] = {0h, bus[7:0], device[4:0], function[2:0], offset[11:0]}

The BIOS may use either configuration space access mechanism during boot. Before booting the OS, BIOS must disable IO access to ECS, enable MMIO configuration and build an ACPI defined MCFG table. BIOS ACPI code must use MMIO to access configuration space.

Per the link specification, BCS accesses utilize link addresses starting at FD_FE00_0000h and ECS accesses utilize link addresses starting at FE_0000_0000h.

2.7.1 MMIO Configuration Coding Requirements

MMIO configuration space accesses must use the uncacheable (UC) memory type.

Instructions used to read MMIO configuration space are required to take the following form:

```
mov eax/ax/al, any_address_mode;
```

Instructions used to write MMIO configuration space are required to take the following form:

```
mov any_address_mode, eax/ax/al;
```

No other source/target registers may be used other than eax/ax/al.

In addition, all such accesses are required not to cross any naturally aligned DW boundary. Access to MMIO configuration space registers that do not meet these requirements result in undefined behavior.

2.7.2 MMIO Configuration Ordering

Since MMIO configuration cycles are not serializing in the way that IO configuration cycles are, their ordering rules relative to posted may result in unexpected behavior.

Therefore, processor MMIO configuration space is designed to match the following ordering relationship that exists naturally with IO-space configuration: if a core generates a configuration cycle followed by a posted-write cycle, then the posted write is held in the processor until the configuration cycle completes. As a result, any unexpected behavior that might have resulted if the posted-write cycle were to pass MMIO configuration cycle is avoided.

2.7.3 Processor Configuration Space

The processor includes configuration space as described in 3 [Registers]. Accesses to unimplemented registers or implemented functions are ignored: writes dropped; reads return 0. Accesses to unimplemented functions also ignored: writes are dropped; however, reads return all F's. The processor does not log any master abort events for accesses to unimplemented registers or functions.

Accesses to device numbers of devices not implemented in the processor are routed based on the configuration map registers. If such requests are master aborted, then the processor can log the event.

2.8 Northbridge (NB)

Each node includes a single northbridge that provides the interface to the local core(s), the interface to system memory, and the interface to system IO devices. The NB includes all power planes except VDD; see 2.5.1 [Processor Power Planes And Voltage Control].

The NB is responsible for routing transactions sourced from cores and link to the appropriate core, cache, DRAM, or link. See 2.4.6 [System Address Map].

2.8.1 NB Architecture

Major NB blocks are: System Request Interface (SRI), Memory Controller (MCT), DRAM Controllers (DCTs), and crossbar (XBAR). SRI interfaces with the core(s). MCT maintains cache coherency and interfaces with the DCTs; MCT maintains a queue of incoming requests called MCQ. XBAR is a switch that routes packets between SRI, MCT, and the link.

The MCT operates on physical addresses. Before passing transactions to the DCTs, the MCT converts physical addresses into *normalized* addresses that correspond to the values programmed into D18F2x[5C:40]_dct[0]

[DRAM CS Base Address]. Normalized addresses include only address bits within the DCTs' range.

2.8.2 NB Routing

2.8.2.1 Address Space Routing

There are four main types of address space routed by the NB:

1. Memory space targeting system DRAM
2. Memory space targeting IO (MMIO)
3. IO space
4. Configuration space.

2.8.2.1.1 DRAM and MMIO Memory Space

Memory space transactions provide the NB with the physical address, cacheability type, access type, and DRAM/MMIO destination type as specified in section 2.4.6.1.2 [Determining The Access Destination for Core Accesses].

Memory-space transactions are handled by the NB as follows:

- IO-device accesses are compared against:
 - If the access matches D18F1x[2CC:2A0,1CC:180,BC:80] [MMIO Base/Limit], then the transaction is routed to the root complex;
 - Else, if the access matches D18F1x[17C:140,7C:40] [DRAM Base/Limit], then the access is routed to the DCT;
 - Else, the access is routed to the UMI.
- For core accesses the routing is determined based on the DRAM/MMIO destination:
 - If the destination is DRAM:
 - Else, if the access matches D18F1x[17C:140,7C:40] [DRAM Base/Limit], then the transaction is routed to the DCT;
 - Else, the access is routed to the UMI.
 - If the destination is MMIO:
 - If the access matches the VGA-compatible MMIO address space and D18F1xF4[VE]=1 then D18F1xF4 describes how the access is routed and controlled;
 - Else, If the access matches D18F1x[2CC:2A0,1CC:180,BC:80] [MMIO Base/Limit], then the transaction is routed to the root complex;
 - Else, the access is routed to the UMI.

2.8.2.1.2 IO Space

IO-space transactions from IO links or cores are routed as follows:

- If the access matches D18F1x[DC:C0] [IO-Space Base/Limit], then the transaction is routed to the root complex;
- Else, If the access matches the VGA-compatible IO address space and D18F1xF4[VE]=1 then D18F1xF4 describes how the access is routed and controlled.
- Else, the access is routed to the UMI.

2.8.2.1.3 Configuration Space

Configuration-space transactions from IO links are master aborted. Configuration-space transactions from cores are routed as follows:

- If the access matches D18F1x[1DC:1D0,EC:E0] [Configuration Map], then the transaction is routed to the specified link;
- Else, the access is routed to link that contains compatibility (subtractive) address space.

2.8.2.1.3.1 Recommended Buffer Count Settings Overview

When changing from the recommended settings, see the register programming requirements in the definition of each register. Some chipsets may further optimize these settings for their platform. If values other than the recommended settings are used, see the register requirements in the definition of each register. Table 11 defines commonly used terms for the following tables.

Table 11: ONION Link Definitions

Term	Definition
LinkGanged	Ganged = 0.

2.8.3 Memory Scrubbers

The processor includes memory scrubbers specified in [MSRC001_10A0](#), [D18F3x58](#), [D18F3x5C](#), and [D18F3x60](#). The scrubbers ensure that all cachelines in memory within or connected to the processor are periodically read and, if correctable errors are discovered, they are corrected.

For recommendations on scrub rates, see [2.14.1.8 \[Scrub Rate Considerations\]](#).

The scrub rate is specified as the time between successive scrub events. A scrub event occurs when a line of memory is checked for errors; the amount of memory that is checked varies based on the memory block (see field descriptions).

The time required to fully scrub the memory of a node is determined as:

- Time = ((memory size in bytes)/64) * (Scrub Rate).
- E.g. If a node contains 1GB of system memory and DramScrub=5.24 ms, then all of the system memory of the node is scrubbed about once every 23 hours.

2.9 DRAM Controllers (DCTs)

The processor includes one DRAM controller (DCT). Each DCT controls one 64-bit DDR3 DRAM channel.

A DRAM channel consists of the group of DRAM interface pins connecting to one series of DIMMs.

BIOS reads [D18F5x84\[DctEn\]](#) to determine the DCT to DDR channel mapping as follows:

- DCT0 controls channel A.

The DCTs operate on normalized addresses corresponding to the values programmed into [D18F2x\[5C:40\]_dct\[0\]](#). Normalized addresses only include address bits within a DCT's range. The physical to normalized address translation varies based on various Northbridge settings. See [2.9.10 \[Memory Hoisting\]](#) and [2.9.11 \[DRAM CC6/PC6 Storage\]](#).

The following restrictions limit the DIMM types and configurations supported by the DCT:

- All DIMMs connected to a node are required to operate at the same MEMCLK frequency, regardless of the channel. All DCTs of a node must be programmed to the same frequency.
- Mixing of DIMM types within a system is not supported.
- RDIMM, LRDIMM, and stacked DRAM type DIMMs are not supported.
- Mixing of ECC and non-ECC DIMMs within a system is not supported

2.9.1 Common DCT Definitions

Table 12: DCT Definitions

Term	Definition								
AutoSelfRefresh	SPDByte[31][2] of the DIMM being configured.								
DataMaskMbType	Motherboard type for processor Data Mask pins. <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>No connect</td></tr> <tr> <td>01b</td><td>Pins are routed per DM rules</td></tr> <tr> <td>10b</td><td>Pins are routed per DQS rules</td></tr> </tbody> </table>	Bits	Description	00b	No connect	01b	Pins are routed per DM rules	10b	Pins are routed per DQS rules
Bits	Description								
00b	No connect								
01b	Pins are routed per DM rules								
10b	Pins are routed per DQS rules								
DdrRate	The DDR data rate (MT/s) as specified by D18F2x94_dct[0][MemClkFreq] and D18F2x2E0_dct[0][M1MemClkFreq] .								
DeviceWidth	SPDByte[7][2:0] of the DIMM being configured.								
DIMM	The DIMM being configured								
DIMM0	DIMM slots 0-n. The DIMMs on each channel are numbered from 0 to n where								
DIMM1	DIMM0 is the DIMM closest to the processor on that channel and DIMMn is the DIMM farthest from the processor on that channel.								
DimmsPopulated	The number of DIMMs populated per channel plus rows of Solder-down DRAM devices .								
DR	Dual Rank								
DramCapacity	SPDByte[4][3:0] of the DIMM being configured.								
ExtendedTemperature-Range	SPDByte[31][0] of the DIMM being configured.								
MRS	JEDEC defined DRAM Mode Register Set.								
NP	No DIMM populated								

Table 12: DCT Definitions

Term	Definition
NumDimmSlots	The number of motherboard DIMM slots per channel plus rows of Solder-down DRAM devices
NumRanks	SPDByte[7][5:3] of the DIMM being configured, or the number of ranks soldered down.
Rank	The rank being configured
RankMap	SPDByte[63][0] of the DIMM being configured.
RowAddrBits	SPDByte[5][5:3] of the DIMM being configured.
Solder-down DRAM	DRAM devices soldered directly to the motherboard.
SODIMM	DCT is configured for SODIMM if (D18F2x90_dct[0][UnbuffDimm]==1) and SODIMMs are populated.
SPD	Serial Presence Detect. In the case of DRAMs soldered on the platform, this refers to a virtual representation of the DRAM vendors' data sheets.
SR	Single Rank
UDIMM	DCT is configured for UDIMM if (D18F2x90_dct[0][UnbuffDimm]==1) and UDIMMs are populated.
VDDIO	DDR VDDIO in V.

2.9.2 DCT Frequency Support

The tables below list the maximum DIMM speeds supported by the processor for different configurations. The motherboard should comply with the relevant AMD socket motherboard design guideline (MBDG) to achieve the rated speeds. In cases where MBDG design options exist, lower-quality options may compromise the maximum achievable speed; motherboard designers should assess the tradeoffs.

Table 13: DDR3 **UDIMM** Maximum Frequency Support with 6-layer Motherboard Design FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	-	-
		-	1	1600	-	-
2	1	1	-	1600	-	-
		-	1	1600	-	-
	2	2	-	1600	-	-
		1	1	1333	-	-
		-	2	1333	-	-

1. Population restrictions (including the order for partially populated channels) may apply.

Table 14: DDR3 **UDIMM** Maximum Frequency Support with 6-layer Motherboard Design FT3 package Microserver

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	1600	-
		-	1	1600	1600	-
2	1	1	-	1600	1600	-
		-	1	1600	1600	-
	2	2	-	1600	1600	-
		1	1	1333	1333	-
		-	2	1333	1333	-

1. Population restrictions (including the order for partially populated channels) may apply.

Table 15: DDR3 **SODIMM** Maximum Frequency Support with 6-layer Motherboard Design FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	1600	1333
		-	1	1600	1600	1333
2	1	1	-	1600	1600	1333
		-	1	1600	1600	1333
	2	2	-	1600	1600	1333
		1	1	1600	1333	1333
		-	2	1600	1333	1333

1. Population restrictions (including the order for partially populated channels) may apply.

Table 16: DDR3 **UDIMM** Maximum Frequency Support with 4-layer Motherboard Design FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	-	-
		-	1	1600	-	-
2	1	1	-	1600	-	-
		-	1	1600	-	-
	2	2	-	1600	-	-
		1	1	1333	-	-
		-	2	1333	-	-

1. Population restrictions (including the order for partially populated channels) may apply.

Table 17: DDR3 SODIMM Maximum Frequency Support with 4-layer Motherboard Design FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	1333-1600 ²	1066-1333 ²
		-	1	1600	1333-1600 ²	1066-1333 ²
2	1	1	-	1333-1600 ²	1333-1600 ²	1066
		-	1	1333-1600 ²	1333-1600 ²	1066
	2	2	-	1333-1600 ²	1333	1066
		1	1	1333	1333	1066
		-	2	1333	1333	1066
1. Population restrictions (including the order for partially populated channels) may apply.						

Table 18: DDR3 SODIMM plus Solder-down DRAM Maximum Frequency with 6-layer Motherboard FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
2	1	1	-	1333	1333	1066
		-	1	1333	1333	1066
	2	2	-	1333	1333	1066
		1	1	1333	1066	1066
		-	2	1333	1066	1066
1. Population restrictions (including the order for partially populated channels) may apply.						

Table 19: DDR3 SODIMM plus Solder-down DRAM Maximum Frequency with 4-layer Motherboard FT3 package

Num-DimmS-lots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
2	1	1	-	1066	1066	1066
		-	1	1066	1066	1066
	2	2	-	1066	1066	1066
		1	1	1066	1066	1066
		-	2	1066	1066	1066
1. Population restrictions (including the order for partially populated channels) may apply.						

Table 20: DDR3 Solder-down DRAM Maximum Frequency Support FT3 package

Num-DimmSlots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	1600	1333
		-	1	1600	1600	1333

1. Population restrictions (including the order for partially populated channels) may apply.

Table 21: DDR3 UDIMM Maximum Frequency Support FS1b package

Num-DimmSlots	Dimms Populated	DRAM		Frequency ¹ (MT/s)		
		SR	DR	1.5V	1.35V	1.25V
1	1	1	-	1600	1600	1600
		-	1	1600	1600	1333-1600 ²
2	1	1	-	1600	1600	1600
		-	1	1600	1600	1333-1600 ²
	2	2	-	1600	1333-1600 ²	1333
		1	1	1600	1333-1600 ²	1333
		-	2	1600	1333-1600 ²	1333

1. Population restrictions (including the order for partially populated channels) may apply.

The tables below list the DIMM populations as supported by the processor. DIMMs must be populated from farthest slot to closest slot to the processor on a per channel basis when a daisy chain topology is used.

Table 22: DDR3 Population Support

NumDimmSlots	DIMM0	DIMM1
1	SR/DR	N/A
2	NP	SR/DR
	SR/DR	SR/DR

2.9.3 DCT Configuration Registers

There are multiple types of DCT configuration registers:

- Registers for which there is one instance. E.g. [D18F2xA4](#) or [D18F2x78_dct\[0\]](#).
- Registers for which there is one instance per NbPstate use [D18F1x10C\[NbPsSel\]](#) for software accesses.
 - [D18F2x210_dct\[0\]_nbp\[3:0\]](#) refers to all instances of the D18F2x210 register.
 - [D18F2x210_dct\[0\]_nbp\[1\]](#) refers to the register for Nb P-state 1 of any or all DCTs.
- Registers for which there is one instance per memory P-state use [D18F1x10C\[MemPsSel\]](#) for software accesses. The syntax for this register type is described by example as follows:
 - [D18F2x2E8_dct\[0\]_mp\[1:0\]](#) refers to all instances of the D18F2x2E8 register.
 - [D18F2x2E8_dct\[0\]_mp\[1\]](#) refers to the register for memory P-state 1 of either or both DCTs.

2.9.4 DDR Pad to Processor Pin Mapping

The relationship of pad drivers to processor pins varies by package as shown in the following table. The pad names in the tables below may be prefixed with “BP_” to obtain the correct bump name.

Table 23: Package pin mapping

Pad	Pin ¹
	FT3
MEMCLK0_H[0]	MA_CLK_H[0]
MEMCLK0_H[1]	MA_CLK_H[1]
MEMCLK0_H[2]	MA_CLK_H[2]
MEMCLK0_H[3]	MA_CLK_H[3]
MEMCLK0_H[4]	NC
MEMCLK0_H[5]	NC
MEMCS0_L[0]	MA0_CS_L[0]
MEMCS0_L[1]	MA0_CS_L[1]
MEMCS0_L[2]	MA1_CS_L[0]
MEMCS0_L[3]	MA1_CS_L[1]
MEMCS0_L[4]	NC
MEMCS0_L[5]	NC
MEMCS0_L[6]	NC
MEMCS0_L[7]	NC
MEMODT0[0]	MA0_ODT[0]
MEMODT0[1]	MA0_ODT[1]
MEMODT0[2]	MA1_ODT[0]
MEMODT0[3]	MA1_ODT[1]
MEMCKE0[0]	MA_CKE[0]
MEMCKE0[1]	MA_CKE[1]
MEMCKE0[2]	MA_CKE[2]
MEMCKE0[3]	MA_CKE[3]
1. For differential pins, only positive polarity pins are shown; negative polarity pins have corresponding mapping and are controlled by the same CSR field. NC = Not connected. BIOS should tri-state or disable the pad for maximum power savings.	

2.9.4.1 DDR Chip to Pad Mapping

The relationship of chip to pad drivers is shown in the following table. BIOS should disable or power down unused chips for maximum power savings.

Table 24: Pad (from chiplet) pin mapping

Chip	Group	Pad ¹
Clk chip 0	0	MEMCLK0_H[1:0]
Clk chip 1	0	MEMCLK0_H[3:2]
Cmd/Addr 0	0	MEMCS0_L[7,5,3,1]
	1	MEMODT0[3:0]
	2	MEMCS0_L[6,4,2,0]
Cmd/Addr 1	0	MEMRAS0_L MEMCAS0_L MEMWE0_L MEMADD0[13]
	1	MEMADD0[10,0] MEMBANK0[1:0]
	2	MEMPAR0
Address 2	0	MEMCKE0[3:0]
	1	MEMADD0[0,1,8,9]
	2	MEMADD0[2,3,10,11]
	3	MEMADD0[4,5,12,13]
	4	MEMADD0[6,7,14,15]
Data ²	0	MEMDATA[5,4,1,0]
	1	MEMDQS_H[0], MEMDQS_D[0]
	2	MEMDATA[7,6,3,2]

1. For differential pads, only positive polarity pads are shown; negative polarity pads have corresponding mapping and are controlled by the same chip.
Only channel A map is shown. For multi-channel products the other channels are similar.

2. Only Data chip 0 is shown. Remaining data chips are repeated with sequential DQ/DQS/DM pin numbers.

2.9.5 DRAM Controller Direct Response Mode

The DCT supports direct response mode for responding to a cache line fill request before the DCT is initialized. In direct response mode, the target DCT responds to a cache line fill request by returning 64 bytes of all ones without issuing a read transaction on the DRAM bus. The BIOS uses this feature, a.k.a dummy response mode, or, graceful abort, to allocate cache lines for temporary data storage. The controller exits direct response mode when [D18F2x7C_dct\[0\]\[EnDramInit\]](#) or [D18F2x90_dct\[0\]\[InitDram\]\[ExitSelfRef\]](#) is set to 1. See [2.3.3 \[Using L2 Cache as General Storage During Boot\]](#).

2.9.6 DRAM Data Burst Mapping

DRAM requests are mapped to data bursts on the DDR bus in the following order:

- When [D18F2x110\[DctDatIntLv\] = 0](#), a 64 B request is mapped to each of the eight sequential data beats as QW0, QW1...QW7.
- When [D18F2x110\[DctDatIntLv\] = 1](#), the order of cache data to QW on the bus is the same except that even

and odd bits are interleaved on the DRAM bus as follows:

- For every 8 bytes in the cache line, even bits map to QW0, QW2, QW4, and QW6 on the DRAM bus.
- For every 8 bytes in the cache line, odd bits map to QW1, QW3, QW5, and QW7 on the DRAM bus.

2.9.7 DCT/DRAM Initialization and Resume

DRAM initialization involves several steps in order to configure the DRAM controllers and the DRAM, and to tune the DRAM channel for optimal performance.

DRAM resume requires several steps to configure the DCTs to properly resume from the S3 state.

The following sequence describes the steps needed after a reset for initialization or resume:

1. Configure the DDR supply voltage regulator. See [2.9.7.1](#).
2. Force NB P-state to NBP0.
3. Force register accesses to M0. See [2.9.7.3](#) for further requirements used in steps below.
4. DDR phy initialization. See [2.9.7.4](#).
5. DRAM device and controller initialization.
 - If BIOS is booting from an unpowered state (ACPI S4, S5 or G3), then it performs the following:
 - a. Program SPD configuration. See [2.9.7.5](#).
 - b. Program Non-SPD configuration. See [2.9.7.6](#).
 - c. Program DCT training specific configuration. See [2.9.7.7](#).
 - d. Program the remaining DCT registers not covered by an explicit sequence dependency.
 - e. DRAM device initialization. See [2.9.7.8](#).
 - If BIOS is resuming the platform from S3 state, then it performs the following:
 - a. Restore all DCT and phy registers that were programmed during the first boot from non-volatile storage. See [2.9.7.5](#) and [2.9.7.6](#) for a review of registers.
 - b. Program `D18F2x90_dct[0][ExitSelfRef] = 1`. Dct sends MR0.
 - c. Restore the trained delayed values (found during the initial boot in step 6 below) from nonvolatile storage.
 - d. Continue at step 8.
6. DRAM data training.
 - A. Write leveling training. See [2.9.7.9.1](#).
 - B. DQS receiver enable training. See [2.9.7.9.2](#) and [2.9.7.9.3](#).
 - C. DQS position training. See [2.9.7.9.4](#).
7. NB P-state specific training. For each NB P-state to `D18F5x170[NbPstateMaxVal]`:
 - A. Force the NB P-state. See [2.9.7.2](#).
 - B. MaxRdLatency training. See [2.9.7.9.5.1](#). Programs NBPx version.
8. Release NB P-state force.
9. Program DRAM phy for power savings. See [2.9.7.10](#).
10. Program DCT for normal operation. See [2.9.7.7](#).

The DRAM subsystem is ready for use.

2.9.7.1 Low Voltage DDR3

The processor supports JEDEC defined DDR3L and DDR3U devices which operate at voltages lower than 1.5V.

Platforms supporting low voltage devices should power up VDDIO at 1.35V. BIOS should not indefinitely operate DIMMs at voltages higher than supported as indicated by SPD Byte 6: Module Nominal Voltage, VDD.

BIOS should consult vendor data sheets for the supply voltage regulator programming requirements. On supported platforms, BIOS must take steps to configure the supply voltage regulators as follows:

1. Read the SPD of all DIMMs within the programmable VDDIO domain and check all of the defined bits within the SPD byte to determine the common operating voltages. (SPD Byte 6, Bits [2:0] indicate support for 1.25V, 1.35V, 1.5V operation. Refer to the JEDEC specification).
2. Configure VDDIO to match the lowest common supported voltage based on the SPD values.
 - If the DIMMs do not specify a common operating voltage then BIOS must take platform vendor defined action to notify the end user of the mismatch and to protect DIMMs from damage. AMD suggests the following possible actions: Configure VDDIO for 1.35V; configure all DIMMs to run at the lowest frequency supported by the DIMMs and the processor; configure 1.5V-only DIMMs with F2x[1, 0][5C:40][TestFail] bit set prior to sending MRS commands and exclude those DIMMs from the system address map; notify the user of the mismatch. The vendor retains all responsibility for operating mismatched DIMMs.
3. Additional derating of the DDR speed may be necessary for reliable operation at lower voltage. See [2.9.2 \[DCT Frequency Support\]](#).

2.9.7.2 NB P-state Specific Configuration

A subset of DCT configuration and training must be repeated for each enabled NB P-state. To accomplish this, BIOS forces the processor to the desired NB P-state and releases the force once DRAM initialization and training is complete. See [2.5.4.1 \[NB P-states\]](#) and [2.5.4.1.2.2 \[NB P-state Transitions\]](#).

2.9.7.3 Memory P-state Specific Configuration

A subset of DCT configuration and training must be repeated for each enabled memory P-state. See also [2.5.7.1 \[Memory P-states\]](#).

To accomplish this, BIOS forces the processor to the NBP0 state and uses the M0 context to train for values that are used by all memory P-states. For example, BIOS uses [D18F2x94_dct\[0\]\[MemClkFreq\]](#) to specify the dram frequency during each pass of training. BIOS saves the trained configuration values at each step and uses them appropriately as outlined below:

1. Force NB P-state to NBP0. See [2.9.7.2](#).
2. Program [D18F1x10C\[MemPsSel\]=0](#). Force memory P-state DCT CSR access context to M0. See [2.9.3](#).
3. Program [D18F2x9C_x0D04_E008_dct\[0\]\[PStateToAccess\]=0](#). Force memory P-state PHY CSR access context to M0.
4. Using the M0 context, BIOS optimally configures the controller and trains at DDR667 according to [2.9.7](#) steps 4 thru 7. Tcl, Trcd, Trp configured per best practices, etc.
 - A. BIOS saves the trained values for use in M1 and for subsequent higher frequencies.
 - B. BIOS saves the controller configuration for use in M1.
 - C. BIOS optimally writes all the values to registers in step 6. It may optionally write the values as each is computed or trained. If this is done then BIOS must ensure that [D18F1x10C\[MemPsSel\]](#) and [D18F2x9C_x0D04_E008_dct\[0\]\[PStateToAccess\]](#) are configured correctly before and after each register access.
5. BIOS increases the frequency and repeats step 4 until the target frequency is trained. The target frequency is always associated with M0.
6. BIOS programs the M1 controller context with the DDR667 configuration and trained results. This step may optionally be performed after the first pass of step 4 above. This must be done before the next subsequent NB P-state change.
 - a. Program [D18F1x10C\[MemPsSel\]=1](#).
 - b. Program [D18F2x9C_x0D04_E008_dct\[0\]\[PStateToAccess\] = 1](#).
 - c. Program [D18F2x2E0_dct\[0\]\[M1MemClkFreq\]](#) and [D18F2x9C_x0D0F_E000_dct\[0\]\[Rate, FreqValid\] = {04h, 1}](#). 667 MT/s

- d. Program DCT configuration and trained delay values saved earlier.

Three groups of registers must be written in the same order as the initialization sequence so h/w correctly computes fence bits:

- Fence values: [D18F2x9C_x0000_000C_dct\[0\]](#), [D18F2x9C_x0D0F_0\[F,8:0\]31_dct\[0\]](#), [D18F2x9C_x0D0F_E019_dct\[0\]](#).
- Address/Command timing delays: [D18F2x9C_x0000_0004_dct\[0\]_mp\[1:0\]](#).
- All other Data/Dqs delays: See step 6 in section 2.9.7.
- e. Program [D18F2x9C_x0D04_E008_dct\[0\]](#)[PStateToAccess] = 0.
- f. Program [D18F1x10C\[MemPsSel\]](#) = 0.

2.9.7.4 DDR Phy Initialization

The BIOS initializes the phy and the internal interface from the DCT to the phy, including the PLLs and the fence value, after each reset and for each time a MEMCLK frequency change is made.

BIOS obtains size, loading, and frequency information about the DIMMs and channels using SPDs prior to phy initialization. BIOS then performs the following actions:

1. Program [D18F2x9C_x0D0F_E013_dct\[0\]](#) = 0118h.
2. For each byte lane and each memory P-state: Program [D18F2x9C_x0D0F_0\[F,8:0\]13_dct\[0\]_mp\[1:0\]](#)[RxSsbMntClkEn] = 0.
3. Program [D18F2xA8_dct\[0\]](#)[MemPhyPllPdMode] = 00b.
4. Force the phy to M0 with the following sequence.
 - A. Program [D18F2x9C_x0D0F_E006_dct\[0\]](#)[PllLockTime] = 190h. Restore the default PLL lock time.
 - B. Program [D18F2x9C_x0000_000B_dct\[0\]](#) = 80800000h. ESR
 - C. Program [D18F2x9C_x0000_000D18F2x9C_x0000_000B_dct\[0\]](#) = 40000000h. PhyPSR. Note: BIOS performs the sequence only on DCTs with an enabled interface ([D18F2x94_dct\[0\]](#)[DisDramInterface]==0).
 - D. For each DCT: Program [D18F2x9C_x0000_000B_dct\[0\]](#) = 80000000h. XSR
5. Phy Voltage Level Programming. See 2.9.7.4.1.
6. DRAM channel frequency change. See 2.9.7.4.2.
7. Phy fence programming. See 2.9.7.4.3.
8. Phy compensation initialization. See 2.9.7.4.4.

2.9.7.4.1 Phy Voltage Level Programming

BIOS programs the following according to the desired phy VDDIO voltage level:

- Program [D18F2x9C_x0D0F_0\[F,8:0\]1F_dct\[0\]_mp\[1:0\]](#)[RxVioLvl].
- Program [D18F2x9C_x0D0F_\[C,8,2\]\[2:0\]1F_dct\[0\]](#)[RxVioLvl].
- Program [D18F2x9C_x0D0F_4009_dct\[0\]](#)[CmpVioLvl, ComparatorAdjust].
- Program [D18F2x9C_x0D0F_4006_dct\[0\]](#)[VrefSel] = 0.
- Program [D18F2x9C_x0D0F_4007_dct\[0\]](#) per platform requirements.

See 2.9.7.1 [Low Voltage DDR3].

2.9.7.4.2 DRAM Channel Frequency Change

The following sequence is used to change the DRAM frequency under all boot conditions, including restoring the DCT state when resuming from the S3 state. BIOS performs the sequence only on DCTs with an enabled interface ([D18F2x94_dct\[0\]](#)[DisDramInterface]==0):

For each DCT:

1. Program [D18F2x9C_x0D0F_E006_dct\[0\]](#)[PllLockTime] = 190h. Restore the default PLL lock time.

2. Program [D18F2x94_dct\[0\]\[MemClkFreqVal\]](#) = 0.
3. Program [D18F2x94_dct\[0\]\[MemClkFreq\]](#) to the desired DRAM frequency.
4. Program the following parameters which must be configured prior to setting MemClkFreqVal:
 - [D18F2x94_dct\[0\]\[ProcOdtDis\]](#)
 - [D18F2x9C_x0000_0004_dct\[0\]_mp\[1:0\]](#)
 - [D18F2x9C_x0D0F_0\[F,8:0\]13_dct\[0\]_mp\[1:0\]\[ProcOdtAdv\]](#)
 - [D18F2x210_dct\[0\]_nbp\[3:0\]\[RdPtrInit, DataTxFifoWrDly\]](#) of the current NB P-state for the target MEMCLK frequency. See also [2.9.7.2](#).
 - IF (target [DdrRate](#) >= 1600) [D18F2x9C_x0D0F_0\[F,8:0\]38_dct\[0\]\[ReducedLoop\]](#) = 10b ENDIF.

For each DCT:

5. Program [D18F2x94_dct\[0\]\[MemClkFreqVal\]](#) = 1. Wait for [D18F2x94_dct\[0\]\[FreqChgInProg\]](#) = 0.

For each DCT:

6. Program [D18F2x9C_x0D0F_E006_dct\[0\]\[PllLockTime\]](#) according to [Table 25](#).

BIOS must observe the following requirements:

- BIOS must not change the PLL frequency after DRAM has exited from self-refresh.
- BIOS must not change the PLL frequency after the DRAM training for DDR3 DIMMs is complete.

Table 25: DDR PLL Lock Time

D18F2xA8_dct[0][MemPhyPllPdMode]	PllLockTime
00b	0Fh
10b	190h

2.9.7.4.2.1 Requirements for DRAM Frequency Change During Training

During DRAM training, BIOS may be required to change the DRAM(MEMCLK) frequency. The steps below describe what is required to prepare the processor and memory subsystem for the new MEMCLK frequency. It is assumed that the memory subsystem has previously been initialized at the current MEMCLK frequency, and this procedure describes only the steps that must be repeated at the new MEMCLK frequency. See [2.9.7.9.1 \[Write Levelization Training\]](#) and [2.9.7.9.2 \[DQS Receiver Enable Training\]](#).

1. Force the NB P-state. See [2.9.7.2](#).
2. Enter self-refresh:
 - A. Program [D18F2x90_dct\[0\]\[DisDllShutdownSR\]](#) = 1.
 - B. Program [D18F2x90_dct\[0\]\[EnterSelfRef\]](#) = 1.
 - C. Wait for [D18F2x90_dct\[0\]\[EnterSelfRef\]](#) = 0.
3. DRAM channel frequency change. See [2.9.7.4.2](#).
4. Change NCLK frequency to meet NCLK-MEMCLK ratio requirements. See [2.5.3.1.5](#).
5. Phy fence programming. See [2.9.7.4.3](#).
6. Phy compensation initialization. See [2.9.7.4.4](#).
7. Program SPD configuration. See [2.9.7.5](#). Re-program frequency dependent parameters according to the new frequency (Twr, Tewl, Tcl, etc.).
8. Program Non-SPD configuration. See [2.9.7.6](#). Re-program frequency dependent parameters according to the new frequency (ODT, addr/cmd timings, etc.).
9. Exit self-refresh:
 - A. Program [D18F2x90_dct\[0\]\[ExitSelfRef\]](#) = 1.
 - B. Wait for [D18F2x90_dct\[0\]\[ExitSelfRef\]](#) = 0.
 - C. Program [D18F2x90_dct\[0\]\[DisDllShutdownSR\]](#) = 0.
10. Re-program devices with frequency dependent mode register field values. See [2.9.7.8](#). (Twr, Tewl, Tcl,

etc.).

2.9.7.4.3 Phy Fence Programming

The DDR phy fence logic is used to adjust the phase relationship between the data fifo and the data going to the pad. After any MEMCLK frequency change and before any memory training, BIOS must perform phy fence training for each channel using the following steps:

1. Program **D18F2x9C_x0D0F_0[F,8:0]31_dct[0]** = 0000_0000h.
2. Program **D18F2x9C_x0D0F_E019_dct[0]** = 0000_0000h.
3. Program **D18F2x9C_x0000_0008_dct[0]_mp[1:0][FenceTrSel]**=10b.
4. Program **D18F2x9C_x0000_00[52:50]_dct[0]**=1313_1313h.
5. Perform phy fence training. See 2.9.7.4.3.1 [Phy Fence Training].
6. Write the calculated fence value to **D18F2x9C_x0000_000C_dct[0][FenceThresholdTxDll]**.
7. Program **D18F2x9C_x0000_0008_dct[0]_mp[1:0][FenceTrSel]**=01b.
8. Program **D18F2x9C_x0000_00[52:50]_dct[0]**=1313_1313h.
9. Perform phy fence training. See 2.9.7.4.3.1 [Phy Fence Training].
10. Write the calculated fence value to **D18F2x9C_x0000_000C_dct[0][FenceThresholdRxDll]**.
11. Program **D18F2x9C_x0000_0008_dct[0]_mp[1:0][FenceTrSel]**=11b.
12. Program **D18F2x9C_x0000_00[52:50]_dct[0]**=1313_1313h.
13. Perform phy fence training. See 2.9.7.4.3.1 [Phy Fence Training].
14. Write the calculated fence value to **D18F2x9C_x0000_000C_dct[0][FenceThresholdTxPad]**.
15. Program Fence2 threshold for data as follows:
 - A. IF (**D18F2x9C_x0000_000C_dct[0][FenceThresholdTxPad]** < 16) THEN
 Fence2_TxPad[4:0] = {1b, **D18F2x9C_x0000_000C_dct[0][19:16]**}
 ELSE
 Fence2_TxPad[4:0] = 00000b
 ENDIF.
 B. IF (**D18F2x9C_x0000_000C_dct[0][FenceThresholdRxDll]** < 16) THEN
 Fence2_RxDll[4:0] = {1b, **D18F2x9C_x0000_000C_dct[0][24:21]**}
 ELSE
 Fence2_RxDll[4:0] = 00000b
 ENDIF.
 C. IF (**D18F2x9C_x0000_000C_dct[0][FenceThresholdTxDll]** < 16) THEN
 Fence2_TxDll[4:0] = {1b, **D18F2x9C_x0000_000C_dct[0][29:26]**}
 ELSE
 Fence2_TxDll[4:0] = 00000b
 ENDIF.
 D. Program **D18F2x9C_x0D0F_0[F,8:0]31_dct[0]** = {000000b, Fence2_TxDll[4:0],
 Fence2_TxPad[4:0]}.
 E. Program **D18F2x9C_x0D0F_E019_dct[0]** = {0b, Fence2_RxDll[4:0], 00000b, Fence2_TxPad[4:0]}.
16. Reprogram **D18F2x9C_x0000_0004_dct[0]_mp[1:0]**. This forces the phy to recompute the fence.

When resuming from S3, BIOS reprograms **D18F2x9C_x0000_000C_dct[0][FenceThresholdTxDll]**, **FenceThresholdRxDll**, **FenceThresholdTxPad**, and **D18F2x9C_x0D0F_E019_dct[0]** from values stored in non-volatile storage instead of training. BIOS reprograms **D18F2x9C_x0D0F_0[F,8:0]31_dct[0]** and **D18F2x9C_x0D0F_E019_dct[0]** as indicated in the steps above.

BIOS may use **D18F2x9C_x0000_000C_dct[0]** and **D18F2x9C_x0D0F_E01A_dct[0]** for local storage of fence values during the intermediate time between training and writing the values into non-volatile storage in preparation for S3.

2.9.7.4.3.1 Phy Fence Training

1. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[PhyFenceTrEn]=1. The PRE tracks phase sign using coarse delay bits. For all lanes, the Tx insertion delay, the phase between PCLK and the DLL output clock, is greater than 0 and less than 1 UI; therefore a seed value is not necessary.
2. Wait 2000 MEMCLKs.
3. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[PhyFenceTrEn]=0.
4. Read the phase recovery engine registers [D18F2x9C_x0000_00\[52:50\]_dct\[0\]](#).
5. Calculate the average of the fine delay values of all byte lanes. If FenceTrSel != 00b subtract 8. If the result is negative then the fence value is zero.

2.9.7.4.4 Phy Compensation Initialization

Each DDR IO driver has a programmable slew rate controlled by the pre-driver calibration code. The recommended slew rate is a function of the DC drive strength. BIOS initializes the recommended nominal slew rate values as follows:

1. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[DisAutoComp] = 1.
2. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[DisablePredriverCal]=1.
3. Program TxPreP/TxPreN for Data and DQS according to [Table 26](#), [Table 27](#), or [Table 28](#).
 - A. Program [D18F2x9C_x0D0F_0\[F,8:0\]0\[A,6\]_dct\[0\]](#)={0000b, TxPreP, TxPreN}.
 - B. Program [D18F2x9C_x0D0F_0\[F,8:0\]02_dct\[0\]](#)={1000b, TxPreP, TxPreN}.
4. Program TxPreP/TxPreN for Cmd/Addr according to [Table 29](#), [Table 30](#), or [Table 31](#).
 - A. Program [D18F2x9C_x0D0F_\[C,8\]\[1:0\]12,0E,0A,06_dct\[0\]](#)={0000b, TxPreP, TxPreN}.
 - B. Program [D18F2x9C_x0D0F_\[C,8\]\[1:0\]02_dct\[0\]](#)={1000b, TxPreP, TxPreN}.
5. Program TxPreP/TxPreN for Clock according to [Table 32](#), [Table 33](#), or [Table 34](#).
 - A. Program [D18F2x9C_x0D0F_2\[2:0\]02_dct\[0\]](#)={1000b, TxPreP, TxPreN}.
6. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[DisAutoComp] = 0.

Table 26: Phy predriver calibration codes for Data/DQS at 1.5V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	000b	FFFh
	001b	410h
	010b	208h
	011b	104h
1. IF (D18F2x9C_x0D0F_0[F,8:0]06) THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0] [DqsDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0] [DataDrvStren] ENDIF. 2. See D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0] and D18F2x9C_x0D0F_0[F,8:0]02_dct[0] .		

Table 27: Phy predriver calibration codes for Data/DQS at 1.35V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	000b	FFFh
	001b	FFFh
	010b	820h
	011b	410h
1.	IF (D18F2x9C_x0D0F_0[F,8:0]06) THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][DqsDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0][DataDrvStren] ENDIF.	
2.	See D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0] and D18F2x9C_x0D0F_0[F,8:0]02_dct[0].	

Table 28: Phy Predriver Calibration Codes for Data/DQS at 1.25V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	000b	FFFh
	001b	FFFh
	010b	FFFh
	011b	FFFh
1.	IF (D18F2x9C_x0D0F_0[F,8:0]06) THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][DqsDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0][DataDrvStren] ENDIF.	
2.	See D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0] and D18F2x9C_x0D0F_0[F,8:0]02_dct[0].	

Table 29: Phy predriver calibration codes for Cmd/Addr at 1.5V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	101b	0C3h
	000b	082h
	001b	041h
	010b	041h
	011b	041h
1.	IF (D18F2x9C_x0D0F_C002) THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CkeDrvStren] ELSEIF (D18F2x9C_x0D0F_800[A,6,2]) THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CsOdtDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0][AddrCmdDrvStren] ENDIF.	
2.	See D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0] and D18F2x9C_x0D0F_[C,8][1:0]02_dct[0].	

Table 30: Phy predriver calibration codes for Cmd/Addr at 1.35V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	101b	208h
	000b	186h
	001b	104h
	010b	0C3h
	011b	082h
1.	IF (D18F2x9C_x0D0F_C002)THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CkeDrvStren] ELSEIF (D18F2x9C_x0D0F_800[A,6,2])THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CsOdtDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0][AddrCmdDrvStren] ENDIF.	
2.	See D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0] and D18F2x9C_x0D0F_[C,8][1:0]02_dct[0].	

Table 31: Phy Predriver Calibration Codes for Cmd/Addr at 1.25V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667- 2133	101b	410h
	000b	30Ch
	001b	28Ah
	010b	208h
	011b	186h
1.	IF (D18F2x9C_x0D0F_C002)THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CkeDrvStren] ELSEIF (D18F2x9C_x0D0F_800[A,6,2])THEN See D18F2x9C_x0000_0000_dct[0]_mp[1:0][CsOdtDrvStren] ELSE See D18F2x9C_x0000_0000_dct[0]_mp[1:0][AddrCmdDrvStren] ENDIF.	
2.	See D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0] and D18F2x9C_x0D0F_[C,8][1:0]02_dct[0].	

Table 32: Phy predriver calibration codes for Clock at 1.5V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	101b	FFFh
	000b	FFFh
	001b	FFFh
	010b	FFFh
	011b	820h
1.	See D18F2x9C_x0000_0000_dct[0]_mp[1:0][ClkDrvStren].	
2.	See D18F2x9C_x0D0F_2[2:0]02_dct[0].	

Table 33: Phy predriver calibration codes for Clock at 1.35V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	101b	FFFh
	000b	FFFh
	001b	FFFh
	010b	FFFh
	011b	FFFh

1. See [D18F2x9C_x0000_0000_dct\[0\]_mp\[1:0\]\[ClkDrvStren\]](#).
 2. See [D18F2x9C_x0D0F_2\[2:0\]02_dct\[0\]](#).

Table 34: Phy Predriver Calibration Codes for Clock at 1.25V

DDR Rate	Drive Strength ¹	{TxPreP, TxPreN} ²
667 - 2133	101b	FFFh
	000b	FFFh
	001b	FFFh
	010b	FFFh
	011b	FFFh

1. See [D18F2x9C_x0000_0000_dct\[0\]_mp\[1:0\]\[ClkDrvStren\]](#).
 2. See [D18F2x9C_x0D0F_2\[2:0\]02_dct\[0\]](#).

2.9.7.5 SPD ROM-Based Configuration

The Serial Presence Detect (SPD) ROM is a non-volatile memory device on the DIMM encoded by the DIMM manufacturer. The description of the SPD is usually provided on a data sheet for the DIMM itself along with data describing the memory devices used. The data describes configuration and speed characteristics of the DIMM and the SDRAM components mounted on the DIMM. The associated data sheet also contains the DIMM byte values that are encoded in the SPD on the DIMM.

BIOS reads the values encoded in the SPD ROM through a system-specific interface. BIOS acquires DIMM configuration information, such as the amount of memory on each DIMM, from the SPD ROM on each DIMM and uses this information to program the DRAM controller registers.

For solder-down DRAM, in the absence of an SPD ROM, BIOS provides the information necessary for DRAM configuration. For convenience, this document may refer to solder-down DRAM as a DIMM, and to DRAM data sheet or JEDEC DRAM specifications as SPD ROM based, unless otherwise noted.

The SPD ROM provides values for several DRAM timing parameters that are required by the DCT. In general, BIOS should use the optimal value specified by the SPD ROM. These parameters are:

- [D18F2x8C_dct\[0\]\[Tref\]](#): See SPD Byte 31: SDRAM Thermal and Refresh Options
- [D18F2x200_dct\[0\]_mp\[1:0\]\[Tras\]](#): Active to precharge time
- [D18F2x200_dct\[0\]_mp\[1:0\]\[Trp\]](#): Precharge time
- [D18F2x200_dct\[0\]_mp\[1:0\]\[Trcd\]](#): RAS to CAS delay
- [D18F2x200_dct\[0\]_mp\[1:0\]\[Tcl\]](#): CAS latency
- [D18F2x204_dct\[0\]_mp\[1:0\]\[Trtp\]](#): Internal read to precharge command delay time

- [D18F2x204_dct\[0\]_mp\[1:0\]](#)[FourActWindow]: Four activate window delay time
- [D18F2x204_dct\[0\]_mp\[1:0\]](#)[Trd]: Row active to row active delay
- [D18F2x204_dct\[0\]_mp\[1:0\]](#)[Trc]: Active to active/refresh time
- [D18F2x208_dct\[0\]](#)[Trfc3, Trfc2, Trfc1, Trfc0]: Refresh recovery delay time
- [D18F2x20C_dct\[0\]_mp\[1:0\]](#)[Twtr]: Internal write to read command delay time
- [D18F2x22C_dct\[0\]_mp\[1:0\]](#)[Twr]: Write recovery time

Optimal cycle time is specified for each DIMM and is used to limit or determine bus frequency. See [2.9.7.8 \[DRAM Device and Controller Initialization\]](#).

The DRAM data sheet or the JEDEC DRAM specification provides values for some DRAM timing parameters that are required by the DCT, regardless of whether the DRAMs are solder-down. Most of these parameters have a fixed time component as part of their specification. If memory P-states are supported (See [2.5.7.1 \[Memory P-states\]](#)) and a timing register does not have per memory P-state contexts, BIOS must evaluate the minimum value for each frequency and choose the most pessimistic value for all frequencies to program into the register. These parameters are:

- [D18F2x20C_dct\[0\]_mp\[1:0\]](#)[Tcw]: CAS write latency
- [D18F2x220_dct\[0\]](#)[Tmr]: MRS command cycle time
- [D18F2x220_dct\[0\]](#)[Tmod]: MRS command recovery time
- [D18F2x224_dct\[0\]](#)[Tzqcs]: Short calibration command recovery time
- [D18F2x224_dct\[0\]](#)[Tzqoper]: Long calibration command recovery time
- [D18F2x248_dct\[0\]_mp\[1:0\]](#)[Txpdll]: Exit precharge power down (with DLL frozen) to command delay.
- [D18F2x248_dct\[0\]_mp\[1:0\]](#)[Txp]: Exit precharge power down to command delay.
- [D18F2x24C_dct\[0\]](#)[Tcksrx]: Clock stable to self refresh exit delay
- [D18F2x24C_dct\[0\]](#)[Tcksre]: Self refresh entry to clock removal delay
- [D18F2x24C_dct\[0\]](#)[Tckesr]: Self refresh entry to command delay
- [D18F2x24C_dct\[0\]](#)[Tpd]: Power down entry to exit delay. BIOS may increase this value above the JEDEC minimum for certain power down modes.

2.9.7.6 Non-SPD ROM-Based Configuration

There are several DRAM timing parameters and DCT configurations that need to be programmed for optimal memory performance. These values are not derived from the SPD ROM. Several of these timing parameters are functions of other configuration values. These interdependencies must be considered when programming values into several DCT register timing fields. The factors to consider when specifying a value for a specific non-SPD timing parameter are:

- Training delay values. See [2.9.7.9 \[DRAM Training\]](#).
- Read and write latency differences.
- The phy's idle clock requirements on the data bus.
- DDR3 ODT timing requirements.
- NCLK frequency
- MEMCLK frequency

The following sub-sections describe how BIOS programs each non-SPD related timing field to a recommended minimum timing value with respect to the above factors.

The following terms are defined to simplify calculations and are calculated in MEMCLKs:

- Latency Difference (LD) = [D18F2x200_dct\[0\]_mp\[1:0\]](#)[Tcl] - [D18F2x20C_dct\[0\]_mp\[1:0\]](#)[Tcw].
• These equations assume [D18F2x200_dct\[0\]_mp\[1:0\]](#)[Tcl] >= [D18F2x20C_dct\[0\]_mp\[1:0\]](#)[Tcw].
- Read ODT Delay (ROD) = MAX(0, [D18F2x240_dct\[0\]_mp\[1:0\]](#)[RdOdtOnDuration] - 6).

- Write ODT Delay (WOD) = MAX(0, D18F2x240_dct[0]_mp[1:0][WrOdtOnDuration] - 6).
- WrEarly = ABS(D18F2x20C_dct[0]_mp[1:0][WrDqDqsEarly]) / 2

2.9.7.6.1 TrdrdSdSc, TrdrdSdDc, and TrdrdDd (Read to Read Timing)

The optimal values for D18F2x218_dct[0]_mp[1:0][TrdrdSdSc, TrdrdSdDc, TrdrdDd] are platform and configuration specific and should be characterized for best performance. Prior to DRAM training, BIOS should program these parameters to the largest defined value. After DRAM training, BIOS should use the guidelines below to configure the recommended platform generic timing values:

- TrdrdSdSc (in MEMCLKs) = 1.
- TrdrdSdDc (in MEMCLKs) = MAX(TrdrdSdSc, 3 + (IF (D18F2xA8_dct[0][PerRankTimingEn]) THEN CEIL(CDD_{TrdrdSdDc} / 2 + 0.5) ELSE 0 ENDIF)).
- TrdrdDd (in MEMCLKs) = MAX(TrdrdSdDc, ROD + 3, CEIL(CDD_{TrdrdDd}/2 + 3.5)).

The Critical Delay Difference (CDD) is the largest delay difference of the channel.

- Each delay difference is D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0][DqsRcvEnGrossDelay] minus D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0][DqsRcvEnGrossDelay].
- For CDD_{TrdrdSdDc}, the subtraction terms are the delays of different chip selects within the same DIMM within the same byte lane.
- For CDD_{TrdrdDd}, the subtraction terms are the delays of different DIMMs within the same byte lane.

2.9.7.6.2 TwrwrSdSc, TwrwrSdDc, TwrwrDd (Write to Write Timing)

The optimal values for D18F2x214_dct[0]_mp[1:0][TwrwrSdSc, TwrwrSdDc, TwrwrDd] are platform and configuration specific and should be characterized for best performance. Prior to DRAM training, BIOS should program these parameters to the largest defined value. After DRAM training, BIOS should use the guidelines below to configure the recommended platform generic timing values:

- TwrwrSdSc (in MEMCLKs) = 1.
- TwrwrSdDc (in MEMCLKs) = MAX(TwrwrSdSc, WOD + 3, 3 + (IF (D18F2xA8_dct[0][PerRankTimingEn]) THEN CEIL(CDD_{TwrwrSdDc} / 2 + 0.5) ELSE 0 ENDIF)).
- TwrwrDd (in MEMCLKs) = MAX(TwrwrSdDc, WOD + 3, CEIL(CDD_{TwrwrDd} / 2 + 3.5)).

The Critical Delay Difference (CDD) is the largest delay difference of the channel.

- Each delay difference is D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][WrDqsGrossDly] minus D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][WrDqsGrossDly].
- For CDD_{TwrwrSdDc}, the subtraction terms are the delays of different chip selects within the same DIMM within the same byte lane.
- For CDD_{TwrwrDd}, the subtraction terms are the delays of different DIMMs within the same byte lane.

2.9.7.6.3 Twrrd (Write to Read DIMM Termination Turn-around)

The optimal value for D18F2x218_dct[0]_mp[1:0][Twrrd] is platform and configuration specific and should be characterized for best performance. Prior to DRAM training, BIOS should program these parameters to the largest defined value. After DRAM training, BIOS should use the guidelines below to configure the recommended platform generic timing values:

- Twrrd (in MEMCLKs) = MAX(1, MAX(WOD, CEIL(CDD_{Twrrd} / 2 + 2 - WrEarly)) - LD + 3).

The Critical Delay Difference (CDD) is the largest delay difference of the channel.

- Each delay difference is D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][WrDqsGrossDly] minus

- For CDD_{Twrdd}, the subtraction terms are the delays of different chip selects within the same byte lane.

2.9.7.6.4 TrwtTO (Read-to-Write Turnaround for Data, DQS Contention)

The optimal value for D18F2x21C_dct[0]_mp[1:0][TrwtTO] is platform and configuration specific and should be characterized for best performance. Prior to DRAM training, BIOS should program this parameter to the largest defined value. After DRAM training, BIOS should use the guidelines below to configure the recommended platform generic timing values after DDR training is complete:

- TrwtTO (in MEMCLKs) = MAX(ROD, CEIL(CDD_{TrwtTO} / 2 + WrEarly)) + LD + 3.
- If 1 DIMM/ch, substitute ROD = 0 in the above equation. Assumes no DIMM ODT switching occurs.

The Critical Delay Difference (CDD) is the largest delay difference of the channel.

- Each delay difference is D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0][DqsRcvEnGrossDelay] minus D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][WrDqsGrossDly].
- For CDD_{TrwtTO}, the subtraction terms are the delays of all chip selects within the same byte lane.

2.9.7.6.5 DRAM ODT Control

BIOS configures the DIMM ODT behavior per chip select according to the DIMM population. The ODT pin patterns for reads and writes are programmed using D18F2x[234:230]_dct[0] and D18F2x[23C:238]_dct[0], respectively.

BIOS also configures the ODT pin pattern used during write leveling by programming D18F2x9C_x0000_0008_dct[0]_mp[1:0][WrLvOdtEn, WrLvOdt]. BIOS programs WrLvOdt with the D18F2x[23C:238]_dct[0] value provided for writes to the rank targeted by training. See 2.9.7.9.1 [Write Lev- elization Training].

Table 35: DDR3 ODT Pattern NumDimmSlots=1

DIMM0 ¹	D18F2x[234:230]_dct[0]		D18F2x[23C:238]_dct[0]	
	D18F2x234	D18F2x230	D18F2x23C	D18F2x238
SR	0000_0000h	0000_0000h	0000_0000h	0000_0001h
DR	0000_0000h	0000_0000h	0000_0000h	0000_0201h

1. DIMM0: BP_MEMCSx[1:0], BP_MEMODTx[1,0].

Table 36: DDR3 ODT Pattern NumDimmSlots=2

DIMM0 ¹	DIMM1 ¹	D18F2x[234:230]_dct[0]		D18F2x[23C:238]_dct[0]	
		D18F2x234	D18F2x230	D18F2x23C	D18F2x238
-	SR	0000_0000h	0000_0000h	0000_0000h	0004_0000h
-	DR	0000_0000h	0000_0000h	0000_0000h	0804_0000h
SR/DR	SR/DR	0000_0000h	0101_0404h	0000_0000h	0905_0605h

1. DIMM0: BP_MEMCSx[1:0], BP_MEMODTx[1,0].
DIMM1: BP_MEMCSx[3:2], BP_MEMODTx[3,2].

2.9.7.6.5.1 DRAM ODT Configuration

These tables document the optimal settings for motherboards which meet the relevant AMD motherboard design guidelines. See [2.9.2 \[DCT Frequency Support\]](#) for an overview of the DIMM population and memory bus speed support.

Table 37: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **UDIMM FT3 package**

Condition					MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	RttNom	RttWr
1	667, 800, 1066	1.5	SR, DR	-	010b	00b
1	1333, 1600, 1866	1.5	SR, DR	-	001b	00b
2	667, 800, 1066	1.5	NP	SR, DR	010b	00b
2	667, 800	1.5	SR, DR	SR, DR	011b	10b
2	1066, 1333	1.5	SR, DR	SR, DR	101b	10b
2	1333, 1600, 1866	1.5	NP	SR, DR	001b	00b
2	1600	1.5	SR, DR	SR, DR	100b	01b

Table 38: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **SODIMM FT3 package**

Condition					MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	RttNom	RttWr
1	667, 800, 1066	1.5, 1.35, 1.25	SR, DR	-	010b	00b
1	1333	1.5, 1.35, 1.25	SR, DR	-	001b	00b
1	1600	1.5, 1.35	SR, DR	-	001b	00b
2	667, 800, 1066	1.5, 1.35, 1.25	NP	SR, DR	010b	00b
2	667, 800	1.5, 1.35, 1.25	SR, DR	SR, DR	011b	10b
2	1066, 1333	1.5, 1.35, 1.25	SR, DR	SR, DR	101b	10b
2	1333	1.5, 1.35, 1.25	NP	SR, DR	001b	00b
2	1600	1.5, 1.35	NP	SR, DR	001b	00b
2	1600	1.5	SR, DR	SR, DR	100b	01b
2	1600	1.35	SR	SR	100b	01b

Table 39: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **SODIMM** plus **Solder-down DRAM** FT3 package

Condition					MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	RttNom	RttWr
2	667, 800, 1066	1.5, 1.35, 1.25	NP	SR, DR	010b	00b
2	667, 800	1.5, 1.35, 1.25	SR, DR	SR, DR	011b	10b
2	1066	1.5, 1.35, 1.25	SR, DR	SR, DR	101b	10b
2	1333	1.5, 1.35	NP	SR, DR	001b	00b
2	1333	1.5	SR, DR	SR, DR	101b	10b
2	1333	1.35	SR	SR	101b	10b

Table 40: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **Solder-down DRAM** FT3 package

Condition				MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	RttNom	RttWr
1	667	1.5, 1.35, 1.25	SR, DR	000b	00b
1	800, 1066	1.5, 1.35, 1.25	SR, DR	010b	00b
1	1333	1.5, 1.35, 1.25	SR, DR	001b	00b
1	1600	1.5, 1.35	SR, DR	001b	00b
1	1866	1.5	SR, DR	001b	00b

Table 41: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **UDIMM** FS1b package

Condition					MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	RttNom	RttWr
1	667, 800, 1066	1.5, 1.35, 1.25	SR, DR	-	010b	00b
1	1333, 1600	1.5, 1.35, 1.25	SR, DR	-	001b	00b
2	667, 800, 1066	1.5, 1.35, 1.25	NP	SR, DR	010b	00b
2	667, 800	1.5, 1.35, 1.25	SR, DR	SR, DR	011b	10b

Table 41: BIOS recommendations for MR1[RttNom] and MR2[RttWr] **UDIMM FS1b package**

Condition					MR1	MR2
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	RttNom	RttWr
2	1066, 1333	1.5, 1.35, 1.25	SR, DR	SR, DR	101b	10b
2	1333, 1600	1.5, 1.35, 1.25	NP	SR, DR	001b	00b
2	1600	1.5, 1.35	SR, DR	SR, DR	100b	01b

2.9.7.6.6 DRAM Address Timing and Output Driver Compensation Control

This section describes the settings required for programming the timing on the address pins, the CS/ODT pins, and the CKE pins. The following tables document the address timing and output driver settings on a per channel basis for DDR3. These tables document the optimal settings for motherboards which meet the relevant AMD socket motherboard design guidelines. See [2.9.2 \[DCT Frequency Support\]](#) for an overview of the DIMM and memory bus speed support.

When POdtOff=0, in all cases the processor ODT is off for writes and is on for reads.

Table 42: BIOS recommendations for SlowAccessMode, PODtOff, Addr/Cmd Timings and Output Driver Control **UDIMM FT3** package

Condition					D18F2x9C_x0000_0000_dct[0].mp[1:0]
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	D18F2x9C_x0000_0004_dct[0].mp[1:0]
					D18F2x9C_x0D0F_0[F,8:0]04_dct[0].mp[1:0]
					D18F2x94_dct[0]
1	667, 800	1.5	SR, DR	-	0 0 0000000h 00002222h
1	1066	1.5	SR	-	0 0 003D3D3Dh 10002222h
1	1066	1.5	DR	-	0 0 0000000h 10002222h
1	1333	1.5	SR	-	0 0 003D3D3Dh 20112222h
1	1333	1.5	DR	-	0 0 00003D3Dh 20112222h
1	1600, 1866	1.5	SR	-	0 0 003C3C3Ch 30332222h
1	1600, 1866	1.5	DR	-	1 0 00003C3Ch 30332222h
2	667, 800	1.5	NP	SR, DR	0 0 0000000h 00002222h
2	667	1.5	SR, DR	SR, DR	1 0 0000000h 10222323h
2	800	1.5	SR, DR	SR, DR	1 0 0000000h 20222323h
2	1066	1.5	NP	SR	0 0 003D3D3Dh 10002222h
2	1066	1.5	NP	DR	0 0 0000000h 10002222h
2	1066, 1333, 1600	1.5	SR, DR	SR, DR	1 0 0000000h 30222323h
2	1333	1.5	NP	SR	0 0 003D3D3Dh 20112222h
2	1333	1.5	NP	DR	0 0 00003D3Dh 20112222h

Table 42: BIOS recommendations for SlowAccessMode, POdtOff, Addr/Cmd Timings and Output Driver Control **UDIMM** FT3 package

Condition					D18F2x9C_x0000_0000_dct[0]_mp[1:0]		
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	D18F2x9C_x0D0F_0[F,8:0]04_dct[0]_mp[1:0]	POdtOff	
2	1600, 1866	1.5	NP	SR	0	0	003C3C3Ch 30332222h
2	1600, 1866	1.5	NP	DR	1	0	00003C3Ch 30332222h

Table 43: BIOS recommendations for SlowAccessMode, PODtOff, Addr/Cmd Timings and Output Driver Control **SODIMM FT3 package**

Condition					D18F2x9C_x0000_0000_dct[0].mp[1:0]
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	D18F2x9C_x0000_0004_dct[0].mp[1:0]
					D18F2x9C_x0D0F_0[F,8:0]04_dct[0].mp[1:0]
					D18F2x94_dct[0]
					SlowAccessMode
					POdtOff
1	667, 800	1.5, 1.35, 1.25	SR, DR	-	0 0 0000000h 00002222h
1	1066	1.5, 1.35, 1.25	SR	-	0 0 003D3D3Dh 10002222h
1	1066	1.5, 1.35, 1.25	DR	-	0 0 0000000h 10002222h
1	1333	1.5, 1.35, 1.25	SR	-	0 0 003D3D3Dh 20112222h
1	1333	1.5, 1.35, 1.25	DR	-	0 0 00003D3Dh 20112222h
1	1600	1.5, 1.35	SR	-	0 0 003C3C3Ch 30332222h
1	1600	1.5, 1.35	DR	-	1 0 00003C3Ch 30332222h
2	667, 800	1.5, 1.35, 1.25	NP	SR, DR	0 0 0000000h 00002222h
2	667	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 10222323h
2	800	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 20222323h
2	1066	1.5, 1.35, 1.25	NP	SR	0 0 003D3D3Dh 10002222h
2	1066	1.5, 1.35, 1.25	NP	DR	0 0 0000000h 10002222h
2	1066, 1333	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 30222323h
2	1333	1.5, 1.35, 1.25	NP	SR	0 0 003D3D3Dh 20112222h
2	1333	1.5, 1.35, 1.25	NP	DR	0 0 00003D3Dh 20112222h
2	1600	1.5, 1.35	NP	SR	0 0 003C3C3Ch 30332222h
2	1600	1.5, 1.35	NP	DR	1 0 00003C3Ch 30332222h
2	1600	1.5	SR, DR	SR, DR	1 0 0000000h 30222323h

Table 43: BIOS recommendations for SlowAccessMode, POdtOff, Addr/Cmd Timings and Output Driver Control **SODIMM FT3 package**

Condition				D18F2x9C_x0000_0000_dct[0]_mp[1:0]			
				D18F2x9C_x0000_0004_dct[0]_mp[1:0]			
				D18F2x9C_x0D0F_0[F,8:0]04_dct[0]_mp[1:0]			
				POdtOff			
				D18F2x94_dct[0]			
				SlowAccessMode			
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	1	0	00000000h
2	1600	1.35	SR	SR			30222323h

Table 44: BIOS recommendations for SlowAccessMode, PODtOff, Addr/Cmd Timings and Output Driver Control **SODIMM plus Solder-down DRAM FT3 package**

Condition					D18F2x9C_x0000_0000_dct[0].mp[1:0]			
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	D18F2x9C_x0D0F_0[F,8:0]04_dct[0].mp[1:0]	POdtOff	D18F2x94_dct[0]	SlowAccessMode
2	667, 800	1.5, 1.35, 1.25	NP	SR, DR	0 0	00000000h	00002222h	
2	667	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0	00000000h	10222323h	
2	800	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0	00000000h	20222323h	
2	1066	1.5, 1.35, 1.25	NP	SR	0 0	003D3D3Dh	10002222h	
2	1066	1.5, 1.35, 1.25	NP	DR	0 0	00000000h	10002222h	
2	1066	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0	00000000h	30222323h	
2	1333	1.5, 1.35	NP	SR	0 0	003D3D3Dh	20112222h	
2	1333	1.5, 1.35	NP	DR	0 0	00003D3Dh	20112222h	
2	1333	1.5	SR, DR	SR, DR	1 0	00000000h	30222323h	
2	1333	1.35	SR	SR	1 0	00000000h	30222323h	

Table 45: BIOS recommendations for SlowAccessMode, POdtOff, Addr/Cmd Timings and Output Driver Control **Solder-down DRAM FT3 package**

Condition				D18F2x9C_x0000_0000_dct[0]_mp[1:0]			
NumDimmSlots	DdrRate	VDDIO	DIMM0	D18F2x9C_x0000_0004_dct[0]_mp[1:0]			
				D18F2x9C_x0D0F_0FF,8:0]04_dct[0]_mp[1:0]			
1	667	1.5, 1.35, 1.25	SR, DR	0	1	00000000h	00000000h
1	800	1.5, 1.35, 1.25	SR, DR	0	0	00000000h	00000000h
1	1066	1.5, 1.35, 1.25	SR	0	0	003D3D3Dh	10000000h
1	1066	1.5, 1.35, 1.25	DR	0	0	00000000h	10000000h
1	1333	1.5, 1.35, 1.25	SR	0	0	003D3D3Dh	20000000h
1	1333	1.5, 1.35, 1.25	DR	0	0	00003D3Dh	20110000h
1	1600	1.5, 1.35	SR	0	0	003C3C3Ch	30110000h
1	1600	1.5, 1.35	DR	1	0	00003C3Ch	30110000h

Table 46: BIOS recommendations for SlowAccessMode, PODtOff, Addr/Cmd Timings and Output Driver Control **UDIMM FS1b** package

Condition					D18F2x9C_x0000_0000_dct[0].mp[1:0]
NumDimmSlots	DdrRate	VDDIO	DIMM0	DIMM1	D18F2x9C_x0000_0004_dct[0].mp[1:0]
					D18F2x9C_x0D0F_0[F,8:0]04_dct[0].mp[1:0]
					D18F2x94_dct[0]
					SlowAccessMode
					PODtOff
1	667, 800	1.5, 1.35, 1.25	SR, DR	-	0 0 0000000h 00002222h
1	1066	1.5, 1.35, 1.25	SR	-	0 0 003D3D3Dh 10002222h
1	1066	1.5, 1.35, 1.25	DR	-	0 0 0000000h 10002222h
1	1333	1.5, 1.35, 1.25	SR	-	0 0 003D3D3Dh 20112222h
1	1333	1.5, 1.35, 1.25	DR	-	0 0 00003D3Dh 20112222h
1	1600	1.5, 1.35, 1.25	SR	-	0 0 003C3C3Ch 30332222h
1	1600	1.5, 1.35, 1.25	DR	-	1 0 00003C3Ch 30332222h
2	667, 800	1.5, 1.35, 1.25	NP	SR, DR	0 0 0000000h 00002222h
2	667	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 10222323h
2	800	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 20222323h
2	1066	1.5, 1.35, 1.25	NP	SR	0 0 003D3D3Dh 10002222h
2	1066	1.5, 1.35, 1.25	NP	DR	0 0 0000000h 10002222h
2	1066, 1333	1.5, 1.35, 1.25	SR, DR	SR, DR	1 0 0000000h 30222323h
2	1333	1.5, 1.35, 1.25	NP	SR	0 0 003D3D3Dh 20112222h
2	1333	1.5, 1.35, 1.25	NP	DR	0 0 00003D3Dh 20112222h
2	1600	1.5, 1.35, 1.25	NP	SR	0 0 003C3C3Ch 30332222h
2	1600	1.5, 1.35, 1.25	NP	DR	1 0 00003C3Ch 30332222h
2	1600	1.5, 1.35	SR, DR	SR, DR	1 0 0000000h 30222323h

2.9.7.7 DCT Training Specific Configuration

The DCT requires certain features be disabled during DRAM device initialization and training. BIOS should program the registers in [Table 47](#) before DRAM device initialization and training. For normal operation, BIOS programs the recommended values if provided in [Table 47](#). BIOS must quiesce all other forms of DRAM traffic on the channel being trained. See [2.9.7 \[DCT/DRAM Initialization and Resume\]](#).

Table 47: DCT Training Specific Register Values

Register	Training	Normal Operation
D18F2x78_dct[0][AddrCmdTriEn]	0	1
D18F2x8C_dct[0][DisAutoRefresh]	1	0
D18F2x90_dct[0][ForceAutoPchg]	0	0
D18F2x90_dct[0][DynPageCloseEn]	0	0
D18F2x94_dct[0][BankSwizzleMode]	0	1
D18F2x94_dct[0][DcqBypassMax]	0	1Fh
D18F2x94_dct[0][PowerDownEn]	0	1
D18F2x94_dct[0][ZqcsInterval]	00b	10b
D18F2x9C_x0000_000D_dct[0]_mp[1:0][RxMax-DurDlNoLock]	000b	See 2.9.7.10
D18F2x9C_x0000_000D_dct[0]_mp[1:0][TxMax-DurDlNoLock]	000b	See 2.9.7.10
D18F2x9C_x0D0F_0[F,8:0]10_dct[0]_mp[1:0][En RxPadStandby]	0	See 2.9.7.10
D18F2xA4[CmdThrottleMode]	000b	See 2.9.12
D18F2xA4[ODTSEn]	000b	See 2.9.12
D18F2xA4[BwCapEn]	0	See 2.9.12
D18F2xA8_dct[0][BankSwap]	0	1
D18F3x58[DramScrub] ²	0	See 2.14.1.8
D18F3x5C[ScrubReDirEn] ²	0	IF (D18F3x44[DramEc- cEn]==1) THEN 1 ELSE 0 ENDIF
1. Programmed specific to the current platform or memory configuration. 2. BIOS must quiesce all other forms of DRAM traffic on the channel when performing writes via D18F2x98_dct[0] . See also D18F3x88[DisDramScrub] .		

2.9.7.8 DRAM Device and Controller Initialization

BIOS initializes the DRAM devices and the controller using either a hardware or a software controlled sequence. Hardware init is supported for verification only. See [2.10.8.8.1 \[Hardware DDR3 Device Initialization\]](#) and [2.9.7.8.1 \[Software DDR3 Device Initialization\]](#).

BIOS must observe additional requirements for changing the PLL frequency when setting [D18F2x90_dct\[0\]\[InitDram\]](#) or [D18F2x7C_dct\[0\]\[EnDramInit\]](#). See [2.9.7.4.2 \[DRAM Channel Frequency](#)

[Change](#).

DRAM initialization is complete after the value of [D18F2x90_dct\[0\]\[InitDram\]](#) transitions from 1 to 0 in the hardware-controlled sequence or the value of [D18F2x7C_dct\[0\]\[EnDramInit\]](#) is written by BIOS from 1 to 0 in the software-controlled sequence.

2.9.7.8.1 Software DDR3 Device Initialization

BIOS should apply the following procedure to each DCT to initialize the DDR3 DIMMs on the channel. This procedure should be run only when booting from an unpowered state (ACPI S4, S5 or G3; not S3, suspend to RAM).

1. Program [D18F2x7C_dct\[0\]\[EnDramInit\]](#) = 1.
2. Wait 200 us.
3. Program [D18F2x7C_dct\[0\]\[DeassertMemRstX\]](#) = 1.
4. Wait 500 us.
5. Program [D18F2x7C_dct\[0\]\[AssertCke\]](#) = 1.
6. Wait 360 ns.
7. Send MRS(2).
8. Send MRS(3). Ordinarily at this time, MrsAddress[2:0] = 000b.
9. Send MRS(1) with MrsAddress[7] = 0 (write leveling disabled).
10. Send MRS(0) with MrsAddress[8] = 1 (reset the DLL).
11. Send two ZQCL commands.
- BIOS instructs the DCT to send a ZQCL command by programming [D18F2x7C_dct\[0\]](#) as follows:
 - Program MrsAddress[10] = 1.
 - Program SendZQCmd = 1.
 - Wait for SendZQCmd = 0.
 - Wait 512 MEMCLKs.
12. Program [D18F2x7C_dct\[0\]\[EnDramInit\]](#) = 0.
13. Program [D18F2x2E8_dct\[0\]_mp\[1:0\]](#), [D18F2x2EC_dct\[0\]_mp\[1:0\]](#) with a copy of the mode register data sent in the steps above, except with [MR0\[DLL\]](#) = 0 (Do not reset the DRAM DLL with a memory P-state change).

2.9.7.8.1.1 DDR3 MR Initialization

BIOS instructs the DCT to send MRS commands by programming [D18F2x7C_dct\[0\]](#) as follows:

1. Program MrsBank and MrsAddress as specified below:
 - MrsBank[2:0] = BA2:BA0.
 - MrsAddress[15:0] = A15:A0.
 - BIOS may need to remap bits, see also [D18F2x\[5C:40\]_dct\[0\]\[OnDimmMirror\]](#).
 - Set all other bits in MrsAddress to zero. BIOS should write reserved fields as 0.
2. Program MrsChipSel as appropriate.
3. Program SendMrsCmd = 1.
4. Wait for SendMrsCmd = 0.

MR0 DDR3 MR0Table 48: BIOS Recommendations for **MR0[WR]**

Condition	MR0
D18F2x22C_dct[0]_mp[1:0][Twr]	WR[3:0]
10h	0000b
5h	0001b
6h	0010b
7h	0011b
8h	0100b
Ah	0101b
Ch	0110b
Eh	0111b
12h	1001b

Table 49: BIOS Recommendations for **MR0[CL[3:0]]**

Condition	MR0
D18F2x200_dct[0]_mp[1:0][Tcl]	CL[3:0]
5h	2h
6h	4h
7h	6h
8h	8h
9h	Ah
Ah	Ch
Bh	Eh
Ch	1h
Dh	3h
Eh	5h
Fh	7h
10h	9h
11h	Bh

Bits	Description
15:14	Reserved.
13	WR[3]: write recovery for autoprecharge. See WR[2:0].
12	PPD: DLL control for precharge powerdown. BIOS: D18F2x84_dct[0][PchgPDModeSel].
11:9	WR[2:0]: write recovery for autoprecharge. WR[3:0] = {WR[3], WR[2:0]}. BIOS: Table 48 .
8	DLL: DLL reset. BIOS: See 2.9.7.8.1 .
7	TM: test mode. BIOS: 0.
6:4	CL[3:1]. CAS latency. See: CL[0].

3	RBT: read burst type. BIOS: 1.
2	CL[0]. CAS latency. CL[3:0] = {CL[3:1], CL[0]}. BIOS: Table 49 .
1:0	BL: burst length. BIOS: D18F2x84_dct[0][BurstCtrl] .

MR1 DDR3 MR1

Bits	Description
15:13	Reserved.
12	Qoff: Qoff. BIOS: See 2.9.7.9.1 . See also D18F2x84_dct[0][Qoff] .
11	TDQS: TDQS enable. BIOS: 0. See D18F2x94_dct[0][RDqsEn] .
10	Reserved.
9	RttNom[2]: RttNom. See: RttNom[0].
8	Reserved.
7	Level: write leveling enable. BIOS: See 2.9.7.9.1 .
6	RttNom[1]: RttNom. See: RttNom[0].
5	DIC[1]: output driver impedance control. See: DIC[0].
4:3	AL: additive latency. BIOS: 0.
2	RttNom[0]: RttNom. RttNom[2:0] = {RttNom[2], RttNom[1], RttNom[0]}. BIOS: See 2.9.7.6.5.1
1	DIC[0]: output driver impedance control. DIC[1:0] = {DIC[1], DIC[0]}. BIOS: 01b.
0	DLL: DLL enable. BIOS: 0.

MR2 DDR3 MR2Table 50: BIOS Recommendations for [MR2\[ASR, SRT\]](#)

Condition		MR2	
AutoSelfRefresh	ExtendedTemperature-Range	ASR	SRT
0	0	0	0
0	1	0	1
1	-	1	0

Bits	Description
15:11	Reserved. MR2
10:9	RttWr: RttWr. BIOS: See 2.9.7.6.5.1 . See also D18F2x84_dct[0][DramTermDyn] .
8	Reserved.
7	SRT: self refresh temperature range. BIOS: Table 50 . See D18F2x84_dct[0][SRT] .
6	ASR: auto self refresh. BIOS: Table 50 . See D18F2x84_dct[0][ASR] .
5:3	CWL: CAS write latency. BIOS: D18F2x20C_dct[0][mp[1:0][Tcwl]] - 5 .
2:0	PASR: partial array self refresh. BIOS: 0.

MR3 DDR3 MR3

Bits	Description
15:3	Reserved.
2	MPR: MPR operation. BIOS: 0.
1:0	MPRLoc: MPR location. BIOS: 0.

2.9.7.9 DRAM Training

This section describes detailed methods used to train the processor DDR interface to DRAM for optimal functionality and performance. DRAM training is performed by BIOS after initializing the DRAM controller. See [2.9.7.8 \[DRAM Device and Controller Initialization\]](#).

Some of the DRAM training steps described in this section require two passes if the target MEMCLK frequency is greater than 333 MHz. For optimal software performance, software may defer the second pass (at target MEMCLK frequency) for each training step until after the first pass (at lowest supported frequency) of all other training steps are complete. See [D18F2x94_dct\[0\]\[MemClkFreq\]](#).

Product specific training requirements are as follows:

- Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[TrNibbleSel\]=0](#).
- Program [D18F2xA8_dct\[0\]\[PerRankTimingEn\]=1](#).

See [2.9.7.7 \[DCT Training Specific Configuration\]](#) for additional training requirements.

In the following subsections, lane is used to describe an 8-bit wide data group, each with its own timing control.

2.9.7.9.1 Write Levelization Training

Write levelization involves using the phase recovery engine in the phy to detect the edge of DQS with respect to the memory clock on the DIMM for write accesses to each lane.

Training is accomplished on a per channel, per rank basis. If the target frequency is greater than 333 MHz then BIOS performs two passes; otherwise, only one pass is required. See [2.9.7.4.2 \[DRAM Channel Frequency Change\]](#).

- Pass 1: Configure the memory subsystem for 333 MHz MEMCLK frequency.
- Pass 2: Configure the memory subsystem for the target MEMCLK frequency. BIOS must reconfigure the phy and the DRAM devices to the new target frequency.

The following describes the steps used for each pass of write levelization training for each channel:

For each rank:

1. Prepare the DIMMs for write levelization using DDR3-defined MR commands.
 - A. Configure the output driver and on-die termination of the target DIMM as follows:
 - For the target rank of the target DIMM, enable write leveling mode and enable the output driver.
 - For all other ranks of the target DIMM, enable write leveling mode and disable the output driver.

- For two or more DIMMs per channel, program Rtt_Nom of the target rank to the corresponding specified Rtt_Wr termination. Otherwise, configure Rtt_Nom of the target DIMM as normal. See [2.9.7.6.6 \[DRAM Address Timing and Output Driver Compensation Control\]](#).
- B. Configure Rtt_Nom on the non-target DIMMs as normal. See [2.9.7.6.6 \[DRAM Address Timing and Output Driver Compensation Control\]](#).
2. Wait 40 MEMCLKs to satisfy DDR3-defined internal DRAM timing parameters tWLMRD, tWLQDEN, and tWLQSEN.
 3. Configure the phy for write leveling training:
 - A. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrtLvTrEn\]=0](#).
 - B. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[TrChipSel\]](#) to specify the target rank to be trained.
 - C. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrLvOdt\]](#) to the proper ODT settings for the current memory subsystem configuration. See [2.9.7.6.5 \[DRAM ODT Control\]](#).
 - D. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrLvOdtEn\]=1](#).
 - E. MFENCE.
 - F. Wait 10 MEMCLKs to allow for ODT signal settling.
 - G. For each lane program an initial value to registers [D18F2x9C_x0000_00\[52:50\]_dct\[0\]](#) to set the gross and fine delay. See [2.9.7.9.1.1 \[Write Leveling Seed Value\]](#).
 4. Perform write leveling of the devices on the DIMM:
 - A. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrtLvTrEn\]=1](#).
 - B. MFENCE.
 - C. Wait 200 MEMCLKs.
 - D. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrtLvTrEn\]=0](#).
 - E. Read from registers [D18F2x9C_x0000_00\[52:50\]_dct\[0\]](#) to get the gross and fine delay settings for the target DIMM and save these values.
 5. Disable write leveling training so that the phy stops driving write leveling ODT.
 - A. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]\[WrLvOdtEn\]=0](#).
 - B. MFENCE.
 - C. Wait 10 MEMCLKs to allow for ODT signal settling.
 6. Program the target DIMM back to normal operation by configuring the following:
 - A. Configure all ranks of the target DIMM for normal operation.
 - B. Enable the output drivers of all ranks of the target DIMM.
 - C. For a two or more DIMM system, program the Rtt_Nom value for the target DIMM to the normal operating termination.

For each rank:

- BIOS calculates and programs the final saved gross and fine delay values for each lane into [D18F2x9C_x0000_00\[4A:30\]_dct\[0\]_mp\[1:0\] \[DRAM DQS Write Timing\]](#).
 - WrDqsFineDly = PhRecFineDly.
 - GrossDly = SeedGross + PhRecGrossDly - SeedPreGross.
 - The Critical Gross Delay (CGD) is the minimum GrossDly of all byte lanes and all DIMMs.
 - If (CGD < 0) Then
 - [D18F2x20C_dct\[0\]_mp\[1:0\]\[WrDqDqsEarly\]](#) = ABS(CGD)
 - WrDqsGrossDly = GrossDly + WrDqDqsEarly
 - Else
 - [D18F2x20C_dct\[0\]_mp\[1:0\]\[WrDqDqsEarly\]](#) = 1.
 - WrDqsGrossDly = GrossDly + 1.

2.9.7.9.1.1 Write Leveling Seed Value

The seed value for pass 1 of write leveling is design and platform specific. The seed value represents the actual clock delay and is platform dependent. The platform vendor may need to characterize and adjust this value for

proper write leveling training. The seed delay value must fall within +/- 1/2 MEMCLK, including silicon PVT margin and jitter of the measured clock delay.

1. Calculate the total seed based on the following:
 - Pass 1: SeedTotal = configuration specific seed value found in [Table 51](#).
 - Pass N:
 - SeedTotalPreScaling = the total delay values obtained from the previous (N-1) pass of write leveling training.
 - Write Leveling Total Delay = [D18F2x9C_x0000_00\[4A:30\]_dct\[0\]_mp\[1:0\]\[WrDqsGrossDly, WrDqsFineDly\]](#) - (0x20 * [D18F2x20C_dct\[0\]_mp\[1:0\]\[WrDqDqsEarly\]](#))
 - SeedTotal = SeedTotalPreScaling*(target frequency)/(frequency from previous pass).
2. SeedGross = SeedTotal DIV 32.
3. SeedFine = SeedTotal MOD 32.
4. If (SeedGross is odd)

then SeedPreGross = 1

else SeedPreGross = 2. Only LSB is used to effect starting PRE gross delay. Setting MSB allows the phase recovery engine a positive and negative adjustment range.
5. Program [D18F2x9C_x0000_00\[52:50\]_dct\[0\]\[PhRecFineDly\]](#) = SeedFine.
6. Program [D18F2x9C_x0000_00\[52:50\]_dct\[0\]\[PhRecGrossDly\]](#) = SeedPreGross.

Table 51: DDR3 Write Leveling Seed Values

DIMM Type	Seed Value ¹
Solder-down DRAM	0Eh
SODIMM	0Eh
UDIMM	15h
1. DDR3-667 (333 MHz).	

2.9.7.9.2 DQS Receiver Enable Training

Receiver enable delay training is used to dynamically determine the optimal delay value for [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#) [DRAM DQS Receiver Enable Timing]. The optimal DQS receiver enable delay value is platform and load specific, and occurs in the middle of a received read preamble. The timing of the preamble includes the inbound DQS propagation delay, which is unknown by BIOS. The training for delay values involves:

1. Configuring the phy PRE for an initial expected phase value (seed).
2. Generating a stream of read DQS edges from the DRAM by issuing multiple read commands.
3. The phy PRE determining the phase between the received DQS edges and a reference clock.
4. Calculating a final delay value for enabling receivers during normal read operations using the phase determined by the phy PRE.

Prior to DQS Receiver Enable Training, BIOS must program [D18F2x210_dct\[0\]_nbp\[3:0\]\[MaxRdLatency\]](#) based on the seeded value of [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#). See [2.9.7.9.5 \[Calculating MaxRdLatency\]](#).

Training is accomplished on a per channel, per rank basis. If the target frequency is greater than 333 MHz then BIOS performs two passes; otherwise only one pass is required. See [2.9.7.4.2 \[DRAM Channel Frequency\]](#)

[Change].

- Pass 1: Configure the memory subsystem for 333 MHz MEMCLK frequency.
- Pass 2: Configure the memory subsystem for the target MEMCLK frequency. BIOS must reconfigure the phy and the DRAM devices to the new target frequency.

The following describes the steps used for each pass of receiver enable training for each channel:

For each rank:

1. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[TrChipSel] to specify the target rank to be trained.
2. For each lane program an initial value to registers [D18F2x9C_x0000_00\[52:50\]_dct\[0\]](#) to set the gross and fine delay as specified in [2.9.7.9.2.1 \[DQS Receiver Enable Training Seed Value\]](#).
3. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[DqsRcvTrEn]=1.
4. Issue 192 read requests to the target rank. See [2.9.8 \[Continuous Pattern Generation\]](#).
5. Program [D18F2x9C_x0000_0008_dct\[0\]_mp\[1:0\]](#)[DqsRcvTrEn]=0.
6. Read [D18F2x9C_x0000_00\[52:50\]_dct\[0\]](#)[PhRecGrossDly, PhRecFineDly] to get the gross and fine delay values for each lane.
7. For each lane, calculate and program the corresponding receiver enable delay values for [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#)[DqsRcvEnGrossDelay, DqsRcvEnFineDelay]. Save the result for use later.
 - DqsRcvEnFineDelay = PhRecFineDly.
 - DqsRcvEnGrossDelay = SeedGross + PhRecGrossDly - SeedPreGross + 1. “+1” to add 1 UI to enable the receiver in the mid point of preamble.

2.9.7.9.2.1 DQS Receiver Enable Training Seed Value

The seed value for pass 1 of receiver enable delay training is design and platform specific and should be determined by characterization for best performance. The seed value represents the total delay from a reference point to the first expected rise edge of DQS on a read CAS measured at the processor pins, in 1 UI/32 increments. The reference point is defined as the clock in which CAS is asserted + CL - 1.

The following steps are taken to determine the seed values needed to program the DRAM Phase Recovery Control Registers:

For each pass and each lane:

1. Calculate the total seed based on the following:
 - Pass 1: SeedTotal = The seed value found in [Table 52](#) + the total delay values obtained from the first pass of write leveling training. See [2.9.7.9.1 \[Write Levelization Training\]](#).
 - Write Leveling Total Delay = [D18F2x9C_x0000_00\[4A:30\]_dct\[0\]_mp\[1:0\]](#)[WrDqsGrossDly, WrDqsFineDly] - (0x20 * [D18F2x20C_dct\[0\]_mp\[1:0\]](#)[WrDqDqsEarly])
 - Pass N:
 - RegisterDelay = 0
 - SeedTotalPreScaling = (the total delay values in [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#) from the previous (N-1) pass of training) - RegisterDelay - 20h. Stored value was adjusted 1 UI to enable the receiver in the mid point of preamble. Subtract 1 UI to get back to the preamble left edge.
 - SeedTotal = RegisterDelay + FLOOR(SeedTotalPreScaling*(target frequency)/(frequency from previous pass)).
2. SeedGross = SeedTotal DIV 32.
3. SeedFine = SeedTotal MOD 32.
4. If (SeedGross is odd)

then SeedPreGross =1

else SeedPreGross = 2. Only LSB is used to effect starting PRE gross delay. Setting MSB allows the phase recovery engine a positive and negative adjustment range.

5. Program [D18F2x9C_x0000_00\[52:50\]_dct\[0\]\[PhRecFineDly\]](#) = SeedFine.
6. Program [D18F2x9C_x0000_00\[52:50\]_dct\[0\]\[PhRecGrossDly\]](#) = SeedPreGross.
7. Program [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]\[DqsRcvEnGrossDelay\]](#) = IF ((NBCOF / DdrRate < 1) && (D18F2x200_dct[0]_mp[1:0][Tcl]=5) && (SeedGross<1) THEN 1 ELSE SeedGross ENDIF.

Table 52. DDR3 DQS Receiver Enable Training Seed Values

DIMM Type	Seed Value ¹
Solder-down DRAM	Char.Temp:20h
SODIMM	Char.Temp:32h
UDIMM	Char.Temp:32h
1. DDR3-667 (333 MHz)	

2.9.7.9.3 DQS Receiver Enable Cycle Training

Receiver enable delay cycle training is used to train the gross delay settings of [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#) to the middle of the received read preamble using the phy PRE phase results.

For each rank and lane:

1. Program [D18F2x9C_x0D0F_0\[F,8:0\]30_dct\[0\]\[BlockRxDqsLock\]](#) = 1.
2. RxEnOrig = [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]\[DqsRcvEnGrossDelay, DqsRcvEnFineDelay\]](#) result from [2.9.7.9.2 \[DQS Receiver Enable Training\]](#). (expected mid-preamble position based on the seed)
3. RxEnOffset = MOD(RxEnOrig + 10h, 40h) (offset by 1/4 MEMCLK, keep only the phase)
4. For each DqsRcvEn value beginning from RxEnOffset incrementing by 1 MEMCLK:
 - A. Program [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]\[DqsRcvEnGrossDelay, DqsRcvEnFineDelay\]](#) with the current value.
 - B. Perform [2.9.7.9.4 \[DQS Position Training\]](#).
 - Record the result for the current DqsRcvEn setting as a pass or fail depending if a data eye is found.
5. Process the array of results and determine a pass-to-fail transition. (Consider a pass in the last array element as a pass-to-fail transition)
 - A. DqsRcvEnCycle = the total delay value of the pass result.
 - B. Program [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]\[DqsRcvEnGrossDelay, DqsRcvEnFineDelay\]](#) = DqsRcvEnCycle - 10h. (subtract 1/4 MEMCLK to place the final DqsRcvEn mid-preamble)
6. Program [D18F2x9C_x0D0F_0\[F,8:0\]30_dct\[0\]\[BlockRxDqsLock\]](#) = 0.

2.9.7.9.4 DQS Position Training

DQS position training is used to place the DQS strobe in the center of the read DQ data eye and to center the write DQ data eye across the write DQS strobe. Determining the correct DRAM DQS and DQ delay settings for both reads and writes is conducted by performing a two dimensional search of the delay settings found in [D18F2x9C_x0000_0\[3:0\]0\[7:5\]_dct\[0\]_mp\[1:0\]](#) [DRAM Read DQS Timing] and [D18F2x9C_x0000_0\[3:0\]0\[3:1\]_dct\[0\]_mp\[1:0\]](#) [DRAM Write Data Timing].

Training is accomplished on a per channel, per rank, and per lane basis.

For DQS position training, BIOS generates a training pattern using continuous read or write data streams. A 2k-bit-time training pattern is recommended for optimal results. To achieve this, BIOS programs [D18F2x260_dct\[0\]\[CmdCount\] = 256](#), [D18F2x250_dct\[0\]\[CmdTgt\]=01b](#), and [D18F2x25\[8,4\]_dct\[0\]](#) to access two different banks of the same CS. See [2.9.8 \[Continuous Pattern Generation\]](#).

Prior to DQS position training, BIOS must program [D18F2x210_dct\[0\]_nbp\[3:0\]\[MaxRdLatency\]](#) based on the current greatest value of [D18F2x9C_x0000_00\[2A:10\]_dct\[0\]_mp\[1:0\]](#). See [2.9.7.9.5 \[Calculating MaxRdLatency\]](#).

The following describes the steps used for DQS position training for each channel:

- Program [D18F2x9C_x0D0F_0\[F,8:0\]1F_dct\[0\]_mp\[1:0\]](#) for all lanes.
 - RxDqInsDly = 0. This could be reset from a prior frequency step. Start out with zero added delay for first try.

For each rank and lane:

1. Select a 64 byte aligned test address.
2. For each write data delay value in [D18F2x9C_x0000_0\[3:0\]0\[3:1\]_dct\[0\]_mp\[1:0\]](#) from Wr-DQS to Wr-DQS plus 1 UI, using the Wr-DQS delay value found in [2.9.7.9.1 \[Write Levelization Training\]](#):
 - Program the write data delay value for the current lane.
 - Write the DRAM training pattern to the test address.
3. For each read DQS delay value in [D18F2x9C_x0000_0\[3:0\]0\[7:5\]_dct\[0\]_mp\[1:0\]](#) from 0 to 1 UI:
 - Program the read DQS delay value for the current lane.
 - Read the DRAM training pattern from the test address.
 - Record the result for the current settings as a pass or fail depending if the pattern is read correctly.
 - Process the array of results and determine the longest string of consecutive passing read DQS delay values.
 - If the read DQS delay results for the current lane contain three or more consecutive passing delay values, then program [D18F2x9C_x0000_0\[3:0\]0\[7:5\]_dct\[0\]_mp\[1:0\]](#) with the average value of the smallest and largest delay values in the string of consecutive passing results.
 - If the average value of passing read DQS delay for the lane is negative, then adjust the input receiver DQ delay in [D18F2x9C_x0D0F_0\[F,8:0\]1F_dct\[0\]_mp\[1:0\]\[RxDqInsDly\]](#) for the lane as follows:
 - IF ([RxDqInsDly < 3](#)) THEN increment [RxDqInsDly](#) and repeat step 3 above for all ranks and lanes; See note below.
 - ELSE program the read DQS delay for the lane with a value of zero. BIOS should also flag an error message for debug analysis.
 - ENDIF.
4. Process the array of results and determine the longest string of consecutive passing write data delay values for the read DQS delay value found in the step above.
 - If the write data delay results for the current lane contain three or more consecutive passing delay values, then program [D18F2x9C_x0000_0\[3:0\]0\[3:1\]_dct\[0\]_mp\[1:0\]](#) with the average value of the smallest and largest delay values in the string of consecutive passing results.

See [Figure 2](#).

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WrDatFineDly (Wr-DQS to Wr-DQS + 1UI)	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
31	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
30	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
29	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
28	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
27	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
26	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
25	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
24	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
23	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
22	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
21	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
20	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
19	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
18	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
17	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P		
16	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
15	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
14	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
13	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
12	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
11	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
10	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
9	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
8	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
7	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
6	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
5	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
4	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
3	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
2	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
1	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
0	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F		
/32	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RdDqsTime

Figure 2: DQS Position Training Example Results

In some cases, a non-zero process, voltage, and temperature dependent insertion delay is added to the DLL programmed read DQS delay. This has the effect of sampling data later than intended and can result in missing the left edge of the passing region when sweeping from 0 to 1 UI because a read DQS delay value of 0 is already in the passing region. Since DQS is periodic, BIOS can recover the missing information by adjusting the algorithm described above to analyze both the in phase data and the data shifted by one bit time at each step of the read DQS delay sweep. See [D18F2x268_dct\[0\]\[NibbleErrSts\]](#) and [D18F2x26C_dct\[0\]\[NibbleErr180Sts\]](#).

As shown in [Figure 3](#), for each delay setting BIOS records a passing result of P_Φ for the data comparison shifted by one bit time if the data at bit times $N=0, 1, \dots, 6$, is read correctly when compared against the data written at bit times $N=1, 2, \dots, 7$. In the array of results, these passing values make up the left piece of information that had been lost due to insertion delay. In order to process the array of results, BIOS calculates the read DQS delay value for a P_Φ result as $RdDqsTimeByte$ minus 1 UI.

Figure 3: DOS Position Training Insertion Delay Recovery Example Results

2.9.7.9.5 Calculating MaxRdLatency

The MaxRdLatency value determines when the memory controller can receive incoming data from the DCTs. Calculating MaxRdLatency consists of summing all the synchronous and asynchronous delays in the path from the processor to the DRAM and back at a given MEMCLK frequency. BIOS incrementally calculates the MaxRdLatency and then finally programs the value into [D18F2x210_dct\[0\].nbp\[3:0\]](#)[MaxRdLatency].

The following steps describe the algorithm used to compute [D18F2x210_dct\[0\].nbp\[3:0\]](#)[MaxRdLatency] used for DRAM training. P, N, and T are used as a temporary placeholders for the incrementally summed value.

1. $P = N = T = 0$
2. If ([D18F2x9C_x0000_0004_dct\[0\].mp\[1:0\]](#)[AddrCmdSetup] = 0 & [D18F2x9C_x0000_0004_dct\[0\].mp\[1:0\]](#)[CsOdtSetup] = 0 & [D18F2x9C_x0000_0004_dct\[0\].mp\[1:0\]](#)[CkeSetup] = 0)
then $P = P + 1$
else $P = P + 2$
3. $P = P + (8 - \text{Worst case in real silicon. See step 4.})$
4. $P = P + \text{NumPclks}$
• NumPclks = 6
5. $P = P + (2 * (\text{D18F2x200_dct[0].mp[1:0].Tcl} - 1 \text{ clocks}))$
6. $P = P + \text{CEIL}(\text{MAX}(\text{D18F2x9C_x0000_00[2A:10].dct[0].mp[1:0].DqsRcvEnGrossDelay}, \text{DqsRcvEnFineDelay}) + \text{D18F2x9C_x0000_0[3:0]0[7:5].dct[0].mp[1:0].RdDqsTime} \text{ PCLks})) + 1$
• Prior to DQS position training, use maximum value for RdDqsTime.
7. If ($\text{NclkFreq}/\text{MemClkFreq} < 2$) then $P = P + 4.5$
Else $P = P + 2.5$
8. $T = T + 1050 \text{ ps}$
9. $N = (P/\text{MemClkFreq} * 2) + T$; Convert from PCLKs plus time to NCLKs.
• See [D18F5x16\[C:0\].NbDid](#), [NbFid](#) and [D18F2x94_dct\[0\].MemClkFreq](#).
10. [D18F2x210_dct\[0\].nbp\[3:0\]](#)[MaxRdLatency] = $\text{CEIL}(N) + \text{NumNclks}$
• NumNclks = 1

2.9.7.9.5.1 MaxRdLatency Training

After DRAM DQS receiver enable training, BIOS optimizes [D18F2x210_dct\[0\].nbp\[3:0\]](#)[MaxRdLatency] using the following algorithm. For MaxRdLatency training, BIOS generates a training pattern using continuous read or write data streams. See [2.9.8 \[Continuous Pattern Generation\]](#).

For each channel:

1. Calculate a starting MaxRdLatency delay value by executing the steps in [2.9.7.9.5](#), excluding steps 4, 7, 8, and 10. It is expected that the first value will result in a test fail.
2. Select 32 64-byte aligned test addresses associated with the rank that has the worst case ([D18F2x9C_x0000_00\[2A:10\].dct\[0\].mp\[1:0\].DqsRcvEnGrossDelay](#), [DqsRcvEnFineDelay](#) + [D18F2x9C_x0000_0\[3:0\]0\[7:5\].dct\[0\].mp\[1:0\].RdDqsTime](#)) register setting.
3. Write the DIMM test addresses with the training pattern.
4. For each MaxRdLatency value incrementing from the value calculated in step 1:
 - A. Program [D18F2x210_dct\[0\].nbp\[3:0\]](#)[MaxRdLatency] with the current value.
 - B. Read the DIMM test addresses.
 - C. Compare the values read against the pattern written.
 - If the pattern is read correctly, go to step 5.
 - D. Program [D18F2x9C_x0000_0050.dct\[0\]](#)=00000000h to reset the RcvFifo.

5. Program [D18F2x210_dct\[0\].nbp\[3:0\]\[MaxRdLatency\]](#) = CEIL(current value + 1 NCLK + (IF (Verification) THEN 1.0 MEMCLK ELSE 1.5 MEMCLK ENDIF) + IF (NclkFreq/MemClkFreq < 2) THEN 1.0 MEMCLK ELSE 0 ENDIF) .

2.9.7.10 DRAM Phy Power Savings

For power savings, BIOS should perform the following actions for each channel:

1. Program [D18F2x88_dct\[0\]\[MemClkDis\]](#) to disable unused MEMCLK pins.
2. Program [D18F2x9C_x0D0F_2\[F,2:0\]30_dct\[0\]\[PwrDn\]](#) for unused MEMCLK pairs.
3. Program [D18F2x9C_x0D0F_0\[F,8:0\]30_dct\[0\]\[PwrDn\]](#) to disable the ECC lane if [D18F2x90_dct\[0\]\[DimmEccEn\]==0](#).
4. Program [D18F2x9C_x0000_000C_dct\[0\]\[CKETri, ODTTri, ChipSelTri\]](#) to disable unused pins.
5. Per byte, if none of [D18F2x9C_x0D0F_0\[F,8:0\]\[17:14\]\[EarlyLateU\[3:0\]\]](#) is set to 1, then Program [D18F2x9C_x0D0F_0\[F,8:0\]13_dct\[0\].mp\[1:0\]\[DlIDisEarlyU\]](#) = 1.
6. Per byte, if none of [D18F2x9C_x0D0F_0\[F,8:0\]\[17:14\]\[EarlyLateL\[3:0\]\]](#) is set to 1, then Program [D18F2x9C_x0D0F_0\[F,8:0\]13_dct\[0\].mp\[1:0\]\[DlIDisEarlyL\]](#) = 1.
7. [D18F2x9C_x0D0F_812F_dct\[0\]\[PARTri\]](#) = 1.
8. [D18F2x9C_x0D0F_812F_dct\[0\]\[Add17Tri, Add16Tri\]](#) = {1b, 1b}
9. Program [D18F2x9C_x0D0F_0\[F,8:0\]10_dct\[0\].mp\[1:0\]\[EnRxPadStandby\]](#) = IF ([DdrRate <= 1600](#)) THEN 1 ELSE 0 ENDIF.
10. Program [D18F2x9C_x0000_000D_dct\[0\].mp\[1:0\]](#) as follows:
 - If ([DdrRate <= 1600](#)) [TxMaxDurDlNoLock](#) = [RxMaxDurDlNoLock](#) = 8h
else [TxMaxDurDlNoLock](#) = [RxMaxDurDlNoLock](#) = 7h.
 - [TxCPUUpdPeriod](#) = [RxCPUUpdPeriod](#) = 011b.
 - [TxDLLWakeUpTime](#) = [RxDLLWakeUpTime](#) = 11b.
11. Program [D18F2x9C_x0D0F_0\[F,8:0\]1C_dct\[0\].mp\[1:0\]](#) as follows:
 - If [D18F2x90_dct\[0\]\[DimmEccEn\]](#) Numlanes = 9 Else Numlanes = 8.
 - If ([DdrRate >= 1866](#)) [DlIWakeTime](#) = 1 Else [DlIWakeTime](#) = 0.
 - Let [MaxRxStggrDly](#) = (([Tcl-1](#))*2) + MIN([DqsRcvEnGrossDelay](#) for all byte lanes) - 6.
 - See [D18F2x9C_x0000_00\[2A:10\].dct\[0\].mp\[1:0\]](#).
 - Let (real) [dRxStggrDly](#) = ([MaxRxStggrDly](#) - [DlIWakeTime](#)) / (Numlanes - 1).
 - For each byte lane in the ordered sequence below, program [RxDlIStggrDly\[5:0\]](#) = an increasing value, starting with 0 for the first byte lane in the sequence and increasing at a rate of [dRxStggrDly](#) for each subsequent byte lane.
 - Sequence: If [D18F2x90_dct\[0\]\[DimmEccEn\]](#) {8, 4, 3, 5, 2, 6, 1, 7, 0} else {4, 3, 5, 2, 6, 1, 7, 0}.
 - Let [MaxTxStggrDly](#) = MIN((([Tcwl-1](#))*2) + MIN([WrDqsGrossDly](#) for all byte lanes) - [WrDqDqsEarly](#) - 4, [MaxRxStggrDly](#))
 - See [D18F2x9C_x0000_00\[4A:30\].dct\[0\].mp\[1:0\]](#).
 - See [D18F2x20C_dct\[0\].mp\[1:0\]](#).
 - Let (real) [dTxStggrDly](#) = ([MaxTxStggrDly](#) - [DlIWakeTime](#)) / (Numlanes - 1).
 - For each byte lane in the ordered sequence below, program [TxDlIStggrDly\[5:0\]](#) = an increasing integer value, starting with 0 for the first byte lane in the sequence and increasing at a rate of [dTxStggrDly](#) for each subsequent byte lane.
 - Sequence: If [D18F2x90_dct\[0\]\[DimmEccEn\]](#) {0, 7, 1, 6, 2, 5, 3, 4, 8} else {0, 7, 1, 6, 2, 5, 3, 4}.
 - [RxDlIStggrEn](#) = [TxDlIStggrEn](#) = 1.
12. Program [D18F2x248_dct\[0\].mp\[1:0\]](#) and then [D18F2x9C_x0D0F_0\[F,8:0\]13_dct\[0\].mp\[1:0\]](#) as follows:
 - For M0 & M1 context program [RxChMntClkEn](#)=[RxSsbMntClkEn](#)=0.
13. Program [D18F2x9C_x0D0F_0\[F,8:0\]30_dct\[0\]\[TxPclkGateEn, PchgPdPclkGateEn, DataCtlPipePclkGateEn\]](#) = {1, 1, 1}.
14. Program [D18F2x9C_x0D0F_0\[F,8:0\]04_dct\[0\].mp\[1:0\]\[TriDM\]](#) = IF ([DataMaskMbType == 0](#)) THEN 1 ELSE 0 ENDIF.

2.9.8 Continuous Pattern Generation

DRAM training relies on the ability to generate a string of continuous reads or writes between the processor and DRAM, such that worst case electrical interactions can be created. This section describes how these continuous strings of accesses may be generated.

2.9.8.1 DCT Training Pattern Generation (Reliable Read Write Mode)

DCT training pattern generation uses pattern generators in the DCT to generate controlled read and write traffic streams. During write pattern generation, data values based off of a deterministic pattern are burst to the DRAM interface. Conversely for reads, data bursts from the DRAM interface are compared against expected data values on a per nibble basis.

Two address modes are available for DRAM training pattern generation, as configured by [D18F2x250_dct\[0\]\[CmdTgt\]](#). For generating a stream of reads or writes to the same rank, address target A mode is used. To generate a stream of accesses to up to two different ranks, address target A and B mode is used.

An overview of the BIOS sequence to generate training patterns is as follows:

- Configure the DCT for pattern generation. See [2.9.7.7 \[DCT Training Specific Configuration\]](#).
- Ensure DIMMs are configured to support 8-beat bursts (BL8 or dynamic burst length on the fly).
- Wait for [D18F2x250_dct\[0\]\[CmdSendInProg\]](#) = 0.
- Program [D18F2x250_dct\[0\]\[CmdTestEnable\]](#) = 1.
- Send activate commands as appropriate. See [2.9.8.1.1 \[Activate and Precharge Command Generation\]](#).
- Send read or write commands as desired. See [2.9.8.1.2 \[Read and Write Command Generation\]](#).
- Send precharge commands as appropriate. See [2.9.8.1.1 \[Activate and Precharge Command Generation\]](#).
- Program [D18F2x250_dct\[0\]\[CmdTestEnable\]](#) = 0.

2.9.8.1.1 Activate and Precharge Command Generation

Prior to sending read or write commands, BIOS must send an activate command to a row in a particular bank of the DRAM devices for access. To send an activate command, BIOS performs the following steps:

- Program [D18F2x28C_dct\[0\]](#) to the desired address as follows:
 - CmdChipSelect = CS[7:0].
 - CmdBank = BA[2:0].
 - CmdAddress = A[17:0] (row address).
- Program [D18F2x28C_dct\[0\]\[SendActCmd\]](#) = 1.
- Wait until [D18F2x28C_dct\[0\]\[SendActCmd\]](#) = 0.
- Wait 75 MEMCLKs. ([D18F2x200_dct\[0\]_mp\[1:0\]\[Tras, Trcd\]](#), [D18F2x204_dct\[0\]_mp\[1:0\]\[FourAc-tWindow, Trrd, Trc\]](#))

After completing its accesses, BIOS must deactivate open rows in the DRAM devices. To send a precharge or precharge all command to deactivate open rows in a bank or in all banks, BIOS performs the following steps:

- Wait 25 MEMCLKs. ([D18F2x204_dct\[0\]_mp\[1:0\]\[Trtp\]](#))
- Program [D18F2x28C_dct\[0\]](#) to the desired address as follows:
 - CmdChipSelect = CS[7:0].
 - Precharge all command:
 - CmdAddress[10] = 1.
 - Precharge command:
 - CmdAddress[10] = 0.
 - CmdBank = BA[2:0].

- Program D18F2x28C_dct[0][SendPchgCmd] = 1.
- Wait until D18F2x28C_dct[0][SendPchgCmd] = 0.
- Wait 25 MEMCLKs. (Trp)

2.9.8.1.2 Read and Write Command Generation

BIOS performs the following steps for read pattern generation:

- Program D18F2x27C_dct[0], D18F2x278_dct[0], and D18F2x274_dct[0] with the data comparison masks for bit lanes of interest.
- Program D18F2x270_dct[0][DataPrbsSeed] the seed for the desired PRBS.
- Program D18F2x260_dct[0][CmdCount] equal to the number of cache line commands.
- Program D18F2x25C_dct[0][BubbleCnt, CmdStreamLen]. See 2.9.8.1.5 [BubbleCnt and CmdStreamLen Programming].
- Program D18F2x25[8,4]_dct[0] to the initial address (column address).
- Program D18F2x250_dct[0] as follows:
 - ResetAllErr and StopOnErr as desired. See 2.9.8.1.4 [Data Comparison].
 - CmdTgt corresponding to D18F2x25[8,4]_dct[0].
 - CmdType = 000b.
 - SendCmd = 1.
- If D18F2x260_dct[0][CmdCount] != 0 (not in infinite mode) then
Wait for D18F2x250_dct[0][TestStatus] = 1 and D18F2x250_dct[0][CmdSendInProg] = 0.
Else
Wait the desired amount of time.
Program D18F2x260_dct[0][CmdCount] = 1.
Wait for D18F2x250_dct[0][TestStatus] = 1 and D18F2x250_dct[0][CmdSendInProg] = 0.
- Program D18F2x250_dct[0][SendCmd] = 0.
- Read D18F2x264_dct[0], D18F2x268_dct[0], and D18F2x26C_dct[0] if applicable.

BIOS performs the following steps for write pattern generation:

- Program D18F2x270_dct[0][DataPrbsSeed] the seed for the desired PRBS.
- Program D18F2x260_dct[0][CmdCount] equal to the number of cache line commands desired.
- Program D18F2x25C_dct[0][BubbleCnt, CmdStreamLen]. See 2.9.8.1.5 [BubbleCnt and CmdStreamLen Programming].
- Program D18F2x25[8,4]_dct[0] to the initial address.
- Program D18F2x250_dct[0] as follows:
 - CmdTgt corresponding to D18F2x25[8,4]_dct[0].
 - CmdType = 001b.
 - SendCmd = 1.
- If D18F2x260_dct[0][CmdCount] != 0 (not in infinite mode) then
Wait for D18F2x250_dct[0][TestStatus] = 1 and D18F2x250_dct[0][CmdSendInProg] = 0.
Else
Wait the desired amount of time.
Program D18F2x260_dct[0][CmdCount] = 1.
Wait for D18F2x250_dct[0][TestStatus] = 1 and D18F2x250_dct[0][CmdSendInProg] = 0.
- Program D18F2x250_dct[0][SendCmd] = 0.

BIOS combines the two sets of steps listed above for alternating write and read pattern generation.

2.9.8.1.3 Configurable Data Patterns

In addition to PRBS mode, D18F2x250_dct[0][DataPatGenSel] and D18F2x2[B4,B0,AC,A8]_dct[0] allow configurable data pattern generation. E.g. Simultaneous Switching Output (SSO) and Inversion Patterns.

Table 53. Configurable Data Pattern Example with 1 Address Target

DQ/ Beat	Write TgtA Cmd 0								Write TgtA Cmd 1								Write TgtA Cmd 2								...
	Beat 0	Beat 1	Beat 2	Beat 3	Beat 4	Beat 5	Beat 6	Beat 7	Beat 8	Beat 9	Beat 10	Beat 11	Beat 12	Beat 13	Beat 14	Beat 15	Beat 16	Beat 17	Beat 18	Beat 19	Beat 20	Beat 21	Beat 22	Beat 23	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0
2	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
3	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0
4	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
5	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0
6	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
7	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	0
8	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1
9	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1
10	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
11	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0
12	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
13	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1
14	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
...																									
ECC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ECC1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0
ECC2	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0	0
ECC3	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0
ECC4	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0
ECC5	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0
ECC6	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
ECC7	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1

- D18F2x250_dct[0][DataPatGenSel] = 10b //Configurable data pattern
D18F2x2[B4,B0,AC,A8]_dct[0] = {FFEE_DDCCh, BBAA_9988h, 7766_5544h, 3322_1100h}

Table 54. Configurable Data Pattern Circular Shift Example with 1 Address Target

DQ/ Beat	Write TgtA Cmd 0								Write TgtA Cmd 1								Write TgtA Cmd 2								...	
	Beat 0	Beat 1	Beat 2	Beat 3	Beat 4	Beat 5	Beat 6	Beat 7	Beat 8	Beat 9	Beat 10	Beat 11	Beat 12	Beat 13	Beat 14	Beat 15	Beat 16	Beat 17	Beat 18	Beat 19	Beat 20	Beat 21	Beat 22	Beat 23	...	
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	1	
1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
2	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
3	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	
4	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	
5	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0	0	
6	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	0	
7	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	1	
8	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	0	0	1	1	0	0	1	1	0		
9	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	0		
10	0	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0	1	
11	1	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	1	0	0	1	1	0	0	1		
12	0	0	1	1	0	0	1	1	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	0	1	
13	1	0	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1	0	1	1	1	0	1		
14	0	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0	0	1	1	0	0	1	1		
15	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1		
...																										
ECC0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	
ECC1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
ECC2	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
ECC3	1	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	
ECC4	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0	0	1	0	0	0	0	1	0	0	
ECC5	1	0	1	0	1	0	1	0	0	0	1	0	0	0	1	0	1	1	0	0	1	1	0	0		
ECC6	0	1	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	
ECC7	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1	0	1	0	1	1	0	1	0		

1. D18F2x250_dct[0][DataPatGenSel] = 11b //User data pattern with circular lane shift
D18F2x2[B4,B0,AC,A8]_dct[0] = {FFEE_DDCCh, BBAA_9988h, 7766_5544h, 3322_1100h}

2.9.8.1.3.1 Static Data Pattern Override

Software is also able to use the bits of D18F2x280_dct[0], D18F2x284_dct[0], and D18F2x288_dct[0] to override the DCT pattern generator on a DQ basis. This can only be used in the D18F2x250_dct[0][DataPatGenSel] = 10b mode. Software programs the following to enable the mode:

- Program D18F2x288_dct[0][PatOvrVal] to the data value desired.
- Program D18F2x280_dct[0][DQPatOvrEn[31:0]], D18F2x284_dct[0][DQPatOvrEn[63:32]], and D18F2x288_dct[0][EccPatOvrEn] to enable the override on the desired bit lanes.

Table 55. Data Pattern Override Example with 1 Address Target

DQ/ Beat	Write TgtA Cmd 0								Write TgtA Cmd 1								Write TgtA Cmd 2								...	
	Beat 0	Beat 1	Beat 2	Beat 3	Beat 4	Beat 5	Beat 6	Beat 7	Beat 8	Beat 9	Beat 10	Beat 11	Beat 12	Beat 13	Beat 14	Beat 15	Beat 16	Beat 17	Beat 18	Beat 19	Beat 20	Beat 21	Beat 22	Beat 23	...	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	
2	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
3	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	
4	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	
5	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	
6	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	
7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
8	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	
9	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1	
10	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
11	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	0	
12	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	
13	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	
14	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	
15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
...																										
ECC0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ECC1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	
ECC2	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	
ECC3	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	
ECC4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
ECC5	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	
ECC6	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0		
ECC7	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	1	

1. D18F2x250_dct[0][DataPatGenSel] = 10b //Configurable data pattern
D18F2x2[B4,B0,AC,A8]_dct[0] = {FFEE_DDCCh, BBAA_9988h, 7766_5544h, 3322_1100h}
D18F2x288_dct[0][PatOvrVal] = 0. //Static 0's
D18F2x280_dct[0][DQPatOvrEn[31:0]] = 0x0000_0080. // DQ7 Override
D18F2x284_dct[0][DQPatOvrEn[63:32]] = 0x0000_0000. // No Override
D18F2x288_dct[0][EccPatOvrEn] = 0x10. // ECC4 Override

2.9.8.1.3.2 Xor Data Pattern Override

Software is also able to use the bits of D18F2x288_dct[0][XorPatOvr] to override the DCT pattern generator with the same XOR function for all byte lanes. This feature can only be used with select D18F2x250_dct[0][DataPatGenSel] PRBS modes. Software programs the following to enable the mode:

- Program D18F2x288_dct[0][XorPatOvr] to the data value of the XOR function desired.
- Output data = IF (DQPatOvrEn) THEN PatOvrVal ELSE (DataPatGen ^ XorPatOvr) ENDIF.

2.9.8.1.4 Data Comparison

The DCT compares the incoming read data against the expected pattern sequence during pattern generation. BIOS may choose to continue command generation and accumulate errors or stop command generation on the first error occurrence by programming D18F2x250_dct[0][StopOnErr].

Error information is reported via D18F2x264_dct[0], D18F2x268_dct[0], D18F2x26C_dct[0], D18F2x294_dct[0], D18F2x298_dct[0] and D18F2x29C_dct[0]. Error information can be masked on per-bit basis by programming D18F2x274_dct[0], D18F2x278_dct[0], and D18F2x27C_dct[0].

BIOS resets the error information by programming D18F2x250_dct[0][ResetAllErr]=1.

Error information is only valid in certain modes of D18F2x250_dct[0][CmdType, CmdTgt] and D18F2x260_dct[0][CmdCount] and when using 64 byte aligned addresses in D18F2x25[8,4]_dct[0][TgtAddress]. Some modes require a series of writes to setup a DRAM data pattern. See Table 56.

Table 56. Command Generation and Data Comparison

Commands	CmdType	Cmd Tgt	Maximum CmdCount ⁴
Read	000b	00b ¹	128
		01b ¹	256 ²
Write-Read	010b	00b	Infinite
		01b ³	256 ²
1. Requires setup writes to store a data pattern in DRAM. The write commands are generated using the same CmdTgt, CmdCount, and DataPrbsSeed settings. 2. D18F2x254[TgtAddress] != D18F2x258[TgtAddress]. 3. Requires setup writes to store a data pattern in DRAM. The write commands are generated programming D18F2x254[TgtAddress] to the intended Target B, CmdTgt=00b, CmdCount to 1/2 of the intended command count, and the same DataPrbsSeed setting. 4. D18F2x250_dct[0][LsfrRollOver]=0. The maximum CmdCount is infinite for all modes listed if D18F2x250_dct[0][LsfrRollOver]=1.			

2.9.8.1.4.1 Activate and Precharge Traffic Generation

The DCT generates ACT and PRE traffic in the available command bandwidth during a WR or RD sequence generated by D18F2x250_dct[0][SendCmd] when D18F2x250_dct[0][ActPchgGenEn]=1. This 16 command sequence repeats until the WR or RD initiated by SendCmd hits a stopping condition.

Software is able to adjust the command spacing and address sequence by programming D18F2x28C_dct[0][CmdChipSelect, CmdAddress[17:4]], D18F2x2B8_dct[0][ActPchgSeq, ActPchgCmdMin], and D18F2x2[C0,BC]_dct[0].

The banks specified by [D18F2x2\[C0,BC\]_dct\[0\]](#) must be in the idle state and must not conflict with the banks used by the SendCmd WR or RD traffic stream. Software is responsible for the ACT/PRE protocol of the WR or RD targets initiated by SendCmd. On a stopping condition for the WR or RD traffic stream, software is responsible for returning all of the possibly open banks to the idle state.

- Example configuration for DRAM Training:
- [D18F2x250_dct\[0\]\[ActPchgGenEn, CmdTgt, CmdType\]](#) = {1b, 1b, 0b}. // Tgt A&B, Reads
- [D18F2x28C_dct\[0\]\[CmdChipSelect\]](#) = CS of TgtA
- [D18F2x28C_dct\[0\]\[CmdAddress\[17:4\]\]](#) = desired upper row address bits.
 - Hardware places the sequence number in row address [3:0].
- [D18F2x2B8_dct\[0\]\[ActPchgSeq, ActPchgCmdMin\]](#) = {0F0Fh, Fh}.
- [D18F2x2BC_dct\[0\]](#) = 5432_5432h; // Banks 2,3,4,5
- [D18F2x2C0_dct\[0\]](#) = 7632_7632h; // Banks 2,3,6,7

2.9.8.1.5 BubbleCnt and CmdStreamLen Programming

BIOS programs [D18F2x25C_dct\[0\]\[BubbleCnt2, BubbleCnt, CmdStreamLen\]](#) to ensure proper channel command spacing in command generation mode.

For continuous pattern generation it is expected that BubbleCnt = 0. In other modes, BIOS programs BubbleCnt, BubbleCnt2, and CmdStreamLen greater than or equal to the relevant DRAM timing parameters shown below to prevent contention on the DRAM bus. In all cases, if the minimum BubbleCnt > 0 or CmdType = 010b then BIOS programs CmdStreamLen = 1.

Table 57. DDR3 Command Generation and BubbleCnt Programming

Commands	CmdType	CmdTgt	BubbleCnt	BubbleCnt2
Read-Read same CS	000b	0xb	D18F2x218_dct[0]_mp[1:0][TrdrdSdSc] - 1; Exclude banned spacing: D18F2x218_dct[0]_mp[1:0][TrdrdBan]	xh
Write-Write same CS	001b	0xb	D18F2x214_dct[0]_mp[1:0][TwrwrSdSc] - 1	xh
Write-Read same CS	010b	00b	D18F2x20C_dct[0]_mp[1:0][Twtr] + D18F2x20C_dct[0]_mp[1:0][TcwL] + 4 - 1	D18F2x21C_dct[0]_mp[1:0][TrwtTO] - 1
Read-Read different CS	000b	01b	D18F2x218_dct[0]_mp[1:0][TrdrdSdDc] - 1; Exclude banned spacing: D18F2x218_dct[0]_mp[1:0][TrdrdBan]	xh
Write-Write different CS	001b	01b	D18F2x214_dct[0]_mp[1:0][TwrwrSdDc] - 1	xh
Write-Read different CS	010b	01b	D18F2x218_dct[0]_mp[1:0][Twrrd] - 1	D18F2x21C_dct[0]_mp[1:0][TrwtTO] - 1

Table 57. DDR3 Command Generation and BubbleCnt Programming

Commands	CmdType	CmdTgt	BubbleCnt	BubbleCnt2
Read-Read different DIMM	000b	01b	D18F2x218_dct[0]_mp[1:0][TrdrdDd] - 1; Exclude banned spacing: D18F2x218_dct[0]_mp[1:0][TrdrdBan]	xh
Write-Write different DIMM	001b	01b	D18F2x214_dct[0]_mp[1:0][TwrrwrDd] - 1	xh
Write-Read different DIMM	010b	01b	D18F2x218_dct[0]_mp[1:0][Twrrd] - 1	D18F2x21C_dct[0]_mp[1:0][TrwtTO] - 1

2.9.9 Memory Interleaving Modes

The processor supports the following memory interleaving modes:

- Chip select: interleaves the physical address space over multiple DIMM ranks on a channel, as opposed to each DIMM owning single consecutive address spaces. See [2.9.9.1 \[Chip Select Interleaving\]](#).

Table 58. Recommended Interleave Configurations

Interleaving Mode	Enabled	Disabled
Chip Select Interleaving	Number of chip selects installed on the channel is a power of two.	Requirements not satisfied.

2.9.9.1 Chip Select Interleaving

The chip select memory interleaving mode has the following requirements:

- The number of chip selects interleaved is a power of two.
- The chip selects are the same size and type.

A BIOS algorithm for programming D18F2x[5C:40]_dct[0] [DRAM CS Base Address] and D18F2x[6C:60]_dct[0] [DRAM CS Mask] in memory interleaving mode is as follows:

- 1.Program all DRAM CS Base Address and DRAM CS Mask registers using contiguous normalized address mapping.
- 2.For each enabled chip select, swap the corresponding BaseAddr[38:27] bits with the BaseAddr[21:11] bits as defined in [Table 59](#).
- 3.For each enabled chip select, swap the corresponding AddrMask[38:27] bits with the AddrMask[21:11] bits as defined in [Table 59](#).

Table 59. DDR3 Swapped Normalized Address Lines for CS Interleaving

Condition			Swapped Base Address and Address Mask bits		
DIMM Address Map ¹	CS Size	BankSwap ²	DctSelBankSwap ²	4 way CS interleaving	2 way CS interleaving
0001b	256MB	0	-	[29:28] and [17:16]	[28] and [16]
		1	1	[29:28] and [12:11]	[28] and [11]
		1	0	[29:28] and [13:12]	[28] and [12]
0010b	512MB	0	-	[30:29] and [17:16]	[29] and [16]
		1	1	[30:29] and [12:11]	[29] and [11]
		1	0	[30:29] and [13:12]	[29] and [12]
0101b	1GB	0	-	[31:30] and [17:16]	[30] and [16]
		1	1	[31:30] and [12:11]	[30] and [11]
		1	0	[31:30] and [13:12]	[30] and [12]
0111b	2GB	0	-	[32:31] and [17:16]	[31] and [16]
		1	1	[32:31] and [12:11]	[31] and [11]
		1	0	[32:31] and [13:12]	[31] and [12]
1010b	4GB	0	-	[33:32] and [17:16]	[32] and [16]
		1	1	[33:32] and [12:11]	[32] and [11]
		1	0	[33:32] and [13:12]	[32] and [12]
1011b	8GB	0	-	[34:33] and [18:17]	[33] and [17]
		1	1	[34:33] and [12:11]	[33] and [11]
		1	0	[34:33] and [13:12]	[33] and [12]

1. See [D18F2x80_dct\[0\] \[DRAM Bank Address Mapping\]](#).
 2. See [D18F2xA8_dct\[0\]\[BankSwap\]](#) and [D18F2x114\[DctSel-BankSwap\]](#).

2.9.10 Memory Hoisting

Memory hoisting reclaims the otherwise inaccessible DRAM that would naturally reside in memory regions used by MMIO. When memory hoisting is configured by BIOS, DRAM physical addresses are repositioned above the 4 GB address level in the address map. In operation, the physical addresses are remapped in hardware to the normalized addresses used by a DCT.

The region of DRAM that is hoisted is defined to be from D18F1xF0[DramHoleBase] to the 4 GB level. Hoisting is enabled by programming [D18F1xF0 \[DRAM Hole Address\]](#) and configuring the DCTs per the equations in this section.

DramHoleSize is defined in order to simplify the following equations in this section and is calculated as follows:

- Define the DRAM hole region as $\text{DramHoleSize}[31:24] = 100h - \text{D18F1xF0}[\text{DramHoleBase}[31:24]]$.

2.9.10.1 DramHoleOffset Programming

D18F1xF0[DramHoleOffset] is programmed to account for the addresses from **D18F1xF0[DramHoleBase]** to 4 GB when it falls inside of a **D18F1x2[1,0][8,0][DctBaseAddr]** and **D18F1x2[1,0][C,4][DctLimitAddr]** region. See [Figure 4](#) as an example memory population.

- Program $\text{D18F1xF0}[\text{DramHoleOffset}[31:23]] = \{\text{DramHoleSize}[31:24], 0b\} + \{\text{DctBaseAddr}[31:27], 0000b\}$;

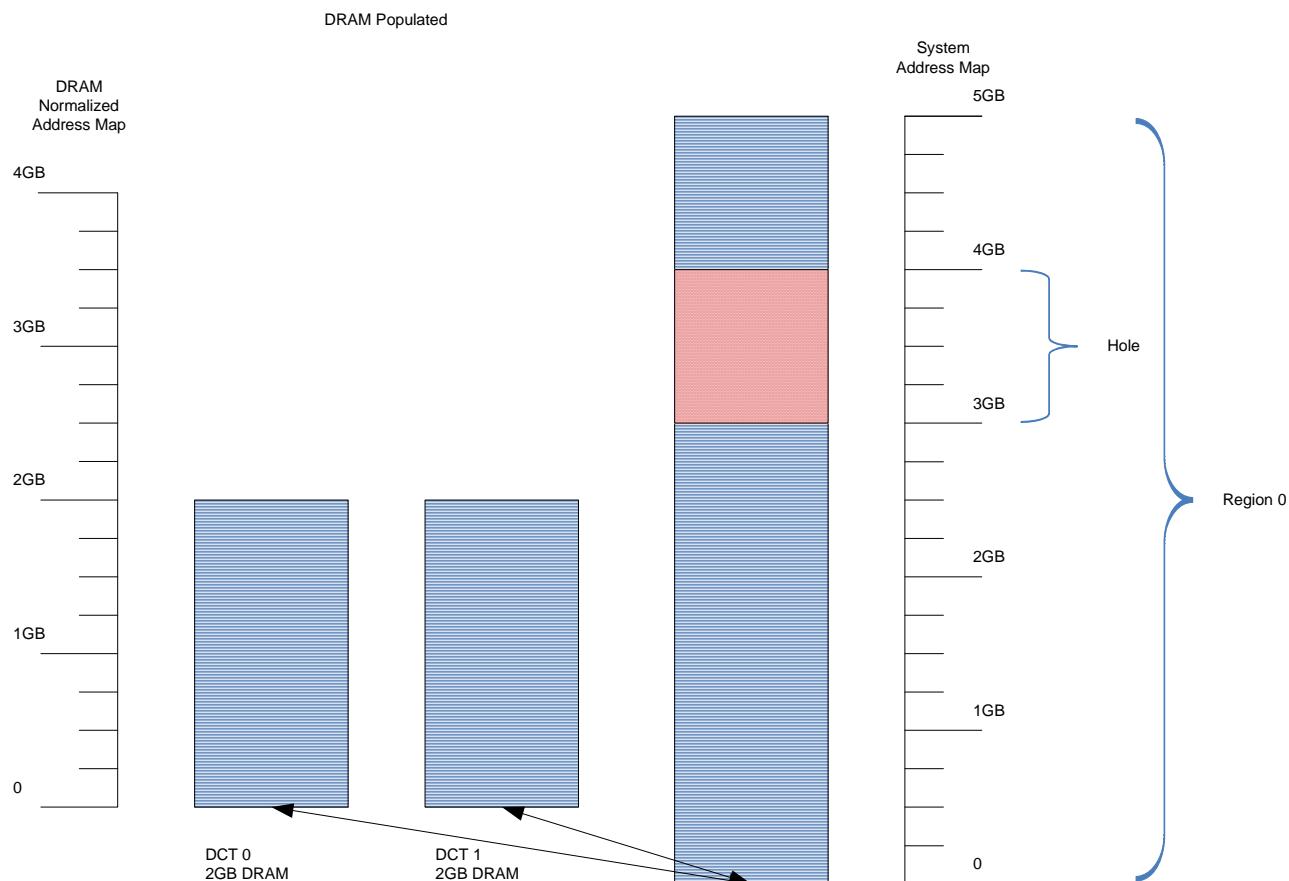


Figure 4: Memory Configuration with Memory Hole inside of Region

D18F1xF0[DramHoleOffset] is unused when the memory hole falls outside of a region. [Figure 5](#) shows an example memory population which uses two memory regions. Region 1 is configured to begin above the memory hole.

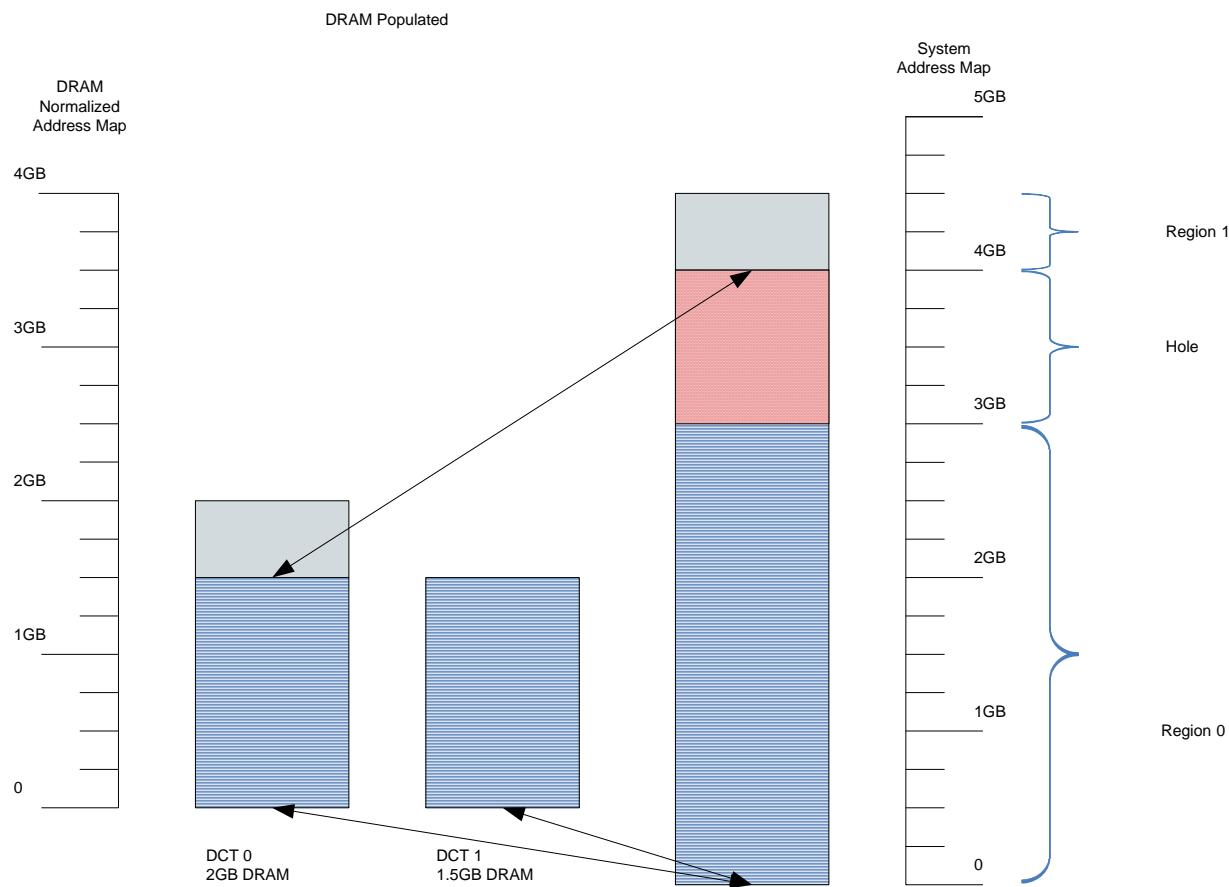


Figure 5: Memory Configuration with Memory Hole outside of Region

2.9.11 DRAM CC6/PC6 Storage

DRAM is used to hold the state information of cores entering the CC6 power management state. As part of the system setup if CC6 or PC6 is enabled, BIOS configures a special region of DRAM to hold the state information. In operation, hardware protects this region from general system accesses while allowing the cores access during C-state transitions.

2.9.11.1 Fixed Storage

The size of each special DRAM storage region is defined to be a fixed 16MB. BIOS configures the storage region at the top of the DRAM range, adjusts [D18F1x\[7:4\]\[C,4\]\[DramLimit\]](#) and the processor top of DRAM specified by [MSRC001_001A\[TOM\]](#) or [MSRC001_001D\[TOM2\]](#) downward accordingly. For UNB designs, the 16MB range is implemented in HW by adjusting [D18F1x124\[DramLimitAddr\]](#). See [Table 60](#).

After finalizing the system DRAM configuration, BIOS must set [D18F2x118\[LockDramCfg\]](#) = 1 to enable the hardware protection.

Table 60. Example storage region configuration

Node	DRAM Populated	D18F1x[17C:140,7C:40] [DramBase, DramLimit]	CC6 DRAM Range	D18F4x128 [CoreStateSaveDestNode]	D18F1x120 [DramBaseAddr], D18F1x124 [DramLimitAddr]
0	256 MB	0 MB, 240 MB - 1	240 MB, 256 MB - 1	0	0 MB, 256 MB - 1

2.9.12 DRAM On DIMM Thermal Management and Power Capping

Each DCT can throttle commands based on the state of the channel EVENT_L pin or when [D18F2xA4\[BwCapEn\]=1](#). The EVENT_L pin is used for thermal management while [D18F2xA4\[BwCapEn\]](#) limits memory power independent of the thermal management solution.

The recommended BIOS configuration for the EVENT_L pin is as follows:

- BIOS may enable command throttling on a DRAM controller if the platform supports the EVENT_L pin by programming [D18F2xA4\[ODTSEn\] = 1](#).
 - The recommended usage is for this pin to be connected to one or more JEDEC defined on DIMM temperature sensors. The DIMM SPD ROM indicates on DIMM temperature sensor support.
 - BIOS configures the temperature sensor(s) to assert EVENT_L pin active low when the trip point is exceeded and deassert EVENT_L when the temperature drops below the trip point minus the sensor defined hysteresis.
 - BIOS programs [D18F2xA4\[CmdThrottleMode\]](#) with the throttling mode to employ when the trip point has been exceeded.
 - The hardware enforces a refresh rate of 3.9 us while EVENT_L is asserted.
- BIOS configures [D18F2x8C_dct\[0\]\[Tref\]](#) based on JEDEC defined temperature range options, as indicated by the DIMM SPD ROM. The two defined temperature ranges are normal (with a case temperature of 85 °C) and extended (with a case temperature of 95 °C). The following recommendation assumes JEDEC defined SPD Byte 31[Extended Temperature Refresh Rate] = 1 devices will not be available in the near future.
 - If all DIMMs support the normal temperature range, or if normal and extended temperature range DIMMs are mixed, BIOS programs [D18F2x8C_dct\[0\]\[Tref\]](#) to 7.8 us and [D18F2xA4\[ODTSEn\] = 1](#), or [D18F2x8C_dct\[0\]\[Tref\]](#) to 3.9 us. BIOS configures the temperature sensor trip point for all DIMMs according to the 85 °C case temperature specification.
 - If all DIMMs support the extended temperature range, BIOS has two options:
 - Follow the recommendation for normal temperature range DIMMs.
 - Program [D18F2x8C_dct\[0\]\[Tref\] = 3.9 us](#) and configure the temperature sensor trip point for all DIMMs according to the 95 °C case temperature specification.
- At startup, the BIOS determines if the DRAMs are hot before enabling a DCT and delays for an amount of time to allow the devices to cool under the influence of the thermal solution. This is accomplished by checking the temperature status in the temperature sensor of each DIMM.
- The DCT latched status of the EVENT_L pin for can be read by system software in [D18F2xAC \[DRAM Controller Temperature Status\]](#).

The relationship between the DRAM case temperature, trip point, and EVENT_L pin sampling interval is outlined as follows:

- The trip point for each DIMM is ordinarily configured to the case temperature specification minus a guard-band temperature for the DIMM.
- The temperature guardband is vendor defined and is used to account for sensor inaccuracy, EVENT_L pin sample interval, and platform thermal design.

- The sampling interval is vendor defined. It is expected to be approximately 1 second.

BIOS may enable bandwidth capping on a DRAM controller by setting [D18F2xA4\[BwCapEn\]](#) = 1 and programming [D18F2xA4\[BwCapCmdThrottleMode\]](#) with the throttling mode to employ. The DCT will employ the larger of the two throttling percentages as specified by [D18F2xA4\[BwCapCmdThrottleMode\]](#) and [D18F2xA4\[CmdThrottleMode\]](#) if the EVENT_L pin is asserted when both [D18F2xA4\[BwCapEn\]](#) = 1 and [D18F2xA4\[ODTSEn\]](#) = 1.

2.10 Thermal Functions

Thermal functions SB-TSI, HTC, PROCHOT_L and THERMTRIP are intended to maintain processor temperature in a valid range by:

- Providing a signal to external circuitry for system thermal management like fan control.
- Lowering power consumption by switching to lower-performance P-state.
- Sending processor to the THERMTRIP state to prevent it from damage.

The processor thermal-related circuitry includes (1) the temperature calculation circuit (TCC) for determining the temperature of the processor and (2) logic that uses the temperature from the TCC. The processor includes a thermal diode as an alternative method for temperature measurement when used with an external thermal diode monitor. The thermal diode does not directly interact with the thermal functions.

2.10.1 The Tctl Temperature Scale

Tctl is a processor temperature control value used for processor thermal management. Tctl is accessible through SB-TSI and [D18F3xA4\[CurTmp\]](#). Tctl is a temperature on its own scale aligned to the processors cooling requirements. Therefore Tctl does not represent a temperature which could be measured on the die or the case of the processor. Instead, it specifies the processor temperature relative to the maximum operating temperature, Tctl,max. Tctl,max is specified in the power and thermal data sheet. Tctl,max is 70 C for lidded processors and 100 C for lidless processors. Tctl is defined as follows for all parts:

A: For Tctl = Tctl_max to 255.875: the temperature of the part is [Tctl - Tctl_max] over the maximum operating temperature. The processor may take corrective actions that affect performance, such as HTC, to support the return to Tctl range B.

B: For Tctl = 0 to Tctl_max - 0.125: the temperature of the part is [Tctl_max - Tctl] under the maximum operating temperature.

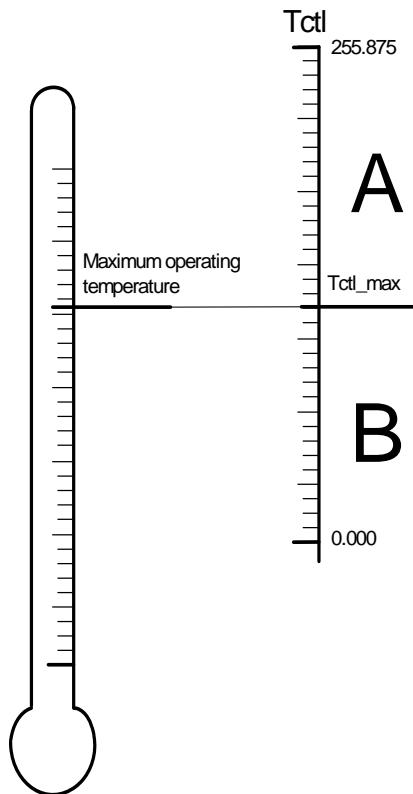


Figure 6: Tctl scale

2.10.2 Temperature Slew Rate Control

The temperature slew rate controls in [D18F3xA4](#) are used to filter processor the processor temperature provided in [D18F3xA4\[CurTmp\]](#) and through SB-TSI. Separate controls are provided for increasing and decreasing temperatures. The latest measured temperature is referred to as Tctlm below.

If downward slew control is enabled ([D18F3xA4\[TmpSlewDnEn\]](#)), Tctl is not updated down unless Tctlm remains below Tctl for a time specified by [D18F3xA4\[PerStepTimeDn\]](#). If at any point before the timer expires Tctlm equals or exceeds Tctl, then the timer resets and Tctl is not updated. If the timer expires, then Tctl is reduced by 0.125. If downward slew control is disabled, then if Tctlm is less than Tctl, Tctl is immediately updated to Tctlm.

The upward slew control works similar to downward slew control except that if Tctlm exceeds Tctl by a value defined by [D18F3xA4\[TmpMaxDiffUp\]](#) then Tctl is immediately updated to Tctlm. Otherwise, Tctlm must remain above Tctl for time specified by [D18F3xA4\[PerStepTimeUp\]](#) before Tctl is incremented by 0.125.

2.10.3 Temperature-Driven Logic

The temperature calculated by the TCC is used by SB-TSI, HTC, THERMTRIP, and PROCHOT_L.

2.10.3.1 PROCHOT_L and Hardware Thermal Control (HTC)

The processor *HTC-active state* is characterized by (1) the assertion of PROCHOT_L, (2) reduced power consumption, and (3) reduced performance. While in the HTC-active state, the processor reduces power consumption by limiting all cores to a P-state (specified by [D18F3x64\[HtcPstateLimit\]](#)). See [2.5.3 \[CPU Power Management\]](#). While in the HTC-active state, software should not change the following: All [D18F3x64](#) fields

(except for HtcActSts and HtcEn), [MSRC001_001F\[DisProcHotPin\]](#). Any change to the previous list of fields when in the HTC-active state can result in undefined behavior. HTC status and control is provided through [D18F3x64](#).

The PROCHOT_L pin acts as both an input and as an open-drain output. As an output, PROCHOT_L is driven low to indicate that the HTC-active state has been entered due to an internal condition, as described by the following text. The minimum assertion and deassertion time for PROCHOT_L is 15 ns.

The processor enters the HTC-active state if all of the following conditions are true:

- [D18F3xE8\[HtcCapable\]](#)=1
- [D18F3x64\[HtcEn\]](#)=1
- PWROK=1
- THERMTRIP_L=1
- The processor is not in the C3 ACPI state.

and any of the following conditions are true:

- Tctl is greater than or equal to the HTC temperature limit ([D18F3x64\[HtcTmpLmt\]](#)).
- PROCHOT_L=0

The processor exits the HTC-active state when all of the following are true:

- Tctl is less than the HTC temperature limit ([D18F3x64\[HtcTmpLmt\]](#)).
- Tctl has become less than the HTC temperature limit ([D18F3x64\[HtcTmpLmt\]](#)) minus the HTC hysteresis limit ([D18F3x64\[HtcHystLmt\]](#)) since being greater than or equal to the HTC temperature limit ([D18F3x64\[HtcTmpLmt\]](#)).
- PROCHOT_L=1.

The default value of the HTC temperature threshold (Tctl_max) is specified in the Power and Thermal Data-sheet.

2.10.3.2 Local Hardware Thermal Control (LHTC)

The *LHTC-active state* of a core is characterized by (1) reduced power consumption and (2) reduced performance of the core. While in the LHTC-active state, the core reduces power consumption by limiting the maximum P-state specified by [D0F0xBC_x3FA1C\[LhtcActivePstateLimit\]](#). See [2.5.3.1 \[Core P-states\]](#).

The LHTC trip point is the same for all cores and is specified by Fuse[LhtcTmpLmt]. The LHTC-active state is independent from the HTC-active state. LHTC does not affect PROCHOT_L output and is not affected by PROCHOT_L input.

A core enters the LHTC-active state if all of the following conditions are true:

- PWROK is asserted.
- The processor is not in the package C6 (PC6) state.
- Tctl maximum for all TCENs is greater than or equal to LHTC temperature limit (specified by Fuse[LhtcTmpLmt]).

A core exits the LHTC-active state when all of the following are true:

- Tctl maximum for all TCENs is less than LHTC temperature low limit (specified by Fuse[LhtcHystLmt]) since being greater than or equal to the LHTC temperature high limit (specified by Fuse[LhtcTmpLmt]).

2.10.3.3 Software P-state Limit Control

[D18F3x68 \[Software P-state Limit\]](#) provides a software mechanism to limit the P-state [MSRC001_0061\[CurP-](#)

stateLimit]. See [2.5.3 \[CPU Power Management\]](#).

2.10.3.4 THERMTRIP

If the processor supports the THERMTRIP state (as specified by [D18F3xE4](#)[ThermtpEn] or [CPUID Fn8000_0007_EDX](#)[TTP], which are the same) and the temperature approaches the point at which the processor may be damaged, the processor enters the THERMTRIP state. The THERMTRIP function is enabled after cold reset (after PWROK asserts and RESET_L deasserts). It remains enabled in all other processor states, except during warm reset (while RESET_L is asserted). The THERMTRIP state is characterized as follows:

- The THERMTRIP_L signal is asserted.
- Nearly all clocks are gated off to reduce dynamic power.
- A low-value VID is generated. Specified by Fuse[ThermVid]; [MSRC001_0071](#)[Min-Vid] is ignored for this voltage transition.
- In addition, the external chipset is expected to place the system into the S5 ACPI state (power off) if THERMTRIP_L is detected to be asserted.

A cold reset is required to exit the THERMTRIP state.

2.11 Root Complex

2.11.1 Overview

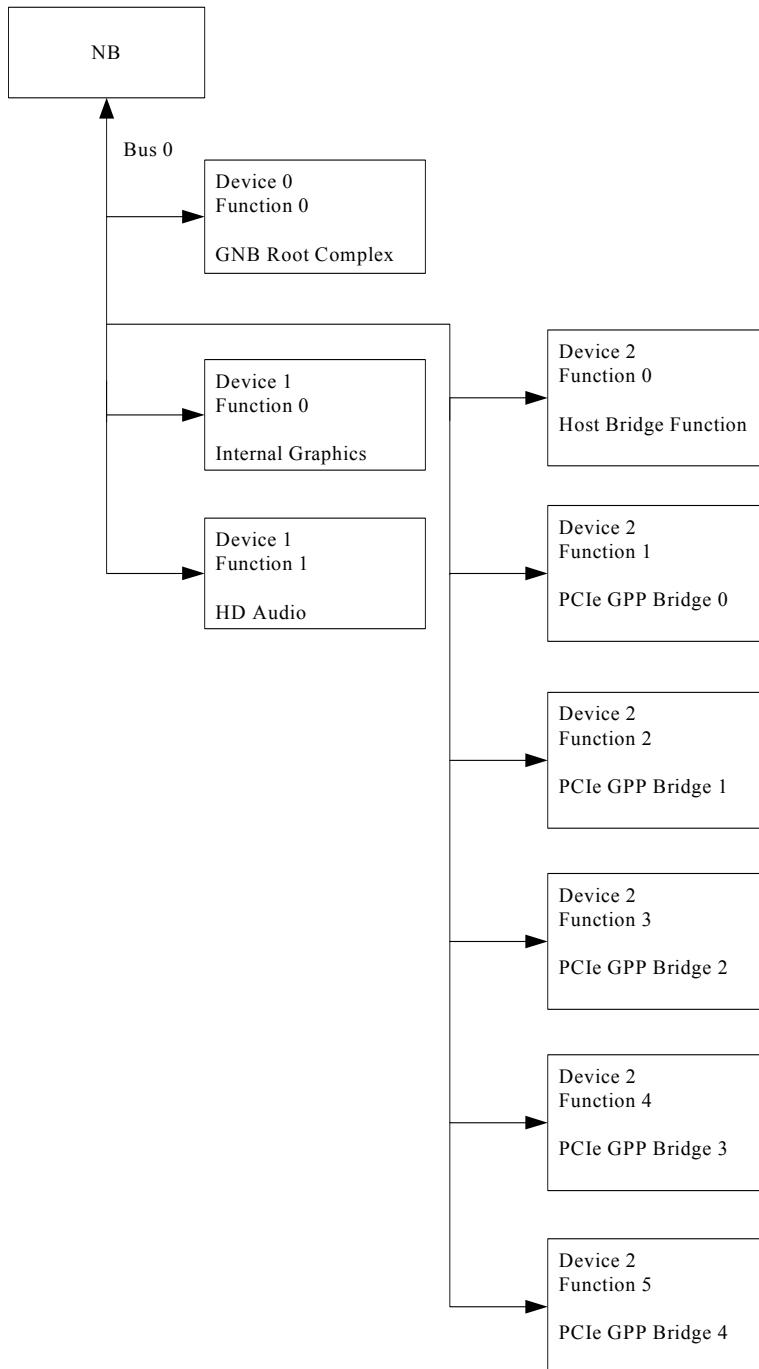


Figure 7: Root complex topology

2.11.2 Interrupt Routing

The GNB includes a fully programmable IOAPIC. The IOAPIC registers are accessed through the [D0F0xF8](#) index and [D0F0xFC](#) data pair registers using two back-to-back config cycles. PCI defined INTx interrupts for

each bridge are routed to IOAPIC pins via the bridge interrupt routing registers located at [D0F0xFC_x1\[4:0\]](#).

2.11.2.1 IOAPIC Configuration

The IOAPIC configuration is performed by the following sequence:

1. Set the base address for the memory mapped registers by programming [D0F0xFC_x01\[IoapicAddr\]](#) and [D0F0xFC_x02\[IoapicAddrUpper\]](#).
2. Enable IOAPIC by programming [D0F0xFC_x00\[IoapicEnable\]](#) = 1.
3. Only if the system is in PIC mode, program [D0F0xFC_x00\[IoapicSbFeatureEn\]](#) = 1. This bit should be programmed to 0 when the system is in APIC mode.

The IOAPIC has a total of 29 interrupt inputs. These inputs are as follows:

- 5 groups of PCIe interrupts each having a 4-bit external interrupt bus (INT A/B/C/D) and a 1-bit bridge interrupt, and
- a 4-bit external interrupt bus from GBIF.

The recommended interrupt routing and swizzling configuration is as shown in [Table 61](#).

Table 61: Recommended Interrupt Routing and Swizzling Configuration

Device	Register	Setting	Description
Dev2Fn1	D0F0xFC_x10[BrExtIntrGrp]	0h	Map INT A/B/C/D to interrupt 0/1/2/3. Map bridge interrupt to interrupt 24.
	D0F0xFC_x10[BrExtIntrSwz]	0h	
	D0F0xFC_x10[BrIntIntrMap]	18h	
Dev2Fn2	D0F0xFC_x11[BrExtIntrGrp]	1h	Map INT A/B/C/D to interrupt 4/5/6/7. Map bridge interrupt to interrupt 25.
	D0F0xFC_x11[BrExtIntrSwz]	0h	
	D0F0xFC_x11[BrIntIntrMap]	19h	
Dev2Fn3	D0F0xFC_x12[BrExtIntrGrp]	2h	Map INT A/B/C/D to interrupt 8/9/10/11. Map bridge interrupt to interrupt 26.
	D0F0xFC_x12[BrExtIntrSwz]	0h	
	D0F0xFC_x12[BrIntIntrMap]	1Ah	
Dev2Fn4	D0F0xFC_x13[BrExtIntrGrp]	3h	Map INT A/B/C/D to interrupt 12/13/14/15. Map bridge interrupt to interrupt 27.
	D0F0xFC_x13[BrExtIntrSwz]	0h	
	D0F0xFC_x13[BrIntIntrMap]	1Bh	
Dev2Fn5	D0F0xFC_x14[BrExtIntrGrp]	4h	Map INT A/B/C/D to interrupt 16/17/18/19. Map bridge interrupt to interrupt 24.
	D0F0xFC_x14[BrExtIntrSwz]	0h	
	D0F0xFC_x14[BrIntIntrMap]	18h	
GBIF	D0F0xFC_x0F[GBIFExtIntrGrp]	5h	Map INT A/B/C/D to interrupt 20/21/22/23.
	D0F0xFC_x0F[GBIFExtIntrSwz]	0h	

2.11.3 Links

2.11.3.1 Overview

There is one 5 x8 PCIe core with five configurable ports. These ports can be divided into 2 groups:

- Gfx: Contains 1 x4 port to create a 4-bit Gfx lane using the upper 4 lanes of the PCIe core.
- GPP: Contains upto 4 General Purpose Ports (GPP) using the lower 4 lanes of the PCIe core.

All PCIe links are capable of supporting Gen1/Gen2 data rates. Function 0 in Device 2 does not control any

hardware. It is always enabled and allows software to scan through all the functions of the device.

Gfx and GPP ports each have a Type 1 Virtual PCI-to-PCI bridge header in the PCI configuration space mapped to devices according to [Figure 7](#).

Each PCIe lane is assigned a unique lane ID that software uses to communicate configuration information to the SMU. [Table 88](#) shows the mapping between lane ID's and lanes.

2.11.3.2 Link Configurations

Lanes of the Gfx ports can be assigned to IO links.

- For each 1x lane, program [D0F0xE4_x0130_0\[C:8\]04](#)[StrapBifMaxPayloadSupport]=1h. Max Payload Support = 256 for performance.

The following link configurations are supported for the GPP links:

Table 62: Supported General Purpose (GPP) Link Configurations

D0F0xE4		GPP Port Lane					
x0130_0080	x0110_0011	Lanes[7:4]	3	2	1	0	
0000_0001h	0000_0300h	x4 Link (Gfx)	x4 Link				
0000_0002h	0000_0203h	x4 Link (Gfx)	x2 Link		x2 Link		
0000_0003h	0000_0201h	x4 Link (Gfx)	x1 Link	x1 Link	x2 Link		
0000_0004h	0000_0200h	x4 Link (Gfx)	x1 Link	x1 Link	x1 Link	x1 Link	

2.11.4 Root Complex Configuration

2.11.4.1 LPC MMIO Requirements

To ensure proper operation of LPC generated DMA requests, the FCH must be configured to send processor generated MMIO writes that target the LPC bus to the FCH as non-posted writes. The MMIO address space of the LPC bus must not be included in the ranges specified by [D18F1x\[2CC:2A0,1CC:180,BC:80\]](#) [MMIO Base/Limit] and non-posted protocol for memory writes must be enabled using the following programming before LPC DMA transactions are initiated.

- Program [D0F0x98_x06](#)[UmiNpMemWrEn] = 1.

2.11.4.2 Configuration for non-FCH Bridges

BIOS should program the following in non-FCH bridges:

- Program [D0F0xCC_x01](#)[CrsEnable] = 1 for [D0F0xC8](#)[NbDevIndSel] = 11h-15h.
- Program [D0F0xCC_x01](#)[SetPowEn] = 1 for [D0F0xC8](#)[NbDevIndSel] = 11h-15h.

2.11.4.3 Link Configuration and Initialization

Link configuration and initialization is performed by the following sequence:

- 2.11.4.3.1 [Link Configuration and Core Initialization]
- 2.11.4.3.2 [Link Training]
- 2.11.4.5 [Link Power Management]
- Lock link configuration registers.

- Program [D0F0xE4_x0140_0010](#)[HwInitWrLock] = 1.
- Program [D0F0x64_x00](#)[HwInitWrLock] = 1.

2.11.4.3.1 Link Configuration and Core Initialization

Link configuration is done on a per link basis. Lane reversal, IO link selection, and lane enablement is configured through this sequence.

1. Place software-reset module into blocking mode:
 - A. Program [D0F0xE4_x0130_8062](#)[ConfigXferMode]=0.
 - B. Program [D0F0xE4_x0130_8062](#)[BlockOnIdle]=0.
2. If the link is an IO link, Program [D0F0xE4_x0140_0011](#)[DynClkLatency]=Fh.
3. Program [D0F0xE4_x0130_0080](#) per [Table 62](#).
4. Program [D0F0xE4_x0130_802\[4:1\]](#) per [Table 62](#).
5. Program [D0F0xE4_x0110_0010](#)[RxDetectTxPwrMode]=1.
6. Program [D0F0xE4_x0110_0010](#)[Ls2ExitTime]=000b.
7. Program [D0F0xE4_x0130_8013](#)[MasterPciePllA, MasterPciePllB] per [Table 62](#).
8. Initiate core reconfiguration sequence:
 - A. Program [D0F0xE4_x0130_8062](#)[ReconfigureEn]=1.
 - B. Program [D0F0xE4_x0130_8060](#)[Reconfigure]=1.
 - C. Wait for [D0F0xE4_x0130_8060](#)[Reconfigure]==0.
 - D. Program [D0F0xE4_x0130_8062](#)[ReconfigureEn]=0.
9. Return software-reset module to non-blocking mode:
 - A. Program [D0F0xE4_x0130_8062](#)[ConfigXferMode]=1.
10. Program [D2F\[5:1\]xE4_xC1](#)[StrapReverseLanes] if necessary.
11. Program [D0F0xE4_x0110_0011](#) per [Table 62](#).
12. For each nibble that has no PCIe lanes in use:
 - A. Program [D0F0xE4_x0110_001\[8:7,3:2\]](#)[PllPowerStateInOff]=111b.
 - B. Program [D0F0xE4_x0110_001\[8:7,3:2\]](#)[PllPowerStateInTxs2]=111b.
 - C. Program [D0F0xE4_x0110_001\[8:7,3:2\]](#)[TxPowerStateInTxs2]=111b.
 - D. Program [D0F0xE4_x0110_001\[8:7,3:2\]](#)[RxPowerStateInRxs2]=111b.
13. For each lane that is not in use, program the corresponding [D0F0xE4_x0130_8029](#)[LaneEnable]=0.
14. Configure PIF parings:
 - A. Program D0F0xE4_x0110_0011=0000_0300h.

2.11.4.3.2 Link Training

Link training is performed on a per link basis. BIOS may train the links in parallel.

2.11.4.4 Miscellaneous Features

2.11.4.4.1 Lane Reversal

Normally, the lanes of each port are physically numbered from n-1 to 0 where n is the number of lanes assigned to the port. Physical lane numbering can be reversed according to the following methods:

- To reverse the physical lane numbering for a specific port, program [D2F\[5:1\]xE4_xC1](#)[StrapReverseLanes]=1.
- To reverse the physical lane numbering for all ports in the GPP or GFX interfaces, program [D0F0xE4_x0140_00C0](#)[StrapReverseAll]=1.

Note that logical port numbering is established during link training regardless of the physical lane numbering.

2.11.4.4.2 Link Speed Changes

Link speed changes can only occur on Gen2 capable links. To verify that Gen2 speeds are supported verify D2F[5:1]x64[LinkSpeed]==02h.

2.11.4.4.2.1 Autonomous Link Speed Changes

To enable autonomous speed changes on a per port basis:

1. Program D2F[5:1]x88[TargetLinkSpeed]=2h.
2. Program D0F0xE4_x0130_0[C:8]03[StrapBifDeemphasisSel]=1.
3. Program D2F[5:1]xE4_xA4[LcGen2EnStrap]=1.
4. Program D2F[5:1]xE4_xC0[StrapAutoRcSpeedNegotiationDis]=0.
5. Program D2F[5:1]xE4_xA4[LcMultUpstreamAutoSpdChngEn]=1.
6. Program D2F[5:1]xE4_xA2[LcUpconfigureDis]=0.

2.11.4.4.3 Deemphasis

Deemphasis strength can be changed on a per-port basis by programming D2F[5:1]xE4_xB5[LcSelectDeemphasis].

2.11.4.5 Link Power Management

2.11.4.5.1 Link States

To enable support for L1 program D2F[5:1]xE4_xA0[LcL1Inactivity]=6h.

To enable support for L0s:

- Program D2F[5:1]xE4_xA1[LcDontGotoL0sifL1Armed]=1.
- Program D2F[5:1]xE4_xA0[LcL0sInactivity]=9h.

2.11.4.5.2 Dynamic Link-width Control

Dynamic link-width control is a power saving feature that reconfigures the link to run with fewer lanes. The inactive lanes are turned off to conserve power.

The Gfx link can switch among widths of: x1, x2, and x4, upto the maximum programmed port width.

The GPP link can switch among widths of: x1, x2, and x4, upto the maximum programmed port width.

The link width is controlled by the following 3 mechanisms:

- Up/Down Reconfiguration: The link is retrained according to the PCI Express specification. This mechanism is only available between Gen2 devices. .

The core has the capability to turn off the inactive lanes of trained links. To enable this feature program D2F[5:1]xE4_xA2[LcDynLanesPwrState]=11b.

2.11.4.6 Link Test and Debug Features

2.11.4.6.1 Compliance Mode

To enable Gen1 software compliance mode program D2F[5:1]xE4_xC0[StrapForceCompliance]=1 for each port to be placed in compliance mode.

To enable Gen2 software compliance mode:

1. BIOS enables Gen2 capability by programming [D0F0xE4_x0140_00C1](#)[StrapGen2Compliance]=1.
2. Program [D2F\[5:1\]xE4_xA4](#)[LcGen2EnStrap]=1.
3. Program [D2F\[5:1\]x88](#)[TargetLinkSpeed]=2h for each port to be placed in compliance mode.
4. Program [D2F\[5:1\]x88](#)[EnterCompliance]=1 for each port to be placed in compliance mode.

2.11.5 BIOS Timer

The root complex implements a 32-bit microsecond timer (see [D0F0xE4_x0130_80F0](#) and [D0F0xE4_x0130_80F1](#)) that the BIOS can use to accurately time wait operations between initialization steps.

To ensure that BIOS waits a minimum number of microseconds between steps BIOS should always wait for one microsecond more than the required minimum wait time.

2.11.6 PCIe Client Interface Control

This interface is accessed through the indexed space registers located at D0F2xF8 within the [Device 0 Function 2 Configuration Registers](#).

BIOS should perform the following steps to initialize the interface:

1. Program [D0F0x64_x0D](#)[PciDev0Fn2RegEn] = 1h.
2. Program credits for the BIF client as follows:
 - A. Program [D0F2xFC_x32_L1i\[1\]](#)[DmaNpHaltDis] = 1h.
 - B. Program [D0F2xFC_x32_L1i\[1\]](#)[DmaBufCredits] = 8h.
 - C. Program [D0F2xFC_x32_L1i\[1\]](#)[DmaBufMaxNpCred] = 8h.
3. Program credits for the PPD client as follows:
 - A. Program [D0F2xFC_x32_L1i\[0\]](#)[DmaBufCredits] = 8h.
 - B. Program [D0F2xFC_x32_L1i\[0\]](#)[DmaBufMaxNpCred] = 7h.
4. Program credits for the INTGEN client as follows:
 - A. Program [D0F2xFC_x32_L1i\[2\]](#)[DmaBufCredits] = 4h.
 - B. Program [D0F2xFC_x32_L1i\[2\]](#)[DmaBufMaxNpCred] = 4h.
5. Program clock gating as follows:
 - A. Program D0F2xFC_x33[L1DmaClkgateEn] = 1h.
 - B. Program D0F2xFC_x33[L1CacheClkgateEn] = 1h.
 - C. Program D0F2xFC_x33[L1CpslvClkgateEn] = 1h.
 - D. Program D0F2xFC_x33[L1DmaInputClkgateEn] = 1h.
 - E. Program D0F2xFC_x33[L1PerfClkgateEn] = 1h.
 - F. Program D0F2xFC_x33[L1MemoryClkgateEn] = 1h.
 - G. Program D0F2xFC_x33[L1RegClkgateEn] = 1h.
 - H. Program D0F2xFC_x33[L1HostreqClkgateEn] = 1h.
 - I. Program D0F2xFC_x33[L1L2ClkgateEn] = 1h.
6. Program [D0F0x64_x0D](#)[PciDev0Fn2RegEn] = 0h.

2.12 System Management Unit (SMU)

The system management unit (SMU) is a subcomponent of the northbridge that is responsible for a variety of system and power management tasks during boot and runtime. The SMU contains a Lattice LM32 microcontroller to assist with many of these tasks.

2.12.1 Software Interrupts

The microcontroller can be interrupted to cause it to perform several initialization and runtime tasks. BIOS and ACPI methods can interrupt the SMU to request a specific action using the following sequence:

1. If a service request requires an argument, program [D0F0xBC_xC210_003C](#)[Argument] with the desired argument.
1. Wait for [D0F0xBC_xC210_0004](#)[IntDone]==1.
2. Program [D0F0xBC_xC210_0000](#)[ServiceIndex] to the desired service index and toggle. This may be done in a single write.
3. Wait for [D0F0xBC_xC210_0004](#)[IntAck]==1.

After performing the steps above, software may continue execution before the interrupt has been serviced. However, software should not rely on the results of the interrupt until the service is complete (see [D0F0xBC_xC210_0004](#)[IntDone]). Interrupting the SMU with a service index that does not exist results in undefined behavior.

Table 63: SMU Software Interrupts

Service Index	Notes
1Eh	Description: BIOSSMC_MSG_LCLK_DPM_ENABLE . Enables LCLK DPM. See 2.5.6.1.3 [LCLK DPM] .
	Input: D0F0xBC_x3FDC8
	Output: None.
3Ah	Description: BIOSSMC_MSG_VDDNB_REQUEST . Request VDDNB voltage.
	Input: Program argument to desired voltage (encoded in mV with two fraction bits). Values outside D18F5x17C [MaxVid, MinVid] range are invalid and result in undefined behavior. <ul style="list-style-type: none"> • D0F0xBC_xC210_003C[Argument] = (Desired Voltage in mV) * 4.
	Output: None.
43h	Description: BIOSSMC_MSG_NBDPM_Enable . Enables NB P-state Adjustments.
	Input: D0F0xBC_x3F9E8
	Output: D0F0xBC_x3F9EC

2.13 Graphics Processor (GPU)

The APU contains an integrated DX11 compliant graphics processor.

2.13.1 Graphics Memory Controller (GMC)

The graphics memory controller is responsible for servicing memory requests from the different blocks within the GPU and forwarding routing them to the appropriate interface. The GMC is also responsible for translating

GPU virtual address to GPU physical addresses and for translating GPU physical addresses to system addresses.

2.13.2 Frame Buffer (FB)

The frame buffer is defined as the portion of system memory dedicated for GPU use.

Table 64: Recommended Frame Buffer Configurations

System Memory Size	Frame Buffer Size
< 1GB	64 MB
= 1GB & < 2GB	256 MB
= 2GB	512 MB

2.14 RAS Features

2.14.1 Machine Check Architecture

The processor contains logic and registers to detect, log, and correct errors in the data or control paths in each core and the Northbridge. The Machine Check Architecture (MCA) defines the facilities by which processor and system hardware errors are logged and reported to system software. This allows system software to perform a strategic role in recovery from and diagnosis of hardware errors.

Refer to the AMD64 Architecture Programmer's Manual for an architectural overview and methods for determining the processor's level of MCA support. See [1.2 \[Reference Documents\]](#).

The ability of hardware to generate a machine check exception upon an error is indicated by [CPUID Fn0000_0001_EDX\[MCE\]](#) or [CPUID Fn8000_0001_EDX\[MCE\]](#).

2.14.1.1 Machine Check Registers

[CPUID Fn0000_0001_EDX\[MCA\]](#) or [CPUID Fn8000_0001_EDX\[MCA\]](#) indicates the presence of the following machine check registers:

- [MSR0000_0179 \[Global Machine Check Capabilities \(MCG_CAP\)\]](#)
 - Reports how many machine check register banks are supported.
- [MSR0000_017A \[Global Machine Check Status \(MCG_STAT\)\]](#)
 - Provides basic information about processor state after the occurrence of a machine check error.
- [MSR0000_017B \[Global Machine Check Exception Reporting Control \(MCG_CTL\)\]](#)
 - Used by software to enable or disable the logging and reporting of machine check errors in the error-reporting banks.

The error-reporting machine check register banks supported in this processor are:

- MC0: Data cache (DC).
 - MC1: Instruction cache (IC).
 - MC2: Bus unit (BU), including L2 cache.
 - MC3: Reserved.
 - MC4: Northbridge (NB), including the IO link. These MSRs are also accessible from configuration space. There is only one NB error-reporting bank, independent of the number of cores.
 - MC5: Fixed-issue reorder buffer (FR) machine check registers.
-
- The register types within each bank are:
 - [MCi_CTL](#), Machine Check Control: Enables error reporting via machine check exception. The [MCi_CTL](#) register in each bank must be enabled by the corresponding enable bit in [MCG_CTL](#) ([MSR0000_017B](#)).
 - [MCi_STATUS](#), Machine Check Status: Logs information associated with errors.
 - [MCi_ADDR](#), Machine Check Address: Logs address information associated with errors.
 - [MCi_MISC](#), Machine Check Miscellaneous: Log miscellaneous information associated with errors, as defined by each error type.
 - [MCi_CTL_MASK](#), Machine Check Control Mask: Inhibit detection of an error source unless otherwise specified.

The following table identifies the registers associated with each error-reporting machine check register bank:

Table 65: MCA register cross-reference table

Register Bank (MCi)	MCA Register				
	CTL	STATUS	ADDR	MISC	CTL_MASK
MC0	MSR0000_0400	MSR0000_0401	MSR0000_0402	MSR0000_0403	MSRC001_0044
MC1	MSR0000_0404	MSR0000_0405	MSR0000_0406	MSR0000_0407	MSRC001_0045
MC2	MSR0000_0408	MSR0000_0409	MSR0000_040A	MSR0000_040B	MSRC001_0046
MC3	MSR0000_040C	MSR0000_040D	MSR0000_040E	MSR0000_040F	MSRC001_0047
MC4	MSR0000_0410	MSR0000_0411	MSR0000_0412	MSR0000_0413	MSRC001_0048
MC5	MSR0000_0414	MSR0000_0415	MSR0000_0416	MSR0000_0417	MSRC001_0049

Corrected, deferred, and uncorrected errors are logged in MCi_STATUS and MCi_ADDR as they occur. Uncorrected errors that are enabled in MCi_CTL result in a Machine Check exception.

Each MCi_CTL register must be enabled by the corresponding enable bit in [MSR0000_017B \[Global Machine Check Exception Reporting Control \(MCG_CTL\)\]](#).

MCi_CTL_MASK allow BIOS to mask the presence of any error source from software for test and debug. When error sources are masked, it is as if the error was not detected. Such masking consequently prevents error responses and actions.

Each MCA bank implements a number of machine check miscellaneous registers, denoted as MCi_MISCj, where j goes from 0 to a maximum of 8. If there is more than one MCi_MISC register in a given bank, a non-zero value in MCi_MISC0[BlkPtr] points to the contiguous block of additional registers.

The presence of valid information in the first MISC register in the bank (MCi_MISC0) is indicated by MCi_STATUS[MiscV]. The presence of valid information in additional implemented MISC registers is indicated by MCi_MISCj[Val] in the target register.

2.14.1.2 Machine Check Errors

The classes of machine check errors are, in priority order from highest to lowest:

- Uncorrected
- Deferred
- Corrected

Uncorrected errors cannot be corrected by hardware and may cause loss of data, corruption of processor state, or both. Uncorrected errors update the status and address registers if not masked from logging in MCi_CTL_MASK. Information in the status and address registers from a previously logged lower priority error is overwritten. Previously logged errors of the same priority are not overwritten. Uncorrected errors that are enabled in MCi_CTL result in reporting to software via machine check exceptions. If an uncorrected error is masked from logging, the error is ignored by hardware (exceptions are noted in the register definitions). If an uncorrected error is disabled from reporting, containment of the error and logging/reporting of subsequent errors may be affected. Therefore, enable reporting of unmasked uncorrected errors for normal operation. Disable reporting of uncorrected errors only for debug purposes.

Deferred errors are errors that cannot be corrected by hardware, but do not cause an immediate interruption in

program flow, loss of data integrity, or corruption of processor state. These errors indicate that data has been corrupted but not consumed; no exception is generated because the data has not been referenced by a core or an IO link. Hardware writes information to the status and address registers in the corresponding bank that identifies the source of the error if deferred errors are enabled for logging. If there is information in the status and address registers from a previously logged lower priority error, it is overwritten. Previously logged errors of the same or higher priority are not overwritten. Deferred errors are not reported via machine check exceptions; they can be seen by polling the MCi_STATUS registers.

Corrected errors are those which have been corrected by hardware and cause no loss of data or corruption of processor state. Hardware writes the status and address registers in the corresponding register bank with information that identifies the source of the error if they are enabled for logging. Corrected errors are not reported via machine check exceptions. Some corrected errors may be reported to software via error thresholding (see [2.14.1.7 \[Error Thresholding\]](#)).

The implications of these categories of errors are:

1. Uncorrected error; hardware did not deal with the problem.
 - Operationally (error handling), action required, because program flow is affected.
 - Diagnostically (fault management), software may collect information to determine if any components should be de-configured or serviced.
2. Deferred error; hardware partially dealt with the problem via containment.
 - Operationally, action optional, because program flow has not been affected. However, steps may be taken by software to prevent access to the data in error.
 - Diagnostically, software may collect information to determine if any components should be de-configured or serviced.
3. Corrected error; hardware dealt with the problem.
 - Operationally, no action required, because program flow is unaffected.
 - Diagnostically, software may collect information to determine if any components should be de-configured or serviced.

Machine check conditions can be simulated to aid in debugging machine check handlers. See [2.14.3 \[Error Injection and Simulation\]](#) for more detail.

2.14.1.3 Error Detection, Action, Logging, and Reporting

Error detection is controlled by the MASK registers:

- Error detection for MCA controlled errors is enabled if not masked by MCi_CTL_MASK (see [Table 65 \[MCA register cross-reference table\]](#)).
- Error masking is performed regardless of MCA bank enablement in MCG_CTL ([MSR0000_017B](#)).

Error action refers to the hardware response to an error, aside from logging and reporting. Enablement of error action for each error is enumerated in the EAC (Error Action Condition) column of the error descriptions tables as follows:

- D: Detected. The error action is taken if the error is detected (i.e., not masked). These actions occur regardless of whether the MCA bank is enabled in MCG_CTL.
- E: Enabled. The error action is taken if the error is detected and the bank is enabled in MCG_CTL.

Error logging refers to the storing of information in the status registers, and is enabled if all of the following are true:

- Error detection is enabled.
- The MCA bank is enabled in MCG_CTL.

Error reporting refers to active notification of errors to software via machine check exceptions, and is enabled if all of the following are true:

- Error logging is enabled.
- The corresponding enable bit for the error in MC_i_CTL is set to 1.

A machine check exception will be generated if all the following are true:

- The error is uncorrected.
- The error is enabled for reporting.
- CR4.MCE is enabled.

Notes:

1. If CR4.MCE is clear, an error configured to cause a machine check exception will cause a shutdown.
2. If error reporting is disabled, the setting of CR4.MCE has no effect.
3. If an uncorrected error is disabled from reporting, containment of the error and logging/reporting of subsequent errors may be affected. Therefore, unmasked uncorrected errors should be enabled for reporting for normal operation. Uncorrected errors should only be disabled from reporting for debug purposes.
4. Errors not associated with a specific core are reflected to core 0 of the compute unit. The error description tables identify which errors are associated or not associated with a specific core of the compute unit.

Throughout the MCA register descriptions, the terms “enabled” and “disabled” generally refer to reporting, and the terms “masked” and “unmasked” generally refer to logging, unless otherwise noted.

Some logged errors increment a counter in MC_i_MISC, which may trigger an interrupt (see [2.14.1.7 \[Error Thresholding\]](#)). Although no machine check exception will be generated, these notifications can be viewed as “correctable machine check interrupts”.

For debug observability only, [D18F3x180\[ConvertUnCorToCorErrEn\]](#) can be used to log NB uncorrected errors as corrected errors.

2.14.1.3.1 MCA conditions that cause Shutdown

The following architectural conditions cause the processor to enter the Shutdown state; see section “Machine-Check Errors” in APM volume 2 for more detail; see [1.2 \[Reference Documents\]](#):

- Attempting to generate an MCE when machine check reporting is disabled at the system level (CR4.MCE=0).
- Attempting to generate an MCE when a machine check is in progress on the same core ([MSR0000_017A\[MCIP\]](#)=1).

The following non-architectural conditions cause the processor to enter the Shutdown state:

- On MCA interrupts, if two or more uncorrected errors occur across MCA banks.

2.14.1.3.2 Error Logging During Overflow

An error to be logged when the status register contains valid data can result in an overflow condition. During error overflow conditions, the new error may not be logged or an error which has already been logged in the status register may be overwritten. For the rules on error overflow, priority, and overwriting, see [MSR0000_0401\[Overflow\]](#).

Overflow alone does not indicate a shutdown condition. Uncorrected errors require software intervention. Therefore, when an uncorrected error cannot be logged, critical error information may have been lost, and MC_i_STATUS[PCC] may be set. If PCC is indicated, software should terminate system processing to prevent

data corruption (see [2.14.1.6 \[Handling Machine Check Exceptions\]](#)). If PCC is not indicated, any MCA data lost due to overflow was informational only and not critical to system hardware operation.

Table 66: Overwrite Priorities for All Banks

			Older Error			
			Uncorrected		Corrected	
			Enabled	Disabled	Enabled	Disabled
Newer Error	Uncorrected	Enabled	- ¹	- ¹	Overwrite	Overwrite
		Disabled	- ¹	- ¹	Overwrite	Overwrite
	Corrected	Enabled	-	-	-	-
		Disabled	-	-	-	-

2.14.1.4 MCA Initialization

The following initialization sequence must be followed:

- MCi_CTL_MASK registers (see [Table 65 \[MCA register cross-reference table\]](#) for list):
 - BIOS must initialize the mask registers to inhibit error detection prior to the initialization of MCi_CTL and [MSR0000_017B](#).
 - BIOS must not clear MASK bits that are reset to 1.
- The MCi_CTL registers must be initialized by the operating system prior to enabling the error reporting banks in MCG_CTL.

If initializing after a cold reset (see [D18F0x6C\[ColdRstDet\]](#)), then BIOS must clear the MCi_STATUS MSRs. If initializing after a warm reset, then BIOS should check for valid MCA errors and if present save the status for later diagnostic use (see [2.14.1.6 \[Handling Machine Check Exceptions\]](#)).

BIOS may initialize the MCA without setting CR4.MCE; this will result in a system shutdown on any machine check which would have caused a machine check exception (followed by a reboot if configured in the chipset). Alternatively, BIOS that wishes to ensure continued operation in the event that a machine check occurs during boot may write MCG_CTL with all ones and write zeros into each MCi_CTL. With these settings, a machine check error will result in MCi_STATUS being written without generating a machine check exception or a system shutdown. BIOS may then poll MCi_STATUS during critical sections of boot to ensure system integrity. Before passing control to the operating system, BIOS should restore the values of those registers to what the operating system is expecting. (Note that using MCi_CTL to disable error reporting on uncorrected errors may affect error containment; see [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).)

Before ECC memory has been initialized with valid ECC check bits, BIOS must ensure that no memory operations are initiated if MCA reporting is enabled. This includes memory operations that may be initiated by hardware prefetching or other speculative execution. It is recommended that, until all of memory has been initialized with valid ECC check bits, the BIOS either does not have any valid MTRRs specifying a DRAM memory type or does not enable DRAM ECC machine check exceptions.

2.14.1.5 Error Code

The MCi_STATUS[ErrorCode] field contains information used to identify the logged error. [Table 67 \[Error Code Types\]](#) identifies how to decode ErrorCode. The MCi_STATUS[ErrorCodeExt] field contains detailed, model-specific information that is used to further narrow identification for error diagnosis, but not error handling by software; see [2.14.1.6 \[Handling Machine Check Exceptions\]](#).

For a given error-reporting bank, Error Code Type is used in conjunction with the Extended Error Code (MC_i_STATUS[ErrorCodeExt]) to uniquely identify the Error Type; the value of ErrorCodeExt is unique within Error Code Type. Details for each Error Type are described in the tables accompanying the MC_i_STATUS register for each bank.

- MC0 (DC); [Table 196 \[MC0 Error Signatures\]](#).
- MC1 (IC); [Table 199 \[MC1 Error Signatures\]](#).
- MC2 (BU); [Table 202 \[MC2 Error Signatures\]](#)
- MC4 (NB); [Table 205 \[MC4 Error Signatures, Part 1\]](#) and [Table 206 \[MC4 Error Signatures, Part 2\]](#).
- MC5 (FR); [Table 214 \[MC5 Error Signatures\]](#).

Table 67: Error Code Types

Error Code	Error Code Type	Description
0000 0000 0001 TTLL	TLB	TT = Transaction Type LL = Cache Level
0000 0001 RRRR TTLL	Memory	Errors in the cache hierarchy (not in NB) RRRR = Memory Transaction Type TT = Transaction Type LL = Cache Level
0000 1PPT RRRR II LL	Bus	General bus errors including link and DRAM PP = Participation Processor T = Timeout RRRR = Memory Transaction Type II = Memory or IO LL = Cache Level
0000 01UU 0000 0000	Internal Unclassified	Internal unclassified errors UU = Internal Error Type

Table 68: Error codes: transaction type (TT)

TT	Transaction Type
00	Instr: Instruction
01	Data
10	Gen: Generic
11	Reserved

Table 69: Error codes: cache level (LL)

LL	Cache Level
00	L0: Emulation memory
01	L1: Level 1
10	L2: Level 2
11	LG: Generic

Table 70: Error codes: memory transaction type (RRRR)

RRRR	Memory Transaction Type
0000	Gen: Generic. Includes scrub errors.

Table 70: Error codes: memory transaction type (RRRR)

RRRR	Memory Transaction Type
0001	RD: Generic Read
0010	WR: Generic Write
0011	DRD: Data Read
0100	DWR: Data Write
0101	IRD: Instruction Fetch
0110	Prefetch
0111	Evict
1000	Snoop (Probe)

Table 71: Error codes: participation processor (PP)

PP	Participation Processor
00	SRC: Local node originated the request
01	RES: Local node responded to the request
10	OBS: Local node observed the error as a third party
11	Generic

Table 72: Error codes: memory or IO (II)

II	Memory or IO
00	Mem: Memory Access
01	Reserved
10	IO: IO Access
11	Gen: Generic

Table 73: Error codes: Internal Error Type (UU)

UU	Internal Error Type
00	Reserved
01	Reserved
10	HWA: Hardware Assertion
11	Reserved

2.14.1.6 Handling Machine Check Exceptions

A machine check handler is invoked to handle an exception for a particular core. Because MCA registers are generally not shared among cores, the handler does not need to coordinate register usage with handler instances on other cores. Those few MCA registers which are shared are noted in the register description. (See also [2.4.2.1 \[Registers Shared by Cores in a L2 complex.\]](#).)

For access to the core MC2 registers, [MSRC001_10A0](#)[McaToMstCoreEn] allows a single core to access the registers through MSR space without contention from other cores. This organization of registers on a per core basis allows independent execution, simplifies exception handling, and reduces the number of conditions which are globally fatal.

For access to the NB MCA registers, [D18F3x44](#)[NbMcaToMstCpuEn] allows a single core (the NBC) to access the registers through MSR space without contention from other cores. This organization of registers on a per core basis allows independent execution, simplifies exception handling, and reduces the number of conditions which are globally fatal.

At a minimum, the machine check handler must be capable of logging error information for later examination. The handler should log as much information as is needed to diagnose the error.

More thorough exception handler implementations can analyze errors to determine if each error is recoverable by software. If a recoverable error is identified, the exception handler can attempt to correct the error and restart the interrupted program. An error may not be recoverable for the process or virtual machine it directly affects, but may be containable, so that other processes or virtual machines in the system are unaffected and system operation is recovered; see [2.14.1.6.1 \[Differentiation Between System-Fatal and Process-Fatal Errors\]](#).

Machine check exception handlers that attempt to recover must be thorough in their analysis and the corrective actions they take. The following guidelines should be used when writing such a handler:

- Data collection:

- All status registers in all error reporting banks must be examined to identify the cause of the machine check exception.
 - Read [MSR0000_0179](#)[Count] to determine the number of status registers visible to the core. The status registers are numbered from 0 to one less than the value found in [MSR0000_0179](#)[Count]. For example, if the Count field indicates five status registers are supported, they are numbered MC0_STATUS to MC4_STATUS. These are generically referred to as MC_i_STATUS.
 - Check the valid bit in each status register (MC_i_STATUS[Val]). The remainder of the status register should be examined only when its valid bit is set.
 - When identifying the error condition and determining how to handle the error, portable exception handlers should examine the following MC_i_STATUS fields: ErrorCode, UC, PCC, CECC, UECC, Deferred, Poison. The expected settings of these and other fields in MC_i_STATUS are identified in the error signatures tables which accompany the descriptions of each MCA status register. See [2.14.1.5 \[Error Code\]](#) for a discussion of error codes and pointers to the error signatures tables.
 - MC_i_STATUS[ErrorCodeExt] should generally not be used by portable code to identify the error condition because it is model specific. ErrorCodeExt is useful in determining the error subtype for root cause analysis.

- Error handlers should collect all available MCA information (status register, address register, miscellaneous register, etc.), but should only interrogate details to the level which affects their actions. Lower level details may be useful for diagnosis and root cause analysis, but not for error handling.

- Recovery:

- Check the valid MC_i_STATUS registers to see if error recovery is possible.
 - Error recovery is not possible when the processor context corrupt indicator (MC_i_STATUS[PCC]) is set to 1.
 - The error overflow status indicator (MC_i_STATUS[Overflow]) does not indicate whether error recovery is possible. See [2.14.1.3.2 \[Error Logging During Overflow\]](#).
 - If error recovery is not possible, the handler should log the error information and return to the operating system for system termination.
- Check MC_i_STATUS[UC] to see if the processor corrected the error. If UC is set, the processor did not correct the error, and the exception handler must correct the error prior to attempting to restart the interrupted program. If the handler cannot correct the error, it should log the error information and return to the operating system. If the error affects only process data, it may be possible to terminate only the affected process or virtual machine. If the error affects processor state, continued use of that processor should not occur. See individual error descriptions for further guidance.

- If [MSR0000_017A\[RIPV\]](#) is set, the interrupted program can be restarted reliably at the instruction pointer address pushed onto the exception handler stack if any uncorrected error has been corrected by software. If RIPV is clear, the interrupted program cannot be restarted reliably, although it may be possible to restart it for debugging purposes. As long as PCC is clear, it may be possible to terminate only the affected process or virtual machine.
- When logging errors, particularly those that are not recoverable, check [MSR0000_017A\[EIPV\]](#) to see if the instruction pointer address pushed onto the exception handler stack is related to the machine check. If EIPV is clear, the address is not ensured to be related to the error.
- See [2.14.1.6.1 \[Differentiation Between System-Fatal and Process-Fatal Errors\]](#) for more explanation on the relationship between PCC, RIPV, and EIPV.
- Exit:
 - When an exception handler is able to successfully log an error condition, clear the MC_i_STATUS registers prior to exiting the machine check handler. Software is responsible for clearing at least MC_i_STATUS[Val].
 - Prior to exiting the machine check handler, be sure to clear [MSR0000_017A\[MCIP\]](#). MCIP indicates that a machine check exception is in progress. If this bit is set when another machine check exception occurs in the same core, the processor enters the shutdown state.

Additional machine check handler portability can be added by having the handler use the CPUID instruction to identify the processor and its capabilities. Implementation specific software can be added to the machine check exception handler based on the processor information reported by CPUID.

In cases where sync flood is the recommended response to a particular error, a machine check exception cannot be used in lieu of the sync flood to stop the propagation of potentially bad data.

2.14.1.6.1 Differentiation Between System-Fatal and Process-Fatal Errors

The bits MC_i_STATUS[PCC], [MSR0000_017A\[RIPV\]](#), and [MSR0000_017A\[EIPV\]](#) form a hierarchy, used by software to determine the degree of corruption and recoverability in the system.

[Table 74](#) shows how these bits are interpreted.

Table 74: Error Scope Hierarchy

PCC	UC	RIPV	EIPV	Deferred	Poison	Comments
1	1	-	-	-	-	System fatal error. Signaled via machine check exception, action required. Error has corrupted system state (PCC=1). The error is fatal to the system and the system processing must be terminated.
0	1	1	1	-	-	RIPV=1, EIPV=0: Should not occur. Restartable errors will indicate the instruction in error in EIP.

Table 74: Error Scope Hierarchy

PCC	UC	RIPV	EIPV	Deferred	Poison	Comments
0	1	0	-	-	0/1	<p>Hardware uncorrected, software containable error. Signaled via machine check exception, action required. The error is confined to the process, however the process cannot be restarted even if the uncorrected error is corrected by software.</p> <p>Poison=1; the error is due to consumption of poison data. If the affected process or virtual machine is terminated, the system may continue operation.</p>
0	0	-	-	1	0	<p>Deferred error. Action optional. A latent error has been discovered, but not yet consumed; a machine check exception will be generated if the affected data is consumed. Error handling software may attempt to correct this data error, or prevent access by processes which map the data, or make the physical resource containing the data inaccessible.</p> <p>Note: May be detected on a demand access or a scrub access.</p>
0	0	-	-	0	0	<p>Corrected error. Signaled via error thresholding mechanisms (2.14.1.7 [Error Thresholding]); no action required.</p>

2.14.1.7 Error Thresholding

For some types of errors, the hardware maintains counts of the number of errors. When the counter reaches a programmable threshold, an event may optionally be triggered to signal software. This is known as error thresholding. The primary purpose of error thresholding is to help software recognize an excessive rate of errors, which may indicate marginal or failing hardware. This information can be used to make decisions about deconfiguring hardware or scheduling service actions. Counts are incremented for corrected, deferred, and uncorrected errors.

The error thresholding hardware counts only the number of errors; it is up to software to track the errors reported over time in order to determine the rate of errors. Thresholding gives error counts on groups of resources. In order to make decisions on individual resources, a finer granularity of error information, such as MCA information for specific errors, must be utilized in order to obtain more accurate counts and to limit the scope of actions to affected hardware.

Thresholding is performed for “Error Threshold Groups” identified in the list below. For all error threshold groups, some number of corrected errors is expected and normal. There are numerous factors influencing error rates, including temperature, voltage, operating speed, and geographic location. The determination of expected error rates is heuristic, with recommended error rates defined below. Although these recommendations are deliberately conservative, they may need to be adjusted if operating in extreme conditions. In addition, the normal error rates are for long term averages and it may not be abnormal for bursts to occur. In order to accommodate the various factors, including software latency to respond and track the error thresholding, additional guardband above the normal rates is recommended before error rates are considered abnormal for purposes of hardware action. These recommendations are for error thresholding purposes, and are not design parameters.

The {MC0, MC1, MC2, MC5} error thresholding banks maintains counters, but do not provide interrupts when the threshold is reached; these counters must be polled.

Error thresholding groups:

- DRAM (MC4)
 - Memory errors are counted and polled or reported via [MSR0000_0413](#).
 - DRAM errors are the errors listed in [Table 204 \[MC4 Error Descriptions\]](#) as “D” (DRAM) in the ETG (Error Threshold Group) column.
 - Operating systems can avoid or stop using memory pages with excessive errors.
- Links (MC4)
 - Link errors are counted and reported via [MSRC000_0408](#).
 - Link errors are the errors listed in [Table 204 \[MC4 Error Descriptions\]](#) as “L” (Cache) in the ETG (Error Threshold Group) column.
 - For a link exhibiting excessive errors, it may be possible to reduce errors by lowering the link frequency or reducing the link width (if a bad lane can be avoided). See [2.11 \[Root Complex\]](#) for details and restrictions on configuring links.

In rare circumstances, such as two simultaneous errors in the same error thresholding group, it is possible for one error not to increment the counter. In these conditions, MC_i_STATUS[Overflow] may indicate that an overflow occurred, but the error counter may only indicate one error.

2.14.1.8 Scrub Rate Considerations

This section gives guidelines for the scrub rate settings available in [D18F3x58 \[Scrub Rate Control\]](#) and [MSRC001_10A0 \[L2I Configuration \(L2I_CFG\)\]](#). Scrubbers are used to periodically read cacheline sized data locations and associated tags. There are two primary benefits to scrubbing. First, scrubbing corrects any corrected errors which are discovered before they can migrate into uncorrected errors. This is particularly important for soft errors, which are caused by external sources such as radiation and which are temporary conditions which do not indicate malfunctioning hardware. Second, scrubbers help identify marginal or failed hardware by finding and logging repeated errors at the same locations (see also [2.14.1.7 \[Error Thresholding\]](#)).

There are many factors which influence scrub rates. Among these are:

- The size of memory or cache to be scrubbed (higher rate for larger size)
- Resistance to upsets (higher rates for more sensitive technologies and lower voltages)
- Geographic location and altitude (higher rate for higher flux density of cosmic radiation)
- Alpha particle contribution of packaging (higher rate for less pure packaging)
- Performance sensitivity (lower rate for more performance sensitivity)
- Risk aversion (higher rate for higher risk aversion)

The baseline recommendations in [Table 75](#) are intended to provide excellent protection at most geographic locations, while having no measurable effect on performance or power consumption. DRAM:

F3x58[DramScrub] should be set to scrub all of memory every 24 hours, unless other guidelines are given by the DRAM vendor. Adjustments may be necessary due to special circumstances. Refer to JEDEC standards for guidelines on adjusting for geographic location.

Table 75: Recommended Scrub Rates per Node

Register	Memory Size per Node (GB)	Register Setting	Scrub Rate
MSRC001_10A0[L2ScrubberInterval]	-	100h	98.6 ms

Table 75: Recommended Scrub Rates per Node

Register	Memory Size per Node (GB)	Register Setting	Scrub Rate
D18F3x58[DramScrub]	0 GB == Size	00h	Disabled
	0 GB < Size <= 1 GB	12h	5.24 ms
	1 GB < Size <= 2 GB	11h	2.62 ms
	2 GB < Size <= 4 GB	10h	1.31 ms
	4 GB < Size <= 8 GB	0Fh	655.4 us
	8 GB < Size <= 16 GB	0Eh	327.7 us
	16 GB < Size <= 32 GB	0Dh	163.8 us
	32 GB < Size <= 64 GB	0Ch	81.9 us
	64 GB < Size <= 128 GB	0Bh	41.0 us
	128 GB < Size <= 256 GB	0Ah	20.5 us
	256 GB < Size	09h	10.2 us

For steady state operation, finding a range of useful scrub rates may be performed by selecting a scrub rate which is high enough to give good confidence about protection from accumulating errors and low enough that it has no measurable effect on performance. The above baselines are made to maximize error coverage without affecting performance and not based on specific processor soft error rates.

For low power states in which the processor core is halted, the power management configuration may affect scrubbing; see [2.8.3 \[Memory Scrubbers\]](#).

2.14.1.9 Error Diagnosis

This section describes generalized information and algorithms for diagnosing errors. The primary goal of diagnosis is to identify the failing component for repair purposes. The secondary goal is to identify the smallest possible sub-component for deallocation, deconfiguration, or design/manufacturing root cause analysis.

Indictment means identifying the part in error. The simplest form of indictment is *self-indictment*, where the bank reporting the error is the faulty unit. The next simplest form of indictment is *eyewitness indictment*, where the faulty unit is not the bank reporting the error, but is identified unambiguously. Both of these forms can be considered direct indictment; the information for indictment is contained in the MCA error information. If an error is not directly indicted, then identifying the faulty unit is more difficult and may not be an explicit part of the error log.

In general, an address logged in the MCA is useful for direct indictment only if the address identifies a physical location in error, such as a cache index. Logical addresses, while identifying the data, do not identify the location of the data.

If possible, physical storage locations in caches should be checked to determine whether the error is a soft error (a temporary upset of the stored value) or a hard fault (malfunctioning hardware). A location which has had a soft error can be corrected by writing a new value to the location; a reread of the location should see the new value. Hard faults cannot be corrected by writing a new value; the hardware persistently returns the previous value. If such checking is not possible, a grossly simplifying assumption can be made that uncorrected errors are hard and corrected errors are soft. Repeated corrected errors from the same location are an indication that the fault is actually hard.

Determining whether corrected errors represent a hard fault or a soft error requires understanding the access

patterns and any attempts to correct the faulty data in place. An attempt to correct the data in place creates two *epochs*, one before the correction event, and one after. If an error is seen at the same location in two different epochs (especially back-to-back epochs), it is more likely that the cause is a hard fault, since the error has persisted or repeated through an in place correction. The more epochs in which an error is seen, the higher the likelihood of it being caused by a hard fault.

As an example, consider a corrected error found during a read from DRAM. If the DRAM redirect scrubber is enabled ([D18F3x5C\[ScrubReDirEn\]](#)), the data in error is corrected in place, and this event conceptually creates a new epoch. If the original fault was due to a soft error, a read of the same data in the new epoch should not encounter a data error. If the original fault was due to a hard fault (e.g., a stuck bit), a read of the data in the new epoch will likely result in another corrected or uncorrected error.

There are numerous correction events that can be used to separate time periods into epochs. These include DRAM redirect scrubs, DRAM sequential scrubs, cache scrubs, cache writes, cache flushes, resets, and others.

2.14.1.9.1 Common Diagnosis Information

A common set of diagnosis information is useful for many problems. [Table 76](#) indicates the minimum set of generally useful diagnostic information that should be collected by software, unless the specifics of the problem are known to be narrower, based on the error code or other information.

It is useful to collect configuration information to ensure that the behavior is not caused by misconfiguration.

Table 76: Registers Commonly Used for Diagnosis

MCA Bank	Status	Configuration
MC0	MSR0000_0401 MSR0000_0402 MSR0000_0403	MSR0000_0400 MSRC001_1022 MSRC001_0044
MC1	MSR0000_0405 MSR0000_0406 MSR0000_0407	MSR0000_0404 MSRC001_1021
MC2	MSR0000_0409 MSR0000_040A MSR0000_040B	MSR0000_0408 MSRC001_0046 MSRC001_1023
MC3	Reserved	Reserved
MC4	MSR0000_0411 MSR0000_0412 MSR0000_0413 MSRC000_0408 D18F3x54 D18F2xAC	MSR0000_0410 MSRC001_0048 D18F3x40 D18F3x44 D18F3xE4 D18F3xE8 MSRC001_001F D18F3x188
MC5	MSR0000_0415 MSR0000_0416 MSR0000_0417	MSR0000_0414 MSRC001_1020

If examining MCA registers after startup, determine the cause of the startup:

- INIT; [D18F0x6C\[InitDet\]](#).
- Cold reset; [D18F0x6C\[ColdRstDet\]](#).
- Warm reset; if not INIT or cold reset.

To see if a link failure occurred, examine [D18F0x\[E4,C4,A4,84\]\[LinkFail\]](#). If set, look for additional information:

- Receipt of a sync, such as during a sync flood, saves a status of Sync Error in MC4_STATUS.
- CRC error saves a status of CRC Error in MC4_STATUS. See [D18F0x\[E4,C4,A4,84\]\[CrcErr,Crc-FloodEn\]](#).
- Link not present does not save status in MC4_STATUS. See [D18F0x\[E4,C4,A4,84\]\[InitComplete\]](#).

Other registers may be needed depending on the specific error symptoms.

2.14.2 DRAM ECC Considerations

DRAM is protected by an error correcting code (ECC). The DRAM error correcting code features an ECC word formed by a symbol based code. The x4 code uses thirty-six 4-bit symbols to make a 144-bit ECC word made up of 128 data bits and 16 check bits.

The x4 code is a single symbol correcting (SSC) and a double symbol detecting (DSD) code. This means the x4 code is able to correct 100% of single symbol errors (any bit error combination within one symbol), and detect 100% of double symbol errors (any bit error combination within two symbols).

2.14.2.1 ECC Syndromes

For memory errors, the sections below describe how to find the DIMM in error. The process varies slightly according to the ECC code in use. To determine which ECC code is being used, see [D18F3x180\[EccSymbol-Size\]](#).

For correctable errors, the DIMM in error is uniquely identified by the error address ([MSR0000_0412\[ErrAddr\]](#)) and the ECC syndrome ([MSR0000_0411\[Syndrome\[15:8\]\]](#) and [MSR0000_0411\[Syndrome\[7:0\]\]](#)). The error address maps to the two DIMMs composing the 128-bit line, and the ECC syndrome identifies one DIMM by identifying the symbol within the line.

2.14.2.1.1 x4 ECC

The use of x4 ECC is indicated in [D18F3x180\[EccSymbolSize\]](#).

The syndrome field uniquely identifies the failing bit positions of a correctable ECC error. Only syndromes identified by [Table 77](#) are correctable by the error correcting code.

Symbols 00h-0Fh map to data bits 0-63; symbols 10h-1Fh map to data bits 64-127; symbols 20-21h map to ECC check bits for data bits 0-63; symbols 22-23h map to ECC check bits for data bits 64-127.

To use [Table 77](#), first find the 16-bit syndrome value in the table. This is performed by using low order 4 bits of the syndrome to select the appropriate error bitmask column. The entire four digit syndrome should then be in one of the rows of that column. The Symbol In Error row indicates which symbol, and therefore which DIMM has the error, and the column indicates which bits within the symbol. To map to the DIMM, use the algorithm in [2.10.5 \[Routing DRAM Requests\]](#).

For example, if the ECC syndrome is 6913h, then symbol 05h has the error, and bits 0 and 1 within that symbol are corrupted, since the syndrome is in column 3h (0011b). Symbol 05h maps to bits 23-20, so the corrupted bits are 20 and 21.

Table 77: x4 ECC Correctable Syndromes

Symbol In Error	Error Bitmask															
	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111	
Data 0	e821	7c32	9413	bb44	5365	c776	2f57	dd88	35a9	a1ba	499b	66cc	8eed	1afe	f2df	
Data 1	5d31	a612	fb23	9584	c8b5	3396	6ea7	eac8	b7f9	4cda	11eb	7f4c	227d	d95e	846f	
Data 2	0001	0002	0003	0004	0005	0006	0007	0008	0009	000a	000b	000c	000d	000e	000f	
Data 3	2021	3032	1013	4044	6065	7076	5057	8088	a0a9	b0ba	909b	c0cc	e0ed	f0fe	d0df	
Data 4	5041	a082	f0c3	9054	c015	30d6	6097	e0a8	b0e9	402a	106b	70fc	20bd	d07e	803f	
Data 5	be21	d732	6913	2144	9f65	f676	4857	3288	8ca9	e5ba	5b9b	13cc	aded	c4fe	7adf	
Data 6	4951	8ea2	c7f3	5394	1ac5	dd36	9467	a1e8	e8b9	2f4a	661b	f27c	bb2d	7cde	358f	
Data 7	74e1	9872	ec93	d6b4	a255	4ec6	3a27	6bd8	1f39	f3aa	874b	bd6c	c98d	251e	51ff	
Data 8	15c1	2a42	3f83	cef4	db35	e4b6	f177	4758	5299	6d1a	78db	89ac	9c6d	a3ee	b62f	
Data 9	3d01	1602	2b03	8504	b805	9306	ae07	ca08	f709	dc0a	e10b	4f0c	720d	590e	640f	
Data 10	9801	ec02	7403	6b04	f305	8706	1f07	bd08	2509	510a	c90b	d60c	4e0d	3a0e	a20f	
Data 11	d131	6212	b323	3884	e9b5	5a96	8ba7	1cc8	cdf9	7eda	afeb	244c	f57d	465e	976f	
Data 12	e1d1	7262	93b3	b834	59e5	ca56	2b87	dc18	3dc9	ae7a	4fab	642c	85fd	164e	f79f	
Data 13	6051	b0a2	d0f3	1094	70c5	a036	c067	20e8	40b9	904a	f01b	307c	502d	80de	e08f	
Data 14	a4c1	f842	5c83	e6f4	4235	1eb6	ba77	7b58	df99	831a	27db	9dac	396d	65ee	c12f	
Data 15	11c1	2242	3383	c8f4	d935	eab6	fb77	4c58	5d99	6e1a	7fdb	84ac	956d	a6ee	b72f	
Data 16	45d1	8a62	cfb3	5e34	1be5	d456	9187	a718	e2c9	2d7a	68ab	f92c	bcfd	734e	369f	
Data 17	63e1	b172	d293	14b4	7755	a5c6	c627	28d8	4b39	99aa	fa4b	3c6c	5f8d	8d1e	eeff	
Data 18	b741	d982	6ec3	2254	9515	fb6d	4c97	33a8	84e9	ea2a	5d6b	11fc	a6bd	c87e	7f3f	
Data 19	dd41	6682	bbc3	3554	e815	53d6	8e97	1aa8	c7e9	7c2a	a16b	2ffc	f2bd	497e	943f	
Data 20	2bd1	3d62	16b3	4f34	64e5	7256	5987	8518	aec9	b87a	93ab	ca2c	e1fd	f74e	dc9f	
Data 21	83c1	c142	4283	a4f4	2735	65b6	e677	f858	7b99	391a	badb	5cac	df6d	9dee	1e2f	
Data 22	8fd1	c562	4ab3	a934	26e5	6c56	e387	fe18	71c9	3b7a	b4ab	572c	d8fd	924e	1d9f	
Data 23	4791	89e2	ce73	5264	15f5	db86	9c17	a3b8	e429	2a5a	6dc6	f1dc	b64d	783e	3faf	
Data 24	5781	a9c2	fe43	92a4	c525	3b66	6ce7	e3f8	b479	4a3a	1dbb	715c	26dd	d89e	8f1f	
Data 25	bf41	d582	6ac3	2954	9615	fcd6	4397	3ea8	81e9	eb2a	546b	17fc	a8bd	c27e	7d3f	
Data 26	9391	e1e2	7273	6464	f7f5	8586	1617	b8b8	2b29	595a	cacb	dcdc	4f4d	3d3e	aeaf	
Data 27	cce1	4472	8893	fdb4	3155	b9c6	7527	56d8	9a39	12aa	de4b	ab6c	678d	ef1e	23ff	
Data 28	a761	f9b2	5ed3	e214	4575	1ba6	bcc7	7328	d449	8a9a	2dfb	913c	365d	688e	cfef	
Data 29	ff61	55b2	aad3	7914	8675	2ca6	d3c7	9e28	6149	cb9a	34fb	e73c	185d	b28e	4def	
Data 30	5451	a8a2	fcf3	9694	c2c5	3e36	6a67	ebe8	bf9	434a	171b	7d7c	292d	d5de	818f	
Data 31	6fc1	b542	da83	19f4	7635	acb6	c377	2e58	4199	9b1a	f4db	37ac	586d	82ee	ed2f	

Table 77: x4 ECC Correctable Syndromes

Symbol In Error	Error Bitmask														
	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Check0	be01	d702	6903	2104	9f05	f606	4807	3208	8c09	e50a	5b0b	130c	ad0d	c40e	7a0f
Check1	4101	8202	c303	5804	1905	da06	9b07	ac08	ed09	2e0a	6f0b	f40c	b50d	760e	370f
Check2	c441	4882	8cc3	f654	3215	bed6	7a97	5ba8	9fe9	132a	d76b	adf0	69bd	e57e	213f
Check3	7621	9b32	ed13	da44	ac65	4176	3757	6f88	19a9	f4ba	829b	b5cc	c3ed	2efe	58df

2.14.3 Error Injection and Simulation

Error injection allows the introduction of errors into the system for test and debug purposes. See the following sections for error injection details:

- DRAM: See [2.14.3.1 \[DRAM Error Injection\]](#).
- Link:
 - [D18F3x44\[GenLinkSel, GenSubLinkSel, GenCrcErrByte1, GenCrcErrByte0\]](#).

Error simulation involves creating the appearance to software that an error occurred, and can be used to debug machine check interrupt handlers. This is performed by manually setting the MCA registers with desired values, and then driving the software via INT18. See [MSRC001_0015\[McStatusWrEn\]](#) for making MCA registers writable for non-zero values. When McStatusWrEn is set, privileged software can write non-zero values to the specified registers without generating exceptions, and then simulate a machine check using the INT18 instruction (INTn instruction with an operand of 18). Setting a reserved bit in these registers does not generate an exception when this mode is enabled. However, setting a reserved bit may result in undefined behavior.

2.14.3.1 DRAM Error Injection

This section gives details and examples on injecting errors into DRAM using [D18F3xBC_x8 \[DRAM ECC\]](#). The intent of DRAM error injection is to cause a discrepancy between the stored data and the stored ECC value. Therefore, DRAM error injection is only possible on DRAM which supports ECC, and in which [D18F2x90_dct\[0\]\[DimmEccEn\]](#) and [D18F3x44\[DramEccEn\]](#) are set.

The memory subsystem operates on 64-byte cachelines. The following fields are used to set how the cacheline is to be corrupted in DRAM:

- [D18F3xB8\[ArrayAddress\]](#) selects a cacheline quadrant (16-byte section) of the cacheline. Each cacheline quadrant is protected by an ECC word. Note that there are special requirements for which bits are used to specify the target quadrant.
- [D18F3xBC_x8\[ErrInjEn\]](#) selects a 16-bit word of the cacheline quadrant selected in ArrayAddress. The 16-bit word identified as ECC[15:0] refers to the bits which store the ECC value; the other 16-bit words address the data on which the ECC is calculated. One or more of these 16-bit words can be selected, and the error bitmask indicated in EccVector is applied to each of the selected words.
- [D18F3xBC_x8\[EccVector\]](#) is a bitmask which selects the individual bits to be corrupted in the 16-bit words selected by ErrInjEn. When selecting the bits to be corrupted for correctable or uncorrectable errors, consider the ECC scheme being used, including symbol size; see [2.14.2 \[DRAM ECC Considerations\]](#) for more details. Note that corrupting more than two symbols may exceed the limits of the ECC to detect the errors; for testing purposes it is recommended that no more than two symbols be corrupted in a single cacheline quadrant.

The distinction between [D18F3xBC_x8\[DramErrEn\]](#) and [D18F3xBC_x8\[EccWrReq\]](#) is that DramErrEn is used to continuously inject errors on every write. This bit is set and cleared by software. EccWrReq is used to inject an error on only one write. This bit is set by software and is cleared by hardware after the error is

injected.

When performing DRAM error injection on multi-node systems, [D18F3xB8](#) and [D18F3xBC_x8](#) of the NB to which the memory is attached must be programmed.

The following can be used to trigger the injection:

- For implicit addressing, the memory address is not an explicit parameter of the error injection interface. Once the error injection registers [D18F3xB8](#) and [D18F3xBC](#) are set, the next non-cached access of the appropriate type will trigger the mechanism and apply it to the accessed address. The access should be non-cached so that it is ensured to be seen by the memory controller. Possible methods to ensure a non-cached access include using the appropriate MTTR to set the memory type to UC or turning off caches. If it is important to know the address, then system activity must be quiesced so that the access can take place under careful software control. Once the error injection pattern is set in [D18F3xB8](#) and [D18F3xBC_x8](#):
 - Set either [D18F3xBC_x8\[EccWrReq\]](#) or [D18F3xBC_x8\[DramErrEn\]](#) to enable the triggering mechanism.
 - The next non-cached access of the appropriate type will trigger the mechanism and apply it to the accessed address.

After the error is injected, the data must be accessed in order for the error detection to be triggered. The error address logged in [MSR0000_0412](#) will correspond to the cacheline quadrant that contains the error.

When using [MSR0000_0411](#) to read MC4_STATUS after an error injection and subsequent error detection, be aware that the setting of [D18F3x44\[NbMcaToMstCpuEn\]](#) can cause different cores to see different values. Alternatively, MC4_STATUS can be read through the PCI-defined configuration space aliases [D18F3x4C](#) and [D18F3x48](#), which do not return different values to different cores, regardless of the setting of [D18F3x44\[NbMcaToMstCpuEn\]](#).

Example 1: Injecting a correctable error with implicit addressing:

- Program error pattern:
 - [D18F3xB8\[ArraySelect\]=1000b](#) // select DRAM as target
 - [D18F3xB8\[ArrayAddress\]=0000000000b](#) // select 16-byte (128-bit) section
 - [D18F3xBC_x8\[ErrInjEn\]=000000001b](#) // select 16-bit word in 16-byte section
 - [D18F3xBC_x8\[EccRdReq\]=0](#) // not a read request
 - [D18F3xBC_x8\[EccVector\]=0001h](#) // set bitmask to inject error into only one symbol
- Program error trigger:
 - [D18F3xBC_x8\[DramErrEn\]=0](#) // inject only a single error
 - [D18F3xBC_x8\[EccWrReq\]=1](#) // a write request; enable injection on next write
- Clean up // if programmed for continuous errors
 - [D18F3xBC_x8\[DramErrEn\]=0](#) // inject only a single error

2.15 Fusion Controller Hub

The processor contains an integrated Fusion Controller Hub (FCH). The FCH supports the following interfaces:

- Universal Serial Bus (USB) versions 1.1, 2.0, and 3.0
- Serial ATA revision 3.0
- Secure Digital (SD)
- System Management Bus (SMBus)
- Low Pin Count (LPC) bus and SPI interface
- High Definition (HD) audio
- Serial IRQ
- Serial Peripheral Interface (SPI) ROM
- Advanced Configuration and Power Interface (ACPI)

The FCH also comprises the following functions:

- Real-Time Clock (RTC)
- Programmable Interrupt Controller (PIC)
- System clock generation
- System Management Interrupt (SMI)
- General-Purpose I/O (GPIO)
- Power management
- Watchdog Timer (WDT)

2.15.1 MMIO Programming for Legacy Devices

The legacy devices LPC, IOAPIC, ACPI, TPM and Watchdog Timer require the base address of the Memory Mapped IO registers to be assigned before these logic blocks are accessed. The Memory Mapped IO register base address and its entire range should be mapped to non-posted memory region by programming the CPU register. See BIOS Developer's Guide for details.

2.15.2 USB Controllers

The processor supports ten USB ports using the BP_USB_HSD[9:0]P/N pins. Ports 0 through 7 are compatible with USB 2.0 (EHCI) and USB 1.1 (OHCI). Ports 8 and 9 are connected to an EHCI/OHCI controller pair or to an xHCI controller, as specified by [PMxEF\[PortRoutingSelect\]](#). The xHCI controller operates at USB1.1, USB 2.0, or USB 3.0 speeds. Support for USB 3.0 varies by product; see [PMxD9_x03\[XhcDis\]](#).

When ports 8 and 9 are connected to the xHCI controller, these ports are accessed using either the BP_USB_HSD[9,8]P/N pins (USB 1.1 and USB2.0) or the BP_USB_SS[1,0][RX,TX]P/N pins (USB 3.0). When ports 8 and 9 are connected to an EHCI/OHCI controller pair, only the BP_USB_HSD[9,8]P/N pins are used.

Table 78: USB Port Mapping

Ports	PMxEF[Por-tRoutingSelect]	USB Version	Controller	Registers	Pins
3-0	X	1.1	OHCI 1	D12F0xXX, OHCI1xXX	BP_USB_HSD[3:0]P/N
		2.0	EHCI 1	D12F2xXX, EHCI1xXX	

Table 78: USB Port Mapping

Ports	PMxEF[PortRoutingSelect]	USB Version	Controller	Registers	Pins
7-4	X	1.1	OHCI 2	D13F0xXX, OHCI2xXX	BP_USB_HSD[7:4]P/N
		2.0	EHCI 2	D13F2xXX, EHCI2xXX	
9-8	0	1.1	OHCI 3	D16F0xXX, OHCI3xXX	BP_USB_HSD[9,8]P/N
		2.0	EHCI 3	D16F2xXX, EHCI3xXX	
	1	1.1	xHCI	D10F0xXX, XHCI* (See 3.26.4.3.2)	BP_USB_HSD[9,8]P/N
		2.0			BP_USB_SS[1,0][RX,TX]P/N
		3.0			

Refer to the following for the USB controller register definitions:

- Section 3.26.4.1 [USB 1.1 (OHCI)] for the OHCI controllers

2.15.2.1 USB Power Management

USB power management functions are controlled by registers outside the USB controller registers spaces.

See the following register definitions in 3.26.13 [Power Management (PM) Registers]:

- PMx80[UsbPeriodicalSetBmSts, Usb20SetBmSts, Usb11SetBmSts, Usb11BmStsEn]
- PMxED [USB Gating]
- PMxEF [USB Enable]
- PMxF0 [USB Control]

2.15.2.2 USB Interrupts

The interrupt mapping is specified by IOC00 [Pci_Intr_Index] and IOC01 [Pci_Intr_Data]. By default, USB interrupts are routed to PCI INTA#, B#, and C#.

For normal operations, MSI must be disabled in all OHCI and EHCI controllers.

2.15.2.3 BIOS Programming Requirements For USB Reset During S3 Resume

Set PMxF0[UsbKbResetEnable]=1 to enable the USB controller to get reset by any software that generates a PCIRST# condition (e.g. a keyboard reset or a write to IOCF9). To avoid losing the USB connection status during the S3 resume procedure, BIOS must ensure that PMxF0[UsbKbResetEnable]=0 before any software-generated PCIRST# reset condition during S3 resume.

2.15.2.4 Enabling the xHCI Controller

Software performs the following sequence to enable the xHCI controller:

1. Program PMxEF[Usb3OhciEnable]=0.
2. Program PMxEF[Usb3EhciEnable]=0.
3. Program PMxEF[PortRoutingSelect]=1.
4. Program XHCI_PMx00[Xhci0Enable]=1.

2.15.2.5 OHCI Arbiter Mode

Software should program the following sequence for all OHCI controllers to set OHCI arbiter mode:

1. Whenever the system resumes from S3/S4/S5, software should reset the USB controllers as follows:
 - A. Program PMxD3[AssertUsbRstB]=0.

- B. Wait for <1 ms.
- C. Program [PMxD3\[AssertUsbRstB\]](#)=1.
- 2. Program [D\[16,13,12\]F0x80\[OHCIArbiterMode\]](#)=11b.
- 3. Program [D\[16,13,12\]F0x80\[OHCIArbVldCtl\]](#)=1b.

2.15.2.6 USB2.0 Controller PHY Configuration and Calibration

Software performs the following sequence to configure EHCI common PHY for each USB port to be used shortly after chip boot up and after USB2.0 EHCI controller initiated the calibration. The register settings have to be re-established to ensure USB2.0 PHY is properly calibrated. It is not needed after waking up from S3.

1. Program HSSLEW=10b.
 - A. Program [EHC1\[3:1\]xB4\[PortNumber\]](#) with the controller port number according to [Table 79](#).
 - B. Program [EHC1\[3:1\]xB4\[VControlModeSel\]](#)=0110b.
 - C. Program HSSLEW value at [EHC1\[3:1\]xB4\[1:0\]](#)=10b.
 - D. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=1.
 - E. Wait for [EHC1\[3:1\]xB4\[VBusy\]](#)=0.
 - F. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=0.
 - G. Wait for [EHC1\[3:1\]xB4\[VBusy\]](#)=0.
 - H. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=1 to lock the PHY control interface.
2. Program [EHC1\[3:1\]xD0\[BgAdj\]](#)=6.
3. Program [EHC1\[3:1\]xC4\[IRefAdj\]](#)=2.
4. Program [EHC1\[3:1\]xC4\[XRefAdj\]](#)=2.
5. Program [EHC1\[3:1\]xC4\[PVI\]](#)=1.
6. Program [EHC1\[3:1\]xC4\[CPAAdj\]](#)=1.
7. Program [EHC1\[3:1\]xC4\[DLLControl\]](#)=90h.
8. Program [EHC1\[3:1\]xD4\[PlIIFilter\]](#)=1.
9. Program [EHC1\[3:1\]xD4\[CalEnable\]](#)=0.
10. Wait for 200 ns.
11. Program [EHC1\[3:1\]xD4\[CalEnable\]](#)=1.
12. Wait for 400 ns.
13. Program [EHC1\[3:1\]xD4\[CalEnable\]](#)=0.

2.15.2.7 USB2.0 Controller ISO Device CRC False Error Detection

Software performs the following sequence to program CDR phase shift limit for each USB port to be used:

1. Program [EHC1\[3:1\]xB4\[PortNumber\]](#) with the controller port number according to [Table 79](#).
2. Program [EHC1\[3:1\]xB4\[VControlModeSel\]](#)=0111b.
3. Program [EHC1\[3:1\]xB4\[2:0\]](#)=101b.
4. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=1.
5. Wait for [EHC1\[3:1\]xB4\[VBusy\]](#)=0.
6. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=0.
7. Wait for [EHC1\[3:1\]xB4\[VBusy\]](#)=0.
8. Program [EHC1\[3:1\]xB4\[VLoadB\]](#)=1 to lock the PHY control interface.

Table 79: USB Port to [EHC1\[3:1\]xB4\[PortNumber\]](#) Mapping

USB Port	Software selects by programming
0	EHC11xB4[PortNumber] =0h
1	EHC11xB4[PortNumber] =1h
2	EHC11xB4[PortNumber] =2h

Table 79: USB Port to [EHC1\[3:1\]xB4\[PortNumber\]](#) Mapping

3	EHC11xB4[PortNumber]=3h
4	EHC12xB4[PortNumber]=0h
5	EHC12xB4[PortNumber]=1h
6	EHC12xB4[PortNumber]=2h
7	EHC12xB4[PortNumber]=3h
8	EHC13xB4[PortNumber]=0h
9	EHC13xB4[PortNumber]=1h

2.15.2.8 xHC USB2.0 Common PHY Calibration

The following programming sequence has to be carried out shortly after chip boot up and after USB2.0 EHCI/XHCI controller initiated the calibration. The register settings have to be re-established to ensure USB2.0 PHY is properly calibrated. It is not needed after waking up from S3.

1. Program HSSLEW=10b.
 - A. Program [D10F0x4C_x4000_0000](#)[PortNumber] with the controller port number according to [Table 80](#).
 - B. Program [D10F0x4C_x4000_0000](#)[VControlModeSel]=0110b.
 - C. Program HSSLEW value at [D10F0x4C_x4000_0000](#)[1:0]=10b.
 - D. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1.
 - E. Wait for [D10F0x4C_x4000_0000](#)[VBusy]=0.
 - F. Program [D10F0x4C_x4000_0000](#)[VLoadB]=0.
 - G. Wait for [D10F0x4C_x4000_0000](#)[VBusy]=0.
 - H. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1 to lock the PHY control interface.
2. Program [D10F0x4C_x4000_0050](#)[BgAdj]=6.
3. Program [D10F0x4C_x4000_000C](#)[IRefAdj]=2.
4. Program [D10F0x4C_x4000_000C](#)[XRefAdj]=2.
5. Program [D10F0x4C_x4000_000C](#)[PVI]=1.
6. Program [D10F0x4C_x4000_000C](#)[CPAdj]=1.
7. Program [D10F0x4C_x4000_000C](#)[DIIControl]=90h.
8. Program [D10F0x4C_x4000_0054](#)[PllFilter]=1.
9. Program [D10F0x4C_x4000_0054](#)[CalEnable]=0.
10. Wait for 200 ns.
11. Program [D10F0x4C_x4000_0054](#)[CalEnable]=1.
12. Wait for 400 ns.
13. Program [D10F0x4C_x4000_0054](#)[CalEnable]=0.

2.15.2.9 USB3.0 PHY Auto-Calibration Enablement

BIOS enables USB3.0 PHY auto-calibration as follows:

1. Program [XHCI_PMx8C](#)[PlIVcoTune[3:0]]=0011b.
2. Program [XHCI_PMx8C](#)[CrPllCalibEn]=1.

2.15.2.10 xHCI ISO Device CRC False Error Detection

Software performs the following sequence to program CDR phase shift limit for each USB port to be used:

1. Program [D10F0x4C_x4000_0000](#)[PortNumber] with the controller port number according to [Table 80](#).
2. Program [D10F0x4C_x4000_0000](#)[VControlModeSel]=0111b.
3. Program [D10F0x4C_x4000_0000](#)[2:0]=101b.

4. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1.
5. Wait for [D10F0x4C_x4000_0000](#)[VBusy]=0.
6. Program [D10F0x4C_x4000_0000](#)[VLoadB]=0.
7. Wait for [D10F0x4C_x4000_0000](#)[VBusy]=0.
8. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1 to lock the PHY control interface.

Table 80: USB Port to [D10F0x4C_x4000_0000](#)[PortNumber] Mapping

USB Port	Software selects by programming
8	D10F0x4C_x4000_0000 [PortNumber]=0h
9	D10F0x4C_x4000_0000 [PortNumber]=1h

2.15.2.11 xHCI PHY Clock Gating

The following programming sequence configures the clock gating in the xHCI PHY. They must be performed for each port after enabling xHCI controller and need to be restored after all power state resumes.

1. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1.
2. Program [D10F0x4C_x4000_0000](#)[PortNumber] with the controller port number according to [Table 80](#).
3. Program [D10F0x4C_x4000_0000](#)[VControlModeSel]=0011b.
4. Program [D10F0x4C_x4000_0000](#)[2]=1.
5. Read [D10F0x4C_x4000_0000](#)[VBusy] to ensure it is 0.
6. Program [D10F0x4C_x4000_0000](#)[VLoadB]=0.
7. Wait for [D10F0x4C_x4000_0000](#)[VBusy]=0.
8. Program [D10F0x4C_x4000_0000](#)[VLoadB]=1 to lock the PHY control interface.

2.15.2.12 xHCI Firmware Preload

Software performs the following programming sequence for firmware preload. Firmware preload should be executed before BIOS de-asserts [XHCI_PMx00](#)[U3CoreReset].

1. Enable firmware preload by programming [XHCI_PMx00](#)[FwLoadMode]=1.
2. Program [XHCI_PMx04](#)[XhciFwPreloadType] with 1 for boot RAM preload and 0 for instruction RAM preload.
3. Program [XHCI_PMx04](#)[XhciFwRomAddr] with the offset of the application firmware in the external ROM.
4. Program [XHCI_PMx08](#)[XhciFwRamAddr]=0.
5. Program [XHCI_PMx08](#)[XhciFwSize]=8000h.
6. Program [XHCI_PMx00](#)[FwPreloadStart]=1 to start firmware preload.
7. Wait for [XHCI_PMx00](#)[FwPreloadComplete]=1.
8. Program [XHCI_PMx00](#)[FwPreloadStart]=0.
9. Program [XHCI_PMx00](#)[U3CoreReset]=0 to de-assert xHC reset.

2.15.2.13 xHCI Clear Pending PME on Sx State Entry

During S3/S4 entry with wake from Sx state enabled, if the xHCI controller received a wake event before the system shutdown into Sx state is completed, [D10F0x54](#)[PmeStatus] may remain set when the system enters into Sx state. This will prevent subsequent wake events from being propagated to the ACPI controller. BIOS should write 1 to clear [D10F0x54](#)[PmeStatus] if [D10F0x54](#)[PmeStatus] is 1 and ACPI GEvent status bit is clear on entry into S3/S4 state.

2.15.2.14 xHCI Enable OHCI3/EHCI3 on S4/S5 State Entry

If xHCI controller is enabled, OHCI3/EHCI3 controllers are disabled for normal operations. See [2.15.2.4 \[Enabling the xHCI Controller\]](#). On S4/S5 entry, OHCI3/EHCI3 controllers should be enabled to avoid possibly stalled IRQ1/IRQ12 interrupts, which could cause keyboard/mouse hang during wake up.

- Program [PMxEF\[Usb3OhciEnable\]](#)=1.
- Program [PMxEF\[Usb3EhciEnable\]](#)=1.

2.15.3 SATA

2.15.3.1 SATA Operating Mode

The SATA host controller can operate in the following modes:

- IDE mode.
- AHCI mode.

Software programs the subclass code and programming interface register to enable the SATA controller as RAID controller, IDE controller, or AHCI controller.

1. Program [D11F0x40\[SubclassCodeWriteEnable\]](#)=1.
2. Program [D11F0x08\[SubclassCode\]](#) and [D11F0x08\[ProgramIF\[7:0\]\]](#) according to [Table 230 \[SATA Controller Subclass Code and ProgramIF Settings\]](#).
3. Program [D11F0x40\[SubclassCodeWriteEnable\]](#)=0.

2.15.3.2 SATA Drive Detection in IDE mode

The following sequence should be included in the SBIOS drive identification loop for SATA drive detection in IDE mode.

1. If any of the SATA port status register at [SATAx1\[A,2\]8\[DET\]==03h](#), program [IDE\[1:0\]x06\[Drive-Head\]=A0h](#) for the corresponding port and go to Step 2.
Else, no SATA drives are attached; exit the detection loop program.
2. If ([IDE\[1:0\]x06\[DriveHead\]==A0h](#)) && ([IDE\[1:0\]x07\[7\]==0](#)) && ([IDE\[1:0\]x07\[3\]==0](#)) for a port, the SATA device on that port is ready.
Else, loop until 30 s time-out; There is no SATA device attached if a time-out occurs.
Note: Most drives don't need 30 s time-out. The 30 s time-out is only needed for some particularly large capacity SATA drives, which require a longer spin-up time during a cold boot.

2.15.3.3 SATA PHY Auto-Calibration Enablement

BIOS enables SATA PHY auto-calibration as follows:

1. Program [D11F0x88\[PlIVcoTune\]](#)=0011b.
2. Program [PMxDC\[PllCalibEn\]](#)=1.
3. Reset PHY:
 - A. Program [D11F0x84\[RSTB\]](#)=0 to assert reset.
 - B. Wait for 100 us.
 - C. Program [D11F0x84\[RSTB\]](#)=1 to release PHY reset.

2.15.3.4 SATA PHY Fine Tuning

The SBIOS should program the SATA controller in the sequence indicated below to fine tune the PHY. Performing this procedure provides sufficient time for the SATA controllers to correctly complete SATA drive

detection. The same procedure is required after the system resumes from the S3 state.

- Gen 3 settings:
 - Program D11F0x80[15:0]=0130h to select Gen 3 for all ports.
 - Program D11F0x98[31:0]=0040f407h.
 - Gen 2 settings:
 - Program D11F0x80[15:0]=0120h to select Gen 2 for all ports.
 - Program D11F0x98[31:0]=00403204h to fine tune PHY for Gen 2.
 - Gen 1 settings:
 - Program D11F0x80[15:0]=0110h to select Gen 1 for all ports.
 - Program D11F0x98[31:0]=00403103h to fine tune PHY for Gen 1.
 - Squelch detector settings:
 - A. Program PMxC8[EPromEFuseSelect]=1b to select Efuse access.
 - B. Program PMxD8[EepromEfuseIndex]=01h.
 - C. Read from PMxD9[4] to get the setting of APU_FCH_FUSE[12].
 - D. IF (PMxD9[4]==0) THEN

SATA RX squelch detection threshold is not fused, program the squelch detector threshold for all ports at all generation speed as follows:

 - Program D11F0x80[15:0]=0130h.
 - Program D11F0x9C[RX_SQDET_TH]=101b.
 - Program D11F0x80[15:0]=0120h.
 - Program D11F0x9C[RX_SQDET_TH]=101b.
 - Program D11F0x80[15:0]=0110h.
 - Program D11F0x9C[RX_SQDET_TH]=101b.

ELSE

 - a. Program PMxD8[EepromEfuseIndex]=02h.
 - b. Read from PMxD9[2:0] to get the fused setting for SATA port 1 squelch detector threshold.
 - c. Program the squelch detector threshold control register for port 1 at all generation speed:
 - Program D11F0x80[15:0]=0031h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[2:0].
 - Program D11F0x80[15:0]=0021h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[2:0].
 - Program D11F0x80[15:0]=0011h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[2:0].
 - d. Program PMxD8[EepromEfuseIndex]=01h.
 - e. Read from PMxD9[7:5] to get the fused setting for SATA port 0 squelch detector threshold.
 - f. Program the squelch detector threshold control register for port 0 at all generation speed:
 - Program D11F0x80[15:0]=0030h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[7:5].
 - Program D11F0x80[15:0]=0020h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[7:5].
 - Program D11F0x80[15:0]=0010h.
 - Program D11F0x9C[RX_SQDET_TH]=PMxD9[7:5].
- ENDIF.

2.15.3.5 SATA PHY Reference Clock Selection

SATA PHY reference clock can originate from either internal or external clock. The following steps select SATA PHY reference clock source:

1. Select one of the following options for reference clock.

- Internal 48 MHz differential non-spread clock from pad (default):
 - a. Program **PMxDA**[RefClkSel]=1 to select reference clock from internal RDL.
 - b. Program **PMxDA**[RefDivSel]=0 to set PHY divider to div-by-1.
 - c. Program **D11F0x8C**[PLL_CLKF]=7Dh to set PLL feedback clock divider value to 6 GHz/48 MHz=7Dh.
 - External 25 MHz crystal non-spread clock from external clock chip (the clock path has to be routed on the board, in order for the setting to take effect):
 - a. Program **PMxDA**[RefClkSel]=0 to select reference clock from an external source, via the PAD_XTALI and PAD_XTALO, to SATA PHY.
 - b. Program **PMxDA**[RefDivSel]=0 to set PHY divider to div-by-1.
 - c. Program **D11F0x8C**[PLL_CLKF]=F0h to set PLL feedback clock divider value to 6 GHz/25 MHz=F0h.
2. Reset PHY:
- A. Program **D11F0x84**[RSTB]=0 to assert reset.
 - B. Wait for 100 us.
 - C. Program **D11F0x84**[RSTB]=1 to release PHY reset.

2.15.3.6 SATA Power Management

2.15.3.6.1 SATA PHY Power Saving

The SATA PHY has different power saving states with the Active state consuming the most power. The table below summarizes the different controls during each power saving state.

2.15.3.7 Enable Shadow Register Reload

When default PHY settings are not optimal, they need to be adjusted by software. Once these settings are re-programmed, software shall program **D11F0x84**[S5ShadowLdDis] to 0 to turn on shadow register reloading. When default PHY settings are optimal and need no adjustment, **D11F0x84**[S5ShadowLdDis] needs not to be altered and shadow register preloading is effectively disabled.

2.15.3.8 SATA Interrupt Handling

2.15.3.8.1 Line Interrupt

The SATA interrupt mapping is specified by **IOC00** [**Pci_Intr_Index**] and **IOC01** [**Pci_Intr_Data**].

2.15.3.8.2 MSI Message

SATA controller supports message-based interrupts. When MSI is enabled and the SATA controller owns N ports, as specified by **SATAx0C** [**Ports Implemented (PI)**], **D11F0x50**[MMC] should be programmed according to platform configurations:

- If **SATAx00**[CCCS]==1, **D11F0x50**[MMC] should be the minimum of 2M which satisfies $2M \geq (N+1)$. For example: if BIOS knows that system has 2 SATA ports in AHCI mode (N=2). If **SATAx00**[CCCS]==1, BIOS should program **D11F0x50**[MMC]=2 to request 4 MSI interrupts. If **SATAx00**[CCCS]==0, BIOS should program **D11F0x50**[MMC]=1 to request 2 MSI interrupts.

MSI capability pointer should be hidden when SATA subclass is configured in IDE mode (see [2.15.3.1 \[SATA Operating Mode\]](#)). To hide SATA MSI capability, the capability pointer offset needs to be re-programmed from its default setting to prevent the driver from enabling this feature.

2.15.3.9 Clear status of SATA PERR

BIOS should clear SATA PERR status soon after a cold boot, warm boot, any S3/S1 resume events, or an [IOCF9](#) initiated reset outside a warm boot before any SATA activity is initiated.

- Write 1 to clear [SMIx3C](#)[SataPerr].
- Write 1 to clear [SMIx84](#)[RasEvent55].

2.15.4 LPC Bus Interface

BIOS should program [D14F3xA0](#)[SpiBaseAddr] with non-zero address to enable the MMIO access to SPI ROM control registers.

2.15.4.1 Enabling LPC DMA function

If DMA is required for the LPC interface, program the registers as the following:

- Program [D14F3x40](#)[LegacyDmaEnable]=1.
- Program [D14F3x78](#)[NoHog]=1.
- Program [PMx08](#)[ArbDmaDis]=1.
- Program [D14F3x78](#)[LDRQ1]=1 and [D14F3x78](#)[LDRQ0]=1.
- Program [PMx04](#)[LegacyDmaPrefetchEnhance]=1 for non-DOS mode. Note: This bit should only be enabled in the ACPI method (called by the OS). This ensures that it is enabled only when the system is in Windows® mode. Under DOS mode, this feature may not work properly and may cause the floppy to malfunction.

2.15.4.2 Enabling SPI 100

To enable the support for SPI 100 MHz speed, software needs to program [SPIx20](#)[UseSpi100]=1. SPI 100 should be enabled on after the Auto ROM sizing has been completed (Auto ROM sizing is done by the software only during the initial boot when the system power state transitions from G3->S5->S0). The actual read speed also depends on the settings at [SPIx22](#) [SPI100 Speed Config].

2.15.5 SD Controller

The SD controller is SD 3.0 compliant host controller.

2.15.6 HD Audio

The FCH has one High Definition Audio controller (HD audio aka. Azalia), which can be enabled/disabled by programming [PMxE8](#)[AzEnable].

The HD audio controller supports up to 4 codecs with one AZ_SDIN pin from each codec. The four AZ_SDIN pins are multiplexed with GPIO167-170 (GPIOxA7-GPIOxAA). If a particular pin is to be used for HD audio functionality and the integrated pull-down is to be used rather than external pull-down resistor, in addition to being configured for HD audio, the following bits need to be set:

- GPIOxA7=3Eh
- GPIOxA8=3Eh
- GPIOxA9=3Eh
- GPIOxAA=3Eh

For example, if only GPIO167 and GPIO168 are to be used for HD audio, then only GPIOxA7 and GPIOxA8 need to be programmed to 3Eh. See [3.26.12](#) [GPIO Pin control registers].

2.15.6.1 HD Audio AF and MSI Capability

The Advanced Feature (AF) capability and MSI capability in HD audio controller are controlled by [D14F2x44\[EnAFCap\]](#) and [D14F2x44\[EnMsiCap\]](#) respectively. The settings of these two bits affect how the AF capability and MSI capability are linked to the capability pointer linked list.

Table 81: HD Audio AF and MSI Capability Settings

D14F2x44 [EnAF-Cap]	D14F2x44 [EnMsi-Cap]	D14F2x50 [NextPtr]	D14F2x60 [CapID]	D14F2x60 [NextPtr]	D14F2x70 [AFC-apID]	D14F2x70 [NextPtr]	D14F2x70 [AFLengt h]	D14F2x70 [25:24]
0	0	0h	0h	0h	0h	0h	0h	0h
0	1	60h	5h	0h	0h	0h	0h	0h
1	0	70h	0h	0h	13h	0h	6h	3h
1	1	60h	5h	70h	13h	0h	6h	3h

2.15.7 ASF Controller

The ASF controller can be used in a slave mode to support DASH clients. When the platform is configured for DASH the BIOS should at the minimum set the following registers to ensure the ASF is configured in slave mode and the control commands are defined properly in the ASF tables.

- When operating in Master mode, BIOS should program [PMx28\[AsfSmMasterEn\]](#)=1. BIOS should program [PMx28\[AsfSmMasterEn\]](#) back to 0 after the master operations are done.
- When operating in Slave mode, BIOS should program [PMx28\[AsfSmMasterEn\]](#)=0.

In addition to support remote DASH operations, BIOS should ensure that the ASF tables define the correct command codes and [ASFx0E \[RemoteCtrlAdr\]](#) has to be programmed with the same value reported in the ASF control data table.

ASF controller can behave like remote control device to accept the command from client side to do the reset/power down/power up/power cycle. BIOS reports those in ASF control data table. The command and command data are defined in [Table 82](#).

Table 82: ASF Remote Control Commands

Remote Control	Control Command	Control data
Reset	50h	00h
Power Up	51h	00h
Power Down	52h	00h
Power Cycle	53h	00h

2.15.8 Integrated Micro-Controller

The FCH supports an integrated micro-controller (IMC) to run the keyboard BIOS and/or other algorithms. The IMC is an enhanced 8051 with a RISC-like architecture which allows it to perform most instructions in 1-4 clocks (instead of 12 clocks in the original 8051).

The IMC can also be enabled by programming [PMxD6\[ImcEnable\]](#).

2.15.9 On-Chip Clock Generator

There are two clocking modes in which this chip can be brought up based on the boot strap pin LPCCLK1. SBIOS should read [MISCx80\[ClkGenStrap\]](#) to determine clock generator mode. SBIOS should program

[MISCx40](#)[OscClkSwitchEn] to 1 to select average 14 MHz OSC clock provided by internal PLL in both internal and external clocking mode.

2.15.9.1 Power Saving In Internal Clock Mode

GPP_CLK_P/N pins are powered off when this chip is strapped to use an external clock, and powered on when strapped to operate in internal clock mode. The GPP_CLK clocks are mapped to corresponding CLK_REQ# pins. The GPP_CLK0/1/2/3 mapping is defined at [MISCx00](#)[15:0]. SLT_GFX_CLK mapping is defined at [MISCx04](#)[7:4]. In internal clock mode, a selected GPP_CLK can be powered off when the corresponding CLK_REQ# is asserted. See [MISCx00](#) && [MISCx04](#) for details.

Software can also program [MISCx04](#)[PCIE_RCLK_PowerDownEnable]=1 to turn off 100 MHz reference clock input buffer in internal clock generator mode for power saving.

2.15.9.2 Global A-Link / B-Link Clock Gating

Software needs to program [MISCx2C](#)[AlinkClkGateOffEn]=1 and [PMx04](#)[ABLinkClkGateEn]=1 to enable global A-link clock gate off function.

Software needs to program [MISCx2C](#)[BlinkClkGateOffEn]=1 and [PMx04](#)[ABLinkClkGateEn]=1 to enable global B-link clock gate off function.

[PMx04](#)[ABLinkClkGateEn] is a non-sticky bit and needs to be programmed to 1 after PCI reset and S3/S4/S5 state, if global A-link / B-link gating function has been enabled. [MISCx2C](#)[AlinkClkGateOffEn] and [MISCx2C](#)[BlinkClkGateOffEn] are sticky bits.

2.15.9.3 CG_PLL CMOS Clock Driver Setting for Power Saving

Software programs the following registers to select CMOS clock driver for CG1_PLL in internal & external clock mode for power saving:

- Program [MISCx1C](#)[CgpllClkDriverUpdate]=0.
- Program [MISCx1C](#)[Cg1ClkDriverType]=1011b and Program [MISCx1C](#)[Cg1RefClk48MHzDriverType]=0010b.
- Perform a software reset through [IOCF9](#).

These settings will only need to be applied once when the chip is booting up from G3-S5->S0. These is no need to do this for every reset since the setting is sticky.

2.15.10 Scallion Gasket

The Scallion gasket (SBG) is responsible for converting between the protocols used by the Scallion interface and the A-link bridge interface. BIOS should program [PMxE0](#) to set up base address before accessing AB configuration registers.

2.15.11 A-Link Bridge

The A-link bridge (AB) sits behind the Scallion gasket and acts as the bridge between Scallion and A-link/B-link bus.

2.15.11.1 Detection of Upstream Interrupts

BIOS should enable AB to detect upstream interrupts for the purpose of system management.

- Program [ABx04_x94](#)[MsiAddr[39:20]] with CPU interrupt delivery address [39:20].
- Program [ABx04_x94](#)[MsiAddrEn]=1.

2.15.11.2 AB Memory Power Saving

The following sequence enables AB memory power saving:

- A. Program [MISCx68\[ABBypassMemDsd\]](#)=0 to enable AB memory DSD.
- B. Program [ABx04_x58\[BIMemSDEn\]](#)=1 to enable B-link memory shutdown.
- C. Program [ABx04_x58\[AlMemSDEn\]](#)=1 to enable A-link memory shutdown.

2.15.11.3 AB Internal Clock Gating

The following sequence enables AB internal clock gating:

- A. Program [ABx04_x54\[BIClkGateDelay\]](#)=10h to set the number of cycles to delay before gating B-link clocks.
- B. Program [ABx04_x10054\[AlClkGateDelay\]](#)=10h to set the number of cycles to delay before gating A-link clocks.
- C. Program [ABx04_x54\[BIClkGateEn\]](#)=1 to enable medium grain B-link clock gating.
- D. Program [ABx04_x54\[DbgClkGateEn\]](#)=1 to disable debug only B-link clocks.
- E. Program [ABx04_x10054\[AlClkGateEn\]](#)=1 to enable medium grain A-link clock gating.
- F. Program [ABx04_x10054\[DbgClkGateEn\]](#)=1 to disable debug only A-link clocks.

2.15.11.4 AB 32/64 Byte DMA Write Enable

To enable AB 32 byte/64 byte DMA write, software needs to program [ABx04_x54\[UpWr16BMode\]](#)=0 and [ABx04_x54\[UpSWrByteCntSbgMode\]](#)=1 to disable 16 byte write splitting and enable SBG mode byte-count calculation logic. Software should also make sure [ABx04_x204\[Dma16ByteMode\]](#)=0.

3 Registers

This section provides detailed field definitions for the core register sets in the processor.

3.1 Register Descriptions and Mnemonics

Each register in this document is referenced with a mnemonic. Each mnemonic is a concatenation of the register-space indicator and the offset of the register. Here are the mnemonics for the various register spaces:

- **IOXXX**: x86-defined input and output address space registers; XXX specifies the hexadecimal byte address of the IO instruction. This space includes IO-space configuration access registers, [IOCF8 \[IO-Space Configuration Address\]](#) and [IOFCF \[IO-Space Configuration Data Port\]](#), the GPU VGA registers, and the legacy block configuration registers. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.2 \[IO Space Registers\]](#) and [3.26.1 \[Legacy Block Configuration Registers \(IO\)\]](#).
- **APICXX0**: APIC memory-mapped registers; XX0 is the hexadecimal byte address offset from the base address. See [2.4.8.1.2 \[APIC Register Space\]](#).
- **CPUID FnXXXX_XXXX_EiX[_xYYY]**: processor capabilities information returned by the CPUID instruction. See [3.18 \[CPUID Instruction Registers\]](#). Each core may only access this information for itself.
- **MSRXXXX_XXXX**: MSRs; XXXX_XXXX is the hexadecimal MSR number. This space is accessed through x86-defined RDMSR and WRMSR instructions. Unless otherwise specified there is one set of these registers [Per-core](#). See [2.4.1 \[L2 complex\]](#).
- **DXFYxZZZ**: PCI-defined configuration space; X specifies the hexadecimal device number (this may be 1 or 2 digits), Y specifies the function number, and ZZZ specifies the hexadecimal byte address (this may be 2 or 3 digits); e.g., D18F3x40 specifies the register at device 18h, function 3, and address 40h. See [2.7 \[Configuration Space\]](#), for details about configuration space.
 - Some register in D18F2xXXX have the _dct[0] mnemonic suffix. See [2.9.3 \[DCT Configuration Registers\]](#).
- **PMCxXXX**: core performance monitor events; XXX is the hexadecimal event counter number programmed into [MSRC001_00\[03:00\]\[EventSelect\]](#); See [2.6.1.1 \[Core Performance Monitor Counters\]](#).
 - When PMCxXXX is followed by [z:y] then UnitMask[z:y] is being specified.
- **L2IPMCxXXX**: L2 performance monitor events; XXX is the hexadecimal event counter number programmed into [MSRC001_023\[6,4,2,0\]\[EventSelect\]](#); See [2.6.1.2 \[L2I Performance Monitor Counters\]](#).
 - When PMCxXXX is followed by [z:y] then UnitMask[z:y] is being specified.
- **NBPMCxXXX**: NB performance monitor events; XXX is the hexadecimal event counter number programmed into [MSRC001_024\[6,4,2,0\]\[EventSelect\]](#); See [2.6.1.3 \[NB Performance Monitor Counters\]](#).
 - When NBPMCxXXX is followed by [z:y] then UnitMask[z:y] is being specified.
- **ABxXX**: ALink Bridge registers; XX specifies the hexadecimal byte address offset from the base address. The base address for this space is specified by [PMxE0 \[ABRegBar\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.2 \[AB Configuration Registers \(Scallion\)\]](#).
- **IDE[Y]xXX**: SATA controller IDE mode IO mapped registers; XX specifies the hexadecimal byte address offset from the base address; Y specifies primary drive (0) or secondary drive (1). The base address for this space is specified in [Table 231 \[IDE Compatibility Mode and Native Mode Address Mapping\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.3.2.1 \[IDE Compatibility Mode and Native Mode \(BAR0, BAR1, BAR2, BAR3\) Registers\]](#).
- **IDE_BMxXX**: SATA controller IDE mode IO mapped bus master registers; XX specifies the hexadecimal byte address offset from the base address. The base address for this space is specified by [D11F0x20 \[Bus Master Interface Register Base Address \(BAR4\)\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.3.2.2 \[IDE Bus Master \(BAR4\) Registers\]](#).

- **SATAxXXX:** SATA controller AHCI mode memory mapped registers; XXX specifies the hexadecimal byte address offset from the base address. The base address for this space is specified by [D11F0x24 \[AHCI Base Address \(BAR5\)\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.3.3 \[SATA Memory Mapped AHCI Registers\]](#).
- **SATA_EMxXX:** SATA controller AHCI mode memory mapped enclosure buffer management registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.3.3.3 \[Enclosure Buffer Management Registers\]](#).
- **OHCI[Y]xXXX:** USB OHCI controller memory mapped registers; XXX specifies the hexadecimal byte address offset from the base address; Y specifies the OHCI controller number; e.g., OHCI[1]x04 specifies OHCI controller 1 memory mapped control register offset 04. The base address for this space is specified by [D\[16,13,12\]F0x10 \[OHCI Base Address\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.4.1.2 \[OHCI Memory Mapped IO Registers\]](#).
- **EHCI[Y]xXX:** USB EHCI controller memory mapped registers; XX specifies the hexadecimal byte address offset from the base address; Y specifies the EHCI controller number; e.g., EHCI[1]x04 specifies EHCI controller 1 memory mapped control register offset 04. The base address for this space is specified by [D\[16,13,12\]F2x10 \[BAR_EHCI\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.4.2.2 \[EHCI Memory Mapped IO Registers\]](#).
- **xHCI_PMxXX:** USB xHCI controller ACPI memory mapped registers; XX specifies the hexadecimal byte address offset from the base address. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.4.3.2 \[xHCI Power Management Registers\]](#).
- **SDHCxXX:** Secure Digital host controller memory mapped registers; XX specifies the hexadecimal byte address offset from the base address. The base address for this space is specified by [{D14F7x14 \[Upper Base Address Reg 0\], D14F7x10 \[Base Address Reg 0\]}](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.6.2 \[SD Host Controller Configuration Registers \(SDHC\)\]](#).
- **ASFxXX:** ASF registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.7.2 \[ASF \(Alert Standard Format\) Registers\]](#).
- **SMBUSxXX:** SMBus registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.7.3 \[SMBus Registers\]](#).
- **IOAPICxXX:** IOAPIC registers; XX specifies the hexadecimal byte address offset from the base address. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.8 \[IOAPIC Registers\]](#).
- **SPIxXX:** SPI memory mapped registers; XX specifies the hexadecimal byte address offset from the base address. The base address is specified by [D14F3xA0 \[SPI Base_Addr\]](#). Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.9.2 \[SPI Registers\]](#).
- **HPETxXXX:** HPET registers; XXX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.10 \[High Precision Event Timer \(HPET\) Registers\]](#).
- **MISCxXX:** ACPI miscellaneous control registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.11 \[Miscellaneous \(MISC\) Registers\]](#).
- **GPIOxXX:** GPIO registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.12.1 \[GPIO Registers\]](#).

- **IOMUX_{XX}**: IOMux registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.12.2 \[IOMux Registers\]](#).
- **PM_{XX}**: power management registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.13 \[Power Management \(PM\) Registers\]](#).
- **PM2_{XX}**: power management block 2 registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.14 \[Power Management Block 2 \(PM2\) Registers\]](#).
- **SMIx_{XX}**: SMI registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.16 \[SMI Registers\]](#).
- **WDTx_{XX}**: Watchdog timer registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.17 \[Watchdog Timer \(WDT\) Registers\]](#).
- **AcDcTimer_{XX}**: AC/DC wake alarm timer registers; XX specifies the hexadecimal byte address offset. Unless otherwise specified, there is one set of these registers per node; the registers in a node are accessible to any core on that node. See [3.26.18 \[Wake Alarm Device \(AcDcTimer\) Registers\]](#).

Each mnemonic may specify the location of one or more registers that share the same base definition. A mnemonic that specifies more than one register will contain one or more ranges within braces. The ranges are specified as follows:

- Comma separated lists [A,B]: Define specific instances of a register, e.g., D0F3x[1,0]40 defines two registers D0F3x40 and D0F3x140.
- Colon separated ranges [A:B]: Defines all registers that contain the range between A and B. Examples:
 - D0F3x[50:40] defines five registers D0F3x40, D0F3x44, D0F3x48, D0F3x4C, and D0F3x50.
 - D[8:2]F0x40 defines seven registers D2F0x40, D3F0x40, D4F0x40, D5F0x40, D6F0x40, D7F0x40, and D8F0x40.
 - D0F0xE4_x013[2:0]_0000 defines three registers D0F0xE4_x0130_0000, D0F0xE4_x0131_0000, and D0F0xE4_x0132_0000.
- Colon separated ranges with a explicit step [A:BstepC]: Defines the registers from A to B, C defines the offset between registers., e.g., D0F3x[50:40:step8] defines three registers D0F3x40, D0F3x48, and D0F3x50.

The processor includes a single set of IO-space and configuration-space registers. However, APIC, CPUID, and MSR register spaces are implemented once per processor core. Access to IO-space and configuration space registers may require software-level techniques to ensure that no more than one core attempts to access a register at a time.

The following is terminology found in the register descriptions.

Table 83: Terminology in Register Descriptions

Term	Definition
BIOS	Software recommendation syntax. See 3.1.2 [Software Recommendation (BIOS, SBIOS, IBIOS)] .
SBIOS	
See	Reference to remote definition. See 3.1.3 [See Keyword (See:)] .
Alias	The alias keyword allows the definition of a soft link between two registers. <ul style="list-style-type: none"> • X is an alias of Y: X is a soft link to the register Y. • X1, X2 are an alias of Y: Both X1 and X2 are soft links to Y.

Table 83: Terminology in Register Descriptions

Term	Definition
IF	Allows conditional definition as a function of register fields. The syntax is:
THEN	• IF (conditional-expression) THEN definition ENDIF.
ELSEIF	• IF (conditional-expression) THEN definition ELSE definition ENDIF.
ELSE	• IF (conditional-expression) THEN definition ELSEIF (conditional-expression) THEN definition ELSE definition ENDIF.
ENDIF	
Access Types	
Read	Capable of being read by software.
Read-only	Capable of being read but not written by software.
Write	Capable of being written by software.
Write-only	Write-only. Capable of being written by software. Reads are undefined.
Read-write	Capable of being written by software and read by software.
Set-by-hardware	Register field is set high by hardware, set low by hardware, or updated by hardware.
Cleared-by-hardware	
Updated-by-hardware	
Updated-by-SMU	
Write-1-to-clear	Software must write a 1 to the bit in order to clear it. Writing a 0 to these bits has no affect.
Write-1-only	Software can set the bit high by writing a 1 to it. Writes of 0 have no effect.
Reset-applied	Takes effect on warm reset.
GP-read	GP exception occurs on read.
GP-write	GP exception occurs on write.
GP-read-write	GP exception occurs on a read or a write.
Per-core	One instance per core. Only valid for MMIO config space. Writes of these bits from one core only affect that core's register. Reads return the values appropriate to that core.
Per-compute-unit	One instance per compute unit. Writes of these bits from one core only affect that compute unit's register. Reads return the values appropriate to that compute unit. See 2.4.2.1 [Registers Shared by Cores in a L2 complex] .
Per-L2	One instance per L2 cache. See CPUID Fn8000_001D_EAX_x2[NumSharingCache] .
Per-node	One instance per node. Only valid for MSR space. See 3.1.1 [Northbridge MSRs In Multi-Core Products] .
Not-same-for-all	Provide indication as to whether all instances of a given register should be the same across all cores/nodes according to the following equation:
Same-for-all	SameOnAllCheckEnabled = (Writable && (same-for-all MSR) && ~(not-same-for-all UpdatedByHw)). UpdatedByHw = (Updated-by-hardware set-by-hardware cleared-by-hardware set-when-done cleared-when-done). MSR's should not be marked with Same-for-all because it is the default setting.
Field Definitions	

Table 83: Terminology in Register Descriptions

Term	Definition
Reserved	Field is reserved for future use. Software is required to preserve the state read from these bits when writing to the register. Software may not depend on the state of reserved fields nor on the ability of such fields to return the state previously written. Reset must be specified if the reset value is not 0. Reset may be omitted if the reset value is 0. Read-write, if it exists, must be in internal-only text. Read-only is implied if Read-write is not specified.
Unused	Field is reserved for future use. Software is not required to preserve the state read from these bits when writing to the register. Software may not depend on the state of unused fields nor on the ability of such fields to return the state previously written.
MBZ	Must be zero. If software attempts to set an MBZ bit to 1, a general-protection exception (#GP) occurs.
RAZ	Read as zero. Writes are ignored, unless RAZ is combined with write-only or write-1-only. Reset may be omitted.
Reset Definitions	
Reset	The reset value of each register is provided below the mnemonic or in the field description. Unless otherwise noted, the register state matches the reset value when RESET_L is asserted (either a cold or a warm reset). Reset values may include: <ul style="list-style-type: none"> • X: an X in the reset value indicates that the field resets (warm or cold) to an unspecified state.
Cold reset	The field state is not affected by a warm reset (even if the field is labeled “cold reset: X”); it is placed into the reset state when PWROK is deasserted. See “Reset” above for the definition of characters that may be found in the cold reset value.
Value	The current value of a read-only field or register. A value statement explicitly defines the field or register as read-only and the value returned under all conditions including after reset events. A field labeled “Value:” will not have a separate reset definition.

3.1.1 Northbridge MSRs In Multi-Core Products

MSRs that control Northbridge functions are shared between all cores on the node in a multi-core processor (e.g. [MSRC001_001F](#)). If control of Northbridge functions is shared between software on all cores, software must ensure that only one core at a time is allowed to access the shared MSR. Some MSR’s are conditionally shared; see [D18F3x44](#)[NbMcaToMstCpuEn].

3.1.2 Software Recommendation (BIOS, SBIOS, IBIOS)

The following keywords specify the recommended value to be set by software.

- BIOS: AMD BIOS.
- SBIOS: Platform BIOS.

Syntax: BIOS: integer-expression. Any of the supported tags can be substituted for BIOS.

If “BIOS:” occurs in a register field then the recommended value is applied to the field. If “BIOS:” occurs after a register name but outside of a register field table row then the recommended value is applied to the width of the register.

3.1.3 See Keyword (See:)

There is a special meaning applied to the use of “See:” that differs from the use of See not followed by a “:”.

- See, not followed by a “:”, simply refers the reader to a document location that contains related information.
- See followed by a “:” is a shorthand notation that indicates that the definition for this register or register field inherits all properties and definitions from the register or register field that follows "See:". Any definition local to the register or register field supercedes this inheritance.

“See:” can be used in the following ways:

- Full register width. [CPUID Fn0000_0001_EAX](#) inherits it’s full register width definition from [D18F3xFC](#).
- Register field. [MSR0000_0277\[PA1MemType\]](#) inherits it’s definition from PA0MemType, however, the local reset of 4h overrides the inherited PA0MemType reset of 6h.
- Valid values definition. [MSR0000_020\[E,C,A,8,6,4,2,0\]\[MemType\]](#), for example, inherits the valid values definition from [Table 191 \[Valid Values for Memory Type Definition\]](#).

3.1.4 Mapping Tables

The following mapping table types are defined.

3.1.4.1 Register Mapping

The register mapping table specifies the specific function for each register in a range of registers.

[Table 176](#), for example, specifies that the D18F5x160 function is for NB P-state 0.

3.1.4.2 Index Mapping

The index mapping table is similar to the register mapping table, but specifies the register by index instead of by full register mnemonic.

[Table 135 \[Index Mapping for D18F2x9C_x0D0F_0\[F,8:0\]02_dct\[0\]\]](#), for example, specifies that the D18F2x98_dct[0][31:0]==0D0F_0002h, or D18F2x9C_x0D0F_0002_dct[0], function is for Byte 0.

3.1.4.3 Field Mapping

The field mapping table maps the fields of a range of registers. The rows are the registers that are mapped. Each column specifies a field bit range that is mapped by that column for all registers. The cell at the intersection of the register and the field bit range specifies the suffix that is appended to the register field. “Reserved” specifies that the field is reserved for the register of that row. “-” indicates no specification and the table cell should be skipped.

3.1.4.4 Broadcast Mapping

The broadcast mapping table maps a register address to a range of register addresses that are read or written as a group when the broadcast register address is read or written. The register address is formed by the concatenation of the row address with the column address. The cell at the intersection of the row and column address is a range of register addresses that will be read or written as a group when the row and column address is read or written.

3.1.4.5 Reset Mapping

The reset mapping table specifies the reset, cold reset, or value for each register in a range of registers.

Table 186 [Reset Mapping for CPUID Fn8000_0000_E[D,C,B]X], for example, specifies that the CPUID Fn0000_0000_EBX register has a value of 6874_7541h, with a comment of “The ASCII characters “h t u A””.

3.1.4.6 Valid Values

The valid values table defines the valid values for one or more register fields. The valid values table is equivalent in function to the Bits/Description tables in register fields (E.g. [MSR0000_0277\[PA0MemType\]](#)) and is most often used when the table becomes too large and unwieldy to be included into the register field. (E.g. [Table 191 \[Valid Values for Memory Type Definition\]](#))

3.1.4.7 BIOS Recommendations

The BIOS recommendations table defines “BIOS.” recommendations that are conditional and complex enough to warrant a table.

Table 164 [BIOS Recommendations for D18F2x1B[4:0]], for example, specifies the BIOS recommendations for **D18F2x1B0[DcqBwThrotWm]** and **D18F2x1B4[DcqBwThrotWm1, DcqBwThrotWm2]**. All cells under the “Condition” header for a given row are ANDed to form the condition for the values to the right of the condition. For example, rows 1-3 and column 1 provide the following equivalent BIOS recommendation:

- **D18F2x1B0[DcqBwThrotWm]: BIOS: IF ([DdrRate==667](#)) THEN 4h ELSEIF ([DdrRate==800](#)) THEN 5h ELSEIF ([DdrRate==1066](#)) THEN 6h ESEIF etc.**

3.2 IO Space Registers

See [3.1 \[Register Descriptions and Mnemonics\]](#) for a description of the register naming convention.

IOCF8 IO-Space Configuration Address

Reset: 0. **IOCF8 [IO-Space Configuration Address]**, and **IOCFC [IO-Space Configuration Data Port]**, are used to access system configuration space, as defined by the PCI specification. **IOCF8** provides the address register and **IOCFC** provides the data port. Software sets up the configuration address by writing to **IOCF8**. Then, when an access is made to **IOCFC**, the processor generates the corresponding configuration access to the address specified in **IOCF8**. See [2.7 \[Configuration Space\]](#).

IOCF8 may only be accessed through aligned, DW IO reads and writes; otherwise, the accesses are passed to the appropriate IO link. Accesses to **IOCF8** and **IOCFC** received from an IO link are treated as all other IO transactions received from an IO link and are forwarded based on the settings in **D18F1x[DC:C0] [IO-Space Base/Limit]**. **IOCF8** and **IOCFC** in the processor are not accessible from an IO link.

Bits	Description
31	ConfigEn: configuration space enable. Read-write. 1=IO read and write accesses to IOCFC are translated into configuration cycles at the configuration address specified by this register. 0=IO read and write accesses are passed to the appropriate IO link and no configuration access is generated.
30:28	Reserved.
27:24	ExtRegNo: extended register number. Read-write. ExtRegNo provides bits[11:8] and RegNo provides bits[7:2] of the byte address of the configuration register. ExtRegNo is reserved unless it is enabled by MSRC001_001F[EnableCf8ExtCfg] .

23:16	BusNo: bus number. Read-write. Specifies the bus number of the configuration cycle.
15:11	Device: bus number. Read-write. Specifies the device number of the configuration cycle.
10:8	Function. Read-write. Specifies the function number of the configuration cycle.
7:2	RegNo: register address. Read-write. See IOCF8[ExtRegNo] .
1:0	Reserved.

IOCF8 IO-Space Configuration Data Port

Bits	Description
31:0	Data. Read-write. Reset: 0. See IOCF8 .

3.3 Device 0 Function 0 (Root Complex) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D0F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1536h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D0F0x04 Status/Command

Reset: 0000_0004h.

Bits	Description
31:21	Reserved.
20	CapList: capability list. Read-only. 1=Capability list supported.
19:3	Reserved.
2	BusMasterEn: bus master enable. Read-only.
1	MemAccessEn: memory access enable. Read-only.
0	IoAccessEn: IO access enable. Read-only.

D0F0x08 Class Code/Revision ID

Reset: 0600_0000h.

Bits	Description
31:8	ClassCode: class code. Read-only. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only.

D0F0x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:24	Reserved.
23	DeviceType. Read-only. 0b=Single function device. 1b=Multi-function device.
22:16	HeaderType. Read-only.
15:8	LatencyTimer. Read-only.
7:0	CacheLineSize. Read-only.

D0F0x2C Subsystem and Subvendor ID

Bits	Description
31:16	SubsystemID . Read-only; updated-by-hardware. Value: D0F0x50[SubsystemID] .
15:0	SubsystemVendorID . Read-only; updated-by-hardware. Value: D0F0x50[SubsystemVendorID] .

D0F0x34 Capabilities Pointer

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer . Read-only. There is no capability list.

D0F0x48 NB Header Write Register

Reset: 0000_0080h.

Bits	Description
31:8	Reserved.
7	DeviceType: device type . Read-write. This field sets the value in the corresponding field in D0F0x0C[DeviceType] . 0b=Single function device. 1b=Multi-function device.
6:0	Reserved.

D0F0x4C PCI Control

Reset: 0000_0000h.

Bits	Description
31:27	Reserved.
26	HPDDis: hot plug message disable . Read-write. 1=Hot plug message generation is disabled.
25:24	Reserved.
23	MMIOEnable: memory mapped IO enable . Read-write. 1=Decoding of MMIO cycles is enabled. The MMIO Base/Limit pair (D0F0x64_x17 and D0F0x64_x18) are decoded. This range is used to create an MMIO hole in the DRAM address range used for DMA decoding. DMA writes that fall into the MMIO range are treated as potential p2p requests. DMA reads that fall into the MMIO range are aborted as unsupported requests.
14:6	Reserved.
5	SerrDis: system error message disable . Read-write. 1=The generation of SERR messages is disabled.
4	PMEDis: PME disable . Read-write. 1=The generation of PME messages is disabled.
3:0	Reserved.

D0F0x60 Miscellaneous Index

Reset: 0000_0000h. The index/data pair registers, [D0F0x60](#) and [D0F0x64](#), are used to access the registers at [D0F0x64_x\[FF:00\]](#). To access any of these registers, the address is first written into the index register, [D0F0x60](#), and then the data is read from or written to the data register, [D0F0x64](#).

Bits	Description
31:7	Reserved.
6:0	MiscIndAddr: miscellaneous index register address. Read-write.

D0F0x64 Miscellaneous Index Data

See [D0F0x60](#). Address: [D0F0x60\[MiscIndAddr\]](#).

Bits	Description
31:0	MiscIndData: miscellaneous index data register.

D0F0x64_x00 Northbridge Control

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7	HwInitWrLock. Read-write. 1=Lock HWInit registers. 0=Unlock HWInit registers. This bit prevents updates to the IOC shadow copies of the BIF core configuration registers locked by D0F0xE4_x0140_0010[HwInitWrLock] .
6:0	Reserved.

D0F0x64_x0C IOC Bridge Control

Reset: 0000_0000h.

Bits	Description

D0F0x64_x0D IOC PCI Configuration

Bits	Description
0	PciDev0Fn2RegEn. Read-write. Reset: 0. 1=Enable configuration accesses to device 0 function 2.

D0F0x64_x16 IOC Advanced Error Reporting Control

Reset: 0000_0001h.

Bits	Description
0	AerUrMsgEn: AER unsupported request message enable. Read-write. BIOS: 0. 1=AER unsupported request messages are enabled.

D0F0x64_x17 Memory Mapped IO Base Address

Reset: 0000_0000h.

Bits	Description
31:0	MmioBase[47:16]: memory mapped IO base address. Read-write.

D0F0x64_x18 Memory Mapped IO Limit

Reset: 0000_0000h.

Bits	Description
31:0	MmioLimit[47:16]: memory mapped IO limit. Read-write.

D0F0x64_x19 Top of Memory 2 Low

Reset: 0000_0000h.

Bits	Description
31:23	Tom2[31:23]: top of memory 2. Read-write. BIOS: MSRC001_001D [TOM2[31:23]]. This field specifies the maximum system address for upstream read and write transactions that are forwarded to the host bridge (from the GNB to the UNB). All addresses less than this system address are forwarded to DRAM and are not checked to determine if the transaction is a peer-to-peer transaction. All upstream reads with addresses greater than or equal to this system address are master aborted. D0F0x64_x46 [P2PMode] controls the GNB response to writes with addresses greater than this system address.
22:1	Reserved.
0	TomEn: top of memory enable. Read-write. BIOS: MSRC001_0010 [MtrrTom2En]. 1=Top of memory check enabled.

D0F0x64_x1A Top of Memory 2 High

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	Tom2[39:32]: top of memory 2. Read-write. BIOS: MSRC001_001D [TOM2[39:32]]. See D0F0x64_x19 [Tom2].

D0F0x64_x1D Internal Graphics PCI Control

Reset: 0000_0000h.

Bits	Description
3	Vga16En: VGA IO 16 bit decoding enable. Read-write. 1=Address bits 15:10 for VGA IO cycles are decoded. 0=Address bits 15:10 for VGA IO cycles are ignored.
2	Reserved.

1	VgaEn: VGA enable. Read-write. 1=Enable VGA range in Intgfx.
0	Reserved.

D0F0x64_x1F FCH Location

Reset: 0002_0001h. NOTE: Register value of 32'b0 indicates the GNB is secondary and there is no FCH connected.

Bits	Description																		
31:16	SBLocatedCore: Indicates which GPP Core has the FCH attached to it. Read-write. This is a one-hot encoded field. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000h</td> <td>No FCH attached.</td> </tr> <tr> <td>0001h</td> <td>FCH located under PPD.</td> </tr> <tr> <td>0002h</td> <td>FCH located under SBG.</td> </tr> <tr> <td>FFFFh-0003h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0000h	No FCH attached.	0001h	FCH located under PPD.	0002h	FCH located under SBG.	FFFFh-0003h	Reserved.								
Bits	Definition																		
0000h	No FCH attached.																		
0001h	FCH located under PPD.																		
0002h	FCH located under SBG.																		
FFFFh-0003h	Reserved.																		
15:0	SBLocatedPort: Indicates which Port on the SBLocatedCore has the FCH. Read-write. This is a one-hot encoded field. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000h</td> <td>No FCH attached.</td> </tr> <tr> <td>0001h</td> <td>FCH located on Port A of SBLocatedCore.</td> </tr> <tr> <td>0002h</td> <td>FCH located on Port B of SBLocatedCore.</td> </tr> <tr> <td>0003h</td> <td>Reserved.</td> </tr> <tr> <td>0004h</td> <td>FCH located on Port C of SBLocatedCore.</td> </tr> <tr> <td>0007h-0005h</td> <td>Reserved.</td> </tr> <tr> <td>0008h</td> <td>FCH located on Port D of SBLocatedCore.</td> </tr> <tr> <td>FFFFh-0009h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0000h	No FCH attached.	0001h	FCH located on Port A of SBLocatedCore.	0002h	FCH located on Port B of SBLocatedCore.	0003h	Reserved.	0004h	FCH located on Port C of SBLocatedCore.	0007h-0005h	Reserved.	0008h	FCH located on Port D of SBLocatedCore.	FFFFh-0009h	Reserved.
Bits	Definition																		
0000h	No FCH attached.																		
0001h	FCH located on Port A of SBLocatedCore.																		
0002h	FCH located on Port B of SBLocatedCore.																		
0003h	Reserved.																		
0004h	FCH located on Port C of SBLocatedCore.																		
0007h-0005h	Reserved.																		
0008h	FCH located on Port D of SBLocatedCore.																		
FFFFh-0009h	Reserved.																		

D0F0x64_x22 LCLK Control 0

Reset: 7F3F_8100h.

Bits	Description
31	Reserved.
30	SoftOverrideClk0. Read-write. BIOS: 0. 1=Dynamic clock gating disabled for the host request path to the PCIe cores.
29	SoftOverrideClk1. Read-write. BIOS: 0. 1=Dynamic clock gating disabled for the host request path to the internal graphics and the host response path.
28	SoftOverrideClk2. Read-write. BIOS: 0. 1=Dynamic clock gating disabled for the host configuration requests.
27	SoftOverrideClk3. Read-write. BIOS: 0. 1=Dynamic clock gating disabled for the debug bus path.
26	SoftOverrideClk4. Read-write. BIOS: 0. 1=Dynamic clock gating disabled for the host request path to the configuration block.

D0F0x64_x23 LCLK Control 1

Reset: 7F3F_8100h.

Bits	Description
31	Reserved.
30	SoftOverrideClk0 . Read-write. BIOS: 0. 1=Dynamic clock gating disabled for upstream DMA requests from all sources.
29	SoftOverrideClk1 . Read-write. BIOS: 0. 1=Dynamic clock gating disabled for upstream DMA requests from the GPPFCH link core.
28	SoftOverrideClk2 . Read-write. BIOS: 0. 1=Dynamic clock gating disabled for upstream DMA requests from internal graphics and its DMA response reordering path.
27	SoftOverrideClk3 . Read-write. BIOS: 0. 1=Dynamic clock gating disabled for upstream DMA requests from internal graphics.
26	SoftOverrideClk4 . Read-write. BIOS: 0. 1=Dynamic clock gating disabled for upstream DMA requests from the Gfx link core.

D0F0x64_x3[4:0] Programmable Device Remap Register

Table 84: Reset values for D0F0x64_x3[4:0]

Register	Reset	Function
D0F0x64_x30	0000_0011h	Program [7:3]DevNum, [2:0]FnNum to map to PortA of PPD.
D0F0x64_x31	0000_0012h	Program [7:3]DevNum, [2:0]FnNum to map to PortB of PPD.
D0F0x64_x32	0000_0013h	Program [7:3]DevNum, [2:0]FnNum to map to PortC of PPD.
D0F0x64_x33	0000_0014h	Program [7:3]DevNum, [2:0]FnNum to map to PortD of PPD.
D0F0x64_x34	0000_0015h	Program [7:3]DevNum, [2:0]FnNum to map to PortE of PPD.

Software can only utilize device and function number combinations that are used by other (local) PCIe bridges. This effectively allows swapping of device and function numbers between bridges.

Bits	Description
31:8	Reserved.
7:0	DevFnMap . Read-write. Program [7:3]DevNum, [2:0]FnNum to map to PortA/B/C/D of each PCIe core.

D0F0x64_x46 IOC Features Control

Reset: 0001_1063h.

Bits	Description
27:24	Reserved.
21:17	Reserved.

16	CgttLclkOverride. Read-write. BIOS: 0. Global bit to disable all LCLK gating branches.										
2:1	<p>P2PMode: peer-to-peer mode. Read-write. Specifies how upstream write transactions above D0F0x64_x19[Tom2] are completed.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Mode 0. Master abort writes that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.</td> </tr> <tr> <td>01b</td> <td>Mode 1. Forward writes to the host bridge that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.</td> </tr> <tr> <td>10b</td> <td>Mode 2. Forward all writes to the host bridge0.</td> </tr> <tr> <td>11b</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	00b	Mode 0. Master abort writes that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.	01b	Mode 1. Forward writes to the host bridge that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.	10b	Mode 2. Forward all writes to the host bridge0.	11b	Reserved.
Bits	Definition										
00b	Mode 0. Master abort writes that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.										
01b	Mode 1. Forward writes to the host bridge that do not hit one of the internal PCI bridges. Forward writes that hit one of the internal PCI bridges to the bridge.										
10b	Mode 2. Forward all writes to the host bridge0.										
11b	Reserved.										

D0F0x7C IOC Configuration Control

Cold reset: 0000_0000h.

Bits	Description
31:1	Reserved.
0	ForceIntGfxDisable: internal graphics disable. Read-write. Setting this bit disables the internal graphics and the HD Audio controller.

D0F0x84 Link Arbitration

Bits	Description
9	PmeTurnOff: PME_Turn_Off message trigger. Read-write. Reset: 0. 1=Trigger a PME_Turn_Off message to all downstream devices if PmeMode=1.
8	PmeMode: PME message mode. Read-write. Reset: 0. 1=PME_Turn_Off message is triggered by writing PmeTurnOff. 0=PME_Turn_Off message is triggered by a PME_Turn_Off message from the FCH.
7:4	Reserved.
3	VgaHole: vga memory hole. Read-write. Reset: 1. This bit creates a hole in memory for the VGA memory range. 1=Requests hitting the VGA range are checked against PCI bridge memory ranges instead of being forwarded to system memory.
2:0	Reserved.

D0F0x90 Northbridge Top of Memory

Reset: 0000_0000h.

Bits	Description
31:23	TopOfDram. Read-write. BIOS: MSRC001_001A [TOM[31:23]]. Specifies the address that divides between MMIO and DRAM. From TopOfDram to 4G is MMIO; below TopOfDram is DRAM. See 2.4.3 [Access Type Determination].
22:0	Reserved.

D0F0x94 Northbridge ORB Configuration Offset

Reset: 0000_0000h.

The index/data pair registers, [D0F0x94](#) and [D0F0x98](#), are used to access the registers at [D0F0x98_x\[FF:00\]](#). To access any of these registers, the address is first written into the index register, [D0F0x94](#), and then the data is read from or written to the data register, [D0F0x98](#).

Bits	Description
31:7	Reserved.
6:0	OrbIndAddr: ORB index register address. Read-write.

D0F0x98 Northbridge ORB Configuration Data Port

See [D0F0x94](#). Address: [D0F0x94\[OrbIndAddr\]](#).

Bits	Description
31:0	OrbIndData: ORB index data register.

D0F0x98_x06 ORB Downstream Control 0

Reset: 0000_0000h.

Bits	Description
31:27	Reserved.
26	UmiNpMemWrEn. Read-write. BIOS: See 2.11.4 . 1=NP protocol over UMI for memory-mapped writes targeting LPC enabled. This bit may be set to avoid a deadlock condition.

D0F0x98_x07 ORB Upstream Arbitration Control 0

Reset: 0000_0080h.

Bits	Description						
31	SMUCsrIsocEn. Read-write. BIOS: 1. 1=CSR accesses go through ISOC channel. If this bit is set, D0F0x98_x1E[HiPriEn] must also be set.						
30:17	Reserved.						
16	SyncFloodOnParityErr. Read-write. Enable short circuit syncflood when arb_np detects a parity error for error containment.						
15	DropZeroMaskWrEn. Read-write. BIOS: 1. 1=Drop byte write request that have all bytes masked. 0=Forward byte write request that have all bytes masked.						
14:8	Reserved.						
7	IommuisocPassPWMode. Read-write. BIOS: 1. 1=Always set PassPW for IOMMU upstream iso-chronous requests.						
6	DmaReqRespPassPWMode. Read-write. BIOS: 0. Specifies the RespPassPW bit for non-posted upstream DMA requests.						
	<table border="1" style="width: 100%;"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Always 1.</td> </tr> <tr> <td>1</td> <td>Value passed from IOC.</td> </tr> </tbody> </table>	Bit	Description	0	Always 1.	1	Value passed from IOC.
Bit	Description						
0	Always 1.						
1	Value passed from IOC.						

5	Reserved.
4	IommuBwOptEn . Read-write. BIOS: 1. 1=Optimize IOMMU L2 byte write by detecting consecutive DW mask and translate the request to DW write.
3	Reserved.
2	IocRdROMapDis . Read-write. 1=Disable mapping relax ordering bit to RdRespPpw bit for IOC reads.
1	IocWrROMapDis . Read-write. 1=Disables mapping relax ordering bit to PassPw bit for IOC writes.
0	IocBwOptEn . Read-write. BIOS: 1. 1=Enable optimization of byte writes by detecting consecutive DW masks and translating the request to DW writes.

D0F0x98_x08 ORB Upstream Arbitration Control 1

This register specifies the weights of the weighted round-robin arbiter in stage 1 of the upstream arbitration for non-posted reads.

Bits	Description
31:24	NpWrrLenD . Read-write. Reset: 8h. BIOS: 8h. This field defines the maximum number of non-posted read requests from the SPG (PSP) that are serviced before the arbiter switches to the next client.
23:16	NpWrrLenC . Read-write. Reset: 8h. BIOS: 1h. This field defines the maximum number of non-posted read requests from the SMU that are serviced before the arbiter switches to the next client.
15:8	NpWrrLenB . Read-write. Reset: 8h. BIOS: 8h. This field defines the maximum number of non-posted read requests from IOMMU that are serviced before the arbiter switches to the next client.
7:0	NpWrrLenA . Read-write. Reset: 8h. BIOS: 8h. This field defines the maximum number of non-posted read requests from IOC that are serviced before the arbiter switches to the next client.

D0F0x98_x09 ORB Upstream Arbitration Control 2

Reset: 0000_0808h.

This register specifies the weights of the weighted round-robin arbiter in stage 1 of the upstream arbitration for posted writes.

Bits	Description
31:16	Reserved.
15:8	PWrrLenB . Read-write. This field defines the maximum number of posted write requests from the IOMMU that are serviced before the arbiter switches to the next client.
7:0	PWrrLenA . Read-write. This field defines the maximum number of posted write requests from the IOC that are serviced before the arbiter switches to the next client.

D0F0x98_x0C ORB Upstream Arbitration Control 5

Reset: 0000_0808h. This register specifies the weights of the weighted round-robin arbiter in stage 2 of the

upstream arbitration.

Bits	Description
31:24	Reserved.
23:16	Reserved.
15:8	GemWrrLenB . Read-write. BIOS: 08h. This field defines the maximum number of non-posted read requests from stage 1 that are getting serviced in the round-robin before the stage 2 arbiter switches to the next client.
7:0	GemWrrLenA . Read-write. BIOS: 08h. This field defines the maximum number of posted write requests from stage 1 that are getting serviced in the round-robin before the stage 2 arbiter switches to the next client.

D0F0x98_x1E ORB Receive Control 0

Reset: 4800_0000h.

Bits	Description
31:24	RxErrStatusDelay . Read-write. BIOS: 48h. Delay error status by number of LCLK cycles to filter false errors caused by reset skew.
23:2	Reserved.
1	HiPriEn . Read-write. BIOS: 1. 1=High priority channel enabled. See D0F0x98_x27 [UrRedirectAddr[31:6]]. IF (D0F0x98_x1E [HiPriEn]==0) THEN (D0F0x98_x07 [SMUCsrIsocEn]==0). IF (D0F0x98_x1E [HiPriEn]==1) THEN (D18F0x[E4,C4,A4,84] [IsocEn]==1) in order to fully enable the Isoc channel on the ONION Link.

D0F0x98_x26 ORB IOMMU Control 0

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	UrRedirectAddr[39:32] . Read-write. See: D0F0x98_x27 [UrRedirectAddr[31:6]].

D0F0x98_x27 ORB IOMMU Control 1

Reset: 0000_0000h.

Bits	Description
31:6	UrRedirectAddr[31:6] . Read-write. BIOS: UrRedirectAddr[39:6] must be programmed to a safe system memory address. UrRedirectAddr[39:6] = { D0F0x98_x26 [UrRedirectAddr[39:32]], UrRedirectAddr[31:6]}. IOMMU requests that are not directed to system memory are redirected to UrRedirectAddr.
5:0	Reserved.

D0F0x98_x28 ORB Transmit Control 0

Reset: 0000_0002h.

Bits	Description
1	ForceCoherentIntr. Read-write. BIOS: 1. 1=Interrupt request are forced to have coherent bit set.
0	Reserved.

D0F0x98_x2C ORB Clock Control

Reset: 000F_0204h.

Bits	Description
31:16	WakeHysteresis. Read-write. Char.Temp.BIOS: 19h. Specifies the amount of time hardware waits after ORB becomes idle before deasserting the wake signal to the NB. Wait time = WakeHysteresis * 200ns. (Wait time = WakeHysteresis * SMU timer pulse distance.) Changes to this field should be done prior to setting DynWakeEn.
15:10	Reserved.
9	SBDmaActiveMask. Read-write. BIOS: 1. 0=SB_DMA_ACTIVE_L state affects OnInbWake state. 1= SB_DMA_ACTIVE_L state is masked out.
8:3	Reserved.
2	CgttLclkOverride. Read-write. BIOS: 0h. Global bit to disable all LCLK gating branches in the ORB.
1	DynWakeEn. Read-write. BIOS: 1. 1=Enable dynamic toggling of the wake signal between ORB and NB. 0=Disable dynamic toggling of the wake signal. See WakeHysteresis.
0	Reserved.

D0F0x98_x37 ORB Allow LDTSTOP Control 0

Reset: 0020_0000h.

Bits	Description
31:28	Reserved.
27:16	LDTStopHystersis. Read-write. Specifies the number of timer periods (200 ns) (SMU timer pulse distance.) the AllowLDTStop signal is held low before ORB asserts the signal again.
15:2	Reserved.
1	DmaActiveOutEn. Read-write. 1=Enable ORB to drive the DMAACTIVE_L pin. Meaningful only when D0F0x98_x37[AllowLDTStopPinMode]==0.
0	AllowLDTStopPinMode. Read-write. Indicates the definition of the ALLOW_LDTSTOP pin. 0=Pin is used as DMAACTIVE_L. 1=Pin is used as ALLOW_LDTSTOP.

D0F0x98_x3A ORB Source Tag Translation Control 2

Reset: 0000_0000h.

Bits	Description
31:0	<p>ClumpingEn. Read-write. BIOS should follow the below requirements. Valid only for PPD and GBIF client clumping; internal unit ID ranges 4h-8h and 14h-17h respectively. Legal PPD clumping settings are: [8:4]=00010b, applicable only in x0/0/0/0/8 system configuration, recommended. Legal GBIF clumping settings are: [23:20]=0010b, 0110b and 1110b which are applicable in any system configuration. 1110b is the recommended value. All other bits of this register must always remain 0. See D18F0x[11C,118,114,110].</p>

D0F0x98_x3B ORB Source Tag Translation Control 3

Reset: 0000_0000h.

Bits	Description
31:0	IocOutstandingMask. Read-write. Limit number of outstanding requests for very dma client via the IOC.

D0F0x98_x4[A,9] ORB LCLK Clock Control 1-0

Reset: 7F3F_8100h.

Bits	Description
31	Reserved.
30	SoftOverrideClk0. Read-write. BIOS: 0. See SoftOverrideClk6.
29	SoftOverrideClk1. Read-write. BIOS: 0. See SoftOverrideClk6.
28	SoftOverrideClk2. Read-write. BIOS: 0. See SoftOverrideClk6.
27	SoftOverrideClk3. Read-write. BIOS: 0. See SoftOverrideClk6.
26	SoftOverrideClk4. Read-write. BIOS: 0. See SoftOverrideClk6.

25	SoftOverrideClk5. Read-write. BIOS: 0. See SoftOverrideClk6.
24	SoftOverrideClk6. Read-write. BIOS: 0. 1=Clock gating disabled. 0=Clock gating enabled. RULE: IF (SoftOverrideClk6==0) THEN (SoftOverrideClk3==0) ENDIF.

D0F0xB8 SMU Index Address

The index/data pair registers, **D0F0xB8** and **D0F0xBC**, are used to access the registers at **D0F0xBC_x[FFFFFFFFFF:00000000]**. To access any of these registers, the address is first written into the index register, **D0F0xB8**, and then the data is read from or written to the data register, **D0F0xBC**. Only a subset of SMU registers are listed in the BKDG.

Bits	Description
31:0	NbSmuIndAddr: smu index address. Read-write. Reset: 0.

D0F0xBC SMU Index Data

See **D0F0xB8**. Address: **D0F0xB8[NbSmuIndAddr]**.

Bits	Description
31:0	NbSmuIndData: smu index data.

D0F0xBC_x3F800 FIRMWARE_FLAGS

Reset: xxxx_xxxxh.

Bits	Description
31:24	TestCount. Read-write; updated-by-SMU. Test count. Increments when ever Test service (Service Index 0) is called.
23:1	Reserved. Read-write.
0	InterruptsEnabled. Read-write. <u>Bits</u> <u>Definition</u> 0 Firmware has not yet enabled interrupts. BIOS/Driver cannot yet send message interrupts to SMC. 1 Firmware has enabled interrupts. BIOS/Driver can send message interrupts to SMC.

D0F0xBC_x3F804 FIRMWARE_VID

Reset: xxxx_xxxxh.

Bits	Description
7:0	FirmwareVid. Read-write. Current voltage set by firmware voltage controller. The default value is specified by Fuse[SclkVid3].

D0F0xBC_x3F820 PM_INTERVAL_CNTL_0

Reset: xxxx_xxxhh.

Bits	Description
31:24	Loadline . Read-write.
23:16	VoltageCntrl . Read-write.
15:8	ThermalCntrl . Read-write. Specifies the period at which the GNB thermal algorithm is run. Period= D0F0xBC_x3F828[TimerPeriod] period*ThermalCntrl. See 2.11.6.3 [GNB Thermal Control] .
7:0	LclkDpm . Read-write.

D0F0xBC_x3F828 PM_TIMER_PERIOD

Bits	Description
31:0	TimerPeriod . Read-write. Reset: X. Specifies the period at which various power management related algorithms are run. Period = TimerPeriod / REFCLK.

D0F0xBC_x3F9D8 PM_CONFIG

Reset: xxxx_xxxhh.

Bits	Description						
31:30	Reserved. Read-write.						
29	SviMode . Read-write. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>SVI1.</td> </tr> <tr> <td>1</td> <td>SVI2.</td> </tr> </tbody> </table>	Bits	Description	0	SVI1.	1	SVI2.
Bits	Description						
0	SVI1.						
1	SVI2.						
28	BapmCoeffOverride . Read-write. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Calculate filter coefficients.</td> </tr> <tr> <td>1</td> <td>Use SW programmed filter coefficients; ignored if D18F4x15C[Boost-Lock]==1.</td> </tr> </tbody> </table>	Bits	Description	0	Calculate filter coefficients.	1	Use SW programmed filter coefficients; ignored if D18F4x15C[Boost-Lock]==1 .
Bits	Description						
0	Calculate filter coefficients.						
1	Use SW programmed filter coefficients; ignored if D18F4x15C[Boost-Lock]==1 .						
27	NbPstateAllCpusIdle . Read-write. BIOS: For CPU P-state associated with D18F3xA8[Pop-DownPstate] , IF (MSRC001_00[6B:64][NbPstate]==0) THEN 1. ELSE 0. ENDIF. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use low NB P-state voltage when AllCpusIdle.</td> </tr> <tr> <td>1</td> <td>Use high NB P-state voltage when AllCpusIdle.</td> </tr> </tbody> </table>	Bits	Description	0	Use low NB P-state voltage when AllCpusIdle.	1	Use high NB P-state voltage when AllCpusIdle.
Bits	Description						
0	Use low NB P-state voltage when AllCpusIdle.						
1	Use high NB P-state voltage when AllCpusIdle.						
26:24	PstateAllCpusIdle . Read-write. BIOS: D18F3xA8[PopDownPstate] . This field specifies the core P-state to use for IDD calculation when AllCpusIdle.						
5	EnableNbDpm . Read-write. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable Dynamic NB Pstate Management. Should be cleared before sending BIOSSMC_MSG_NBDPM_Disable message to SMU.</td> </tr> <tr> <td>1</td> <td>Enable Dynamic NB Pstate Management. Should be set before sending BIOSSMC_MSG_NBDPM_Enable message to SMU.</td> </tr> </tbody> </table>	Bits	Description	0	Disable Dynamic NB Pstate Management. Should be cleared before sending BIOSSMC_MSG_NBDPM_Disable message to SMU.	1	Enable Dynamic NB Pstate Management. Should be set before sending BIOSSMC_MSG_NBDPM_Enable message to SMU.
Bits	Description						
0	Disable Dynamic NB Pstate Management. Should be cleared before sending BIOSSMC_MSG_NBDPM_Disable message to SMU.						
1	Enable Dynamic NB Pstate Management. Should be set before sending BIOSSMC_MSG_NBDPM_Enable message to SMU.						

3	EnableLpmx. Read-write.						
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable LPMx. Should be cleared before sending BIOSSMC_MSG_LPMX_DISABLE message to SMU.</td></tr> <tr> <td>1</td><td>Enable LPMx. Should be set before sending BIOSSMC_MSG_LPMX_ENABLE message to SMU.</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0	Disable LPMx. Should be cleared before sending BIOSSMC_MSG_LPMX_DISABLE message to SMU.	1	Enable LPMx. Should be set before sending BIOSSMC_MSG_LPMX_ENABLE message to SMU.
<u>Bits</u>	<u>Description</u>						
0	Disable LPMx. Should be cleared before sending BIOSSMC_MSG_LPMX_DISABLE message to SMU.						
1	Enable LPMx. Should be set before sending BIOSSMC_MSG_LPMX_ENABLE message to SMU.						
2	EnableTdcLimit. Read-write.						
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable TDC Limit Check. Should be cleared before sending BIOSSMC_MSG_TDC_LIMIT_DISABLE message to SMU.</td></tr> <tr> <td>1</td><td>Enable TDC Limit Check. Should be set before sending BIOSSMC_MSG_TDC_LIMIT_ENABLE message to SMU.</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0	Disable TDC Limit Check. Should be cleared before sending BIOSSMC_MSG_TDC_LIMIT_DISABLE message to SMU.	1	Enable TDC Limit Check. Should be set before sending BIOSSMC_MSG_TDC_LIMIT_ENABLE message to SMU.
<u>Bits</u>	<u>Description</u>						
0	Disable TDC Limit Check. Should be cleared before sending BIOSSMC_MSG_TDC_LIMIT_DISABLE message to SMU.						
1	Enable TDC Limit Check. Should be set before sending BIOSSMC_MSG_TDC_LIMIT_ENABLE message to SMU.						
1	EnableBapm. Read-write.						
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable BAPM. Should be cleared before sending BIOSSMC_MSG_BAPM_DISABLE message to SMU.</td></tr> <tr> <td>1</td><td>Enable BAPM. Should be set before sending BIOSSMC_MSG_BAPM_ENABLE message to SMU.</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0	Disable BAPM. Should be cleared before sending BIOSSMC_MSG_BAPM_DISABLE message to SMU.	1	Enable BAPM. Should be set before sending BIOSSMC_MSG_BAPM_ENABLE message to SMU.
<u>Bits</u>	<u>Description</u>						
0	Disable BAPM. Should be cleared before sending BIOSSMC_MSG_BAPM_DISABLE message to SMU.						
1	Enable BAPM. Should be set before sending BIOSSMC_MSG_BAPM_ENABLE message to SMU.						
0	EnableVpcAccumulators. Read-write.						
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Disable Voltage, Power, Current Accumulator. Should be cleared before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.</td></tr> <tr> <td>1</td><td>Enable Voltage, Power, Current Accumulator. Should be set before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0	Disable Voltage, Power, Current Accumulator. Should be cleared before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.	1	Enable Voltage, Power, Current Accumulator. Should be set before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.
<u>Bits</u>	<u>Description</u>						
0	Disable Voltage, Power, Current Accumulator. Should be cleared before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.						
1	Enable Voltage, Power, Current Accumulator. Should be set before sending SMC_MSG_CONFIG_VPC_ACCUMULATOR message to SMU.						

D0F0xBC_x3F9E8 NB_DPM_CONFIG_1

Reset: xxxx_xxxxh.

Bits	Description										
31:24	DpmXNbPsHi. Read-write. See: Dpm0PgNbPsLo.										
23:16	DpmXNbPsLo. Read-write. See: Dpm0PgNbPsLo.										
15:8	Dpm0PgNbPsHi. Read-write. See: Dpm0PgNbPsLo.										
7:0	Dpm0PgNbPsLo. Read-write. Indexes the NB P-state used during specific levels of GPU activity. See 2.5.4.1 [NB P-states] .										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>NB P-state Indexed</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>D18F3x160 (see D18F5x16[C:0]).</td></tr> <tr> <td>01b</td><td>D18F3x164 (see D18F5x16[C:0]).</td></tr> <tr> <td>10b</td><td>D18F3x168 (see D18F5x16[C:0]).</td></tr> <tr> <td>11b</td><td>D18F3x16C (see D18F5x16[C:0]).</td></tr> </tbody> </table>	<u>Bits</u>	<u>NB P-state Indexed</u>	00b	D18F3x160 (see D18F5x16[C:0]).	01b	D18F3x164 (see D18F5x16[C:0]).	10b	D18F3x168 (see D18F5x16[C:0]).	11b	D18F3x16C (see D18F5x16[C:0]).
<u>Bits</u>	<u>NB P-state Indexed</u>										
00b	D18F3x160 (see D18F5x16[C:0]).										
01b	D18F3x164 (see D18F5x16[C:0]).										
10b	D18F3x168 (see D18F5x16[C:0]).										
11b	D18F3x16C (see D18F5x16[C:0]).										

D0F0xBC_x3F9EC NB_DPM_CONFIG_2

Reset: xxxx_xxxxh.

Bits	Description
31:25	Reserved.
24	EnableNbPsi1 . Read-write. Specifies how PSI1_L functions for VDDNB. 0=SMU firmware clears D18F5x188[NbPsi1] to 0. 1=SMU firmware sets D18F5x188[NbPsi1] to 1 whenever the GPU is power gated and in DPM0. See 2.5.6.1.2 [SCLK DPM] and 2.5.6.2 [GPU and Root Complex Power Gating] .
23:17	Reserved.
16	SkipDPM0 . Read-write. Specifies whether SMU waits for SCLK DPM to transition to state 0 before transitioning UNB to the NB P-states indexed Dpm0PgNbPsHi and Dpm0PgNbPsLo. 0=Wait for SCLK DPM state 0. 1=Do not wait for SCLK DPM state 0. See 2.5.4.1 [NB P-states] .
15:9	Reserved.
8	SkipPG . Read-write. Specifies whether SMU waits for the GPU to be power gated before transitioning UNB to the NB P-states indexed Dpm0PgNbPsHi and Dpm0PgNbPsLo. 0=Wait for GPU power gating. 1=Do not wait for GPU power gating. See 2.5.4.1 [NB P-states] .
7:0	Hysteresis . Read-write. Specifies the time the GPU must be idle before transitioning to the NB P-states indexed by Dpm0PgNbPsHi and Dpm0PgNbPsLo.

D0F0xBC_x3F9F4 CSR_GNB_1

Bits	Description
31:24	SviTrimValueVddNB . Read-write. Reset: x. BIOS: D18F5x188[NbLoadLineTrim].
23:16	SviTrimValueVdd . Read-write. Reset: x. BIOS: D18F5x12C[CoreLoadLineTrim].
15:0	Reserved.

D0F0xBC_x3F9F8 CSR_GNB_3

Reset: xxxx_xxxxh.

Bits	Description
31:16	Reserved. Read-write.
15:8	SviLoadLineOffsetVddNB . Read-write. Reset: x. BIOS: D18F5x188[NbOffsetTrim].
7:0	SviLoadLineOffsetVdd . Read-write. Reset: x. BIOS: D18F5x12C[CoreOffsetTrim].

D0F0xBC_x3FD[8C:00:step14] LCLK DPM Control 0

Reset: xxxx_xxxxh. See [2.5.6.1.3 \[LCLK DPM\]](#). Each register in D0F0xBC_x3FD[8C:00:step14] corresponds to one LCLK DPM state as follows.

Table 85: Register Mapping for D0F0xBC_x3FD[8C:00:step14]

Register	Function	Register	Function
D0F0xBC_x3FD00	State 0	D0F0xBC_x3FD50	State 4
D0F0xBC_x3FD14	State 1	D0F0xBC_x3FD64	State 5
D0F0xBC_x3FD28	State 2	D0F0xBC_x3FD78	State 6
D0F0xBC_x3FD3C	State 3	D0F0xBC_x3FD8C	State 7

Bits	Description
31:24	StateValid. Read-write. 1=DPM state is valid. 0=DPM state is invalid.
23:16	LclkDivider. Read-write. Specifies the LCLK divisor for this DPM state.
15:8	VID. Read-write. Specifies the VDDNB VID for this DPM state.
7:0	LowVoltageReqThreshold. Read-write.

D0F0xBC_x3FD[94:08:step14] LCLK DPM Control 2

Reset: xxxx_xxxhh. See 2.5.6.1.3 [LCLK DPM]. Each register in D0F0xBC_x3FD[94:08:step14] corresponds to one LCLK DPM state as follows.

Table 86: Register Mapping for D0F0xBC_x3FD[94:08:step14]

Register	Function	Register	Function
D0F0xBC_x3FD08	State 0	D0F0xBC_x3FD58	State 4
D0F0xBC_x3FD1C	State 1	D0F0xBC_x3FD6C	State 5
D0F0xBC_x3FD30	State 2	D0F0xBC_x3FD80	State 6
D0F0xBC_x3FD44	State 3	D0F0xBC_x3FD94	State 7

Bits	Description
31:16	ResidencyCounter. Read-write; S3-check-exclude.
15:8	HysteresisUp. Read-write; S3-check-exclude.
7:0	HysteresisDown. Read-write; S3-check-exclude.

D0F0xBC_x3FD[9C:10:step14] LCLK DPM Activity Thresholds

Reset: xxxx_xxxhh. See 2.5.6.1.3 [LCLK DPM]. Each register in D0F0xBC_x3FD[9C:10:step14] corresponds to one LCLK DPM state as follows.

Table 87: Register Mapping for D0F0xBC_x3FD[9C:10:step14]

Register	Function	Register	Function
D0F0xBC_x3FD10	State 0	D0F0xBC_x3FD60	State 4
D0F0xBC_x3FD24	State 1	D0F0xBC_x3FD74	State 5
D0F0xBC_x3FD38	State 2	D0F0xBC_x3FD88	State 6
D0F0xBC_x3FD4C	State 3	D0F0xBC_x3FD9C	State 7

Bits	Description
31:24	ActivityThreshold. Read-write. This field specifies the activity threshold as a percentage from 0 to 100%. When the current activity is above the threshold, DPM state is shifted up and when current activity is below the threshold, DPM state is shifted down.
23:16	EnabledForThrottle. Read-write.
15:0	Reserved.

D0F0xBC_x3FDC8 SMU_LCLK_DPM_CNTL

Reset: xxxx_xxxhh.

Bits	Description
31:24	LclkDpmEn. Read-write. 1b=Enable LCLK DPM
23:16	VoltageChgEn. Read-write. 1=Enable voltage change during LCLK DPM state transition.
15:8	LclkDpmBootState. Read-write.
7:0	Reserved.

D0F0xBC_x3FDD0 SMU_LCLK_DPM_THERMAL_THROTTLING_CNTL

Reset: xxxx_xxxhh. See 2.11.6.3 [GNB Thermal Control].

Bits	Description						
31:24	TtHtcActive. Read-write.						
23:16	LclkTtMode. Read-write; updated-by-SMU. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>LCLK thermal throttling is not active. The temperature is below the threshold.</td> </tr> <tr> <td>100b</td> <td>High temperature threshold has been reached and LCLK state is shifted down</td> </tr> </tbody> </table>	Bits	Definition	000b	LCLK thermal throttling is not active. The temperature is below the threshold.	100b	High temperature threshold has been reached and LCLK state is shifted down
Bits	Definition						
000b	LCLK thermal throttling is not active. The temperature is below the threshold.						
100b	High temperature threshold has been reached and LCLK state is shifted down						
15:8	TemperatureSel. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Use local (GNB) maximum temperature for LCLK thermal throttling.</td> </tr> <tr> <td>1</td> <td>Use global maximum temperature for LCLK thermal throttling.</td> </tr> </tbody> </table>	Bits	Definition	0	Use local (GNB) maximum temperature for LCLK thermal throttling.	1	Use global maximum temperature for LCLK thermal throttling.
Bits	Definition						
0	Use local (GNB) maximum temperature for LCLK thermal throttling.						
1	Use global maximum temperature for LCLK thermal throttling.						
7:0	LclkThermalThrottlingEn. Read-write. 1=Enable LCLK thermal throttling.						

D0F0xBC_x3FDD4 SMU_LCLK_DPM_THERMAL_THROTTLING_THRESHOLDS

Reset: xxxx_xxxhh. See 2.11.6.3 [GNB Thermal Control].

Bits	Description
31:16	HighThreshold. Read-write. Specifies the high thermal threshold for LCLK thermal throttling. See D18F5xA8_x383[GblMaxTemp].
15:0	LowThreshold. Read-write. Specifies the low thermal threshold for LCLK thermal throttling. See D18F5xA8_x383[GblMaxTemp].

D0F0xBC_xC020_008C LCLK_DEEP_SLEEP_CNTL

Bits	Description																		
2:0	DivId. Read-write. Reset: 5. BIOS: 100b. <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Clock OFF</td></tr> <tr> <td>001b</td><td>Divide by 2</td></tr> <tr> <td>010b</td><td>Divide by 4</td></tr> <tr> <td>011b</td><td>Divide by 8</td></tr> <tr> <td>100b</td><td>Divide by 16</td></tr> <tr> <td>101b</td><td>Divide by 32</td></tr> <tr> <td>110b</td><td>Reserved</td></tr> <tr> <td>111b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	000b	Clock OFF	001b	Divide by 2	010b	Divide by 4	011b	Divide by 8	100b	Divide by 16	101b	Divide by 32	110b	Reserved	111b	Reserved
Bits	Description																		
000b	Clock OFF																		
001b	Divide by 2																		
010b	Divide by 4																		
011b	Divide by 8																		
100b	Divide by 16																		
101b	Divide by 32																		
110b	Reserved																		
111b	Reserved																		

D0F0xBC_xC020_0110 Activity Monitor Control

Bits	Description												
31:11	Reserved.												
10	EnOrbDsCnt. Read-write. Reset: X. 1=Enable ORB downstream counter.												
9	EnOrbUsCnt. Read-write. Reset: X. 1=Enable ORB upstream counter.												
8	EnBifCnt. Read-write. Reset: X. 1=Enable BIF counter.												
4:3	BusyCntSel. Read-write. Reset: 0. Specifies subcomponents or activity monitored by the LCLK activity monitor. <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>GFX DMA (BIF)</td><td>10b</td><td>ORB Downstream activity</td></tr> <tr> <td>01b</td><td>ORB Upstream activity</td><td>11b</td><td>ORB Up/downstream activity max</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	GFX DMA (BIF)	10b	ORB Downstream activity	01b	ORB Upstream activity	11b	ORB Up/downstream activity max
Bits	Definition	Bits	Definition										
00b	GFX DMA (BIF)	10b	ORB Downstream activity										
01b	ORB Upstream activity	11b	ORB Up/downstream activity max										
2	Reserved.												
1	PeriodCntRst. Read-write. Reset: X.												
0	ActivityCntRst. Read-write. Reset: X.												

D0F0xBC_xC210_0000 CPU Interrupt RequestSee [2.12.1 \[Software Interrupts\]](#).

Bits	Description
31:17	Reserved.
16:1	ServiceIndex. Read-write; S3-check-exclude. Reset: 0.
0	IntToggle. Read-write; S3-check-exclude. Reset: 0.

D0F0xBC_xC210_0004 CPU Interrupt StatusSee [2.12.1 \[Software Interrupts\]](#).

Bits	Description
31:2	Reserved.

1	IntDone. Read-only; updated-by-hardware. Reset: 0.
0	IntAck. Read-only; updated-by-hardware. Reset: 0.

D0F0xBC_xC210_003C CPU Interrupt ArgumentSee [2.12.1 \[Software Interrupts\]](#).

Bits	Description
31:0	Argument. Read-write. Reset: 0. Optional argument for a software interrupt.

D0F0xBC_xC210_0040 CPU Interrupt ResponseSee [2.12.1 \[Software Interrupts\]](#).

Bits	Description
31:0	Argument. Read-write. Reset: 0. Optional response data upon completing a software interrupt.

D0F0xC8 DEV Index Address

The index/data pair registers, [D0F0xC8](#) and [D0F0xCC](#) are used to access the registers at [D0F0xCC_x\[FF:00\]](#). To access any of these registers, the address is first written into the index register, [D0F0xC8](#), and then the data is read from or written to the data register, [D0F0xCC](#). Specific bridges (Device/Function) are selected using the [D0F0xC8\[NbDevIndSel\]](#) field.

Bits	Description																								
31:24	Reserved.																								
23:16	NbDevIndSel: Device selector. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>10h-00h</td> <td>Reserved</td> <td>15h</td> <td>D2F5</td> </tr> <tr> <td>11h</td> <td>D2F1</td> <td>FFh-16h</td> <td>Reserved</td> </tr> <tr> <td>12h</td> <td>D2F2</td> <td></td> <td></td> </tr> <tr> <td>13h</td> <td>D2F3</td> <td></td> <td></td> </tr> <tr> <td>14h</td> <td>D2F4</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	10h-00h	Reserved	15h	D2F5	11h	D2F1	FFh-16h	Reserved	12h	D2F2			13h	D2F3			14h	D2F4		
Bits	Definition	Bits	Definition																						
10h-00h	Reserved	15h	D2F5																						
11h	D2F1	FFh-16h	Reserved																						
12h	D2F2																								
13h	D2F3																								
14h	D2F4																								
15:7	Reserved.																								
6:0	NbDevIndAddr: Bridge (Device) index address. Read-write. Reset: 0.																								

D0F0xCC DEV Index DataSee [D0F0xC8](#). Address: [D0F0xC8\[NbDevIndAddr\]](#).

Bits	Description
31:0	NbDevIndData: dev index data.

D0F0xCC_x01 IOC Bridge Control

Reset: 0000_0000h.

Bits	Description
31:24	ApicRange . Read-write. Sets the bridge APIC range.
23	ApicEnable . Read-write. 1=Enables the bridge APIC range decoding. Requests fall in bridge APIC range if addr[39:12]={20'h00_FEC, APIC_Range[7:0]}.
22:21	Reserved.
20	SetPowEn . Read-write. 1=Enable generation of set_slot_power message to the bridge.
19	Reserved.
18	CrsEnable . Read-write. 1=Enables the hardware retry on receiving configuration request retry status.
17	ExtDevCrsEn . Read-write. 1=Reset the bridge CRS counter when an external device is plugged in or the link is down.
16	ExtDevPlug . Read-write. 1=Indicates to IOC that an external device is being plugged on the bridge.
15:4	Reserved.
3	P2pDis . Read-write. 1=Disables local peer-to-peer transactions forwarded to this bridge.
2	CfgDis . Read-write. 1=Configuration accesses to this bridge are disabled. Non-FCH bridges are not expected to set this bit.
1	BusMasterDis . Read-write. 1=The bridge's ability to operate as a bus master is disabled. This overrides the Bus Master Enable bit in the bridge.
0	BridgeDis . Read-write. 1=The bridge is hidden and no accesses are allowed to this bridge.

D0F0xD4_x0109_14C3 Bif Doorbell Control Ind

Reset: 0000_0000h.

Bits	Description

D0F0xD4_x0109_14E1 CC Bif Bx Strap0 Ind

Reset: 0000_C004h.

Bits	Description
12	StrapBifDoorbellBarDis . Read-write.
5:3	StrapBifMemApSize . Read-write.
2:1	StrapBifRegApSize . Read-write.
0	Reserved.

D0F0xD4_x0109_14E2 CC Bif Bx Strap1 Ind

Reset: 0000_0000h.

Bits	Description
3	StrapBifF064BarDisA . Read-write.
1	StrapBifIoBarDis . Read-write.
0	Reserved.

D0F0xD4_x0109_1507 CC Bif Bx Pinstrap0 Ind

Reset: 0000_0802h.

Bits	Description
7:5	StrapBifMemApSizePin. Read-write.

D0F0xE0 Link Index Address 1

Reset: 0130_8001h.

D0F0xE0 and **D0F0xE4** are used to access **D0F0xE4_x[FFFF_FFFF:0000_0000]**. To read or write to one of these register, the address is written first into the address register **D0F0xE0** and then the data is read from or written to the data register **D0F0xE4**.

The phy index registers (**D0F0xE4_x0[2:1]xxx_xxxx**) mapping to a specific phy, pin or pin group is shown in a table in the register definition. For example, to perform a read or write operation to configure Gfx phy 0 (P_GFX_[T,R]X[P,N][7:0] pin group) compensation, software should program **D0F0xE0[31:0]=0120_0000h**. Accessing any register number that is not listed in the mapping table may result in undefined behavior.

Some phy registers support broadcast write operations to groups of 4 or 8 lanes. For example, to perform broadcast write operation to configure Gfx Link[3:0] (P_GFX_RX[P,N][3:0] lanes) receiver phase loop filter, software should program **D0F0xE0[31:0]=0120_5602h**.

Bits	Description												
31:24	BlockSelect: block select. Read-write; S3-check-exclude. This field is used to select the specific register block to access. The encodings supported depends on the FrameType selected. <table> <thead> <tr> <th><u>FrameType</u></th> <th><u>Encoding</u></th> </tr> </thead> <tbody> <tr> <td>01h</td> <td>1=GPP link core</td> </tr> <tr> <td>10h</td> <td>1=Phy interface 0</td> </tr> <tr> <td>20h</td> <td>1=Phy 0</td> </tr> <tr> <td>30h</td> <td>1=Wrapper</td> </tr> <tr> <td>40h</td> <td>1=IO link core</td> </tr> </tbody> </table>	<u>FrameType</u>	<u>Encoding</u>	01h	1=GPP link core	10h	1=Phy interface 0	20h	1=Phy 0	30h	1=Wrapper	40h	1=IO link core
<u>FrameType</u>	<u>Encoding</u>												
01h	1=GPP link core												
10h	1=Phy interface 0												
20h	1=Phy 0												
30h	1=Wrapper												
40h	1=IO link core												
23:16	FrameType: frame type. Read-write; S3-check-exclude. This field is used to select the type of register block to access. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Destination</u></th> </tr> </thead> <tbody> <tr> <td>10h</td> <td>GPP Phy interface block registers.</td> </tr> <tr> <td>20h</td> <td>GPP Phy registers.</td> </tr> <tr> <td>30h</td> <td>GPP Wrapper registers.</td> </tr> <tr> <td>40h</td> <td>GPP IO Link registers.</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Destination</u>	10h	GPP Phy interface block registers.	20h	GPP Phy registers.	30h	GPP Wrapper registers.	40h	GPP IO Link registers.		
<u>Bits</u>	<u>Destination</u>												
10h	GPP Phy interface block registers.												
20h	GPP Phy registers.												
30h	GPP Wrapper registers.												
40h	GPP IO Link registers.												
15:0	PcieIndxAddr: index address. Read-write; S3-check-exclude.												

D0F0xE4 Link Index Data 1

S3-check-exclude. See **D0F0xE0**. Address: {**D0F0xE0[BlockSelect]**,**D0F0xE0[FrameType]**,**D0F0xE0[PcieIndxAddr]**}.

Bits	Description
31:0	PcieIndxData: index data.

3.3.1 PIF Registers

D0F0xE4_x0110_0010 PIF Control (GPPSB_PIF0_CNTL)

Reset: 3190_44D8h.

Bits	Description																				
19:17	Ls2ExitTime: LS2 exit time. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>14us</td> <td>100b</td> <td>30us</td> </tr> <tr> <td>001b</td> <td>10us</td> <td>101b</td> <td>100ns</td> </tr> <tr> <td>010b</td> <td>15us</td> <td>110b</td> <td>100us</td> </tr> <tr> <td>011b</td> <td>20us</td> <td>111b</td> <td>50us</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	14us	100b	30us	001b	10us	101b	100ns	010b	15us	110b	100us	011b	20us	111b	50us
Bits	Definition	Bits	Definition																		
000b	14us	100b	30us																		
001b	10us	101b	100ns																		
010b	15us	110b	100us																		
011b	20us	111b	50us																		
7	RxDetectTxPwrMode: receiver detection transmitter power mode. Read-write. 1=Transmitter is powered on.																				
6	RxDetectFifoResetMode: receiver detect FIFO reset mode. Read-write. BIOS: 1. 1=The transmit FIFO is reset after receiver detection. 0=The transmit FIFO is not reset after receiver detection.																				
4	EiDetCycleMode: electrical idle detect mode. Read-write. 1=Electrical idle cycle detection mode is enabled in L1. 0=Electrical idle detection is always enabled in L1.																				

D0F0xE4_x0110_0011 PIF Pairing (PIF0_PAIRING)

Reset: 0200_0000h.

Bits	Description
31:26	Reserved.
25	MultiPif: x16 link. Read-write. 1=Lanes 7:0 are paired with a second PIF to create a x16 link.
24:21	Reserved.
20	X16Lane150: x16 link lanes 15:0. Read-write. 1=Lanes 15:0 are paired to create a x16 link.
19:18	Reserved.
17	X8Lane158: x8 link lanes 15:8. Read-write. 1=Lanes 15:8 are paired to create a x8 link.
16	X8Lane70: x8 link lanes 7:0. Read-write. 1=Lanes 7:0 are paired to create a x8 link.
15:12	Reserved.
11	X4Lane1512: x4 link lanes 15:12. Read-write. 1=Lanes 15:12 are paired to create a x4 link.
10	X4Lane118: x4 link lanes 11:8. Read-write. 1=Lanes 11:8 are paired to create a x4 link.
9	X4Lane74: x4 link lanes 7:4. Read-write. 1=Lanes 7:4 are paired to create a x4 link.
8	X4Lane30: x4 link lanes 3:0. Read-write. 1=Lanes 3:0 are paired to create a x4 link.
7	X2Lane1514: x2 link lanes 15:14. Read-write. 1=Lanes 15:14 are paired to create a x2 link
6	X2Lane1312: x2 link lanes 13:12. Read-write. 1=Lanes 13:12 are paired to create a x2 link
5	X2Lane1110: x2 link lanes 11:10. Read-write. 1=Lanes 11:10 are paired to create a x2 link
4	X2Lane98: x2 link lanes 9:8. Read-write. 1=Lanes 9:8 are paired to create a x2 link

3	X2Lane76: x2 link lanes 7:6. Read-write. 1=Lanes 7:6 are paired to create a x2 link.
2	X2Lane54: x2 link lanes 5:4. Read-write. 1=Lanes 5:4 are paired to create a x2 link.
1	X2Lane32: x2 link lanes 3:2. Read-write. 1=Lanes 3:2 are paired to create a x2 link.
0	X2Lane10: x2 link lanes 1:0. Read-write. 1=Lanes 1:0 are paired to create a x2 link.

D0F0xE4_x0110_001[8:7,3:2] PIF Power Down Control [3:0] (PIF0_PWRDOWN)

Reset: 0001_1FA2h.

Table 88: Index addresses for D0F0xE4_x0110_001[8:7,3:2]

D0F0xE0[31:16]	D0F0xE0[15:0]			
	0018h	0017h	0013h	0012h
0110h	PIF Lanes 15-12	PIF Lanes 11-8	PIF Lanes 7-4	PIF Lanes 3-0

Bits	Description																				
31:29	PllPwrOverrideVal: PLL power state override value. Read-write. See TxPowerStateInTxs2.																				
28	PllPwrOverrideEn: PLL power state override enable. Read-write. 1=PLL forced to the power state specified by PllPwrOverrideVal.																				
27	Reserved.																				
26:24	PllRampUpTime: PLL ramp time. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>10 us</td> <td>100b</td> <td>50 us</td> </tr> <tr> <td>001b</td> <td>5 us</td> <td>101b</td> <td>300 us</td> </tr> <tr> <td>010b</td> <td>15 us</td> <td>110b</td> <td>500 us</td> </tr> <tr> <td>011b</td> <td>22 us</td> <td>111b</td> <td>800 us</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	10 us	100b	50 us	001b	5 us	101b	300 us	010b	15 us	110b	500 us	011b	22 us	111b	800 us
Bits	Definition	Bits	Definition																		
000b	10 us	100b	50 us																		
001b	5 us	101b	300 us																		
010b	15 us	110b	500 us																		
011b	22 us	111b	800 us																		
23:17	Reserved.																				
16	Tx2p5clkClockGatingEn. Read-write. 1=The 2.5x TxClk is gated if the lane is idle 0=The 2.5x TxClk is never gated.																				
15:13	Reserved.																				
12:10	PllPowerStateInOff: PLL off power state. Read-write. See: TxPowerStateInTxs2. All links associated with the PLL must be in the off state to transition the PLL to this state.																				
9:7	PllPowerStateInTxs2: PLL L1 power state. Read-write. See: TxPowerStateInTxs2. All links associated with the PLL must be in L1 to transition the PLL to this state.																				
6:4	RxPowerStateInRxs2: receiver L1 power state. Read-write. See: TxPowerStateInTxs2.																				
3	ForceRxEnInL0s: force receiver enable in L0s. Read-write. 1=The phy CDR is always enabled in L0s.																				
2:0	TxPowerStateInTxs2: transmitter L1 power state. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>L0</td> <td>100b</td> <td>Reserved</td> </tr> <tr> <td>001b</td> <td>LS1</td> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>010b</td> <td>LS2</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>Reserved</td> <td>111b</td> <td>Off</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	L0	100b	Reserved	001b	LS1	101b	Reserved	010b	LS2	110b	Reserved	011b	Reserved	111b	Off
Bits	Definition	Bits	Definition																		
000b	L0	100b	Reserved																		
001b	LS1	101b	Reserved																		
010b	LS2	110b	Reserved																		
011b	Reserved	111b	Off																		

3.3.2 Phy Registers

3.3.2.1 Global Phy Control Registers

D0F0xE4_x0120_0004 Phy Global Control 0

Bits	Description
17:16	CfgIdleDetTh. Read-write. Reset: 1. BIOS: 0. Idle detector threshold control

D0F0xE4_x0120_4440 Phy RO PLL Control

Bits	Description										
14:13	PllDbgRoIPFDResetCntrl. Read-write. Reset: 0. BIOS: 2. PFD reset pulse width control. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>PFD reset pulse width = 603 ps (@85C_tt)</td> </tr> <tr> <td>01b</td> <td>PFD reset pulse width = 190 ps (@85C_tt)</td> </tr> <tr> <td>10b</td> <td>PFD reset pulse width = 397 ps (@85C_tt)</td> </tr> <tr> <td>11b</td> <td>PFD reset pulse width = 82 ps (@85C_tt)</td> </tr> </tbody> </table>	Bits	Definition	00b	PFD reset pulse width = 603 ps (@85C_tt)	01b	PFD reset pulse width = 190 ps (@85C_tt)	10b	PFD reset pulse width = 397 ps (@85C_tt)	11b	PFD reset pulse width = 82 ps (@85C_tt)
Bits	Definition										
00b	PFD reset pulse width = 603 ps (@85C_tt)										
01b	PFD reset pulse width = 190 ps (@85C_tt)										
10b	PFD reset pulse width = 397 ps (@85C_tt)										
11b	PFD reset pulse width = 82 ps (@85C_tt)										

D0F0xE4_x0120_4450 PhyRO PLL Override Control 0

Bits	Description						
30	PllCfgROVTOIBiasCntrlOvrdVal0. Read-write. Reset: 1. BIOS: 0. Override value bit for CP_PLL_CFG_RO_VTOI_BIAS_CNTRL.						
7:0	PllCfgROBWcntrlOvrdVal0. Read-write. Reset: 8Dh. BIOS: 90h. Override value bit for CP_PLL_CFG_RO_BW_CNTRL. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[7:3]</td> <td>Proportional CP current setting</td> </tr> <tr> <td>[2:0]</td> <td>Integral CP current setting</td> </tr> </tbody> </table>	Bit	Definition	[7:3]	Proportional CP current setting	[2:0]	Integral CP current setting
Bit	Definition						
[7:3]	Proportional CP current setting						
[2:0]	Integral CP current setting						

3.3.3 Wrapper Registers

D0F0xE4_x0130_0046 Subsystem and Vendor ID

Bits	Description
31:16	SubsystemID: subsystem id . Read-write. Reset: 1234h. Specifies the value returned by D2F[5:1]xB4[SubsystemID].
15:0	SubsystemVendorID: subsystem vendor id . Read-write. Reset: 1022h. Specifies the value returned by D2F[5:1]xB4[SubsystemVendorID].

D0F0xE4_x0130_0080 Link Configuration (PCIE_LINK_CONFIG)

Reset: 0000_0000h.

Bits	Description																				
31:4	Reserved.																				
3:0	StrapBifLinkConfig . Read-write; strap. BIOS: See Table 62 . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Reserved</td> <td>0100b</td> <td>4 x1 IO Links (GPPFCH Only)</td> </tr> <tr> <td>0001b</td> <td>x4 IO Link (GPPFCH Only)</td> <td>0101b</td> <td>Reserved</td> </tr> <tr> <td>0010b</td> <td>2 x2 IO Links (GPPFCH Only)</td> <td>011xb</td> <td>Reserved</td> </tr> <tr> <td>0011b</td> <td>1 x2 IO Link, 2 x1 IO Links (GPPFCH Only)</td> <td>1xxxb</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000b	Reserved	0100b	4 x1 IO Links (GPPFCH Only)	0001b	x4 IO Link (GPPFCH Only)	0101b	Reserved	0010b	2 x2 IO Links (GPPFCH Only)	011xb	Reserved	0011b	1 x2 IO Link, 2 x1 IO Links (GPPFCH Only)	1xxxb	Reserved
Bits	Definition	Bits	Definition																		
0000b	Reserved	0100b	4 x1 IO Links (GPPFCH Only)																		
0001b	x4 IO Link (GPPFCH Only)	0101b	Reserved																		
0010b	2 x2 IO Links (GPPFCH Only)	011xb	Reserved																		
0011b	1 x2 IO Link, 2 x1 IO Links (GPPFCH Only)	1xxxb	Reserved																		

D0F0xE4_x0130_0[C:8]00 Link Hold Training Control (PCIE_HOLD_TRAINING)

Table 89: Index address mapping for D0F0xE4_x0130_0[C:8]00

Index	Function
0130_0800h	GPPSB PortA
0130_0900h	GPPSB PortB
0130_0A00h	GPPSB PortC
0130_0B00h	GPPSB PortD
0130_0C00h	GPPSB PortE

Bits	Description
31:1	Reserved.
0	HoldTraining: hold link training . Read-write. Reset: 1. 1=Hold training on link.

D0F0xE4_x0130_0[C:8]03 Link Deemphasis Control (LC_MISC_PORT)

Table 90: Index address mapping for D0F0xE4_x0130_0[C:8]03

Index	Function
0130_0803h	GPPSB PortA
0130_0903h	GPPSB PortB
0130_0A03h	GPPSB PortC
0130_0B03h	GPPSB PortD
0130_0C03h	GPPSB PortE

Bits	Description
31:6	Reserved.
5	StrapBifDeemphasisSel. Read-write; strap. Reset: 1. Controls the default value of D2F[5:1]x88[SelectableDeemphasis]. 1=RC advertises -3.5dB. 0=RC advertises -6dB.

D0F0xE4_x0130_0[C:8]04 Link AER Control

Bits	Description
3:1	StrapBifMaxPayloadSupport. Read-write; strap. Reset: 2h. BIOS: See 2.11.3.2 [Link Configurations].

D0F0xE4_x0130_0[C:8]05 Link Training Control

Reset: 1800_0000h.

Table 91: Index address mapping for D0F0xE4_x0130_0[C:8]05

Index	Function
0130_0805h	GPPSB PortA
0130_0905h	GPPSB PortB
0130_0A05h	GPPSB PortC
0130_0B05h	GPPSB PortD
0130_0C05h	GPPSB PortE

Bits	Description
31:24	StrapBifInitialNFTs. Read-write; strap. BIOS: 40h. Specifies the number of Fast Training Sets(FTS) transmitted. FTS are special packets transmitted to exit out of the PCIe L0s sleep state.

D0F0xE4_x0130_8002 IO Link Wrapper Scratch

Cold reset: 0000_0000h.

Bits	Description
31:0	PcieWrapScratch: Scratch. Read-write.

D0F0xE4_x0130_8011 Link Transmit Clock Gating Control

Bits	Description
25	Reserved.
24	TxclkLcntGateEnable . Read-write. Reset: 0. BIOS: 1. 1=Enable clock gating the lane counter.
23	DebugBusClkEnable . Read-write. Reset: 1. BIOS: 0. 1=Enable the debug bus clock.
22:17	TxclkPermGateLatency . Read-write. Reset: 3Fh. Specifies the number of clocks to wait after detecting an entry into L1 before gating off the permanent clock branches.
16	RcvrDetClkEnable . Read-write. Reset: 0. 1=Enable the receiver detect clock.
15:10	TxclkRegsGateLatency . Read-write. Reset: 3Fh. Specifies the number of clocks to wait after idle is signalled before gating off the register clock branch.
9	TxclkRegsGateEnable . Read-write. Reset: 0. BIOS: 1. 1=Enable clock gating the register clock.
8	TxclkPermStop . Read-write. Reset: 0. 1>All transmitter clocks disabled. This bit should only be set if all links associated with the PCIe core are unconnected.
7	TxclkDynGateEnable . Read-write. Reset: 0. BIOS: 1. 1=Dynamic clock gating enabled. 0=Dynamic clock gating disabled.
6	TxclkPermGateEven . Read-write. Reset: 1. 1=Gate the permanent clock branches for an even number of clocks.
5:0	TxclkDynGateLatency . Read-write. Reset: 3Fh. Specifies the number of clocks to wait after idle is signalled before gating off the dynamic clock branch.

D0F0xE4_x0130_8012 Link Idle-Resume Clock Gating Control

Bits	Description
31:14	Reserved.
13:8	Pif1xIdleResumeLatency . Read-write. Reset: 00_0111b. Specifies the number of clocks to wait after enabling TXCLK1X_PIF before sending the acknowledge.
7	Pif1xIdleGateEnable . Read-write. Reset: 0. BIOS: 1. 1=Enable idle resume gating of TXCLK1X_PIF.
6	Reserved.
5:0	Pif1xIdleGateLatency . Read-write. Reset: 0_0001b. Specifies the number of clocks to wait before turning off TXCLK1X_PIF.

D0F0xE4_x0130_8013 Transmit Clock Pll Control

Reset: 0000_0001h.

Bits	Description
31:15	Reserved.
14:13	PhyRxIsoDis . Read-write. 1=Isolate PHY signals to PIF.
12	Reserved.

11	Reserved.
10	TxclkSelPifBOverride . Read-write. 1=Override TxclkPifB selection.
9	TxclkSelPifAOverride . Read-write. 1=Override TxclkPifA selection.
8	TxclkSelCoreOverride . Read-write. 1=Override TxclkCore selection.
7	Reserved.
6	Reserved.
5	ClkDividerResetOverrideB . Read-write. 1=Force clock divider B enabled.
4	ClkDividerResetOverrideA . Read-write. 1=Force clock divider A enabled.
3	Reserved.
2	Reserved.
1	MasterPciePllB . Read-write. 1=PLL B is the master source for all PCIe transmitter clock branches.
0	MasterPciePllA . Read-write. 1=PLL A is the master source for all PCIe transmitter clock branches.

D0F0xE4_x0130_8014 Link Transmit Clock Gating Control 2

Reset: 0000_0000h.

Bits	Description
31:28	SpareRegRw . Read-write. Spare register.
27	Reserved.
26	Reserved.
25	Reserved.
24	Reserved.
23:21	Reserved.
20	TxclkPermGateOnlyWhenPllPwrDn . Read-write. BIOS: 1. 1=Gating of the permanent clock branch only occurs when the PLL is powered down.
19:16	Reserved.
15	Reserved.
14	Reserved.

13	PcieGatePifB1xEnable. Read-write. BIOS: 1. 1=Enable gating of the PIF B 1x clock branches in PCIe mode.
12	PcieGatePifA1xEnable. Read-write. BIOS: 1. 1=Enable gating of the PIF A 1x clock branches in PCIe mode.
11:6	Reserved.
5	Reserved.
4	Reserved.
3	Reserved.
2	Reserved.
1	TxclkPrbsGateEnable. Read-write. BIOS: 1. 1=Enable gating of the PRBS clock branch.
0	TxclkPermGateEnable. Read-write. BIOS: 1. 1=Enable gating of the permanent clock branch.

D0F0xE4_x0130_8015 IO Link IOC Control

Bits	Description
31:24	Reserved.
23	RefclkRegsGateEnable. Read-write. Reset:0. BIOS: 1. 1=Enable gating of REFCLK_REGS.
22	Reserved.
21:16	RefclkRegsGateLatency. Read-write. Reset:3Fh. Specifies the number of clocks to wait before turning off REFCLK_REGS.

D0F0xE4_x0130_8016 Link Clock Switching Control

Reset: 003F_001Fh.

Bits	Description
31:24	Reserved.
23	LclkDynGateEnable. Read-write. 1=Enable LCLK_DYN clock gating.
22	LclkGateFree. Read-write. IF (REG== D0F0xE4_x013[1:0]_8016) THEN BIOS: 1. ENDIF. 1=LCLK gating is controlled independent of TXCLK gating.
21:16	LclkDynGateLatency. Read-write. Specifies the number of clocks to wait before turning off LCLK_DYN.
5:0	CalibAckLatency. Read-write. Specifies the number of clocks after calibration is complete before the acknowledge signal is asserted.

D0F0xE4_x0130_802[4:1] Transmitter Lane Mux

Table 92: Lane index addresses for D0F0xE4_x0130_802[4:1]

D0F0xE0[31:4]	D0F0xE0[3:0]			
	4h	3h	2h	1h
0130_802h	Lanes[15:12]	Lanes[11:8]	Lanes[7:4]	Lanes[3:0]

Table 93: Reset Mapping for D0F0xE4_x0130_802[4:1]

Register	Reset
D0F0xE4_x0130_8024	0F0E_0D0Ch
D0F0xE4_x0130_8023	0B0A_0908h
D0F0xE4_x0130_8022	0706_0504h
D0F0xE4_x0130_8021	0302_0100h

Table 94: Field mapping for D0F0xE4_x0130_802[4:1]

Register	Bits			
	31:24	23:16	15:8	7:0
D0F0xE4_x0130_8024	TXLane15	TXLane14	TXLane13	TXLane12
D0F0xE4_x0130_8023	TXLane11	TXLane10	TXLane9	TXLane8
D0F0xE4_x0130_8022	TXLane7	TXLane6	TXLane5	TXLane4
D0F0xE4_x0130_8021	TXLane3	TXLane2	TXLane1	TXLane0

Bits	Description																																					
31:24	TXLane . Read-write. Specifies the controller lanes that are mapped to TX lane n of the PIF. See: D0F0xE4_x0130_802[4:1][7:0].																																					
23:16	TXLane . Read-write. Specifies the controller lanes that are mapped to TX lane n of the PIF. See: D0F0xE4_x0130_802[4:1][7:0].																																					
15:8	TXLane . Read-write. Specifies the controller lanes that are mapped to TX lane n of the PIF. See: D0F0xE4_x0130_802[4:1][7:0].																																					
7:0	TXLane . Read-write. Specifies the controller lanes that are mapped to TX lane n of the PIF.																																					
	<table border="1"> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Controller lane 0.</td> <td>8h</td> <td>Controller lane 8.</td> </tr> <tr> <td>1h</td> <td>Controller lane 1.</td> <td>9h</td> <td>Controller lane 9.</td> </tr> <tr> <td>2h</td> <td>Controller lane 2.</td> <td>10h</td> <td>Controller lane 10.</td> </tr> <tr> <td>3h</td> <td>Controller lane 3.</td> <td>11h</td> <td>Controller lane 11.</td> </tr> <tr> <td>4h</td> <td>Controller lane 4.</td> <td>12h</td> <td>Controller lane 12.</td> </tr> <tr> <td>5h</td> <td>Controller lane 5.</td> <td>13h</td> <td>Controller lane 13.</td> </tr> <tr> <td>6h</td> <td>Controller lane 6.</td> <td>14h</td> <td>Controller lane 14.</td> </tr> <tr> <td>7h</td> <td>Controller lane 7.</td> <td>15h</td> <td>Controller lane 15.</td> </tr> </tbody> </table>		Bits	Definition	Bits	Definition	0h	Controller lane 0.	8h	Controller lane 8.	1h	Controller lane 1.	9h	Controller lane 9.	2h	Controller lane 2.	10h	Controller lane 10.	3h	Controller lane 3.	11h	Controller lane 11.	4h	Controller lane 4.	12h	Controller lane 12.	5h	Controller lane 5.	13h	Controller lane 13.	6h	Controller lane 6.	14h	Controller lane 14.	7h	Controller lane 7.	15h	Controller lane 15.
Bits	Definition	Bits	Definition																																			
0h	Controller lane 0.	8h	Controller lane 8.																																			
1h	Controller lane 1.	9h	Controller lane 9.																																			
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3h	Controller lane 3.	11h	Controller lane 11.																																			
4h	Controller lane 4.	12h	Controller lane 12.																																			
5h	Controller lane 5.	13h	Controller lane 13.																																			
6h	Controller lane 6.	14h	Controller lane 14.																																			
7h	Controller lane 7.	15h	Controller lane 15.																																			

D0F0xE4_x0130_802[8:5] Receiver Lane Mux (LM_PCIERXMUX)

Reset: 0302_0100h.

Table 95: Lane index addresses for D0F0xE4_x0130_802[8:5]

D0F0xE0[31:4]	D0F0xE0[3:0]			
	8h	7h	6h	5h
0130_802h	Lanes[15:12]	Lanes[11:8]	Lanes[7:4]	Lanes[3:0]

Table 96: Reset Mapping for D0F0xE4_x0130_802[8:5]

Register	Reset
D0F0xE4_x0130_8028	0F0E_0D0Ch
D0F0xE4_x0130_8027	0B0A_0908h
D0F0xE4_x0130_8026	0706_0504h
D0F0xE4_x0130_8025	0302_0100h

Table 97: Field mapping for D0F0xE4_x0130_802[8:5]

Register	Bits			
	31:24	23:16	15:8	7:0
D0F0xE4_x0130_8028	RXLane15	RXLane14	RXLane13	RXLane12
D0F0xE4_x0130_8027	RXLane11	RXLane10	RXLane9	RXLane8
D0F0xE4_x0130_8026	RXLane7	RXLane6	RXLane5	RXLane4
D0F0xE4_x0130_8025	RXLane3	RXLane2	RXLane1	RXLane0

Bits	Description																																				
31:24	RXLane . Read-write. Specifies the PIF RX lanes that are mapped to controller lane n. See: D0F0xE4_x0130_802[8:5][7:0].																																				
23:16	RXLane . Read-write. Specifies the PIF RX lanes that are mapped to controller lane n. See: D0F0xE4_x0130_802[8:5][7:0].																																				
15:8	RXLane . Read-write. Specifies the PIF RX lanes that are mapped to controller lane n. See: D0F0xE4_x0130_802[8:5][7:0].																																				
7:0	RXLane . Read-write. Specifies the PIF RX lanes that are mapped to controller lane n. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>PIF RX lane 0.</td> <td>8h</td> <td>PIF RX lane 8.</td> </tr> <tr> <td>1h</td> <td>PIF RX lane 1.</td> <td>9h</td> <td>PIF RX lane 9.</td> </tr> <tr> <td>2h</td> <td>PIF RX lane 2.</td> <td>10h</td> <td>PIF RX lane 10.</td> </tr> <tr> <td>3h</td> <td>PIF RX lane 3.</td> <td>11h</td> <td>PIF RX lane 11.</td> </tr> <tr> <td>4h</td> <td>PIF RX lane 4.</td> <td>12h</td> <td>PIF RX lane 12.</td> </tr> <tr> <td>5h</td> <td>PIF RX lane 5.</td> <td>13h</td> <td>PIF RX lane 13.</td> </tr> <tr> <td>6h</td> <td>PIF RX lane 6.</td> <td>14h</td> <td>PIF RX lane 14.</td> </tr> <tr> <td>7h</td> <td>PIF RX lane 7.</td> <td>15h</td> <td>PIF RX lane 15.</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0h	PIF RX lane 0.	8h	PIF RX lane 8.	1h	PIF RX lane 1.	9h	PIF RX lane 9.	2h	PIF RX lane 2.	10h	PIF RX lane 10.	3h	PIF RX lane 3.	11h	PIF RX lane 11.	4h	PIF RX lane 4.	12h	PIF RX lane 12.	5h	PIF RX lane 5.	13h	PIF RX lane 13.	6h	PIF RX lane 6.	14h	PIF RX lane 14.	7h	PIF RX lane 7.	15h	PIF RX lane 15.
Bits	Definition	Bits	Definition																																		
0h	PIF RX lane 0.	8h	PIF RX lane 8.																																		
1h	PIF RX lane 1.	9h	PIF RX lane 9.																																		
2h	PIF RX lane 2.	10h	PIF RX lane 10.																																		
3h	PIF RX lane 3.	11h	PIF RX lane 11.																																		
4h	PIF RX lane 4.	12h	PIF RX lane 12.																																		
5h	PIF RX lane 5.	13h	PIF RX lane 13.																																		
6h	PIF RX lane 6.	14h	PIF RX lane 14.																																		
7h	PIF RX lane 7.	15h	PIF RX lane 15.																																		

D0F0xE4_x0130_8029 Lane Enable (LM_LANEENABLE)

Reset: 0000_FFFFh.

Bits	Description				
31:16	Reserved.				
15:0	LaneEnable. Read-write. 1=Lane enabled for transmit. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[15:0]</td> <td>Lane <BIT> enable</td> </tr> </tbody> </table>	Bit	Definition	[15:0]	Lane <BIT> enable
Bit	Definition				
[15:0]	Lane <BIT> enable				

D0F0xE4_x0130_8060 Soft Reset Command 0

Cold reset: 0000_0000h.

Bits	Description
17	Bif0CalibrationReset. Read-write. 1=The BIF 0 calibration block reset is asserted.
16	Bif0GlobalReset. Read-write. 1=The BIF 0 global reset is asserted.
3	WaitState. Read-only. 1=Reset cycle is in the wait state.
2	ResetComplete. Read-only; real-time-update. 1=Reset cycle is complete.
0	Reconfigure. Read-write; Cleared-when-done. 1=Trigger atomic reconfiguration if D0F0xE4_x0130_8062[ReconfigureEn]=1.

D0F0xE4_x0130_8062 Soft Reset Control 0

Cold reset: 0001_0880h.

Bits	Description
11	ConfigXferMode. Read-write. 1=PCIe core strap settings take effect immediately. 0=PCIe core strap settings take effect when the PCIe core is reset.
10	BlockOnIdle. Read-write. 1=The PCIe core must be idle before hardware initiates a reconfiguration. 0=The PCIe core does not have to be idle before hardware initiates a reconfiguration.
4:2	ResetPeriod. Read-write. BIOS:2h. Specifies the amount of time that resets are asserted during an atomic reset or reconfiguration. 5h-7h: Reserved.
0	ReconfigureEn. Read-write. 1=Atomic reconfiguration enabled.

D0F0xE4_x0130_80F0 BIOS Timer

Reset: 0000_0000h.

Bits	Description
31:0	MicroSeconds. Read-write; Updated-by-hardware; real-time-update. This field increments once every microsecond when the timer is enabled. The counter rolls over and continues counting when it reaches its FFFF_FFFFh. A write to this register causes the counter to reset and begin counting from the value written.

D0F0xE4_x0130_80F1 BIOS Timer Control

Reset: 0000_0064h.

Bits	Description
31:8	Reserved.
7:0	ClockRate . Read-write. Specifies the frequency of the reference clock in 1 MHz increments. <u>Bits</u> <u>Definition</u> 00h Timer disabled FFh-01h <ClockRate> MHz

3.3.4 IO Link Registers**D0F0xE4_x0140_0002 IO Link Hardware Debug**

Reset: 0000_0000h.

Bits	Description
0	HwDebug[0]: ignore DLLPs in L1 . Read-write. BIOS: 1. 1=DLLPs are ignored in L1 so the TXCLK can be turned off.

D0F0xE4_x0140_0010 IO Link Control 1

Reset: 80E3_110Bh.

Bits	Description
12:10	RxUmiAdjPayloadSize . Read-write. BIOS: 100b. Payload size for the UMI link. <u>Bits</u> <u>Definition</u> <u>Bits</u> <u>Definition</u> 00xb Reserved. 100b 64 bytes 010b 16 bytes 101b Reserved. 011b 32 bytes. 11xb Reserved.
9	UmiNpMemWrite: memory write mapping enable . Read-write. 1=Internal non-posted memory writes are transferred to UMI.
3:1	LcHotPlugDelSel: enhanced hot plug counter select . Read-write. <u>Bits</u> <u>Definition</u> <u>Bits</u> <u>Definition</u> 0h 15 ms 4h 150 ms 1h 20 ms 5h 200 ms 2h 50 ms 6h 275 ms 3h 100 ms 7h 335 ms
0	HwInitWrLock: hardware init write lock . Read-write. 1=Lock HWInit registers. 0=Unlock HWInit registers.

D0F0xE4_x0140_0011 IO Link Config Control

Reset: 0000_000Fh.

Bits	Description
3:0	DynClkLatency: dynamic clock latency. Read-write. BIOS: See 2.11.4.3.1 [Link Configuration and Core Initialization]. Specifies the number of clock cycles after logic goes idle before clocks are gated off.

D0F0xE4_x0140_001C IO Link Control 2 (PCIE_CNTL2)

Reset: 0E00_0109h.

Bits	Description
10:6	TxArbMstLimit: transmitter arbitration master limit. Read-write. BIOS: 4h. Defines together with TxArbSlvLimit a round robin arbitration pattern for downstream accesses. TxArbMstLimit defines the weight for downstream CPU requests and TxArbSlvLimit for the downstream read responses.
5:1	TxArbSlvLimit: transmitter arbitration slave limit. Read-write. BIOS: 4h. See TxArbMstLimit for details
0	TxArbRoundRobinEn: transmitter round robin arbitration enabled. Read-write. BIOS: 1. 1=Enable transmitter round robin arbitration. 0=Disable transmitter round robin arbitration.

D0F0xE4_x0140_0020 IO Link Chip Interface Control (PCIE_CI_CNTL)

Reset: 0000_0050h.

Bits	Description
9	CiRcOrderingDis: chip interface RC ordering disable. Read-write. 0=RC ordering logic is enabled. 1=RC ordering logic is disabled.

D0F0xE4_x0140_0040 IO Link Phy Control (PCIE_P_CNTL)

Reset: 0001_0000h.

Bits	Description										
15:14	PElecIdleMode: electrical idle mode for physical layer. Read-write. BIOS: 01b. Defines which electrical idle signal is used, either inferred by link controller or from phy. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Gen1 - entry:PHY, exit:PHY; Gen2 - entry:INF, exit:PHY.</td> </tr> <tr> <td>01b</td> <td>Gen1 - entry:INF, exit:PHY; Gen2 - entry:INF, exit:PHY.</td> </tr> <tr> <td>10b</td> <td>Gen1 - entry:PHY, exit:PHY; Gen2 - entry:PHY, exit:PHY.</td> </tr> <tr> <td>11b</td> <td>Gen1 - entry: PHY, exit: PHY; Gen2 - entry: PHY, exit: PHY.</td> </tr> </tbody> </table>	Bits	Definition	00b	Gen1 - entry:PHY, exit:PHY; Gen2 - entry:INF, exit:PHY.	01b	Gen1 - entry:INF, exit:PHY; Gen2 - entry:INF, exit:PHY.	10b	Gen1 - entry:PHY, exit:PHY; Gen2 - entry:PHY, exit:PHY.	11b	Gen1 - entry: PHY, exit: PHY; Gen2 - entry: PHY, exit: PHY.
Bits	Definition										
00b	Gen1 - entry:PHY, exit:PHY; Gen2 - entry:INF, exit:PHY.										
01b	Gen1 - entry:INF, exit:PHY; Gen2 - entry:INF, exit:PHY.										
10b	Gen1 - entry:PHY, exit:PHY; Gen2 - entry:PHY, exit:PHY.										
11b	Gen1 - entry: PHY, exit: PHY; Gen2 - entry: PHY, exit: PHY.										

D0F0xE4_x0140_00B0 IO Link Strap Control (PCIE_STRAP_F0)

Reset: 0000_8001h.

Bits	Description
5	StrapF0AerEn. Read-write. 1=AER support enabled. 0=AER support disabled.
2	StrapF0MsiEn. Read-write. BIOS: 1. Overrides MSI enable.

D0F0xE4_x0140_00C0 IO Link Strap Miscellaneous (PCIE_STRAP_MISC)

Bits	Description
30	StrapFlrEn. Read-write. Reset:0.
29	StrapMstAddr64En. Read-write. Reset: 0.
28	StrapReverseAll. Read-write. Reset: 0.

D0F0xE4_x0140_00C1 IO Link Strap Miscellaneous2 (PCIE_STRAP_MISC2)

Bits	Description
1	StrapGen2Compliance. Read-write. Reset: 0.
0	StrapLinkBwNotificationCapEn. Read-write. Reset: 0.

D0F0xF8 Northbridge IOAPIC Index

Reset: 0000_0000h. The index/data pair registers, [D0F0xF8](#) and [D0F0xFC](#), are used to access the registers at [D0F0xFC_x\[FF:00\]](#). To access any of these registers, the address is first written into the index register, [D0F0xF8](#), and then the data is read from or written to the data register, [D0F0xFC](#).

Bits	Description
31:8	Reserved.
7:0	IOAPICIndAddr: IOAPIC index register address. Read-write.

D0F0xFC Northbridge IOAPIC Data

Reset: 0000_0000h. See [D0F0xF8](#). Address: [D0F0xF8\[IOAPICIndAddr\]](#).

Bits	Description
31:0	IOAPICIndData: IOAPIC index data register. Read-write.

D0F0xFC_x00 IOAPIC Feature Control Register

Reset: 0000_0004h.

Bits	Description
31:5	Reserved.

4	IoapicSbFeatureEn. Read-write. 1=Enable masked interrupts to be routed back to the FCH PIC/IOAPIC.
3	Reserved.
2	IoapicIdExtEn. Read-write. Extend the IOAPIC ID from 4-bit to 8-bit. 0=4-bit ID. 1=8-bit ID.
1	Reserved.
0	IoapicEnable. Read-write. 1=Enables the INTGEN block to decode IOAPIC addresses. BIOS: 1. BIOS should always set this bit after programming the IOAPIC BAR in the init sequence.

D0F0xFC_x01 IOAPIC Base Address LowerReset: FEC0_0000h. See [3.16 \[Northbridge IOAPIC Registers\]](#).

Bits	Description
31:8	IoapicAddr. Read-write. IOAPIC Base Address bits [31:8].
7:0	Reserved.

D0F0xFC_x02 IOAPIC Base Address UpperReset: 0000_0000h. See [3.16 \[Northbridge IOAPIC Registers\]](#).

Bits	Description
31:0	IoapicAddrUpper. Read-write. IOAPIC Base Address bits [63:32].

D0F0xFC_x0F IOAPIC GBIF Interrupt Routing Register

Reset: 0000_0000h.

Bits	Description										
31:6	Reserved.										
5:4	GBIFExtIntrSwz. Read-write. Swizzle GBIF INTA/B/C/D based on the value in this field before mapping them onto the IOAPIC pins. <table style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Interrupt Swizzling</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>ABCD</td> </tr> <tr> <td>01b</td> <td>BCDA</td> </tr> <tr> <td>10b</td> <td>CDAB</td> </tr> <tr> <td>11b</td> <td>DABC</td> </tr> </tbody> </table>	Bits	Interrupt Swizzling	00b	ABCD	01b	BCDA	10b	CDAB	11b	DABC
Bits	Interrupt Swizzling										
00b	ABCD										
01b	BCDA										
10b	CDAB										
11b	DABC										
3	Reserved.										
2:0	GBIFExtIntrGrp. Read-write. Map GBIF INTA/B/C/D to IOAPIC pins [((grp+1)*4)-1:(grp*4)]. For GBIF, only INTA/B are used. INTC/D should be tied off.										

D0F0xFC_x1[4:0] IOAPIC BR Interrupt Routing Register

Reset: 0000_0000h.

Bits	Description
31:21	Reserved.
20:16	BrIntIntrMap. Read-write. Map bridge n interrupts to IOAPIC redirection table entry.

15:6	Reserved.										
5:4	BrExtIntrSwz. Read-write. Swizzle bridge n external INTA/B/C/D based on the value in this field before mapping them onto the IOAPIC pins. <table> <thead> <tr> <th>Bits</th> <th>Interrupt Swizzling</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>ABCD</td> </tr> <tr> <td>01b</td> <td>BCDA</td> </tr> <tr> <td>10b</td> <td>CDAB</td> </tr> <tr> <td>11b</td> <td>DABC</td> </tr> </tbody> </table>	Bits	Interrupt Swizzling	00b	ABCD	01b	BCDA	10b	CDAB	11b	DABC
Bits	Interrupt Swizzling										
00b	ABCD										
01b	BCDA										
10b	CDAB										
11b	DABC										
3	Reserved.										
2:0	BrExtIntrGrp. Read-write. Map bridge n external INTA/B/C/D to IOAPIC pins [((grp+1)*4)-1:(grp*4)].										

D0F0xFC_x30 IOAPIC Serial IRQ Status

Reset: 0000_0000h.

Bits	Description
31:0	InternalIrqSts. Read-only. Shows the status of the 32 IOAPIC interrupt pins.

D0F0xFC_x3[F:E] IOAPIC Scratch [1:0] Register

Reset: 0000_0000h.

Bits	Description
31:0	Scratch. Read-write.

3.4 Device 0 Function 2 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space]. See 2.11.6 [PCIe Client Interface Control].

D0F2xF8 PCIe Client Interface Index

The index/data pair registers, [D0F2xF8](#) and [D0F2xFC](#) are used to access the registers at [D0F2xFC_x\[FFFF:0000\]_L1i\[3:0\]](#). To access any of these registers, the address is first written into the index register, [D0F2xF8](#), and then the data is read from or written to the data register, [D0F2xFC](#).

Registers in the L1 indexed space have one instance per L1 denoted by [_L1i\[x\]](#) where [x=D0F2xF8\[L1cfgSel\]](#). The syntax for this register type is described by example as follows:

- [D0F2xFC_x32](#) refers to all instances of the [D0F2xFC_x32_L1i](#) registers.
- [D0F2xFC_x32_L1i_L1i\[1\]](#) refers to the [D0F2xFC_x32](#) register instance for the BIF L1.

Bits	Description										
31	L1cfgEn. Read-write. Reset: 0. 1=Enable writes to D0F2xFC .										
30:20	Reserved.										
19:16	L1cfgSel. Read-write. Reset: 0. This field selects one of the four L1s to access. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>PPD L1</td> </tr> <tr> <td>1h</td> <td>BIF L1</td> </tr> <tr> <td>2h</td> <td>INTGEN L1</td> </tr> <tr> <td>Fh-3h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	0h	PPD L1	1h	BIF L1	2h	INTGEN L1	Fh-3h	Reserved
Bits	Description										
0h	PPD L1										
1h	BIF L1										
2h	INTGEN L1										
Fh-3h	Reserved										
15:0	L1cfgIndex. Read-write. Reset: 0.										

D0F2xFC PCIe Client Interface Data

IF ([D0F2xF8\[L1cfgEn\]](#)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0000_0000h. See [D0F2xF8](#). Address: [D0F2xF8\[L1cfgIndex\]](#).

Bits	Description
31:0	L1cfgData.

D0F2xFC_x32_L1i L1_CNTRL_4

Bits	Description
31:20	Reserved.
19:17	Reserved.
16	DmaNpHaltDis. Read-write. Reset: 0.
15:10	DmaBufMaxNpCred. Read-write. Reset: Fh.
9:4	DmaBufCredits. Read-write. Reset: 10h.
3	Reserved.

2	Reserved.
1	Reserved.
0	Reserved.

D0F2xFC_x33_L1i L1_CLKCNTRL_0

Bits	Description
31	L1L2ClkgateEn. Read-write. Reset: 0. BIOS: 1.
30:12	Reserved.
11	L1HostreqClkgateEn. Read-write. Reset: 0. BIOS: 1.
10	L1RegClkgateEn. Read-write. Reset: 0. BIOS: 1.
9	L1MemoryClkgateEn. Read-write. Reset: 0. BIOS: 1.
8	L1PerfClkgateEn. Read-write. Reset: 0. BIOS: 1.
7	L1DmaInputClkgateEn. Read-write. Reset: 0. BIOS: 1.
6	L1CpslvClkgateEn. Read-write. Reset: 0. BIOS: 1.
5	L1CacheClkgateEn. Read-write. Reset: 0. BIOS: 1.
4	L1DmaClkgateEn. Read-write. Reset: 0. BIOS: 1.
3:2	Reserved.
1:0	L1ClkgateLen. Read-write. Reset: 0.

3.5 Device 1 Function 0 (Internal Graphics) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D1F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: Fuse[DEVICE_ID]. See: D0F0xD4_x0130_14AA[StrapBifF0DeviceId].
15:0	VendorID: vendor ID. Read-only. Value: IF (Fuse[StrapBifVendorId] == 0) THEN 1002h ELSE 1022h ENDIF.

D1F0x04 Status/Command Register

Reset: 0010_0000h.

Bits	Description
31	ParityErrorDetected: detected parity error. Read; Write-1-to-clear. 1=Poisoned TLP received.
30	SignaledSystemError: signaled system error. Read; Write-1-to-clear. 1=A non-fatal or fatal error message was sent and SerrEn=1.
29	ReceivedMasterAbort: received master abort. Read; Write-1-to-clear. 1=A completion with an unsupported request completion status was received.
28	ReceivedTargetAbort: received target abort. Read; Write-1-to-clear. 1=A completion with completer abort completion status was received.
27	SignalTargetAbort: Signaled target abort. Read-only.
26:25	DevSelTiming: DEVSEL# Timing. Read-only.
24	MasterDataPerr: master data parity error. Read; Write-1-to-clear. 1=ParityErrorEn=1 and either a poisoned completion was received or the device poisoned a write request.
23	FastBackCapable: fast back-to-back capable. Read-only.
22	UDFEn: UDF enable. Read-only.
21	PCI66En: 66 MHz capable. Read-only.
20	CapList: capability list. Read-only. 1=Capability list supported.
19	IntStatus: interrupt status. Read-only. 1=INTx interrupt message pending.
18:11	Reserved.
10	IntDis: interrupt disable. Read-write. 1=INTx interrupt messages generation disabled.
9	FastB2BEn: fast back-to-back enable. Read-only.
8	SerrEn: System error enable. Read-write. 1=Enables reporting of non-fatal and fatal errors detected.
7	Stepping: Stepping control. Read-only.
6	ParityErrorEn: parity error response enable. Read-write.
5	PalSnoopEn: VGA palette snoop enable. Read-only.
4	MemWriteInvalidateEn: memory write and invalidate enable. Read-only.

3	SpecialCycleEn: special cycle enable. Read-only.
2	BusMasterEn: bus master enable. Read-write. 1=Memory and IO read and write request generation enabled.
1	MemAccessEn: IO access enable. Read-write. This bit controls if memory accesses targeting this device are accepted. 1=Enabled. 0=Disabled.
0	IoAccessEn: IO access enable. Read-write. This bit controls if IO accesses targeting this device are accepted. 1=Enabled. 0=Disabled.

D1F0x08 Class Code/Revision ID Register

Bits	Description
31:8	ClassCode. Value: IF (D0F0xD4_x0130_14B6 [StrapBifVgaDis]==0) THEN 03_0000h. ELSE 03_8000h. ENDIF.
7:0	RevID: revision ID. Value: {Fuse[MajorRevId], Fuse[MinorRevId]}.

D1F0x0C Header Type Register

Reset: 0080_0000h.

Bits	Description
31:24	BIST. Read-only.
23:16	HeaderTypeReg. Read-only. The header type field indicates a header type 0 and that this is a multi-function device.
15:8	LatencyTimer. Read-only. These bits are fixed at their default value.
7:0	CacheLineSize. Read-write. This field specifies the system cache line size in units of double words.

D1F0x10 Graphic Memory Base AddressIF ([D0F0xD4_x0109_14E2](#)[StrapBifF064BarDisA]==1) THEN Reset: 0000_0008h. ELSE Reset: 0000_000Ch. ENDIF.

Bits	Description										
31:26	BaseAddr[31:26]: base address. Read-write. The amount of memory requested by the graphics memory BAR is controlled by D0F0xD4_x0109_1507 [StrapBifMemApSizePin] and D0F0xD4_x0109_14E1 [StrapBifMemApSize].										
25:4	BaseAddr[25:4]: base address. Read-only.										
3	Pref: prefetchable. Read-only. 1=Prefetchable memory region.										
2:1	Type: base address register type. Read-only. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>32-bit BAR</td> </tr> <tr> <td>01b</td> <td>Reserved</td> </tr> <tr> <td>10b</td> <td>64-bit BAR</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	32-bit BAR	01b	Reserved	10b	64-bit BAR	11b	Reserved
Bits	Description										
00b	32-bit BAR										
01b	Reserved										
10b	64-bit BAR										
11b	Reserved										
0	MemSpace: memory space type. Read-only. 0=Memory mapped base address.										

D1F0x14 Graphics Memory Base Address 64

Reset: 0000_0000h.

Bits	Description
31:0	BaseAddr[63:32]: base address. Read-write. This field is reserved if (D0F0xD4_x0109_14E2[StrapBifF064BarDisA]==1).

D1F0x18 Graphics Doorbell Base Address

IF ([D0F0xD4_x0109_14E2\[StrapBifF064BarDisA\]==1](#)) THEN Reset: 0000_0008h. ELSE Reset: 0000_000Ch. ENDIF. This register is reserved and reset is 0000_0000h if ([D0F0xD4_x0109_14E1\[StrapBifDoorbellBarDis\]==1](#)).

Bits	Description										
31:23	BaseAddr[31:23]: base address. Read-write.										
22:4	BaseAddr[22:4]: base address. Read-only.										
3	Pref: prefetchable. Read-only. 1=Prefetchable memory region.										
2:1	Type: base address register type. Read-only. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>32-bit BAR</td> </tr> <tr> <td>01b</td> <td>Reserved</td> </tr> <tr> <td>10b</td> <td>64-bit BAR</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	32-bit BAR	01b	Reserved	10b	64-bit BAR	11b	Reserved
Bits	Description										
00b	32-bit BAR										
01b	Reserved										
10b	64-bit BAR										
11b	Reserved										
0	MemSpace: memory space type. Read-only. 0=Memory mapped base address.										

D1F0x1C Graphics Doorbell Base Address 64

Reset: 0000_0000h.

Bits	Description
31:0	BaseAddr[63:32]: base address. Read-write. This field is reserved if (D0F0xD4_x0109_14E1[StrapBifDoorbellBarDis]==1 D0F0xD4_x0109_14E2[StrapBifF064BarDisA]==1).

D1F0x20 Graphics IO Base Address

Reset: 0000_0000h. This register is called Base Address 4 if ([D0F0xD4_x0109_14E2\[StrapBifF064BarDisA\]==1](#)).

Bits	Description
31:0	Reserved.

D1F0x24 Graphics Memory Mapped Registers Base Address

Reset: 0000_0000h.

Bits	Description
31:16	BaseAddr[31:16]: base address. Read-write. The amount of memory requested by the graphics memory mapped registers BAR is controlled by D0F0xD4_x0109_14E1[StrapBifRegApSize] .
15:4	BaseAddr[15:4]: base address. Read-only.
3	Pref: prefetchable. Read-only. 0=Non-prefetchable memory region.
2:1	Type: base address register type. Read-only. 00b=32-bit BAR.
0	MemSpace: memory space type. Read-only. 0=Memory mapped base address.

D1F0x2C Subsystem and Subvendor ID RegisterReset: 0000_0000h. This register can be modified through [D1F0x4C](#).

Bits	Description
31:16	SubsystemID. Read-only.
15:0	SubsystemVendorID. Read-only.

D1F0x30 Expansion ROM Base Address

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F0x34 Capabilities Pointer

Reset: 0000_0050h.

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Pointer to PM capability.

D1F0x3C Interrupt Line

Reset: 0000_01FFh.

Bits	Description
31:16	Reserved.
15:8	InterruptPin: interrupt pin. Read-only. This field identifies the legacy interrupt message the function uses.
7:0	InterruptLine: interrupt line. Read-write. This field contains the interrupt line routing information.

D1F0x4C Subsystem and Subvendor ID Mirror

Reset: 0000_0000h.

Bits	Description
31:16	SubsystemID. Read-write. This field sets the value in the corresponding field in D1F0x2C .
15:0	SubsystemVendorID. Read-write. This field sets the value in the corresponding field in D1F0x2C .

D1F0x50 Power Management Capability

Bits	Description
31:27	PmeSupport. Value: 0_0000b. Indicates that there is no PME support.
26	D2Support: D2 support. Value: 1. D2 is supported
25	D1Support: D1 support. Value: 1. D1 is supported
24:22	AuxCurrent: auxiliary current. Value: 0.
21	DevSpecificInit: device specific initialization. Value: 0. Indicates that there is no device specific initialization necessary.
20	Reserved.
19	PmeClock. Value: 0.
18:16	Version: version. Value: 011b.
15:8	NextPtr: next pointer. Value: 58h
7:0	CapID: capability ID. Value: 01h. Indicates that the capability structure is a PCI power management data structure.

D1F0x54 Power Management Control and Status

Reset: 0000_0000h.

Bits	Description
31:24	PmeData. Read-only.
23	BusPwrEn. Read-only.
22	B2B3Support. Read-only. B states are not supported.
21:16	Reserved.
15	PmeStatus: PME status. Read-only.
14:13	DataScale: data scale. Read-only.
12:9	DataSelect: data select. Read-only.
8	PmeEn: PME# enable. Read-only.
7:4	Reserved.
3	NoSoftReset: no soft reset. Read-only. Software is required to re-initialize the function when returning from D3hot.

2	Reserved.						
1:0	PowerState: power state. Read-write. This 2-bit field is used both to determine the current power state of the root port and to set the root port into a new power state. <table style="margin-left: 20px;"> <tr> <td><u>Bits</u></td> <td><u>Definition</u></td> </tr> <tr> <td>00b</td> <td>D0</td> </tr> <tr> <td>11b</td> <td>D3hot</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	00b	D0	11b	D3hot
<u>Bits</u>	<u>Definition</u>						
00b	D0						
11b	D3hot						

D1F0x58 PCI Express Capability

Bits	Description
31:30	Reserved.
29:25	IntMessageNum: interrupt message number. Value: 0. This field indicates which MSI vector is used for the interrupt message.
24	SlotImplemented: Slot implemented. Value: 0.
23:20	DeviceType: device type. Value: 9h.
19:16	Version. Value: 2h.
15:8	NextPtr: next pointer. Value: IF (D0F0xD4_x0130_14BE[StrapBifMsiDis]==0) THEN A0h. ELSE 00h. ENDIF.
7:0	CapID: capability ID. Value: 10h.

D1F0x5C Device Capability

Bits	Description
31:29	Reserved.
28	FlrCapable: function level reset capability. Value: 0.
27:26	CapturedSlotPowerScale: captured slot power limit scale. Value: 0.
25:18	CapturedSlotPowerLimit: captured slot power limit value. Value: 0.
17:16	Reserved.
15	RoleBasedErrReporting: role-based error reporting. Value: 1.
14:12	Reserved.
11:9	L1AcceptableLatency: endpoint L1 Acceptable Latency. Value: 111b.
8:6	L0SAcceptableLatency: endpoint L0s Acceptable Latency. Value: 110b.
5	ExtendedTag: extended tag support. Value: 1. 8 bit tag support.
4:3	PhantomFunc: phantom function support. Value: 0. No phantom functions supported.
2:0	MaxPayloadSupport: maximum supported payload size. Value: 000b. 128 bytes max payload size.

D1F0x60 Device Control and Status

Reset: 0000_0810h.

Bits	Description
31:22	Reserved.
21	TransactionsPending: transactions pending. Read-only.
20	AuxPwr: auxiliary power. Read-only.
19	UsrDetected: unsupported request detected. Read; Write-1-to-clear. 1=Unsupported request received.
18	FatalErr: fatal error detected. Read; Write-1-to-clear. 1=Fatal error detected.
17	NonFatalErr: non-fatal error detected. Read; Write-1-to-clear. 1=Non-fatal error detected.
16	CorrErr: correctable error detected. Read; Write-1-to-clear. 1=Correctable error detected.
15	BridgeCfgRetryEn: bridge configuration retry enable. Read-only.
14:12	MaxRequestSize: maximum request size. Read-only.
11	NoSnoopEnable: enable no snoop. Read-write. 1=The device is permitted to set the No Snoop bit in requests.
10	AuxPowerPmEn: auxiliary power PM enable. Read-only. This capability is not implemented.
9	PhantomFuncEn: phantom functions enable. Read-only. Phantom functions are not supported.
8	ExtendedTagEn: extended tag enable. Read-write. 1=8-bit tag request tags. 0=5-bit request tag.
7:5	MaxPayloadSize: maximum supported payload size. Read-only. 000b=Indicates a 128 byte maximum payload size.
4	RelaxedOrdEn: relaxed ordering enable. Read-write. 1=The device is permitted to set the Relaxed Ordering bit.
3	UsrReportEn: unsupported request reporting enable. Read-write. 1=Enables signaling unsupported requests by sending error messages.
2	FatalErrEn: fatal error reporting enable. Read-write. 1=Enables sending ERR_FATAL message when a fatal error is detected.
1	NonFatalErrEn: non-fatal error reporting enable. Read-write. 1=Enables sending ERR_NONFATAL message when a non-fatal error is detected.
0	CorrErrEn: correctable error reporting enable. Read-write. 1=Enables sending ERR_CORR message when a correctable error is detected.

D1F0x64 Link Capability

Bits	Description
31:24	PortNumber: port number. Read-only. Value: 0.This field indicates the PCI Express port number for the given PCI Express link.
23	Reserved.
22	AspmOptionalityCompliance: ASP Optionality ECN capability. Read-only. Value: 0b.
21	LinkBWNotificationCap: link bandwidth notification capability. Read-only. Value: 0b.
20	DLActiveReportingCapable: data link layer active reporting capability. Read-only. Value: 0b.

19	SurpriseDownErrReporting: surprise down error reporting capability. Read-only. Value: 0b.
18	ClockPowerManagement: clock power management. Read-only. Value: 0b.
17:15	L1ExitLatency: L1 exit latency. Read-only. Value: 0b.
14:12	L0sExitLatency: L0s exit latency. Read-only. Value: 0b.
11:10	PMSupport: active state power management support. Read-only. Value: 0b.
9:4	LinkWidth: maximum link width. Read-only. Value: 0.
3:0	LinkSpeed: link speed. Read-only. Value: 0b.

D1F0x68 Link Control and Status

Reset: 0000_0000h.

Bits	Description
31	LinkAutonomousBWStatus: link autonomous bandwidth status. Read-only.
30	LinkBWManagementStatus: link bandwidth management status. Read-only.
29	DLActive: data link layer link active. Read-only. This bit indicates the status of the data link control and management state machine. Reads return a 1 to indicate the DL_Active state, otherwise 0 is returned.
28	SlotClockCfg: slot clock configuration. Read-only. 1=the root port uses the same clock that the platform provides.
27	LinkTraining: link training. Read-only. 1=Indicates that the physical layer link training state machine is in the configuration or recovery state, or that 1b was written to the RetrainLink bit but link training has not yet begun. Hardware clears this bit when the link training state machine exits the configuration/recovery state.
26	Reserved.
25:20	NegotiatedLinkWidth: negotiated link width. Read-only. This field indicates the negotiated width of the given PCI Express link.
19:16	LinkSpeed: link speed. Read-only.
15:12	Reserved.
11	LinkAutonomousBWIntEn: link autonomous bandwidth interrupt enable. Read-only.
10	LinkBWManagementEn: link bandwidth management interrupt enable. Read-only.
9	HWAutonomousWidthDisable: hardware autonomous width disable. Read-only. 1=Hardware not allowed to change the link width except to correct unreliable link operation by reducing link width.
8	ClockPowerManagementEn: clock power management enable. Read-only.
7	ExtendedSync: extended sync. Read-only. 1=Forces the transmission of additional ordered sets when exiting the L0s state and when in the recovery state.
6	CommonClockCfg: common clock configuration. Read-only. 1=Indicates that the root port and the component at the opposite end of this Link are operating with a distributed common reference clock. 0=Indicates that the upstream port and the component at the opposite end of this Link are operating with asynchronous reference clock.
5	RetrainLink: retrain link. Read-only. This bit does not apply to endpoints.
4	LinkDis: link disable. Read-only. This bit does not apply to endpoints.
3	ReadCplBoundary: read completion boundary. Read-only. 0=64 byte read completion boundary.

2	Reserved.												
1:0	PmControl: active state power management enable. Read-only. This field controls the level of ASPM supported on the given PCI Express link. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disabled.</td> <td>10b</td> <td>L1 Entry Enabled.</td> </tr> <tr> <td>01b</td> <td>L0s Entry Enabled.</td> <td>11b</td> <td>L0s and L1 Entry Enabled.</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Disabled.	10b	L1 Entry Enabled.	01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.
Bits	Definition	Bits	Definition										
00b	Disabled.	10b	L1 Entry Enabled.										
01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.										

D1F0x7C Device Capability 2

Reset: 0000_0000h.

Bits	Description												
31:24	Reserved.												
23:22	MaxEndEndTlpPrefixes: Max number of End-End TLP prefixes supported. Read-only. IF (D1F0x7C[EndEndTlpPrefixSupported]==0) THEN Reserved. ENDIF. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>4 End-End TLP Prefixes.</td> <td>10b</td> <td>2 End-End TLP Prefixes.</td> </tr> <tr> <td>01b</td> <td>1 End-End TLP Prefix.</td> <td>11b</td> <td>3 End-End TLP Prefixes.</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	4 End-End TLP Prefixes.	10b	2 End-End TLP Prefixes.	01b	1 End-End TLP Prefix.	11b	3 End-End TLP Prefixes.
Bits	Definition	Bits	Definition										
00b	4 End-End TLP Prefixes.	10b	2 End-End TLP Prefixes.										
01b	1 End-End TLP Prefix.	11b	3 End-End TLP Prefixes.										
21	EndEndTlpPrefixSupported: End-End TLP Prefix supported. Read-only.												
20	ExtendedFmtFieldSupported. Read-only. 1=Function supports 3-bit definition of Fmt field. 0=Function supports 2-bit definition of Fmt field.												
19:18	ObffSupported: Optimized buffer flush/fill supported. Read-only.												
17:14	Reserved.												
13:12	TphCplrSupported. Read-only.												
11	LtrSupported: Latency Tolerance Reporting supported. Read-only.												
10	NoRoEnabledP2pPassing. Read-only.												
9:6	Reserved.												
5	AriForwardingSupported: ARI forwarding supported. Read-only.												
4	CplTimeoutDisSupported: completion timeout disable supported. Read-only.												
3:0	CplTimeoutRangeSupported: completion timeout range supported. Read-only.												

D1F0x80 Device Control and Status 2

Reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15	EndEndTlpPrefixBlocking. Read-only.
14:13	ObffEn. Read-only.
12:11	Reserved.
10	LtrEn. Read-only.
9	IdoCompletionEn. Read-only.
8	IdoRequestEn. Read-only.
7:6	Reserved.

5	AriForwardingEn. Read-only.
4	CplTimeoutDis: completion timeout disable. Read-only.
3:0	CplTimeoutValue: completion timeout range supported. Read-only.

D1F0x84 Link Capability 2

Bits	Description
31:9	Reserved.
8	CrosslinkSupported: Crosslink Supported. Read-only. Reset: 0. 1=Crosslink supported.
7:1	SupportedLinkSpeed: Supported Link Speed. Read-only. Reset: 07h. Specifies what link speeds are supported. Bit 1 = 2.5 GT/s, Bit2 = 5.0 Gt/s, Bit 3 = 8.0 GT/s.
0	Reserved.

D1F0x88 Link Control and Status 2

Reset: 0000_0000h.

Bits	Description
31:22	Reserved.
21	LinkEqualizationRequest. Read-only. Set when hardware requests link equalization to be performed.
20	EqualizationPhase3Success: Phase3 of Tx equalization procedure completed. Read-only.
19	EqualizationPhase2Success: Phase2 of Tx equalization procedure completed. Read-only.
18	EqualizationPhase1Success: Phase1 of Tx equalization procedure completed. Read-only.
17	EqualizationComplete: Tx equalization procedure completed. Read-only.
16	CurDeemphasisLevel: current deemphasis level. Read-only. 1=-3.5 dB. 0=-6 dB.
15:13	Reserved.
12	ComplianceDeemphasis: compliance deemphasis. Read-only. This bit defines the deemphasis level used in compliance mode. 1=-3.5 dB. 0=-6 dB.
11	ComplianceSOS: compliance SOS. Read-only. 1=The device transmits skip ordered sets in between the modified compliance pattern.
10	EnterModCompliance: enter modified compliance. Read-only. 1=The device transmits modified compliance pattern.
9:7	XmitMargin: transmit margin. Read-only. This field controls the non-deemphasized voltage level at the transmitter pins.
6	SelectableDeemphasis: selectable deemphasis. Read-only.
5	HwAutonomousSpeedDisable: hardware autonomous speed disable. Read-only. 1=Disables hardware generated link speed changes.
4	EnterCompliance: enter compliance. Read-only. 1=Force link to enter compliance mode.
3:0	TargetLinkSpeed: target link speed. Read-only. This field defines the upper limit of the link operational speed.

D1F0xA0 MSI Capability

Bits	Description
31:24	Reserved.
23	Msi64bit: MSI 64 bit capability. Read-only. Reset: 1. 1=The device is capable of sending 64-bit MSI messages. 0=The device is not capable of sending a 64-bit message address.
22:20	MsiMultiEn: MSI multiple message enable. Read-write. Reset: 000b. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). When MSI is enabled, a function is allocated at least 1 vector.
19:17	MsiMultiCap: MSI multiple message capability. Read-only. Reset: 000b. 000b=The device is requesting one vector.
16	MsiEn: MSI enable. Read-write. Reset: 0. 1=MSI generation is enabled and INTx generation is disabled. 0=MSI generation disabled and INTx generation is enabled.
15:8	NextPtr: next pointer. Read-only. Reset: 00h
7:0	CapID: capability ID. Read-only. Reset: 05h. 05h=MSI capability structure.

D1F0xA4 MSI Message Address Low

Reset: 0000_0000h.

Bits	Description
31:2	MsiMsgAddrLo: MSI message address. Read-write. This register specifies the dword aligned address for the MSI memory write transaction.
1:0	Reserved.

D1F0xA8 MSI Message Address High

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	MsiMsgAddrHi: MSI message address. Read-write. This register specifies the upper 8-bits of the MSI address in 64 bit MSI mode.

D1F0xAC MSI Message Data

Reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15:0	MsiData: MSI message data. Read-write. This register specifies lower 16 bits of data for the MSI memory write transaction. The upper 16 bits are always 0.

D1F0x100 Vendor Specific Enhanced Capability

Reset: 0061_000Bh.

Bits	Description
31:20	NextPtr: next pointer. Read-only.
19:16	CapVer: capability version. Read-only.
15:0	CapID: capability ID. Read-only.

D1F0x104 Vendor Specific Header

Reset: 0101_0001h.

Bits	Description
31:20	VsecLen: vendor specific enhanced next pointer. Read-only.
19:16	VsecRev: vendor specific enhanced capability version. Read-only.
15:0	VsecID: vendor specific enhanced capability ID. Read-only.

D1F0x108 Vendor Specific 1

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write.

D1F0x10C Vendor Specific 2

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write.

3.6 Device 1 Function 1 (Audio Controller) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D1F1x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: Fuse[STRAP_AZALIA_DID].
15:0	VendorID: vendor ID. Read-only. Value: IF (Fuse[StrapBifVendorId] == 0) THEN 1002h ELSE 1022h ENDIF.

D1F1x04 Status/Command

Reset: 0010_0000h.

Bits	Description
31	ParityErrorDetected: detected parity error. Read; Write-1-to-clear. 1=Poisoned TLP received.
30	SignaledSystemError: signaled system error. Read; Write-1-to-clear. 1=A non-fatal or fatal error message was sent and SerrEn=1.
29	ReceivedMasterAbort: received master abort. Read; Write-1-to-clear. 1=A completion with an unsupported request completion status was received.
28	ReceivedTargetAbort: received target abort. Read; Write-1-to-clear. 1=A completion with completer abort completion status was received.
27	SignalTargetAbort: Signaled target abort. Read-only.
26:25	DevselTiming: DEVSEL# Timing. Read-only.
24	MasterDataPerr: master data parity error. Read; Write-1-to-clear. 1=ParityErrorEn=1 and either a poisoned completion was received or the device poisoned a write request.
23	FastBackCapable: fast back-to-back capable. Read-only.
22	UDFEn: UDF enable. Read-only.
21	PCI66En: 66 MHz capable. Read-only.
20	CapList: capability list. Read-only. 1=capability list supported.
19	IntStatus: interrupt status. Read-only. 1=INTx interrupt message pending.
18:11	Reserved.
10	IntDis: interrupt disable. Read-write. 1=INTx interrupt messages generation disabled.
9	FastB2BEn: fast back-to-back enable. Read-only.
8	SerrEn: System error enable. Read-write. 1=Enables reporting of non-fatal and fatal errors detected.
7	Stepping: Stepping control. Read-only.
6	ParityErrorEn: parity error response enable. Read-write.

5	PalSnoopEn: VGA palette snoop enable. Read-only.
4	MemWriteInvalidateEn: memory write and invalidate enable. Read-only.
3	SpecialCycleEn: special cycle enable. Read-only.
2	BusMasterEn: bus master enable. Read-write. 1=Memory and IO read and write request generation enabled.
1	MemAccessEn: IO access enable. Read-write. This bit controls if memory accesses targeting this device are accepted. 1=Enabled. 0=Disabled.
0	IoAccessEn: IO access enable. Read-write. This bit controls if IO accesses targeting this device are accepted. 1=Enabled. 0=Disabled.

D1F1x08 Class Code/Revision ID

Reset: 0403_0000h.

Bits	Description
31:8	ClassCode. Read-only.
7:0	RevID: revision ID. Read-only.

D1F1x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:24	BIST. Read-only. These bits are fixed at their default values.
23:16	HeaderTypeReg. Read-only. 80h=Type 0 multi-function device.
15:8	LatencyTimer. Read-only. These bits are fixed at their default value.
7:0	CacheLineSize. Read-write. This field specifies the system cache line size in units of double words.

D1F1x10 Audio Registers Base Address

Reset: 0000_0000h.

Bits	Description
31:14	BaseAddr: base address. Read-write.
13:4	Reserved.
3	Pref: prefetchable. Read-only. 0=Non-prefetchable memory region.
2:1	Type: base address register type. Read-only. 00b=32-bit base address register.
0	MemSpace: memory space type. Read-only. 0=Memory mapped base address.

D1F1x14 Base Address 1

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x18 Base Address 2

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x1C Base Address 3

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x20 Base Address 4

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x24 Base Address 5

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x2C Subsystem and Subvendor IDReset: 0000_0000h. This register can be modified through [D1F1x4C](#).

Bits	Description
31:16	SubsystemID . Read-only.
15:0	SubsystemVendorID . Read-only.

D1F1x30 Expansion ROM Base Address

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D1F1x34 Capabilities Pointer

Reset: 0000_0050h.

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Pointer to PM capability.

D1F1x3C Interrupt Line

Reset: 0000_02FFh.

Bits	Description
31:16	Reserved.
15:8	InterruptPin: interrupt pin. Read-only. This field identifies the legacy interrupt message the function uses.
7:0	InterruptLine: interrupt line. Read-write. This field contains the interrupt line routing information.

D1F1x4C Subsystem and Subvendor ID Mirror

Reset: 0000_0000h.

Bits	Description
31:16	SubsystemID. Read-write. This field sets the value in the corresponding field in D1F1x2C .
15:0	SubsystemVendorID. Read-write. This field sets the value in the corresponding field in D1F1x2C .

D1F1x50 Power Management Capability

Bits	Description
31:27	PmeSupport. Value: 0_0000b. Indicates that there is no PME support.
26	D2Support: D2 support. Value: 1. D2 is supported
25	D1Support: D1 support. Value: 1. D1 is supported
24:22	AuxCurrent: auxiliary current. Value: 0.
21	DevSpecificInit: device specific initialization. Value: 0. Indicates that there is no device specific initialization necessary.
20	Reserved.
19	PmeClock. Value: 0.
18:16	Version: version. Value: 011b.
15:8	NextPtr: next pointer. Value: IF (D0F0xD4_x0130_14BE[StrapBifMsiDis]==0) THEN A0h. ELSE 00h. ENDIF.
7:0	CapID: capability ID. Value: 01h. Indicates that the capability structure is a PCI power management data structure.

D1F1x54 Power Management Control and Status

Reset: 0000_0000h.

Bits	Description								
31:24	PmeData . Read-only.								
23	BusPwrEn . Read-only.								
22	B2B3Support . Read-only. B states are not supported.								
21:16	Reserved.								
15	PmeStatus: PME status . Read-only.								
14:13	DataScale: data scale . Read-only.								
12:9	DataSelect: data select . Read-only.								
8	PmeEn: PME# enable . Read-only.								
7:4	Reserved.								
3	NoSoftReset: no soft reset . Read-only. Software is required to re-initialize the function when returning from D3hot.								
2	Reserved.								
1:0	PowerState: power state . Read-write. This 2-bit field is used both to determine the current power state of the root port and to set the root port into a new power state. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>D0</td> </tr> <tr> <td>01b, 10b</td> <td>Reserved</td> </tr> <tr> <td>11b</td> <td>D3hot</td> </tr> </tbody> </table>	Bits	Definition	00b	D0	01b, 10b	Reserved	11b	D3hot
Bits	Definition								
00b	D0								
01b, 10b	Reserved								
11b	D3hot								

D1F1x58 PCI Express Capability

Bits	Description
31:30	Reserved.
29:25	IntMessageNum: interrupt message number . Value: 0. This field indicates which MSI vector is used for the interrupt message.
24	SlotImplemented: Slot implemented . Value: 0.
23:20	DeviceType: device type . Value: 9h.
19:16	Version . Value: 2h.
15:8	NextPtr: next pointer . Value: IF (D0F0xD4_x0130_14BE[StrapBifMsiDis]==0) THEN A0h. ELSE 00h. ENDIF.
7:0	CapID: capability ID . Value: 10h.

D1F1x5C Device Capability

Bits	Description
31:29	Reserved.

28	FlrCapable: function level reset capability. Value: IF (D0F0xD4_x0130_14BC[StrapBifFlrEn]==1) THEN 1h. ELSE 0h. ENDIF.
27:26	CapturedSlotPowerScale: captured slot power limit scale. Value: 0.
25:18	CapturedSlotPowerLimit: captured slot power limit value. Value: 0.
17:16	Reserved.
15	RoleBasedErrReporting: role-based error reporting. Value: 1.
14:12	Reserved.
11:9	L1AcceptableLatency: endpoint L1 Acceptable Latency. Value: 111b.
8:6	L0SAcceptableLatency: endpoint L0s Acceptable Latency. Value: 110b.
5	ExtendedTag: extended tag support. Value: 1. 8 bit tag support.
4:3	PhantomFunc: phantom function support. Value: 0. No phantom functions supported.
2:0	MaxPayloadSupport: maximum supported payload size. Value: 000b. 128 bytes max payload size.

D1F1x60 Device Control and Status

Reset: 0000_0810h.

Bits	Description
31:22	Reserved.
21	TransactionsPending: transactions pending. Read-only.
20	AuxPwr: auxiliary power. Read-only.
19	UsrDetected: unsupported request detected. Read; Write-1-to-clear. 1=Unsupported request received.
18	FatalErr: fatal error detected. Read; Write-1-to-clear. 1=Fatal error detected.
17	NonFatalErr: non-fatal error detected. Read; Write-1-to-clear. 1=Non-fatal error detected.
16	CorrErr: correctable error detected. Read; Write-1-to-clear. 1=Correctable error detected.
15	BridgeCfgRetryEn: bridge configuration retry enable. Read-only.
14:12	MaxRequestSize: maximum request size. Read-only. 0=The root port never generates read requests with size exceeding 128 bytes.
11	NoSnoopEnable: enable no snoop. Read-write. 1=The device is permitted to set the No Snoop bit in requests.
10	AuxPowerPmEn: auxiliary power PM enable. Read-only. This capability is not implemented.
9	PhantomFuncEn: phantom functions enable. Read-only. Phantom functions are not supported.
8	ExtendedTagEn: extended tag enable. Read-write. 1=8-bit tag request tags. 0=5-bit request tag.
7:5	MaxPayloadSize: maximum supported payload size. Read-only. 000b=Indicates a 128 byte maximum payload size.
4	RelaxedOrdEn: relaxed ordering enable. Read-write. 1=The device is permitted to set the Relaxed Ordering bit.
3	UsrReportEn: unsupported request reporting enable. Read-write. 1=Enables signaling unsupported requests by sending error messages.

2	FatalErrEn: fatal error reporting enable. Read-write. 1=Enables sending ERR_FATAL message when a fatal error is detected.
1	NonFatalErrEn: non-fatal error reporting enable. Read-write. 1=Enables sending ERR_NONFATAL message when a non-fatal error is detected.
0	CorrErrEn: correctable error reporting enable. Read-write. 1=Enables sending ERR_CORR message when a correctable error is detected.

D1F1x64 Link Capability

Bits	Description
31:24	PortNumber: port number. Value: 0. This field indicates the PCI Express port number for the given PCI Express link.
23:22	Reserved.
21	LinkBWNotificationCap: link bandwidth notification capability. Read-only. Value: 0b.
20	DLActiveReportingCapable: data link layer active reporting capability. Read-only. Value: 0b.
19	SurpriseDownErrReporting: surprise down error reporting capability. Read-only. Value: 0b.
18	ClockPowerManagement: clock power management. Read-only. Value: 0b.
17:15	L1ExitLatency: L1 exit latency. Read-only. Value: 0b.
14:12	L0sExitLatency: L0s exit latency. Read-only. Value: 0b.
11:10	PMSupport: active state power management support. Read-only. Value: 0b.
9:4	LinkWidth: maximum link width. Read-only. Value: 0.
3:0	LinkSpeed: link speed. Read-only. Value: 0b.

D1F1x68 Link Control and Status

Reset: 0000_0000h.

Bits	Description
31	LinkAutonomousBWStatus: link autonomous bandwidth status. Read-only.
30	LinkBWManagementStatus: link bandwidth management status. Read-only.
29	DLActive: data link layer link active. Read-only. This bit indicates the status of the data link control and management state machine. Reads return a 1 to indicate the DL_Active state, otherwise 0 is returned.
28	SlotClockCfg: slot clock configuration. Read-only. 1=The root port uses the same clock that the platform provides.
27	LinkTraining: link training. Read-only. 1=Indicates that the physical layer link training state machine is in the configuration or recovery state, or that 1b was written to the RetrainLink bit but link training has not yet begun. Hardware clears this bit when the link training state machine exits the configuration/recovery state.
26	Reserved.
25:20	NegotiatedLinkWidth: negotiated link width. Read-only. This field indicates the negotiated width of the given PCI Express link.

19:16	LinkSpeed: link speed. Read-only. <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Reserved</td></tr> <tr> <td>1h</td><td>2.5 Gb/s.</td></tr> <tr> <td>2h</td><td>5 Gb/s.</td></tr> <tr> <td>Fh-3h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	0h	Reserved	1h	2.5 Gb/s.	2h	5 Gb/s.	Fh-3h	Reserved		
Bits	Description												
0h	Reserved												
1h	2.5 Gb/s.												
2h	5 Gb/s.												
Fh-3h	Reserved												
15:12	Reserved.												
11	LinkAutonomousBWIntEn: link autonomous bandwidth interrupt enable. Read-only.												
10	LinkBWManagementEn: link bandwidth management interrupt enable. Read-only.												
9	HWAutonomousWidthDisable: hardware autonomous width disable. Read-only. 1=Hardware not allowed to change the link width except to correct unreliable link operation by reducing link width.												
8	ClockPowerManagementEn: clock power management enable. Read-only.												
7	ExtendedSync: extended sync. Read-only. 1=Forces the transmission of additional ordered sets when exiting the L0s state and when in the recovery state.												
6	CommonClockCfg: common clock configuration. Read-only. 1=Indicates that the root port and the component at the opposite end of this Link are operating with a distributed common reference clock. 0=Indicates that the upstream port and the component at the opposite end of this Link are operating with asynchronous reference clock.												
5	RetrainLink: retrain link. Read-only. This bit does not apply to endpoints.												
4	LinkDis: link disable. Read-only. This bit does not apply to endpoints.												
3	ReadCplBoundary: read completion boundary. Read-only. 0=64 byte read completion boundary.												
2	Reserved.												
1:0	PmControl: active state power management enable. Read-only. This field controls the level of ASPM supported on the given PCI Express link. <table border="1"> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Disabled.</td><td>10b</td><td>L1 Entry Enabled.</td></tr> <tr> <td>01b</td><td>L0s Entry Enabled.</td><td>11b</td><td>L0s and L1 Entry Enabled.</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Disabled.	10b	L1 Entry Enabled.	01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.
Bits	Definition	Bits	Definition										
00b	Disabled.	10b	L1 Entry Enabled.										
01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.										

D1F1x7C Device Capability 2

Reset: 0000_0000h.

Bits	Description
31:5	Reserved.
4	CplTimeoutDisSup: completion timeout disable supported. Read-only.
3:0	CplTimeoutRangeSup: completion timeout range supported. Read-only.

D1F1x80 Device Control and Status 2

Reset: 0000_0000h.

Bits	Description
31:5	Reserved.
4	CplTimeoutDis: completion timeout disable. Read-only.
3:0	CplTimeoutValue: completion timeout range supported. Read-only.

D1F1x84 Link Capability 2

Bits	Description
31:0	Reserved.

D1F1x88 Link Control and Status 2

Reset: 0000_0000h.

Bits	Description
31:17	Reserved.
16	CurDeemphasisLevel: current deemphasis level. Read-only. 1=-3.5 dB. 0=-6 dB.
15:13	Reserved.
12	ComplianceDeemphasis: compliance deemphasis. Read-only. This bit defines the deemphasis level used in compliance mode. 1=-3.5 dB. 0=-6 dB.
11	ComplianceSOS: compliance SOS. Read-only. 1=The device transmits skip ordered sets in between the modified compliance pattern.
10	EnterModCompliance: enter modified compliance. Read-only. 1=The device transmits modified compliance pattern.
9:7	XmitMargin: transmit margin. Read-only. This field controls the non-deemphasized voltage level at the transmitter pins.
6	SelectableDeemphasis: selectable deemphasis. Read-only.
5	HwAutonomousSpeedDisable: hardware autonomous speed disable. Read-only. 1=Disables hardware generated link speed changes.
4	EnterCompliance: enter compliance. Read-only. 1=Force link to enter compliance mode.
3:0	TargetLinkSpeed: target link speed. Read-only. This field defines the upper limit of the link operational speed.

D1F1xA0 MSI Capability

Bits	Description
31:24	Reserved.
23	Msi64bit: MSI 64 bit capability. Read-only. Reset: 1. 1=The device is capable of sending 64-bit MSI messages. 0=The device is not capable of sending a 64-bit message address.
22:20	MsiMultiEn: MSI multiple message enable. Read-write. Reset: 000b. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). When MSI is enabled, a function is allocated at least 1 vector.
19:17	MsiMultiCap: MSI multiple message capability. Read-only. Reset: 000b. 000b=The device is requesting one vector.
16	MsiEn: MSI enable. Read-write. Reset: 0. 1=MSI generation is enabled and INTx generation is disabled. 0=MSI generation disabled and INTx generation is enabled.
15:8	NextPtr: next pointer. Read-only. Reset: 00h.
7:0	CapID: capability ID. Read-only. Reset: 05h. 05h=MSI capability structure.

D1F1xA4 MSI Message Address Low

Reset: 0000_0000h.

Bits	Description
31:2	MsiMsgAddrLo: MSI message address. Read-write. This register specifies the dword aligned address for the MSI memory write transaction.
1:0	Reserved.

D1F1xA8 MSI Message Address High

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	MsiMsgAddrHi: MSI message address. Read-write. This register specifies the upper 8-bits of the MSI address in 64 bit MSI mode.

D1F1xAC MSI Message Data

Reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15:0	MsiData: MSI message data. Read-write. This register specifies lower 16 bits of data for the MSI memory write transaction. The upper 16 bits are always 0.

D1F1x100 Vendor Specific Enhanced Capability

Reset: 0111_000Bh.

Bits	Description
31:20	NextPtr: next pointer. Read-only.
19:16	CapVer: capability version. Read-only.
15:0	CapID: capability ID. Read-only.

D1F1x104 Vendor Specific Header

Reset: 0101_0001h.

Bits	Description
31:20	VsecLen: vendor specific enhanced next pointer. Read-only.
19:16	VsecRev: vendor specific enhanced capability version. Read-only.
15:0	VsecID: vendor specific enhanced capability ID. Read-only.

D1F1x108 Vendor Specific 1

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write.

D1F1x10C Vendor Specific 2

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write.

3.7 Device 2 Function 0 (Host Bridge) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space. D2F0 registers do not control any hardware. They ensure that software can configure functions 1 through 4.

D2F0x00 Device/Vendor ID (Host Bridge)

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1538h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D2F0x04 Status/Command

Reset: 0000_0000h.

Bits	Description
31:16	Status. Read-only. Tied to 0x0h.
15:0	Command. Read-only. Tied to 0x0h.

D2F0x08 Class Code/Revision ID

Reset: 0600_0000h.

Bits	Description
31:8	ClassCode: class code. Read-only. Tied to 0x06_0000h.
7:0	RevId: revision identifier. Read-only. Tied to 0x0h.

D2F0x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:24	Reserved.
23	DeviceType. Read-only. 1=Indicates that the northbridge block is a multi-function device. 0=Indicates that the northbridge block is a single function device.
22:16	HeaderType. Read-only. Indicates multiple functions present in this device.
15:0	Reserved.

D2F0x40 Header Type Write

Reset: 0000_0080h.

Bits	Description
31:8	Reserved.
7	DeviceType . Read-write. This field sets the value in D2F0x0C[DeviceType]. 0=Single function device. 1=Multi-function device.
6:0	Reserved.

3.8 Device 2 Function [5:1] (Root Port) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space. See 2.11.1 [Overview].

D2F[5:1]x00 Device/Vendor ID

Table 98: Register Mapping for D2F[5:1]x00

D2F[5:1]x00	Function
D2F1x00	GPP Bridge 0
D2F2x00	GPP Bridge 1
D2F3x00	GPP Bridge 2
D2F4x00	GPP Bridge 3
D2F5x00	GPP Bridge 4

Bits	Description
31:16	DeviceID: device ID . Read-only. Value: 1439h.
15:0	VendorID: vendor ID . Read-only. Value: 1022h.

D2F[5:1]x04 Status/Command Register

Reset: 0010_0000h.

Bits	Description
31	ParityErrorDetected: detected parity error . Read; Write-1-to-clear.
30	SignaledSystemError: signaled system error . Read; Write-1-to-clear. 1=System error signalled.
29	ReceivedMasterAbort: received master abort . Read; Write-1-to-clear.
28	ReceivedTargetAbort: received target abort . Read; Write-1-to-clear.
27	SignalTargetAbort: signaled target abort . Read; Write-1-to-clear.
26:25	DevselTiming: DEVSEL# Timing . Read-only.

24	DataPerr: data parity error. Read; Write-1-to-clear.
23	FastBackCapable: fast back-to-back capable. Read-only.
22	Reserved.
21	PCI66En: 66 MHz capable. Read-only.
20	CapList: capability list. Read-only. 1= Capability list present.
19	IntStatus: interrupt status. Read-only. 1=An INTx interrupt Message is pending in the device.
18:11	Reserved.
10	IntDis: interrupt disable. Read-write.
9	FastB2BEn: fast back-to-back enable. Read-only.
8	SerrEn: system error enable. Read-write. 1=System error reporting enabled.
7	Stepping: Stepping control. Read-only.
6	ParityErrorEn: parity error response enable. Read-write.
5	PalSnoopEn: VGA palette snoop enable. Read-only.
4	MemWriteInvalidateEn: memory write and invalidate enable. Read-only.
3	SpecialCycleEn: special cycle enable. Read-only.
2	BusMasterEn: bus master enable. Read-write.
1	MemAccessEn: IO access enable. Read-write. This bit controls if memory accesses targeting this device are accepted or not. 1=Enabled. 0=Disabled.
0	IoAccessEn: IO access enable. Read-write. This bit controls if IO accesses targeting this device are accepted or not. 1=Enabled. 0=Disabled.

D2F[5:1]x08 Class Code/Revision ID Register

Reset: 0604_00xxh.

Bits	Description
31:8	ClassCode. Read-only. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only.

D2F[5:1]x0C Header Type Register

Reset: 0001_0000h.

Bits	Description
31:24	BIST. Read-only. These bits are fixed at their default values.
23	DeviceType. Read-only. 0=Single function device. 1=Multi-function device.
22:16	HeaderType. Read-only. These bits are fixed at their default values. Indicates a Type 0 or Type 1 configuration space.
15:8	LatencyTimer. Read-only. This field does not control any hardware.
7:0	CacheLineSize. Read-write.

D2F[5:1]x18 Bus Number and Secondary Latency Register

Reset: 0000_0000h.

Bits	Description
31:24	SecondaryLatencyTimer: secondary latency timer. Read-only. This field is always 0.
23:16	SubBusNumber: subordinate number. Read-write. This field contains the highest-numbered bus that exists on the secondary side of the bridge.
15:8	SecondaryBus: secondary bus number. Read-write. This field defines the bus number of the secondary bus interface.
7:0	PrimaryBus: primary bus number. Read-write. This field defines the bus number of the primary bus interface.

D2F[5:1]x1C IO Base and Secondary Status Register

Reset: 0000_0101h.

Bits	Description
31	ParityErrorDetected: detected parity error. Read; Write-1-to-clear. A Poisoned TLP was received regardless of the state of the D2F[5:1]x04[ParityErrorEn] .
30	ReceivedSystemError: signaled system error. Read; Write-1-to-clear. 1=A System Error was detected.
29	ReceivedMasterAbort: received master abort. Read; Write-1-to-clear. 1=A CPU transaction is terminated due to a master-abort.
28	ReceivedTargetAbort: received target abort. Read; Write-1-to-clear. 1=A CPU transaction (except for a special cycle) is terminated due to a target-abort.
27	SignalTargetAbort: signaled target abort. Read; Write-1-to-clear.
26:25	DevselTiming: DEVSEL# Timing. Read-only.
24	MasterDataPerr: master data parity error. Read; Write-1-to-clear. 1=The link received a poisoned or poisoned a downstream write and D2F[5:1]x3C[ParityResponseEn] =1.
23	FastBackCapable: fast back-to-back capable. Read-only.
22	Reserved.
21	PCI66En: 66 MHz capable. Read-only.
20	CapList: capability list. Read-only.
19:16	Reserved.
15:12	IOLimit[15:12]. Read-write. Lower part of the limit address. Upper part is defined in D2F[5:1]x30 .
11:8	IOLimitType. Read-only. 0=16-bit. 1=32-bit.
7:4	IOBase[15:12]. Read-write. Lower part of the base address. Upper part is defined in D2F[5:1]x30 .
3:0	IOBaseType. Read-only. 0=16-bit. 1=32-bit.

D2F[5:1]x20 Memory Limit and Base Register

Reset: 0000_0000h.

Bits	Description
31:20	MemLimit[31:20] . Read-write.
19:16	MemLimitType . Read-only. 0=32-bit. 1=64-bit.
15:4	MemBase[31:20] . Read-write.
3:0	MemBaseType . Read-only. 0=32-bit. 1=64-bit.

D2F[5:1]x24 Prefetchable Memory Limit and Base Register

Reset: 0001_0001h.

Bits	Description
31:20	PrefMemLimit . Read-write. Lower part of the limit address. Upper part is defined in D2F[5:1]x2C .
19:16	PrefMemLimitType . Read-only. 0=32-bit. 1=64-bit.
15:4	PrefMemBase[31:20] . Read-write. Lower part of the base address. Upper part is defined in D2F[5:1]x28 .
3:0	PrefMemBaseType . Read-only. 0=32-bit. 1=64-bit.

D2F[5:1]x28 Prefetchable Memory Base High Register

Reset: 0000_0000h.

Bits	Description
31:0	PrefMemBase[63:32] . Read-write. Upper part of the base address. Lower part is defined in D2F[5:1]x24 .

D2F[5:1]x2C Prefetchable Memory Limit High Register

Reset: 0000_0000h.

Bits	Description
31:0	PrefMemLimit[63:32] . Read-write. Upper part of the limit address. Lower part is defined in D2F[5:1]x24 .

D2F[5:1]x30 IO Base and Limit High Register

Reset: 0000_0000h.

Bits	Description
31:16	IOLimit[31:16] . Read-write. Upper part of the limit address. Lower part is defined in D2F[5:1]x1C .
15:0	IOBase[31:16] . Read-write. Upper part of the base address. Lower part is defined in D2F[5:1]x1C .

D2F[5:1]x34 Capabilities Pointer Register

Reset: 0000_0050h.

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Pointer to PM capability.

D2F[5:1]x3C Bridge Control Register

Reset: 0000_00FFh.

Bits	Description
31:24	Reserved.
23	FastB2BCap: Fast back-to-back capability. Read-only.
22	SecondaryBusReset: Secondary bus reset. Read-write. Setting this bit triggers a hot reset on the corresponding PCI Express Port.
21	MasterAbortMode: Master abort mode. Read-only.
20	Vga16En: VGA IO 16 bit decoding enable. Read-write. 1= Address bits 15:10 for VGA IO cycles are decoded. 0=Address bits 15:10 for VGA IO cycles are ignored.
19	VgaEn: VGA enable. Read-write. Affects the response by the bridge to compatible VGA addresses. When it is set, the bridge decodes and forwards the following accesses on the primary interface to the secondary interface: Memory accesses in the range of A_0000h to B_FFFFh and IO address where address bits 9:0 are in the ranges of 3B0h to 3BBh or 3C0h to 3DFh. For IO cycles the decoding of address bits 15:10 depends on Vga16En.
18	IsaEn: ISA enable. Read-write.
17	SerrEn: SERR enable. Read-write.
16	ParityResponseEn: Parity response enable. Read-write. Controls the bridge's response to poisoned TLPs on its secondary interface. 1=The bridge takes its normal action when a poisoned TLP is received. 0=The bridge ignores any poisoned TLPs that it receives and continues normal operation.
15:11	IntPinR: interrupt pin. Read-only.
10:8	IntPin: interrupt pin. IF (D0F0xE4_x0140_0010[HwInitWrLock]==1) THEN Read-only. ELSE Read-write. ENDIF.
7:0	IntLine: Interrupt line. Read-write.

D2F[5:1]x50 Power Management Capability Register

Reset: 0003_5801h.

Bits	Description
31:27	PmeSupport. Read-only.
26	D2Support: D2 support. Read-only. D2 is not supported
25	D1Support: D1 support. Read-only. D1 is not supported

24:22	AuxCurrent: auxiliary current. IF (D0F0xE4_x0140_0010[HwInitWrLock]==1) THEN Read-only. ELSE Read-write. ENDIF. Auxiliary current is not supported.
21	DevSpecificInit: device specific initialization. Read-only. This field is hardwired to 0 to indicate that there is no device specific initialization necessary.
20	Reserved.
19	PmeClock. Read-only. 0=Indicate that PCI clock is not needed to generate PME messages.
18:16	Version: version. Read-only. 3=PMI Spec 1.2
15:8	NextPtr: next pointer. Read-only. 58h=Address of the next capability structure.
7:0	CapID: capability ID. Read-only. 01h=PCI power management data structure.

D2F[5:1]x54 Power Management Control and Status Register

Bits	Description												
31:24	PmiData. Read-only. Reset: 0.												
23	BusPwrEn. Read-only. Reset: 0.												
22	B2B3Support. Read-only. Reset: 0. B states are not supported.												
21:16	Reserved.												
15	PmeStatus: PME status. Read; Write-1-to-clear. Reset: 0. This bit is set when the root port would issue a PME message (independent of the state of the PmeEn bit). Once set, this bit remains set until it is reset by writing a 1 to this bit location. Writing a 0 has no effect.												
14:13	DataScale: data scale. Read-only. Reset: 0.												
12:9	DataSelect: data select. Read-only. Reset: 0.												
8	PmeEn: PME# enable. Read-write. Reset: 0.												
7:4	Reserved.												
3	NoSoftReset: no soft reset. Read-only. Reset: 0. Software is required to re-initialize the function when returning from D3 _{hot} .												
2	Reserved.												
1:0	PowerState: power state. Read-write. Reset: 0. This 2-bit field is used both to determine the current power state of the root port and to set the root port into a new power state. <table border="1" style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>D0</td> <td>10b</td> <td>Reserved</td> </tr> <tr> <td>01b</td> <td>Reserved</td> <td>11b</td> <td>D3</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	D0	10b	Reserved	01b	Reserved	11b	D3
Bits	Definition	Bits	Definition										
00b	D0	10b	Reserved										
01b	Reserved	11b	D3										

D2F[5:1]x58 PCI Express Capability Register

Reset: 0042_A010h.

Bits	Description
31:30	Reserved.
29:25	IntMessageNum: interrupt message number. Read-only. This register indicates which MSI vector is used for the interrupt message.
24	SlotImplemented: Slot implemented. IF (D0F0xE4_x0140_0010[HwInitWrLock]==1) THEN Read-only. ELSE Read-write. ENDIF. 1=The IO Link associated with this port is connected to a slot.

23:20	DeviceType: device type. Read-only. 4h=Root complex.
19:16	Version. Read-only. 2h=GEN 2 compliant.
15:8	NextPtr: next pointer. Read-only. A0h=Pointer to the next capability structure.
7:0	CapID: capability ID. Read-only. 10h=PCIe® Capability structure.

D2F[5:1]x5C Device Capability Register

Reset: 0000_0020h.

Bits	Description
31:29	Reserved.
28	FlrCapable: function level reset capability. Read-only.
27:26	CapturedSlotPowerScale: captured slot power limit scale. Read-only.
25:18	CapturedSlotPowerLimit: captured slot power limit value. Read-only.
17:16	Reserved.
15	RoleBasedErrReporting: role-based error reporting. Read-only.
14:12	Reserved.
11:9	L1AcceptableLatency: endpoint L1 Acceptable Latency. Read-only.
8:6	L0SAcceptableLatency: endpoint L0s Acceptable Latency. Read-only.
5	ExtendedTag: extended tag support. Read-only. 1: 8 bit tag supported 0: 5 bit tag supported.
4:3	PhantomFunc: phantom function support. Read-only. 0=No phantom functions supported.
2:0	MaxPayloadSupport: maximum supported payload size. Read-only. 000b=128 bytes max payload size.

D2F[5:1]x60 Device Control and Status Register

Reset: 0000_2810h.

Bits	Description
31:22	Reserved.
21	TransactionsPending: transactions pending. Read-only. 0=No internally generated non-posted transactions pending.
20	AuxPwr: auxiliary power. IF (D0F0xE4_x0140_0010[HwInitWrLock]==1) THEN Read-only. ELSE Read-write. ENDIF.
19	UsrDetected: unsupported request detected. Read; Write-1-to-clear. 1=The port received an unsupported request. Errors are logged in this register even if error reporting is disabled.
18	FatalErr: fatal error detected. Read; Write-1-to-clear. 1=The port detected a fatal error. Errors are logged in this register even if error reporting is disabled.
17	NonFatalErr: non-fatal error detected. Read; Write-1-to-clear. T1=The port detected a non-fatal error. Errors are logged in this register even if error reporting is disabled.
16	CorrErr: correctable error detected. Read; Write-1-to-clear. 1=The port detected a correctable error. Errors are logged in this register even if error reporting is disabled.

15	BridgeCfgRetryEn: bridge configuration retry enable. Read-only.																
14:12	MaxRequestSize: maximum request size. Read-write.																
11	NoSnoopEnable: enable no snoop. Read-write. 1=The port is permitted to set the No Snoop bit in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency.																
10	AuxPowerPmEn: auxiliary power PM enable. Read-only.																
9	PhantomFuncEn: phantom functions enable. Read-only.																
8	ExtendedTagEn: extended tag enable. Read-write. 1=8-bit tags generation enabled. 0=5-bit tags are used.																
7:5	MaxPayloadSize: maximum supported payload size. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>128B</td> <td>3h</td> <td>1024B</td> </tr> <tr> <td>1h</td> <td>256B</td> <td>4h</td> <td>2048B</td> </tr> <tr> <td>2h</td> <td>512B</td> <td>5h</td> <td>4096B</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0h	128B	3h	1024B	1h	256B	4h	2048B	2h	512B	5h	4096B
Bits	Definition	Bits	Definition														
0h	128B	3h	1024B														
1h	256B	4h	2048B														
2h	512B	5h	4096B														
4	RelaxedOrdEn: relaxed ordering enable. Read-write. 1=The root port is permitted to set the relaxed ordering bit in the attributes field of transactions it initiates that do not require strong write ordering.																
3	UsrReportEn: unsupported request reporting enable. Read-write. 1=Reporting of unsupported requests enabled.																
2	FatalErrEn: fatal error reporting enable. Read-write. 1=Enable sending ERR_FATAL messages.																
1	NonFatalErrEn: non-fatal error reporting enable. Read-write. 1=Enable sending ERR_NONFATAL messages.																
0	CorrErrEn: correctable error reporting enable. Read-write. 1=Enable sending ERR_CORR messages.																

D2F[5:1]x64 IO Link Capability Register

Read-only.

Bits	Description
31:24	PortNumber: port number. Reset: 0. This field indicates the port number for the given IO link.
23	Reserved.
22	AspmOptionalityCompliance. Reset: 1. This field indicates if the component supports the ASPM Optionality ECN.
21	LinkBWNotificationCap: link bandwidth notification capability. Reset: 0. This bit is controlled by ~D2F[5:1]xE4_xB1[LcLinkBwNotificationDis].
20	DLActiveReportingCapable: data link layer active reporting capability. Reset: 0.
19	SurpriseDownErrReporting. Reset: 0. 1=This field indicates if the component supports the detecting and reporting of a Surprise Down error condition.
18	ClockPowerManagement: clock power management. Reset: 0. 0=Indicates that the reference clock must not be removed while in L1 or L2/L3 ready link states.
17:15	L1ExitLatency: L1 exit latency. Reset: 010b. 010b=Indicate an exit latency between 2 us and 4 us.

14:12	L0sExitLatency: L0s exit latency. Reset: 001b. 001b=Indicates an exit latency between 64 ns and 128 ns.																														
11:10	PMSupport: active state power management support. Reset: 11b. 11b=Indicates support of L0s and L1.																														
9:4	LinkWidth: maximum link width. Value: 10h. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved.</td> </tr> <tr> <td>01h</td> <td>1 lanes</td> </tr> <tr> <td>02h</td> <td>2 lanes</td> </tr> <tr> <td>03h</td> <td>Reserved.</td> </tr> <tr> <td>04h</td> <td>4 lanes</td> </tr> <tr> <td>07h-05h</td> <td>Reserved.</td> </tr> <tr> <td>08h</td> <td>8 lanes</td> </tr> <tr> <td>0Bh-09h</td> <td>Reserved.</td> </tr> <tr> <td>0Ch</td> <td>12 lanes</td> </tr> <tr> <td>0Fh-0Dh</td> <td>Reserved.</td> </tr> <tr> <td>10h</td> <td>16 lanes</td> </tr> <tr> <td>1Fh-11h</td> <td>Reserved.</td> </tr> <tr> <td>20h</td> <td>32 lanes</td> </tr> <tr> <td>3Fh-21h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	00h	Reserved.	01h	1 lanes	02h	2 lanes	03h	Reserved.	04h	4 lanes	07h-05h	Reserved.	08h	8 lanes	0Bh-09h	Reserved.	0Ch	12 lanes	0Fh-0Dh	Reserved.	10h	16 lanes	1Fh-11h	Reserved.	20h	32 lanes	3Fh-21h	Reserved.
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1Fh-11h	Reserved.																														
20h	32 lanes																														
3Fh-21h	Reserved.																														
3:0	LinkSpeed: link speed. Value: IF (D2F[5:1]xE4_xA4[LcGen2EnStrap]==0 THEN 1h ELSEIF (D2F[5:1]xE4_xA4[LcGen2EnStrap]==1 THEN 2h ENDIF. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved.</td> </tr> <tr> <td>1h</td> <td>2.5 Gb/s</td> </tr> <tr> <td>2h</td> <td>5.0 Gb/s</td> </tr> <tr> <td>Fh-3h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0h	Reserved.	1h	2.5 Gb/s	2h	5.0 Gb/s	Fh-3h	Reserved.																				
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Fh-3h	Reserved.																														

D2F[5:1]x68 IO Link Control and Status Register

Reset: 1001_0000h.

Bits	Description
31	LinkAutonomousBWStatus: link autonomous bandwidth status. IF (D2F[5:1]x64[LinkBWNotificationCap]==0) THEN Read-only. ELSE Read-write; updated-by-hardware. ENDIF.
30	LinkBWManagementStatus: link bandwidth management status. IF (D2F[5:1]x64[LinkBWNotificationCap]==0) THEN Read-only. ELSE Read-write; updated-by-hardware. ENDIF.
29	DLActive: data link layer link active. Read-only; updated-by-hardware. This bit indicates the status of the data link control and management state machine. 1=DL_Active state. 0>All other states.
28	SlotClockCfg: slot clock configuration. Read-only; updated-by-hardware. 1=The root port uses the same clock that the platform provides.
27	LinkTraining: link training. Read-only; updated-by-hardware. This read-only bit indicates that the physical layer link training state machine is in the configuration or recovery state, or that 1b was written to the RetrainLink bit but link training has not yet begun. Hardware clears this bit when the link training state machine exits the configuration/recovery state.

26	Reserved.																														
25:20	<p>NegotiatedLinkWidth: negotiated link width. Read-only; updated-by-hardware. This field indicates the negotiated width of the given PCI Express link.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved.</td> </tr> <tr> <td>01h</td> <td>1 lanes</td> </tr> <tr> <td>02h</td> <td>2 lanes</td> </tr> <tr> <td>03h</td> <td>Reserved.</td> </tr> <tr> <td>04h</td> <td>4 lanes</td> </tr> <tr> <td>07h-05h</td> <td>Reserved.</td> </tr> <tr> <td>08h</td> <td>8 lanes</td> </tr> <tr> <td>0Bh-09h</td> <td>Reserved.</td> </tr> <tr> <td>0Ch</td> <td>12 lanes</td> </tr> <tr> <td>0Fh-0Dh</td> <td>Reserved.</td> </tr> <tr> <td>10h</td> <td>16 lanes</td> </tr> <tr> <td>1Fh-11h</td> <td>Reserved.</td> </tr> <tr> <td>20h</td> <td>32 lanes</td> </tr> <tr> <td>3Fh-21h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	00h	Reserved.	01h	1 lanes	02h	2 lanes	03h	Reserved.	04h	4 lanes	07h-05h	Reserved.	08h	8 lanes	0Bh-09h	Reserved.	0Ch	12 lanes	0Fh-0Dh	Reserved.	10h	16 lanes	1Fh-11h	Reserved.	20h	32 lanes	3Fh-21h	Reserved.
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19:16	<p>LinkSpeed: link speed. Read-only; updated-by-hardware.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved.</td> </tr> <tr> <td>01h</td> <td>2.5 Gb/s</td> </tr> <tr> <td>02h</td> <td>5.0 Gb/s</td> </tr> <tr> <td>Fh-3h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	00h	Reserved.	01h	2.5 Gb/s	02h	5.0 Gb/s	Fh-3h	Reserved.																				
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02h	5.0 Gb/s																														
Fh-3h	Reserved.																														
15:12	Reserved.																														
11	<p>LinkAutonomousBWIntEn: link autonomous bandwidth interrupt enable. Read-write. 1=Enables the generation of an interrupt to indicate that the Link AutonomousBWStatus bit has been set.</p>																														
10	<p>LinkBWManagementIntEn: link bandwidth management interrupt enable. Read-write. 1=Enables the generation of an interrupt to indicate that the LinkBWManagementStatus has been set.</p>																														
9	<p>HWAutonomousWidthDisable: hardware autonomous width disable. Read-write. 1=Disables hardware from changing the link width for reasons other than attempting to correct unreliable link operation by reducing link width.</p>																														
8	<p>ClockPowerManagementEn: clock power management enable. Read-write.</p>																														
7	<p>ExtendedSync: extended sync. Read-write. 1=Forces the transmission of additional ordered sets when exiting the L0s state and when in the recovery state.</p>																														
6	<p>CommonClockCfg: common clock configuration. Read-write. 1=Indicates that the root port and the component at the opposite end of this IO link are operating with a distributed common reference clock. 0=Indicates that the root port and the component at the opposite end of this IO Link are operating with asynchronous reference clock.</p>																														
5	<p>RetrainLink: retrain link. Read-write; cleared-when-done. 1=Initiate link retraining.</p>																														
4	<p>LinkDis: link disable. Read-write. 1=Disable link. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual link state.</p>																														
3	<p>ReadCplBoundary: read completion boundary. Read-only. 0=64 byte read completion boundary.</p>																														

2	Reserved.												
1:0	PmControl: active state power management enable. Read-write. This field controls the level of ASPM supported on the given IO link. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disabled.</td> <td>10b</td> <td>L1 Entry Enabled.</td> </tr> <tr> <td>01b</td> <td>L0s Entry Enabled.</td> <td>11b</td> <td>L0s and L1 Entry Enabled.</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Disabled.	10b	L1 Entry Enabled.	01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.
Bits	Definition	Bits	Definition										
00b	Disabled.	10b	L1 Entry Enabled.										
01b	L0s Entry Enabled.	11b	L0s and L1 Entry Enabled.										

D2F[5:1]x6C Slot Capability Register

Reset: 0004_0000h.

Bits	Description												
31:19	PhysicalSlotNumber: physical slot number. IF (D0F0xE4_x0140_0010[HwInitWrLock]==0) THEN Read-write. ELSE Read-only. ENDIF. This field indicates the physical slot number attached to this port. This field is set to a value that assigns a slot number that is unique within the chassis, regardless of the form factor associated with the slot. This field must be initialized to 0 for ports connected to devices that are on the system board.												
18	NoCmdCplSupport: no command completed support. Read-write. 1=Indicates that this slot does not generate software notification when an issued command is completed by the hot-plug controller.												
17	ElecMechIIPresent: electromechanical interlock present. Read-write. 0=Indicates that a electro-mechanical interlock is not implemented for this slot.												
16:15	SlotPwrLimitScale: slot power limit scale. IF (D0F0xE4_x0140_0010[HwInitWrLock]==0) THEN Read-write. ELSE Read-only. ENDIF. Specifies the scale used for the SlotPwrLimitValue. Range of Values: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.0</td> <td>10b</td> <td>0.01</td> </tr> <tr> <td>01b</td> <td>0.1</td> <td>11b</td> <td>0.001</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	1.0	10b	0.01	01b	0.1	11b	0.001
Bits	Definition	Bits	Definition										
00b	1.0	10b	0.01										
01b	0.1	11b	0.001										
14:7	SlotPwrLimitValue: slot power limit value. IF (D0F0xE4_x0140_0010[HwInitWrLock]==0) THEN Read-write. ELSE Read-only. ENDIF. In combination with the SlotPwrLimitScale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) calculated by multiplying the value in this field by the value in the SlotPwrLimitScale field.												
6	HotplugCapable: hot-plug capability. IF (D0F0xE4_x0140_0010[HwInitWrLock]==0) THEN Read-write. ELSE Read-only. ENDIF. 1=Indicates that this slot is capable of supporting hot-plug operations.												
5	HotplugSurprise: hot-plug surprise. IF (D0F0xE4_x0140_0010[HwInitWrLock]==0) THEN Read-write. ELSE Read-only. ENDIF. 1=Indicates that an adapter present in this slot might be removed from the system without any prior notification.												
4	PwrIndicatorPresent: power indicator present. Read-write. 0=Indicates that a power indicator is not implemented for this slot.												
3	AttnIndicatorPresent: attention indicator present. Read-write. 0=Indicates that a attention indicator is not implemented for this slot.												
2	MrlSensorPresent: manual retention latch sensor present. Read-write. 0=Indicates that a manual retention latch sensor is not implemented for this slot.												
1	PwrControllerPresent: power controller present. Read-write. 0=A power controller is not implemented for this slot.												
0	AttnButtonPresent: attention button present. Read-write. 0=An attention button is not implemented for this slot.												

D2F[5:1]x70 Slot Control and Status Register

IF (D2F[5:1]x58[SlotImplemented]==0) THEN Reset: 0040_0000h. ELSE Reset: 0000_0000h. ENDIF.

Bits	Description
31:25	Reserved.
24	DIStateChanged: data link layer state change. Read; Write-1-to-clear. This bit is set when the value reported in the D2F[5:1]x68[DIActive] is changed. In response to a data link layer state changed event, software must read D2F[5:1]x68[DIActive] to determine if the link is active before initiating configuration cycles to the hot plugged device.
23	ElecMechIISts: electromechanical interlock status. Read-only.
22	PresenceDetectState: presence detect state. Read-only. This bit indicates the presence of an adapter in the slot based on the physical layer in-band presence detect mechanism. The in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. 0=Slot empty. 1=Card present in slot. For root ports not connected to slots (D2F[5:1]x58[SlotImplemented]=0b), this bit returns always 1.
21	MrlSensorState. Read-only.
20	CmdCpl: command completed. Read-only.
19	PresenceDetectChanged: presence detect changes. Read; Write-1-to-clear. This bit is set when the value reported in PresenceDetectState is changed.
18	MrlSensorChanged. Read; Write-1-to-clear.
17	PwrFaultDetected. Read; Write-1-to-clear.
16	AttnButtonPressed: attention button pressed. Read-only.
15:13	Reserved.
12	DIStateChangedEn: data link layer state changed enable. Read-write. 1=Enables software notification when D2F[5:1]x68[DIActive] is changed.
11	ElecMechIICntl: electromechanical interlock control. Read-only.
10	PwrControllerCntl: power controller control. Read-only.
9:8	PwrIndicatorCntl: power indicator control. Read-only.
7:6	AttnIndicatorControl: attention indicator control. Read-only.
5	HotplugIntrEn: hot-plug interrupt enable. Read-only.
4	CmdCplIntrEn: command complete interrupt enable. Read-only.
3	PresenceDetectChangedEn: presence detect changed enable. Read-only.
2	MrlSensorChangedEn: manual retention latch sensor changed enable. Read-only.
1	PwrFaultDetectedEn: power fault detected enable. Read-only.
0	AttnButtonPressedEn: attention button pressed enable. Read-only.

D2F[5:1]x74 Root Complex Capability and Control Register

Reset: 0001_0000h.

Bits	Description
31:17	Reserved.

16	CrsSoftVisibility: CRS software visibility. Read-only. 1=Indicates that the root port supports returning configuration request retry status (CRS) completion status to software.
15:5	Reserved.
4	CrsSoftVisibilityEn: CRS software visibility enable. Read-write. 1=Enables the root port returning configuration request retry status (CRS) completion status to software.
3	PmIntEn: PME interrupt enable. Read-write. 1=Enables interrupt generation upon receipt of a PME message as reflected D2F[5:1]x78[PmeStatus] . A PME interrupt is also generated if D2F[5:1]x78[PmeStatus] =1 and this bit is set by software.
2	SerrOnFatalErrEn: system error on fatal error enable. Read-write. 1=Indicates that a system error should be generated if a fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself.
1	SerrOnNonFatalErrEn: system error on non-fatal error enable. Read-write. 1=Indicates that a system error should be generated if a non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself. See 2.13.7.8 [SERR Message] .
0	SerrOnCorrErrEn: system error on correctable error enable. Read-write. 1=Indicates that a system error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with this root port, or by the root port itself. See 2.13.7.8 [SERR Message] .

D2F[5:1]x78 Root Complex Status Register

Reset: 0000_0000h.

Bits	Description
31:18	Reserved.
17	PmePending: PME pending. Read-only. This bit indicates that another PME is pending when PmeStatus is set. When PmeStatus is cleared by software; the PME is delivered by hardware by setting the PmeStatus bit again and updating the requestor ID appropriately. PmePending is cleared by hardware if no more PMEs are pending.
16	PmeStatus: pme status. Read; Write-1-to-clear. This bit indicates that PME was asserted by the requestor ID indicated in the PmeRequestorID field. Subsequent PMEs are kept pending until PmeStatus is cleared by writing a 1.
15:0	PmeRequestorId: pme requestor ID. Read-only. This field indicates the PCI requestor ID of the last PME requestor.

D2F[5:1]x7C Device Capability 2

Reset: 0000_0000h.

Bits	Description
31:24	Reserved.
23:22	MaxEndEndTlpPrefixes: Max number of End-End TLP prefixes supported. Read-only. IF (D2F[5:1]x7C[EndEndTlpPrefixSupported]==0) THEN Reserved. ENDIF.

Bits	Definition	Bits	Definition
00b	4 End-End TLP Prefixes.	10b	2 End-End TLP Prefixes.
01b	1 End-End TLP Prefix.	11b	3 End-End TLP Prefixes.

21	EndEndTlpPrefixSupported: End-End TLP Prefix supported. Read-only.
20	ExtendedFmtFieldSupported. Read-only. 1=Supports the 3-bit definition of the Fmt field. 0=Supports the 2-bit definition of the Fmt field. Must be set for functions that support End-End TLP prefixes.
19:18	ObffSupported: optimized buffer flush/fill supported. Read-only.
17:14	Reserved.
13:12	Reserved.
11	LtrSupported: latency tolerance supported. Read-only.
10	Reserved.
9:6	Reserved.
5	AriForwardingSupported. Read-only.
4	CplTimeoutDisSup: completion timeout disable supported. Read-only.
3:0	CplTimeoutRangeSup: completion timeout range supported. Read-only. Fh=Completion timeout range is 64s to 50us.

D2F[5:1]x80 Device Control and Status 2

Reset: 0000_8000h.

Bits	Description																																
31:16	Reserved.																																
15	EndEndTlpPrefixBlocking. Read-only. 1=Forwarding of End-End TLP Prefixes is not supported. This bit is hardwired to 1b.																																
14:13	ObffEn: optimized buffer flush/fill enable. Read-write.																																
12:11	Reserved.																																
10	LtrEn: latency tolerance reporting enable. Read-write.																																
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8	Reserved.																																
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4	CplTimeoutDis: completion timeout disable. Read-write. 1=Completion timeout disabled.																																
3:0	CplTimeoutValue: completion timeout value. Read-write. BIOS: 6h. <table> <thead> <tr> <th>Bits</th> <th>Timeout Range</th> <th>Bits</th> <th>Timeout Range</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>50ms-50us</td> <td>9h</td> <td>900ms-260ms</td> </tr> <tr> <td>1h</td> <td>100us-50us</td> <td>Ah</td> <td>3.5s-1s</td> </tr> <tr> <td>2h</td> <td>10ms-1ms</td> <td>Ch-Bh</td> <td>Reserved</td> </tr> <tr> <td>4h-3h</td> <td>Reserved</td> <td>Dh</td> <td>13s-4s</td> </tr> <tr> <td>5h</td> <td>55ms-16ms</td> <td>Eh</td> <td>64s-4s</td> </tr> <tr> <td>6h</td> <td>210ms-65ms</td> <td>Fh</td> <td>Reserved</td> </tr> <tr> <td>8h-7h</td> <td>Reserved</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Timeout Range	Bits	Timeout Range	0h	50ms-50us	9h	900ms-260ms	1h	100us-50us	Ah	3.5s-1s	2h	10ms-1ms	Ch-Bh	Reserved	4h-3h	Reserved	Dh	13s-4s	5h	55ms-16ms	Eh	64s-4s	6h	210ms-65ms	Fh	Reserved	8h-7h	Reserved		
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4h-3h	Reserved	Dh	13s-4s																														
5h	55ms-16ms	Eh	64s-4s																														
6h	210ms-65ms	Fh	Reserved																														
8h-7h	Reserved																																

D2F[5:1]x84 IO Link Capability 2

Bits	Description
31:9	Reserved.
8	CrossLinkSupported . Read-only. Reset: 0.
7:3	Reserved.
2:1	SupportedLinkSpeed . Read-only. Reset: 3h. Specifies the supported link speeds. Bit 1=2.5GT/s, Bit 2=5.0GT/s.
0	Reserved.

D2F[5:1]x88 IO Link Control and Status 2

Bits	Description																								
31:22	Reserved.																								
21	LinkEqualizationRequest . Read; write-1-to-clear. Reset: 0. 1=Hardware requests link equalization to be performed.																								
20	EqualizationPhase3Success . Read-only. Reset: 0. 1=Phase 3 of the Transmitter Equalization procedure has completed successfully. Write 1 to clear.																								
19	EqualizationPhase2Success . Read-only. Reset: 0. 1=Phase 2 of the Transmitter Equalization procedure has completed successfully. Write 1 to clear.																								
18	EqualizationPhase1Success . Read-only. Reset: 0. 1=Phase 1 of the Transmitter Equalization procedure has completed successfully. Write 1 to clear.																								
17	EqualizationComplete . Read-only. Reset: 0. 1=Transmitter Equalization procedure has completed. Write 1 to clear.																								
16	CurDeemphasisLevel: current deemphasis level . Read-only. Reset: D2F[5:1]xE4_xA4[LcGen2EnStrap]. 1=-3.5 dB. 0=-6 dB																								
15:12	ComplianceDeemphasis: compliance deemphasis . Read-write. Reset: 0. In Gen2 this field defines the compliance deemphasis level when EnterCompliance is set. Software should leave this field in its default state. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>DeEmph=-6 dB, Preshoot=0 dB</td> </tr> <tr> <td>1h</td> <td>DeEmph=-3.5 dB, Preshoot=0 dB</td> </tr> <tr> <td>2h</td> <td>DeEmph=-4.5 dB, Preshoot=0 dB</td> </tr> <tr> <td>3h</td> <td>DeEmph=-2.5 dB, Preshoot=0 dB</td> </tr> <tr> <td>4h</td> <td>DeEmph=-0 dB, Preshoot=0 dB</td> </tr> <tr> <td>5h</td> <td>DeEmph=-0 dB, Preshoot=2 dB</td> </tr> <tr> <td>6h</td> <td>DeEmph=-0 dB, Preshoot=2.5 dB</td> </tr> <tr> <td>7h</td> <td>DeEmph=-6 dB, Preshoot=3.5 dB</td> </tr> <tr> <td>8h</td> <td>DeEmph=-3.5 dB, Preshoot=3.5 dB</td> </tr> <tr> <td>9h</td> <td>DeEmph=-0 dB, Preshoot=3.5 dB</td> </tr> <tr> <td>Fh-Ah</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0h	DeEmph=-6 dB, Preshoot=0 dB	1h	DeEmph=-3.5 dB, Preshoot=0 dB	2h	DeEmph=-4.5 dB, Preshoot=0 dB	3h	DeEmph=-2.5 dB, Preshoot=0 dB	4h	DeEmph=-0 dB, Preshoot=0 dB	5h	DeEmph=-0 dB, Preshoot=2 dB	6h	DeEmph=-0 dB, Preshoot=2.5 dB	7h	DeEmph=-6 dB, Preshoot=3.5 dB	8h	DeEmph=-3.5 dB, Preshoot=3.5 dB	9h	DeEmph=-0 dB, Preshoot=3.5 dB	Fh-Ah	Reserved.
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4h	DeEmph=-0 dB, Preshoot=0 dB																								
5h	DeEmph=-0 dB, Preshoot=2 dB																								
6h	DeEmph=-0 dB, Preshoot=2.5 dB																								
7h	DeEmph=-6 dB, Preshoot=3.5 dB																								
8h	DeEmph=-3.5 dB, Preshoot=3.5 dB																								
9h	DeEmph=-0 dB, Preshoot=3.5 dB																								
Fh-Ah	Reserved.																								
11	ComplianceSOS: compliance SOS . Read-write. Reset: 0. 1=The device transmits skip ordered sets in between the modified compliance pattern.																								

10	EnterModCompliance: enter modified compliance. Read-write. Reset: 0. 1=The device transmits modified compliance pattern. Software should leave this field in its default state.								
9:7	XmitMargin: transmit margin. Read-write. Reset: 0. This field controls the non-deemphasized voltage level at the transmitter pins. Software should leave this field in its default state.								
6	SelectableDeemphasis: selectable deemphasis. Read-only. Reset: D2F[5:1]xE4_xA4[LcGen2EnStrap]. 0=Selectable deemphasis is not supported. 1=Selectable deemphasis supported.								
5	HwAutonomousSpeedDisable: hardware autonomous speed disable. Read-write. Cold reset: 0. 1=Support for hardware changing the link speed for device specific reasons disabled.								
4	EnterCompliance: enter compliance. Read-write. Cold reset: 0. 1=Force the link to enter the compliance mode.								
3:0	TargetLinkSpeed: target link speed. Read-write. Reset: 2h. This field defines the upper limit of the link operational speed. Writes of reserved encodings are not valid. Hardware prevents writes of reserved encodings from changing the state of this field. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> </tr> <tr> <td>1h</td> <td>2.5GT/s</td> </tr> <tr> <td>2h</td> <td>5.0GT/s</td> </tr> </tbody> </table>	Bits	Definition	0h	Reserved	1h	2.5GT/s	2h	5.0GT/s
Bits	Definition								
0h	Reserved								
1h	2.5GT/s								
2h	5.0GT/s								

D2F[5:1]x8C Slot Capability 2

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D2F[5:1]x90 Slot Control and Status 2

Reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D2F[5:1]xA0 MSI Capability Register

Reset: 0000_B005h.

Bits	Description
31:24	Reserved.
23	Msi64bit: MSI 64 bit capability. Read-only. 1=The device is capable of sending 64-bit MSI messages. 0=The device is not capable of sending a 64-bit message address.
22:20	MsiMultiEn: MSI multiple message enable. Read-write. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). When MSI is enabled, a function is allocated at least 1 vector.
19:17	MsiMultiCap: MSI multiple message capability. Read-only. 000b=The device is requesting one vector.

16	MsiEn: MSI enable. Read-write. 1=MSI generation is enabled and INTx generation is disabled. 0=MSI generation disabled and INTx generation is enabled.
15:8	NextPtr: next pointer. Read-only.
7:0	CapID: capability ID. Read-only. 05h=MSI capability structure.

D2F[5:1]xA4 MSI Message Address Low

Reset: 0000_0000h.

Bits	Description
31:2	MsiMsgAddrLo: MSI message address. Read-write. This register specifies the dword aligned address for the MSI memory write transaction.
1:0	Reserved.

D2F[5:1]xA8 MSI Message Address High

Reset: 0000_0000h.

Bits	Description
31:0	MsiMsgAddrHi: MSI message address. Read-write. This register specifies the upper 32-bits of the MSI address.

D2F[5:1]xAC MSI Message Data

Reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15:0	MsiData: MSI message data. Read-write. This register specifies lower 16 bits of data for the MSI memory write transaction. The upper 16 bits are always 0.

D2F[5:1]xB0 Subsystem and Subvendor Capability ID Register

Reset: 0000_B80Dh.

Bits	Description
31:16	Reserved.
15:8	NextPtr: next pointer. Read-only.
7:0	CapID: capability ID. Read-only.

D2F[5:1]xB4 Subsystem and Subvendor ID Register

Reset: 0000_0000h.

Bits	Description
31:16	SubsystemID. Read-only.
15:0	SubsystemVendorID. Read-only.

D2F[5:1]xB8 MSI Capability Mapping

Reset: A803_0008h.

Bits	Description
31:27	CapType: capability type. Read-only.
26:18	Reserved.
17	FixD. Read-only.
16	En. Read-only.
15:8	NextPtr: next pointer. Read-only.
7:0	CapID: capability ID. Read-only.

D2F[5:1]xBC MSI Mapping Address Low

Bits	Description
31:20	MsiMapAddrLo. Read-only. Reset: 0. Lower 32-bits of the MSI address.
19:0	Reserved.

D2F[5:1]xC0 MSI Mapping Address High

Bits	Description
31:0	MsiMapAddrHi. Read-only. Reset: 0. Upper 32-bits of the MSI address.

D2F[5:1]xE0 Root Port Index

Reset: 0000_0000h.

The index/data pair registers, [D2F\[5:1\]xE0](#) and [D2F\[5:1\]xE4](#), are used to access the registers at [D2F\[5:1\]xE4_x\[FF:00\]](#). To access any of these registers, the address is first written into the index register, [D2F\[5:1\]xE0](#), and then the data is read from or written to the data register, [D2F\[5:1\]xE4](#).

Bits	Description
31:8	Reserved.
7:0	PcieIndex. Read-write.

D2F[5:1]xE4 Root Port DataSee [D2F\[5:1\]xE0](#). Address: [D2F\[5:1\]xE0\[PcieIndex\]](#).

Bits	Description
31:0	PcieData. Read-write.

D2F[5:1]xE4_x20 Root Port TX Control

Reset: 0050_8000h.

Bits	Description
15	TxFlushTlpDis: TLP flush disable. Read-write. 1=Disable flushing TLPs when the link is down.

D2F[5:1]xE4_x50 Root Port Lane Status

Reset: 0000_0000h.

Bits	Description																				
31:7	Reserved.																				
6:1	PhyLinkWidth: port link width. Read-only; updated-by-hardware. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00_0000b</td> <td>disabled</td> <td>00_1000b</td> <td>x8</td> </tr> <tr> <td>00_0001b</td> <td>x1</td> <td>01_0000b</td> <td>x12</td> </tr> <tr> <td>00_0010b</td> <td>x2</td> <td>10_0000b</td> <td>x16</td> </tr> <tr> <td>00_0100b</td> <td>x4</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00_0000b	disabled	00_1000b	x8	00_0001b	x1	01_0000b	x12	00_0010b	x2	10_0000b	x16	00_0100b	x4		
Bits	Definition	Bits	Definition																		
00_0000b	disabled	00_1000b	x8																		
00_0001b	x1	01_0000b	x12																		
00_0010b	x2	10_0000b	x16																		
00_0100b	x4																				
0	PortLaneReversal: port lane reversal. Read-only. 1=Port lanes order is reversed.																				

D2F[5:1]xE4_x6A Root Port Error Control

Reset: 0000_0500h.

Bits	Description
0	ErrReportingDis: advanced error reporting disable. Read-write. BIOS: 1. 1=Error reporting disabled. 0=Error reporting enabled.

D2F[5:1]xE4_x70 Root Port Receiver Control

Reset: 0188_4000h.

Bits	Description																				
19	RxCbCplTimeoutMode: RCB completion timeout mode. Read-write. BIOS: 1. 1=Timeout on link down.																				
18:16	RxCbCplTimeout: RCB completion timeout. Read-write. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Disabled</td> <td>100b</td> <td>50ms</td> </tr> <tr> <td>001b</td> <td>50us</td> <td>101b</td> <td>100ms</td> </tr> <tr> <td>010b</td> <td>10ms</td> <td>110b</td> <td>500ms</td> </tr> <tr> <td>011b</td> <td>25ms</td> <td>111b</td> <td>1ms</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	Disabled	100b	50ms	001b	50us	101b	100ms	010b	10ms	110b	500ms	011b	25ms	111b	1ms
Bits	Definition	Bits	Definition																		
000b	Disabled	100b	50ms																		
001b	50us	101b	100ms																		
010b	10ms	110b	500ms																		
011b	25ms	111b	1ms																		

D2F[5:1]xE4_xA0 Per Port Link Controller (LC) Control

Reset: 4000_0030h.

Bits	Description			
23	LcL1ImmediateAck: immediate ACK ASPM L1 entry. Read-write. BIOS: 1. 1=Alwyas ACK ASPM L1 entry DLLPs.			
15:12	LcL1Inactivity: L1 inactivity timer. Read-write.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	0h	L1 disabled	8h	400us
	1h	1us	9h	1ms
	2h	2us	Ah	40us
	3h	4us	Bh	10ms
	4h	10us	Ch	40ms
	5h	20us	Dh	100ms
	6h	40us	Eh	400ms
	7h	100us	Fh	reserved
11:8	LcL0sInactivity: L0s inactivity timer. Read-write.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	0h	L0s disabled	8h	4us
	1h	40ns	9h	10us
	2h	80ns	Ah	40us
	3h	120ns	Bh	100us
	4h	200ns	Ch	400us
	5h	400ns	Dh	1ms
	6h	1us	Eh	4ms
	7h	2us	Fh	reserved
7:4	Lc16xClearTxPipe. Read-write. BIOS: 3h. Specifies the number of clock to drain the TX pipe.			

D2F[5:1]xE4_xA1 LC Training Control

Reset: 5400_1880h.

Bits	Description			
11	LcDontGotoL0sifL1Armed: prevent Ls0 entry is L1 request in progress. Read-write. BIOS: 1. 1=Prevent the LTSSM from transitioning to Rcv_L0s if an acknowledged request to enter L1 is in progress.			

D2F[5:1]xE4_xA2 LC Link Width Control

Reset: 00A0_0006h.

Bits	Description			
31:24	Reserved.			
22:21	LcDynLanesPwrState: unused link power state. Read-write. Controls the state of unused links after a reconfiguration.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	00b	on	10b	SB2
	01b	SB1	11b	Off

20	LcUpconfigCapable: upconfigure capable. Read-only; updated-by-hardware. 1=Both ends of the link are upconfigure capable. 0=Both ends of the link are not upconfigure capable.																				
13	LcUpconfigureDis: upconfigure disable. Read-write. 1=Disable link upconfigure.																				
12	LcUpconfigureSupport: upconfigure support. Read-write.																				
11	LcShortReconfigEn: short re-configuration enable. Read-write. 1=Enable short link re-configuration																				
10	LcRenegotiateEn: link reconfiguration enable. Read-write. 1=Enable link re-negotiation.																				
9	LcRenegotiationSupport: re-negotiation support. Read-only; updated-by-hardware. 1=Link re-negotiation not supported by the downstream device.																				
8	LcReconfigNow: re-configure link. Read-write; cleared-when-done. 1=Initiate link width change.																				
7	LcReconfigArcMissingEscape. Read-write. 1=Expedite transition from Recovery.Idle to Detect during a long reconfiguration.																				
6:4	LcLinkWidthRd: current link width. Read-only; updated-by-hardware. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> <td>100b</td> <td>8</td> </tr> <tr> <td>001b</td> <td>1</td> <td>101b</td> <td>12</td> </tr> <tr> <td>010b</td> <td>2</td> <td>110b</td> <td>16</td> </tr> <tr> <td>011b</td> <td>4</td> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	0	100b	8	001b	1	101b	12	010b	2	110b	16	011b	4	111b	Reserved
Bits	Definition	Bits	Definition																		
000b	0	100b	8																		
001b	1	101b	12																		
010b	2	110b	16																		
011b	4	111b	Reserved																		
3	Reserved.																				
2:0	LcLinkWidth: link width required. Read-write. See: LcLinkWidthRd.																				

D2F[5:1]xE4_xA3 LC Number of FTS Control

Reset: 00FF_020Ch.

Bits	Description
9	LcXmitFtsBeforeRecovery: transmit FTS before recovery. Read-write. 1=Transmit FTS before recovery.

D2F[5:1]xE4_xA4 LC Link Speed Control

Reset: 0440_0100h.

Bits	Description
27	LcMultUpstreamAutoSpdChngEn: enable multiple automatic speed changes. Read-write. 1=Enable multiple automatic speed changes when D2F[5:1]xE4_xC0[StrapAutoRcSpeedNegotiationDis]=0 and no failures occurred in previous speed change attempts.
19	LcOtherSideSupportsGen2: downstream link supports gen2. Read-only; updated-by-hardware. 1=The downstream link currently supports gen2.
12	LcSpeedChangeAttemptFailed: speed change attempt failed. Read-only; updated-by-hardware. 1=LcSpeedChangeAttemptsAllowed has been reached. This bit and the related counter can be cleared using the LcClrFailedSpdChangeCnt bit.
9	LcInitiateLinkSpeedChange: initiate link speed change. Read-write; cleared-when-done. 1=Initiate link speed negotiation.

6	LcForceDisSwSpeedChange: force disable software speed changes. Read-write. 1=Force the PCIe core to disable speed changes initiated by private registers.
0	LcGen2EnStrap: Gen2 PCIe support enable. Read-write. 1=Gen2 PCIe support enabled. 0=Gen2 PCIe support disabled.

D2F[5:1]xE4_xA5 LC State 0

Cold reset: 0000_0000h.

Bits	Description
31:30	Reserved.
29:24	LcPrevState3: previous link state 3. Read-only; updated-by-hardware. See: Table 99 [Link controller state encodings] .
23:22	Reserved.
21:16	LcPrevState2: previous link state 2. Read-only; updated-by-hardware. See: Table 99 [Link controller state encodings]
15:14	Reserved.
13:8	LcPrevState1: previous link state 1. Read-only; updated-by-hardware. See: Table 99 [Link controller state encodings] .
7:6	Reserved.
5:0	LcCurrentState: current link state. Read-only; updated-by-hardware. See: Table 99 [Link controller state encodings] .

Table 99: Link controller state encodings

Bits	Description	Bits	Description	Bits	Description
00h	s_Detect_Quiet.	12h	Rcv_L0_and_Tx_L0s.	24h	s_Rcvd_Loopback.
01h	s_Start_common_Mode.	13h	Rcv_L0_and_Tx_L0s_FTS.	25h	s_Rcvd_Loopback_Idle.
02h	s_Check_Common_Mode.	14h	Rcv_L0s_and_Tx_L0.	26h	s_Rcvd_Reset_Idle.
03h	s_Rcvr_Detect.	15h	Rcv_L0s_and_Tx_L0_Idle.	27h	s_Rcvd_Disable_Entry.
04h	s_No_Rcvr_Loop	16h	Rcv_L0s_and_Tx_L0s.	28h	s_Rcvd_Disable_Idle.
05h	s_Poll_Quiet.	17h	Rcv_L0s_and_Tx_L0s_FTS.	29h	s_Rcvd_Disable.
06h	s_Poll_Active.	18h	s_L1_Entry.	2Ah	s_Detect_Idle.
07h	s_Poll_Compliance.	19h	s_L1_Idle.	2Bh	s_L23_Wait.
08h	s_Poll_Config.	1Ah	s_L1_Wait	2Ch	Rcv_L0s_Skp_and_Tx_L0.
09h	s_Config_Step1.	1Bh	s_L1.	2Dh	Rcv_L0s_Skp_and_Tx_L0_Idle.
0Ah	s_Config_Step3.	1Ch	s_L23_Stall.	2Eh	Rcv_L0s_Skp_and_Tx_L0s.
0Bh	s_Config_Step5.	1Dh	s_L23_Entry.	2Fh	Rcv_L0s_Skp_and_Tx_L0_FTS.
0Ch	s_Config_Step2.	1Eh	s_L23_Entry.	30h	s_Config_Step2b.
0Dh	s_Config_Step4.	1Fh	s_L23_Ready.	31h	s_Recovery_Speed.
0Eh	s_Config_Step6.	20h	s_Recovery_lock.	32h	s_Poll_Compliance_Idle.
0Fh	s_Config_Idle.	21h	s_Recovery_Config.	33h	s_Rcvd_Loopback_Speed.
10h	Rcv_L0_and_Tx_L0.	22h	s_Recovery_Idle.	3Fh-34h	Reserved.
11h	Rcv_L0_and_Tx_L0_Idle.	23h	s_Training_Bit.		

D2F[5:1]xE4_xB1 LC Control 2

Reset: 8608_0280h.

Bits Description

20	LcBlockEIIdleinL0: block electrical idle in L0. Read-write. BIOS: 1. 1=Prevent electrical idle from causing the receiver to transition from L0 to L0s.
19	LcDeassertRxEnInL0s: deassert RX_EN in L0s. Read-write. 1=Turn off transmitters in L0s.

D2F[5:1]xE4_xB5 LC Control 3

Reset: 2850_5020h.

Bits Description

30	LcGoToRecovery: go to recovery. Read-write. 1=Force link in the L0 state to transition to the Recovery state.
3	LcRcvdDeemphasis: received deemphasis. Read-only; updated-by-hardware. Deemphasis advertised by the downstream device. 1=3.5dB. 0=6dB.
2:1	LcSelectDeemphasisCntl: deemphasis control. Read-write. Specifies the deemphasis used by the transmitter. Bits Definition <u>00b</u> Use deemphasis from LcSelectDeemphasis. 01b Use deemphasis advertised by the downstream device. 10b 6dB 11b 3.5dB
0	LcSelectDeemphasis: downstream deemphasis. Read-write. Specifies the downstream deemphasis. 1=3.5dB. 0=6dB.

D2F[5:1]xE4_xC0 LC Strap Override

Reset: 0000_0000h.

Bits Description

15	StrapAutoRcSpeedNegotiationDis: autonomous speed negotiation disable strap override. Read-write. 1=Disable autonomous root complex speed negotiation to Gen2.
13	StrapForceCompliance: force compliance strap override. Read-write.

D2F[5:1]xE4_xC1 Root Port Miscellaneous Strap Override

Reset: 0000_0000h.

Bits Description

31:6	Reserved.
5	StrapLtrSupported. Read-write.
4:3	StrapObffSupported. Read-write.

2	StrapExtendedFmtSupported: Extended Fmt Supported strap override. Read-write.
1	StrapE2EPrefixEn: E2E Prefix En strap override. Read-write.
0	StrapReverseLanes: reverse lanes strap override. Read-write.

D2F[5:1]xE4_xD0 Root Port ECC Skip OS Feature

Reset: 0000_0100h.

Bits	Description
31:16	BchEccErrorStatus. Read-write. Indicates that lane errors are above the specified threshold. (One bit per lane.)
15:8	BchEccErrorThreshold. Read-write. Error threshold.
7:1	Reserved.
0	StrapBchEccEn. Read-write.

D2F[5:1]x100 Vendor Specific Enhanced Capability Register

Bits	Description
31:20	NextPtr: next pointer. Read-only. IF (D0F0xE4_x0140_00B0 [StrapF0VcEn] == 1) THEN Reset: 110h. ELSEIF (D0F0xE4_x0140_00B0 [StrapF0DsnEn] == 1) THEN Reset: 140h. ELSEIF (D0F0xE4_x0140_00B0 [StrapF0AerEn] == 1) THEN Reset: 150h. ELSEIF (D0F0xE4_x0140_00C1 [StrapGen3Compliance] == 1) THEN 270h. ELSEIF (D0F0xE4_x0140_00B0 [StrapF0AcsEn] == 1) THEN 2A0h. ELSE Reset: 000h. ENDIF.
19:16	CapVer: capability version. Read-only. Reset: 1h.
15:0	CapID: capability ID. Read-only. Reset: Bh.

D2F[5:1]x104 Vendor Specific Header Register

Reset: 0101_0001h.

Bits	Description
31:20	VsecLen: vendor specific enhanced capability structure length. Read-only. Defined the number of bytes of the entire vendor specific enhanced capability structure including the header.
19:16	VsecRev: vendor specific enhanced capability version. Read-only.
15:0	VsecID: vendor specific enhanced capability ID. Read-only.

D2F[5:1]x108 Vendor Specific 1 Register

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write. This field does not control any hardware.

D2F[5:1]x10C Vendor Specific 2 Register

Reset: 0000_0000h.

Bits	Description
31:0	Scratch: scratch. Read-write. This field does not control any hardware.

D2F[5:1]x128 Virtual Channel 0 Resource Status Register

Reset: 0002_0000h.

Bits	Description
31:18	Reserved.
17	VcNegotiationPending: virtual channel negotiation pending. Read-only; updated-by-hardware. 1=Virtual channel negotiation in progress. This bit must be 0 before the virtual channel can be used.
16	PortArbTableStatus: port arbitration table status. Read-only.
15:0	Reserved.

D2F[5:1]x150 Advanced Error Reporting Capability

Bits	Description
31:20	NextPtr: next pointer. Read-only. IF (D0F0xE4_x0140_00C1 [StrapGen3Compliance] == 1) THEN 270h. ELSEIF (D0F0xE4_x0140_00B0 [StrapF0AcsEn] == 1) THEN 2A0h. ELSE Reset: 000h. ENDIF.
19:16	CapVer: capability version. Read-only. Reset: 2h.
15:0	CapID: capability ID. Read-only. Reset: 1h.

D2F[5:1]x154 Uncorrectable Error Status

Cold reset: 0000_0000h.

Bits	Description
31:26	Reserved.
25	TlpPrefixStatus: TLP prefix blocked status. Read; Write-1-to-clear.
24	AtomicOpEgressBlockedTLPStatus: atomic op egress blocked TLP status. Read; Write-1-to-clear.
23	McBlockedTLPStatus: MC blocked TLP status. Read; Write-1-to-clear.

22	UncorrInteralErrStatus: uncorrectable internal error status. Read; Write-1-to-clear.
21	AcsViolationStatus: access control service status. Read; Write-1-to-clear.
20	UnsuppReqErrStatus: unsupported request error status. Read; Write-1-to-clear. The header of the unsupported request is logged.
19	EcrcErrStatus: end-to-end CRC error status. Read; Write-1-to-clear.
18	MalTlpStatus: malformed TLP status. Read; Write-1-to-clear. The header of the malformed TLP is logged.
17	RevOvflStatus: receiver overflow status. Read-only.
16	UnexpCplStatus: unexpected completion timeout status. Read; Write-1-to-clear. The header of the unexpected completion is logged.
15	CplAbortErrStatus: completer abort error status. Read; Write-1-to-clear.
14	CplTimeoutStatus: completion timeout status. Read; Write-1-to-clear.
13	FcErrStatus: flow control error status. Read-only.
12	PsnErrStatus: poisoned TLP status. Read; Write-1-to-clear. The header of the poisoned transaction layer packet is logged.
11:6	Reserved.
5	SurprdnErrStatus: surprise down error status. Read-only. 0=Detection and reporting of surprise down errors is not supported.
4	DlpErrStatus: data link protocol error status. Read; Write-1-to-clear.
3:0	Reserved.

D2F[5:1]x158 Uncorrectable Error Mask

Cold reset: 0000_0000h.

Bits	Description
31:26	Reserved.
25	TlpPrefixMask: TLP prefix blocked mask. Read-only.
24	AtomicOpEgressBlockedTLPMask: atomic op egress blocked TLP mask. Read-only.
23	McBlockedTLPMask: MC blocked TLP mask. Read-only.
22	UncorrInteralErrMask: uncorrectable internal error mask. Read-write.
21	AcsViolationMask: access control service mask. IF (D0F0xE4_x0140_00B0[StrapF0AcsEn] ==1) THEN Read-write. ELSE Read-only. ENDIF. 1=ACS violation errors are not reported.
20	UnsuppReqErrMask: unsupported request error mask. Read-write. 1=Unsupported request errors are not reported.
19	EcrcErrMask: end-to-end CRC error mask. Read-write.
18	MalTlpMask: malformed TLP mask. Read-write. 1=Malformed TLP errors are not reported.
17	RevOvflMask: receiver overflow mask. Read-only.
16	UnexpCplMask: unexpected completion timeout mask. Read-write. 1=Unexpected completion errors are not reported.
15	CplAbortErrMask: completer abort error mask. Read-write.

14	CplTimeoutMask: completion timeout mask. Read-write. 1=Completion timeout errors are not reported.
13	FcErrMask: flow control error mask. Read-only.
12	PsnErrMask: poisoned TLP mask. Read-write. 1=Poisoned TLP errors are not reported.
11:6	Reserved.
5	SurprdnErrMask: surprise down error mask. Read-only.
4	DlpErrMask: data link protocol error mask. Read-write. 1=Data link protocol errors are not reported.
3:0	Reserved.

D2F[5:1]x15C Uncorrectable Error Severity

Cold reset: 0006_2030h.

Bits	Description
31:26	Reserved.
25	TlpPrefixSeverity: TLP prefix blocked severity. Read-only.
24	AtomicOpEgressBlockedTLPSeverity: atomic op egress blocked TLP severity. Read-only.
23	McBlockedTLPSeverity: MC blocked TLP severity. Read-only.
22	UncorrInternalErrSeverity: uncorrectable internal error severity. Read-only.
21	AcsViolationSeverity: access control service severity. IF (D0F0xE4_x0140_00B0[StrapF0AcsEn]==1) THEN Read-write. ELSE Read-only. ENDIF. 1=Fatal error. 0=Non-fatal error.
20	UnsuppReqErrSeverity: unsupported request error severity. Read-write. 1=Fatal error. 0=Non-fatal error.
19	EcrcErrSeverity: end-to-end CRC error severity. Read-only.
18	MalTlpSeverity: malformed TLP severity. Read-write. 1=Fatal error. 0=Non-fatal error.
17	RcvOvflSeverity: receiver overflow severity. Read-only.
16	UnexpCplSeverity: unexpected completion timeout severity. Read-write. 1=Fatal error. 0=Non-fatal error.
15	CplAbortErrSeverity: completer abort error severity. Read-only.
14	CplTimeoutSeverity: completion timeout severity. Read-write. 1=Fatal error. 0=Non-fatal error.
13	FcErrSeverity: flow control error severity. Read-only.
12	PsnErrSeverity: poisoned TLP severity. Read-write. 1=Fatal error. 0=Non-fatal error.
11:6	Reserved.
5	SurprdnErrSeverity: surprise down error severity. Read-only.
4	DlpErrSeverity: data link protocol error severity. Read-write. 1=Fatal error. 0=Non-fatal error.
3:0	Reserved.

D2F[5:1]x160 Correctable Error Status

Cold reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15	HdrLogOvflStatus: header log overflow status. Read-only.
14	CorrIntErrStatus: corrected internal error status. Read; Write-1-to-clear.
13	AdvisoryNonfatalErrStatus: advisory non-fatal error status. Read; Write-1-to-clear. 1=A non-fatal unsupported request errors or a non-fatal unexpected completion errors occurred.
12	ReplayTimerTimeoutStatus: replay timer timeout status. Read; Write-1-to-clear.
11:9	Reserved.
8	ReplayNumRolloverStatus: replay. Read; Write-1-to-clear. 1=The same transaction layer packet has been replayed three times and has caused the link to re-train.
7	BadDlppStatus: bad data link layer packet status. Read; Write-1-to-clear. 1=A link CRC error was detected.
6	BadTlpStatus: bad transaction layer packet status. Read; Write-1-to-clear. 1=A bad non-duplicated sequence ID or a link CRC error was detected.
5:1	Reserved.
0	RcvErrStatus: receiver error status. Read-only. 1=An 8B10B or disparity error was detected.

D2F[5:1]x164 Correctable Error Mask

Cold reset: 0000_6000h.

Bits	Description
31:16	Reserved.
15	HdrLogOvflMask: header log overflow mask. Read-only.
14	CorrIntErrMask: corrected internal error mask. Read-write.
13	AdvisoryNonfatalErrMask: advisory non-fatal error mask. Read-write. 1=Error is not reported.
12	ReplayTimerTimeoutMask: replay timer timeout mask. Read-write. 1=Error is not reported.
11:9	Reserved.
8	ReplayNumRolloverMask: replay. Read-write. 1=Error is not reported.
7	BadDlppMask: bad data link layer packet mask. Read-write. 1=Error is not reported.
6	BadTlpMask: bad transaction layer packet mask. Read-write. 1=Error is not reported.
5:1	Reserved.
0	RcvErrMask: receiver error mask. Read-only. 1=Error is not reported.

D2F[5:1]x168 Advanced Error Control

Cold reset: 0000_0000h.

Bits	Description
31:12	Reserved.

11	TlpPrefixLogPresent. Read-only. IF (D2F[5:1]x7C[EndEndTlpPrefixSupported]==0) THEN Reserved. ENDIF. 1=If FirstErrPtr is valid then the TLP Prefix Log register contains valid information.
10	MultiHdrRecdEn. Read-only. 1=Enables recording more than one error header.
9	MultiHdrRecdCap. Read-only. 1=Specifies that the function is capable of recording more than one error header.
8	EcrcCheckEn: data link protocol error severity. Read-write. 0=Specifies that End-to-end CRC generation is not supported.
7	EcrcCheckCap: data link protocol error severity. Read-only. 0=Specifies that end-to-end CRC check is not supported.
6	EcrcGenEn: end-to-end CRC enable. Read-only. 0=Specifies that End-to-end CRC generation is not supported.
5	EcrcGenCap: end-to-end CRC capability. Read-only. 0=Specifies that end-to-end CRC generation is not supported.
4:0	FirstErrPtr: first error pointer. Read-only. The First Error Pointer identifies the bit position of the first error reported in the Uncorrectable Error Status register.

D2F[5:1]x16C Header Log DW0

Cold reset: 0000_0000h.

Bits	Description
31:0	TlpHdr: transaction layer packet header log. Read-only. Contains the header for a transaction layer packet corresponding to a detected error. The upper byte represents byte 0 of the header.

D2F[5:1]x170 Header Log DW1

Cold reset: 0000_0000h.

Bits	Description
31:0	TlpHdr: transaction layer packet header log. Read-only. Contains the header for a transaction layer packet corresponding to a detected error. The upper byte represents byte 4 of the header.

D2F[5:1]x174 Header Log DW2

Cold reset: 0000_0000h.

Bits	Description
31:0	TlpHdr: transaction layer packet header log. Read-only. Contains the header for a transaction layer packet corresponding to a detected error. The upper byte represents byte 8 of the header.

D2F[5:1]x178 Header Log DW3

Cold reset: 0000_0000h.

Bits	Description
31:0	TlpHdr: transaction layer packet header log. Read-only. Contains the header for a transaction layer packet corresponding to a detected error. The upper byte represents byte 12 of the header.

D2F[5:1]x17C Root Error Command

Reset: 0000_0000h.

Bits	Description
31:3	Reserved.
2	FatalErrRepEn: fatal error reporting enable. Read-write. 1=Enables the generation of an interrupt when a fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
1	NonfatalErrRepEn: non-fatal error reporting enable. Read-write. 1=Enables generation of an interrupt when a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port.
0	CorrErrRepEn: correctable error reporting enable. Read-write. 1=Enables generation of an interrupt when a correctable error is reported by any of the devices in the hierarchy associated with this Root Port.

D2F[5:1]x180 Root Error Status

Cold reset: 0000_0000h.

Bits	Description
31:27	AdvErrIntMsgNum: advanced error interrupt message number. Read-only.
26:7	Reserved.
6	NFatalErrMsgRcvd: fatal error message received. Read; Write-1-to-clear. Set to 1 when one or more fatal uncorrectable error messages have been received.
5	NonFatalErrMsgRcvd: non-fatal error message received. Read; Write-1-to-clear. Set to 1 when one or more non-fatal uncorrectable error messages have been received.
4	FirstUncorrFatalRcvd: first uncorrectable fatal error message received. Read; Write-1-to-clear. Set to 1 when the first uncorrectable error message received is for a fatal error.
3	MultErrFatalNonfatalRcvd: ERR_FATAL/NONFATAL message received. Read; Write-1-to-clear. Set when either a fatal or a non-fatal error is received and ErrFatalNonfatalRcvd is already set.
2	ErrFatalNonfatalRcvd: ERR_FATAL/NONFATAL message received. Read; Write-1-to-clear. Set when either a fatal or a non-fatal error is received and this bit is not already set.
1	MultErrCorrRcvd: multiple ERR_COR messages received. Read; Write-1-to-clear. Set when a correctable error message is received and ErrCorrRcvd is already set.
0	ErrCorrRcvd: ERR_COR message received. Read; Write-1-to-clear. Set when a correctable error message is received and this bit is not already set.

D2F[5:1]x184 Error Source ID

Cold reset: 0000_0000h.

Bits	Description
31:16	ErrFatalNonfatalSrcID: ERR_FATAL/ERR_NONFATAL source identification. Read-only. Loaded with the requestor ID indicated in the received ERR_FATAL or ERR_NONFATAL message when D2F[5:1]x180 [ErrFatalNonfatalRcvd] is not already set.
15:0	ErrCorlSrcID: ERR_COR source identification. Read-only. Loaded with the requestor ID indicated in the received ERR_COR message when D2F[5:1]x180 [ErrCorrRcvd] is not already set.

3.9 Device 18h Function 0 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1530h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F0x04 Status/Command

Bits	Description
31:16	Status. Read-only. Value: 0010h. Bit[20] is set to indicate the existence of a PCI-defined capability block.
15:0	Command. Read-only. Value: 0000h.

D18F0x08 Class Code/Revision ID

Bits	Description
31:8	ClassCode. Read-only. Value: 060000h. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only. Value: 00h.

D18F0x0C Header Type

Read-only. Value: 0080_0000h.

Bits	Description
31:0	HeaderTypeReg. These bits are fixed at their default values. The header type field indicates that there are multiple functions present in this device.

D18F0x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Value: 00h.

D18F0x[5C:40] Routing Table

Reset: 0004_0201h. As each packet is processed by the node, it is routed to the appropriate links, or remains in the node that is processing the packet, based on the source/destination node and the type of packet being pro-

cessed. The destination of requests and responses determines which of these eight registers is used to route the packet; the source of probes and broadcasts determines which of these eight registers is used to route the packet. Once the routing table register is identified, the packet is routed to the destinations based on the state of the field (in that routing table register) that corresponds to the packet type.

Table 100: Register Mapping for D18F0x[5C:40]

Register	Function
D18F0x40	Node 0
D18F0x[5C:44]	Reserved

Bits	Description

D18F0x60 Node ID

Bits	Description										
20:16	CpuCnt[4:0]: CPU count bits[4:0]. Read-write. Reset: 0. Specifies the number of cores to be enabled (the boot core plus those cores enabled through D18F0x1DC[CpuEn]). <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>1 core</td> </tr> <tr> <td>02h-01h</td> <td><CpuCnt[4:0] + 1> cores</td> </tr> <tr> <td>03h</td> <td>4 cores</td> </tr> <tr> <td>1Fh-04h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00h	1 core	02h-01h	<CpuCnt[4:0] + 1> cores	03h	4 cores	1Fh-04h	Reserved
Bits	Description										
00h	1 core										
02h-01h	<CpuCnt[4:0] + 1> cores										
03h	4 cores										
1Fh-04h	Reserved										

D18F0x64 Unit ID

Reset: 0000_00E0h.

Bits	Description
31:16	Reserved.
15:11	Reserved. Read-write.
10:8	Reserved. Read-write.
7:6	HbUnit: host bridge Unit ID. Read-only. Specifies the coherent link Unit ID of the host bridge used by the coherent fabric.
5:4	MctUnit: memory controller Unit ID. Read-only. Specifies the coherent link Unit ID of the memory controller.
3:0	Reserved.

D18F0x68 Link Transaction Control

Bits	Description										
31	Reserved. Read-write.										
30:28	Reserved. Read-write.										
27:26	Reserved.										
25	Reserved. Read-write.										
24	Reserved. Read-write.										
23	InstallStateS . Read-write. Reset: 0. 1=Forces the default read block (RdBlk) install state to be shared instead of exclusive.										
22:21	DsNpReqLmt: downstream non-posted request limit . Read-write. Reset: 00b. BIOS: 10b. Note: RS880 chipsets set this to 01b due to a chipset issue; this issue has been fixed in all chipsets after the RS880. This specifies the maximum number of downstream non-posted requests issued by core(s) which may be outstanding on the IO links attached to this node at one time. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No limit</td> </tr> <tr> <td>01b</td> <td>limited to 1</td> </tr> <tr> <td>10b</td> <td>limited to 4</td> </tr> <tr> <td>11b</td> <td>limited to 8</td> </tr> </tbody> </table>	Bits	Description	00b	No limit	01b	limited to 1	10b	limited to 4	11b	limited to 8
Bits	Description										
00b	No limit										
01b	limited to 1										
10b	limited to 4										
11b	limited to 8										
20	SeqIdSrcNodeEn: sequence ID source node enable . Read-write. Reset: 0. 1=The source node ID of requests is provided in the SeqID field of the corresponding downstream IO link request packets. This may be useful for debug applications, in order to match downstream packets with their originating node. For normal operation, this bit should be cleared. Correct ordering of requests between different nodes is not ensured when this bit is set. Semaphore sharing between differing nodes may not work properly in systems which are capable of processing IO requests with differing non-zero SeqIds out of request order.										
19	ApicExtSpur: APIC extended spurious vector enable . Read-write. Reset: 0. This enables the extended APIC spurious vector functionality; it affects APICF0[Vector]. 0=The lower 4 bits of the spurious vector are read-only 1111b. 1=The lower 4 bits of the spurious vector are writable.										
18	ApicExtId: APIC extended ID enable . Read-write. Reset: 0. Enables the extended APIC ID functionality. 0=APIC ID is 4 bits. 1=APIC ID is 8 bits.										
17	ApicExtBrdCst: APIC extended broadcast enable . Read-write. Reset: 0. Enables the extended APIC broadcast functionality. 0=APIC broadcast is 0Fh. 1=APIC broadcast is FFh. If ApicExtBrdCst=1 then software must assert ApicExtId.										
16	LintEn: local interrupt conversion enable . Read-write. Reset: 0. 1=Enables the conversion of broadcast ExtInt and NMI interrupt requests to LINT0 and LINT1 local interrupts, respectively, before delivering to the local APIC. This conversion only takes place if the local APIC is hardware enabled. LINT0 and LINT1 are controlled by APIC3[60:50]. 0=ExtInt/NMI interrupts delivered unchanged.										
15	LimitCldtCfg: limit coherent link configuration space range . Read-write. Reset: 0. BIOS: 1.										

14:13	Reserved. Read-write.
12	Reserved. Read-write.
11	RespPassPW: response PassPW. Read-write. Reset: 0. BIOS: 1. 1=The PassPW bit in all downstream link responses is set, regardless of the originating request packet. This technically breaks the PCI ordering rules but it is not expected to be an issue in the downstream direction. Setting this bit improves the latency of upstream requests by allowing the downstream responses to pass posted writes. 0=The PassPW bit in downstream responses is based on the RespPassPW bit of the original request.
10	DisFillP: disable fill probe. Read-write. Reset: 0. Controls probes for core-generated fills. 0=Probes issued for cache fills. 1=Probes not issued for cache fills. BIOS: 0. BIOS may set if single core.
9	DisRmtPMemC: disable remote probe memory cancel. Read-write. Reset: 0. 1=Only probed caches on the same node as the target memory controller may generate MemCancel coherent link packets. MemCancels are used to attempt to save DRAM and/or link bandwidth associated with the transfer of stale DRAM data. 0=Probes hitting dirty blocks may generate MemCancel packets, regardless of the location of the probed cache.
8	DisPMemC: disable probe memory cancel. Read-write. Reset: 0. Controls generation of MemCancel coherent link packets. MemCancels are used to attempt to save DRAM and/or coherent link bandwidth associated with the transfer of stale DRAM data. 0=Probes hitting dirty blocks of the core cache may generate MemCancel packets. 1=Probes may not generate MemCancel packets.
7	CPURdRspPassPW: CPU read response PassPW. Read-write. Reset: 0. 1=Read responses to core-generated reads are allowed to pass posted writes. 0=core responses do not pass posted writes. This bit is not expected to be set. This bit may only be set during the boot process.
6	CPUReqPassPW: CPU request PassPW. Read-write. Reset: 0. 1=Core-generated requests are allowed to pass posted writes. 0=Core requests do not pass posted writes. This bit is not expected to be set. This bit may only be set during the boot process.
5	Reserved.
4	DisMTS: disable memory controller target start. Read-write. Reset: 0. BIOS: 1. 1=Disables use of TgtStart. TgtStart is used to improve scheduling of back-to-back ordered transactions by indicating when the first transaction is received and ordered at the memory controller.
3	DisWrDwP: disable write doubleword probes. Read-write. Reset: 0. BIOS: 1. 1=Disables generation of probes for core-generated, WrSized doubleword commands.
2	DisWrBP: disable write byte probes. Read-write. Reset: 0. BIOS: 1. 1=Disables generation of probes for core-generated, WrSized byte commands.
1	DisRdDwP: disable read doubleword probe. Read-write. Reset: 0. BIOS: 1. 1=Disables generation of probes for core-generated, RdSized doubleword commands.
0	DisRdBP: disable read byte probe. Read-write. Reset: 0. BIOS: 1. 1=Disables generation of probes for core-generated, RdSized byte commands.

D18F0x6C Link Initialization Control

Bits	Description
30	RlsLnkFullTokCntImm: release upstream full token count immediately. Read-write. Reset: 0b. BIOS: 1 after buffer counts have been programmed. 1=Apply buffer counts programmed in D18F0x[F0,D0,B0,90] and D18F0x[F4,D4,B4,94] immediately without requiring warm reset. Once this bit is set, additional changes to the buffer counts only take effect upon warm reset.
28	RlsIntFullTokCntImm: release internal full token count immediately. Read-write. Reset: 0b. BIOS: 1 after buffer counts have been programmed. 1=Apply buffer counts programmed in D18F3x6C , D18F3x70 , D18F3x74 , D18F3x78 , D18F3x7C , D18F3x140 , D18F3x144 , D18F3x1[54:48] , D18F3x17C , and D18F3x1A0 immediately without requiring warm reset. Once this bit is set, additional changes to the buffer counts only take effect upon warm reset.
27	ApplyIsocModeEnNow. Read-write. Reset: 0b. BIOS: 1 after RlsLnkFullTokCntImm and RlsIntFullTokCntImm have been set. 1=Apply the programmed value in D18F0x[E4,C4,A4,84] [IsocEn] immediately without requiring warm reset. This bit may only be set if RlsLnkFullTokCntImm and RlsIntFullTokCntImm are set and isochronous buffers have been allocated. RULE: IF (ApplyIsocModeEnNow) THEN (D18F3x1[54:48] [IsocPreqTok0] > 0).
23	Reserved. Read-write.
22:21	Reserved. Read-write.
20	Reserved. Read-write.
19:16	Reserved. Read-write.
15:12	Reserved. Read-write.
11	Reserved. Read-write.
10:9	BiosRstDet[2:1]: BIOS reset detect bits[2:1]. See: BiosRstDet[0].
8	Reserved.
6	InitDet: CPU initialization command detect. Read-write. Reset: 0. This bit may be used by software to distinguish between an INIT and a warm/cold reset by setting it to a 1 before an initialization event is generated. This bit is cleared by RESET_L but not by an INIT command.
5	BiosRstDet[0]: BIOS reset detect bit[0]. Read-write; S3-check-exclude. Cold reset: 0. BiosRst-
	Det[2:0] = {BiosRstDet[2:1], BiosRstDet[0]}. May be used to distinguish between a reset event generated by the BIOS versus a reset event generated for any other reason by setting one or more of the bits to a 1 before initiating a BIOS-generated reset event.
4	ColdRstDet: cold reset detect. Read-write. Cold reset: 0. This bit may be used to distinguish between a cold versus a warm reset event by setting the bit to a 1 before an initialization event is generated.
3:2	Reserved.

1	Reserved. Read-write.
0	RouteTblDis: routing table disable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 1. ENDIF. BIOS: 0.

D18F0x[E4,C4,A4,84] Link Control

Table 101: Register Mapping for D18F0x[E4,C4,A4,84]

Register	Function
D18F0x84	ONION Link
D18F0x[E4,C4,A4]	Reserved

This register is derived from the link control register defined in the link specification.

Bits	Description
15	Addr64BitEn: 64-bit address packet enable. Read-write. Reset: 0000b. 1=Requests to addresses greater than FF_FFFF_FFFFh are supported by this IO link. 0=Requests to addresses greater than FF_FFFF_FFFFh are master aborted as if the end of chain was reached. BIOS is required to ensure that the link-specification-defined “64 Bit Address Feature” bit in the device on the other side of the link is set prior to setting this bit. For coherent links, this bit is unused. D18F0x68[CHtExtAddrEn] is required to be set if this bit is set for any IO link. The link specification indicates that this bit is cleared by a warm reset; therefore this bit may be in a different state than an IO device on the other side of the link after a warm reset; care should be taken by BIOS to place devices on both sides of the link in the same state after a warm reset, before any packets to the high-order addresses enabled by this bit are generated.
14:13	Reserved. Read-write.
12	IsocEn: isochronous flow-control mode enable. Read-write. Reset: 0b. BIOS: 1 if the link is an ONION Link. This bit is set to place the link into isochronous flow-control mode (IFCM), as defined by the link specification. 1=IFCM. 0=Normal flow-control mode. See D18F0x6C[ApplyIsocModeEnNow] .
5	Reserved.
4	LinkFail: link failure. Read; set-by-hardware; write-1-to-clear. Cold reset: 0. This bit is set high by the hardware if a sync flood is received by the link. See 2.14.1.9.1 [Common Diagnosis Information] .

D18F0x[EC,CC,AC,8C] Link Feature Capability

This register is derived from the link feature capability register defined in the link specification. Unless otherwise specified: 0=The feature is not supported; 1=The feature is supported.

Table 102: Register Mapping for D18F0x[EC,CC,AC,8C]

Register	Function
D18F0x8C	ONION Link
D18F0x[EC,CC,AC]	Reserved

Bits	Description
31:6	Reserved.
5	UnitIdReOrderDis: UnitID reorder disable. Read-write. Reset: 0. 1=Upstream reordering for different UnitIDs is not supported; i.e., all upstream packets are ordered as if they have the same UnitID. 0=Reordering based on UnitID is supported.
4	Reserved. Reset: 1.
3:2	Reserved.
1	Reserved. Reset: 1.
0	Reserved. Reset: 1.

D18F0x[F0,D0,B0,90] Link Base Channel Buffer Count

Read-write; Reset-applied.

Table 103: Register Mapping for D18F0x[F0,D0,B0,90]

Register	Function
D18F0x90	ONION Link
D18F0x[F0,D0,B0]	Reserved

D18F0x[F0,D0,B0,90] and D18F0x[F4,D4,B4,94] specify the *hard-allocated* link flow-control buffer counts in each virtual channel available to the transmitter at the other end of the link; it also provides the *free buffers* that may be used by any of the virtual channels, as needed. Base channel buffers are specified in D18F0x[F0,D0,B0,90]; isochronous buffer counts (if in IFCM) are specified in D18F0x[F4,D4,B4,94]. For all fields that specify buffer counts in D18F0x[F0,D0,B0,90] and D18F0x[F4,D4,B4,94], if the link is ganged, then the number of buffers allocated is 2 times the value of the field; If the link is unganged, then the number of buffers allocated is the value of the field.

The cold or warm reset value is determined by whether the link initializes, whether the link is IO/coherent, whether the link is ganged/unganged, and whether the settings are locked by LockBc. Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use D18F0x6C[RlsLnkFullTokCntImm] or D18F0x6C[RlsLnkFullTokCntOnRst] for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

The hard-allocated buffer counts are transmitted to the device at the other end of the link in buffer release messages after link initialization. The remaining buffers are held in the free list (specified by FreeData and FreeCmd) used to optimize buffer usage. When a transaction is received, if a free-list buffer is available, it is used for storage instead of one of the hard allocated buffers; as a result, a buffer release (for one of the hard allocated buffers used by the incoming request) can be immediately sent back to the device at the other end of the link without waiting for the transaction to be routed beyond the flow-control buffers.

Table 104: Link Buffer Definitions

Term	Definition
LpbSize	Link Packet Command Buffer size. LpbSize = 24.
LpbdSize	Link Packet Data Buffer size. LpbdSize = 16.
LcsSize	Link Command Scheduler size. LcsSize = 32.

Buffer allocation rules:

- The total number of command buffers allocated in the base and isochronous registers of a link cannot exceed **LpbSize**:
 - Rule: $(D18F0x[F0,D0,B0,90][NpReqCmd] + D18F0x[F0,D0,B0,90][PReq] + D18F0x[F0,D0,B0,90][RspCmd] + D18F0x[F0,D0,B0,90][ProbeCmd] + D18F0x[F0,D0,B0,90][FreeCmd] + D18F0x[F4,D4,B4,94][IsocNpReqCmd] + D18F0x[F4,D4,B4,94][IsocPReq] + D18F0x[F4,D4,B4,94][IsocRspCmd]) \leq LpbSize$.
- The total number of data buffers allocated in the base and isochronous registers of a link cannot exceed **LpbdSize**:
 - Rule: $(D18F0x[F0,D0,B0,90][NpReqData] + D18F0x[F0,D0,B0,90][RspData] + D18F0x[F0,D0,B0,90][PReq] + D18F0x[F0,D0,B0,90][FreeData] + D18F0x[F4,D4,B4,94][IsocPReq] + D18F0x[F4,D4,B4,94][IsocNpReqData] + D18F0x[F4,D4,B4,94][IsocRspData]) \leq LpbdSize$.
- The total number of hard allocated command buffers cannot exceed **LcsSize**.
 - Rule: $(D18F0x[F0,D0,B0,90][ProbeCmd] + D18F0x[F0,D0,B0,90][RspCmd] + D18F0x[F0,D0,B0,90][PReq] + D18F0x[F0,D0,B0,90][NpReqCmd] + D18F0x[F4,D4,B4,94][IsocRspCmd] + D18F0x[F4,D4,B4,94][IsocPReq] + D18F0x[F4,D4,B4,94][IsocNpReqCmd]) \leq LcsSize$.

Bits	Description
31	LockBc: lock buffer count register. Cold reset: 0. BIOS: 1. 1=The buffer count registers, D18F0x[F0,D0,B0,90] and D18F0x[F4,D4,B4,94] are locked such that warm resets do not place the registers back to their default value. Setting this bit does not prevent the buffer counts from being updated after a warm reset based on the value of the buffer counts before the warm reset. 0=Upon warm reset, the buffer count registers return to their default value after the link initializes regardless of the value before the warm reset.
30	PReq[3]: posted request command and data buffer count [3]. IF (LockBc) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 0. See: PReq[2:0].
29:28	NpReqData[3:2]: non-posted request data buffer count [3:2]. IF (LockBc) THEN Cold reset: 00b. ELSE THEN Reset: 00b. ENDIF. BIOS: IF (REG==D18F0x90) THEN 00b ELSE 11b ENDIF. See: NpReqData[1:0].

27:25	FreeData: free data buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: 0.
24:20	FreeCmd: free command buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: IF (REG==D18F0x90) THEN 00h ELSE 00h ENDIF.
19:18	RspData: response data buffer count. IF (LockBc) THEN Cold reset: 1. ELSE THEN Reset: 1. ENDIF. BIOS: IF (REG==D18F0x90) THEN 1 ELSE 0 ENDIF.
17:16	NpReqData[1:0]: non-posted request data buffer count [1:0]. NpReqData[3:0] = {NpReqData[3:2], NpReqData[1:0]}. IF (LockBc) THEN Cold reset: 01b. ELSE THEN Reset: 01b. ENDIF. BIOS: IF (REG==D18F0x90) THEN 01b ELSE 11b ENDIF.
15:12	ProbeCmd: probe command buffer count. IF (LockBc) THEN Cold reset: 0h. ELSE THEN Reset: 0h. ENDIF. BIOS: 0h.
11:8	RspCmd: response command buffer count. IF (LockBc) THEN Cold reset: 1h. ELSE THEN Reset: 1h. ENDIF. BIOS: IF (REG==D18F0x90) THEN 1h ELSE 0h ENDIF.
7:5	PReq[2:0]: posted request command and data buffer count [2:0]. PReq[3:0] = {PReq[3], PReq[2:0]}. Specifies the number of posted command and posted data buffers allocated. IF (LockBc) THEN Cold reset: 110b. ELSE Reset: 110b. ENDIF. BIOS: 101b.
4:0	NpReqCmd: non-posted request command buffer count. IF (LockBc) THEN Cold reset: 09h. ELSE THEN Reset: 09h. ENDIF. BIOS: IF (REG==D18F0x90) THEN 05h ELSE 18h ENDIF.

D18F0x[F4,D4,B4,94] Link Isochronous Channel Buffer CountRead-write; Reset-applied. See [D18F0x\[F0,D0,B0,90\]](#).

Table 105: Register Mapping for D18F0x[F4,D4,B4,94]

Register	Function
D18F0x94	ONION Link
D18F0x[F4,D4,B4]	Reserved

Bits	Description
31:29	Reserved.

28:27	IsocRspData: isochronous response data buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: 0.
26:25	IsocNpReqData: isochronous non-posted request data buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: IF (REG==D18F0x94) THEN 1 ELSE 0 ENDIF.
24:22	IsocRspCmd: isochronous response command buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: 0.
21:19	IsocPReq: isochronous posted request command and data buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. This specifies the number of isochronous posted command and posted data buffers allocated. BIOS: 0.
18:16	IsocNpReqCmd: isochronous non-posted request command buffer count. IF (D18F0x[F0,D0,B0,90][LockBc]) THEN Cold reset: 0. ELSE THEN Reset: 0. ENDIF. BIOS: IF (REG==D18F0x94) THEN 1 ELSE 0 ENDIF.
15:8	SecBusNum: secondary bus number. Reset: 0. Specifies the configuration-space bus number of the IO link. When configured as a coherent link, this register has no meaning. This field should match the corresponding D18F1x[1DC:1D0,EC:E0][BusNumBase], unless D18F1x[1DC:1D0,EC:E0][DevCmpEn]=1, in which case this field should be 00h). <ul style="list-style-type: none"> Rule: IF (~D18F1x[1DC:1D0,EC:E0][DevCmpEn]) THEN (D18F0x[F4,D4,B4,94][SecBus-Num]==D18F1x[1DC:1D0,EC:E0][BusNumBase]). Rule: IF (D18F1x[1DC:1D0,EC:E0][DevCmpEn]) THEN (D18F0x[F4,D4,B4,94][SecBus-Num]==00h).
7:0	Reserved.

D18F0x[F8,D8,B8,98] Link Type

Table 106: Register Mapping for D18F0x[F8,D8,B8,98]

Register	Function
D18F0x98	ONION Link
D18F0x[F8,D8,B8]	Reserved

Bits	Description
31:6	Reserved.
5	PciEligible. Read-only. Reset: 1. 1=Hardware has determined this is not a HyperTransport link.
4:3	Reserved.
2	Reserved. Reset: 1.
1	Reserved. Reset: 1.
0	Reserved. Reset: 1.

D18F0x[11C,118,114,110] Link Clumping Enable

Reset: 0000_0000h. D18F0x[11C,118,114,110] are associated with the whole link if it is ganged or sublink 0 if

it is unganged; If the node does not support a link, then the corresponding register addresses become reserved.

Table 107: Register Mapping for D18F0x[11C,118,114,110]

Register	Function
D18F0x110	ONION Link
D18F0x11[C:4]	Reserved

These registers specify how UnitIDs of upstream non-posted requests may be clumped per the link specification. The processor does not clump requests that it generates in the downstream direction.

Bits	Description
31:1	ClumpEn. Read-write. Each bit of this register corresponds to a link UnitID number. E.g., bit 2 corresponds to UnitID 02h, etc. 1=The specified UnitID is ordered in the same group as the specified UnitID - 1. For example if this register is programmed to 0000_00C0h, then UnitIDs 7h, 6h, and 5h are all ordered as if they are part of the same UnitID. This is used to allow more than 32 tags to be assigned to a single stream for the purposes of ordering. Bit 1 must be set by BIOS for the ONION link. Other bits must be set per GNB requirements. (See D0F0x98_x3A .) For ONIONPlus links, BIOS must program this field to 7FFF_FFF9h.
0	Reserved.

D18F0x150 Link Global Retry Control

Cold reset: 0000_0000h.

Bits	Description
31:0	Reserved.

D18F0x168 Extended Link Transaction Control

Read-write.

Bits	Description
20	XcsSecPickerDstNcHt. Reset: 0. BIOS: 1. 1=Enable scheduling un-ordered responses via the secondary XCS picker to the Onion bus(es). This feature is intended for single-node systems only.
18	Reserved.
14:12	Reserved. Read-write.

D18F0x16C Link Global Extended Control

Reset: 0000_0000h.

Bits	Description

D18F0x[18C:170] Link Extended Control

These registers provide control for each link. They are mapped to the links as follows:

Table 108: Register Mapping for D18F0x[18C:170]

Register	Function
D18F0x170	ONION Link
D18F0x1[8C:74]	Reserved

Reset: 0000_0001h.

Bits	Description
------	-------------

D18F0x1A0 Link Initialization Status

Table 109: Onion Definitions

Term	Definition
OnionPlus	OnionPlus link detected. OnionPlus = (D18F0x1A0[OnionPlusCap]).

Bits	Description										
31	InitStatusValid: initialization status valid. Read-only; Updated-by-hardware. Reset: 0. 1=Indicates that the rest of the information in this register is valid for all links; each link is either not connected or the initialization is complete.										
30:28	Reserved.										
27:24	OnionPlusCap. Read-only; Updated-by-hardware. Reset: 0h. 1=OnionPlus capable link detected. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Link 0</td> </tr> <tr> <td>[1]</td> <td>Link 1</td> </tr> <tr> <td>[2]</td> <td>Link 2</td> </tr> <tr> <td>[3]</td> <td>Link 3</td> </tr> </tbody> </table>	Bit	Description	[0]	Link 0	[1]	Link 1	[2]	Link 2	[3]	Link 3
Bit	Description										
[0]	Link 0										
[1]	Link 1										
[2]	Link 2										
[3]	Link 3										
23:4	Reserved.										
3:2	InitComplete1: initialization complete for link 1. See: InitComplete0.										
1:0	InitComplete0: initialization complete for link 0. Read-only; Updated-by-hardware. Reset: 00b. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Internal northbridge link (ONION) has not completed initialization.</td> </tr> <tr> <td>10b-01b</td> <td>Reserved</td> </tr> <tr> <td>11b</td> <td>Internal northbridge link (ONION) has completed initialization.</td> </tr> </tbody> </table>	Bits	Description	00b	Internal northbridge link (ONION) has not completed initialization.	10b-01b	Reserved	11b	Internal northbridge link (ONION) has completed initialization.		
Bits	Description										
00b	Internal northbridge link (ONION) has not completed initialization.										
10b-01b	Reserved										
11b	Internal northbridge link (ONION) has completed initialization.										

D18F0x1DC Core Enable

Reset: 0000_0000h.

Bits	Description
31:16	Reserved. Reserved for CpuEn expansion.

15:1	CpuEn: core enable. Read-write. This field is used to enable each of the cores after a reset. 1=Enable the core to start fetching and executing code from the boot vector. The most significant bit N is indicated by CpuCoreNum, as defined in section 2.4.4 [Processor Cores and Downcoring]. All bits greater than N are reserved. <table><thead><tr><th><u>Bit</u></th><th><u>Description</u></th></tr></thead><tbody><tr><td>[0]</td><td>Core 1 enable</td></tr><tr><td>[1]</td><td>Core <BIT+1> enable</td></tr><tr><td>[2]</td><td>Core 3 enable</td></tr><tr><td>[15:3]</td><td>Reserved</td></tr></tbody></table>	<u>Bit</u>	<u>Description</u>	[0]	Core 1 enable	[1]	Core <BIT+1> enable	[2]	Core 3 enable	[15:3]	Reserved
<u>Bit</u>	<u>Description</u>										
[0]	Core 1 enable										
[1]	Core <BIT+1> enable										
[2]	Core 3 enable										
[15:3]	Reserved										
0	Reserved.										

3.10 Device 18h Function 1 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F1x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1531h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F1x08 Class Code/Revision ID

Bits	Description
31:8	ClassCode. Read-only. Value: 060000h. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only. Value: 00h. Processor revision. 00h=A0.

D18F1x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:0	HeaderTypeReg. Read-only. These bits are fixed at their default values. The header type field indicates that there are multiple functions present in this device.

D18F1x[17C:140,7C:40] DRAM Base/Limit

The following sets of registers specify the DRAM address ranges:

Table 110: Register Mapping for D18F1x[17C:140,7C:40]

Function	Base Low	Limit Low	Base High	Limit High
Range 0	D18F1x40	D18F1x44	D18F1x140	D18F1x144
Reserved	D18F1x48, D18F1x[7:5][8,0]	D18F1x4C, D18F1x[7:5][C,4]	D18F1x148, D18F1x1[7:5][8,0]	D18F1x14C, D18F1x1[7:5][C,4]

Transaction addresses that are within the specified base/limit range are routed to the DstNode. See 2.8.2 [NB Routing].

DRAM mapping rules:

F1x0XX registers provide the low address bits. F1x1XX registers are reserved.

- Transaction addresses are within the defined range if:
 $\{DramBase[39:24], 00_0000h\} \leq address[39:0] \leq \{DramLimit[39:24], FF_FFFFh\}$.
- DRAM regions must not overlap each other.
- Accesses to addresses that map to both DRAM, as specified by the DRAM base and limit registers (F1x[1, 0][7C:40]), and MMIO, as specified by D18F1x[2CC:2A0,1CC:180,BC:80], are routed to MMIO only.

- Programming of the DRAM address maps must be consistent with the Memory-Type Range Registers (MTRRs) and the top of memory registers, [MSRC001_001A](#) and [MSRC001_001D](#). CPU accesses only hit within the DRAM address maps if the corresponding MTRR is of type DRAM. Accesses from IO links are routed based on the DRAM base and limit registers (F1x[1, 0][7C:40]) only.
- The appropriate RE or WE bit(s) must be set. When initializing a base/limit pair, the BIOS must write the [limit] register before either the RE or WE bit is set. When changing a base/limit pair that is already enabled, the BIOS should clear RE and WE before changing the address range.
- See [2.8.2.1.1 \[DRAM and MMIO Memory Space\]](#).

When memory hoisting is enabled in a node via [D18F1x2\[1,0\]\[8,0\]\[LgcyMmioHoleEn\]](#), the corresponding BaseAddr/LimitAddr should be configured to account for the memory hoisted above the hole. See [2.9.10 \[Memory Hoisting\]](#).

D18F1x[7:4][8,0] DRAM Base Low

IF ([D18F2x118\[LockDramCfg\]](#)) THEN Read-only. ELSE Read-write. ENDIF. IF ([BootFromDRAM && REG==D18F1x40](#)) THEN Cold reset: 0000_0003h. ELSE Reset: 0000_0000h. ENDIF.

Table 111: Register Mapping for D18F1x[7:4][8,0]

Register	Function
D18F1x40	Range 0
D18F1x48	Reserved
D18F1x[7:5][8,0]	Reserved

Bits	Description
31:16	DramBase[39:24]: DRAM base address register bits[39:24].
15:2	Reserved.
1	WE: write enable. 1=Writes to this address range are enabled.
0	RE: read enable. 1=Reads to this address range are enabled.

D18F1x[7:4][C,4] DRAM Limit Low

IF ([D18F2x118\[LockDramCfg\]](#)) THEN Read-only. ELSE Read-write. ENDIF.

Table 112: Register Mapping for D18F1x[7:4][C,4]

Register	Function
D18F1x44	Range 0
D18F1x4C	Reserved
D18F1x[7:5][C,4]	Reserved

Bits	Description
31:16	DramLimit[39:24]: DRAM limit address register bits[39:24]. IF (BootFromDRAM && REG==D18F1x44) THEN Cold reset: 01FFh. ELSE Reset: FCFFh. ENDIF.
15:11	Reserved.

10:8	Reserved.
7:3	Reserved.
2:0	DstNode: destination Node ID. Reset: 000b. Specifies the node that a packet is routed to if it is within the address range.

D18F1x[2CC:2A0,1CC:180,BC:80] MMIO Base/Limit

These registers, The memory mapped IO base and limit registers D18F1x[2CC:2A0,1CC:180,BC:80] specify the mapping from memory addresses to the corresponding node and IO link for MMIO transactions. Address ranges are specified by upto 16 sets of base/limit registers.

Table 113: Register Mapping for D18F1x[2CC:2A0,1CC:180,BC:80]

Function	MMIO Base Low	MMIO Limit Low	MMIO Base/Limit High
Range 0	D18F1x80	D18F1x84	Reserved
Range 1	D18F1x88	D18F1x8C	Reserved
Range 2	D18F1x90	D18F1x94	Reserved
Range 3	D18F1x98	D18F1x9C	Reserved
Range 4	D18F1xA0	D18F1xA4	Reserved
Range 5	D18F1xA8	D18F1xAC	Reserved
Range 6	D18F1xB0	D18F1xB4	Reserved
Range 7	D18F1xB8	D18F1xBC	Reserved
Range 8	D18F1x1A0	D18F1x1A4	Reserved
Range 9	D18F1x1A8	D18F1x1AC	Reserved
Range 10	D18F1x1B0	D18F1x1B4	Reserved
Range 11	D18F1x1B8	D18F1x1BC	Reserved
Reserved	D18F1x2[B8,B0,A8, A0]	D18F1x2[BC,B4,AC, A4]	Reserved

Transaction addresses that are within the specified base/limit range are routed to the node specified by DstNode and the link specified by DstLink. See [2.8.2 \[NB Routing\]](#).

MMIO mapping rules:

- Transaction addresses are within the defined range if:
 $\{MMIOBase[39:16], 0000h\} \leqslant \text{address}[39:0] \leqslant \{\text{MMIOLimit}[39:16], FFFFh\}$.
- MMIO regions must not overlap each other.
- Accesses to addresses that map to both DRAM, as specified by the DRAM base and limit registers (see [D18F1x\[17C:140,7C:40\]](#)), and MMIO, as specified by the memory mapped IO base and limit registers (F1x[BC:80]), are routed to MMIO only.
- Programming of the MMIO address maps must be consistent with the Memory-Type Range Registers (MTRRs) and the top of memory registers, [MSRC001_001A](#) and [MSRC001_001D](#). CPU accesses only hit within the MMIO address maps if the corresponding MTRR is of type IO. Accesses from IO links are routed based on [D18F1x\[2CC:2A0,1CC:180,BC:80\]](#).
- The appropriate RE or WE bit(s) must be set. When initializing a base/limit pair, the BIOS must write the limit register before either the RE or WE bit is set. When changing a base/limit pair that is already enabled, the BIOS should clear RE and WE before changing the address range.
- Scenarios in which the address space of multiple MMIO ranges target the same IO device is supported.

- See [2.8.2.1.1 \[DRAM and MMIO Memory Space\]](#).

D18F1x[2B:1A,B:8][8,0] MMIO Base Low

Table 114: Register Mapping for D18F1x[2B:1A,B:8][8,0]

Register	Function
D18F1x80	Range 0
D18F1x88	Range 1
D18F1x90	Range 2
D18F1x98	Range 3
D18F1xA0	Range 4
D18F1xA8	Range 5
D18F1xB0	Range 6
D18F1xB8	Range 7
D18F1x1A0	Range 8
D18F1x1A8	Range 9
D18F1x1B0	Range 10
D18F1x1B8	Range 11
D18F1x2[B:A][8,0]	Reserved

Bits	Description
31:8	MMIOBase[39:16]: MMIO base address register bits[39:16] . Read-write. Reset: 0.
7:4	Reserved.
3	Lock . Read-write. Reset: 0. 1=the memory mapped IO base and limit registers (D18F1x[2CC:2A0,1CC:180,BC:80]) are read-only (including this bit). WE or RE in this register must be set in order for this to take effect.
1	WE: write enable . Read-write. Reset: 0. 1=Writes to this address range are enabled.
0	RE: read enable . Read-write. Reset: 0. 1=Reads to this address range are enabled.

D18F1x[2B:1A,B:8][C,4] MMIO Limit Low

Table 115: Register Mapping for D18F1x[2B:1A,B:8][C,4]

Register	Function
D18F1x84	Range 0
D18F1x8C	Range 1
D18F1x94	Range 2
D18F1x9C	Range 3
D18F1xA4	Range 4
D18F1xAC	Range 5
D18F1xB4	Range 6

Table 115: Register Mapping for D18F1x[2B:1A,B:8][C,4]

D18F1xBC	Range 7
D18F1x1A4	Range 8
D18F1x1AC	Range 9
D18F1x1B4	Range 10
D18F1x1BC	Range 11
D18F1x2[BC,B4,AC,A4]	Reserved.

Bits	Description										
31:8	MMIOLimit[39:16]: MMIO limit address register bits[39:16]. Read-write. Reset: 0.										
7	NP: non-posted. Read-write. Reset: 0. 1=CPU write requests to this MMIO range are passed through the non-posted channel. This may be used to force writes to be non-posted for MMIO regions which map to the legacy ISA/LPC bus, or in conjunction with D18F0x68[DsNpReqLmt] in order to allow downstream CPU requests to be counted and thereby limited to a specified number. This latter use of the NP bit may be used to avoid loop deadlock scenarios in systems that implement a region in an IO device that reflects downstream accesses back upstream. See the link summary of deadlock scenarios for more information. 0=CPU writes to this MMIO range use the posted channel. This bit does not affect requests that come from IO links (the virtual channel of the request is specified by the IO request). If two MMIO ranges target the same IO device and the NP bit is set differently in both ranges, unexpected transaction ordering effects are possible. In particular, using PCI- and IO-link-defined producer-consumer semantics, if a producer (e.g., the processor) writes data using a non-posted MMIO range followed by a flag to a posted MMIO range, then it is possible for the device to see the flag updated before the data is updated.										
6	DstSubLink: destination sublink. Read-write. Reset: 0. When a link is unganged, this bit specifies the destination sublink of the link specified by the memory mapped IO base and limit registers F1x[BC:80][DstLink]. 0=The destination link is sublink 0. 1=The destination link is sublink 1. If the link is ganged, then this bit must be low.										
5:4	DstLink: destination link ID. Read-write. Reset: 0. For transactions within this MMIO range, this field specifies the destination IO link number of the destination node. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Link 0</td> </tr> <tr> <td>01b</td> <td>Link 1</td> </tr> <tr> <td>10b</td> <td>Link 2</td> </tr> <tr> <td>11b</td> <td>Link 3</td> </tr> </tbody> </table>	Bits	Description	00b	Link 0	01b	Link 1	10b	Link 2	11b	Link 3
Bits	Description										
00b	Link 0										
01b	Link 1										
10b	Link 2										
11b	Link 3										
3	Reserved.										
2:0	DstNode: destination node ID bits. Read-write. Reset: 0. For transactions within this MMIO range, this field specifies the destination node ID.										

D18F1x[DC:C0] IO-Space Base/Limit

The IO-space base and limit registers, D18F1x[DC:C0], specify the mapping from IO addresses to the corresponding node and IO link for transactions resulting from x86-defined IN and OUT instructions. IO address ranges are specified by upto 8 sets of base/limit registers. The first set is F1xC0 and F1xC4, the second

set is F1xC8 and F1xCC, and so forth. Transaction addresses that are within the specified base/limit range are routed to the node specified by DstNode and the link specified by DstLink. See [2.8.2 \[NB Routing\]](#).

IO mapping rules:

- IO-space transaction addresses are within the defined range if:
 $\{IOBase[24:12], 000h\} \leq address \leq \{IOLimit[24:12], FFFh\}$ and as specified by the IE bit; or
 if the address is in the range specified by the VE bits.
- IO regions must not overlap each other.
- The appropriate RE or WE bit(s) must be set.
- See [2.8.2.1.2 \[IO Space\]](#).

D18F1x[1F:1E,D:C][8,0] IO-Space Base

Table 116: Register Mapping for D18F1x[1F:1E,D:C][8,0]

Register	Function
D18F1xC0	Range 0
D18F1xC8	Range 1
D18F1xD0	Range 2
D18F1xD8	Range 3
D18F1x1[F:E][8,0]	Reserved

Bits	Description
31:25	Reserved.
24:12	IOBase[24:12]: IO base address register bits[24:12] . Read-write. Reset: 0.
11:6	Reserved.
5	IE: ISA enable . Read-write. Reset: 0. 1=The IO-space address window is limited to the first 256 B of each 1 KB block specified; this only applies to the first 64 KB of IO space. 0=The PCI IO window is not limited in this way.
4	VE: VGA enable . Read-write. Reset: 0. 1=Include IO-space transactions targeting the VGA-compatible address space within the IO-space window of this base/limit pair. These include IO accesses in which address bits[9:0] range from 3B0h to 3BBh or 3C0h to 3DFh (address bits[15:10] are not decoded); this only applies to the first 64 KB of IO space; i.e., address bits[24:16] must be low). 0=IO-space transactions targeting VGA-compatible address ranges are not added to the IO-space window. This bit should only ever be set in one register. The MMIO range associated with the VGA enable bit in the PCI specification is NOT included in the VE bit definition; to map this range to an IO link, see D18F1xF4 [VGA Enable] . When D18F1xF4[VE] is set, the state of this bit is ignored.
3:2	Reserved.
1	WE: write enable . Read-write. Reset: 0. 1=Writes to this IO-space address range are enabled.
0	RE: read enable . Read-write. Reset: 0. 1=Reads to this IO-space address range are enabled.

D18F1x[1F:1E,D:C][C,4] IO-Space Limit

Table 117: Register Mapping for D18F1x[1F:1E,D:C][C,4]

Register	Function
D18F1xC4	Range 0
D18F1xCC	Range 1
D18F1xD4	Range 2
D18F1xDC	Range 3
D18F1x1[F:E][C,4]	Reserved

Bits	Description										
31:25	Reserved.										
24:12	IOLimit[24:12]: IO limit address register bits[24:12]. Read-write. Reset: 0.										
11:7	Reserved.										
6	DstSubLink: destination sublink. Read-write. Reset: 0. When a link is unganged, this bit specifies the destination sublink of the link specified by F1x[DC:C0][DstLink]. 0=The destination link is sublink 0. 1=The destination link is sublink 1. If the link is ganged, then this bit must be low.										
5:4	DstLink: destination link ID. Read-write. Reset: 0. For transactions within this IO-space range, this field specifies the destination IO link number of the destination node. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Link 0</td> </tr> <tr> <td>01b</td> <td>Link 1</td> </tr> <tr> <td>10b</td> <td>Link 2</td> </tr> <tr> <td>11b</td> <td>Link 3</td> </tr> </tbody> </table>	Bits	Description	00b	Link 0	01b	Link 1	10b	Link 2	11b	Link 3
Bits	Description										
00b	Link 0										
01b	Link 1										
10b	Link 2										
11b	Link 3										
3	Reserved.										
2:0	DstNode: destination node ID bits. Read-write. Reset: 0. For transactions within this IO-space range, this field specifies the destination node ID.										

D18F1x[1DC:1D0,EC:E0] Configuration Map

D18F1x[1DC:1D0,EC:E0] specify the mapping from configuration address to the corresponding node and IO link. Configuration address ranges are specified by upto 8 pairs of base/limit registers. Transaction addresses that are within the specified base/limit range are routed to the node specified by DstNode and the link specified by DstLink. See [2.8.2 \[NB Routing\]](#).

Table 118: Register Mapping for D18F1x[1DC:1D0,EC:E0]

Register	Function
D18F1xE0	Range 0
D18F1xE4	Range 1
D18F1xE8	Range 2
D18F1xEC	Range 3
D18F1x1[DC:D0]	Reserved

Configuration space mapping rules:

- Configuration addresses (to “BusNo” and “Device” as specified by [IOCF8 \[IO-Space Configuration\]](#)

[Address](#) in the case of IO accesses or [2.7 \[Configuration Space\]](#) in the case of MMIO accesses) are within the defined range if:

({BusNumBase[7:0]} <= BusNo <= {BusNumLimit[7:0]}) & (DevCmpEn==0); or
 ({BusNumBase[4:0]} <= Device <= {BusNumLimit[4:0]}) & (DevCmpEn==1) & (BusNo== 00h).

- Configuration regions must not overlap each other.
- The appropriate RE or WE bit(s) must be set.
- See [2.8.2.1.3 \[Configuration Space\]](#).

Bits	Description
31:24	BusNumLimit[7:0]: bus number limit bits[7:0] . Read-write. Reset: 0.
23:16	BusNumBase[7:0]: bus number base bits[7:0] . Read-write. Reset: 0.
2	DevCmpEn: device number compare mode enable . Read-write. Reset: 0. 1=A device number range rather than a bus number range is used to specify the configuration-space window (see above). This is used to enable multiple IO links to be configured as Bus 0.
1	WE: write enable . Read-write. Reset: 0. 1=Writes to this configuration-space address range are enabled.
0	RE: read enable . Read-write. Reset: 0. 1=Reads to this configuration-space address range are enabled.

D18F1xF0 DRAM Hole Address

IF ([D18F2x118\[LockDramCfg\] && ~D18F3x12C\[OverrideLockDramCfg\]](#)) THEN Read-only. ELSE Read-write. ENDIF. Same-for-all. Reset: 0000_0000h. See [2.9.10 \[Memory Hoisting\]](#).

Bits	Description
31:24	DramHoleBase[31:24]: DRAM hole base address . Specifies the base address of the IO hole, below the 4GB address level, that is used in memory hoisting. Normally, DramHoleBase >= MSRC001_001A[TOM[31:24]] .
23:16	Reserved.
15:7	DramHoleOffset[31:23]: DRAM hole offset address . When D18F1x2[1,0][8,0][LgcyMmio-HoleEn]==1 , this offset is subtracted from the physical address of certain accesses in forming the normalized address.
6:3	Reserved.
2	Reserved. Read-write.
1	DramMemHoistValid: dram memory hoist valid . 1=Memory hoisting for the address range is enabled. 0=Memory hoisting is not enabled. This bit should be set if any D18F1x2[1,0][8,0][LgcyMmioHoleEn]==1 or DramHoleBase != 0.
0	DramHoleValid: dram hole valid . 1=Memory hoisting is enabled in the node. 0=Memory hoisting is not enabled. This bit should be set in the node that owns the DRAM address space that is hoisted above the 4 GB address level. See DramHoleBase.

D18F1xF4 VGA Enable

Reset: 0000_0000h. All these bits are read-write unless Lock is set.

Bits	Description										
31:15	Reserved.										
14	DstSubLink: destination sublink. Read-write. When a link is unganged, this bit specifies the destination sublink of the link specified by D18F1xF4[DstLink]. 0=The destination link is sublink 0. 1=The destination link is sublink 1. If the link is ganged, then this bit must be low.										
13:12	DstLink: destination link ID. Read-write. For transactions within the D18F1xF4[VE]-defined ranges, this field specifies the destination IO link number of the destination node. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Link 0</td> </tr> <tr> <td>01b</td> <td>Link 1</td> </tr> <tr> <td>10b</td> <td>Link 2</td> </tr> <tr> <td>11b</td> <td>Link 3</td> </tr> </tbody> </table>	Bits	Description	00b	Link 0	01b	Link 1	10b	Link 2	11b	Link 3
Bits	Description										
00b	Link 0										
01b	Link 1										
10b	Link 2										
11b	Link 3										
11:7	Reserved.										
6:4	DstNode: destination node ID. Read-write. For transactions within the D18F1xF4[VE]-defined range, this field specifies the destination node ID.										
3	Lock. Read-write. 1=All the bits in this register (D18F1xF4) are read-only (including this bit).										
1	NP: non-posted. Read-write. 1=CPU write requests to the D18F1xF4[VE]-defined MMIO range are passed through the non-posted channel. 0=CPU writes may be posted.										
0	VE: VGA enable. Read-write. 1=Transactions targeting the VGA-compatible address space are routed and controlled as specified by this register. The VGA-compatible address space is: (1) the MMIO range A_0000h through B_FFFFh; (2) IO-space accesses in which address bits[9:0] range from 3B0h to 3BBh or 3C0h to 3DFh (address bits[15:10] are not decoded; this only applies to the first 64 KB of IO space; i.e., address bits[24:16] must be low). 0=Transactions targeting the VGA-compatible address space are not affected by the state of this register. When this bit is set, the state of D18F1xF4[VE] is ignored.										

D18F1x10C DCT Configuration Select

Reset: 0000_0000h.

Bits	Description										
5:4	NbPsSel: NB P-state configuration select. Read-write. Specifies the set of DCT Pstate registers to which software configuration accesses are routed. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>NB P-state 0</td> </tr> <tr> <td>01b</td> <td>NB P-state 1</td> </tr> <tr> <td>10b</td> <td>NB P-state 2</td> </tr> <tr> <td>11b</td> <td>NB P-state 3</td> </tr> </tbody> </table> <p>The following registers must be programmed for each NB P-state enabled by D18F5x16[C:0][NbPstateEn]:</p> <ul style="list-style-type: none"> • D18F2x210_dct[0]_nbp[3:0][MaxRdLatency, DataTx_fifoWrDly]. • D18F2x210_dct[0]_nbp[3:0][RdPtrInit]. <p>This field is ignored on accesses to registers other than listed above.</p>	Bits	Description	00b	NB P-state 0	01b	NB P-state 1	10b	NB P-state 2	11b	NB P-state 3
Bits	Description										
00b	NB P-state 0										
01b	NB P-state 1										
10b	NB P-state 2										
11b	NB P-state 3										

3	<p>MemPsSel: Memory P-state configuration select. Read-write. Specifies the set of DCT controller registers to which software configuration accesses are routed. This register works independently of NbPsSel. 0=Memory P-state 0. 1=Memory P-state 1. See 2.5.7.1 [Memory P-states] and 2.9.3 [DCT Configuration Registers]. The following registers must be programmed for each memory P-state enabled by D18F5x16[C:0][MemPstate]:</p> <ul style="list-style-type: none"> • D18F2x2E8_dct[0]_mp[1:0] • D18F2x2EC_dct[0]_mp[1:0] <p>The _mp[D18F2x2E0_dct[0][CurMemPstate]] SPR state is used for MRS during h/w dram init.</p>						
2:0	<p>DctCfgSel: DRAM controller configuration select. Read-write. Specifies DCT controller to which software configuration accesses are routed. See 2.9.3 [DCT Configuration Registers].</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 15%;">Bits</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">000b</td> <td style="text-align: left;">DCT 0</td> </tr> <tr> <td style="text-align: left;">111b-001b</td> <td style="text-align: left;">Reserved</td> </tr> </tbody> </table>	Bits	Description	000b	DCT 0	111b-001b	Reserved
Bits	Description						
000b	DCT 0						
111b-001b	Reserved						

D18F1x120 DRAM Base System Address

IF (D18F2x118[LockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Cold reset: 0000_0000h. D18F1x120 and D18F1x124 are required to specify the base and limit system address range of the DRAM connected to the local node.

DRAM accesses to the local node with physical address Addr[47:0] that are within the following range are directed to the DCTs:

{DramBaseAddr[47:27], 000_0000h} <= Addr[47:0] <= {DramLimitAddr[47:27], 7FF_FFFFh};

DRAM accesses to the local node that are outside of this range are master aborted.

The address of the DRAM transaction is normalized before passing it to the DCTs by subtracting DramBaseAddr.

This range is also used to specify the range of DRAM covered by the scrubber (see [D18F3x58](#) and [D18F3x5C](#)).

Bits	Description
31:21	Reserved. Read-write.
20:0	DramBaseAddr[47:27].

D18F1x124 DRAM Limit System Address

IF (D18F2x118[LockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. See [D18F1x120 \[DRAM Base System Address\]](#).

Bits	Description
31:21	Reserved. Read-write.
20:0	DramLimitAddr[47:27].

23:21	Reserved. Read-write.
20:0	DramLimitAddr[47:27] . IF (BootFromDRAM) THEN Cold reset: 00_003Fh. ELSE Cold reset: 1F_FFFFh. ENDIF.

D18F1x2[1C:00] DRAM Controller Base/Limit

The DRAM controller base and limit registers define a DRAM controller address range and specify the mapping of physical DRAM addresses to a DCT as selected by DctSel or DctIntLvEn. The following base/limit register pairs specify the address ranges:

Table 119: Register Mapping for D18F1x2[1C:00]

Function	Base Address	Limit Address
Range 0	D18F1x200	D18F1x204
Reserved	D18F1x208, D18F1x21[8,0]	D18F1x20C, D18F1x21[C,4]

BIOS should observe the following DCT configuration requirements:

- DRAM addresses are within the defined range if:
 $\{DctBaseAddr[39:27], 000b, 00_0000h\} \leqslant \text{address}[39:0] \leqslant \{DctLimitAddr[39:27], 111b, FF_FFFFh\}$.
- DCT base/limit address ranges must not overlap each other.
- A maximum of two address ranges may be mapped to a single DCT.

Hoisting. When memory hoisting is enabled via LegacyMmioHoleEn, the corresponding DctBaseAddr/DctLimitAddr should be configured to account for the memory hoisted above the hole. A contiguous memory hole should only be mapped by one DctBaseAddr/DctLimitAddr pair. See [2.9.10 \[Memory Hoisting\]](#).

D18F1x2[1,0][8,0] DRAM Controller Base

IF (D18F2x118[LockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0000_0000h.

Table 120: Register Mapping for D18F1x2[1,0][8,0]

Register	Function
D18F1x200	Range 0
D18F1x208	Reserved
D18F1x21[8,0]	Reserved

Bits	Description
31:24	Reserved. Read-write.
23:11	DctBaseAddr[39:27]: DRAM controller base address [39:27]. Read-write. Specifies the base physical address bits for this address range.
10:7	Reserved.

6:4	DctSel: DRAM controller select. Read-write. Specifies the DCT mapped to this address range.						
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td><td>DCT 0</td></tr> <tr> <td style="text-align: center;">111b-010b</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	000b	DCT 0	111b-010b	Reserved
<u>Bits</u>	<u>Definition</u>						
000b	DCT 0						
111b-010b	Reserved						
3	Reserved. Read-write.						
2	Reserved. Read-write.						
1	LgcyMmioHoleEn: legacy mmio hole enable. Read-write. BIOS: See 2.9.10 [Memory Hoisting] . 1=Enable memory hoisting for this address range. BIOS sets this bit for an address range that spans the 4GB boundary and contains a hole for addresses used by MMIO. 0=Memory hoisting is not enabled.						
0	DctAddrVal: DRAM controller address valid. Read-write. 1=Specifies this address range is valid and enabled. 0=This address range is not enabled.						

D18F1x2[1,0][C,4] DRAM Controller LimitIF ([D18F2x118](#)[LockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0000_0000h.

Table 121: Register Mapping for D18F1x2[1,0][C,4]

Register	Function
D18F1x204	Range 0
D18F1x20C	Reserved
D18F1x21[C,4]	Reserved

Bits	Description
31:24	Reserved. Read-write.
23:11	DctLimitAddr[39:27]: DRAM controller limit address bits [39:27]. Read-write. Specifies the limit physical address bits for this address range.
10:4	Reserved.
3:0	Reserved. Read-write.

3.11 Device 18h Function 2 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F2x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1532h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F2x08 Class Code/Revision ID

Reset: 0600_0000h.

Bits	Description
31:8	ClassCode. Read-only. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only.

D18F2x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:0	HeaderTypeReg. Read-only. These bits are fixed at their default values. The header type field indicates that there multiple functions present in this device.

D18F2x[5C:40]_dct[0] DRAM CS Base Address

IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. IF (BootFromDRAM && REG==D18F2x40_dct[0]) THEN Cold reset: 0000_0001h. ELSE Reset: 0000_0000h. ENDIF. See 2.9.3 [DCT Configuration Registers].

These registers along with D18F2x[6C:60]_dct[0] [DRAM CS Mask], translate DRAM request addresses (to a DRAM controller) into DRAM chip selects. Supported DIMM sizes are specified in D18F2x80_dct[0] [DRAM Bank Address Mapping]. For more information on the DRAM controllers, see 2.9 [DRAM Controllers (DCTs)].

For each chip select, there is a DRAM CS Base Address register. For each CS pair there is a DRAM CS Mask Register. For each CS pair, an even CS must be populated if the odd CS is populated.

Table 122: DIMM, Chip Select, and Register Mapping

Base Address Registers	Mask Register	Logical DIMM	Chip Select ¹
D18F2x40_dct[x]	F2x60	0	BP_MEMCS[x]_L[0]
D18F2x44_dct[x]			BP_MEMCS[x]_L[1]

Table 122: DIMM, Chip Select, and Register Mapping

Base Address Registers	Mask Register	Logical DIMM	Chip Select ¹
D18F2x48_dct[x]	F2x64	1	BP_MEMCS[x]_L[2]
D18F2x4C_dct[x]			BP_MEMCS[x]_L[3]
D18F2x[5C:50]_dct[x]	F2x6[C,8]	Reserved	
1. See 2.9.4 [DDR Pad to Processor Pin Mapping]			

The DRAM controller operates on the normalized physical address of the DRAM request. The normalized physical address includes all of the address bits that are supported by a DRAM controller. See [2.8 \[Northbridge \(NB\)\]](#).

Each base address register specifies the starting normalized address of the block of memory associated with the chip select. Each mask register specifies the additional address bits that are consumed by the block of memory associated with the chip selects. If both chip selects of a DIMM are used, they must be the same size; in this case, a single mask register covers the address space consumed by both chip selects.

Lower-order address bits are provided in the base address and mask registers, as well. These allow memory to be interleaved between chip selects, such that contiguous physical addresses map to the same DRAM page of multiple chip selects. See [2.9.9.1 \[Chip Select Interleaving\]](#). The hardware supports the use of lower-order address bits to interleave chip selects if (1) the each chip select of the memory system spans the same amount of memory and (2) the number of chip selects of the memory system is a power of two.

System BIOS is required to assign the largest DIMM chip-select range to the lowest normalized address of the DRAM controller. As addresses increase, the chip-select size is required to remain constant or decrease. This is necessary to keep DIMM chip-select banks on aligned address boundaries, regardless as to the amount of address space covered by each chip select.

For each normalized address for requests that enters a DRAM controller, a ChipSelect[i] is asserted if:

```
CSEnable[i] &
( { (InputAddr[38:27] & ~AddrMask[i][38:27]),
    (InputAddr[21:11] & ~AddrMask[i][21:11]) } ==
  { (BaseAddr[i][38:27] & ~AddrMask[i][38:27]),
    (BaseAddr[i][21:11] & ~AddrMask[i][21:11]) } );
```

Bits	Description
31	Reserved.
30:19	BaseAddr[38:27]: normalized physical base address bits [38:27].
18:16	Reserved.
15:5	BaseAddr[21:11]: normalized physical base address bits [21:11].
4	Reserved.

3	OnDimmMirror: on-DIMM mirroring (ODM) enabled. 1=Address and bank bits are swapped by hardware for MRS commands sent to this chip select. This mode accounts for routing on the DIMM. Hardware bit swapping does not occur for commands sent via D18F2x7C_dct[0][SendMrsCmd] when D18F2x7C_dct[0][EnDramInit] = 0. This bit is expected to be set for the odd numbered rank of unbuffered DDR3 DIMMs if SPD byte 63 indicates that address mapping is mirrored. The following bits are swapped when enabled: <ul style="list-style-type: none">• BA0 and BA1.• A3 and A4.• A5 and A6.• A7 and A8.
2	TestFail: memory test failed. Set by BIOS to indicate that a rank is present but has failed memory training or a memory consistency test, indicating that the memory is bad. BIOS should treat CSEnable=1 and TestFail=1 as mutually exclusive.
1	Reserved. Read-write.
0	CSEnable: chip select enable.

D18F2x[6C:60]_dct[0] DRAM CS Mask

IF ([D18F2x118\[LockDramCfg\]](#) & [~D18F3x12C\[OverrideLockDramCfg\]](#)) THEN Read-only. ELSE Read-write. ENDIF. IF ([BootFromDRAM](#) && (REG==[D18F2x60_dct\[0\]](#))) THEN Cold reset: 0038_FFE0h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [D18F2x\[5C:40\]_dct\[0\]](#).

Bits	Description
31	Reserved.
30:19	AddrMask[38:27]: normalized physical address mask bits [38:27].
18:16	Reserved.
15:5	AddrMask[21:11]: normalized physical address mask bits [21:11].
4	Reserved.
3:2	Reserved.
1:0	Reserved. Read-write.

D18F2x78_dct[0] DRAM Control

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
30:18	Reserved.
17	AddrCmdTriEn: address command tristate enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. BIOS: See 2.9.7.7 . 1=Tristate the address, command, and bank buses when a Deselect command is issued.
15	Reserved. Read-write.

14:11	Reserved.
10:0	Reserved.

D18F2x7C_dct[0] DRAM Initialization

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.7.8 \[DRAM Device and Controller Initialization\]](#).

BIOS can directly control the DRAM initialization sequence using this register. To do so, BIOS sets EnDramInit to start DRAM initialization. BIOS should then complete the initialization sequence specified in the appropriate JEDEC specification. After completing the sequence, BIOS clears EnDramInit to complete DRAM initialization. BIOS should not assert LDTSTOP_L while EnDramInit is set. Setting more than one of the command bits in this register (SendControlWord, SendMrsCmd, and SendAutoRefresh) at a time results in undefined behavior.

Bits	Description
31	EnDramInit: enable DRAM initialization. Read-write. 1=Place the DRAM controller in the BIOS-controlled DRAM initialization mode. The DCT deasserts CKE when this bit is set. BIOS must wait until D18F2x98_dct[0][DctAccessDone] = 1 before programming AssertCke=1 and DeassertMemRstX=1. BIOS must clear this bit after DRAM initialization is complete. BIOS must not set this bit on a DCT with no attached DIMMs.
30	Reserved. Read; write-1-only; cleared-by-hardware.
29	SendZQCmd: send ZQ command. Read; write-1-only; cleared-by-hardware. 1=The DCT sends the ZQ calibration command with either all even or all odd chip selects active. The first command targets even chip selects. Subsequent commands alternate between even and odd chip selects. This bit is cleared by the hardware after the command completes. This bit is valid only when EnDramInit=1. Rtl hardcoded to send a ZQCL command, MrsAddress has no effect.
28	AssertCke: assert CKE. Read-write; S3-check-exclude. Setting this bit causes the DCT to assert the CKE pins. This bit cannot be used to deassert the CKE pins.
27	DeassertMemRstX: deassert memory reset. Read-write; S3-check-exclude. Setting this bit causes the DCT to deassert the memory reset. This bit cannot be used to assert the memory reset pin.
26	SendMrsCmd: send MRS command. Read; write-1-only; cleared-by-hardware. 1=The DCT sends the MRS commands defined by the MrsChipSel, MrsAddress, and MrsBank fields of this register. This bit is cleared by hardware after the command completes. Reserved if D18F2x78_dct[0][AddrCmdTriEn] =1.
25	SendAutoRefresh: send auto refresh command. Read; write-1-only; cleared-by-hardware. 1=The DCT sends an auto refresh command. This bit is cleared by hardware after the command completes.
24	Reserved. Read-write.

23:21	MrsChipSel: MRS command chip select. Read-write; S3-check-exclude. Specifies which DRAM chip select is used for MRS commands. Defined only if (~EnDramInit ~D18F2x90_dct[0][Unbuf-fDimm]); otherwise MRS commands are sent to all chip selects.								
	<table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>MRS command is sent to CS0</td> </tr> <tr> <td>110b-001b</td> <td>MRS command is sent to CS<MrsChipSel></td> </tr> <tr> <td>111b</td> <td>MRS command is sent to CS7</td> </tr> </tbody> </table>	Bits	Description	000b	MRS command is sent to CS0	110b-001b	MRS command is sent to CS<MrsChipSel>	111b	MRS command is sent to CS7
Bits	Description								
000b	MRS command is sent to CS0								
110b-001b	MRS command is sent to CS<MrsChipSel>								
111b	MRS command is sent to CS7								
20:18	MrsBank[2:0]: bank address for MRS commands. Read-write; S3-check-exclude. Specifies the data driven on the DRAM bank pins for MRS commands.								
17:0	MrsAddress[17:0]: address for MRS commands. Read-write; S3-check-exclude. Specifies the data driven on the DRAM address pins for MRS commands.								

D18F2x80_dct[0] DRAM Bank Address Mapping

IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. IF (BootFromDRAM) THEN Cold reset: 0000_000Ah. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). These fields specify DIMM configuration information. These fields are required to be programmed based on the DRAM device size and with information of the DIMM. [Table 123](#) shows the bit numbers for each position.

Bits	Description
31:16	Reserved.
15:8	Reserved. Read-write.
7:4	DimmAddrMap1: DIMM 1 address map.
3:0	DimmAddrMap0: DIMM 0 address map.

Table 123: DDR3 DRAM Address Mapping

Bits	CS Size	Device size, width	Bank			Address																
			2	1	0		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0000b		Reserved				Row																
						Col																
0001b	256MB	512Mb, x16 1Gb, x32	15	14	13	Row	x	x	x	x	17	16	27	26	25	24	23	22	21	20	19	18
						Col	x	x	x	x	x	AP	12	11	10	9	8	7	6	5	4	3
0010b	512MB	512Mb, x8 1Gb, x16 2Gb, x32	15	14	13	Row	x	x	x	17	16	28	27	26	25	24	23	22	21	20	19	18
						Col	x	x	x	x	x	AP	12	11	10	9	8	7	6	5	4	3
0011b		Reserved				Row																
						Col																
0100b		Reserved				Row																
						Col																
0101b	1GB	1Gb, x8 2Gb, x16 4Gb, x32	15	14	13	Row	x	x	17	16	29	28	27	26	25	24	23	22	21	20	19	18
						Col	x	x	x	x	x	AP	12	11	10	9	8	7	6	5	4	3
0110b		Reserved																				

Table 123: DDR3 DRAM Address Mapping

Bits	CS Size	Device size, width	Bank			Address																	
			2	1	0		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0111b	2GB	2Gb, x8	15	14	13	Row	x	17	16	30	29	28	27	26	25	24	23	22	21	20	19	18	
		4Gb, x16 8Gb, x32				Col	x	x	x	x	x	AP	12	11	10	9	8	7	6	5	4	3	
1000b		Reserved																					
1001b		Reserved																					
1010b	4GB	4Gb, x8	15	14	13	Row	17	16	31	30	29	28	27	26	25	24	23	22	21	20	19	18	
		8Gb, x16				Col	x	x	x	x	x	AP	12	11	10	9	8	7	6	5	4	3	
1011b	8GB	8Gb, x8	16	15	14	Row	17	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	
						Col	x	x	x	x	13	AP	12	11	10	9	8	7	6	5	4	3	
1111b- 1100b		Reserved																					

D18F2x84_dct[0] DRAM MRS

IF (BootFromDRAM) THEN Cold reset: 0000_0005h. ELSE Reset: 0000_0005h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). The fields of this register are applied to the MRS during HW DRAM initialization.

Bits	Description
31:24	Reserved.

23	<p>PchgPDModeSel: precharge power down mode select. Read-write. BIOS: 1. Specifies how a chip select enters and exits power down mode. This mode is enabled by D18F2x94_dct[0][PowerDownEn] and its behavior varies based on the setting of D18F2x94_dct[0][PowerDownMode] and MR0[PPD] in D18F2x2E8_dct[0]_mp[1:0][MxMr0]. This register is applied to the MRS during HW DRAM initialization.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>PowerDownMode</u></th><th style="text-align: left;"><u>PchgPDModeSel</u></th><th style="text-align: left;"><u>MR0[PPD]</u></th><th style="text-align: left;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0b</td><td>0b</td><td>0b</td><td>Full channel slow exit (DLL off)</td></tr> <tr> <td>0b</td><td>0b</td><td>1b</td><td>Full channel fast exit (DLL on)</td></tr> <tr> <td>0b</td><td>1b</td><td>xb</td><td>Full channel dynamic fast exit/slow exit</td></tr> <tr> <td>1b</td><td>0b</td><td>0b</td><td>Reserved (Full channel slow exit)</td></tr> <tr> <td>1b</td><td>0b</td><td>1b</td><td>Partial channel fast exit (DLL on)</td></tr> <tr> <td>1b</td><td>1b</td><td>xb</td><td>Partial channel dynamic fast exit/slow exit</td></tr> </tbody> </table> <p>See D18F2x248_dct[0]_mp[1:0][Txpdll, Txp]. In dynamic fast exit/slow exit power down mode, the DCT dynamically issues MRS command(s) to the DRAM to specify the powerdown mode; the DCT specifies fast exit mode when chip selects on one of the two CKEs has recently been active; it specifies deep power down when chip selects on all CKEs have been idle. PchgPDModeSel=0 && MR0[PPD]=1 fast exit modes are reserved if S3 is also supported .</p>	<u>PowerDownMode</u>	<u>PchgPDModeSel</u>	<u>MR0[PPD]</u>	<u>Description</u>	0b	0b	0b	Full channel slow exit (DLL off)	0b	0b	1b	Full channel fast exit (DLL on)	0b	1b	xb	Full channel dynamic fast exit/slow exit	1b	0b	0b	Reserved (Full channel slow exit)	1b	0b	1b	Partial channel fast exit (DLL on)	1b	1b	xb	Partial channel dynamic fast exit/slow exit
<u>PowerDownMode</u>	<u>PchgPDModeSel</u>	<u>MR0[PPD]</u>	<u>Description</u>																										
0b	0b	0b	Full channel slow exit (DLL off)																										
0b	0b	1b	Full channel fast exit (DLL on)																										
0b	1b	xb	Full channel dynamic fast exit/slow exit																										
1b	0b	0b	Reserved (Full channel slow exit)																										
1b	0b	1b	Partial channel fast exit (DLL on)																										
1b	1b	xb	Partial channel dynamic fast exit/slow exit																										
1:0	<p>BurstCtrl: burst length control. Read-write. BIOS: 01b. Specifies the number of sequential beats of DQ related to one read or write command. Requests from the processor are always 64-byte-length. Requests generated by D18F2x250_dct[0] are always 64-byte-length. Requests from GMC may be 32-byte or 64-byte-length. Software must ensure that GMC requests are disabled to configure the DCT and DRAMs for 8-beat burst length (e.g. during training). If this mode is changed, software must issue a mode-register set command to MR0 of the DRAMs to place them in the same mode.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th><th style="text-align: left;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>8 beats</td></tr> <tr> <td>01b</td><td>Dynamic 4 or 8 beats</td></tr> <tr> <td>11b-10b</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	8 beats	01b	Dynamic 4 or 8 beats	11b-10b	Reserved																				
<u>Bits</u>	<u>Description</u>																												
00b	8 beats																												
01b	Dynamic 4 or 8 beats																												
11b-10b	Reserved																												

D18F2x88_dct[0] DRAM Timing Low

IF ([BootFromDRAM](#)) THEN Cold reset: 3E00_0000h. ELSE Reset: 3F00_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description														
31:30	Reserved.														
29:24	<p>MemClkDis: MEMCLK disable. Read-write. 1=Disable the MEMCLK. 0=Enable MEMCLK. All enabled clocks should be 0; all no-connect and unused clocks should be 1.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left;"><u>Bit</u></th><th style="text-align: left;"><u>Pad</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>BP_MEMCLK_H[0]</td></tr> <tr> <td>[1]</td><td>BP_MEMCLK_H[1]</td></tr> <tr> <td>[2]</td><td>BP_MEMCLK_H[2]</td></tr> <tr> <td>[3]</td><td>BP_MEMCLK_H[3]</td></tr> <tr> <td>[4]</td><td>BP_MEMCLK_H[4]</td></tr> <tr> <td>[5]</td><td>BP_MEMCLK_H[5]</td></tr> </tbody> </table>	<u>Bit</u>	<u>Pad</u>	[0]	BP_MEMCLK_H[0]	[1]	BP_MEMCLK_H[1]	[2]	BP_MEMCLK_H[2]	[3]	BP_MEMCLK_H[3]	[4]	BP_MEMCLK_H[4]	[5]	BP_MEMCLK_H[5]
<u>Bit</u>	<u>Pad</u>														
[0]	BP_MEMCLK_H[0]														
[1]	BP_MEMCLK_H[1]														
[2]	BP_MEMCLK_H[2]														
[3]	BP_MEMCLK_H[3]														
[4]	BP_MEMCLK_H[4]														
[5]	BP_MEMCLK_H[5]														
23:0	Reserved.														

D18F2x8C_dct[0] DRAM Timing High

IF ([BootFromDRAM](#)) THEN Cold reset: 0003_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Configuration Registers].

Bits	Description
31:19	Reserved.
18	DisAutoRefresh: disable automatic refresh. Read-write. BIOS: See 2.9.7.7 . 1=Automatic refresh is disabled.
17:16	Tref: refresh rate. Read-write. BIOS: See 2.9.7.5 . This specifies the average time between refresh requests to all DRAM devices. <u>Bits</u> <u>Description</u> 00b Undefined behavior. This is only intended to be used for simulation. Refresh rows on average every X MEMCLKs, where X is a function of the maximum Trfc value for all DIMMs in the system as follows: if Trfc_max=000b, X=768 if Trfc_max=001b, X=768 if Trfc_max=010b, X=1024 if Trfc_max=011b, X=2048 if Trfc_max=1xxb, X=3072 01b Reserved 10b Every 7.8 us 11b Every 3.9 us
15:0	Reserved.

D18F2x90_dct[0] DRAM Configuration Low

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:28	IdleCycLimit: idle cycle limit. Read-write. IF (BootFromDRAM) THEN Cold reset: 8h. ELSE Reset: 8h. ENDIF. BIOS: 8h. Specifies the number of MEMCLK cycles an idle page is open before it is closed if DynPageCloseEn=0. This field is ignored if DynPageCloseEn=1. This field is an upper limit for idle time whereas IdleCycLowLimit is a lower limit. <u>Bits</u> <u>Description</u> 0h 8 clocks Fh-1h <IdleCycLimit>*16 clocks
27	DisDllShutdownSR: disable DLL shutdown in self-refresh mode. Read-write. IF (BootFromDRAM) THEN Cold reset: 1. ELSE Reset: 1. ENDIF. BIOS: See 2.9.7.7 . 1=Disable the power saving features of shutting down DDR phy DLLs during DRAM self refresh and memory P-states. 0=Shutdown DLLs during DRAM self refresh and allow memory P-state transitions.
26	Reserved.
25	PendRefPaybackS3En: pending refresh payback S3 enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 1. Specifies the S3 refresh payback behavior when PendRefPayback=0. 1=Pending refreshes are paid back on S3 entry. 0=Pending refreshes are not paid back on S3 entry.

24	StagRefEn: Stagger Refresh Enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 1. 1=The DRAM controller arbitrates refreshes among chip selects based on the Tstag value (round robin algorithm). See D18F2x228_dct[0] . 0=DCT arbitrates among chip selects using the Trfc value (linear sequential algorithm). See D18F2x208_dct[0] .										
23	ForceAutoPchg: force auto precharging. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: See 2.9.7.7 . 1=Force auto-precharge cycles with every read or write command. In order to meet UMA traffic bandwidth and latency performance targets in the CSRD, specific page hit ratios for display requests must be realized. Setting ForceAutoPchg violates these CSRD targets, and therefore, should not be set in UMA systems. Setting this bit may negatively impact non-UMA (generalized) stutter mode performance as well.										
22:21	IdleCycLowLimit: idle cycle low limit. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. Specifies the number of MEMCLK cycles a page is allowed to be open before it may be closed by the dynamic page close logic. This field is ignored if D18F2x90_dct[0][DynPageCloseEn] = 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>16 clocks</td> </tr> <tr> <td>01b</td> <td>32 clocks</td> </tr> <tr> <td>10b</td> <td>64 clocks</td> </tr> <tr> <td>11b</td> <td>96 clocks</td> </tr> </tbody> </table>	Bits	Description	00b	16 clocks	01b	32 clocks	10b	64 clocks	11b	96 clocks
Bits	Description										
00b	16 clocks										
01b	32 clocks										
10b	64 clocks										
11b	96 clocks										
20	DynPageCloseEn: dynamic page close enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. See 2.9.7.7 [DCT Training Specific Configuration] . 1=The DRAM controller dynamically determines when to close open pages based on the history of that particular page and D18F2x90_dct[0][IdleCycLowLimit] . 0=Any open pages not auto-precharged by the DRAM controller are automatically closed after IdleCycLimit clocks of inactivity.										
19	DimmEccEn: DIMM ECC enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=ECC checking is capable of being enabled for all DIMMs on the DRAM controller by D18F3x44[DramEccEn] . This bit should not be set unless all populated DIMMs support ECC check bits. 0=ECC checking is disabled on the DRAM controller.										
18	PendRefPayback: pending refresh payback. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 0. 1=The DRAM controller executes all pending refresh commands before entering the self refresh state. 0=The controller enters the self refresh state regardless of the number of pending refreshes; applies to any self refresh entry if PendRefPaybackS3En=0, else any non-S3 self refresh entry.										
17	EnterSelfRef: enter self refresh command. Read, write-1-only; cleared-by-hardware. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=The DRAM controller places the DRAMs into self refresh mode. The DRAM interface is tristated 1 MEMCLK after the self refresh command is issued to the DRAMs. Once entered, the DRAM interface must remain in self refresh mode for a minimum of 5 MEMCLKs. This bit is read as a 1 while the enter-self-refresh command is executing; it is read as 0 at all other times.										
16	UnbuffDimm: unbuffered DIMM. IF (~Fuse[UnbDimmDis] & ~Fuse[RegDimmDis]) THEN Read-write ELSE Read-only ENDIF. IF (BootFromDRAM) THEN Cold reset: 1. ELSE Reset: (~Fuse[UnbDimmDis] & Fuse[RegDimmDis]). ENDIF. BIOS: 1. 1=The DRAM controller is connected to unbuffered DIMMs. 0=Reserved.										

15:12	Reserved. Read-write.
11	Reserved.
10	Reserved.
9	Reserved.
8	Reserved. Read-write.
7	Reserved.
6:2	Reserved.
1	ExitSelfRef: exit self refresh (after suspend to RAM or for DRAM training) command. Read, write-1-only; cleared-by-hardware. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. Writing a 1 to this bit causes the DRAM controller to bring the DRAMs out of self refresh mode. It also causes the DRAM controller to issue ZQCL and MRS MR0 commands (using DCT internal versions of the MR0 state). This command should be executed by BIOS when returning from the suspend to RAM state, after the DRAM controller configuration registers are properly initialized, or when self refresh is used during DRAM training. This bit is read as a 1 while the exit-self-refresh command is executing; it is read as 0 at all other times. This bit should not be set if the DCT is disabled.

D18F2x94_dct[0] DRAM Configuration High

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description						
31	DphyMemPsSelEn: Ddr phy MemPsSel enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 1h. ELSE Reset: 1h. ENDIF. BIOS: 1. 1=The DCT uses D18F1x10C[MemPsSel] to select the memory P-state context of a phy register accessed by software with DctOffset[29:20]==0D0h . DctOffset[6] is ignored. 0=Software accesses use DctOffset[6] to select context of those registers. If DctOffset[29:20]!=0D0h then this register has no effect. See D18F2x9C_x0D04_E008_dct[0][PStateToAccess] .						
30:29	Reserved.						
28:24	DcqBypassMax: DRAM controller queue bypass maximum. Read-write. IF (BootFromDRAM) THEN Cold reset: 0Fh. ELSE Reset: 0h. ENDIF. BIOS: 2.9.7.7 . The DRAM controller arbiter normally allows transactions to pass other transactions in order to optimize DRAM bandwidth. This field specifies the maximum number of times that the oldest memory-access request in the DRAM controller queue may be bypassed before the arbiter decision is overridden and the oldest memory-access request is serviced instead. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No bypass; the oldest request is never bypassed.</td> </tr> <tr> <td>1Fh-1h</td> <td>The oldest request may be bypassed no more than <DcqBypassMax> time.</td> </tr> </tbody> </table>	Bits	Description	0h	No bypass; the oldest request is never bypassed.	1Fh-1h	The oldest request may be bypassed no more than < DcqBypassMax > time.
Bits	Description						
0h	No bypass; the oldest request is never bypassed.						
1Fh-1h	The oldest request may be bypassed no more than < DcqBypassMax > time.						

23	ProcOdtDis: processor on-die termination disable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0Fh. ELSE Reset: 0h. ENDIF. 1=The processor-side on-die termination is disabled. 0=Processor-side on-die termination enabled. Changes to this bit must be performed prior to setting MemClkFreqVal.
22	BankSwizzleMode: bank swizzle mode. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 2.9.7.7. 1=Remaps the DRAM device bank address bits as a function of normalized physical address bits. Each of the bank address bits, as specified in D18F2x80_dct[0], are remapped as follows: <ul style="list-style-type: none"> Define X as a bank address bit (e.g., X=15 if the bank bit is specified to be address bit 15). Define S(n) as the state of address bit n (0 or 1) and B as the remapped bank address bit. Then, B= S(X) ^ S(X + 3) ^ S(X + 6); for an 8-bank DRAM. For example, encoding 02h of Table 123 would be remapped from Bank[2:0]={A15, A14, A13} to the following: Bank[2:0] = {A15^A18^A21, A14^A17^A20, A13^A16^A19}.
21	FreqChgInProg: frequency change in progress. Read-only. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=A MEMCLK frequency change is in progress. The DDR phy asserts this bit when it is in the process of locking the PLL. BIOS should not program the phy registers while this bit is set. 0=DRAM-interface commands can be sent to the phy.
20	SlowAccessMode: slow access mode (a.k.a. 2T mode). Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=One additional MEMCLK of setup time is provided on all DRAM address and control signals (not including CS, CKE, and ODT); i.e., these signals are driven for two MEMCLK cycles rather than one. 0=DRAM address and control signals are driven for one MEMCLK cycle. 2T mode may be needed in order to meet electrical requirements of certain DIMM speed and loading configurations. If memory P-states are enabled then BIOS must set this bit if 2T timing is recommended for either memory P-state.
19	Reserved. Reset: 1.
18	Reserved. Read-write.
17	Reserved. Read-write.
16	PowerDownMode: power down mode. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 1. Specifies how a chip select or group of chip selects enters power down mode when enabled by D18F2x94_dct[0][PowerDownEn]. A chip select enters power down mode when the DCT deasserts the CKE pin. The command and address signals tristate one MEMCLK after CKE deasserts. The DCT behavior varies based on the setting of D18F2x84_dct[0][PchgPDModeSel]. See also Table 122 [DIMM, Chip Select, and Register Mapping]. <p>0=Channel CKE control mode; the DRAM channel is placed in power down mode when all chip selects associated with the channel are idle; CKE pins for the channel operate in lock step in terms of placing the channel in power down mode.</p> <p>1=Chip select CKE control mode; the chip select group controlled by a CKE pin is placed in power down mode when no transactions are pending.</p>

15	<p>PowerDownEn: power down mode enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 2.9.7.7.</p> <p>1=Power down mode is enabled. Only precharge power down mode is supported, not active power down mode. See PowerDownMode, D18F2x84_dct[0][PchgPDModeSel], D18F2xA8_dct[0][PrtlChPDEnhEn], AggrPDEn, PDPhyPSDis], and D18F2x248_dct[0]_mp[1:0][PchgPDEnDelay].</p>										
14	<p>DisDramInterface: disable the DRAM interface. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=The DRAM controller is disabled and the DRAM interface is placed into a low power state. This bit must be set if there are no DIMMs connected to the DCT.</p>										
11:10	<p>ZqesInterval: ZQ calibration short interval. Read-write. IF (BootFromDRAM) THEN Cold reset: 00b. ELSE Reset: 00b. ENDIF. BIOS: See 2.9.7.7. This field specifies the programmable interval for the controller to send out the DRAM ZQ calibration short command.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>ZQ calibration short command is disabled</td> </tr> <tr> <td>01b</td> <td>64 ms</td> </tr> <tr> <td>10b</td> <td>128 ms</td> </tr> <tr> <td>11b</td> <td>256 ms</td> </tr> </tbody> </table>	Bits	Description	00b	ZQ calibration short command is disabled	01b	64 ms	10b	128 ms	11b	256 ms
Bits	Description										
00b	ZQ calibration short command is disabled										
01b	64 ms										
10b	128 ms										
11b	256 ms										
9:8	Reserved.										
7	<p>MemClkFreqVal: memory clock frequency valid. Read-write. Reset: 0. System BIOS should set this bit after setting up D18F2x94_dct[0][MemClkFreq] to the proper value. This indicates to the DRAM controller that it may start driving MEMCLK at the proper frequency. This bit should not be set if the DCT is disabled. BIOS must change each DCT's operating frequency in order. See 2.9.7.4.2 [DRAM Channel Frequency Change].</p>										
6:5	Reserved. Reserved for future expansion of MemClkFreq.										
4:0	<p>MemClkFreq: memory clock frequency. Read-write. IF (BootFromDRAM) THEN Cold reset: 010b. ELSE Reset: 000b. ENDIF. Specifies the frequency and rate of the DRAM interface (MEMCLK). See: Table 124 [Valid Values for Memory Clock Frequency Value Definition]. The rate is twice the frequency. See D18F5x84[DdrMaxRate] and D18F5x84[DdrMaxRateEnf]. See MemClkFreqVal.</p>										

Table 124: [Valid Values for Memory Clock Frequency Value Definition](#)

Bits	Description
04h	333 MHz. (667 MT/s)
06h	400 MHz. (800 MT/s)
0Ah	533 MHz. (1066 MT/s)
0Eh	667 MHz. (1333 MT/s)
12h	800 MHz. (1600 MT/s)
16h	933 MHz. (1866 MT/s)
19h	1050 MHz. (2100 MT/s)
1Ah	1066 MHz. (2133 MT/s)

D18F2x98_dct[0] DRAM Controller Additional Data Offset

Reset: 8000_0000h. See [2.9.3 \[DCT Configuration Registers\]](#).

Each DCT includes an array of registers that are used primarily to control DRAM-interface electrical parameters. Access to these registers is accomplished as follows:

Reads:

1. Write the register number to [D18F2x98_dct\[0\]\[DctOffset\]](#) with [D18F2x98_dct\[0\]\[DctAccessWrite\]=0](#).
2. Read the register contents from [D18F2x9C_dct\[0\]](#).

Writes:

1. Write all 32 bits of register data to [D18F2x9C_dct\[0\]](#) (individual byte writes are not supported).
2. Write the register number to [D18F2x98_dct\[0\]\[DctOffset\]](#) with [D18F2x98_dct\[0\]\[DctAccessWrite\]=1](#).
 - The data will be delivered to the phy similar to a posted memory-write, and the write will complete without any further action. However, to ensure that the contents of the array register write have been delivered to the phy, software issues a subsequent configuration register read or write to any register in the northbridge. For example, reading [D18F2x98_dct\[0\]](#) will accomplish this.

Registers for which there is one instance per memory P-state (listed with “_mp[1:0]” appended to the register mnemonic) use [D18F1x10C\[MemPsSel\]](#), [D18F2x94_dct\[0\]\[DphyMemPsSelEn\]](#), and [D18F2x9C_x0D04_E008_dct\[0\]\[PStateToAccess\]](#) for software accesses. BIOS programs these fields appropriately to ensure consistency of registers with controller fields and DDR phy fields.

- [D18F2x9C_x0000_0\[3:0\]0\[3:1\].dct\[0\].mp\[1:0\]](#) refers to all instances of the [D18F2x9C_x0000_0\[3:0\]0\[3:1\]](#) register.
- [D18F2x9C_x0000_0\[3:0\]0\[3:1\].dct\[0\].mp\[1\]](#) refers to the register for memory P-state 1 of either or both DCTs.
- It is recommended that BIOS program context sensitive registers in batches (training/restoring all registers of a context before selecting a new context). BIOS should do the following prior to a new “batch”:
 - Program [D18F2x94_dct\[0\]\[DphyMemPsSelEn\]=1](#).
 - Program [D18F2x9C_x0D04_E008_dct\[0\]\[PStateToAccess\]=target](#).
 - Program [D18F1x10C\[MemPsSel\]=target](#).

Writes to any register in this additional address space causes the FIFO pointers to be reset. Therefore, it is recommended that only BIOS write these registers.

Reads or writes to any register in this additional address space collide with system self-refresh requests. Once power management is enabled software should temporarily disable power management prior to accessing these registers.

Bits	Description
30	DctAccessWrite: DRAM controller read/write select. RAZ; write. 0=Specifies a read access. 1=Specifies a write access.
29:0	DctOffset: DRAM controller offset. Read-write.

D18F2x9C_dct[0] DRAM Controller Additional Data Port

Reset: 0000_0000h. S3-check-exclude. See [D18F2x98_dct\[0\]](#) for register access information. See [2.9.3 \[DCT Configuration Registers\]](#). Address: [D18F2x98_dct\[0\]\[DctOffset\]](#).

Bits	Description
31:0	Data. Read-write.

D18F2x9C_x0000_0000_dct[0]_mp[1:0] DRAM Output Driver Compensation Control

See [2.9.7.6.6 \[DRAM Address Timing and Output Driver Compensation Control\]](#).

Bits	Description																		
31	Reserved.																		
30:28	ProcOdt: processor on-die termination. Read-write. Cold reset: 011b. Specifies the resistance of the on-die termination resistors. This field is valid only when D18F2x94_dct[0][ProcOdtDis]=0 . <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>240 ohms +/- 20%</td> </tr> <tr> <td>001b</td> <td>120 ohms +/- 20%</td> </tr> <tr> <td>010b</td> <td>80 ohms +/- 20%</td> </tr> <tr> <td>011b</td> <td>60 ohms +/- 20%</td> </tr> <tr> <td>111b-100b</td> <td>Reserved 80 ohms +/- 20%</td> </tr> </tbody> </table>	Bits	Description	000b	240 ohms +/- 20%	001b	120 ohms +/- 20%	010b	80 ohms +/- 20%	011b	60 ohms +/- 20%	111b-100b	Reserved 80 ohms +/- 20%						
Bits	Description																		
000b	240 ohms +/- 20%																		
001b	120 ohms +/- 20%																		
010b	80 ohms +/- 20%																		
011b	60 ohms +/- 20%																		
111b-100b	Reserved 80 ohms +/- 20%																		
27:23	Reserved.																		
22:20	DqsDrvStren: DQS drive strength. Read-write. Cold reset: 011b. Specifies the drive strength of the DQS pins. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0.75x</td> </tr> <tr> <td>001b</td> <td>1.0x</td> </tr> <tr> <td>010b</td> <td>1.25x</td> </tr> <tr> <td>011b</td> <td>1.5x</td> </tr> <tr> <td>100b</td> <td>0.0x. Driver disabled.</td> </tr> <tr> <td>101b</td> <td>Reserved (0.5x)</td> </tr> <tr> <td>110b</td> <td>0.5x</td> </tr> <tr> <td>111b</td> <td>Reserved (0.75x)</td> </tr> </tbody> </table>	Bits	Description	000b	0.75x	001b	1.0x	010b	1.25x	011b	1.5x	100b	0.0x. Driver disabled.	101b	Reserved (0.5x)	110b	0.5x	111b	Reserved (0.75x)
Bits	Description																		
000b	0.75x																		
001b	1.0x																		
010b	1.25x																		
011b	1.5x																		
100b	0.0x. Driver disabled.																		
101b	Reserved (0.5x)																		
110b	0.5x																		
111b	Reserved (0.75x)																		
19	Reserved.																		
18:16	DataDrvStren: data drive strength. Read-write. Cold reset: 011b. This field specifies the drive strength of the DRAM data pins. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0.75x</td> </tr> <tr> <td>001b</td> <td>1.0x</td> </tr> <tr> <td>010b</td> <td>1.25x</td> </tr> <tr> <td>011b</td> <td>1.5x</td> </tr> <tr> <td>100b</td> <td>0.0x. Driver disabled.</td> </tr> <tr> <td>101b</td> <td>Reserved (0.5x)</td> </tr> <tr> <td>110b</td> <td>0.5x</td> </tr> <tr> <td>111b</td> <td>Reserved (0.75x)</td> </tr> </tbody> </table> This field is applied to DM signals as well.	Bits	Description	000b	0.75x	001b	1.0x	010b	1.25x	011b	1.5x	100b	0.0x. Driver disabled.	101b	Reserved (0.5x)	110b	0.5x	111b	Reserved (0.75x)
Bits	Description																		
000b	0.75x																		
001b	1.0x																		
010b	1.25x																		
011b	1.5x																		
100b	0.0x. Driver disabled.																		
101b	Reserved (0.5x)																		
110b	0.5x																		
111b	Reserved (0.75x)																		
15	Reserved.																		

14:12	ClkDrvStren: MEMCLK drive strength. Read-write. Cold reset: 011b. This field specifies the drive strength of the MEMCLK pins.																		
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>1.0x</td></tr> <tr> <td>001b</td><td>1.25x</td></tr> <tr> <td>010b</td><td>1.5x</td></tr> <tr> <td>011b</td><td>2.0x</td></tr> <tr> <td>100b</td><td>0.0x. Driver disabled.</td></tr> <tr> <td>101b</td><td>0.75x</td></tr> <tr> <td>110b</td><td>0.5x</td></tr> <tr> <td>111b</td><td>Reserved 1.0x</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	000b	1.0x	001b	1.25x	010b	1.5x	011b	2.0x	100b	0.0x. Driver disabled.	101b	0.75x	110b	0.5x	111b	Reserved 1.0x
<u>Bits</u>	<u>Description</u>																		
000b	1.0x																		
001b	1.25x																		
010b	1.5x																		
011b	2.0x																		
100b	0.0x. Driver disabled.																		
101b	0.75x																		
110b	0.5x																		
111b	Reserved 1.0x																		
11	Reserved.																		
10:8	AddrCmdDrvStren: address/command drive strength. Read-write. Cold reset: 011b. This field specifies the drive strength of the address, RAS, CAS, WE, bank and parity pins.																		
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>1.0x</td></tr> <tr> <td>001b</td><td>1.25x</td></tr> <tr> <td>010b</td><td>1.5x</td></tr> <tr> <td>011b</td><td>2.0x</td></tr> <tr> <td>100b</td><td>0.0x. Driver disabled.</td></tr> <tr> <td>101b</td><td>0.75x</td></tr> <tr> <td>110b</td><td>0.5x</td></tr> <tr> <td>111b</td><td>Reserved 1.0x</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	000b	1.0x	001b	1.25x	010b	1.5x	011b	2.0x	100b	0.0x. Driver disabled.	101b	0.75x	110b	0.5x	111b	Reserved 1.0x
<u>Bits</u>	<u>Description</u>																		
000b	1.0x																		
001b	1.25x																		
010b	1.5x																		
011b	2.0x																		
100b	0.0x. Driver disabled.																		
101b	0.75x																		
110b	0.5x																		
111b	Reserved 1.0x																		
7	Reserved.																		
6:4	CsOdtDrvStren: CS/ODT drive strength. Read-write. Cold reset: 011b. This field specifies the drive strength of the CS and ODT pins.																		
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>1.0x</td></tr> <tr> <td>001b</td><td>1.25x</td></tr> <tr> <td>010b</td><td>1.5x</td></tr> <tr> <td>011b</td><td>2.0x</td></tr> <tr> <td>100b</td><td>0.0x. Driver disabled.</td></tr> <tr> <td>101b</td><td>0.75x</td></tr> <tr> <td>110b</td><td>0.5x</td></tr> <tr> <td>111b</td><td>Reserved 1.0x</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	000b	1.0x	001b	1.25x	010b	1.5x	011b	2.0x	100b	0.0x. Driver disabled.	101b	0.75x	110b	0.5x	111b	Reserved 1.0x
<u>Bits</u>	<u>Description</u>																		
000b	1.0x																		
001b	1.25x																		
010b	1.5x																		
011b	2.0x																		
100b	0.0x. Driver disabled.																		
101b	0.75x																		
110b	0.5x																		
111b	Reserved 1.0x																		

3	Reserved.																		
2:0	CkeDrvStren: CKE drive strength. Read-write. Cold reset: 011b. This field specifies the drive strength of the CKE pins. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>1.0x</td> </tr> <tr> <td>001b</td> <td>1.25x</td> </tr> <tr> <td>010b</td> <td>1.5x</td> </tr> <tr> <td>011b</td> <td>2.0x</td> </tr> <tr> <td>100b</td> <td>0.0x. Driver disabled.</td> </tr> <tr> <td>101b</td> <td>0.75x</td> </tr> <tr> <td>110b</td> <td>0.5x</td> </tr> <tr> <td>111b</td> <td>Reserved 1.0x</td> </tr> </tbody> </table>	Bits	Description	000b	1.0x	001b	1.25x	010b	1.5x	011b	2.0x	100b	0.0x. Driver disabled.	101b	0.75x	110b	0.5x	111b	Reserved 1.0x
Bits	Description																		
000b	1.0x																		
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101b	0.75x																		
110b	0.5x																		
111b	Reserved 1.0x																		

D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0] DRAM Write Data TimingBIOS: See [2.9.7.9.4 \[DQS Position Training\]](#).**Table 125:** Index Mapping for D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0000_0001h	DIMM/CS 0 Bytes 3-0
0000_0002h	DIMM/CS 0 Bytes 7-4
0000_0003h	DIMM/CS 0 ECC
0000_0101h	DIMM/CS 1 Bytes 3-0
0000_0102h	DIMM/CS 1 Bytes 7-4
0000_0103h	DIMM/CS 1 ECC
0000_0201h	Reserved/CS 2 Bytes 3-0
0000_0202h	Reserved/CS 2 Bytes 7-4
0000_0203h	Reserved/CS 2 ECC
0000_0301h	Reserved/CS 3 Bytes 3-0
0000_0302h	Reserved/CS 3 Bytes 7-4
0000_0303h	Reserved/CS 3 ECC

Table 126: Byte Lane Mapping for D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0]

Register	Bits			
	31:24	23:16	15:8	7:0
D18F2x9C_x0000_0[3:0]01_dct[0]_mp[1:0]	Byte3	Byte2	Byte1	Byte0
D18F2x9C_x0000_0[3:0]02_dct[0]_mp[1:0]	Byte7	Byte6	Byte5	Byte4
D18F2x9C_x0000_0[3:0]03_dct[0]_mp[1:0]	Reserved	Reserved	Reserved	ECC

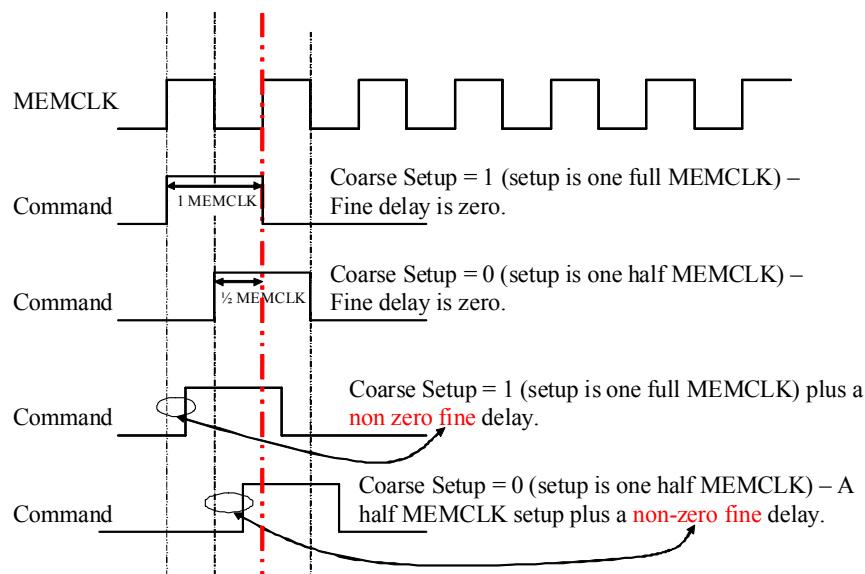
If D18F2xA8_dct[0][PerRankTimingEn]=1 then the function is CS. Otherwise the function is DIMM.

These registers control the timing of write DQ with respect to MEMCLK and allow transmit DQS to be centered in the data eye. The delay starts 1 UI before the rising edge of MEMCLK corresponding to the CAS-write-latency. See [2.9.7.9 \[DRAM Training\]](#). WrDatGrossDly must be programmed for a given DIMM and lane such that WrDatDly - WrDqsDly <= 0.5 MEMCLKs.

Bits	Description										
31:29	WrDatGrossDly: write data gross delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][7:5].										
28:24	WrDatFineDly: write data fine delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][4:0].										
23:21	WrDatGrossDly: write data gross delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][7:5].										
20:16	WrDatFineDly: write data fine delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][4:0].										
15:13	WrDatGrossDly: write data gross delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][7:5].										
12:8	WrDatFineDly: write data fine delay. See: D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0][4:0].										
7:5	WrDatGrossDly: write data gross delay. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>No delay</td> </tr> <tr> <td>001b</td> <td>0.5 MEMCLK delay</td> </tr> <tr> <td>110b-010b</td> <td><WrDatGrossDly>/2 MEMCLK delay</td> </tr> <tr> <td>111b</td> <td>3.5 MEMCLK delay</td> </tr> </tbody> </table> <p>Verification constraints: WrDatGrossDly must be programmed to ensure that WrDatGrossDly - D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][WrDqsGrossDly] <= 0.5 MEMCLKs.</p>	Bits	Description	000b	No delay	001b	0.5 MEMCLK delay	110b-010b	<WrDatGrossDly>/2 MEMCLK delay	111b	3.5 MEMCLK delay
Bits	Description										
000b	No delay										
001b	0.5 MEMCLK delay										
110b-010b	<WrDatGrossDly>/2 MEMCLK delay										
111b	3.5 MEMCLK delay										
4:0	WrDatFineDly: write data fine delay. Read-write. Cold reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><WrDatFineDly>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<WrDatFineDly>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay		
Bits	Description										
00h	0/64 MEMCLK delay										
1Eh-01h	<WrDatFineDly>/64 MEMCLK delay										
1Fh	31/64 MEMCLK delay										

D18F2x9C_x0000_0004_dct[0]_mp[1:0] DRAM Address/Command Timing Control

BIOS: 2.9.7.6.6.

**Figure 8: Address/Command Timing at the Processor Pins**

This register controls the timing of the address, command, chip select, ODT and clock enable pins with respect to MEMCLK as shown in [Figure 8](#). See [2.9.7.4.2 \[DRAM Channel Frequency Change\]](#) and [2.9.7.4.3 \[Phy Fence Programming\]](#). 2T timing is controlled by [D18F2x94_dct\[0\]\[SlowAccessMode\]](#). If a setup time (coarse delay) field is changed and [D18F2x94_dct\[0\]\[MemClkFreqVal\]=1](#), then software must toggle MemClkFreqVal for the delay to take effect.

Bits	Description								
31:22	Reserved.								
21	AddrCmdSetup: address/command setup time. Read-write. Reset: 0. Selects the default setup time for the address and command pins versus MEMCLK. 0=1/2 MEMCLK (1 1/2 MEMCLK for 2T timing). 1=1 MEMCLK (2 MEMCLKs for 2T timing).								
20:16	AddrCmdFineDelay: address/command fine delay. Specifies the time that the address and command pins are delayed from the default setup time. See: CkeFineDelay.								
15:14	Reserved.								
13	CsOdtSetup: CS/ODT setup time. Selects the default setup time for the CS and ODT pins versus MEMCLK. See: CkeSetup.								
12:8	CsOdtFineDelay: CS/ODT fine delay. Specifies the time that the CS and ODT pins are delayed from the default setup time. See: CkeFineDelay.								
7:6	Reserved.								
5	CkeSetup: CKE setup time. Read-write. Reset: 0. Selects the default setup time for the CKE pins versus MEMCLK. 0=1/2 MEMCLK. 1=1 MEMCLK.								
4:0	CkeFineDelay: CKE fine delay. Read-write. Cold reset: 00h. Specifies the time that the CKE pins are delayed from the default setup time. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><CkeFineDelay>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<CkeFineDelay>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay
Bits	Description								
00h	0/64 MEMCLK delay								
1Eh-01h	<CkeFineDelay>/64 MEMCLK delay								
1Fh	31/64 MEMCLK delay								

D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0] DRAM Read DQS Timing

Table 127: Index Mapping for D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0000_0005h	DIMM/CS 0 Bytes 3-0
0000_0006h	DIMM/CS 0 Bytes 7-4
0000_0007h	DIMM/CS 0 ECC
0000_0105h	DIMM/CS 1 Bytes 3-0
0000_0106h	DIMM/CS 1 Bytes 7-4
0000_0107h	DIMM/CS 1 ECC
0000_0205h	Reserved/CS 2 Bytes 3-0
0000_0206h	Reserved/CS 2 Bytes 7-4
0000_0207h	Reserved/CS 2 ECC
0000_0305h	Reserved/CS 3 Bytes 3-0
0000_0306h	Reserved/CS 3 Bytes 7-4
0000_0307h	Reserved/CS 3 ECC

Table 128: Byte Lane Mapping for D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0]

Register	Bits			
	29:25	21:17	13:9	5:1
D18F2x9C_x0000_0[3:0]05_dct[0]_mp[1:0]	Byte3	Byte2	Byte1	Byte0
D18F2x9C_x0000_0[3:0]06_dct[0]_mp[1:0]	Byte7	Byte6	Byte5	Byte4
D18F2x9C_x0000_0[3:0]07_dct[0]_mp[1:0]	Reserved	Reserved	Reserved	ECC

If D18F2xA8_dct[0][PerRankTimingEn]=1 then the function is CS. Otherwise the function is DIMM.

These registers control the timing of read (input) DQS signals with respect to DQ. See [2.9.7.9 \[DRAM Training\]](#). Writes to D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0] set

D18F2x9C_x0D0F_0[F,8:0]2[3:0]_dct[0]_mp[1:0][RdDqsTimeU, RdDqsTimeL] = {RdDqsTime, RdDqsTime}. Reads from D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0] return

D18F2x9C_x0D0F_0[F,8:0]2[3:0]_dct[0]_mp[1:0][RdDqsTimeL].

The actual delay applied to the DQS input signal before sampling data includes an internal part dependent (insertion) delay plus the nominal delay specified by the register setting.

Bits	Description								
31:30	Reserved.								
29:25	RdDqsTime: read DQS timing control. See: D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0][5:1] .								
24:22	Reserved.								
21:17	RdDqsTime: read DQS timing control. See: D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0][5:1] .								
16:14	Reserved.								
13:9	RdDqsTime: read DQS timing control. See: D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0][5:1] .								
8:6	Reserved.								
5:1	RdDqsTime: read DQS timing control. Read-write. Cold reset: 0Fh. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><RdDqsTime>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<RdDqsTime>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay
Bits	Description								
00h	0/64 MEMCLK delay								
1Eh-01h	<RdDqsTime>/64 MEMCLK delay								
1Fh	31/64 MEMCLK delay								
0	Reserved.								

D18F2x9C_x0000_0008_dct[0]_mp[1:0] DRAM Phy Control

Cold reset: 0208_0000h. See [2.9.7.9 \[DRAM Training\]](#). This register also provides access to the multiplier and divider values used in the DDR phy. The default values for the given MEMCLK frequency of the PLL when D18F2x94_dct[0][MemClkFreqVal]=1 can be found: [MACOREPLL Spec:1.4.3.1 Suggested DDR Phy Frequency Settings for 100Mhz RefClk].

Bits	Description
31	Reserved. Read-write.
30	DisAutoComp: disable automatic compensation. Read-write. BIOS: See 2.9.7.4.4 . 1=Disable the compensation control state machine. 0=The phy automatic compensation engine is enabled.
29	DisablePredriverCal: disable predriver calibration. Read-write. BIOS: See 2.9.7.4.4 . 1=Disable the update of predriver codes to all pads.

13	DqsRcvTrEn: DQS receiver training enable. Read-write. 1=Initiate hardware assisted read DQS receiver training. The phy waits for back to back read requests from the DCT (using the read pending signal), discards the first 20 UI worth of DQS samples to account for asynchronous read return latency, and enables the PRE for updating using subsequent samples until the read pipeline is interrupted with a deassertion of read pending. At that time, the PRE will stop updating regardless of the state of this bit, and waits for another string of back to back read requests. During the time that the PRE is enabled for sampling, the phy starts in high gain mode, where two samples contribute to one LSB of phase change; this persists for 64 samples. The phy then changes to a low gain mode, where 32 samples contribute to one LSB of phase change. A minimum of 400 samples will assure convergence. This can be accomplished with multiple strings of reads of at least 56 UI. 0=Stop read DQS receiver training. This allows BIOS to reliably read the DQS receiver training data.										
12	WrLvOdtEn: write levelization ODT enabled. Read-write. 1=ODT specified by WrLvOdt is enabled during write levelization training. 0=ODT is disabled during write levelization training.										
11:8	WrLvOdt: write levelization ODT. Read-write; S3-check-exclude. Specifies the state of the ODT pins when WrLvOdtEn is set. 1=ODT is enabled. 0=ODT is disabled. See 2.9.7.6.5 [DRAM ODT Control] . Tri-state enable for ODT is turned off by the phy when WrLvOdtEn=1. <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Pad</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>BP_MEMODT[0][0]</td> </tr> <tr> <td>[1]</td> <td>BP_MEMODT[0][1]</td> </tr> <tr> <td>[2]</td> <td>BP_MEMODT[0][2]</td> </tr> <tr> <td>[3]</td> <td>BP_MEMODT[0][3]</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Pad</u>	[0]	BP_MEMODT[0][0]	[1]	BP_MEMODT[0][1]	[2]	BP_MEMODT[0][2]	[3]	BP_MEMODT[0][3]
<u>Bit</u>	<u>Pad</u>										
[0]	BP_MEMODT[0][0]										
[1]	BP_MEMODT[0][1]										
[2]	BP_MEMODT[0][2]										
[3]	BP_MEMODT[0][3]										
7:6	FenceTrSel: fence train select. Read-write; S3-check-exclude. Specifies the flop to be used for phy based fence training. See PhyFenceTrEn. This field is shared by D18F2x9C_x0000_0008_dct[0]_mp0 and D18F2x9C_x0000_0008_dct[0]_mp1. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>PRE flop (legacy 45nm phy fence training)</td> </tr> <tr> <td>01b</td> <td>RxDll flop (applies to DqsRcvEn timing)</td> </tr> <tr> <td>10b</td> <td>TxDll flop (applies to RxValid timing only during DqsRcvEn training)</td> </tr> <tr> <td>11b</td> <td>TxPad flop (applies to WrDat, WrDqs, and Addr/Cmd/Cs/Odt/Cke timing)</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	PRE flop (legacy 45nm phy fence training)	01b	RxDll flop (applies to DqsRcvEn timing)	10b	TxDll flop (applies to RxValid timing only during DqsRcvEn training)	11b	TxPad flop (applies to WrDat, WrDqs, and Addr/Cmd/Cs/Odt/Cke timing)
<u>Bits</u>	<u>Description</u>										
00b	PRE flop (legacy 45nm phy fence training)										
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11b	TxPad flop (applies to WrDat, WrDqs, and Addr/Cmd/Cs/Odt/Cke timing)										
5:4	TrChipSel: training DIMM select. Read-write; S3-check-exclude. Specifies a timing control for a corresponding rank which is to be trained. If D18F2xA8_dct[0][PerRankTimingEn] =1 then the function is CS. Otherwise the function is DIMM. This field also selects which bit of the x4DIMM field is used (which is then used to determine which nibble is trained). To ensure complete consistency with 45nm product phy based training, if PerRankTimingEn=1 then x4DIMM[] must be zero. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>DIMM/CS 0</td> </tr> <tr> <td>01b</td> <td>DIMM/CS 1</td> </tr> <tr> <td>10b</td> <td>DIMM:Reserved/CS 2</td> </tr> <tr> <td>11b</td> <td>DIMM:Reserved/CS 3</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	DIMM/CS 0	01b	DIMM/CS 1	10b	DIMM:Reserved/CS 2	11b	DIMM:Reserved/CS 3
<u>Bits</u>	<u>Description</u>										
00b	DIMM/CS 0										
01b	DIMM/CS 1										
10b	DIMM:Reserved/CS 2										
11b	DIMM:Reserved/CS 3										
3	PhyFenceTrEn: phy fence training enable. Read-write. 1=Initiate phy based fence training. 0=Stop the phy based fence training engine.										
2	TrNibbleSel: training nibble select. Read-write. BIOS: 0. Specifies nibbles of each DIMM data byte trained during write levelization training. 0=Lower nibbles. 1=Upper nibbles.										
0	WrtLvTrEn: write levelization training enable. Read-write. 1=Initiate write levelization (tDQSS margining) training. 0=The phy stops driving DQS and exits write levelization training.										

D18F2x9C_x0000_000B_dct[0] DRAM Phy Status Register

Bits	Description
31	DynModeChange: dynamic mode change. RAZ; write. Reset: 0. 1=Phy enters the state specified by PhySelfRefreshMode. When writing a 1 to this bit, values written to bits [22:0] of the register are ignored.
30	PhyPSReq: phy pstate request. RAZ; write. Reset: 0. 1=Phy enters the memory P-state specified by PhyPS. When writing a 1 to this bit, values written to bits [22:0] of the register are ignored.
29:27	Reserved.
26	PhyPS: phy pstate. RAZ; write. Reset: 0. 1=M1. 0=M0. See PhyPSReq.
23	PhySelfRefreshMode: phy self refresh mode. RAZ; write. Reset: 0. 1=Enter self refresh mode. 0=Exit self refresh mode. See DynModeChange.

D18F2x9C_x0000_000C_dct[0] DRAM Phy Miscellaneous

Bits	Description										
31	Reserved.										
30:26	FenceThresholdTxDll: phy fence threshold transmit DLL. Read-write; S3-check-exclude. Cold reset: 13h. BIOS: See 2.9.7.4.3 . This field specifies the fence delay threshold value used to create the fence bit in the DLL delay registers for DQS receiver valid. This field is only used during DQS receiver enable training to time the internal phy signal RxValid. See FenceThresholdTxPad.										
25:21	FenceThresholdRxDll: phy fence threshold DQS receiver enable. Read-write; S3-check-exclude. Cold reset: 13h. BIOS: See 2.9.7.4.3 . This field specifies the fence delay threshold value used to create the fence bit in the DLL delay registers for DQS receiver enable. See FenceThresholdTxPad.										
20:16	FenceThresholdTxPad: phy fence threshold transmit pad. Read-write; S3-check-exclude. Cold reset: 13h. BIOS: See 2.9.7.4.3 . This field specifies the fence delay threshold value used to create the fence bit in the DLL delay registers for write data, write DQS, Addr/Cmd, CS, ODT, and CKE. The corresponding fence bit is set by hardware when the DLL delay register is written if DLL delay >= FenceThresholdTxPad. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><FenceThresholdTxPad>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<FenceThresholdTxPad>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay		
Bits	Description										
00h	0/64 MEMCLK delay										
1Eh-01h	<FenceThresholdTxPad>/64 MEMCLK delay										
1Fh	31/64 MEMCLK delay										
15:12	CKETri: CKE tri-state. Read-write. Cold reset: 0h. 0=The CKE signal is not tri-stated. 1=Tri-state unconnected CKE signal from the processor. See 2.9.4 [DDR Pad to Processor Pin Mapping] . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit</th> <th>Pad</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>BP_MEMCKE[0][0]</td> </tr> <tr> <td>[1]</td> <td>BP_MEMCKE[0][1]</td> </tr> <tr> <td>[2]</td> <td>BP_MEMCKE[0][2]</td> </tr> <tr> <td>[3]</td> <td>BP_MEMCKE[0][3]</td> </tr> </tbody> </table>	Bit	Pad	[0]	BP_MEMCKE[0][0]	[1]	BP_MEMCKE[0][1]	[2]	BP_MEMCKE[0][2]	[3]	BP_MEMCKE[0][3]
Bit	Pad										
[0]	BP_MEMCKE[0][0]										
[1]	BP_MEMCKE[0][1]										
[2]	BP_MEMCKE[0][2]										
[3]	BP_MEMCKE[0][3]										

11:8	ODTTri: ODT tri-state. Read-write. Cold reset: 0h. 0=The ODT signals are not tri-stated unless directed to by the DCT. 1=Tri-state unconnected ODT signals from the processor. See 2.9.4 [DDR Pad to Processor Pin Mapping] .																		
	<table> <thead> <tr> <th>Bit</th> <th>Pad</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>BP_MEMODT[0][0]</td> </tr> <tr> <td>[1]</td> <td>BP_MEMODT[0][1]</td> </tr> <tr> <td>[2]</td> <td>BP_MEMODT[0][2]</td> </tr> <tr> <td>[3]</td> <td>BP_MEMODT[0][3]</td> </tr> </tbody> </table>	Bit	Pad	[0]	BP_MEMODT[0][0]	[1]	BP_MEMODT[0][1]	[2]	BP_MEMODT[0][2]	[3]	BP_MEMODT[0][3]								
Bit	Pad																		
[0]	BP_MEMODT[0][0]																		
[1]	BP_MEMODT[0][1]																		
[2]	BP_MEMODT[0][2]																		
[3]	BP_MEMODT[0][3]																		
7:0	ChipSelTri: chip select tri-state. Read-write. Cold reset: 00h. 0=The chip select signals are not tri-stated unless directed to by the DCT. 1=Tri-state unpopulated chip selects when motherboard termination is available. See 2.9.4 [DDR Pad to Processor Pin Mapping] . ChipSelTri must be programmed to 1b for each pad not connected to a processor pin when D18F2x250_dct[0][LoopbackBistReq]=1 .																		
	<table> <thead> <tr> <th>Bit</th> <th>Pad</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>BP_MEMCS[0]_L[0]</td> </tr> <tr> <td>[1]</td> <td>BP_MEMCS[0]_L[1]</td> </tr> <tr> <td>[2]</td> <td>BP_MEMCS[0]_L[2]</td> </tr> <tr> <td>[3]</td> <td>BP_MEMCS[0]_L[3]</td> </tr> <tr> <td>[4]</td> <td>BP_MEMCS[0]_L[4]</td> </tr> <tr> <td>[5]</td> <td>BP_MEMCS[0]_L[5]</td> </tr> <tr> <td>[6]</td> <td>BP_MEMCS[0]_L[6]</td> </tr> <tr> <td>[7]</td> <td>BP_MEMCS[0]_L[7]</td> </tr> </tbody> </table>	Bit	Pad	[0]	BP_MEMCS[0]_L[0]	[1]	BP_MEMCS[0]_L[1]	[2]	BP_MEMCS[0]_L[2]	[3]	BP_MEMCS[0]_L[3]	[4]	BP_MEMCS[0]_L[4]	[5]	BP_MEMCS[0]_L[5]	[6]	BP_MEMCS[0]_L[6]	[7]	BP_MEMCS[0]_L[7]
Bit	Pad																		
[0]	BP_MEMCS[0]_L[0]																		
[1]	BP_MEMCS[0]_L[1]																		
[2]	BP_MEMCS[0]_L[2]																		
[3]	BP_MEMCS[0]_L[3]																		
[4]	BP_MEMCS[0]_L[4]																		
[5]	BP_MEMCS[0]_L[5]																		
[6]	BP_MEMCS[0]_L[6]																		
[7]	BP_MEMCS[0]_L[7]																		

D18F2x9C_x0000_000D_dct[0].mp[1:0] DRAM Phy DLL Control

Cold Reset: 0000_0000h. This register defines programmable options for the phy's DLLs for power savings. There are two identical sets of configuration registers: one for the transmit DLLs (those running off of the phy's internal PCLK which is running at rate of 2*MEMCLK) and receive DLLs (those running off of the DQS from the DIMMs). These values are programmed by BIOS based on programmed DDR frequency. This register must be programmed before DRAM device initialization.

Bits	Description
31:26	Reserved.
25:24	RxDLLWakeUpTime: receive DLL wakeup time. Read-write. BIOS: See 2.9.7.10 . Specifies the number of PCLKs that the DLL standby signal must deassert prior to a DLL relock event or before read traffic is sent to the receive DLLs.
23	Reserved.
22:20	RxCPUdpPeriod: receive charge pump period. Read-write. BIOS: See 2.9.7.10 . Specifies the number of DLL relocks required to keep the receive DLLs locked for the period where there is no read traffic.
19:16	RxMaxDurDliNoLock: receive maximum duration DLL no lock. Read-write. BIOS: See 2.9.7.7 . Specifies the number of PCLK cycles that occur before the phy DLLs relock. A DLL relock occurs every $2^{RxMaxDurDliNoLock}$ if there are no reads during the period. 0=DLL power saving(standby) disabled. If RxMaxDurDliNoLock!=0 (standby is enabled), D18F2x9C_x0D0F_0[F,8:0]0C_dct[0][DliRstRelock] must be set to 1 prior to writing this register and then DliRstRelock must be cleared after the register write.
15:10	Reserved.

9:8	TxDLLWakeUpTime: transmit DLL wakeup time. Read-write. BIOS: See 2.9.7.10 . Specifies the number of PCLK's that the DLL standby signal must deassert prior to a DLL relock event or before write traffic is sent to transmit DLLs.
7	Reserved.
6:4	TxCPUpdPeriod: transmit charge pump DLL wakeup time. Read-write. BIOS: See 2.9.7.10 . Specifies the number of DLL relocks required to keep the TxDLLs locked for the period where there is no write traffic.
3:0	TxMaxDurDllNoLock: transmit maximum duration DLL no lock. Read-write. BIOS: See 2.9.7.7 . Specifies the number of PCLK cycles that occur before the phy DLLs relock. A DLL relock occurs every $2^{\text{TxMaxDurDllNoLock}}$ if there are no writes during the period. 0=DLL power saving(standby) disabled. If TxMaxDurDllNoLock!=0 (standby is enabled), D18F2x9C_x0D0F_0[F:8:0]0C_dct[0][DllRstRelock] must be set to 1 prior to writing this register and then DllRstRelock must be cleared after the register write.

D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0] DRAM DQS Receiver Enable Timing**Table 129: Index Mapping for D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0]**

D18F2x98_dct[0][31:0]	Function
0000_0010h	DIMM/CS 0 Bytes 1-0
0000_0011h	DIMM/CS 0 Bytes 3-2
0000_0012h	DIMM/CS 0 ECC
0000_0013h	DIMM /CS 1 Bytes 1-0
0000_0014h	DIMM /CS 1 Bytes 3-2
0000_0015h	DIMM /CS 1 ECC
0000_0016h	Reserved /CS 2 Bytes 1-0
0000_0017h	Reserved /CS 2 Bytes 3-2
0000_0018h	Reserved /CS 2 ECC
0000_0019h	Reserved /CS 3 Bytes 1-0
0000_001Ah	Reserved /CS 3 Bytes 3-2
0000_001Bh	Reserved /CS 3 ECC
0000_001[F:C]h	Reserved
0000_0020h	DIMM/CS 0 Bytes 5-4
0000_0021h	DIMM/CS 0 Bytes 7-6
0000_0023h	DIMM /CS 1 Bytes 5-4
0000_0024h	DIMM /CS 1 Bytes 7-6

Table 129: Index Mapping for D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0]

0000_0025h	Reserved
0000_0026h	Reserved /CS 2 Bytes 5-4
0000_0027h	Reserved /CS 2 Bytes 7-6
0000_0029h	Reserved /CS 3 Bytes 5-4
0000_002Ah	Reserved /CS 3 Bytes 7-6

Table 130: Byte Lane Mapping for D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0]

Register	Bits	
	25:16	9:0
D18F2x9C_x0000_001[9,6,3,0]_dct[0]_mp[1:0]	Byte1	Byte0
D18F2x9C_x0000_001[A,7,4,1]_dct[0]_mp[1:0]	Byte3	Byte2
D18F2x9C_x0000_001[B,8,5,2]_dct[0]_mp[1:0]	Reserved	ECC
D18F2x9C_x0000_002[9,6,3,0]_dct[0]_mp[1:0]	Byte5	Byte4
D18F2x9C_x0000_002[A,7,4,1]_dct[0]_mp[1:0]	Byte7	Byte6

If D18F2xA8_dct[0][PerRankTimingEn]=1 then the function is CS. Otherwise the function is DIMM.

Each of these registers control the timing of the receiver enable from the start of the read preamble with respect to MEMCLK. See 2.9.7.9 [DRAM Training]. These delay registers must be programmed such that across all DIMMs and lanes MAX(DqsRcvEnDelay) - MIN(DqsRcvEnDelay) <= 7 UI.

Bits	Description										
31:26	Reserved.										
25:21	DqsRcvEnGrossDelay: DQS receiver enable gross delay. See: D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0][9:5].										
20:16	DqsRcvEnFineDelay: DQS receiver enable fine delay. See: D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0][4:0].										
15:10	Reserved.										
9:5	DqsRcvEnGrossDelay: DQS receiver enable gross delay. Read-write. Reset: 01h. Rule: IF ((NBCOF / DdrRate < 1) && (D18F2x200_dct[0]_mp[1:0][Tcl]=5)) THEN DqsRcvEnGrossDelay >= 1 ENDIF. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>No delay</td></tr> <tr> <td>01h</td> <td>0 MEMCLK delay</td></tr> <tr> <td>1Eh-02h</td> <td><DqsRcvEnGrossDelay>/2 MEMCLK delay</td></tr> <tr> <td>1Fh</td> <td>15.5 MEMCLK delay</td></tr> </tbody> </table>	Bits	Description	00h	No delay	01h	0 MEMCLK delay	1Eh-02h	<DqsRcvEnGrossDelay>/2 MEMCLK delay	1Fh	15.5 MEMCLK delay
Bits	Description										
00h	No delay										
01h	0 MEMCLK delay										
1Eh-02h	<DqsRcvEnGrossDelay>/2 MEMCLK delay										
1Fh	15.5 MEMCLK delay										
4:0	DqsRcvEnFineDelay: DQS receiver enable fine delay. Read-write. Cold reset: 00h. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td></tr> <tr> <td>1Eh-01h</td> <td><DqsRcvEnFineDelay>/64 MEMCLK delay</td></tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td></tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<DqsRcvEnFineDelay>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay		
Bits	Description										
00h	0/64 MEMCLK delay										
1Eh-01h	<DqsRcvEnFineDelay>/64 MEMCLK delay										
1Fh	31/64 MEMCLK delay										

D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0] DRAM DQS Write TimingBIOS: See [2.9.7.9 \[DRAM Training\]](#).**Table 131: Index Mapping for D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0]**

D18F2x98_dct[0][31:0]	Function
0000_0030h	DIMM/CS 0 Bytes 1-0
0000_0031h	DIMM/CS 0 Bytes 3-2
0000_0032h	DIMM/CS 0 ECC
0000_0033h	DIMM /CS 1 Bytes 1-0
0000_0034h	DIMM /CS 1 Bytes 3-2
0000_0035h	DIMM /CS 1 ECC
0000_0036h	Reserved /CS 2 Bytes 1-0
0000_0037h	Reserved /CS 2 Bytes 3-2
0000_0038h	Reserved /CS 2 ECC
0000_0039h	Reserved /CS 3 Bytes 1-0
0000_003Ah	Reserved /CS 3 Bytes 3-2
0000_003Bh	Reserved /CS 3 ECC
0000_0040h	DIMM/CS 0 Bytes 5-4
0000_0041h	DIMM/CS 0 Bytes 7-6
0000_0043h	DIMM /CS 1 Bytes 5-4
0000_0044h	DIMM /CS 1 Bytes 7-6
0000_0046h	Reserved /CS 2 Bytes 5-4
0000_0047h	Reserved /CS 2 Bytes 7-6
0000_0049h	Reserved /CS 3 Bytes 5-4
0000_004Ah	Reserved /CS 3 Bytes 7-6

Table 132: Byte Lane Mapping for D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0]

Register	Bits	
	23:16	7:0
D18F2x9C_x0000_003[9,6,3,0]_dct[0]_mp[1:0]	Byte1	Byte0
D18F2x9C_x0000_003[A,7,4,1]_dct[0]_mp[1:0]	Byte3	Byte2
D18F2x9C_x0000_003[B,8,5,2]_dct[0]_mp[1:0]	Reserved	ECC
D18F2x9C_x0000_004[9,6,3,0]_dct[0]_mp[1:0]	Byte5	Byte4
D18F2x9C_x0000_004[A,7,4,1]_dct[0]_mp[1:0]	Byte7	Byte6

If D18F2xA8_dct[0][PerRankTimingEn]=1 then the function is CS. Otherwise the function is DIMM. Each of these registers control the DQS timing delay for write commands relative to MEMCLK. The delay starts at the rise edge of MEMCLK corresponding to the CAS-writelatency. Each control includes a gross timing field and a fine timing field, the sum of which is the total delay. See 2.9.7.9 [DRAM Training].

Bits	Description										
31:29	Reserved. Read-write.										
28:24	Reserved.										
23:21	WrDqsGrossDly: DQS write gross delay. See: D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][7:5].										
20:16	WrDqsFineDly: DQS write fine delay. See: D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0][4:0].										
15:13	Reserved. Read-write.										
12:8	Reserved.										
7:5	WrDqsGrossDly: DQS write gross delay. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>No delay</td> </tr> <tr> <td>001b</td> <td>0.5 MEMCLK delay</td> </tr> <tr> <td>110b-010b</td> <td><WrDqsGrossDly>/2 MEMCLK delay</td> </tr> <tr> <td>111b</td> <td>3.5 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	000b	No delay	001b	0.5 MEMCLK delay	110b-010b	<WrDqsGrossDly>/2 MEMCLK delay	111b	3.5 MEMCLK delay
Bits	Description										
000b	No delay										
001b	0.5 MEMCLK delay										
110b-010b	<WrDqsGrossDly>/2 MEMCLK delay										
111b	3.5 MEMCLK delay										
4:0	WrDqsFineDly: DQS write fine delay. Read-write. Cold reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><WrDqsFineDly>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<WrDqsFineDly>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay		
Bits	Description										
00h	0/64 MEMCLK delay										
1Eh-01h	<WrDqsFineDly>/64 MEMCLK delay										
1Fh	31/64 MEMCLK delay										

D18F2x9C_x0000_00[52:50]_dct[0] DRAM Phase Recovery Control

These registers are used by BIOS for hardware assisted DRAM training. Writes to these registers seed the phase recovery engine prior to training. Reads from the registers indicate how much the phase recovery engine has advanced to align the MEMCLK and DQS edges and is under hardware control. See 2.9.7.9 [DRAM Training].

Table 133: Index Mapping for D18F2x9C_x0000_00[52:50]_dct[0]

D18F2x98_dct[0][31:0]	Function
0000_0050h	Bytes 3-0
0000_0051h	Bytes 7-4
0000_0052h	ECC

Table 134: Byte Lane Mapping for D18F2x9C_x0000_00[52:50]_dct[0]

Register	Bits			
	31:24	23:16	15:8	7:0
D18F2x9C_x0000_0050_dct[0]	Byte3	Byte2	Byte1	Byte0
D18F2x9C_x0000_0051_dct[0]	Byte7	Byte6	Byte5	Byte4
D18F2x9C_x0000_0052_dct[0]	Reserved	Reserved	Reserved	ECC

Bits	Description										
31	Reserved.										
30:29	PhRecGrossDly: phase recovery gross delay. See: PhRecGrossDly.										
28:24	PhRecFineDly: phase recovery fine delay. See: PhRecFineDly.										
23	Reserved.										
22:21	PhRecGrossDly: phase recovery gross delay. See: PhRecGrossDly.										
20:16	PhRecFineDly: phase recovery fine delay. See: PhRecFineDly.										
15	Reserved.										
14:13	PhRecGrossDly: phase recovery gross delay. See: PhRecGrossDly.										
12:8	PhRecFineDly: phase recovery fine delay. See: PhRecFineDly.										
7	Reserved.										
6:5	PhRecGrossDly: phase recovery gross delay. Read-write; S3-check-exclude. Reset: X. Gross timing indicates the number of half-MEMCLK periods that the phase recovery engine advanced while aligning edges. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No delay</td> </tr> <tr> <td>01b</td> <td>0.5 MEMCLK delay</td> </tr> <tr> <td>10b</td> <td>1.0 MEMCLK delay</td> </tr> <tr> <td>11b</td> <td>1.5 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00b	No delay	01b	0.5 MEMCLK delay	10b	1.0 MEMCLK delay	11b	1.5 MEMCLK delay
Bits	Description										
00b	No delay										
01b	0.5 MEMCLK delay										
10b	1.0 MEMCLK delay										
11b	1.5 MEMCLK delay										
4:0	PhRecFineDly: phase recovery fine delay. Read-write; S3-check-exclude. Reset: X. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>0/64 MEMCLK delay</td> </tr> <tr> <td>1Eh-01h</td> <td><PhRecFineDly>/64 MEMCLK delay</td> </tr> <tr> <td>1Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Description	00h	0/64 MEMCLK delay	1Eh-01h	<PhRecFineDly>/64 MEMCLK delay	1Fh	31/64 MEMCLK delay		
Bits	Description										
00h	0/64 MEMCLK delay										
1Eh-01h	<PhRecFineDly>/64 MEMCLK delay										
1Fh	31/64 MEMCLK delay										

D18F2x9C_x0D0F_0[F,8:0]02_dct[0] Data Byte Transmit PreDriver Calibration

Cold reset: xxxx_xxxxh. BIOS: See 2.9.7.4.4. DBYTE.

Table 135: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]02_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0802h	0702h	0602h	0502h	0402h	0302h	0202h	0102h	0002h
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 136: Broadcast Mapping for D18F2x9C_x0D0F_0[F,8:0]02_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]
	OF02h
0D0Fh	D18F2x9C_x0D0F_0[8:0]02

Table 137: Valid Values for D18F2x9C_x0D0F_0[F,8:0]02_dct[0][TxPreP]

Bits	Description
0h	Slew Rate 0 (slowest)
8h-1h	Reserved
9h	Slew Rate 1
11h-Ah	Reserved
12h	Slew Rate 2
1Ah-13h	Reserved
1Bh	Slew Rate 3
23h-1Ch	Reserved
24h	Slew Rate 4
2Ch-25h	Reserved
2Dh	Slew Rate 5
35h-2Eh	Reserved
36h	Slew Rate 6
3Eh-37h	Reserved
3Fh	Slew Rate 7 (fastest)

Bits	Description
31:16	Reserved.
15	ValidTxAndPre: predriver calibration code valid. Read-write; cleared-by-hardware. 1=Predriver calibration codes are copied from this register and D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0] into the associated transmit pad. Hardware clears this field after the copy is complete.
14:12	Reserved. Read-write.
11:6	TxPreP: PMOS predriver calibration code. Read-write; S3-check-exclude. Specifies the rising edge slew rate of the transmit pad. See: Table 137 [Valid Values for D18F2x9C_x0D0F_0[F,8:0]02_dct[0][TxPreP]]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.
5:0	TxPreN: NMOS predriver calibration code. Read-write; S3-check-exclude. Specifies the falling edge slew rate of the transmit pad. See: Table 137 [Valid Values for D18F2x9C_x0D0F_0[F,8:0]02_dct[0][TxPreP]]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.

D18F2x9C_x0D0F_0[F,8:0]0[B,7,3]_dct[0] Data Byte P0dt Configuration

Cold reset: 0000_xxhh. See D18F2x9C_x0D0F_1C00_dct[0]. DBYTE.

Table 138: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]0[B,7,3]_dct[0]

D18F2x98_dct[0][31:0]	Function
0D0F_000[B,7,3]h	Byte 0
0D0F_010[B,7,3]h	Byte 1
0D0F_020[B,7,3]h	Byte 2
0D0F_030[B,7,3]h	Byte 3
0D0F_040[B,7,3]h	Byte 4
0D0F_050[B,7,3]h	Byte 5
0D0F_060[B,7,3]h	Byte 6
0D0F_070[B,7,3]h	Byte 7
0D0F_080[B,7,3]h	ECC
0D0F_0F0[B,7,3]h	D18F2x9C_x0D0F_0[8:0]0[B,7,3]

Bits	Description
31:16	Reserved.
15:14	Reserved. Read-write.
13:8	PODtD: pmos ODT calibration data. Read-write; S3-check-exclude.
7:6	Reserved. Read-write.
5:0	NOdtD: nmos ODT calibration data. Read-write; S3-check-exclude.

D18F2x9C_x0D0F_0[F,8:0]04_dct[0]_mp[1:0] Data Byte 1.5X Pad Configuration

Cold reset: 0000_0033h. DBYTE.

Table 139: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]04_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_0004h	Byte 0
0D0F_0104h	Byte 1
0D0F_0204h	Byte 2
0D0F_0304h	Byte 3
0D0F_0404h	Byte 4
0D0F_0504h	Byte 5
0D0F_0604h	Byte 6
0D0F_0704h	Byte 7
0D0F_0804h	ECC
0D0F_0F04h	D18F2x9C_x0D0F_0[8:0]04

Bits	Description
13	TriDM: tri-state DM. Read-write. BIOS: 2.9.7.10 . Read-write. Specifies tri-state control for the memory DM signal. 1=Signal is tri-stated. 0=Signal is not tri-stated.

12	POdtOff: processor ODT off. Read-write. BIOS: See 2.9.7.6.6 . 1=Phy disables receiver pad termination. 0=Phy enables receiver pad termination. Hardware programs this field for the current M-state (D18F2x9C_x0D00_E008_dct[0] [PhyPS]) with the value in D18F2x94_dct[0] [ProcOdtDis] (via D18F2x9C_x0000_000B_dct[0] [ProcOdtDis]) when the memory frequency is updated. See 2.9.7.4.2 . BIOS must reprogram this field after each frequency change if the target value differs from D18F2x94_dct[0] [ProcOdtDis].
11:0	Reserved. Read-write.

D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0] Data Byte Transmit PreDriver Calibration 2Cold reset: xxxx_xxxxh. BIOS: See [2.9.7.4.4](#). DBYTE.Table 140: [Index Mapping](#) for D18F2x9C_x0D0F_0[F,8:0]06_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0806h	0706h	0606h	0506h	0406h	0306h	0206h	0106h	0006h
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 141: [Index Mapping](#) for D18F2x9C_x0D0F_0[F,8:0]0A_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	080Ah	070Ah	060Ah	050Ah	040Ah	030Ah	020Ah	010Ah	000Ah
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 142: [Broadcast Mapping](#) for D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0F0Ah				0F06h				
0D0Fh	D18F2x9C_x0D0F_0[8:0]0A					D18F2x9C_x0D0F_0[8:0]06			

Bits	Description
11:6	TxPreP: PMOS predriver calibration code. Read-write. This field specifies the rising edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreP]. After updating this value, BIOS must program D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [ValidTxAndPre]=1 for the change to take effect.
5:0	TxPreN: NMOS predriver calibration code. Read-write. This field specifies the falling edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreN]. After updating this value, BIOS must program D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [ValidTxAndPre]=1 for the change to take effect.

D18F2x9C_x0D0F_0[F,8:0]10_dct[0]_mp[1:0] Data Byte DLL Power Management

Cold reset: 0000_0000h. DBYTE.

Table 143: [Index Mapping](#) for D18F2x9C_x0D0F_0[F,8:0]10_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_0010h	Byte 0
0D0F_0110h	Byte 1

Table 143: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]10_dct[0]_mp[1:0]

0D0F_0210h	Byte 2
0D0F_0310h	Byte 3
0D0F_0410h	Byte 4
0D0F_0510h	Byte 5
0D0F_0610h	Byte 6
0D0F_0710h	Byte 7
0D0F_0810h	Byte 8
0D0F_0F10h	Byte 8-0

Bits	Description
12	EnRxPadStandby: enable receiver pad standby. Read-write. BIOS: See 2.9.7.7 . 1=Phy receiver standby mode is enabled to save power when not receiving data. 0=Phy receiver standby mode is disabled.

D18F2x9C_x0D0F_0[F,8:0]13_dct[0]_mp[1:0] Data Byte DLL Configuration**Table 144: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]13_dct[0]_mp[1:0]**

D18F2x98_dct[0][31:0]	Function
0D0F_0013h	Byte 0
0D0F_0113h	Byte 1
0D0F_0213h	Byte 2
0D0F_0313h	Byte 3
0D0F_0413h	Byte 4
0D0F_0513h	Byte 5
0D0F_0613h	Byte 6
0D0F_0713h	Byte 7
0D0F_0813h	Byte 8
0D0F_0F13h	Byte 8-0

Bits	Description
14	ProcOdtAdv: ProcOdt advance. Read-write. Cold reset: 1. BIOS: IF ((Solder-down DRAM SODIMM) && DdrRate <= 1333) THEN 0 ELSE 1 ENDIF. 0=ProcOdt is asserted 1.5 PCLK before DqsEn (pipeline, untimed). 1=If preceding write, ProcOdt is asserted 2.5 PCLK before DqsEn, else, ProcOdt is asserted 5.0 PCLK before DqsEn. 45nm DDR phy asserted ProcOdt 1.0 PCLK before DqsEn.
13	ExtraProcOdtAdv: extra ProcOdt advance. Read-write. Cold reset: 0. BIOS: 0. Reserved if ProcOdtAdv=0. 1=For a read without preceding read or write commands, ProcOdt is asserted with the CAS command (rising edge of TxActive). 0=Extra ProcOdt is disabled.
12:9	Reserved. Read-write.

8	RxSsbMntClkEn: receive channel maintenance clock enable. Read-write. Cold reset: 0. BIOS: 2.9.7.10 . 1=Enable receive channel maintenance clocks to improve internal timing margin at the cost of some extra power. To enable clock generation, BIOS must first enable maintenance clocks in the DCT (see D18F2x248_dct[0]_mp[1:0][RxChMntClkEn]). 0=Disable clocks. The maintenance clock period is fixed at 8 PCLKs when no traffic occurs.
1	DllDisEarlyU: DLL disable early upper. Read-write. Cold reset: 0. BIOS: See 2.9.7.10 . 1=Disable upper receiver DQS DLL early timing for power savings.
0	DllDisEarlyL: DLL disable early lower. Read-write. Cold reset: 0. BIOS: See 2.9.7.10 . 1=Disable lower receiver DQS DLL early timing for power savings.

D18F2x9C_x0D0F_0[F,8:0]1C_dct[0]_mp[1:0] Data Byte DLL Power Management

Cold reset: 0000_0000h. DBYTE.

Table 145: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]1C_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_001Ch	Byte 0
0D0F_011Ch	Byte 1
0D0F_021Ch	Byte 2
0D0F_031Ch	Byte 3
0D0F_041Ch	Byte 4
0D0F_051Ch	Byte 5
0D0F_061Ch	Byte 6
0D0F_071Ch	Byte 7
0D0F_081Ch	Byte 8
0D0F_0F1Ch	Byte 8-0

Bits	Description
15	RxDllStggrEn: Rx DLL stagger enable. Read-write. BIOS: 2.9.7.10 . 1=Insert RxDllStggrDly delay prior to waking the receive DLLs from standby. 0=DLLs wake from standby at the default pending-activity reference point.
14	Reserved.
13:8	RxDllStggrDly[5:0]: Rx DLL stagger delay. Read-write. BIOS: 2.9.7.10 . Specifies the delay in PCLK cycles from a CAS command or an internal DLL maintenance lock timing event before the receive DLLs exit standby if the data bus is still idle. If data bus traffic is pending and the DLLs are in standby then they wake immediately regardless of the delay value.
7	TxDllStggrEn: Tx DLL stagger enable. Read-write. BIOS: 2.9.7.10 . 1=Insert TxdllStggrDly delay prior to waking the transmit DLL from standby. 0=DLL wakes from standby at the default pending-activity reference point.
6	Reserved.
5:0	TxdllStggrDly[5:0]: Tx DLL stagger delay. Read-write. BIOS: 0. BIOS: 2.9.7.10 . Specifies the delay in PCLK cycles from a CAS command or an internal DLL maintenance lock timing event before the transmit DLL exits standby if the data bus is still idle. If data bus traffic is pending and the DLL is in standby then it wakes immediately regardless of the delay value.

D18F2x9C_x0D0F_0[F,8:0]1E_dct[0]_mp[1:0] Data Byte Receiver Bias Current Control

Cold reset: 0000_5220h. DBYTE.

Table 146: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]1E_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_001Eh	Byte 0
0D0F_011Eh	Byte 1
0D0F_021Eh	Byte 2
0D0F_031Eh	Byte 3
0D0F_041Eh	Byte 4
0D0F_051Eh	Byte 5
0D0F_061Eh	Byte 6
0D0F_071Eh	Byte 7
0D0F_081Eh	Byte 8
0D0F_0F1Eh	Byte 8-0

Bits	Description																		
14:12	DllCSRBiasTrim: dll csr biast trim. Read-write. BIOS: 001b. The MSB bit adjusts the DAC current profile that is used only by the delayline, which adjusts the tuning curve of the delayline. The remaining two bits affect the global bias current. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>-25%</td> </tr> <tr> <td>001b</td> <td>Nominal</td> </tr> <tr> <td>010b</td> <td>+50%</td> </tr> <tr> <td>011b</td> <td>+100</td> </tr> <tr> <td>100b</td> <td>-25% + delayline adjust</td> </tr> <tr> <td>101b</td> <td>Nominal + delayline adjust</td> </tr> <tr> <td>110b</td> <td>+50% + delayline adjust</td> </tr> <tr> <td>111b</td> <td>+100 + delayline adjust</td> </tr> </tbody> </table>	Bits	Description	000b	-25%	001b	Nominal	010b	+50%	011b	+100	100b	-25% + delayline adjust	101b	Nominal + delayline adjust	110b	+50% + delayline adjust	111b	+100 + delayline adjust
Bits	Description																		
000b	-25%																		
001b	Nominal																		
010b	+50%																		
011b	+100																		
100b	-25% + delayline adjust																		
101b	Nominal + delayline adjust																		
110b	+50% + delayline adjust																		
111b	+100 + delayline adjust																		
11:8	Reserved. Read-write.																		
7	Reserved. Read-write.																		
6:0	Reserved. Read-write.																		

D18F2x9C_x0D0F_0[F,8:0]1F_dct[0]_mp[1:0] Data Byte Receiver Configuration

Cold reset: 0000_2003h. DBYTE.

Table 147: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]1F_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_001Fh	Byte 0
0D0F_011Fh	Byte 1
0D0F_021Fh	Byte 2
0D0F_031Fh	Byte 3
0D0F_041Fh	Byte 4
0D0F_051Fh	Byte 5

Table 147: Index Mapping for [D18F2x9C_x0D0F_0\[F,8:0\]1F_dct\[0\]_mp\[1:0\]](#)

0D0F_061Fh	Byte 6
0D0F_071Fh	Byte 7
0D0F_081Fh	Byte 8
0D0F_0F1Fh	Byte 8-0

Bits	Description												
7:5	RxDqInsDly: receive DQ insertion delay. Read-write. BIOS: 2.9.7.9.4 . This control adds insertion delay to the Rx DQ path so that the delay through RxDqs+DLL insertion delay+Clk distribution better matches the DQ data propagation delay. Each stage expected to add 25 to 50 ps to DQ. <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr><td>000b</td><td>Min delay</td></tr> <tr><td>001b</td><td>Delay 1</td></tr> <tr><td>010b</td><td>Delay 2</td></tr> <tr><td>011b</td><td>Max delay</td></tr> <tr><td>111b-100b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	000b	Min delay	001b	Delay 1	010b	Delay 2	011b	Max delay	111b-100b	Reserved
Bits	Description												
000b	Min delay												
001b	Delay 1												
010b	Delay 2												
011b	Max delay												
111b-100b	Reserved												
4:3	RxVioLvl: receiver voltage level. Read-write. BIOS: 2.9.7.4.1 . Specifies the VDDIO voltage level. <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr><td>00b</td><td>1.5 V</td></tr> <tr><td>01b</td><td>1.35 V</td></tr> <tr><td>10b</td><td>1.25 V (Phy spec: 1.2 V)</td></tr> <tr><td>11b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	00b	1.5 V	01b	1.35 V	10b	1.25 V (Phy spec: 1.2 V)	11b	Reserved		
Bits	Description												
00b	1.5 V												
01b	1.35 V												
10b	1.25 V (Phy spec: 1.2 V)												
11b	Reserved												
2:0	Reserved. Read-write.												

D18F2x9C_x0D0F_0[F,8:0]2[3:0]_dct[0]_mp[1:0] Data Byte RxDqs DLL ConfigurationCold reset: 0000_0F0Fh. See [D18F2x9C_x0000_0\[3:0\]0\[7:5\]_dct\[0\]_mp\[1:0\]](#).Table 148: Index Mapping for [D18F2x9C_x0D0F_0\[F,8:0\]2\[3:0\]_dct\[0\]_mp\[1:0\]](#)

D18F2x98_dct[0][31:0]	Function
0D0F_0020h	DIMM/CS 0 Byte 0
0D0F_0120h	DIMM/CS 0 Byte 1
0D0F_0220h	DIMM/CS 0 Byte 2
0D0F_0320h	DIMM/CS 0 Byte 3
0D0F_0420h	DIMM/CS 0 Byte 4
0D0F_0520h	DIMM/CS 0 Byte 5
0D0F_0620h	DIMM/CS 0 Byte 6
0D0F_0720h	DIMM/CS 0 Byte 7
0D0F_0820h	DIMM/CS 0 Byte 8
0D0F_0F20h	DIMM/CS 0 Byte 8-0
0D0F_0021h	DIMM/CS 1 Byte 0
0D0F_0121h	DIMM/CS 1 Byte 1
0D0F_0221h	DIMM/CS 1 Byte 2
0D0F_0321h	DIMM/CS 1 Byte 3
0D0F_0421h	DIMM/CS 1 Byte 4

Table 148: Index Mapping for D18F2x9C_x0D0F_0[F,8:0]2[3:0]_dct[0]_mp[1:0]

0D0F_0521h	DIMM/CS 1 Byte 5
0D0F_0621h	DIMM/CS 1 Byte 6
0D0F_0721h	DIMM/CS 1 Byte 7
0D0F_0821h	DIMM/CS 1 Byte 8
0D0F_0F21h	DIMM/CS 1 Byte 8-0
0D0F_0022h	Reserved/CS 2 Byte 0
0D0F_0122h	Reserved/CS 2 Byte 1
0D0F_0222h	Reserved/CS 2 Byte 2
0D0F_0322h	Reserved/CS 2 Byte 3
0D0F_0422h	Reserved/CS 2 Byte 4
0D0F_0522h	Reserved/CS 2 Byte 5
0D0F_0622h	Reserved/CS 2 Byte 6
0D0F_0722h	Reserved/CS 2 Byte 7
0D0F_0822h	Reserved/CS 2 Byte 8
0D0F_0F22h	Reserved/CS 2 Byte 8-0
0D0F_0023h	Reserved/CS 3 Byte 0
0D0F_0123h	Reserved/CS 3 Byte 1
0D0F_0223h	Reserved/CS 3 Byte 2
0D0F_0323h	Reserved/CS 3 Byte 3
0D0F_0423h	Reserved/CS 3 Byte 4
0D0F_0523h	Reserved/CS 3 Byte 5
0D0F_0623h	Reserved/CS 3 Byte 6
0D0F_0723h	Reserved/CS 3 Byte 7
0D0F_0823h	Reserved/CS 3 Byte 8
0D0F_0F23h	Reserved/CS 3 Byte 8-0

If D18F2xA8_dct[0][PerRankTimingEn]=1 then the function is CS. Otherwise the function is DIMM.

Bits	Description
12:8	RdDqsTimeU: read DQS timing control upper nibble. Read-write. <u>Bits</u> <u>Description</u> 1Fh-00h <RdDqsTimeU>/64 MEMCLK delay
7:5	Reserved. Read-write.
4:0	RdDqsTimeL: read DQS timing control lower nibble. Read-write. <u>Bits</u> <u>Description</u> 1Fh-00h <RdDqsTimeL>/64 MEMCLK delay

D18F2x9C_x0D0F_0[8:0]2[9:4]_dct[0]_mp[1:0] Data Byte DLL Configuration

Cold reset: 0000_0000h. Updated by hardware during 2.9.7.4.3 [Phy Fence Programming].

Bits	Description
31:16	Reserved.
15	FenceBitO: fence bit odd. Read-write.

14	Fence2BitO: fence2 bit odd. Read-write.
13:8	Reserved. Read-write.
7	FenceBitE: fence bit even. Read-write.
6	Fence2BitE: fence2 bit even. Read-write.
5:0	Reserved. Read-write.

D18F2x9C_x0D0F_0[F,8:0]30_dct[0] Data Byte DLL Configuration and Power Down

Cold reset: 0000_0001h. DBYTE.

Table 149: Index Addresses for D18F2x9C_x0D0F_0[F,8:0]30_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0830h	0730h	0630h	0530h	0430h	0330h	0230h	0130h	0030h
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 150: Broadcast Write Index Address for D18F2x9C_x0D0F_0[F,8:0]30_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0F30h								
0D0Fh	D18F2x9C_x0D0F_0[8:0]30								

Bits	Description
9	TxPclkGateEn: tx pclk gating enable. Read-write. BIOS: 2.9.7.10 . 1=DQS TX data pipe PCLK gating is enabled. 0=PCLK gating disabled.
8	BlockRxDqsLock: block rx dqs lock. Read-write. BIOS: 2.9.7.9.3 . Specifies how the receive DLLs lock. 1=Lock on PCLK. 0=Lock on both PCLK and the received DQS
7	PchgPdPClkGateEn: precharge powerdown pclk gating enable. Read-write. BIOS: 2.9.7.10 . 1=Data control pipe PCLK gating is enabled. 0=PCLK gating disabled.
6	DataCtlPipePclkGateEn: data control pipe pclk gating enable. Read-write. BIOS: 2.9.7.10 . 1=Data control pipe PCLK gating is enabled. 0=PCLK gating disabled.
4	PwrDn: power down. Read-write. BIOS: 2.9.7.10 . 1=Turn off DLL circuitry (DLLs, pads, bias macros, regulator).
3:0	Reserved. Read-write.

D18F2x9C_x0D0F_0[F,8:0]31_dct[0] Data Byte Fence2 ThresholdBIOS: [2.9.7.4.3](#). DBYTE.

Table 151: Index addresses for D18F2x9C_x0D0F_0[F,8:0]31_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0831h	0731h	0631h	0531h	0431h	0331h	0231h	0131h	0031h
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 152: Broadcast write index address for D18F2x9C_x0D0F_0[F,8:0]31_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]
	0F31h
0D0Fh	D18F2x9C_x0D0F_0[8:0]31

Bits	Description										
31:10	Reserved.										
9	Fence2EnableTxDll: phy fence2 enable transmit DLL. Read-write. Cold reset: 0. 1=Enable the use of Fence2ThresholdTxDll for transmit DLL fence threshold. 0=Use D18F2x9C_x0000_000C_dct[0][FenceThresholdTxDll].										
8:5	Fence2ThresholdTxDll: phy fence2 threshold transmit DLL. Read-write. Cold reset: 0. If Fence2EnableTxDll=1, this field specifies the fence delay threshold value used to create the fence bit in the DLL delay registers for DQS receiver valid. This field is only used during DQS receiver enable training to time the internal phy signal RxValid. See Fence2ThresholdTxPad.										
4	Fence2EnableTxPad: fence2 enable transmit pad. Read-write; S3-check-exclude. Cold reset: 0. 1=Enable the use of Fence2ThresholdTxPad for transmit pad fence threshold. 0=Use D18F2x9C_x0000_000C_dct[0][FenceThresholdTxPad].										
3:0	Fence2ThresholdTxPad: phy fence2 threshold transmit pad. Read-write; S3-check-exclude. Cold reset: 0. If Fence2EnableTxPad=1, this field specifies the fence delay threshold value used to create the fence bit in the DLL delay registers for write data and write DQS. This field is only used during write leveling training. The corresponding fence bit is set by hardware when the DLL delay register is written if DLL delay >= FenceThresholdTxPad. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No delay</td> </tr> <tr> <td>1h</td> <td>1/64 MEMCLK delay</td> </tr> <tr> <td>Eh-2h</td> <td><Fence2ThresholdTxPad> MEMCLK delay</td> </tr> <tr> <td>Fh</td> <td>15/64 MEMCLK delay</td> </tr> </tbody> </table>	Bits	Definition	0h	No delay	1h	1/64 MEMCLK delay	Eh-2h	<Fence2ThresholdTxPad> MEMCLK delay	Fh	15/64 MEMCLK delay
Bits	Definition										
0h	No delay										
1h	1/64 MEMCLK delay										
Eh-2h	<Fence2ThresholdTxPad> MEMCLK delay										
Fh	15/64 MEMCLK delay										

D18F2x9C_x0D0F_0[F,8:0]38_dct[0] Data Byte DLL Control Register

DBYTE.

Table 153: Index addresses for D18F2x9C_x0D0F_0[F,8:0]38_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]								
	0838h	0738h	0638h	0538h	0438h	0338h	0238h	0138h	0038h
0D0Fh	ECC	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0

Table 154: Broadcast write index address for D18F2x9C_x0D0F_0[F,8:0]38_dct[0]

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]
	0F38h
0D0Fh	D18F2x9C_x0D0F_0[8:0]38

Bits	Description										
31:16	Reserved.										
15	Reserved. Read-write.										
14:13	ReducedLoop: reduced loop. Read-write. Cold reset: 0. Specifies additional delay imposed before the phase comparator, which has the effect of locking the DLL to a shorter period. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No delay.</td> </tr> <tr> <td>01b</td> <td>1/3 maximum additional delay</td> </tr> <tr> <td>10b</td> <td>2/3 maximum additional delay</td> </tr> <tr> <td>11b</td> <td>Maximum additional delay</td> </tr> </tbody> </table>	Bits	Description	00b	No delay.	01b	1/3 maximum additional delay	10b	2/3 maximum additional delay	11b	Maximum additional delay
Bits	Description										
00b	No delay.										
01b	1/3 maximum additional delay										
10b	2/3 maximum additional delay										
11b	Maximum additional delay										
12:0	Reserved. Read-write.										

D18F2x9C_x0D0F_1C00_dct[0] Clock Transmit PreDriver Calibration

Cold reset: xxxx_xxxxh. D3DBYTE.

Table 155: Broadcast write index address for [D18F2x9C_x0D0F_1C00_dct\[0\]](#)

D18F2x98_dct[0][31:16]	D18F2x98_dct[0][15:0]
	1C00h
0D0Fh	D18F2x9C_x0D0F_0[F,8:0]0[B,7,3]_dct[0]

Bits	Description
13:8	POdtD: pmos ODT calibration data. Write-only.
7:6	Reserved.
5:0	NOdtD: nmos ODT calibration data. Write-only.

D18F2x9C_x0D0F_2[2:0]02_dct[0] Clock Transmit PreDriver CalibrationCold reset: xxxx_xxxxh. BIOS: See [2.9.7.4.4. D3CLK](#).Table 156: [Index Mapping for D18F2x9C_x0D0F_2\[2:0\]02_dct\[0\]](#)

D18F2x98_dct[0][31:0]	Function
0D0F_2002h	Clock 0 Pad Group 0
0D0F_2102h	Clock 1 Pad Group 0
0D0F_2202h	Reserved

Bits	Description
31:16	Reserved.
15	ValidTxAndPre: predriver calibration code valid. Read-write; cleared-by-hardware. 1=Predriver calibration codes are copied from this register into the associated transmit pad. Hardware clears this field after the copy is complete.
14:12	Reserved. Read-write.

11:6	TxPreP: PMOS predriver calibration code. Read-write. This field specifies the rising edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreP]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.
5:0	TxPreN: NMOS predriver calibration code. Read-write. This field specifies the falling edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreN]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.

D18F2x9C_x0D0F_[C,8,2][2:0]1E_dct[0]_mp[1:0] Phy Control

Cold reset: 0000_5020h. ABYTE2, D3CSODT, D3CLK.

Table 157: Index address mapping for [D18F2x9C_x0D0F_\[C,8,2\]\[2:0\]1E_dct\[0\]_mp\[1:0\]](#)

D18F2x98_dct[0][31:0]	Function
0D0F_201Eh	Clock 0
0D0F_211Eh	Clock 1
0D0F_221Eh	Reserved
0D0F_801Eh	Cmd/Addr 0
0D0F_811Eh	Cmd/Addr 1
0D0F_821Eh	Reserved
0D0F_C01Eh	Address
0D0F_C11Eh	Reserved
0D0F_C21Eh	Reserved

Bits	Description
7	Reserved.
6:0	Reserved. Read-write.

D18F2x9C_x0D0F_[C,8,2][2:0]1F_dct[0] Receiver Configuration

Cold reset: 0000_2000h. ABYTE2, D3CSODT, D3CLK.

Table 158: Index address mapping for [D18F2x9C_x0D0F_\[C,8,2\]\[2:0\]1F_dct\[0\]](#)

D18F2x98_dct[0][31:0]	Function
0D0F_201Fh	Clock 0
0D0F_211Fh	Clock 1
0D0F_221Fh	Reserved
0D0F_801Fh	Cmd/Addr 0
0D0F_811Fh	Cmd/Addr 1
0D0F_821Fh	Reserved
0D0F_C01Fh	Address
0D0F_C11Fh	Reserved
0D0F_C21Fh	Reserved

Bits	Description										
4:3	RxVioLvl: receiver voltage level. Read-write. BIOS: See 2.9.7.4.1 . Specifies the VDDIO voltage level. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.5 V</td> </tr> <tr> <td>01b</td> <td>1.35 V</td> </tr> <tr> <td>10b</td> <td>1.25 V (Phy spec:1.2 V)</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	1.5 V	01b	1.35 V	10b	1.25 V (Phy spec:1.2 V)	11b	Reserved
Bits	Description										
00b	1.5 V										
01b	1.35 V										
10b	1.25 V (Phy spec:1.2 V)										
11b	Reserved										
2:0	Reserved. Read-write.										

D18F2x9C_x0D0F_[C,8,2][2:0]20_dct[0]_mp[1:0] DLL Delay and Configuration

Cold reset: 0000_8000h. ABYTE2, D3CSODT, D3CLK. Updated by hardware during [2.9.7.4.3 \[Phy Fence Programming\]](#).

Table 159: Index Addresses for D18F2x9C_x0D0F_[C,8,2][2:0]20_dct[0]_mp[1:0]

D18F2x98_dct[0][31:0]	Function
0D0F_2020h	Clock 0
0D0F_2120h	Clock 1
0D0F_2220h	Reserved
0D0F_8020h	Cmd/Addr 0
0D0F_8120h	Cmd/Addr 1
0D0F_8220h	Reserved
0D0F_C020h	Address
0D0F_C120h	Reserved
0D0F_C220h	Reserved

Bits	Description
31:16	Reserved.
15	Reserved. Read-write.
13:8	Reserved. Read-write.
7	FenceBit: fence bit. Read-write.
6	Fence2Bit: fence2 bit. Read-write.
5:0	Reserved. Read-write.

D18F2x9C_x0D0F_2[F,2:0]30_dct[0] Clock DLL Configuration and Power Down

Cold reset: 0000_0001h. D3CLK.

Table 160: Index Addresses for D18F2x9C_x0D0F_2[F,2:0]30_dct[0]

D18F2x98_dct[0][31:0]	Function
0D0F_2030h	Clock 0
0D0F_2130h	Clock 1
0D0F_2230h	Reserved
0D0F_2F30h	Clock 1-0

Bits	Description
31:16	Reserved.
15:5	Reserved. Read-write.
4	PwrDn: power down. Read-write. 1=Turn off DLL circuitry (DLLs, pads, bias macros, regulator).
3:0	Reserved. Read-write.

D18F2x9C_x0D0F_4006_dct[0] DRAM Phy MemVref Observation Configuration

Cold reset: 0000_0002h. D3CMP.

Bits	Description
31:16	Reserved.
15:9	Reserved. Read-write.
2:0	VrefSel: vref selection. Read-write. <u>Bits</u> <u>Description</u> 000b Connections to the bump and internal VREF bus are driven tri-state. 001b Internal Rx. VrefDAC is sent to the DQ receivers; pad connection is tri-state. 010b External Rx. External Vref from the pad is sent to the DQ receivers. 011b Internal Tx. VrefDAC is sent out on the pad; internal connection is tri-state. 110b-100b Reserved. 111b Internal Rx & Tx. VrefDAC is sent to all the DQ receivers and pad.

D18F2x9C_x0D0F_4007_dct[0] DRAM Phy MemVref Configuration

Cold reset: 0000_0002h. D3CMP.

Bits	Description
31:16	Reserved.
15:9	Reserved. Read-write.
8:3	VrefDAC: vref DAC. Read-write. Controls the relative offset for the internal generated Vref from nominal VDDIO/2. <u>Bits</u> <u>Description</u> 1Eh-00h <VrefDAC>% 20h-1Fh Reserved 3Eh-21h 20h - <VrefDAC>% 3Fh Reserved
2:0	VrefSel: vref selection. Read-write. <u>Bits</u> <u>Description</u> 000b Reseved. 001b Internal Rx. VrefDAC is sent to the DQ receivers; pad connection is tri-state. 010b External Rx. External Vref from the pad is sent to the DQ receivers. 011b Internal Tx. VrefDAC is sent out on the pad; internal connection is tri-state. 110b-100b Reserved. 111b Internal Rx & Tx. VrefDAC is sent to all the DQ receivers and pad.

D18F2x9C_x0D0F_4009_dct[0] Phy Cmp MemReset Configuration

Cold reset: 0000_2000h. D3CMP.

Bits	Description										
31:16	Reserved.										
15:14	CmpVioLvl: cmp voltage level. Read-write. BIOS: See 2.9.7.4.1 . This field specifies the VDDIO voltage level. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.5 V</td> </tr> <tr> <td>01b</td> <td>1.35 V</td> </tr> <tr> <td>10b</td> <td>1.25 V (Phy spec:1.2 V)</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	1.5 V	01b	1.35 V	10b	1.25 V (Phy spec:1.2 V)	11b	Reserved
Bits	Description										
00b	1.5 V										
01b	1.35 V										
10b	1.25 V (Phy spec:1.2 V)										
11b	Reserved										
13:4	Reserved. Read-write.										
3:2	ComparatorAdjust: comparator adjust. Read-write. BIOS: D18F2x9C_x0D0F_0[F,8:0]1F_dct[0]_mp[1:0] [RxVioLvl]. This field specifies the adjustment signals for the comparator differential amplifier in madpcmpana.										
1:0	Reserved. Read-write.										

D18F2x9C_x0D0F_[C,8][1:0]02_dct[0] Transmit PreDriver CalibrationCold reset: xxxx_xxxxh. BIOS: See [2.9.7.4.4](#). ABYTE2, D3CSODT.

Table 161: Index Mapping for D18F2x9C_x0D0F_[C,8][1:0]02_dct[0]

D18F2x98_dct[0][31:0]	Function
0D0F_8002h	Cmd/Addr 0 Pad Group 0
0D0F_8102h	Cmd/Addr 1 Pad Group 0
0D0F_C002h	Address Pad Group 0

Bits	Description
31:16	Reserved.
15	ValidTxAndPre: predriver calibration code valid. Read-write; cleared-by-hardware. 1=Predriver calibration codes are copied from this register and D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0] into the associated transmit pad. Hardware clears this field after the copy is complete.
14:12	Reserved. Read-write.
11:6	TxPreP: PMOS predriver calibration code. Read-write. This field specifies the rising edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreP]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.
5:0	TxPreN: NMOS predriver calibration code. Read-write. This field specifies the falling edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreN]. After updating this value, BIOS must program ValidTxAndPre=1 for the change to take effect.

D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0] Transmit PreDriver Calibration 2Cold reset: xxxx_xxxxh. BIOS: See [2.9.7.4.4](#). ABYTE2, D3CSODT.

Table 162: Index Mapping for D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0]

D18F2x98_dct[0][31:0]	Function
0D0F_8006h	Cmd/Addr 0 Pad Group 1
0D0F_800Ah	Cmd/Addr 0 Pad Group 2
0D0F_8106h	Cmd/Addr 1 Pad Group 1
0D0F_810Ah	Cmd/Addr 1 Pad Group 2
0D0F_C006h	Address Pad Group 1
0D0F_C00Ah	Address Pad Group 2
0D0F_C00Eh	Address Pad Group 3
0D0F_C012h	Address Pad Group 4

Bits	Description
11:6	TxPreP: PMOS predriver calibration code. Read-write. This field specifies the rising edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreP]. After updating this value, BIOS must program D18F2x9C_x0D0F_[C,8][1:0]02_dct[0] [ValidTxAndPre]=1 for the change to take effect.
5:0	TxPreN: NMOS predriver calibration code. Read-write. This field specifies the falling edge slew rate of the transmit pad. See: D18F2x9C_x0D0F_0[F,8:0]02_dct[0] [TxPreN]. After updating this value, BIOS must program D18F2x9C_x0D0F_[C,8][1:0]02_dct[0] [ValidTxAndPre]=1 for the change to take effect.

D18F2x9C_x0D0F_812F_dct[0] Tristate Configuration

Reset: 0000_00A0h. BIOS: See [2.9.7.10. D3CSODT](#).

Bits	Description
7	Add16Tri: MEMADD[16] tri-state. Read-write. Specifies tri-state control for the memory address[16] signal. 1=Signal is tri-stated. 0=Signal is not tri-stated.
6	Reserved. Read-write.
5	Add17Tri: MEMADD[17] tri-state. Read-write. Specifies tri-state control for the memory address[17] signal. 1=Signal is tri-stated. 0=Signal is not tri-stated.
4:1	Reserved. Read-write.
0	PARTri: MEMPAR tri-state. Read-write. Specifies tri-state control for the memory parity signal. 1=Signal is tri-stated. 0=Signal is not tri-stated.

D18F2x9C_x0D0F_[C,8][F:0]30_dct[0] Cmd/Addr DLL Configuration and Power Down

Cold reset: 0000_0001h. BIOS: See [2.9.7.4. ABYTE2, D3CSODT](#).

Table 163: Index Mapping for D18F2x9C_x0D0F_[C,8][F:0]30_dct[0]

D18F2x98_dct[0][31:0]	Function
0D0F_8030h	Cmd/Addr 0
0D0F_8130h	Cmd/Addr 1
0D0F_8F30h	Cmd/Addr 0 and Cmd/Addr 1
0D0F_C030h	Address 2

Bits	Description
31:16	Reserved.
15:5	Reserved. Read-write.
4	PwrDn: power down. Read-write. 1=Turn off DLL circuitry (DLLs, pads, bias macros, regulator).
3:0	Reserved. Read-write.

D18F2x9C_x0D0F_C021_dct[0]_mp[1:0] DLL Delay and ConfigurationCold reset: 0000_0000h. ABYTE2. Updated by hardware during [2.9.7.4.3 \[Phy Fence Programming\]](#).

Bits	Description
31:16	Reserved.
15:8	Reserved. Read-write.
7	FenceBit: fence bit. Read-write.
6	Fence2Bit: fence2 bit. Read-write.
5:0	Reserved. Read-write.

D18F2x9C_x0D0F_E000_dct[0]_mp[1:0] Phy Master Configuration

Cold reset: 0000_0002h. MASTER.

Bits	Description
31:16	Reserved.
15:14	Rate[4:3]. See: Rate[2:0].
13:4	Reserved. Read-write.
3	FreqValid: Frequency valid. Read-write. 1=The memory frequency specified with the Rate field is valid. software must set this bit when programming Rate for the setting to take effect. Regardless of this bit, a new rate does not take effect unless the target register context is of the current memory P-state, or until the memory P-state is changed to the target Rate context.
2:0	Rate[2:0]. Read-write. Rate[4:0] = {Rate[4:3], Rate[2:0]}. Rate[4:0] is the 5-bit DDR data rate that the phy uses to configure the PLL. See Table 124 [Valid Values for Memory Clock Frequency Value Definition] . Software must set FreqValid=1 when programming this field. If memory P-states are enabled then software must program the M1 context. It is not necessary for software to program the M0 context when using D18F2x94_dct[0][MemClkFreqVal] .

D18F2x9C_x0D0F_E006_dct[0] Phy PLL Lock Time

Cold reset: 0000_0190h. MASTER.

Bits	Description
31:16	Reserved.
15:0	PllLockTime: pll lock time. Read-write. Specifies the number of 5ns periods the phy waits for PLLs to lock during a frequency change. See 2.9.7.4.2 [DRAM Channel Frequency Change] .

D18F2x9C_x0D00_E008_dct[0] Phy Master Configuration

Cold reset: 0000_0013h. MASTER.

Bits	Description
31:13	Reserved.
12	PhyPS: Phy memory P-state. Read-only; updated-by-hardware. Indicates the current memory P-state for the phy (not the DCT/NB). 0=M0. 1=M1. Writes to this nibble cause a PhyPS change.
11:5	Reserved.
4:0	FenceValue: fence value. Read-only; updated-by-hardware. Indicates the fence value used to create the fence bit in the DLL delay registers. See 2.9.7.4.3 [Phy Fence Programming] .

D18F2x9C_x0D04_E008_dct[0] Phy Master Configuration

Cold reset: 0000_0013h. MASTER.

Bits	Description
31:9	Reserved.
8	PStateToAccess: P-state to access. Read-write. Specifies the memory P-state context for context sensitive DDR phy CSR accesses using D18F2x98_dct[0] when DctOffset[29:20]!=0D0h. 0=M0, 1=M1. The processor updates this field during a memory P-state change with the target state. See D18F2x94_dct[0][DphyMemPsSelEn] .
7:0	Reserved. Read-write; S3-check-exclude.

D18F2x9C_x0D0F_E00A_dct[0] Phy Dynamic Power Mode

Cold reset: 0000_0000h. MASTER.

Bits	Description
4	Reserved. Read-write.
3:0	Reserved. Read-write.

D18F2x9C_x0D0F_E013_dct[0] Phy PLL Regulator Wait Time

Cold reset: 0000_0118h. MASTER.

Bits	Description
31:16	Reserved.
15:0	PllRegWaitTime: PLL regulator wait time. Read-write. BIOS: 2.9.7.4 . 1=Specifies the number of 5 ns periods the phy waits for the PLL to become stable when coming out of PLL regulator off power down mode.

D18F2x9C_x0D0F_E019_dct[0] Fence2

Cold reset: 0000_0000h. BIOS: [2.9.7.4.3](#). MASTER.

Bits	Description										
31:15	Reserved.										
14	Fence2EnableRxDll: phy fence2 enable receive DLL. Read-write. 1=Enable the use of Fence2ThresholdRxDll for DQS receiver enable second fence threshold. 0=Disable second fence. See D18F2x9C_x0000_000C_dct[0] [FenceThresholdRxDll] for first fence.										
13:10	Fence2ThresholdRxDll: phy fence2 threshold DQS receiver enable. Read-write. If Fence2EnableRxDll=1, this field specifies the fence delay threshold value used to create the second fence bit in the DLL delay registers for DQS receiver enable. See Fence2ThresholdTxPad.										
9:5	Reserved.										
4	Fence2EnableTxPad: fence2 enable transmit pad. Read-write. 1=Enable the use of Fence2ThresholdTxPad for transmit pad second fence threshold. 0=Disable second fence. See D18F2x9C_x0000_000C_dct[0] [FenceThresholdTxPad] for first fence.										
3:0	Fence2ThresholdTxPad: phy fence2 threshold transmit pad. Read-write. If Fence2EnableTxPad=1, this field specifies the second fence delay threshold value used to create the second fence bit (fence2) in the DLL delay registers for CLK, command, address, write data and write DQS. The corresponding fence2 bit is set by hardware when the DLL delay register is written if DLL delay >={1'b1, Fence2ThresholdTxPad}.										
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>16/64 MEMCLK delay</td> </tr> <tr> <td>1h</td> <td>17/64 MEMCLK delay</td> </tr> <tr> <td>Eh-2h</td> <td>{1,<Fence2ThresholdTxPad>}/64 MEMCLK delay</td> </tr> <tr> <td>Fh</td> <td>31/64 MEMCLK delay</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0h	16/64 MEMCLK delay	1h	17/64 MEMCLK delay	Eh-2h	{1,<Fence2ThresholdTxPad>}/64 MEMCLK delay	Fh	31/64 MEMCLK delay
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1h	17/64 MEMCLK delay										
Eh-2h	{1,<Fence2ThresholdTxPad>}/64 MEMCLK delay										
Fh	31/64 MEMCLK delay										

[D18F2x9C_x0D0F_E01A_dct\[0\]](#) M1 Fence Value

Cold reset: 0000_0000h. BIOS: [2.9.7.4.3](#). MASTER. This register is used by BIOS to temporarily store the trained fence values for the M1 memory P-state, and has no effect on the operation of the hardware. See [2.9.7.4.3](#). Note: fence2 value is recomputed by BIOS based on the fence value saved here.

Bits	Description
31:16	Reserved.
15	Reserved. Read-write.
14:10	TxDll: Transmit dll fence value. Read-write; S3-check-exclude. BIOS saves the trained TxDll to this field until such time as it is able to write the value to NVRAM.
9:5	RxDll: Receiver dll fence value. Read-write; S3-check-exclude. BIOS saves the trained RxDll to this field until such time as it is able to write the value to NVRAM.
4:0	TxPad: Transmit pad fence value. Read-write; S3-check-exclude. BIOS saves the trained TxPad to this field until such time as it is able to write the value to NVRAM.

D18F2xA4 DRAM Controller Temperature Throttle

See [2.9.3 \[DCT Configuration Registers\]](#). Writes to any DCT will be broadcast to all DCTs since this logic is per DCT instance. Reads will return DCT0 result.

See [2.9.12 \[DRAM On DIMM Thermal Management and Power Capping\]](#). Independent channel throttling may still be observed by having separate EVENT_L values.

Bits	Description																																		
31:24	Reserved.																																		
23:20	<p>BwCapCmdThrottleMode: bandwidth capping command throttle mode. Read-write. Reset: 0. Specifies the command throttle mode when BwCapEn=1. The DCT throttles commands over a rolling window of 100 clock cycles, maintaining the average throttling as specified by this field.</p> <p>MSRC001_0079[BwCapCmdThrottleMode] is an alias of D18F2xA4[BwCapCmdThrottleMode].</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Command throttling is disabled</td> </tr> <tr> <td>0001b</td> <td>Throttle commands by 30%</td> </tr> <tr> <td>0010b</td> <td>Throttle commands by 40%</td> </tr> <tr> <td>0011b</td> <td>Throttle commands by 50%</td> </tr> <tr> <td>0100b</td> <td>Throttle commands by 55%</td> </tr> <tr> <td>0101b</td> <td>Throttle commands by 60%</td> </tr> <tr> <td>0110b</td> <td>Throttle commands by 65%</td> </tr> <tr> <td>0111b</td> <td>Throttle commands by 70%</td> </tr> <tr> <td>1000b</td> <td>Throttle commands by 75%</td> </tr> <tr> <td>1001b</td> <td>Throttle commands by 80%</td> </tr> <tr> <td>1010b</td> <td>Throttle commands by 85%</td> </tr> <tr> <td>1011b</td> <td>Throttle commands by 90%</td> </tr> <tr> <td>1100b</td> <td>Throttle commands by 95%</td> </tr> <tr> <td>1101b</td> <td>Reserved</td> </tr> <tr> <td>1110b</td> <td>Throttle commands as specified by CmdThrottleMode</td> </tr> <tr> <td>1111b</td> <td>Reserved</td> </tr> </tbody> </table> <p>Throttling should not be enabled until after DRAM initialization (D18F2x110[DramEnable]=1) and training (see 2.9.7.9 [DRAM Training]) are complete. See MSRC001_0079.</p>	Bits	Description	0000b	Command throttling is disabled	0001b	Throttle commands by 30%	0010b	Throttle commands by 40%	0011b	Throttle commands by 50%	0100b	Throttle commands by 55%	0101b	Throttle commands by 60%	0110b	Throttle commands by 65%	0111b	Throttle commands by 70%	1000b	Throttle commands by 75%	1001b	Throttle commands by 80%	1010b	Throttle commands by 85%	1011b	Throttle commands by 90%	1100b	Throttle commands by 95%	1101b	Reserved	1110b	Throttle commands as specified by CmdThrottleMode	1111b	Reserved
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19:15	Reserved.																																		

14:12	<p>CmdThrottleMode: command throttle mode. Read-write. Reset: 0. BIOS: See 2.9.7.7 [DCT Training Specific Configuration]. Specifies the command throttle mode when ODTSEN=1 and the EVENT_L pin is asserted. The DCT throttles commands over a rolling window of 100 clock cycles, maintaining the average throttling as specified by this field.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Command throttling is disabled.</td></tr> <tr> <td>001b</td><td>Throttle commands by 30%.</td></tr> <tr> <td>010b</td><td>Throttle commands by 50%.</td></tr> <tr> <td>011b</td><td>Throttle commands by 60%.</td></tr> <tr> <td>100b</td><td>Throttle commands by 70%.</td></tr> <tr> <td>101b</td><td>Throttle commands by 80%.</td></tr> <tr> <td>110b</td><td>Throttle commands by 90%.</td></tr> <tr> <td>111b</td><td>Place the DRAM devices in powerdown mode (see D18F2x94_dct[0][Power-DownMode]) when EVENT_L is asserted. This mode is not valid if D18F2x94_dct[0][PowerDownEn]=0. Throttling should not be enabled until after DRAM initialization (D18F2x110[DramEnable]=1) and training (See 2.9.7.9 [DRAM Training]) are complete. See also BwCapEn.</td></tr> </tbody> </table>	Bits	Description	000b	Command throttling is disabled.	001b	Throttle commands by 30%.	010b	Throttle commands by 50%.	011b	Throttle commands by 60%.	100b	Throttle commands by 70%.	101b	Throttle commands by 80%.	110b	Throttle commands by 90%.	111b	Place the DRAM devices in powerdown mode (see D18F2x94_dct[0][Power-DownMode]) when EVENT_L is asserted. This mode is not valid if D18F2x94_dct[0][PowerDownEn] =0. Throttling should not be enabled until after DRAM initialization (D18F2x110[DramEnable] =1) and training (See 2.9.7.9 [DRAM Training]) are complete. See also BwCapEn.
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11	<p>BwCapEn: bandwidth capping enable. Read-write. Reset: 0. 1=The memory command throttle mode specified by BwCapCmdThrottleMode is applied. This bit is used by software to enable command throttling independent of the state of the EVENT_L pin. If this bit is set, ODTSEN=1, and the EVENT_L pin is asserted, the larger of the two throttle percentages specified by CmdThrottleMode and BwCapCmdThrottleMode is used. See MSRC001_0079.</p>																		
10:9	Reserved.																		
8	<p>ODTSEN: on DIMM temperature sensor enable. Read-write. Reset: 0. BIOS: See 2.9.7.7 [DCT Training Specific Configuration]. Enables the monitoring of the EVENT_L pin and indicates whether the on DIMM temperature sensors of the DIMMs on a channel are enabled. 0=Disabled. 1=Enabled. While the EVENT_L pin is asserted, the controller (a) doubles the refresh rate (if Tref=7.8 us), and (b) throttles the address bus utilization as specified by CmdThrottleMode[2:0].</p>																		
7:0	Reserved.																		

D18F2xA8_dct[0] DRAM Controller Miscellaneous 2

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31	PerRankTimingEn: per rank timing enable. Read-write. Reset: 0. BIOS: 1. Specifies the mapping between chip selects and a set of programmable timing delays. 1=Each chip select is controlled by a set of timing delays. A maximum of 4 chip selects are supported per channel. 0=Each chip select pair is controlled by a set timing delays.
30	Reserved. Read-write. Defined as ExtAddrEn.
29	Reserved. Read-write. Defined as RefChCmdMgmtDis.

28	FastSelfRefEntryDis: fast self refresh entry disable. Read-write; Same-for-all. Reset: 1. BIOS: ~D18F2x1B4[FlushWrOnS3StpGnt]. 1=DCT pushes outstanding transactions to memory prior to entering self refresh. 0=DCT enters self refresh immediately unless instructed to push outstanding transactions to memory by D18F2x11C[FlushWrOnStpGnt] or D18F2x1B4[FlushWrOnS3StpGnt].										
27:26	Reserved. Read-write.										
25:24	Reserved.										
22	PrtlChPDEnhEn: partial channel power down enh enable. Read-write. Reset: 0. BIOS: 0. Selects the channel idle hysteresis for fast exit/slow exit mode changes when (D18F2x94_dct[0][Power-DownMode] & D18F2x84_dct[0][PchgPDMModeSel]). 1=Hysteresis specified by D18F2x244_dct[0][PrtlChPDDynDly]. 0=256 clock hysteresis.										
21	AggrPDEn: aggressive power down enable. Read-write. Reset: 0. BIOS: 1. 1=The DCT places the DRAM devices in precharge power down mode when pages are closed as specified by D18F2x248_dct[0]_mp[1:0][AggrPDDelay]. 0=The DCT places the DRAM devices in precharge power down mode when pages are closed as specified by D18F2x90_dct[0][DynPageCloseEn].										
20	BankSwap: swap bank address. Read-write. Reset: 0. BIOS: See 2.9.7.7. 1=Swap the DRAM bank address bits. The normalized address bits used for bank address are swapped with lower order address bits. If D18F2x114[DctSelBankSwap]==1 then normalized address bits 10:8 are swapped else normalized address bits 11:9 are swapped. See D18F2x80_dct[0]. This swap happens before D18F2x94_dct[0][BankSwizzleMode] is applied.										
17:16	MemPhyPllPdMode: memory phy PLL powerdown mode. Read-write; Same-for-all. Reset: 00b. BIOS: 10b. These bits control how the memory PLL powers down during self-refresh. If self-refresh is requested for an NB p-state change, then the memory PLL is not powered down. These bits are sent to phy 0x0B[25:24] by SR SM. Memory phy PLL powerdown can only be enabled if NB PLL power down is enabled. See D18F5x128[NbPllPwrDwnRegEn]. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>PLL powerdown is disabled</td> </tr> <tr> <td>01b</td> <td>PLL VCO powerdown during SR</td> </tr> <tr> <td>10b</td> <td>PLL regulator powerdown during SR</td> </tr> <tr> <td>11b</td> <td>PLL VCO and regulator powerdown during SR</td> </tr> </tbody> </table>	Bits	Description	00b	PLL powerdown is disabled	01b	PLL VCO powerdown during SR	10b	PLL regulator powerdown during SR	11b	PLL VCO and regulator powerdown during SR
Bits	Description										
00b	PLL powerdown is disabled										
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10b	PLL regulator powerdown during SR										
11b	PLL VCO and regulator powerdown during SR										
15:8	Reserved. Read-write.										
7:6	Reserved. Read-write.										
5	Reserved. Read-write.										
4	Reserved. Read-write..										
3:2	Reserved. Read-write.										
1:0	Reserved.										

D18F2xAC DRAM Controller Temperature Status

Cold reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:4	Reserved.
3:2	Reserved.

1	Reserved. Read-write. Deprecated MemTrip0.
0	MemTempHot0: Memory temperature hot, DCT0. Read; Write-1-to-clear. 1=The EVENT_L pin was asserted indicating the memory temperature exceeded the normal operating limit; the DCT may be throttling the interface to aid in cooling. See D18F2xA4 .

D18F2xF8 P-state Power Information 1

Read-only.

Bits	Description										
31:24	PwrValue3: P3 power value. See PwrValue0. Value: Fuse[PwrValue[3][7:0]].										
23:16	PwrValue2: P2 power value. See PwrValue0. Value: Fuse[PwrValue[2][7:0]].										
15:8	PwrValue1: P1 power value. See PwrValue0. Value: Fuse[PwrValue[1][7:0]].										
7:0	PwrValue0: P0 power value. PwrValue and PwrDiv together specify the expected power draw of a single core in P0 and 1/NumCores of the Northbridge in the NB P-state as specified by MSRC001_00[6B:64][NbPstate] . NumCores is defined to be the number of cores per node at cold reset. Value: Fuse[PwrValue[0][7:0]]. <table> <thead> <tr> <th><u>PwrDiv</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>PwrValue / 1 W, Range: 0 to 255 W</td> </tr> <tr> <td>01b</td> <td>PwrValue / 10 W, Range: 0 to 25.5 W</td> </tr> <tr> <td>10b</td> <td>PwrValue / 100 W, Range: 0 to 2.55 W</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>PwrDiv</u>	<u>Description</u>	00b	PwrValue / 1 W, Range: 0 to 255 W	01b	PwrValue / 10 W, Range: 0 to 25.5 W	10b	PwrValue / 100 W, Range: 0 to 2.55 W	11b	Reserved
<u>PwrDiv</u>	<u>Description</u>										
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01b	PwrValue / 10 W, Range: 0 to 25.5 W										
10b	PwrValue / 100 W, Range: 0 to 2.55 W										
11b	Reserved										

D18F2xFC P-state Power Information 2

Read-only.

Bits	Description
31:24	Reserved.
23:22	PwrDiv7: P7 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[7][1:0]].
21:20	PwrDiv6: P6 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[6][1:0]].
19:18	PwrDiv5: P5 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[5][1:0]].
17:16	PwrDiv4: P4 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[4][1:0]].
15:14	PwrDiv3: P3 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[3][1:0]].
13:12	PwrDiv2: P2 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[2][1:0]].
11:10	PwrDiv1: P1 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[1][1:0]].
9:8	PwrDiv0: P0 power divisor. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrDiv[0][1:0]].
7:0	PwrValue4: P4 power value. See D18F2xF8 [PwrValue0]. Value: Fuse[PwrValue[4][7:0]].

D18F2x104 P-state Power Information 3

Read-only.

Bits	Description
31:24	Reserved.

23:16	PwrValue7: P7 power value. See D18F2xF8[PwrValue0] . Value: Fuse[PwrValue[7][7:0]].
15:8	PwrValue6: P6 power value. See D18F2xF8[PwrValue0] . Value: Fuse[PwrValue[6][7:0]].
7:0	PwrValue5: P5 power value. See D18F2xF8[PwrValue0] . Value: Fuse[PwrValue[5][7:0]].

D18F2x110 DRAM Controller Select LowIF ([BootFromDRAM](#)) THEN Cold reset: 0000_0004h. ELSE Reset: 0000_0000h. ENDIF.

Bits	Description
31:11	Reserved.
10	MemCleared: memory cleared. Read-only; updated-by-hardware. 1=Memory has been cleared since the last warm reset. This bit is set by MemClrInit. See MemClrInit.
9	MemClrBusy: memory clear busy. Read-only; updated-by-hardware. 1=The memory clear operation in either of the DCTs is in progress. Reads or writes to DRAM while the memory clear operation is in progress result in undefined behavior.
8	DramEnable: DRAM enabled. Read-only. 1>All of the used DCTs are initialized (see 2.9.7.8 [DRAM Device and Controller Initialization]) or have exited from self refresh (D18F2x90_dct[0][ExitSelfRef] transitions from 1 to 0). A DCT is considered to be used if D18F2x94_dct[0][DisDramInterface]=0 and the corresponding bit in D18F5x84[DctEn] =1.
7:6	Reserved. Read-write. DctSelIntLvAddr[1:0]. This field must be remain zero or the address bit selection in D18F2xA8[BankSwap] does not function correctly.
5	DctDatIntLv: DRAM controller data interleave enable. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. BIOS: D18F3x44[DramEccEn] . 1=DRAM data bits from every two consecutive 64-bit DRAM lines are interleaved in the ECC calculation such that a dead bit of a DRAM device is correctable.
4	Reserved.
3	MemClrInit: memory clear initialization. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. 1=The node writes 0's to all locations of system memory attached to the node and sets the MemCleared bit. The status of the memory clear operation can be determined by reading the MemClrBusy and MemCleared bits. This command is ignored if MemClrBusy=1 when the command is received. DramEnable must be set before setting MemClrInit. The memory prefetcher must be disabled by setting D18F2x11C[PrefloDis] and D18F2x11C[PrefCpuDis] before memory clear initialization and then can be re-enabled when MemCleared=1. Memory hole remapping must be disabled before setting MemClrInit. See D18F1x2[1,0][8,0][LgcyMmioHoleEn] . Software may then reenable memory hole remapping when the memory clear is complete.
2:0	Reserved.[2]: Read-write.

D18F2x114 DRAM Controller Select HighIF ([D18F2x118\[LockDramCfg\]](#) & [~D18F3x12C\[OverrideLockDramCfg\]](#)) THEN Read-only. ELSE Read-write. ENDIF. IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0200h. ELSE Reset: 0000_0000h. ENDIF.

Bits	Description
31:10	Reserved.

9	DctSelBankSwap: select DRAM bank swap address. BIOS: 1. See D18F2xA8_dct[0][BankSwap] . This bit is DctSelIntLvAddr[2] in the hardware.
8:0	Reserved.

D18F2x118 Memory Controller Configuration Low

Fields in this register (bits[17:0]) indicate priority of request types. Variable priority requests enter the memory controller as medium priority and are promoted to high priority if they have not been serviced in the time specified by MctVarPriCntLmt. This feature may be useful for isochronous IO traffic. If isochronous traffic is specified to be high priority, it may have an adverse effect on the bandwidth and performance of the devices associated with the other types of traffic. However, if isochronous traffic is specified as medium priority, the processor may not meet the isochronous bandwidth and latency requirements. The variable priority allows the memory controller to optimize DRAM transactions until isochronous traffic reaches a time threshold and must be serviced more quickly.

Bits	Description																																							
31:28	MctVarPriCntLmt: variable priority time limit. Read-write. Reset: 0000b. Temp.BIOS: 0001b.																																							
	<table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>80ns</td> <td>1000b</td> <td>720ns</td> </tr> <tr> <td>0001b</td> <td>160ns</td> <td>1001b</td> <td>800ns</td> </tr> <tr> <td>0010b</td> <td>240ns</td> <td>1010b</td> <td>880ns</td> </tr> <tr> <td>0011b</td> <td>320ns</td> <td>1011b</td> <td>960ns</td> </tr> <tr> <td>0100b</td> <td>400ns</td> <td>1100b</td> <td>1040ns</td> </tr> <tr> <td>0101b</td> <td>480ns</td> <td>1101b</td> <td>1120ns</td> </tr> <tr> <td>0110b</td> <td>560ns</td> <td>1110b</td> <td>1200ns</td> </tr> <tr> <td>0111b</td> <td>640ns</td> <td>1111b</td> <td>1280ns</td> </tr> </tbody> </table>				Bits	Description	Bits	Description	0000b	80ns	1000b	720ns	0001b	160ns	1001b	800ns	0010b	240ns	1010b	880ns	0011b	320ns	1011b	960ns	0100b	400ns	1100b	1040ns	0101b	480ns	1101b	1120ns	0110b	560ns	1110b	1200ns	0111b	640ns	1111b	1280ns
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0000b	80ns	1000b	720ns																																					
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0010b	240ns	1010b	880ns																																					
0011b	320ns	1011b	960ns																																					
0100b	400ns	1100b	1040ns																																					
0101b	480ns	1101b	1120ns																																					
0110b	560ns	1110b	1200ns																																					
0111b	640ns	1111b	1280ns																																					
27	Reserved.																																							
26:24	McqHiPriByPassMax: memory controller high priority bypass max. Read-write. Reset: 100b. Specifies the number of times a medium- or low-priority DRAM request may be bypassed by high-priority DRAM requests.																																							
23	Reserved.																																							
22:20	McqMedPriByPassMax: memory controller medium bypass low priority max. Read-write. Reset: 100b. Specifies the number of times a low-priority DRAM request may be bypassed by medium-priority DRAM requests.																																							

19	<p>LockDramCfg. Write-1-only. Reset: 0. BIOS: See 2.9.11 [DRAM CC6/PC6 Storage], 2.5.3.2.3.3 [Core C6 (CC6) State].</p> <p>The following registers are read-only if (LockDramCfg=1 & D18F3x12C[OverrideLockDram-Cfg]=0); otherwise the access type is specified by the register:</p> <ul style="list-style-type: none"> • D18F1xF0 [DRAM Hole Address] • D18F2x[5C:40]_dct[0] [DRAM CS Base Address] • D18F2x[6C:60]_dct[0] [DRAM CS Mask] • D18F2x80_dct[0] [DRAM Bank Address Mapping] • D18F2xB8 [Trace Buffer Base/Limit Address] • D18F2xBC [Trace Buffer Address Pointer] • D18F2xC0 [Trace Buffer Control] • D18F2x110 [DRAM Controller Select Low] • D18F2x114 [DRAM Controller Select High] • D18F2x120 [Trace Buffer Extended Address] • D18F2x250_dct[0] [DRAM Loopback and Training Control] • D18F4x128[CoreStateSaveDestNode] <p>The following registers are read-only if LockDramCfg=1; otherwise the access type is specified by the register:</p> <ul style="list-style-type: none"> • D18F1x[17C:140,7C:40] [DRAM Base/Limit] • D18F1x120 [DRAM Base System Address] • D18F1x124 [DRAM Limit System Address] • D18F2x118[CC6SaveEn] 										
18	<p>CC6SaveEn. IF (D18F2x118[LockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=CC6 save area is enabled; CC6 save area is initialized by microcode when the patch is loaded. See 2.5.3.2.7 [BIOS Requirements for Initialization] and 2.4.13.2.1 [Microcode Patch Procedure Overview]. BIOS: (D18F4x118[PwrGateEnCstAct0] D18F4x118[PwrGateEnCstAct1] D18F4x11C[PwrGateEnCstAct2] D18F4x118[PwrOffEnCstAct0] D18F4x118[PwrOffEnCstAct1] D18F4x11C[PwrOffEnCstAct2]).</p>										
17:16	<p>MctPriScrub: scrubber priority. Read-write. Reset: 00b.</p> <table border="1" data-bbox="262 1220 669 1396"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Medium</td></tr> <tr> <td>01b</td><td>Reserved</td></tr> <tr> <td>10b</td><td>High</td></tr> <tr> <td>11b</td><td>Variable</td></tr> </tbody> </table>	Bits	Description	00b	Medium	01b	Reserved	10b	High	11b	Variable
Bits	Description										
00b	Medium										
01b	Reserved										
10b	High										
11b	Variable										
15:14	<p>MctPriTrace: trace-mode request priority. See: MctPriCpuRd. Read-write. Reset: 10b. This must be set to high.</p>										
13:12	<p>MctPriIsoc: display refresh read priority. See: MctPriCpuRd. Read-write. Reset: 10b.</p>										
11:10	<p>MctPriWr: default write priority. See: MctPriCpuRd. Read-write. Reset: 01b.</p>										
9:8	<p>MctPriDefault: default non-write priority. See: MctPriCpuRd. Read-write. Reset: 00b.</p>										
7:6	<p>MctPriIsocWr: IO write with the isoch bit set priority. See: MctPriCpuRd. Read-write. Reset: 00b. This does not apply to isochronous traffic that is classified as display refresh.</p>										
5:4	<p>MctPriIsocRd: IO read with the isoch bit set priority. See: MctPriCpuRd. Read-write. Reset: 10b. This does not apply to isochronous traffic that is classified as display refresh.</p>										

3:2	MctPriCpuWr: CPU write priority. See: MctPriCpuRd. Read-write. Reset: 01b.										
1:0	MctPriCpuRd: CPU read priority. Read-write. Reset: 00b. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Medium</td> </tr> <tr> <td>01b</td> <td>Low</td> </tr> <tr> <td>10b</td> <td>High</td> </tr> <tr> <td>11b</td> <td>Variable</td> </tr> </tbody> </table>	Bits	Description	00b	Medium	01b	Low	10b	High	11b	Variable
Bits	Description										
00b	Medium										
01b	Low										
10b	High										
11b	Variable										

D18F2x11C Memory Controller Configuration High

The two main functions of this register are to control write bursting and memory prefetching.

Write bursting. DctWrLimit and MctWrLimit specify how writes may be burst from the MCT into the DCT to improve DRAM efficiency. When the number of writes in the MCT reaches the value specified in MctWrLimit, then they are all burst to the DCTs at once. Prior to reaching the watermark, a limited number of writes can be passed to the DCTs (specified by DctWrLimit), tagged as low priority, for the DCTs to complete when otherwise idle. Rules regarding write bursting:

- Write bursting mode only applies to low-priority writes. Medium and high priority writes are not withheld from the DCTs for write bursting.
- If write bursting is enabled, writes stay in the MCQ until the threshold specified by MctWrLimit is reached.
- Once the threshold is reached, all writes in MCQ are converted to medium priority.
- Any write in MCQ that matches the address of a subsequent access is promoted to either medium priority or the priority of the subsequent access, whichever is higher.
- DctWrLimit only applies to low-priority writes.

Memory prefetching. The MCT prefetcher detects stride patterns in the stream of requests and then, for predictable stride patterns, generates prefetch requests. A stride pattern is a pattern of requests through system memory that are the same number of cachelines apart. The prefetcher supports strides of -4 to +4 cachelines, which can include alternating patterns (e.g. +1, +2, +1, +2), and can prefetch 1, 2, 3, 4, or 5 cachelines ahead, depending on the confidence. In addition, a fixed stride mode (non-alternating) may be used for IO requests which often have fixed stride patterns. This mode bypasses the stride predictor such that CPU-access stride predictions are not adversely affected by IO streams.

The MCT tracks several stride patterns simultaneously. The prefetch table size is 32. Each of these has a confidence level associated with it that varies as follows:

- Each time a request is received that matches the stride pattern, the confidence level increases by one.
- Each time a request is received within +/- 4 cachelines of the last requested cacheline in the pattern that does not match the pattern, then the confidence level decreases by one.
- When the confidence level reaches the saturation point specified by PrefConfSat, then it no-longer increments.

Each request that is not within +/- 4 cachelines of the last requested cacheline line of all the stride patterns tracked initiates a new stride pattern by displacing one of the existing least-recently-used stride patterns.

The memory prefetcher uses an adaptive prefetch scheme to adjust the prefetch distance based upon the buffer space available for prefetch request data. The adaptive scheme counts the total number of prefetch requests and the number of prefetch requests that cannot return data because of buffer availability. After every 16 prefetch requests, the prefetcher uses the following rules to adjust the prefetch distance:

- If the ratio of prefetch requests that cannot return data to total prefetch requests is greater than or equal to D18F2x1B0[AdapPrefMissRatio] then the prefetch distance is reduced by D18F2x1B0[AdapPrefNega-

- tiveStep].
- If the ratio of prefetch requests that cannot return data to total prefetch requests is less than [D18F2x1B0\[AdapPrefMissRatio\]](#) then the prefetch distance is increased by [D18F2x1B0\[AdapPrefPositiveStep\]](#).
 - If the adjusted prefetch distance is greater than the prefetch distance defined for the current confidence level, the prefetch distance for the current confidence level is used.

The adaptive prefetch scheme supports fractional prefetch distances by alternating between two whole number prefetch distances. For example a prefetch distance of 1.25 causes a prefetch distance sequence of: 1, 1, 1, 2, 1, 1, 2.

Bits	Description										
31	MctScrubEn: MCT scrub enable. Read-write. Reset: 0. 1=Enables periodic flushing of prefetches and writes based on the DRAM scrub rate. This is used to ensure that prefetch and write data aging is not so long that soft errors accumulate and become uncorrectable. When enabled, each DRAM scrub event causes a single prefetch to be de-allocated (the oldest one) and all queued writes to be flushed to DRAM.										
30	FlushWr: flush writes command. Read; write-1-only; cleared-by-hardware. Reset: 0. Setting this bit causes write bursting to be canceled and all outstanding writes to be flushed to DRAM. This bit is cleared when all writes are flushed to DRAM.										
29	FlushWrOnStpGnt: flush writes on stop-grant. Read-write. Reset: 0. BIOS: ~ D18F2x1B4[FlushWrOnS3StpGnt] . 1=Causes write bursting to be canceled and all outstanding writes to be flushed to DRAM when in the stop-grant state.										
28	Reserved. Read-write. Defined as PrefDramTrainMode for previous projects.										
27:25	PrefThreeConf: prefetch three-ahead confidence. Read-write. Reset: 100b. Temp.BIOS: 110b. Confidence level required in order to prefetch three cachelines ahead (same encoding as PrefTwoConf below).										
24:22	PrefTwoConf: prefetch two-ahead confidence. Read-write. Reset: 011b. Temp.BIOS: 011b. Confidence level required in order to prefetch two cachelines ahead. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> </tr> <tr> <td>110b-001b</td> <td>[PrefTwoConf*2]</td> </tr> <tr> <td>111b</td> <td>14</td> </tr> </tbody> </table>	Bits	Description	000b	0	110b-001b	[PrefTwoConf*2]	111b	14		
Bits	Description										
000b	0										
110b-001b	[PrefTwoConf*2]										
111b	14										
21:20	PrefOneConf: prefetch one-ahead confidence. Read-write. Reset: 10b. Temp.BIOS: 10b. Confidence level required in order to prefetch one ahead (0 through 3).										
19:18	PrefConfSat: prefetch confidence saturation. Read-write. Reset: 00b. Temp.BIOS: 00b. Specifies the point at which prefetch confidence level saturates and stops incrementing. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>15</td> </tr> <tr> <td>01b</td> <td>7</td> </tr> <tr> <td>10b</td> <td>3</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	15	01b	7	10b	3	11b	Reserved
Bits	Description										
00b	15										
01b	7										
10b	3										
11b	Reserved										
17:16	PrefFixDist: prefetch fixed stride distance. Read-write. Reset: 00b. Specifies the distance to prefetch ahead if in fixed stride mode. 00b=1 cacheline; 01b=2 cachelines; 10b=3 cachelines; 11b=4 cachelines.										
15	PrefFixStrideEn: prefetch fixed stride enable. Read-write. Reset: 0. 1=The prefetch stride for all requests (CPU and IO) is fixed (non-alternating).										

14	PrefIoFixStrideEn: Prefetch IO fixed stride enable. Read-write. Reset: 0. 1=The prefetch stride for IO requests is fixed (non-alternating).										
13	PrefIoDis: prefetch IO-access disable. Read-write. Reset: 1. BIOS: 0. 1=Disables IO requests from triggering prefetch requests.										
12	PrefCpuDis: prefetch CPU-access disable. Read-write. Reset: 1. BIOS: 0. 1=Disables CPU requests from triggering prefetch requests.										
11:7	MctPrefReqLimit: memory controller prefetch request limit. Read-write. Reset: 1Eh. Specifies the maximum number of outstanding prefetch requests allowed. See D18F3x78 for restrictions on this field.										
6:2	MctWrLimit: memory controller write-burst limit. Read-write. Reset: 1Fh. BIOS:0Ch. Specifies the number of writes in the memory controller queue before they are burst into the DCTs. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>32</td> </tr> <tr> <td>1Dh-01h</td> <td>[32-MctWrLimit]</td> </tr> <tr> <td>1Eh</td> <td>2</td> </tr> <tr> <td>1Fh</td> <td>Write bursting disabled</td> </tr> </tbody> </table>	Bits	Description	00h	32	1Dh-01h	[32-MctWrLimit]	1Eh	2	1Fh	Write bursting disabled
Bits	Description										
00h	32										
1Dh-01h	[32-MctWrLimit]										
1Eh	2										
1Fh	Write bursting disabled										
1:0	DctWrLimit: DRAM controller write limit. Read-write. Reset: 00b. Temp.BIOS: 00b. Specifies the maximum number of writes allowed in the DCT queue when write bursting is enabled, prior to when the number of writes in MCQ exceeds the watermark specified by MctWrLimit. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>0</td> </tr> <tr> <td>01b</td> <td>2</td> </tr> <tr> <td>10b</td> <td>4</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	0	01b	2	10b	4	11b	Reserved
Bits	Description										
00b	0										
01b	2										
10b	4										
11b	Reserved										

D18F2x1B0 Extended Memory Controller Configuration Low

The main function of this register is to control the memory prefetcher. See [D18F2x11C \[Memory Controller Configuration High\]](#) about the adaptive prefetch scheme.

Table 164: BIOS Recommendations for D18F2x1B[4:0]

Condition	D18F2x1B0	D18F2x1B4	
DdrRate	DcqBwThrotWm	DcqBwThrotWm1	DcqBwThrotWm2
667	0h	3h	4h
800	0h	3h	5h
1066	0h	4h	6h
1333	0h	5h	8h
1600	0h	6h	9h
1866	0h	7h	Ah
2133	0h	8h	Ch

Bits	Description																																
31:28	<p>DcqBwThrotWm: dcq bandwidth throttle watermark. Read-write. Reset: 3h. BIOS: Table 164. Specifies the number of outstanding DRAM read requests before new DRAM prefetch requests and speculative prefetch requests are throttled. 0h=Throttling is disabled. Legal values are 0h through Ch. Programming this field to a non-zero value disables D18F2x1B4[DcqBwThrotWm1], DcqBwThrotWm2.</p> <p>Rule: D18F2x1B0[DcqBwThrotWm]<=Ch. See D18F3x18C[DcqDepthCtl].</p> <p>The percentage of DCQ occupancy affected by this field varies with memory speed as follows:</p> <table> <thead> <tr> <th>Memory Speed</th> <th>100%</th> <th>150%</th> <th>200%</th> </tr> </thead> <tbody> <tr> <td>DDR3-667</td> <td>3h</td> <td>4h</td> <td>5h</td> </tr> <tr> <td>DDR3-800</td> <td>3h</td> <td>5h</td> <td>6h</td> </tr> <tr> <td>DDR3-1066</td> <td>4h</td> <td>6h</td> <td>8h</td> </tr> <tr> <td>DDR3-1333</td> <td>5h</td> <td>8h</td> <td>Ah</td> </tr> <tr> <td>DDR3-1600</td> <td>6h</td> <td>9h</td> <td>Ch</td> </tr> <tr> <td>DDR3-1866</td> <td>7h</td> <td>Ah</td> <td>Eh</td> </tr> <tr> <td>DDR3-2133</td> <td>8h</td> <td>Ch</td> <td>10h</td> </tr> </tbody> </table> <p>The BIOS recommended values are based off the 150% column.</p>	Memory Speed	100%	150%	200%	DDR3-667	3h	4h	5h	DDR3-800	3h	5h	6h	DDR3-1066	4h	6h	8h	DDR3-1333	5h	8h	Ah	DDR3-1600	6h	9h	Ch	DDR3-1866	7h	Ah	Eh	DDR3-2133	8h	Ch	10h
Memory Speed	100%	150%	200%																														
DDR3-667	3h	4h	5h																														
DDR3-800	3h	5h	6h																														
DDR3-1066	4h	6h	8h																														
DDR3-1333	5h	8h	Ah																														
DDR3-1600	6h	9h	Ch																														
DDR3-1866	7h	Ah	Eh																														
DDR3-2133	8h	Ch	10h																														
27:25	<p>PrefFiveConf: prefetch five-ahead confidence. Read-write. Reset: 110b. BIOS: 111b. Confidence level required in order to prefetch five cachelines ahead.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> </tr> <tr> <td>110b-001b</td> <td>[PrefFiveConf*2]</td> </tr> <tr> <td>111b</td> <td>14</td> </tr> </tbody> </table>	Bits	Description	000b	0	110b-001b	[PrefFiveConf*2]	111b	14																								
Bits	Description																																
000b	0																																
110b-001b	[PrefFiveConf*2]																																
111b	14																																
24:22	<p>PrefFourConf: prefetch four-ahead confidence. Read-write. Reset: 101b. BIOS: 111b. Confidence level required in order to prefetch four cachelines ahead.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> </tr> <tr> <td>110b-001b</td> <td>[PrefFourConf*2]</td> </tr> <tr> <td>111b</td> <td>14</td> </tr> </tbody> </table>	Bits	Description	000b	0	110b-001b	[PrefFourConf*2]	111b	14																								
Bits	Description																																
000b	0																																
110b-001b	[PrefFourConf*2]																																
111b	14																																
21	Reserved.																																
20	DblPrefEn: double prefetch enable. Read-write. Reset: 0. 1=The memory prefetcher only generates prefetch requests when it is able to generate a pair of prefetch requests to consecutive cache lines.																																
19:18	Reserved.																																
17:13	Reserved. Reset: 11100b. Read-write.																																
12	EnSplitDctLimits: split DCT write limits enable. Read-write. Reset: 0. BIOS: 1. 1=The number of writes specified by D18F2x11C[DctWrLimit, MctWrLimit] is per DCT. 0=The number of writes specified by D18F2x11C[DctWrLimit, MctWrLimit] is for the even[0,2] or odd[1,3] DCT channels. 0=The number of writes specified by D18F2x11C[DctWrLimit, MctWrLimit] is total writes independent of DCT. Setting this bit also affects the encoding of D18F2x11C[DctWrLimit] .																																
11	DisIoCohPref: disable coherent prefetched for IO. IF (Fuse[DisCohIOPref]) THEN Read-only. ELSE Read-write. ENDIF. IF (Fuse[DisCohIOPref]) THEN Reset: 1 ELSE Reset: 0 ENDIF. 1=Probes are not generated for prefetches generated for reads from IO devices.																																

10:8	CohPrefPrbLmt: coherent prefetch probe limit. IF (Fuse[DisCohPref]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 000b. BIOS: 000b. Specifies the maximum number of probes that can be outstanding for memory prefetch requests.										
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Probing disabled for memory prefetch requests</td></tr> <tr> <td>111b-001b</td><td>Reserved.</td></tr> </tbody> </table>	Bits	Description	000b	Probing disabled for memory prefetch requests	111b-001b	Reserved.				
Bits	Description										
000b	Probing disabled for memory prefetch requests										
111b-001b	Reserved.										
7:6	Reserved.										
5:4	AdapPrefNegativeStep: adaptive prefetch negative step. Read-write. Reset: 00b. BIOS: 00b. Specifies the step size that the adaptive prefetch scheme uses when decreasing the prefetch distance.										
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>2/16</td></tr> <tr> <td>01b</td><td>4/16</td></tr> <tr> <td>10b</td><td>8/16</td></tr> <tr> <td>11b</td><td>16/16</td></tr> </tbody> </table>	Bits	Description	00b	2/16	01b	4/16	10b	8/16	11b	16/16
Bits	Description										
00b	2/16										
01b	4/16										
10b	8/16										
11b	16/16										
3:2	AdapPrefPositiveStep: adaptive prefetch positive step. Read-write. Reset: 00b. BIOS: 00b. Specifies the step size that the adaptive prefetch scheme uses when increasing the prefetch distance.										
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1/16</td></tr> <tr> <td>01b</td><td>2/16</td></tr> <tr> <td>10b</td><td>4/16</td></tr> <tr> <td>11b</td><td>8/16</td></tr> </tbody> </table>	Bits	Description	00b	1/16	01b	2/16	10b	4/16	11b	8/16
Bits	Description										
00b	1/16										
01b	2/16										
10b	4/16										
11b	8/16										
1:0	AdapPrefMissRatio: adaptive prefetch miss ratio. Read-write. Reset: 00b. BIOS: 01b. Specifies the ratio of prefetch requests that do not have data buffer available to the total number of prefetch requests at which the adaptive prefetch scheme begins decreasing the prefetch distance.										
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1/16</td></tr> <tr> <td>01b</td><td>2/16</td></tr> <tr> <td>10b</td><td>4/16</td></tr> <tr> <td>11b</td><td>8/16</td></tr> </tbody> </table>	Bits	Description	00b	1/16	01b	2/16	10b	4/16	11b	8/16
Bits	Description										
00b	1/16										
01b	2/16										
10b	4/16										
11b	8/16										

D18F2x1B4 Extended Memory Controller Configuration High Register

Bits	Description
31	FlushOnMmioWrEn: flush on mmio write enable. Read-write. Reset: 0. 1=Any CPU-sourced MMIO write that matches D18F1x[2CC:2A0,1CC:180,BC:80] causes the memory controller data buffers to be flushed to memory.
30:28	S3SmafId: S3 SMAF id. Read-write. Reset: 100b. SMAF encoding of D18F3x[84:80] corresponding to the ACPI S3 state when FlushWrOnS3StpGnt=1. Reserved when FlushWrOnS3StpGnt=0.
27	FlushWrOnS3StpGnt: flush write on S3 stop grant. Read-write. Reset: 0. BIOS: 1. 1=Write bursting is canceled and all outstanding writes are flushed to DRAM when in the stop-grant state and the SMAF code is equal to S3SmafId, indicating entry into the ACPI S3 state. See D18F2xA8_dct[0][FastSelfRefEntryDis], D18F2x11C[FlushWrOnStpGnt].

26	EnSplitMctDatBuffers: enable split MCT data buffers. Read-write. Reset: 0. BIOS: 1. 1=Enable resource allocation into the split buffer resources (a single DCT allocates into MCD_HI and MCD_LO). This field was intended to be set only if NCLK frequency < 2 * MEMCLK frequency for any P-state, but has no impact on operation when the ratio above is false. BIOS must program this bit before any DRAM memory accesses are issued from the processor (including CAR initialization; if accesses are carefully controlled, this may be programmed after CAR initialization but before DCT initialization).
25	SmuCfgLock: SMU configuration lock. Read-write; updated-by-hardware. (SMU). Reset: 0. This field should never be cleared by software. The following registers are read-only if (LockSmuCfg=1 && D18F3x12C[OverrideLockDramCfg]=0); otherwise the access type is specified by the register: <ul style="list-style-type: none"> • D18F4x10C [TDP Limit 2] • D18F4x15C [Core Performance Boost Control] • D18F5x12C [Clock Power/Timing Control 4] • D18F5x170 [Northbridge P-state Control] • D18F5x188 [Clock Power/Timing Control 5] SMU accesses are not locked by this field, only software accesses limited. This bit is set when BAPM or NB DPM are enabled by SMU.
22	SpecPrefDisWm1: speculative prefetch disable watermark 1. Read-write. Reset: 0. 0=Disable speculative prefetches at the DcqBwThrotWm2 limit. 1=Disable speculative prefetches at the DcqBwThrotWm1 limit. See also D18F2x1B0[SpecPrefDis].
21	RegionAlloWm2: region prefetch allocate watermark 2. Read-write. Reset: 0. See DemandAlloWm2.
20	RegionPropWm2: region prefetch propagate watermark 2. Read-write. Reset: 0. See DemandPropWm2.
19	StrideAlloWm2: stride prefetch allocate watermark 2. Read-write. Reset: 1. See DemandAlloWm2.
18	StridePropWm2: stride prefetch propagate watermark 2. Read-write. Reset: 1. See DemandPropWm2.
17	DemandAlloWm2: demand request allocate watermark 2. Read-write. Reset: 1. Specifies the behavior from the DcqBwThrotWm1 limit to the DcqBwThrotWm2 limit. 0=Requests do not allocate a new MPT entry. 1=Requests allocate a new MPT entry; defined only if (DemandAlloWm1 & DemandPropWm2).
16	DemandPropWm2: demand request propagate watermark 2. Read-write. Reset: 1. Specifies the behavior from the DcqBwThrotWm1 limit to the DcqBwThrotWm2 limit. 0=Requests do not update existing MPT entries. 1=Requests update existing MPT entries with new address and stride info; defined only if (DemandPropWm1=1).
15	RegionAlloWm1: region prefetch allocate watermark 1. Read-write. Reset: 0. See DemandAlloWm1.
14	RegionPropWm1: region prefetch propagate watermark 1. Read-write. Reset: 1. See DemandPropWm1.
13	StrideAlloWm1: stride prefetch allocate watermark 1. Read-write. Reset: 1. See DemandAlloWm1.
12	StridePropWm1: stride prefetch propagate watermark 1. Read-write. Reset: 1. See DemandPropWm1.

11	DemandAlloWm1: demand request allocate watermark 1. Read-write. Reset: 1. Specifies the behavior prior to the DcqBwThrotWm1 limit. 0=Requests do not allocate a new MPT entry. 1=Requests allocate a new MPT entry; defined only if (DemandPropWm1=1).
10	DemandPropWm1: demand request propagate watermark 1. Read-write. Reset: 1. Specifies the behavior prior to the DcqBwThrotWm1 limit. 0=Requests do not update existing MPT entries. 1=Requests update existing MPT entries with new address and stride info.
9:5	DcqBwThrotWm2: DCQ bandwidth throttle watermark 2. Read-write. Reset: 06h. BIOS: Table 164 . Specifies a prefetch throttling watermark based on the number of outstanding DRAM read requests. This field is reserved when D18F2x1B0[DcqBwThrotWm] != 0. When throttling is enabled, if the number of outstanding DRAM read requests exceeds DcqBwThrotWm2 both request allocate and propagate are blocked and new prefetches are disabled. When throttling is enabled, DcqBwThrotWm2 should be programmed to a value greater than DcqBwThrotWm1. 0h=Throttling is disabled. Legal values are 0h through 18h. Rule: D18F2x1B4[DcqBwThrotWm2] <=18h. See D18F3x18C[DcqDepthCtl] . The BIOS recommended values are based off the 150% column of D18F2x1B0[DcqBwThrotWm] .
4:0	DcqBwThrotWm1: DCQ bandwidth throttle watermark 1. Read-write. Reset: 03h. BIOS: Table 164 . Specifies a prefetch throttling watermark based on the number of outstanding DRAM read requests. This field is reserved when D18F2x1B0[DcqBwThrotWm] != 0. 0h=Throttling is disabled. Legal values are 0h through 18h. Rule: D18F2x1B4[DcqBwThrotWm1] <=18h. See D18F3x18C[DcqDepthCtl] . The BIOS recommended values are based off the 100% column of D18F2x1B0[DcqBwThrotWm] .

D18F2x1BC_dct[0] DRAM CKE to CS Map

IF ([BootFromDRAM](#)) THEN Cold reset: Reset: 0000_AA55h ELSE Reset: 0000_AA55h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Table 165: Field Mapping for [D18F2x1BC_dct\[0\]](#)

Register	Bits			
	31:24	23:16	15:8	7:0
D18F2x1BC_dct[0]	CKE3	CKE2	CKE1	CKE0

Table 166: BIOS Recommendations for [D18F2x1BC_dct\[0\]](#)

Condition:	D18F2x1BC_dct[0]	
Package	NumDimmSlots	
FT3	1, 2	08040201h

Bits	Description
31:24	CSMapCKE: CS map CKE. See: D18F2x1BC_dct[0][7:0] .
23:16	CSMapCKE: CS map CKE. See: D18F2x1BC_dct[0][7:0] .

15:8	CSMapCKE: CS map CKE. See: D18F2x1BC_dct[0][7:0] .												
7:0	<p>CSMapCKE: CS map CKE. Read-write. BIOS: See Table 166 [BIOS Recommendations for D18F2x1BC_dct[0]]. Maps the CS to CKE relationship, which varies by platform and DIMM. 1=This CKE is associated with the listed chip select. 0=This CKE is not associated with the listed chip select. See also D18F2x9C_x0000_000C_dct[0][CKETri].</p> <p>E.g. D18F2x1BC_dct[0]=0000_AA55h means that CKE0 controls all the even CSes, CKE1 controls all the odd CSes, and CKE2 & CKE3 are unused. Only 1 CKE may be assigned to a CS across D18F2x1BC_dct[0]. Only even CKEs may be assigned to even CSes. Only odd CKEs may be assigned to odd CSes.</p> <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>CS0</td> </tr> <tr> <td>[1]</td> <td>CS1</td> </tr> <tr> <td>[2]</td> <td>CS2</td> </tr> <tr> <td>[3]</td> <td>CS3</td> </tr> <tr> <td>[7:4]</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	[0]	CS0	[1]	CS1	[2]	CS2	[3]	CS3	[7:4]	Reserved
<u>Bit</u>	<u>Description</u>												
[0]	CS0												
[1]	CS1												
[2]	CS2												
[3]	CS3												
[7:4]	Reserved												

D18F2x200_dct[0]_mp[1:0] DDR3 DRAM Timing 0

IF ([BootFromDRAM](#)) THEN Cold reset: 1505_0505h. ELSE Reset: 0F05_0505h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description								
31:30	Reserved.								
29:24	<p>Tras: row active strobe. Read-write. BIOS: See 2.9.7.5 [SPD ROM-Based Configuration]. Specifies the minimum time in memory clock cycles from an activate command to a precharge command, both to the same chip select bank.</p> <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>07h-00h</td> <td>Reserved</td> </tr> <tr> <td>2Ah-08h</td> <td><Tras> clocks</td> </tr> <tr> <td>3Fh-2Bh</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	07h-00h	Reserved	2Ah-08h	<Tras> clocks	3Fh-2Bh	Reserved
<u>Bits</u>	<u>Description</u>								
07h-00h	Reserved								
2Ah-08h	<Tras> clocks								
3Fh-2Bh	Reserved								
23:21	Reserved.								
20:16	<p>Trp: row precharge time. Read-write. BIOS: See 2.9.7.5 [SPD ROM-Based Configuration]. Specifies the minimum time in memory clock cycles from a precharge command to an activate command or auto refresh command, both to the same bank.</p> <p>Rule: D18F2x200_dct[0]_mp[1:0][Trp] > D18F2x24C_dct[0][Tpd].</p> <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>04h-00h</td> <td>Reserved</td> </tr> <tr> <td>13h-05h</td> <td><Trp> clocks</td> </tr> <tr> <td>1Fh-14h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	04h-00h	Reserved	13h-05h	<Trp> clocks	1Fh-14h	Reserved
<u>Bits</u>	<u>Description</u>								
04h-00h	Reserved								
13h-05h	<Trp> clocks								
1Fh-14h	Reserved								
15:13	Reserved.								

12:8	Trcd: RAS to CAS delay. Read-write. BIOS: See 2.9.7.5 [SPD ROM-Based Configuration] . Specifies the time in memory clock cycles from an activate command to a read/write command, both to the same bank.								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>04h-00h</td><td>Reserved</td></tr> <tr> <td>13h-05h</td><td><Trcd> clocks</td></tr> <tr> <td>1Fh-14h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	04h-00h	Reserved	13h-05h	<Trcd> clocks	1Fh-14h	Reserved
<u>Bits</u>	<u>Description</u>								
04h-00h	Reserved								
13h-05h	<Trcd> clocks								
1Fh-14h	Reserved								
7:5	Reserved.								
4:0	Tcl: CAS latency. Read-write. BIOS: See 2.9.7.5 [SPD ROM-Based Configuration] . Specifies the time in memory clock cycles from the CAS assertion for a read cycle until data return (from the perspective of the DRAM devices).								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>04h-00h</td><td>Reserved</td></tr> <tr> <td>13h-05h</td><td><Tcl> clocks</td></tr> <tr> <td>1Fh-14h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	04h-00h	Reserved	13h-05h	<Tcl> clocks	1Fh-14h	Reserved
<u>Bits</u>	<u>Description</u>								
04h-00h	Reserved								
13h-05h	<Tcl> clocks								
1Fh-14h	Reserved								

D18F2x204_dct[0]_mp[1:0] DDR3 DRAM Timing 1

IF (BootFromDRAM) THEN Cold reset: 040A_040Dh. ELSE Reset: 0400_040Bh. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description										
31:28	Reserved.										
27:24	Trtp: read CAS to precharge time. Read-write. BIOS: See 2.9.7.5 . Specifies the earliest time in memory clock cycles a page can be closed after having been read. Satisfying this parameter ensures read data is not lost due to a premature precharge.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>3h-0h</td><td>Reserved</td></tr> <tr> <td>Bh-4h</td><td><Trtp> clocks</td></tr> <tr> <td>Fh-Ch</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	3h-0h	Reserved	Bh-4h	<Trtp> clocks	Fh-Ch	Reserved		
<u>Bits</u>	<u>Description</u>										
3h-0h	Reserved										
Bh-4h	<Trtp> clocks										
Fh-Ch	Reserved										
23:22	Reserved.										
21:16	FourActWindow: four bank activate window. Read-write. BIOS: See 2.9.7.5 . Specifies the rolling tFAW window in memory clock cycles during which no more than 4 banks in an 8-bank device are activated.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>00h</td><td>No tFAW window restriction</td></tr> <tr> <td>05h-01h</td><td>Reserved</td></tr> <tr> <td>2Ch-06h</td><td>[FourActWindow] clocks</td></tr> <tr> <td>3Fh-2Dh</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00h	No tFAW window restriction	05h-01h	Reserved	2Ch-06h	[FourActWindow] clocks	3Fh-2Dh	Reserved
<u>Bits</u>	<u>Description</u>										
00h	No tFAW window restriction										
05h-01h	Reserved										
2Ch-06h	[FourActWindow] clocks										
3Fh-2Dh	Reserved										
15:12	Reserved.										
11:8	Trrd: row to row delay (or RAS to RAS delay). Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time in memory clock cycles between activate commands to different chip select banks.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0h</td><td>Reserved</td></tr> <tr> <td>9h-1h</td><td><Trrd> clocks</td></tr> <tr> <td>Fh-Ah</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	Reserved	9h-1h	<Trrd> clocks	Fh-Ah	Reserved		
<u>Bits</u>	<u>Description</u>										
0h	Reserved										
9h-1h	<Trrd> clocks										
Fh-Ah	Reserved										

7:6	Reserved.								
5:0	<p>Trc: row cycle time. Read-write. BIOS: See 2.9.7.5. Specifies the minimum time in memory clock cycles from and activate command to another activate command or an auto refresh command, all to the same chip select bank.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>09h-00h</td> <td>Reserved</td> </tr> <tr> <td>3Ah-0Ah</td> <td><Trc> clocks</td> </tr> <tr> <td>3Fh-3Bh</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	09h-00h	Reserved	3Ah-0Ah	<Trc> clocks	3Fh-3Bh	Reserved
Bits	Description								
09h-00h	Reserved								
3Ah-0Ah	<Trc> clocks								
3Fh-3Bh	Reserved								

D18F2x208_dct[0] DDR3 DRAM Timing 2

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description																
31:27	Reserved.																
26:24	Trfc3: auto refresh row cycle time for CS 6 and 7. See: Trfc0.																
23:19	Reserved.																
18:16	Trfc2: auto refresh row cycle time for CS 4 and 5. See: Trfc0.																
15:11	Reserved.																
10:8	Trfc1: auto refresh row cycle time for CS 2 and 3. See: Trfc0.																
7:3	Reserved.																
2:0	<p>Trfc0: auto refresh row cycle time for CS 0 and 1. Read-write. IF (BootFromDRAM) THEN Cold reset: 100b. ELSE Reset: 100b. ENDIF. BIOS: 2.9.7.5. Specifies the minimum time from a refresh command to the next valid command, except NOP or DES. The recommended programming of this register varies based on DRAM density and speed.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Reserved</td> </tr> <tr> <td>001b</td> <td>90 ns (all speeds, 512 Mbit)</td> </tr> <tr> <td>010b</td> <td>110 ns (all speeds, 1 Gbit)</td> </tr> <tr> <td>011b</td> <td>160 ns (all speeds, 2 Gbit)</td> </tr> <tr> <td>100b</td> <td>300 ns (all speeds, 4 Gbit)</td> </tr> <tr> <td>101b</td> <td>350 ns (all speeds, 8 Gbit)</td> </tr> <tr> <td>111b-110b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	000b	Reserved	001b	90 ns (all speeds, 512 Mbit)	010b	110 ns (all speeds, 1 Gbit)	011b	160 ns (all speeds, 2 Gbit)	100b	300 ns (all speeds, 4 Gbit)	101b	350 ns (all speeds, 8 Gbit)	111b-110b	Reserved
Bits	Description																
000b	Reserved																
001b	90 ns (all speeds, 512 Mbit)																
010b	110 ns (all speeds, 1 Gbit)																
011b	160 ns (all speeds, 2 Gbit)																
100b	300 ns (all speeds, 4 Gbit)																
101b	350 ns (all speeds, 8 Gbit)																
111b-110b	Reserved																

D18F2x20C_dct[0]_mp[1:0] DDR3 DRAM Timing 3

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description										
31:18	Reserved.										
17:16	<p>WrDqDqsEarly: DQ and DQS write early. Read-Write. Reset: 0. Specifies the DQ and DQS launch timing for write commands relative to the Tcwl MEMCLK.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>0 MEMCLK early (aligned with Tcwl MEMCLK rising edge)</td> </tr> <tr> <td>01b</td> <td>0.5 MEMCLK early</td> </tr> <tr> <td>10b</td> <td>Reserved ;1.0 MEMCLK early</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	0 MEMCLK early (aligned with Tcwl MEMCLK rising edge)	01b	0.5 MEMCLK early	10b	Reserved ;1.0 MEMCLK early	11b	Reserved
Bits	Description										
00b	0 MEMCLK early (aligned with Tcwl MEMCLK rising edge)										
01b	0.5 MEMCLK early										
10b	Reserved ;1.0 MEMCLK early										
11b	Reserved										

15:12	Reserved. [15:12] are reserved for Twtr.								
11:8	Twtr: internal DRAM write to read command delay. Read-write. IF (BootFromDRAM) THEN Cold reset: 7h. ELSE Reset: 4h. ENDIF. BIOS: See 2.9.7.5. Specifies the minimum number of memory clock cycles from a write operation to a read operation, both to the same chip select. This is measured from the rising clock edge following last non-masked data strobe of the write to the rising clock edge of the next read command. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3h-0h</td> <td>Reserved</td> </tr> <tr> <td>Bh-4h</td> <td><Twtr> clocks</td> </tr> <tr> <td>Fh-Ch</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	3h-0h	Reserved	Bh-4h	<Twtr> clocks	Fh-Ch	Reserved
Bits	Description								
3h-0h	Reserved								
Bh-4h	<Twtr> clocks								
Fh-Ch	Reserved								
7:5	Reserved.								
4:0	Tcwl: CAS write latency. Read-write. IF (BootFromDRAM) THEN Cold reset: 5h. ELSE Reset: 5h. ENDIF. BIOS: See 2.9.7.5. Specifies the number of memory clock cycles from internal write command to first write data in at the DRAM. This register is applied to the MRS during HW DRAM initialization. See 2.9.7.8 [DRAM Device and Controller Initialization]. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>04h-00h</td> <td>Reserved</td> </tr> <tr> <td>0Ah-05h</td> <td><Tcwl> clocks</td> </tr> <tr> <td>1Fh-0Bh</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	04h-00h	Reserved	0Ah-05h	<Tcwl> clocks	1Fh-0Bh	Reserved
Bits	Description								
04h-00h	Reserved								
0Ah-05h	<Tcwl> clocks								
1Fh-0Bh	Reserved								

D18F2x210_dct[0]_nbp[3:0] DRAM NB P-state

See 2.9.3 [DCT Configuration Registers]. For D18F2x210_dct[0]_nbp[x], x=D18F1x10C[NbPsSel]; see D18F1x10C[NbPsSel].

Table 167: BIOS Recommendations for RdPtrInit

Condition		D18F2x210_dct[0]_nbp[3:0]
NBCOF >= DdrRate	DdrRate	RdPtrInit
0	-	0010b
1	667, 800, 1066, 1333, 1600	0110b
1	1866, 2133	0101b

Bits	Description								
31:22	MaxRdLatency: maximum read latency. Read-write. IF (BootFromDRAM) THEN Cold reset: Fuse[PA_MaxRdLatency[9:0]]. ELSE Reset: 000h. ENDIF. BIOS: See 2.9.7.9.5 [Calculating MaxRdLatency]. Specifies the maximum round-trip latency in the system from the processor to the DRAM devices and back. The DRAM controller uses this to help determine when the first two beats of incoming DRAM read data can be safely transferred to the NCLK domain. The time includes the asynchronous and synchronous latencies. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>0 NCLKs</td> </tr> <tr> <td>3FEh-001h</td> <td><MaxRdLatency> NCLKs</td> </tr> <tr> <td>3FFh</td> <td>1023 NCLKs</td> </tr> </tbody> </table>	Bits	Description	000h	0 NCLKs	3FEh-001h	<MaxRdLatency> NCLKs	3FFh	1023 NCLKs
Bits	Description								
000h	0 NCLKs								
3FEh-001h	<MaxRdLatency> NCLKs								
3FFh	1023 NCLKs								
21:19	Reserved.								

18:16	DataTxFifoWrDly: data transmit FIFO write delay. Read-write. IF (BootFromDRAM) THEN Cold reset: 0h. ELSE Reset: 0. ENDIF. BIOS: 0h. Specifies the DCT to phy write data FIFO delay.																		
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr><td>000b</td><td>0 MEMCLK</td></tr> <tr><td>001b</td><td>0.5 MEMCLK</td></tr> <tr><td>010b</td><td>1.0 MEMCLK</td></tr> <tr><td>011b</td><td>1.5 MEMCLKs</td></tr> <tr><td>100b</td><td>2.0 MEMCLKs</td></tr> <tr><td>101b</td><td>2.5 MEMCLKs</td></tr> <tr><td>110b</td><td>3.0 MEMCLKs</td></tr> <tr><td>111b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	000b	0 MEMCLK	001b	0.5 MEMCLK	010b	1.0 MEMCLK	011b	1.5 MEMCLKs	100b	2.0 MEMCLKs	101b	2.5 MEMCLKs	110b	3.0 MEMCLKs	111b	Reserved
Bits	Description																		
000b	0 MEMCLK																		
001b	0.5 MEMCLK																		
010b	1.0 MEMCLK																		
011b	1.5 MEMCLKs																		
100b	2.0 MEMCLKs																		
101b	2.5 MEMCLKs																		
110b	3.0 MEMCLKs																		
111b	Reserved																		
15:4	Reserved.																		
3:0	RdPtrInit: read pointer initial value. Read-write. IF (BootFromDRAM) THEN Cold reset: 4h. ELSE Reset: 6h. ENDIF. BIOS: Table 167 . There is a synchronization FIFO between the NB clock domain and memory clock domain. Each increment of this field positions the read pointer one half clock cycle closer to the write pointer thereby reducing the latency through the FIFO. BIOS must program this field for the current or target NB P-state prior to a frequency change or NB P-state change.																		
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr><td>0001b-0000b</td><td>Reserved</td></tr> <tr><td>0010b</td><td>3 MEMCLK</td></tr> <tr><td>0011b</td><td>2.5 MEMCLK</td></tr> <tr><td>0100b</td><td>2 MEMCLKs</td></tr> <tr><td>0101b</td><td>1.5 MEMCLKs</td></tr> <tr><td>0110b</td><td>1 MEMCLKs</td></tr> <tr><td>1111b-0111b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	0001b-0000b	Reserved	0010b	3 MEMCLK	0011b	2.5 MEMCLK	0100b	2 MEMCLKs	0101b	1.5 MEMCLKs	0110b	1 MEMCLKs	1111b-0111b	Reserved		
Bits	Description																		
0001b-0000b	Reserved																		
0010b	3 MEMCLK																		
0011b	2.5 MEMCLK																		
0100b	2 MEMCLKs																		
0101b	1.5 MEMCLKs																		
0110b	1 MEMCLKs																		
1111b-0111b	Reserved																		

D18F2x214_dct[0]_mp[1:0] DDR3 DRAM Timing 4

IF (BootFromDRAM) THEN Cold reset: 0001_0304h. ELSE Reset: 0001_0202h. ENDIF.

Bits	Description												
31:20	Reserved.												
19:16	TwrwrSdSc: write to write timing same DIMM same chip select. Read-write. BIOS: See 2.9.7.6.2 [TwrwrSdSc, TwrwrSdDc, TwrwrDd (Write to Write Timing)] . Specifies the minimum number of cycles from the last clock of virtual CAS of the first write-burst operation to the clock in which CAS is asserted for a following write-burst operation.												
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr><td>0h</td><td>Reserved</td></tr> <tr><td>1h</td><td>1 clock</td></tr> <tr><td>Ah-2h</td><td><TwrwrSdSc> clocks</td></tr> <tr><td>Bh</td><td>11 clocks</td></tr> <tr><td>Fh-Ch</td><td>Reserved</td></tr> </tbody> </table> <p>e.g. TwrwrSdSc=1h, BL=8: WR NOP NOP NOP (LVC) WR NOP NOP NOP (LVC) ...</p> <p>e.g. TwrwrSdSc=2h, BL=8: WR NOP NOP NOP (LVC) NOP WR NOP NOP (LVC) ...</p>	Bits	Description	0h	Reserved	1h	1 clock	Ah-2h	<TwrwrSdSc> clocks	Bh	11 clocks	Fh-Ch	Reserved
Bits	Description												
0h	Reserved												
1h	1 clock												
Ah-2h	<TwrwrSdSc> clocks												
Bh	11 clocks												
Fh-Ch	Reserved												
15:12	Reserved.												

11:8	TwrwrSdDc: write to write timing same DIMM different chip select. See: TwrwrDd.								
7:4	Reserved.								
3:0	TwrwrDd: write to write timing different DIMM. Read-write. BIOS: See 2.9.7.6.2 [TwrwrSdSc, TwrwrSdDc, TwrwrDd (Write to Write Timing)] . Specifies the minimum number of cycles from the last clock of virtual CAS of the first write-burst operation to the clock in which CAS is asserted for a following write-burst operation. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>1h-0h</td> <td>Reserved</td> </tr> <tr> <td>Bh-2h</td> <td><TwrwrDd> clocks</td> </tr> <tr> <td>Fh-Ch</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	1h-0h	Reserved	Bh-2h	<TwrwrDd> clocks	Fh-Ch	Reserved
<u>Bits</u>	<u>Description</u>								
1h-0h	Reserved								
Bh-2h	<TwrwrDd> clocks								
Fh-Ch	Reserved								

D18F2x218_dct[0]_mp[1:0] DDR3 DRAM Timing 5

IF (BootFromDRAM) THEN Cold reset: 0102_0303h. ELSE Reset: 0103_0203h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description										
31:30	TrdrdBan: read to read timing ban. Read-write. BIOS: 00b. Bans the traffic for the specified cases where the number of cycles from the last clock of virtual CAS of a first read-burst operation to the clock in which CAS is asserted for a following read-burst operation. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Ban disabled, traffic allowed as specified by TrdrdSdSc, TrdrdSdDc, TrdrdDd.</td> </tr> <tr> <td>01b</td> <td>Ban Trdrd traffic at 2 MEMCLKs.</td> </tr> <tr> <td>10b</td> <td>Ban Trdrd traffic at 2 and 3 MEMCLKs.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table> e.g. TrdrdSdSc=1h, TrdrdSdScBan=1h, BL=8: Allowed: RD NOP NOP NOP (LVC) RD NOP NOP NOP (LVC) ... Allowed: RD NOP NOP NOP (LVC) NOP NOP RD NOP NOP NOP (LVC) ... Banned: RD NOP NOP NOP (LVC) NOP RD NOP NOP NOP (LVC) ...	<u>Bits</u>	<u>Description</u>	00b	Ban disabled, traffic allowed as specified by TrdrdSdSc, TrdrdSdDc, TrdrdDd.	01b	Ban Trdrd traffic at 2 MEMCLKs.	10b	Ban Trdrd traffic at 2 and 3 MEMCLKs.	11b	Reserved
<u>Bits</u>	<u>Description</u>										
00b	Ban disabled, traffic allowed as specified by TrdrdSdSc, TrdrdSdDc, TrdrdDd.										
01b	Ban Trdrd traffic at 2 MEMCLKs.										
10b	Ban Trdrd traffic at 2 and 3 MEMCLKs.										
11b	Reserved										
29:28	Reserved.										
27:24	TrdrdSdSc: read to read timing same DIMM same chip select. Read-write. BIOS: See 2.9.7.6.1 [TrdrdSdSc, TrdrdSdDc, and TrdrdDd (Read to Read Timing)] . Specifies the minimum number of cycles from the last clock of virtual CAS of a first read-burst operation to the clock in which CAS is asserted for a following read-burst operation. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> </tr> <tr> <td>Bh-1h</td> <td><TrdrdSdSc> clocks</td> </tr> <tr> <td>Fh-Ch</td> <td>Reserved</td> </tr> </tbody> </table> e.g. TrdrdSdSc=1h, BL=8: RD NOP NOP NOP (LVC) RD NOP NOP NOP (LVC) ... e.g. TrdrdSdSc=2h, BL=8: RD NOP NOP NOP (LVC) NOP RD NOP NOP NOP (LVC) ...	<u>Bits</u>	<u>Description</u>	0h	Reserved	Bh-1h	<TrdrdSdSc> clocks	Fh-Ch	Reserved		
<u>Bits</u>	<u>Description</u>										
0h	Reserved										
Bh-1h	<TrdrdSdSc> clocks										
Fh-Ch	Reserved										
23:20	Reserved.										
19:16	TrdrdSdDc: read to read timing same DIMM different chip select. See: TrdrdDd.										
15:12	Reserved.										

11:8	<p>Twrrd: write to read DIMM termination turnaround. Read-write. BIOS: See 2.9.7.6.3 [Twrrd (Write to Read DIMM Termination Turn-around)]. Specifies the minimum number of cycles from the last clock of virtual CAS of the first write-burst operation to the clock in which CAS is asserted for a following read-burst operation, both to different chip selects.</p> <table border="0"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th><th style="text-align: left;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0h</td><td>Reserved</td></tr> <tr> <td>Bh-1h</td><td><Twrrd> clocks</td></tr> <tr> <td>Fh-Ch</td><td>Reserved</td></tr> </tbody> </table> <p>e.g. Twrrd=1h, BL=8: WR NOP NOP NOP (LVC) RD NOP NOP NOP (LVC) ...</p>	<u>Bits</u>	<u>Description</u>	0h	Reserved	Bh-1h	<Twrrd> clocks	Fh-Ch	Reserved
<u>Bits</u>	<u>Description</u>								
0h	Reserved								
Bh-1h	<Twrrd> clocks								
Fh-Ch	Reserved								
7:4	Reserved.								
3:0	<p>TrdrdDd: read to read timing different DIMM. Read-write. BIOS: See 2.9.7.6.1 [TrdrdSdSc, TrdrdSdDc, and TrdrdDd (Read to Read Timing)]. Specifies the minimum number of cycles from the last clock of virtual CAS of a first read-burst operation to the clock in which CAS is asserted for a following read-burst operation.</p> <table border="0"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>1h-0h</td> <td>Reserved</td> </tr> <tr> <td>Bh-2h</td> <td><TrdrdDd> clocks</td> </tr> <tr> <td>Fh-Ch</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	1h-0h	Reserved	Bh-2h	<TrdrdDd> clocks	Fh-Ch	Reserved
<u>Bits</u>	<u>Description</u>								
1h-0h	Reserved								
Bh-2h	<TrdrdDd> clocks								
Fh-Ch	Reserved								

D18F2x21C_dct[0]_mp[1:0] DDR3 DRAM Timing 6

IF (BootFromDRAM) THEN Cold reset: 0005_0500h. ELSE Reset: 0004_0300h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description								
31:21	Reserved. [23:21] are reserved for TrwtWB.								
20:16	<p>TrwtWB: read to write turnaround for opportunistic write bursting. Read-write. BIOS: TrwtTO + 1. Specifies the minimum number of clock cycles from the last clock of virtual CAS of a first read-burst operation to the clock in which CAS is asserted for a following write-burst operation. The purpose of this field is to hold off write operations until several cycles have elapsed without a read cycle; this may result in performance benefits.</p> <table border="0"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>02h-00h</td> <td>Reserved</td> </tr> <tr> <td>1Ch-03h</td> <td><TrwtWB> clocks</td> </tr> <tr> <td>1Fh-1Dh</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	02h-00h	Reserved	1Ch-03h	<TrwtWB> clocks	1Fh-1Dh	Reserved
<u>Bits</u>	<u>Description</u>								
02h-00h	Reserved								
1Ch-03h	<TrwtWB> clocks								
1Fh-1Dh	Reserved								
15:13	Reserved.								

12:8	TrwtTO: read to write turnaround. Read-write. BIOS: See 2.9.7.6.4 [TrwtTO (Read-to-Write Turnaround for Data, DQS Contention)] . Specifies the minimum number of clock cycles from the last clock of virtual CAS of a first read-burst operation to the clock in which CAS is asserted for a following write-burst operation. <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>01h-00h</td><td>Reserved</td></tr> <tr> <td>1Bh-02h</td><td><TrwtTO> clocks</td></tr> <tr> <td>1Fh-1Ch</td><td>Reserved</td></tr> </tbody> </table> e.g. TrwtTO=2h, BL=8: RD NOP NOP NOP (LVC) NOP WR NOP NOP NOP (LVC) ...	<u>Bits</u>	<u>Description</u>	01h-00h	Reserved	1Bh-02h	<TrwtTO> clocks	1Fh-1Ch	Reserved
<u>Bits</u>	<u>Description</u>								
01h-00h	Reserved								
1Bh-02h	<TrwtTO> clocks								
1Fh-1Ch	Reserved								
7:0	Reserved.								

D18F2x220_dct[0] DDR3 DRAM Timing 7

IF (BootFromDRAM) THEN Cold reset: 0000_0505h. ELSE Reset: 0000_0C04h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description								
31:13	Reserved. [15:13] are reserved for Tmod.								
12:8	Tmod: mode register command delay. Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time in memory clock cycles from an MRS command to another non-MRS command (excluding NOP and DES), all to the same chip select. <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>1h-0h</td><td>Reserved</td></tr> <tr> <td>14h-2h</td><td><Tmod> clocks</td></tr> <tr> <td>1Fh-15h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	1h-0h	Reserved	14h-2h	<Tmod> clocks	1Fh-15h	Reserved
<u>Bits</u>	<u>Description</u>								
1h-0h	Reserved								
14h-2h	<Tmod> clocks								
1Fh-15h	Reserved								
7:4	Reserved.								
3:0	Tmrdrd: mode register command cycle time. Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time in memory clock cycles from an MRS command to another MRS command, all to the same chip select. <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>1h-0h</td><td>Reserved</td></tr> <tr> <td>8h-2h</td><td><Tmrdrd> clocks</td></tr> <tr> <td>Fh-9h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	1h-0h	Reserved	8h-2h	<Tmrdrd> clocks	Fh-9h	Reserved
<u>Bits</u>	<u>Description</u>								
1h-0h	Reserved								
8h-2h	<Tmrdrd> clocks								
Fh-9h	Reserved								

D18F2x224_dct[0] DDR3 DRAM Timing 8

IF (BootFromDRAM) THEN Cold reset: 0000_0408h. ELSE Reset: 0000_0408h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:11	Reserved. [15:11] are reserved for Tzqcs.

10:8	Tzqes: Zq short cal command delay. Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time in memory clock cycles from a ZQCS command to any other command (excluding NOP and DES) on the channel.																																				
	<table> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Reserved</td><td>100b</td><td>64 clocks</td></tr> <tr> <td>001b</td><td>16 clocks</td><td>101b</td><td>80 clocks</td></tr> <tr> <td>010b</td><td>32 clocks</td><td>110b</td><td>96 clocks</td></tr> <tr> <td>011b</td><td>48 clocks</td><td>111b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	Bits	Description	000b	Reserved	100b	64 clocks	001b	16 clocks	101b	80 clocks	010b	32 clocks	110b	96 clocks	011b	48 clocks	111b	Reserved																
Bits	Description	Bits	Description																																		
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001b	16 clocks	101b	80 clocks																																		
010b	32 clocks	110b	96 clocks																																		
011b	48 clocks	111b	Reserved																																		
7:4	Reserved.																																				
3:0	Tzqoper: Zq long cal command delay. Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time in memory clock cycles from a ZQCL command to any other command (excluding NOP and DES) on the channel.																																				
	<table> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000b</td><td>Reserved</td><td>1000b</td><td>256 clocks</td></tr> <tr> <td>0001b</td><td>32 clocks</td><td>1001b</td><td>288 clocks</td></tr> <tr> <td>0010b</td><td>64 clocks</td><td>1010b</td><td>320 clocks</td></tr> <tr> <td>0011b</td><td>96 clocks</td><td>1011b</td><td>352 clocks</td></tr> <tr> <td>0100b</td><td>128 clocks</td><td>1100b</td><td>384 clocks</td></tr> <tr> <td>0101b</td><td>160 clocks</td><td>1111b-1101b</td><td>Reserved</td></tr> <tr> <td>0110b</td><td>192 clocks</td><td></td><td></td></tr> <tr> <td>0111b</td><td>224 clocks</td><td></td><td></td></tr> </tbody> </table>	Bits	Description	Bits	Description	0000b	Reserved	1000b	256 clocks	0001b	32 clocks	1001b	288 clocks	0010b	64 clocks	1010b	320 clocks	0011b	96 clocks	1011b	352 clocks	0100b	128 clocks	1100b	384 clocks	0101b	160 clocks	1111b-1101b	Reserved	0110b	192 clocks			0111b	224 clocks		
Bits	Description	Bits	Description																																		
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0100b	128 clocks	1100b	384 clocks																																		
0101b	160 clocks	1111b-1101b	Reserved																																		
0110b	192 clocks																																				
0111b	224 clocks																																				

D18F2x228_dct[0] DDR3 DRAM Timing 9

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description								
31:24	Tstag3: auto refresh stagger time for logical DIMM 3. See: Tstag0.								
23:16	Tstag2: auto refresh stagger time for logical DIMM 2. See: Tstag0.								
15:8	Tstag1: auto refresh stagger time for logical DIMM 1. See: Tstag0.								
7:0	<p>Tstag0: auto refresh stagger time for logical DIMM 0. Read-write. IF (BootFromDRAM) THEN Cold reset: 14h. ELSE Reset: 00h. ENDIF. BIOS: MAX(D18F2x204_dct[0].mp[1:0][Trdd], CEIL(D18F2x204_dct[0].mp[1:0][FourActWindow]/4)).</p> <p>Specifies the number of clocks between auto refresh commands to different ranks of a DIMM when D18F2x90_dct[0][StagRefEn]=1.</p> <p>For UDIMM and RDIMMs, the assumption is that the worst Trdd/Tfaw spec is a best available proxy for a minimum stagger value.</p> <p>$Tstag_{max} = D18F2x8C_dct[0][Tref] \text{ clocks} / \# \text{ of physical ranks present}$, such that all ranks can be refreshed within a Tref period.</p> <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>0 clocks</td></tr> <tr> <td>FEh-01h</td><td><Tstag0> clocks</td></tr> <tr> <td>FFh</td><td>255 clocks</td></tr> </tbody> </table>	Bits	Description	00h	0 clocks	FEh-01h	<Tstag0> clocks	FFh	255 clocks
Bits	Description								
00h	0 clocks								
FEh-01h	<Tstag0> clocks								
FFh	255 clocks								

D18F2x22C_dct[0]_mp[1:0] DDR3 DRAM Timing 10

IF (BootFromDRAM) THEN Cold reset: 0000_000Ch. ELSE Reset: 0000_000Ch. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description																												
31:5	Reserved.																												
4:0	Twr: write recovery. Read-write. BIOS: See 2.9.7.5 . Specifies the minimum time from the last data write until the chip select bank precharge. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>4h-0h</td> <td>Reserved</td> </tr> <tr> <td>8h-5h</td> <td>8 to 5 clocks</td> </tr> <tr> <td>9h</td> <td>Reserved</td> </tr> <tr> <td>Ah</td> <td>10 clocks</td> </tr> <tr> <td>Bh</td> <td>Reserved</td> </tr> <tr> <td>Ch</td> <td>12 clocks</td> </tr> <tr> <td>Dh</td> <td>Reserved</td> </tr> <tr> <td>Eh</td> <td>14 clocks</td> </tr> <tr> <td>Fh</td> <td>Reserved</td> </tr> <tr> <td>10h</td> <td>16 clocks</td> </tr> <tr> <td>11h</td> <td>Reserved</td> </tr> <tr> <td>12h</td> <td>18 clocks</td> </tr> <tr> <td>1Fh-13h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	4h-0h	Reserved	8h-5h	8 to 5 clocks	9h	Reserved	Ah	10 clocks	Bh	Reserved	Ch	12 clocks	Dh	Reserved	Eh	14 clocks	Fh	Reserved	10h	16 clocks	11h	Reserved	12h	18 clocks	1Fh-13h	Reserved
Bits	Description																												
4h-0h	Reserved																												
8h-5h	8 to 5 clocks																												
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Fh	Reserved																												
10h	16 clocks																												
11h	Reserved																												
12h	18 clocks																												
1Fh-13h	Reserved																												

D18F2x[234:230]_dct[0] DDR3 DRAM Read ODT Pattern [High:Low]

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). This register is used by BIOS to specify the state of the ODT pins during DDR reads. F2x230 is used to control chip selects 0-3. F2x234 is used to control chip selects 4-7.

See [2.9.7.6.5 \[DRAM ODT Control\]](#) and Table343 [DIMM, Chip Select, and Register Mapping] for more information.

Bits	Description
31:28	Reserved.
27:24	RdOdtPatCs73: read ODT pattern chip select [7,3]. See: RdOdtPatCs40.
23:20	Reserved.
19:16	RdOdtPatCs62: read ODT pattern chip select [6,2]. See: RdOdtPatCs40.
15:12	Reserved.
11:8	RdOdtPatCs51: read ODT pattern chip select [5,1]. See: RdOdtPatCs40.
7:4	Reserved.
3:0	RdOdtPatCs40: read ODT pattern chip select [4,0]. Read-write. Specifies the state of ODT[3:0] pins when a read occurs to the specified chip select.

D18F2x[23C:238]_dct[0] DDR3 DRAM Write ODT Pattern [High:Low]

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). This register is used by BIOS to specify the state of the ODT pins during DDR

writes. F2x238 is used to control chip selects 0-3. F2x23C is used to control chip selects 4-7.

See [2.9.7.6.5 \[DRAM ODT Control\]](#) and [Table343 \[DIMM, Chip Select, and Register Mapping\]](#) for more information.

Bits	Description
31:28	Reserved.
27:24	WrOdtPatCs73: write ODT pattern chip select [7,3]. See: WrOdtPatCs40.
23:20	Reserved.
19:16	WrOdtPatCs62: write ODT pattern chip select [6,2]. See: WrOdtPatCs40.
15:12	Reserved.
11:8	WrOdtPatCs51: write ODT pattern chip select [5,1]. See: WrOdtPatCs40.
7:4	Reserved.
3:0	WrOdtPatCs40: write ODT pattern chip select [4,0]. Read-write. Specifies the state of ODT[3:0] pins when a write occurs to the specified chip select.

D18F2x240_dct[0]_mp[1:0] DDR3 DRAM ODT Control

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description								
31:15	Reserved.								
14:12	WrOdtOnDuration: write ODT on duration. Read-write. BIOS: 6. Specifies the number of memory clock cycles that ODT is asserted for writes. Normally, WrOdtOnDuration = BL/2 + 2. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 clocks (Don't assert ODT)</td> </tr> <tr> <td>5h-1h</td> <td><WrOdtOnDuration> clocks</td> </tr> <tr> <td>7h-6h</td> <td><WrOdtOnDuration> clocks</td> </tr> </tbody> </table>	Bits	Description	0h	0 clocks (Don't assert ODT)	5h-1h	<WrOdtOnDuration> clocks	7h-6h	<WrOdtOnDuration> clocks
Bits	Description								
0h	0 clocks (Don't assert ODT)								
5h-1h	<WrOdtOnDuration> clocks								
7h-6h	<WrOdtOnDuration> clocks								
11	Reserved.								
10:8	WrOdtTrnOnDly: Write ODT Turn On Delay. Read-write. BIOS: 0. Specifies the number of memory clock cycles that ODT assertion is delayed relative to write CAS. (0h = ODT asserted with internal CAS). <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 clocks</td> </tr> <tr> <td>7h-1h</td> <td><WrOdtTrnOnDly> clocks, Reserved if (WrOdtOnDuration=0)</td> </tr> </tbody> </table>	Bits	Description	0h	0 clocks	7h-1h	<WrOdtTrnOnDly> clocks, Reserved if (WrOdtOnDuration=0)		
Bits	Description								
0h	0 clocks								
7h-1h	<WrOdtTrnOnDly> clocks, Reserved if (WrOdtOnDuration=0)								

7:4	RdOdtOnDuration: Read ODT On Duration. Read-write. BIOS: 6. Specifies the number of memory clock cycles that ODT is asserted for an eight-beat read burst. The controller will shorten the ODT pulse duration by two clock cycles if the burst is chopped. Normally, RdOdtOnDuration = BL/2 + 2.										
	<table> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 clocks (Don't assert ODT)</td> </tr> <tr> <td>5h-1h</td> <td><RdOdtOnDuration> clocks</td> </tr> <tr> <td>9h-6h</td> <td><RdOdtOnDuration> clocks</td> </tr> <tr> <td>Fh-Ah</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	0 clocks (Don't assert ODT)	5h-1h	<RdOdtOnDuration> clocks	9h-6h	<RdOdtOnDuration> clocks	Fh-Ah	Reserved
<u>Bits</u>	<u>Description</u>										
0h	0 clocks (Don't assert ODT)										
5h-1h	<RdOdtOnDuration> clocks										
9h-6h	<RdOdtOnDuration> clocks										
Fh-Ah	Reserved										
3:0	RdOdtTrnOnDly: Read ODT Turn On Delay. Read-write. BIOS: MAX(0, D18F2x200_dct[0].mp[1:0][Tcl] - D18F2x20C_dct[0].mp[1:0][Tcwl]). Specifies the number of clock cycles that ODT assertion is delayed relative to read CAS. (0h = ODT asserted with internal CAS).										
	<table> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 clocks</td> </tr> <tr> <td>Fh-0h</td> <td><RdOdtTrnOnDly> clocks, Reserved if (RdOdtOnDuration=0)</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	0 clocks	Fh-0h	<RdOdtTrnOnDly> clocks, Reserved if (RdOdtOnDuration=0)				
<u>Bits</u>	<u>Description</u>										
0h	0 clocks										
Fh-0h	<RdOdtTrnOnDly> clocks, Reserved if (RdOdtOnDuration=0)										

D18F2x244_dct[0] DRAM Controller Miscellaneous 3

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description										
7:4	Reserved.										
3:0	PrtlChPDDynDly: partial channel power down dynamic delay. Read-write. BIOS:4h. Specifies the channel idle hysteresis for fast exit/slow exit mode changes when D18F2xA8_dct[0][PrtlChP-DEnhEn]=1.										
	<table> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 clocks</td> </tr> <tr> <td>7h-1h</td> <td><PrtlChPDDynDly*32> clocks</td> </tr> <tr> <td>8h</td> <td>256 clocks</td> </tr> <tr> <td>Fh-9h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	0 clocks	7h-1h	<PrtlChPDDynDly*32> clocks	8h	256 clocks	Fh-9h	Reserved
<u>Bits</u>	<u>Description</u>										
0h	0 clocks										
7h-1h	<PrtlChPDDynDly*32> clocks										
8h	256 clocks										
Fh-9h	Reserved										

D18F2x248_dct[0].mp[1:0] DRAM Power Management 0

IF (BootFromDRAM) THEN Cold reset: 0000_0C05h. ELSE Reset: 0000_0A03h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31	RxChMntClkEn: Receive channel maintenance clocks. Read-Write. BIOS: 0. 1=Enable receive channel maintenance clocks to improve internal timing margin at the cost of some extra power. 0=Disable clocks. To disable clocks, BIOS must first disable clock generation in the phy (see D18F2x9C_x0D0F_0[F,8:0]13_dct[0].mp[1:0][RxSsbMntClkEn]).
30	Reserved.

29:24	<p>AggrPDDelay: aggressive power down delay. Read-Write. BIOS: 20h. Specifies a hysteresis count from the last DRAM activity for the DCT to close pages prior to precharge power down. The counter does not start until the DCQ, RDQ, and WDQ are empty. The counter runs orthogonal to the page policy specified by D18F2x90_dct[0][DynPageCloseEn]. Reserved if D18F2xA8_dct[0][AggrPDEn]==0. See PchgPDEnDelay and D18F2x94_dct[0][PowerDownEn].</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>64 clocks</td></tr> <tr> <td>01h</td><td>1 clock</td></tr> <tr> <td>3Eh-02h</td><td><AggrPDDelay> clocks</td></tr> <tr> <td>3Fh</td><td>63 clocks</td></tr> </tbody> </table>	Bits	Description	00h	64 clocks	01h	1 clock	3Eh-02h	<AggrPDDelay> clocks	3Fh	63 clocks
Bits	Description										
00h	64 clocks										
01h	1 clock										
3Eh-02h	<AggrPDDelay> clocks										
3Fh	63 clocks										
23:22	Reserved.										
21:16	<p>PchgPDEnDelay: precharge power down entry delay. Read-write. BIOS: IF (D18F2xA8_dct[0][AggrPDEn]) THEN (D18F2x200_dct[0].mp[1:0][Tcl] + 5 + CEIL((MAX(D18F2x9C_x0000_00[2A:10].dct[0].mp[1:0][DqsRcvEnGrossDelay]) + 0.5) / 2)) ELSE 00h ENDIF.</p> <p>Specifies the power down entry delay. If D18F2xA8_dct[0][AggrPDEn]==0, this delay behaves as a hysteresis. This field must satisfy the minimum power down entry delay requirements. See also D18F2x94_dct[0][PowerDownEn].</p> <p>Rule: PchgPDEnDelay == 0 PchgPDEnDelay >= D18F2x200_dct[0].mp[1:0][Tcl] + 5 + CEIL((MAX(D18F2x9C_x0000_00[2A:10].dct[0].mp[1:0][DqsRcvEnGrossDelay]) + 0.5) / 2).</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>64 clocks</td></tr> <tr> <td>01h</td><td>1 clock</td></tr> <tr> <td>3Eh-02h</td><td><PchgPDEnDelay> clocks</td></tr> <tr> <td>3Fh</td><td>63 clocks</td></tr> </tbody> </table>	Bits	Description	00h	64 clocks	01h	1 clock	3Eh-02h	<PchgPDEnDelay> clocks	3Fh	63 clocks
Bits	Description										
00h	64 clocks										
01h	1 clock										
3Eh-02h	<PchgPDEnDelay> clocks										
3Fh	63 clocks										
15:13	Reserved.										
12:8	<p>Txdll: exit DLL and precharge powerdown to command delay. Read-write. Specifies the minimum time that the DCT waits to issue a command after exiting precharge powerdown mode if the DLL was also disabled.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>09h-00h</td><td>Reserved</td></tr> <tr> <td>1Dh-0Ah</td><td><Txdll> clocks</td></tr> <tr> <td>1Fh-1Eh</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	09h-00h	Reserved	1Dh-0Ah	<Txdll> clocks	1Fh-1Eh	Reserved		
Bits	Description										
09h-00h	Reserved										
1Dh-0Ah	<Txdll> clocks										
1Fh-1Eh	Reserved										
7:4	Reserved.										
3:0	<p>Txp: exit precharge PD to command delay. Read-write. Specifies the minimum time that the DCT waits to issue a command after exiting precharge powerdown mode.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>2h-0h</td><td>Reserved</td></tr> <tr> <td>8h-3h</td><td><Txp> clocks</td></tr> <tr> <td>Fh-9h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	2h-0h	Reserved	8h-3h	<Txp> clocks	Fh-9h	Reserved		
Bits	Description										
2h-0h	Reserved										
8h-3h	<Txp> clocks										
Fh-9h	Reserved										

D18F2x24C_dct[0] DDR3 DRAM Power Management 1

IF ([BootFromDRAM](#)) THEN Cold reset: 0214_0803h. ELSE Reset: 0214_0803h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:30	Reserved.
29:24	Tcksrx: clock stable to self refresh exit delay. Read-write. Specifies the minimum time in memory clock cycles that the DCT waits to assert CKE after clock frequency is stable. <u>Bits</u> <u>Description</u> 01h-00h Reserved 0Eh-02h <Tcksrx> clocks 3Fh-0Fh Reserved
23:22	Reserved.
21:16	Tcksre: self refresh to command delay. Read-write. Specifies the minimum time in memory clock cycles that the DCT waits to remove external clocks after entering self refresh or powerdown. <u>Bits</u> <u>Description</u> 04h-00h Reserved 27h-05h <Tcksre> clocks 3Fh-28h Reserved
15:14	Reserved.
13:8	Tckesr: self refresh to command delay. Read-write. Specifies the minimum time in memory clock cycles that the DCT waits to issue a command after entering self refresh. <u>Bits</u> <u>Description</u> 01h-00h Reserved 2Bh-02h <Tckesr> clocks 3Fh-2Ch Reserved
7:4	Reserved.
3:0	Tpd: minimum power down entry to exit. Read-write. Specifies minimum time in memory clock cycles for powerdown entry to exit timing. <u>Bits</u> <u>Description</u> 0h Reserved Ah-1h <Tpd> clocks Fh-Bh Reserved

D18F2x250_dct[0] DRAM Loopback and Training Control

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See 2.9.3 [DCT Configuration Registers]. See 2.9.8 [Continuous Pattern Generation].

Bits	Description
20:18	DataPatGenSel: data pattern generator select. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only; S3-check-exclude. ELSE Read-write; S3-check-exclude. ENDIF. <u>Bits</u> <u>Description</u> 000b PRBS23 I. 001b PRBS23 II. Within a byte lane, the DQ[n] value is offset 8n bit times from DQ[0]. 010b Configurable data pattern. See D18F2x2[B4,B0,AC,A8]_dct[0]. 011b Configurable data pattern with circular lane shift. See D18F2x2[B4,B0,AC,A8]_dct[0]. 100b PRBS23 III. Within a byte lane, each DQ[n] value is equal to DQ[0]. 111b-101b Reserved.

17	ActPchgGenEn: activate precharge generation enable. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. 1=The DCT generates ACT and PRE traffic in the available command bandwidth from SendCmd. 0=Traffic generation is not enabled. Reserved if ~CmdTestEnable .										
15	Reserved. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read; write-1-only; cleared-by-hardware. ENDIF.										
13	LfsrRollOver: LFSR roll over. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Specifies the behavior of DataPrbsSeed and the data comparison logic if the generated address wraps around to equal D18F2x25[8,4]_dct[0][TgtAddress] . 0=The PRBS will not be re-seeded. 1=The PRBS will be re-seeded.										
12	CmdSendInProg: command in progress. Read-only; updated-by-hardware. 0=DCT is idle. 1=DCT is busy.										
11	SendCmd: send command. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. 0=Stop command generation. 1=Begin command generation as specified in CmdTgt, CmdType, and D18F2x260_dct[0][CmdCount] . BIOS must set this field to a 0 after a command series is completed. Reserved if ~CmdTestEnable .										
10	TestStatus: test status. Read-only. 0=Command generation is in progress. 1=Command generation has completed. Reserved if (~(SendCmd & (D18F2x260_dct[0][CmdCount] > 0) StopOnErr)) .										
9:8	CmdTgt: command target. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Specifies the SendCmd command target address mode. See D18F2x25[8,4]_dct[0] . <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Issue commands to address Target A</td> </tr> <tr> <td>01b</td> <td>Issue alternating commands to address Target A and Target B</td> </tr> <tr> <td>11b-10b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	Issue commands to address Target A	01b	Issue alternating commands to address Target A and Target B	11b-10b	Reserved		
<u>Bits</u>	<u>Description</u>										
00b	Issue commands to address Target A										
01b	Issue alternating commands to address Target A and Target B										
11b-10b	Reserved										
7:5	CmdType: command type. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Specifies the SendCmd command type. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Read</td> </tr> <tr> <td>001b</td> <td>Write</td> </tr> <tr> <td>010b</td> <td>Alternating write and read</td> </tr> <tr> <td>111b-011b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	000b	Read	001b	Write	010b	Alternating write and read	111b-011b	Reserved
<u>Bits</u>	<u>Description</u>										
000b	Read										
001b	Write										
010b	Alternating write and read										
111b-011b	Reserved										
4	StopOnErr: stop on error. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. Specifies the DCT behavior if a data comparison error occurs. 1=Stop command generation. DCT behavior is imprecise, depending on when an error is detected vs. in-flight commands. 0=Continue command generation. If StopOnErr=1, BIOS must program ResetAllErr=1 when programming SendCmd=1.										
3	ResetAllErr: reset all errors. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read; write-1-only; cleared-by-hardware. ENDIF. 1=Clear error status bits and error counters in D18F2x264_dct[0] , D18F2x268_dct[0] , and D18F2x26C_dct[0] . This bit may be written along with SendCmd.										
2	CmdTestEnable: command test enable. IF (D18F2x118[LockDramCfg] & ~D18F3x12C[OverrideLockDramCfg]) THEN Read-only. ELSE Read-write. ENDIF. 0=Disable the command generation mode. 1=Enable the command generation mode. See SendCmd. Enabling this mode disables the DCT speculative precharge logic. Reserved if D18F2x250_dct[0][LoopbackBistEn] .										

D18F2x25[8,4]_dct[0] DRAM Target [B, A] Base

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Table 168: Register Mapping for D18F2x25[8,4]_dct[0]

Register	Function
D18F2x254_dct[0]	Target A
D18F2x258_dct[0]	Target B

Bits	Description				
31:27	Reserved.				
26:24	TgtChipSelect: target chip select. Read-write; S3-check-exclude. Specifies the chip select. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>111b-000b</td> <td>CS<TgtChipSelect></td> </tr> </tbody> </table>	Bits	Description	111b-000b	CS<TgtChipSelect>
Bits	Description				
111b-000b	CS<TgtChipSelect>				
23:21	TgtBank: target bank [2:0]. Read-write; S3-check-exclude. Specifies the bank address.				
20:16	Reserved.				
15:10	TgtAddress[15:10]: target address [15:10]. Read-write; S3-check-exclude. Specifies the upper column address bits [15:10]. Software must always program bit 10 and bit 12 equal to 0.				
9:0	TgtAddress[9:0]: target address [9:0]. Read-write; S3-check-exclude. Specifies the column address bits [9:0]. Column address bits [15:10] = 0. The address sequencing in a command series occurs as follows: TgtAddress[9:3] is incremented by one with wrap around. The increment occurs after each command if D18F2x250_dct[0][CmdType] = 00b or if (D18F2x250_dct[0][CmdType] = 010b and D18F2x250_dct[0][CmdTgt] = 01b). The increment occurs after each command pair if (D18F2x250_dct[0][CmdType] = 010b and D18F2x250_dct[0][CmdTgt] = 00b). The value of TgtAddress is not updated by hardware.				

D18F2x25C_dct[0] DRAM Command 0

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0001h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:22	BubbleCnt2: bubble count 2. See: BubbleCnt. Specifies the number of NOP commands inserted after the last clock of virtual CAS of each read-burst operation in alternating write and read mode. Defined only if (D18F2x250_dct[0][CmdType] == 010b); otherwise reserved.								
21:12	BubbleCnt: bubble count. Read-write; S3-check-exclude. Specifies the number of NOP commands inserted after the last clock of virtual CAS of the last command of the command stream specified by CmdStreamLen. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>0 command bubbles</td> </tr> <tr> <td>3FEh-001h</td> <td><BubbleCnt> command bubbles</td> </tr> <tr> <td>3FFh</td> <td>3FFh command bubbles</td> </tr> </tbody> </table>	Bits	Description	000h	0 command bubbles	3FEh-001h	<BubbleCnt> command bubbles	3FFh	3FFh command bubbles
Bits	Description								
000h	0 command bubbles								
3FEh-001h	<BubbleCnt> command bubbles								
3FFh	3FFh command bubbles								
11:9	Reserved.								

8	CmdTimingEn: command timing enable. Read-write; S3-check-exclude. 1=Forces DCT to schedule RRW commands initiated by D18F2x250_dct[0][SendCmd] to adhere to the same DRAM timing parameters as normal traffic. 0=Commands initiated by D18F2x250_dct[0][SendCmd] ignore DRAM timing parameters.										
7:0	<p>CmdStreamLen: command stream length. Read-write; S3-check-exclude. Specifies the number of commands(CAS's on the bus) generated before BubbleCnt bubbles are inserted.</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 10%;">Bits</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">00h</td> <td>Reserved</td> </tr> <tr> <td style="text-align: left;">01h</td> <td>1 command</td> </tr> <tr> <td style="text-align: left;">FEh-02h</td> <td><CmdStreamLen> commands; defined only if ~(D18F2x250_dct[0][CmdType]=010b)</td> </tr> <tr> <td style="text-align: left;">FFh</td> <td>255 commands; defined only if ~(D18F2x250_dct[0][CmdType]=010b)</td> </tr> </tbody> </table> <p>The following two examples apply for DDR3:</p> <p>e.g. CmdType=000b, BubbleCnt=3, CmdStreamLen=2: RD NOP NOP NOP (LVC) RD NOP NOP NOP (LVC) NOP NOP NOP RD ...</p> <p>e.g. CmdType=010b, BubbleCnt=2 CmdStreamLen=1: WR NOP NOP NOP (LVC) NOP NOP RD NOP NOP NOP (LVC) NOP NOP ...</p>	Bits	Description	00h	Reserved	01h	1 command	FEh-02h	<CmdStreamLen> commands; defined only if ~(D18F2x250_dct[0][CmdType] =010b)	FFh	255 commands; defined only if ~(D18F2x250_dct[0][CmdType] =010b)
Bits	Description										
00h	Reserved										
01h	1 command										
FEh-02h	<CmdStreamLen> commands; defined only if ~(D18F2x250_dct[0][CmdType] =010b)										
FFh	255 commands; defined only if ~(D18F2x250_dct[0][CmdType] =010b)										

D18F2x260_dct[0] DRAM Command 1

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description						
31:21	Reserved.						
20:0	<p>CmdCount: command count. Read-write; S3-check-exclude. Specifies the maximum number of commands to generate when D18F2x250_dct[0][SendCmd]=1. See also D18F2x250_dct[0][StopOnErr].</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 10%;">Bits</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">0h</td> <td>Infinite commands.</td> </tr> <tr> <td style="text-align: left;">1F_FFFFh-1h</td> <td><CmdCount> commands</td> </tr> </tbody> </table>	Bits	Description	0h	Infinite commands.	1F_FFFFh-1h	<CmdCount> commands
Bits	Description						
0h	Infinite commands.						
1F_FFFFh-1h	<CmdCount> commands						

D18F2x264_dct[0] DRAM Status 0

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description
00h	0000_0000h

31:25	<p>ErrDqNum: error DQ number. Read-only; S3-check-exclude. Indicates the DQ bit of the first error occurrence when D18F2x264_dct[0][ErrCnt] > 0. Cleared by D18F2x250_dct[0][ResetAllErr].</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding-bottom: 2px;"><u>Bits</u></th><th style="text-align: left; padding-bottom: 2px;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td style="padding-top: 2px;">3Fh-00h</td><td>Data[<ErrDqNum>]</td></tr> <tr> <td style="padding-top: 2px;">47h-40h</td><td>ECC[7:0]</td></tr> <tr> <td style="padding-top: 2px;">7Fh-48h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	3Fh-00h	Data[<ErrDqNum>]	47h-40h	ECC[7:0]	7Fh-48h	Reserved		
<u>Bits</u>	<u>Description</u>										
3Fh-00h	Data[<ErrDqNum>]										
47h-40h	ECC[7:0]										
7Fh-48h	Reserved										
24:0	<p>ErrCnt: error count. Read; set-by-hardware; write-1-to-clear. Specifies a saturating counter indicating the number of DQ bit errors detected. Counts a maximum of 1 error per bit-lane per each bit-time. Status is accumulated until cleared by D18F2x250_dct[0][ResetAllErr]. Errors can be masked on per-bit basis by programming D18F2x274_dct[0], D18F2x278_dct[0], and D18F2x27C_dct[0].</p> <p>IF D18F2x250_dct[0][LoopbackBistEn] = 1, Mx_RESET_L can be used as an external trigger when an error event occurs. In this mode, a pulse at least 1 MEMCLK wide is asserted on the Mx_RESET_L pin when an error is counted. If D18F2x250_dct[0][StopOnErr]=1, Mxx_RESET_L will be asserted until cleared by D18F2x250_dct[0][ResetAllErr]. In this mode, if any LFSR seed is detected as all 0's then hardware writes all 1's to this field.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding-bottom: 2px;"><u>Bits</u></th><th style="text-align: left; padding-bottom: 2px;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td style="padding-top: 2px;">0h</td><td>0 errors</td></tr> <tr> <td style="padding-top: 2px;">1FF_FFFDh-1h</td><td><ErrCnt> errors</td></tr> <tr> <td style="padding-top: 2px;">1FF_FFFEh</td><td>1FF_FFFEh errors</td></tr> <tr> <td style="padding-top: 2px;">1FF_FFFFh</td><td>1FF_FFFFh or more errors, or any LFSR seed is zero when in loopback mode</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	0 errors	1FF_FFFDh-1h	<ErrCnt> errors	1FF_FFFEh	1FF_FFFEh errors	1FF_FFFFh	1FF_FFFFh or more errors, or any LFSR seed is zero when in loopback mode
<u>Bits</u>	<u>Description</u>										
0h	0 errors										
1FF_FFFDh-1h	<ErrCnt> errors										
1FF_FFFEh	1FF_FFFEh errors										
1FF_FFFFh	1FF_FFFFh or more errors, or any LFSR seed is zero when in loopback mode										

D18F2x268_dct[0] DRAM Status 1

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description										
31:20	Reserved.										
19:0	<p>NibbleErrSts: nibble error status. Read-only; S3-check-exclude. Indicates error detection status on a per nibble basis when D18F2x264_dct[0][ErrCnt] > 0. Status is accumulated until cleared by D18F2x250_dct[0][ResetAllErr].</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding-bottom: 2px;"><u>Bit</u></th><th style="text-align: left; padding-bottom: 2px;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td style="padding-top: 2px;">[15:0]</td><td>Data[<(NibbleErrSts*4)+3>:<NibbleErrSts*4>]</td></tr> <tr> <td style="padding-top: 2px;">[16]</td><td>ECC[3:0]</td></tr> <tr> <td style="padding-top: 2px;">[17]</td><td>ECC[7:4]</td></tr> <tr> <td style="padding-top: 2px;">[19:18]</td><td>Reserved</td></tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	[15:0]	Data[<(NibbleErrSts*4)+3>:<NibbleErrSts*4>]	[16]	ECC[3:0]	[17]	ECC[7:4]	[19:18]	Reserved
<u>Bit</u>	<u>Description</u>										
[15:0]	Data[<(NibbleErrSts*4)+3>:<NibbleErrSts*4>]										
[16]	ECC[3:0]										
[17]	ECC[7:4]										
[19:18]	Reserved										

D18F2x26C_dct[0] DRAM Status 2

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description

31:18	Reserved.								
17:0	<p>NibbleErr180Sts: nibble error 180 status. Read-only; S3-check-exclude. Indicates error detection status on a per nibble basis when D18F2x264_dct[0][ErrCnt] > 0, comparing read data against data shifted 1-bit time earlier. I.e. Hardware compares an incoming bit time 180 degrees out of phase, N=0, 1, ..., 6 read to bit time N=1, 2, ..., 7 written. Status is accumulated until cleared by D18F2x250_dct[0][ResetAllErr].</p> <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[15:0]</td> <td>Data[<(NibbleErr180Sts)*4)+3>:<NibbleErr180Sts*4>]</td> </tr> <tr> <td>[16]</td> <td>ECC[3:0]</td> </tr> <tr> <td>[17]</td> <td>ECC[7:4]</td> </tr> </tbody> </table>	Bit	Description	[15:0]	Data[<(NibbleErr180Sts)*4)+3>:<NibbleErr180Sts*4>]	[16]	ECC[3:0]	[17]	ECC[7:4]
Bit	Description								
[15:0]	Data[<(NibbleErr180Sts)*4)+3>:<NibbleErr180Sts*4>]								
[16]	ECC[3:0]								
[17]	ECC[7:4]								

D18F2x270_dct[0] DRAM PRBS

See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description										
31	Reserved.										
23:19	Reserved.										
18:0	<p>DataPrbsSeed: data PRBS seed. Read-write; S3-check-exclude. IF (BootFromDRAM) THEN Cold reset: 7FFFFh. ELSE Reset: 7FFFh. ENDIF. Specifies the seed value used for creating pseudo random traffic on the data bus. This register must be written with a non-zero seed value. PRBS23 is based on a 23 bit LFSR with polynomial $G(x) = x^{23} + x^{18} + 1$. The LFSR for each byte lane is seeded as follows: {DataPrbsSeed, 4-bit byte lane index}. PRBS bits [7:0] map to byte lane bits [7:0]. Recommended BIOS values for DRAM training:</p> <table> <thead> <tr> <th>CmdCount</th> <th>DataPrbsSeed</th> </tr> </thead> <tbody> <tr> <td>32</td> <td>62221h</td> </tr> <tr> <td>64</td> <td>66665h</td> </tr> <tr> <td>128</td> <td>26666h</td> </tr> <tr> <td>256</td> <td>44443h</td> </tr> </tbody> </table>	CmdCount	DataPrbsSeed	32	62221h	64	66665h	128	26666h	256	44443h
CmdCount	DataPrbsSeed										
32	62221h										
64	66665h										
128	26666h										
256	44443h										

D18F2x274_dct[0] DRAM DQ Mask Low

See [D18F1x10C\[DctCfgSel\]](#). See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:0	<p>DQMask[31:0]: DQ mask. Read-write; S3-check-exclude. DQMask[63:0] = {D18F2x278_dct[0][DQMask[63:32]], DQMask[31:0]}. IF (BootFromDRAM) THEN Cold reset: 0000_0000_0000_0000h. ELSE Reset: 0000_0000_0000_0000h. ENDIF. 1=The corresponding DQ bit will not be compared. 0=The corresponding DQ bit will be compared. See D18F2x264_dct[0][ErrCnt].</p> <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Data[0]</td> </tr> <tr> <td>[62:1]</td> <td>Data[<DQMask>]</td> </tr> <tr> <td>[63]</td> <td>Data[63]</td> </tr> </tbody> </table>	Bit	Description	[0]	Data[0]	[62:1]	Data[<DQMask>]	[63]	Data[63]
Bit	Description								
[0]	Data[0]								
[62:1]	Data[<DQMask>]								
[63]	Data[63]								

D18F2x278_dct[0] DRAM DQ Mask High

Bits	Description
31:0	DQMask[63:32]: DQ mask. See: D18F2x274_dct[0][DQMask[31:0]] .

D18F2x27C_dct[0] DRAM ECC and EDC Mask

IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:20	Reserved.								
19:16	Reserved.								
15:8	Reserved.								
7:0	EccMask: ECC mask. Read-write; S3-check-exclude. 1=The corresponding ECC DQ bit will not be compared. 0=The corresponding ECC DQ bit will be compared. See D18F2x264_dct[0][ErrCnt] . <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>ECC[0]</td> </tr> <tr> <td>[6:1]</td> <td>ECC[<EccMask>]</td> </tr> <tr> <td>[7]</td> <td>ECC[7].</td> </tr> </tbody> </table>	Bit	Description	[0]	ECC[0]	[6:1]	ECC[<EccMask>]	[7]	ECC[7].
Bit	Description								
[0]	ECC[0]								
[6:1]	ECC[<EccMask>]								
[7]	ECC[7].								

D18F2x280_dct[0] DRAM DQ Pattern Override 0

See [D18F1x10C\[DctCfgSel\]](#). See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:0	DQPatOvrEn[31:0]: DQ pattern override enable. Read-write; S3-check-exclude. DQPatOvrEn[63:0] = { D18F2x284_dct[0][DQPatOvrEn[63:32]] , DQPatOvrEn[31:0] }. IF (BootFromDRAM) THEN Cold reset: 0000_0000_0000_0000h. ELSE Reset: 0000_0000_0000_0000h. ENDIF. 1=The pattern on this DQ bit lane will be overridden with a static value specified by D18F2x288_dct[0][PatOvrVal] . 0=The pattern on this DQ bit lane will not be overridden. Reserved if D18F2x250_dct[0][DataPatGenSel] != 10b. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Data[0]</td> </tr> <tr> <td>[62:1]</td> <td>Data[<DQPatOvrEn[31:0]>]</td> </tr> <tr> <td>[63]</td> <td>Data[63]</td> </tr> </tbody> </table>	Bit	Description	[0]	Data[0]	[62:1]	Data[<DQPatOvrEn[31:0]>]	[63]	Data[63]
Bit	Description								
[0]	Data[0]								
[62:1]	Data[<DQPatOvrEn[31:0]>]								
[63]	Data[63]								

D18F2x284_dct[0] DRAM DQ Pattern Override 1

Bits	Description
31:0	DQPatOvrEn[63:32]: DQ pattern override enable. See: D18F2x280_dct[0][DQPatOvrEn[31:0]] .

D18F2x288_dct[0] DRAM DQ Pattern Override 2

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See D18F1x10C[DctCfgSel]. See 2.9.3 [DCT Configuration Registers]. See 2.9.8 [Continuous Pattern Generation].

Bits	Description										
31:24	XorPatOvr: xor pattern override. Read-write; S3-check-exclude. Specifies the override data pattern used. for creating traffic on the data bus. The output data for each DQ of each byte lane will be XOR'd with the specified values. Reserved if D18F2x250_dct[0][DataPatGenSel] != 100b. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>DQ[0]</td> </tr> <tr> <td>[1]</td> <td>DQ[1]</td> </tr> <tr> <td>[6:2]</td> <td>DQ[<XorPatOvr>]</td> </tr> <tr> <td>[7]</td> <td>DQ[7]</td> </tr> </tbody> </table>	Bit	Description	[0]	DQ[0]	[1]	DQ[1]	[6:2]	DQ[<XorPatOvr>]	[7]	DQ[7]
Bit	Description										
[0]	DQ[0]										
[1]	DQ[1]										
[6:2]	DQ[<XorPatOvr>]										
[7]	DQ[7]										
23:9	Reserved.										
8	PatOvrVal: pattern override value. Read-write; S3-check-exclude. Specifies the override data pattern used. for creating traffic on the data bus. 1=Static 1's. 0=Static 0's. Reserved if D18F2x250_dct[0][DataPatGenSel] != 10b.										
7:0	EccPatOvrEn: ECC pattern override enable. Read-write; S3-check-exclude. See D18F2x280_dct[0][DQPatOvrEn] <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>ECC[0]</td> </tr> <tr> <td>[1]</td> <td>ECC[1]</td> </tr> <tr> <td>[6:2]</td> <td>ECC[<EccPatOvr>]</td> </tr> <tr> <td>[7]</td> <td>ECC[7].</td> </tr> </tbody> </table>	Bit	Description	[0]	ECC[0]	[1]	ECC[1]	[6:2]	ECC[<EccPatOvr>]	[7]	ECC[7].
Bit	Description										
[0]	ECC[0]										
[1]	ECC[1]										
[6:2]	ECC[<EccPatOvr>]										
[7]	ECC[7].										

D18F2x28C_dct[0] DRAM Command 2

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See 2.9.3 [DCT Configuration Registers]. See 2.9.8 [Continuous Pattern Generation]. This register may only be used when D18F2x250_dct[0][CmdTestEnable]=1.

Bits	Description
31	SendActCmd: send activate command. Read; write-1-only; cleared-by-hardware. 1=The DCT sends an activate command as specified by ChipSelect, Bank, and Address. This bit is cleared by hardware after the command completes.
30	SendPchgCmd: send precharge all command. Read; write-1-only; cleared-by-hardware. The DCT sends a precharge command based on CmdAddress[10]. This bit is cleared by hardware after the command completes. 0=Command has completed. 1=If (CmdAddress[10]=1) then send a precharge all command as specified by CmdChipSelect; If (CmdAddress[10]=0) then send a precharge command as specified by CmdChipSelect, CmdBank.

29:22	CmdChipSelect: command chip select. Read-write; S3-check-exclude. Specifies the chip select. <table border="1"> <thead> <tr> <th><u>Bit</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>[7:0]</td><td>CS<CmdChipSelect></td></tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	[7:0]	CS<CmdChipSelect>
<u>Bit</u>	<u>Description</u>				
[7:0]	CS<CmdChipSelect>				
21:19	CmdBank: command bank [2:0]. Read-write; S3-check-exclude. Specifies the bank address. <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>7h-0h</td><td>Bank<CmdBank></td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	7h-0h	Bank<CmdBank>
<u>Bits</u>	<u>Description</u>				
7h-0h	Bank<CmdBank>				
18	Reserved.				
17:0	CmdAddress: command address [17:0]. Read-write; S3-check-exclude. Specifies the row address.				

D18F2x290_dct[0] DRAM Status 3

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description				
31:27	Reserved.				
26:24	ErrBeatNum: error beat number. Read-only. Indicates the data beat of the first error occurrence in the command reported by ErrCmdNum when D18F2x264_dct[0][ErrCnt] > 0 and D18F2x260_dct[0][CmdCount] > 0 . Cleared by D18F2x250_dct[0][ResetAllErr] . <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>7h-0h</td><td><ErrBeatNum> beat</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	7h-0h	<ErrBeatNum> beat
<u>Bits</u>	<u>Description</u>				
7h-0h	<ErrBeatNum> beat				
23:21	Reserved.				
20:0	ErrCmdNum: error command number. Read-only. Indicates the command number of the first error occurrence when D18F2x264_dct[0][ErrCnt] > 0 and D18F2x260_dct[0][CmdCount] > 0 . Cleared by D18F2x250_dct[0][ResetAllErr] . <table border="1"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>1F_FFFh-0h</td><td><ErrCmdNum> command</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	1F_FFFh-0h	<ErrCmdNum> command
<u>Bits</u>	<u>Description</u>				
1F_FFFh-0h	<ErrCmdNum> command				

D18F2x294_dct[0] DRAM Status 4

See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:0	DQErr[31:0]: DQ error. Read-only; S3-check-exclude. DQErr[63:0] = { D18F2x298_dct[0][DQErr[63:32]] , DQErr[31:0] }. IF (BootFromDRAM) THEN Cold reset: 0000_0000_0000_0000h. ELSE Reset: 0000_0000_0000_0000h. ENDIF. Indicates error detection status on a per bit basis when D18F2x264_dct[0][ErrCnt] > 0 . Status is accumulated until cleared by D18F2x250_dct[0][ResetAllErr] . <table border="1"> <thead> <tr> <th><u>Bit</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Data[0]</td></tr> <tr> <td>[62:1]</td><td>Data[<DQErr>]</td></tr> <tr> <td>[63]</td><td>Data[63]</td></tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	[0]	Data[0]	[62:1]	Data[<DQErr>]	[63]	Data[63]
<u>Bit</u>	<u>Description</u>								
[0]	Data[0]								
[62:1]	Data[<DQErr>]								
[63]	Data[63]								

D18F2x298_dct[0] DRAM Status 5

Bits	Description
31:0	DQEErr[63:32]: DQ error. See: D18F2x294_dct[0][DQEErr[31:0]] .

D18F2x29C_dct[0] DRAM Status 6

IF (BootFromDRAM) THEN Cold reset: 0000_0000h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:20	Reserved.								
19:16	Reserved.								
15:8	Reserved.								
7:0	EccErr: ECC error. Read-only; S3-check-exclude. Indicates ECC error detection status on a per bit basis when D18F2x264_dct[0][ErrCnt] > 0. Status is accumulated until cleared by D18F2x250_dct[0][ResetAllErr] . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>ECC[0]</td> </tr> <tr> <td>[6:1]</td> <td>ECC[<EccErr>]</td> </tr> <tr> <td>[7]</td> <td>ECC[7]</td> </tr> </tbody> </table>	Bit	Description	[0]	ECC[0]	[6:1]	ECC[<EccErr>]	[7]	ECC[7]
Bit	Description								
[0]	ECC[0]								
[6:1]	ECC[<EccErr>]								
[7]	ECC[7]								

D18F2x2[B4,B0,AC,A8]_dct[0] DRAM User Data Pattern

IF (BootFromDRAM) THEN Cold reset: 5555_5555h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Table 169: Register Mapping for D18F2x2[B4,B0,AC,A8]_dct[0]

Register	Function
D18F2x2A8_dct[0]	Nibble Lanes 0, 4, 8, 12, 16
D18F2x2AC_dct[0]	Nibble Lanes 1, 5, 9, 13, 17
D18F2x2B0_dct[0]	Nibble Lanes 2, 6, 10, 14
D18F2x2B4_dct[0]	Nibble Lanes 3, 7, 11, 15

Table 170: Field Mapping for D18F2x2[B4,B0,AC,A8]_dct[0]

Register	Bits			
	31:24	23:16	15:8	7:0
D18F2x2A8_dct[0]	DQ3, DQ19, DQ35, DQ51, ECC3	DQ2, DQ18, DQ34, DQ50, ECC2	DQ1, DQ17, DQ33, DQ49, ECC1	DQ0, DQ16, DQ32, DQ48, ECC0
D18F2x2AC_dct[0]	DQ7, DQ23, DQ39, DQ55, ECC7	DQ6, DQ22, DQ38, DQ54, ECC6	DQ5, DQ21, DQ37, DQ53, ECC5	DQ4, DQ20, DQ36, DQ52, ECC4
D18F2x2B0_dct[0]	DQ11, DQ27, DQ43, DQ59	DQ10, DQ26, DQ42, DQ58	DQ9, DQ25, DQ41, DQ57	DQ8, DQ24, DQ40, DQ56
D18F2x2B4_dct[0]	DQ15, DQ31, DQ47, DQ63	DQ14, DQ30, DQ46, DQ62	DQ13, DQ29, DQ45, DQ61	DQ12, DQ28, DQ44, DQ60

Bits	Description								
31:24	DataPattern: data pattern. See: D18F2x2[B4,B0,AC,A8]_dct[0][7:0] .								
23:16	DataPattern: data pattern. See: D18F2x2[B4,B0,AC,A8]_dct[0][7:0] .								
15:8	DataPattern: data pattern. See: D18F2x2[B4,B0,AC,A8]_dct[0][7:0] .								
7:0	DataPattern: data pattern. Read-write; S3-check-exclude. Specifies a data pattern used for creating traffic on the data bus for the specified bit lanes. See D18F2x250_dct[0][DataPatGenSel] . <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Pattern Data Beat 0</td> </tr> <tr> <td>[6:1]</td> <td>Pattern Data Beat 1 to Pattern Data Beat 6</td> </tr> <tr> <td>[7]</td> <td>Pattern Data Beat 7</td> </tr> </tbody> </table>	Bit	Description	[0]	Pattern Data Beat 0	[6:1]	Pattern Data Beat 1 to Pattern Data Beat 6	[7]	Pattern Data Beat 7
Bit	Description								
[0]	Pattern Data Beat 0								
[6:1]	Pattern Data Beat 1 to Pattern Data Beat 6								
[7]	Pattern Data Beat 7								

D18F2x2B8_dct[0] DRAM Command 3

IF (BootFromDRAM) THEN Cold reset: 0000_0F00h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#). See [2.9.8 \[Continuous Pattern Generation\]](#).

Bits	Description								
31:16	ActPchgSeq: activate precharge sequence. Read-write; S3-check-exclude. Specifies the command that will be generated in the sequence, corresponding to the sixteen target entries in D18F2x2[C0,BC]_dct[0] . 1=Activate. 0=Precharge. <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>ACT/PRE [0]</td> </tr> <tr> <td>[14:1]</td> <td>ACT/PRE [<ActPchgSeq>]</td> </tr> <tr> <td>[15]</td> <td>ACT/PRE [15]</td> </tr> </tbody> </table>	Bit	Description	[0]	ACT/PRE [0]	[14:1]	ACT/PRE [<ActPchgSeq>]	[15]	ACT/PRE [15]
Bit	Description								
[0]	ACT/PRE [0]								
[14:1]	ACT/PRE [<ActPchgSeq>]								
[15]	ACT/PRE [15]								

15:12	Reserved.						
11:8	<p>ActPchgCmdMin: activate precharge command minimum. Read-write; S3-check-exclude. Specifies the minimum time in memory clock cycles from an activate or precharge command to the next activate or precharge command in the ActPchgSeq sequence.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Reserved</td> </tr> <tr> <td>Fh-1h</td> <td>[<ActPchgCmdMin>] clocks</td> </tr> </tbody> </table>	Bits	Description	0	Reserved	Fh-1h	[<ActPchgCmdMin>] clocks
Bits	Description						
0	Reserved						
Fh-1h	[<ActPchgCmdMin>] clocks						
7:0	Reserved.						

D18F2x2[C0,BC]_dct[0] DRAM Command 4 & 5

Reset: 0000_0000h. See 2.9.3 [DCT Configuration Registers]. See 2.9.8 [Continuous Pattern Generation].

Table 171: Field Mappings for D18F2x2[C0,BC]_dct[0]

Register	Bits							
	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
D18F2x2BC_dct[0]	ACT/PRE 7	ACT/PRE 6	ACT/PRE 5	ACT/PRE 4	ACT/PRE 3	ACT/PRE 2	ACT/PRE 1	ACT/PRE 0
D18F2x2C0_dct[0]	ACT/PRE 15	ACT/PRE 14	ACT/PRE 13	ACT/PRE 12	ACT/PRE 11	ACT/PRE 10	ACT/PRE 9	ACT/PRE 8

Bits	Description						
31:28	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
27:24	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
23:20	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
19:16	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
15:12	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
11:8	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
7:4	ActPchgTgtBank: activate precharge target bank. See: D18F2x2[C0,BC]_dct[0][3:0].						
3:0	<p>ActPchgTgtBank: activate precharge target bank. Read-write; S3-check-exclude. Specifies the bank address used for this command of the sequence.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>7h-0h</td> <td>Bank [<ActPchgTgtBank>]</td> </tr> <tr> <td>Fh-8h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	7h-0h	Bank [<ActPchgTgtBank>]	Fh-8h	Reserved
Bits	Description						
7h-0h	Bank [<ActPchgTgtBank>]						
Fh-8h	Reserved						

D18F2x2E0_dct[0] Memory P-state Control and Status

See 2.9.3 [DCT Configuration Registers].

Bits	Description
31	Reserved.

30	FastMstateDis: fast M-state change disable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. 1=The DCT changes MEMCLK frequency only after the NCLK frequency has changed. 0=The DCT changes MEMCLK frequency while the northbridge changes NCLK.								
29	Reserved.								
28:24	M1MemClkFreq: M1 memory clock frequency. Read-write. IF (BootFromDRAM) THEN Cold reset: 00h. ELSE Reset: 00h. ENDIF. Specifies the frequency of the DRAM interface (MEMCLK) for memory P-state 1. See Table 124 [Valid Values for Memory Clock Frequency Value Definition] . The hardware enforces D18F5x84[DdrMaxRateEnf] when writes to this field occur. See D18F5x84[DdrMaxRate] and D18F5x84[DdrMaxRateEnf] . Hardware does not generate a x0B write for this register. BIOS must also program D18F2x9C_x0D0F_E000_dct[0]_mp[1:0][Rate] for M1.								
23	Reserved. Reserved for MxMrs3En.								
22:20	MxMrsEn: Mx Mrs enable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0h. ELSE Reset: 0h. ENDIF. 1=The DCT writes to the DRAM MR after a memory P-state change. 0=The DCT does not write to the DRAM MR. <table border="0"> <tr> <th style="text-align: center;">Bit</th> <th style="text-align: center;">Description, MR value</th> </tr> <tr> <td style="text-align: center;">[0]</td> <td>MR0, D18F2x2E8_dct[0]_mp[1:0][MxMr0]</td> </tr> <tr> <td style="text-align: center;">[1]</td> <td>MR1, D18F2x2E8_dct[0]_mp[1:0][MxMr1]</td> </tr> <tr> <td style="text-align: center;">[2]</td> <td>MR2, D18F2x2EC_dct[0]_mp[1:0][MxMr2]</td> </tr> </table>	Bit	Description, MR value	[0]	MR0, D18F2x2E8_dct[0]_mp[1:0][MxMr0]	[1]	MR1, D18F2x2E8_dct[0]_mp[1:0][MxMr1]	[2]	MR2, D18F2x2EC_dct[0]_mp[1:0][MxMr2]
Bit	Description, MR value								
[0]	MR0, D18F2x2E8_dct[0]_mp[1:0][MxMr0]								
[1]	MR1, D18F2x2E8_dct[0]_mp[1:0][MxMr1]								
[2]	MR2, D18F2x2EC_dct[0]_mp[1:0][MxMr2]								
19:1	Reserved.								
0	CurMemPstate: current memory P-state. Reset: 0h. Read-only; updated-by-hardware. Specifies the current memory P-state. 0=M0. 1=M1.								

D18F2x2E8_dct[0]_mp[1:0] MRS Buffer

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:16	MxMr1: Mx MR1. Read-write. IF (BootFromDRAM) THEN Cold reset: 0000h. ELSE Reset: 0000h. ENDIF. Specifies the value written to DRAM MR1 after a memory P-state change. If the M1 value is the same as the M0 value, then BIOS should optimize P-state switching latency by programming D18F2x2E0_dct[0][MxMrsEn]=0 .
15:0	MxMr0: Mx MR0. Read-write. IF (BootFromDRAM) THEN Cold reset: 0000h. ELSE Reset: 0000h. ENDIF. Specifies the value written to DRAM MR0 after a memory P-state change. If the M1 value is the same as the M0 value, then BIOS should optimize P-state switching latency by programming D18F2x2E0_dct[0][MxMrsEn]=0 .

D18F2x2EC_dct[0]_mp[1:0] MRS Buffer

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:16	Reserved.
15:0	MxMr2: Mx MR2. Read-write. IF (BootFromDRAM) THEN Cold reset: 0000h. ELSE Reset: 0000h. ENDIF. Specifies the value written to DRAM MR2 after a memory P-state change. If the M1 value is the same as the M0 value, then BIOS should optimize P-state switching latency by programming D18F2x2E0_dct[0][MxMrsEn]=0 .

D18F2x2F0_dct[0]_mp[1:0] DRAM Controller Misc 3See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:1	Reserved.
0	EffArbDis: Efficient arbitration disable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 0. 0=The DCT optimizes the arbitration phases to improve performance (in addition to EarlyArbEn=1, this applies to non-page-hit DRAM commands) under certain traffic conditions whenever the NCLK to MEMCLK ratio is less than 2:1. The DCT arbitrates normally with other ratios. 1=The DCT arbitrates normally, requiring 3 NCLKs, at all NCLK:MEMCLK ratios. If the NCLK to MEMCLK ratio is less than 2:1, the DCT issues non-PH commands at most every other MEMCLK cycle.

D18F2x400_dct[0] GMC to DCT Control 0IF ([BootFromDRAM](#)) THEN Cold reset: 0000_0404h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

The GMC to DCT interface (GARLIC) controls how DRAM bus resources are allocated and arbitrated between the MCT and the GMC. A token is the unit of available resource and is equivalent to a DCQ entry. A minimum count ensures a number of available DCQ entries. A token limit for MCT or GMC ensures resources are not all allocated to the GMC, or MCT respectively. Limits are configured bimodal: for normal GMC traffic and for when urgent (nominally display refresh) GMC traffic is occurring.

Rule: [D18F2x400_dct\[0\]\[MctTokenLimit\]](#) + [D18F2x400_dct\[0\]\[GmcTokenLimit\]](#) <= 16.Rule: [D18F2x400_dct\[0\]\[GmcTokenLimit\]](#) >= 1.Rule: [D18F2x400_dct\[0\]\[MctTokenLimit\]](#) >= 1.Rule: [D18F2x404_dct\[0\]\[UrGmcTokenLimit\]](#) + [D18F2x404_dct\[0\]\[UrMctTokenLimit\]](#) <= 16.Rule: [D18F2x404_dct\[0\]\[UrGmcMinTokens\]](#) + [D18F2x404_dct\[0\]\[UrMctMinTokens\]](#) <= 16.Rule: [D18F2x400_dct\[0\]\[MctTokenLimit\]](#) == [D18F2x404_dct\[0\]\[UrMctTokenLimit\]](#).

Bits	Description				
31:16	Reserved.				
15:12	Reserved.				
11:8	GmcTokenLimit: GMC token limit. Read-write.BIOS: 4h. Limit of outstanding GMC tokens. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Fh-0h</td> <td><GmcTokenLimit> tokens</td> </tr> </tbody> </table>	Bits	Description	Fh-0h	<GmcTokenLimit> tokens
Bits	Description				
Fh-0h	<GmcTokenLimit> tokens				
7:4	Reserved.				
3:0	MctTokenLimit: MCT token limit. Read-write. BIOS: 4h. Limit of outstanding MCT tokens. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Fh-0h</td> <td><MctTokenLimit> tokens</td> </tr> </tbody> </table>	Bits	Description	Fh-0h	<MctTokenLimit> tokens
Bits	Description				
Fh-0h	<MctTokenLimit> tokens				

D18F2x404_dct[0] GMC to DCT Control 1IF ([BootFromDRAM](#)) THEN Cold reset: 0004_0004h. ELSE Reset: 0000_0000h. ENDIF. See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description						
31	UrgentTknDis: Urgent token disable. Read-write. BIOS: 0. 0=When urgent GMC traffic is requested (GarlicTokUrg), override the programmed values in D18F2x400_dct[0] and force the token scheme to heavily weight towards graphics by using the programmable token limits in D18F2x404_dct[0] . 1=Token scheme remains at the previously programmed non-urgent token limits in D18F2x400_dct[0] regardless of urgent GMC traffic.						
30:28	Reserved.						
27:24	UrGmcMinTokens: Display refresh GMC minimum tokens. Read-write. BIOS: 4. Urgent mode minimum number of tokens assigned to the GMC. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Fh-0h</td> <td><UrGmcMinTokens> tokens</td> </tr> </tbody> </table>	Bits	Description	Fh-0h	<UrGmcMinTokens> tokens		
Bits	Description						
Fh-0h	<UrGmcMinTokens> tokens						
23:21	Reserved.						
20:16	UrGmcTokenLimit: Display refresh GMC token limit. Read-write. BIOS: 04h. Urgent mode limit of outstanding GMC tokens. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>10h-0h</td> <td><UrGmcTokenLimit> tokens</td> </tr> <tr> <td>1Fh-11h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	10h-0h	<UrGmcTokenLimit> tokens	1Fh-11h	Reserved
Bits	Description						
10h-0h	<UrGmcTokenLimit> tokens						
1Fh-11h	Reserved						
15:12	Reserved.						
11:8	UrMctMinTokens: Display refresh MCT minimum tokens. Read-write. BIOS: 4. Urgent mode minimum number of tokens assigned to the MCT. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Fh-0h</td> <td><UrMctMinTokens> tokens</td> </tr> </tbody> </table>	Bits	Description	Fh-0h	<UrMctMinTokens> tokens		
Bits	Description						
Fh-0h	<UrMctMinTokens> tokens						
7:5	Reserved.						
4:0	UrMctTokenLimit: Display refresh MCT token limit. Read-write. BIOS: 04h. Urgent mode limit of outstanding MCT tokens. Rule: IF (!(D18F2x404_dct[0] [UrgentTknDis])) THEN D18F2x404_dct[0] [UrMctTokenLimit] <= D18F2x400_dct[0] [MctTokenLimit]. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>10h-0h</td> <td><UrMctTokenLimit> tokens</td> </tr> <tr> <td>1Fh-11h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	10h-0h	<UrMctTokenLimit> tokens	1Fh-11h	Reserved
Bits	Description						
10h-0h	<UrMctTokenLimit> tokens						
1Fh-11h	Reserved						

D18F2x408_dct[0] GMC to DCT Control 2

See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description						
28:24	CpuElevPrioPeriod: Cpu elevate priority period. Read-write. Reset: 0. BIOS: Ch. Specifies the hysteresis of how often a new MCT read can be elevated to high priority if no other MCT reads currently exist in the DCQ. If CpuElevPrioPeriod==0, MCT will continuously elevate the priority of a new lone MCT read to high. Reserved if CpuElevPrioDis==1. Since this field controls internal timing in the NCLK domain, external bus equivalence is approximate. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>hysteresis counter disabled</td> </tr> <tr> <td>1Fh-01h</td> <td><CpuElevPrioPeriod*32> MEMCLKs (*32 CmdOut, +/- NCLK)</td> </tr> </tbody> </table>	Bits	Description	00h	hysteresis counter disabled	1Fh-01h	<CpuElevPrioPeriod*32> MEMCLKs (*32 CmdOut, +/- NCLK)
Bits	Description						
00h	hysteresis counter disabled						
1Fh-01h	<CpuElevPrioPeriod*32> MEMCLKs (*32 CmdOut, +/- NCLK)						
23:3	Reserved.						

2	NonP0UrgentTknDis: non-P0 urgent token disable. Read-write. Reset: 0. BIOS: 0. 0=Switch from normal GMC traffic token scheme defined by D18F2x400_dct[0] to urgent GMC traffic token scheme defined by D18F2x404_dct[0] when all processors are not in software P0 state. 1=Use normal GMC traffic token scheme when all processors are not in software P0 state.
1	TokenAllocSelect: Token allocation select. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 0. 0=When both the MCT and GMC have less than their maximum outstanding tokens, tokens are allocated by alternating between each. 1= When both the MCT and GMC have less than their maximum outstanding tokens, tokens are allocated to whichever has less (DCQ entries + current outstanding).
0	CpuElevPrioDis: Cpu elevate priority disable. Read-write. IF (BootFromDRAM) THEN Cold reset: 0. ELSE Reset: 0. ENDIF. BIOS: 0. 1=Reads from MCT arbitrate with GMC traffic normally. 0=Elevate the priority of a new MCT read to high if no other MCT reads currently exist in the DCQ. This can alleviate CPU stalls during very long graphics requests.

D18F2x420_dct[0] GMC to DCT FIFO Config 1See [2.9.3 \[DCT Configuration Registers\]](#).

Bits	Description
31:12	Reserved.
7:4	Reserved.

3.12 Device 18h Function 3 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F3x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1533h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F3x04 Status/Command

Bits	Description
31:16	Status. Read-only. Reset: 0000h, except bit[20]. Bit[20] is set to indicate the existence of a PCI-defined capability block, if one exists.
15:0	Command. Read-only. Reset: 0000h.

D18F3x08 Class Code/Revision ID

Bits	Description
31:8	ClassCode. Read-only. Reset: 060000h. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only. Reset: 00h.

D18F3x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:0	HeaderTypeReg. Read-only. These bits are fixed at their default values. The header type field indicates that there are multiple functions present in this device.

D18F3x34 Capability Pointer

Bits	Description
31:8	Reserved.
7:0	CapPtr. Read-only. Value: 00h. DEV not implemented.

D18F3x40 MCA NB Control

Read-write. Reset: 0000_0000_0000_0000h. [MSR0000_0410](#)[31:0] is an alias of D18F3x40. See [MSR0000_0410](#)[31:0].

Bits	Description
63:32	Unused.
31	McaCpuDatErrEn: L2 complex data error. 1=Enables MCA reporting of CPU data errors sent to the NB.
29:28	Unused. Read-write.
27	Unused. Read-write.
26	NbArrayParEn: northbridge array parity error reporting enable. 1=Enables reporting of parity errors in the NB arrays.
25	UsPwDatErrEn: upstream data error enable. Read-write. 1=Enables MCA reporting of upstream posted writes in which the EP bit is set as indicated by the ONION error bits.
24:18	Unused. Read-write.
17	CpPktDatEn: completion packet error reporting enable. Read-write. 1=Enables MCA reporting of completion packets with the EP bit set. Any response packet with data errors detected by ONION will generate this error.
16	NbIntProtEn: northbridge internal bus (ONION) protocol error reporting enable. Read-write. 1=Enables MCA reporting of protocol errors detected on the northbridge internal bus (ONION). When possible, this enable should be cleared before initiating a warm reset to avoid logging spurious errors due to RESET_L signal skew.
15:13	Unused. Read-write.
12	WDTRptEn: watchdog timer error reporting enable. 1=Enables MCA reporting of watchdog timer errors. The watchdog timer checks for NB system accesses for which a response is expected but no response is received. See D18F3x44 [MCA NB Configuration] for information regarding configuration of the watchdog timer duration. This bit does not affect operation of the watchdog timer in terms of its ability to complete an access that would otherwise cause a system hang. This bit only affects whether such errors are reported through MCA.
11	AtomicRMWEn: atomic read-modify-write error reporting enable. 1=Enables MCA reporting of atomic read-modify-write (RMW) commands received from an IO link. Atomic RMW commands are not supported. An atomic RMW command results in a link error response being generated back to the requesting IO device. The generation of the link error response is not affected by this bit.
10	Unused. Read-write.
9	TgtAbortEn: target abort error reporting enable. 1=Enables MCA reporting of target aborts to a link. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of this bit.
8	MstrAbortEn: master abort error reporting enable. 1=Enables MCA reporting of master aborts to a link. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of this bit.
7:6	Unused. Read-write.
5	SyncPktEn: link sync packet error reporting enable. 1=Enables MCA reporting of link-defined sync error packets detected on link. The NB floods its outgoing link with sync packets after detecting a sync packet on the incoming link independent of the state of this bit.

4:2	Unused. Read-write.
1	UECCEn: uncorrectable ECC error reporting enable. 1=Enables MCA reporting of DDR3 DRAM uncorrectable ECC errors which are detected in the NB. In some cases data may be forwarded to the core prior to checking ECC in which case the check takes place in one of the other error reporting banks.
0	CECCEn: correctable ECC error reporting enable. 1=Enables MCA reporting of DDR3 DRAM correctable ECC errors which are detected in the NB.

D18F3x44 MCA NB Configuration

See [D18F3x180 \[Extended NB MCA Configuration\]](#). It is expected that all fields of this register are programmed to the same value in all nodes, except for the fields used for link error injection: GenLinkSel, GenSubLinkSel, GenCrcErrByte1, GenCrcErrByte0.

Bits	Description
31	NbMcaLogEn: northbridge MCA log enable. Read-write. Reset: 0. 1=Enables logging (but not reporting) of NB MCA errors even if MCA is not globally enabled.
30	SyncFloodOnDramAdrParErr: sync flood on DRAM address parity error. Read-write. Reset: 0. BIOS: 1. 1=Enable sync flood on detection of a DRAM address parity error.
29	DisMstAbortCpuErrRsp: master abort CPU error response disable. Read-write. Reset: 0. 1=Disables master abort reporting through the CPU MCA error-reporting banks; Suppresses sending of RDE to CPU; Does not log any MCA information in the NB.
28	DisTgtAbortCpuErrRsp: target abort CPU error response disable. Read-write. Reset: 0. 1=Disables target abort reporting through the CPU MCA error-reporting banks; Suppresses sending of RDE to CPU; Does not log any MCA information in the NB.
27	NbMcaToMstCpuEn: machine check errors to master CPU only. Read-write. Reset: 0. BIOS: 1. 1=NB MCA errors in CMP device are only reported to the node base core (NBC), and the NB MCA registers in MSR space (MSR0000_0410 , MSR0000_0411 , MSR0000_0412 , MSR0000_0413 , MSR0000_0408 , and MSRC001_0048) are only accessible from the NBC; reads of these MSRs from other cores return 0's and writes are ignored. This allows machine check handlers running on different cores to avoid coordinating accesses to the NB MCA registers. This field does not affect PCI-defined configuration space accesses to these registers, which are accessible from all cores. See 3.1 [Register Descriptions and Mnemonics] for a description of MSR space and 3 [Registers] for PCI-defined configuration space. 0=NB MCA errors may be reported to the core that originated the request, if applicable and known, and the NB MCA registers in MSR space are accessible from any core. Note: <ul style="list-style-type: none">• When the CPU which originated the request is known, it is stored in MSR0000_0411[ErrCoreId], regardless of the setting of NbMcaToMstCpuEn. See Table 206 for errors where ErrCoreId is known.• If IO originated the request, then the error is reported to the NBC, regardless of the setting of NbMcaToMstCpuEn.
26	FlagMcaCorrErr: correctable error MCA exception enable. Read-write. Reset: 0. 1=Raise a machine check exception for correctable and deferred machine check errors which are enabled in D18F3x40 .

25	DisPciCfgCpuErrRsp: PCI configuration CPU error response disable. Read-write. Reset: 0. 1=Disables generation of an error response to the core on detection of a master abort, target abort, or data error condition, and disables logging and reporting through the MCA error-reporting banks for PCI configuration accesses. For NB WDT errors on PCI configuration accesses, this prevents sending an error response to the core, but does not affect logging and reporting of the NB WDT error. See D18F3x180[DisPciCfgCpuMstAbortRsp] , which applies only to master aborts.										
24	IoRdDatErrEn: IO read data error log enable. Read-write. Reset: 0. 1=Enables MCA logging and reporting of errors on transactions from IO devices upon detection of a target abort, master abort, or data error condition. 0=Errors on transactions from IO devices are not logged in MCA, although error responses to the requesting IO device may still be generated. Errors include the following for requests sourced from IO: <ul style="list-style-type: none">• Target abort, master abort, or data error• P2P compatibility space error (either request or response)• Extended addressing error										
23	ChipKillEccCap: chip-kill ECC mode. Read-only; updated-by-hardware. Reset: 0. 1=Chipkill ECC mode capable; ECC checking is based on x8 ECC symbols (D18F3x180[EccSymbolSize]) and can be used for chipkill. 0=Chipkill ECC mode not capable; ECC checking is based on two interleaved, unganged 64/8-bit data/ECC lines and x4 ECC symbols and cannot be used for chipkill. See 2.14.2 [DRAM ECC Considerations] .										
22	DramEccEn: DRAM ECC enable. Read-write. Reset: 0. 1=Enables ECC check/correct mode. This bit must be set in order for ECC checking/correcting by the NB to be enabled. If set, ECC is checked and correctable errors are corrected irrespective of whether machine check ECC reporting is enabled. The hardware only allows values to be programmed into this field which are consistent with the ECC capabilities of the device as specified in D18F3xE8 [Northbridge Capabilities] . Attempts to write values inconsistent with the capabilities results in this field not being updated. This bit does not affect ECC checking in the northbridge arrays.										
21	SyncFloodOnAnyUcErr: sync flood on any UC error. Read-write. Reset: 0. BIOS: 1. 1=Enable sync flood of all links with sync packets on detection of any NB MCA error that is uncorrectable, including northbridge array errors and link protocol errors.										
20	SyncFloodOnWDT: sync flood on watchdog timer error. Read-write. Reset: 0. BIOS: 1. 1=Enable sync flood of all links with sync packets on detection of a watchdog timer error. See D18F3x18C[Dis-SrqReqCompOnWDT] .										
19:18	GenSubLinkSel: sublink select for CRC error generation. Read-write. Reset: 0. Selects the sub-link of a link selected by GenLinkSel to be used for CRC error injection through GenCrcErrByte0 and GenCrcErrByte1. When the link is ganged, GenSubLinkSel must be 00b. When the link is unganged, the following values indicate which sublink is selected: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th style="text-align: center;">Bits</th> <th style="text-align: center;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Sublink 0</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>Sublink 1</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>Reserved</td> </tr> <tr> <td style="text-align: center;">11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	Sublink 0	01b	Sublink 1	10b	Reserved	11b	Reserved
Bits	Description										
00b	Sublink 0										
01b	Sublink 1										
10b	Reserved										
11b	Reserved										

17	GenCrcErrByte1: generate CRC error on byte lane 1. Read-Write. Reset: 0. 1=For ganged links (see GenSubLinkSel), a CRC error is injected on byte lane 1 of the link specified by GenLinkSel. For ganged links in retry mode or unganged links, this field is reserved, and GenCrcErrByte0 must be used. The data carried by the link is unaffected. This bit is cleared after the error has been generated. For ganged links in retry mode, GenCrcErrByte1 has no effect; only GenCrcErrByte0 may be used.																								
16	GenCrcErrByte0: generate CRC error on byte lane 0. Read-Write. Reset: 0. 1=Causes a CRC error to be injected on byte lane 0 of the link specified by GenLinkSel and the sublink specified by GenSubLinkSel. The data carried by the link is unaffected. This bit is cleared after the error has been generated. For ganged links in retry mode, GenCrcErrByte1 has no effect; only GenCrcErrByte0 may be used.																								
15:14	GenLinkSel: link select for CRC error generation. Read-Write. Reset: 00b. Selects the link to be used for CRC error injection through GenCrcErrByte1/GenCrcErrByte0. <table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>link 0</td></tr> <tr> <td>01b</td><td>link 1</td></tr> <tr> <td>10b</td><td>link 2</td></tr> <tr> <td>11b</td><td>link 3</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	link 0	01b	link 1	10b	link 2	11b	link 3														
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00b	link 0																								
01b	link 1																								
10b	link 2																								
11b	link 3																								
13:12	WDTBaseSel: watchdog timer time base select. Read-write. Reset: 0. Selects the time base used by the watchdog timer. The counter selected by WDTCntSel determines the maximum count value in the time base selected by WDTBaseSel. <table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>1.31 ms</td></tr> <tr> <td>01b</td><td>1.28 us</td></tr> <tr> <td>10b</td><td>Reserved.</td></tr> <tr> <td>11b</td><td>Reserved. (WDT disabled)</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	1.31 ms	01b	1.28 us	10b	Reserved.	11b	Reserved. (WDT disabled)														
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00b	1.31 ms																								
01b	1.28 us																								
10b	Reserved.																								
11b	Reserved. (WDT disabled)																								
11:9	WDTCntSel[2:0]: watchdog timer count select bits[2:0]. Read-write. Reset: 0. Selects the count used by the watchdog timer. WDTCntSel = {D18F3x180[WDTCntSel[3]], D18F3x44[WDTCntSel[2:0]]}. The counter selected by WDTCntSel determines the maximum count value in the time base selected by WDTBaseSel. WDTCntSel is encoded as: <table> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>0000b</td><td>4095</td></tr> <tr> <td>0001b</td><td>2047</td></tr> <tr> <td>0010b</td><td>1023</td></tr> <tr> <td>0011b</td><td>511</td></tr> <tr> <td>0100b</td><td>255</td></tr> <tr> <td>0101b</td><td>127</td></tr> <tr> <td>0110b</td><td>63</td></tr> <tr> <td>0111b</td><td>31</td></tr> <tr> <td>1000b</td><td>8191</td></tr> <tr> <td>1001b</td><td>16383</td></tr> <tr> <td>1111b-1010b</td><td>Reserved</td></tr> </tbody> </table> Because WDTCntSel is split between two registers, care must be taken when programming WDTCntSel to ensure that a reserved value is never used by the watchdog timer or undefined behavior could result.	<u>Bits</u>	<u>Description</u>	0000b	4095	0001b	2047	0010b	1023	0011b	511	0100b	255	0101b	127	0110b	63	0111b	31	1000b	8191	1001b	16383	1111b-1010b	Reserved
<u>Bits</u>	<u>Description</u>																								
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0110b	63																								
0111b	31																								
1000b	8191																								
1001b	16383																								
1111b-1010b	Reserved																								
8	WDTDis: watchdog timer disable. Read-write. Cold reset: 0. 1=Disables the watchdog timer. The watchdog timer is enabled by default and checks for NB system accesses for which a response is expected and where no response is received. If such a condition is detected the outstanding access is completed by generating an error response back to the requestor. An MCA error may also be generated if enabled in D18F3x40 [MCA NB Control] .																								

7	IoErrDis: IO error response disable. Read-write. Reset: 0. 1=Disables setting either Error bit in link response packets to IO devices on detection of a target or master abort error condition.
6	CpuErrDis: CPU error response disable. Read-write. Reset: 0. BIOS: 1. 1=Disables generation of a read data error response to the core on detection of a target or master abort error condition.
5	IoMstAbortDis: IO master abort error response disable. Read-write. Reset: 0. 1=Signals target abort instead of master abort in link response packets to IO devices on detection of a master abort error condition. When IoMstAbortDis and D18F3x180[ChgMstAbortToNoErr] are both set, D18F3x180[ChgMstAbortToNoErr] takes precedence.
4	SyncPktPropDis: sync packet propagation disable. Read-write. Reset: 0. BIOS: 0. 1=Disables flooding of all outgoing links with sync packets when a sync packet is detected on an incoming link. Sync packets are propagated by default.
3	SyncPktGenDis: sync packet generation disable. Read-write. Reset: 0. BIOS: 0. 1=Disables flooding of all outgoing links with sync packets when a CRC error is detected on an incoming link. By default, sync packet generation for CRC errors is controlled through D18F0x[E4,C4,A4,84] [Link Control] .
2	SyncFloodOnDramUcEcc: sync flood on uncorrectable DRAM ECC error. Read-write. Reset: 0. BIOS: 1. 1=Enable sync flood of all links with sync packets on detection of an uncorrectable DRAM ECC error.
1	CpuRdDatErrEn: CPU read data error log enable. Read-write. Reset: 0. 1=Enables reporting of read data errors (master aborts and target aborts) for data destined for the CPU on this node. This bit should be clear if read data error logging is enabled for the remaining error reporting blocks in the CPU. Logging the same error in more than one block may cause a single error event to be treated as a multiple error event and cause the CPU to enter shutdown.
0	Reserved.

D18F3x48 MCA NB Status Low

Bits	Description
31:0	MSR0000_0411 [31:0] is an alias of D18F3x48. See MSR0000_0411 .

D18F3x4C MCA NB Status High

Bits	Description
31:0	MSR0000_0411 [63:32] is an alias of D18F3x4C. See MSR0000_0411 .

D18F3x50 MCA NB Address Low

Bits	Description
31:0	MSR0000_0412 [31:0] is an alias of D18F3x50. See MSR0000_0412 [31:0].

D18F3x54 MCA NB Address High

Bits	Description
31:0	MSR0000_0412[63:32] is an alias of D18F3x54 . See MSR0000_0412[63:32] .

D18F3x58 Scrub Rate Control

This register specifies the ECC sequential scrubbing rate for lines of memory and cache. See [2.8.3 \[Memory Scrubbers\]](#). Scrub rates are a platform consideration. See [2.14.1.8 \[Scrub Rate Considerations\]](#).

Bits	Description																																																																				
31:29	Reserved.																																																																				
28:24	Reserved. Read-write.																																																																				
23:5	Reserved.																																																																				
4:0	DramScrub: DRAM scrub rate. Specifies time between 64 B scrub events. See D18F3x5C and D18F3x60 . <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Disable sequential scrubbing</td> <td>10h</td> <td>1.31 ms</td> </tr> <tr> <td>01h</td> <td>40 ns¹</td> <td>11h</td> <td>2.62 ms</td> </tr> <tr> <td>02h</td> <td>80 ns¹</td> <td>12h</td> <td>5.24 ms</td> </tr> <tr> <td>03h</td> <td>160 ns¹</td> <td>13h</td> <td>10.49 ms</td> </tr> <tr> <td>04h</td> <td>320 ns¹</td> <td>14h</td> <td>20.97 ms</td> </tr> <tr> <td>05h</td> <td>640 ns</td> <td>15h</td> <td>42 ms</td> </tr> <tr> <td>06h</td> <td>1.28 us</td> <td>16h</td> <td>84 ms</td> </tr> <tr> <td>07h</td> <td>2.56 us</td> <td>1Eh-17h</td> <td>Reserved</td> </tr> <tr> <td>08h</td> <td>5.12 us</td> <td>1Fh</td> <td>20 ns</td> </tr> <tr> <td>09h</td> <td>10.2 us</td> <td></td> <td></td> </tr> <tr> <td>0Ah</td> <td>20.5 us</td> <td></td> <td></td> </tr> <tr> <td>0Bh</td> <td>41.0 us</td> <td></td> <td></td> </tr> <tr> <td>0Ch</td> <td>81.9 us</td> <td></td> <td></td> </tr> <tr> <td>0Dh</td> <td>163.8 us</td> <td></td> <td></td> </tr> <tr> <td>0Eh</td> <td>327.7 us</td> <td></td> <td></td> </tr> <tr> <td>0Fh</td> <td>655.4 us</td> <td></td> <td></td> </tr> </tbody> </table> Note: 1. This setting is not supported (and is not verified) except as a DRAM scrub rate when no other memory accesses are being performed.	Bits	Description	Bits	Description	00h	Disable sequential scrubbing	10h	1.31 ms	01h	40 ns ¹	11h	2.62 ms	02h	80 ns ¹	12h	5.24 ms	03h	160 ns ¹	13h	10.49 ms	04h	320 ns ¹	14h	20.97 ms	05h	640 ns	15h	42 ms	06h	1.28 us	16h	84 ms	07h	2.56 us	1Eh-17h	Reserved	08h	5.12 us	1Fh	20 ns	09h	10.2 us			0Ah	20.5 us			0Bh	41.0 us			0Ch	81.9 us			0Dh	163.8 us			0Eh	327.7 us			0Fh	655.4 us		
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D18F3x5C DRAM Scrub Address Low

In addition to sequential DRAM scrubbing, the DRAM scrubber has a redirect mode for scrubbing DRAM locations accessed during normal operation. This is enabled by setting [D18F3x5C\[ScrubReDirEn\]](#). When a DRAM read is generated by any agent other than the DRAM scrubber, correctable ECC errors are corrected as the data is passed to the requestor, but the data in DRAM is not corrected if redirect scrubbing mode is disabled. In scrubber redirect mode, correctable errors detected during normal DRAM read accesses redirect the scrubber to the location of the error. After the scrubber corrects the location in DRAM, it resumes scrubbing from where it left off. DRAM scrub address registers are not modified by the redirect scrubbing

mode. Sequential scrubbing and scrubber redirection can be enabled independently or together. ECC errors detected by the scrubber are logged in the MCA registers (See [D18F3x40 \[MCA NB Control\]](#)).

Bits	Description
31:6	ScrubAddr[31:6]: DRAM scrubber address bits[31:6]. Read-write; updated-by-hardware. ScrubAddr[47:6] = { D18F3x60 [ScrubAddr[47:32]], ScrubAddr[31:6]}. Reset: 0. ScrubAddr points to a DRAM cacheline in physical address space. BIOS should initialize the scrubber address register to the base address of the node specified by D18F1x[17C:140,7C:40] [DRAM Base/Limit] prior to enabling sequential scrubbing through D18F3x58 [DramScrub]. When sequential scrubbing is enabled: it starts at the address that the scrubber address registers are initialized to; it increments through address space and updates the scrubber address registers as it does so; when the scrubber reaches the DRAM limit address specified by D18F1x[17C:140,7C:40] , it wraps around to the base address. Reads of the scrubber address registers provide the next cacheline to be scrubbed.
5:1	Reserved.
0	ScrubReDirEn: DRAM scrubber redirect enable. Read-write. Reset: 0. BIOS: See Table 47 [DCT Training Specific Register Values] . If a correctable error is discovered from a non-scrubber DRAM read, then the data is corrected before it is returned to the requestor; however, the DRAM location may be left in a corrupted state (until the next time the scrubber address counts up to that location, if sequential scrubbing is enabled through D18F3x58 [DramScrub]). 1=Enables the scrubber to immediately scrub any address in which a correctable error is discovered. This bit and sequential scrubbing can be enabled independently or together; if both are enabled, the scrubber jumps from the scrubber address to where the correctable error was discovered, scrubs that location, and then jumps back to where it left off; the scrubber address register is not affected during scrubber redirection.

D18F3x60 DRAM Scrub Address High

Bits	Description
31:16	Reserved.
15:0	ScrubAddr[47:32]: DRAM scrubber address bits[47:32]. See: D18F3x5C [ScrubAddr[31:6]]. Reset: 0.

D18F3x64 Hardware Thermal Control (HTC)

See [2.10.3.1 \[PROCHOT_L and Hardware Thermal Control \(HTC\)\]](#). If Fuse[HtcMsrLock]=1, then HtcPstateLimit, HtcHystLmt, HtcTmpLmt, HtcClkInact, HtcClkAct, HtcPstateSel, and HtcEn fields are reserved. [MSRC001_003E](#) is an alias of [D18F3x64](#). If [D18F3xE8](#)[HtcCapable]=0 then this register is reserved.

Bits	Description
31	Reserved.
30:28	HtcPstateLimit: HTC P-state limit select. IF (~Fuse[HtcMsrLock]) THEN Read-write. ELSE Read-only. ENDIF. Reset: Fuse[HtcStcPstateLimit]. Specifies the P-state limit of all cores when in the P-state based HTC-active state. This field uses hardware P-state numbering and is not changed on a write if the value written is greater than D18F3xDC [HwPstateMaxVal] or less than D18F4x15C [NumBoostStates]. See 2.10.3.1 [PROCHOT_L and Hardware Thermal Control (HTC)] and 2.5.3.1.1.2 [Hardware P-state Numbering] .

27:24	HtcHystLmt: HTC hysteresis. IF (~Fuse[HtcMsrLock]) THEN Read-write. ELSE Read-only. ENDIF. Reset: Fuse[HtcHystLmt[3:0]]. The processor exits the HTC-active state when (Tctl or Tctlm < (HtcTmpLmt - HtcHystLmt). Modifying HtcHystLmt via BIOS should be done early in POST.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0h</td> <td style="text-align: center;">0</td> </tr> <tr> <td style="text-align: center;">1h</td> <td style="text-align: center;">0.5</td> </tr> <tr> <td style="text-align: center;">Eh-2h</td> <td style="text-align: center;"><HtcHystLmt*0.5></td> </tr> <tr> <td style="text-align: center;">Fh</td> <td style="text-align: center;">7.5</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	0	1h	0.5	Eh-2h	<HtcHystLmt*0.5>	Fh	7.5
<u>Bits</u>	<u>Description</u>										
0h	0										
1h	0.5										
Eh-2h	<HtcHystLmt*0.5>										
Fh	7.5										
23	HtcSlewSel: HTC slew-controlled temperature select. Read-write. Reset: 0. 1=HTC logic is driven by the slew-controlled temperature, Tctl, specified in D18F3xA4 [Reported Temperature Control] . 0=HTC logic is driven by the measured control temperature, Tctlm, with no slew controls.										
22:16	HtcTmpLmt: HTC temperature limit. IF (~Fuse[HtcMsrLock]) THEN Read-write. ELSE Read-only. ENDIF. Reset: Fuse[HtcTmpLmt[6:0]]. The processor enters the HTC-active state when Tctl or Tctlm reaches or exceeds the temperature limit defined by this register. Modifying HtcTmpLmt via BIOS should be done early in POST. Increasing above the default value is not supported.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00h</td> <td style="text-align: center;">52</td> </tr> <tr> <td style="text-align: center;">01h</td> <td style="text-align: center;">52.5</td> </tr> <tr> <td style="text-align: center;">7Eh-02h</td> <td style="text-align: center;"><(HtcTmpLmt*0.5) + 52></td> </tr> <tr> <td style="text-align: center;">7Fh</td> <td style="text-align: center;">115.5</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00h	52	01h	52.5	7Eh-02h	<(HtcTmpLmt*0.5) + 52>	7Fh	115.5
<u>Bits</u>	<u>Description</u>										
00h	52										
01h	52.5										
7Eh-02h	<(HtcTmpLmt*0.5) + 52>										
7Fh	115.5										
7	PslApicLoEn: P-state limit lower value change APIC interrupt enable. Read-write. Reset: 0. PslApicLoEn and PslApicHiEn enable interrupts using APIC330 [LVT Thermal Sensor] of each core when the active P-state limit in MSRC001_0061 [CurPstateLimit] changes. PslApicLoEn enables the interrupt when the limit value becomes lower (indicating higher performance). PslApicHiEn enables the interrupt when the limit value becomes higher (indicating lower performance). 1=Enable interrupt. See D18F5x88 [EnAllPstateLimitEnterIntr, EnAllPstateLimitExitIntr].										
6	PslApicHiEn: P-state limit higher value change APIC interrupt enable. Read-write. Reset: 0. See PslApicLoEn.										
5	HtcActSts: HTC-active status. Read; set-by-hardware; write-1-to-clear. Reset: 0. This bit is set by hardware when the processor enters the HTC-active state. It is cleared by writing a 1 to it.										
4	HtcAct: HTC-active state. Read-only, updated-by-hardware. Reset: X. (Can be asserted out of reset when Fuse[HtcMsrLock]=1 and the processor immediately goes into the HTC-active state). 1=The processor is currently in the HTC-active state. 0=The processor is not in the HTC-active state.										
0	HtcEn: HTC enable. IF (~Fuse[HtcMsrLock]) THEN Read-write. ELSE Read-only. ENDIF. Reset: Fuse[HtcMsrLock]. BIOS: IF (D18F3x64 [HtcTmpLmt]==0) THEN 0 ELSE 1 ENDIF. 1=HTC is enabled; the processor is capable of entering the HTC-active state.										

D18F3x68 Software P-state Limit

See [2.10.3.3 \[Software P-state Limit Control\]](#). [MSRC001_003F](#) is an alias of [D18F3x68](#). If [D18F3xE8](#)[HtcCapable]=0 then this register is reserved.

Bits	Description
31	Reserved.
30:28	SwPstateLimit: software P-state limit select. Read-write. Reset: Fuse[HtcStcPstateLimit]. Specifies a P-state limit for all cores. Uses hardware P-state numbering; see 2.5.3.1.1.2 [Hardware P-state Numbering] . Not changed on a write if the value written is greater than D18F3xDC [HwPstateMaxVal] or less than D18F4x15C [NumBoostStates]. See SwPstateLimitEn.

27:6	Reserved. Read-write.
5	SwPstateLimitEn: software P-state limit enable. Read-write. Reset: 0. 1=SwPstateLimit is enabled.
4:0	Reserved. Read-write.

D18F3x6C Data Buffer Count

Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

- To ensure deadlock free operation the following minimum buffer allocations are required:
 - Rule: [D18F3x6C\[UpRspDBC\]](#) ≥ 1 .
 - Rule: [D18F3x6C\[DnReqDBC\]](#) ≥ 1 .
 - Rule: [D18F3x6C\[UpReqDBC\]](#) ≥ 1 .
 - Rule: [D18F3x6C\[DnRspDBC\]](#) ≥ 1 .
- If [D18F0x\[E4,C4,A4,84\]\[IsocEn\]](#)=1: [IsocRspDBC](#) ≥ 1 .
- The total number of data buffers allocated in this register and [D18F3x7C](#) must satisfy the following equation:
 - Rule: [D18F3x6C\[UpReqDBC\]](#) + [D18F3x6C\[UpRspDBC\]](#) + [D18F3x6C\[DnReqDBC\]](#) + [D18F3x6C\[DnRspDBC\]](#) + [D18F3x6C\[IsocRspDBC\]](#) + (IF ([D18F3x7C\[Sri2XbarFreeRspDBC\]](#)==0) THEN ([D18F3x7C\[Sri2XbarFreeXreqDBC\]](#)*2) ELSE [D18F3x7C\[Sri2XbarFreeXreqDBC\]](#) ENDIF) + [D18F3x7C\[Sri2XbarFreeRspDBC\]](#) ≤ 16 .

Bits	Description
31	Reserved.
30:28	IsocRspDBC: isochronous response data buffer count. Read-write. Reset: 3. BIOS: 1.
27:19	Reserved.
18:16	UpRspDBC: upstream response data buffer count. Read-write. Reset: 2. BIOS: 1.
15	Reserved. Read-write.
14:8	Reserved.
7:6	DnRspDBC: downstream response data buffer count. Read-write. Reset: 2. BIOS: 1.
5:4	DnReqDBC: downstream request data buffer count. Read-write. Reset: 1. BIOS: 1.
3	Reserved.
2:0	UpReqDBC: upstream request data buffer count. Read-write. Reset: 2. BIOS: 2.

D18F3x70 SRI to XBAR Command Buffer Count

Reset: 1111_2153h. Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

- To ensure deadlock free operation the following minimum buffer allocations are required:
 - Rule: [D18F3x70\[UpRspCBC\]](#) ≥ 1 .
 - Rule: [D18F3x70\[UpPreqCBC\]](#) ≥ 1 .
 - Rule: [D18F3x70\[DnPreqCBC\]](#) ≥ 1 .
 - Rule: [D18F3x70\[UpReqCBC\]](#) ≥ 1 .

- Rule: [D18F3x70\[DnReqCBC\]](#) >= 1.
- Rule: [D18F3x70\[DnRspCBC\]](#) >= 1.
- If any of the [D18F0x\[E4,C4,A4,84\]](#)[IsocEn] bits are set:
IsocReqCBC >= 1 IsocRspCBC >= 1
- If [D18F0x\[E4,C4,A4,84\]](#)[IsocEn]=1 and isochronous posted requests may be generated by the system:
IsocPreqCBC >= 1
- The total number of SRI to XBAR commandbuffers allocated in this register and [D18F3x7C](#) must satisfy the following equation:
 - Rule: [D18F3x70\[IsocRspCBC\]](#) + [D18F3x70\[IsocPreqCBC\]](#) + [D18F3x70\[IsocReqCBC\]](#) + [D18F3x70\[UpRspCBC\]](#) + [D18F3x70\[DnPreqCBC\]](#) + [D18F3x70\[UpPreqCBC\]](#) + [D18F3x70\[DnReqCBC\]](#) + [D18F3x70\[DnRspCBC\]](#) + [D18F3x70\[UpReqCBC\]](#) + [D18F3x7C\[Sri2XbarFreeRspCBC\]](#) + [D18F3x7C\[Sri2XbarFreeXreqCBC\]](#) <= 24.

Bits	Description
31	Reserved.
30:28	IsocRspCBC: isoc response command buffer count. Read-write. BIOS: 1.
27	Reserved.
26:24	IsocPreqCBC: isoc posted request command buffer count. Read-write. BIOS: 0.
23	Reserved.
22:20	IsocReqCBC: isoc request command buffer count. Read-write. BIOS: 1.
19	Reserved.
18:16	UpRspCBC: upstream response command buffer count. Read-write. BIOS: 3.
15	Reserved.
14:12	DnPreqCBC: downstream posted request command buffer count. Read-write. BIOS: 1.
11	Reserved.
10:8	UpPreqCBC: upstream posted request command buffer count. Read-write. BIOS: 1.
7:6	DnRspCBC: downstream response command buffer count. Read-write. BIOS: 1.
5:4	DnReqCBC: downstream request command buffer count. Read-write. BIOS: 1.
3	Reserved.
2:0	UpReqCBC: upstream request command buffer count. Read-write. BIOS: 3

D18F3x74 XBAR to SRI Command Buffer Count

Reset: 0007_1111h. Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

Table 172: Buffer Definitions

Term	Definition
SpqSize	Probe command queue size. SpqSize = 20.
SrqSize	SRQ (XBAR command and probe response to SRI) queue size. SrqSize = 36.
PrbRsp	SRQ entries hard allocated to probe responses. PrbRsp = 4.
MpbcSize	MPB command buffer size. MpbcSize = 24.
McqSize	MCT command queue size. McqSize = 36.

- To ensure deadlock free operation the following minimum buffer allocations are required:
 - Rule: [D18F3x74\[ProbeCBC\]](#) ≥ 2 .
 - Rule: [D18F3x74\[UpReqCBC\]](#) ≥ 1 .
 - Rule: [D18F3x74\[UpPreqCBC\]](#) ≥ 1 .
 - $(IsocReqCBC + IsocPreqCBC + DRReqCBC) \leq 31$.
 - $(IsocReqCBC + IsocPreqCBC + DRReqCBC) \leq (McqSize - 16)$.
- If any of [D18F0x\[E4,C4,A4,84\]\[IsocEn\]](#) bits are set, then $IsocReqCBC \geq 1$.
- If any of the [D18F0x\[E4,C4,A4,84\]\[IsocEn\]](#) bits are set and isochronous posted requests may be generated by the system:
 $IsocPreqCBC \geq 1$
- The total number of XBAR to SRI commandbuffers allocated in this register and [D18F3x7C](#) must satisfy the following equation:
 - Rule: [D18F3x74\[UpReqCBC\] + D18F3x74\[UpPreqCBC\] + D18F3x74\[DnReqCBC\] + D18F3x74\[DnPreqCBC\] + D18F3x74\[IsocReqCBC\] + D18F3x74\[IsocPreqCBC\] + D18F3x74\[DRReqCBC\] + D18F3x7C\[Xbar2SriFreeListCBC\] + \(D18F3x1A0\[CpuCmdBufCnt\] * NumOfCompUnitsOnNode\] + D18F3x1A0\[CpuToNbFreeBufCnt\] + PrbRsp \leq SrqSize](#)
- The total number of SPQ (probe command) buffers allocated must satisfy the following equation:
 - Rule: [\(D18F3x17C\[SPQPrbFreeCBC\] + D18F3x74\[ProbeCBC\]\) \leq SpqSize](#).

Bits	Description
31:28	DRReqCBC: display refresh request command buffer count. Read-write. BIOS: 0.
27	Reserved.
26:24	IsocPreqCBC: isochronous posted request command buffer count. Read-write. BIOS: 1.
23:20	IsocReqCBC: isochronous request command buffer count. Read-write. BIOS: 1.

19:16	ProbeCBC: probe command buffer count. Read-write. BIOS: Ch.								
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>0 buffers</td></tr> <tr> <td>Ch-1h</td><td><ProbeCBC> buffers</td></tr> <tr> <td>Fh-Dh</td><td>Reserved.</td></tr> </tbody> </table>	Bits	Description	0h	0 buffers	Ch-1h	<ProbeCBC> buffers	Fh-Dh	Reserved.
Bits	Description								
0h	0 buffers								
Ch-1h	<ProbeCBC> buffers								
Fh-Dh	Reserved.								
15	Reserved.								
14:12	DnPreqCBC: downstream posted request command buffer count. Read-write. BIOS: 0.								
11	Reserved.								
10:8	UpPreqCBC: upstream posted request command buffer count. Read-write. BIOS: 1.								
7	Reserved.								
6:4	DnReqCBC: downstream request command buffer count. Read-write. BIOS: 0.								
3	Reserved.								
2:0	UpReqCBC: upstream request command buffer count. Read-write. BIOS: 1.								

D18F3x78 MCT to XBAR Buffer Count

Reset: 0024_0519h. Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

- To ensure deadlock free operation the following minimum buffer allocations are required:

$$\begin{array}{lll} \text{ProbeCBC} \geq 1 & \text{RspCBC} \geq 1 & \text{RspDBC} \geq 2 \\ \text{RspDBC} \geq \text{D18F2x11C[MctPrefReqLimit]} + 2 \end{array}$$

- The total number of command buffers allocated in this register must satisfy the following equation:

Rule: ([D18F3x78\[ProbeCBC\]](#) + [D18F3x78\[RspCBC\]](#)) \leq [MpbcSize](#).

Bits	Description												
31:22	Reserved.												
21:16	RspDBC: response data buffer count. Read-write.												
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>01h-00h</td><td>Reserved</td></tr> <tr> <td>02h</td><td>2 Buffers</td></tr> <tr> <td>1Fh-03h</td><td><RspDBC> Buffers</td></tr> <tr> <td>20h</td><td>32 Buffers</td></tr> <tr> <td>3Fh-21h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	01h-00h	Reserved	02h	2 Buffers	1Fh-03h	<RspDBC> Buffers	20h	32 Buffers	3Fh-21h	Reserved
Bits	Description												
01h-00h	Reserved												
02h	2 Buffers												
1Fh-03h	<RspDBC> Buffers												
20h	32 Buffers												
3Fh-21h	Reserved												

15:13	Reserved.
12:8	ProbeCBC: probe command buffer count. Read-write. BIOS: 8h.
7:6	Reserved.
5:0	RspCBC: response command buffer count. Read-write. BIOS: 10h.

D18F3x7C Free List Buffer Count

Reset: 0003_660Ch. Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values. See [D18F3x6C](#) and [D18F3x70](#).

- To ensure deadlock free operation the following minimum buffer allocations are required:
 - Rule: IF ([D18F3x7C\[Sri2XbarFreeRspCBC\]==0](#)) THEN ([D18F3x7C\[Sri2XbarFreeXreqCBC\]>2](#)).
 - Rule: IF ([D18F3x7C\[Sri2XbarFreeRspCBC\]!=0](#)) THEN ([D18F3x7C\[Sri2XbarFreeRspCBC\]>2](#)).
 - Rule: IF ([D18F3x7C\[Sri2XbarFreeRspDBC\]==0](#)) THEN ([D18F3x7C\[Sri2XbarFreeXreqDBC\]>2](#)).
 - Rule: IF ([D18F3x7C\[Sri2XbarFreeRspDBC\]!=0](#)) THEN ([D18F3x7C\[Sri2XbarFreeRspDBC\]>2](#)).
 - Rule: [D18F3x7C\[Xbar2SriFreeListCBC\] >= \(D18F3x1A0\[CpuToNbFreeBufCnt\] * NumOfCompUnitsOnNode\) + 2](#).

Bits	Description
31	Reserved.
30:28	Xbar2SriFreeListCBInc: XBAR to SRI free list command buffer increment. Read-write. This field is use to add buffers to the free list pool if they are reclaimed from hard allocated entries without having to go through warm reset. This field may only be programmed after buffers have been allocated and released via D18F0x6C[RlsLnkFullTokCntImm] or D18F0x6C[RlsLnkFullTokCntOnRst] .
27:23	Reserved.
22:20	Sri2XbarFreeRspDBC: SRI to XBAR free response data buffer count. Read-write. BIOS: 0.
19:16	Sri2XbarFreeXreqDBC: SRI to XBAR free request and posted request data buffer count. Read-write. BIOS: 5h. If Sri2XbarFreeRspDBC=0h, then these buffers are shared between requests, responses and posted requests and the number of buffers allocated is two times the value of this field.
15:12	Sri2XbarFreeRspCBC: SRI to XBAR free response command buffer count. Read-write. BIOS: 0h.
11:8	Sri2XbarFreeXreqCBC: SRI to XBAR free request and posted request command buffer count. Read-write. BIOS: 6h. If Sri2XbarFreeRspCBC=0h, then these buffers are shared between requests, responses and posted requests and the number of buffers allocated is two times the value of this field.
7:6	Reserved.
5:0	Xbar2SriFreeListCBC: XBAR to SRI free list command buffer count. Read-write. BIOS: 1Bh.

D18F3x[84:80] ACPI Power State Control

This block consists of eight identical 8-bit registers, one for each System Management Action Field (SMAF) code associated with STPCLK assertion commands from the link. Refer to the descriptions below for the associated ACPI state and system management actions for each of the 8 SMAF codes. The SmafAct fields specify the system management actions taken when the corresponding SMAF code is received. For instance, a SMAF code of 5 results in the power management actions specified by SmafAct5. Some ACPI states and associated SMAF codes may not be supported in certain conditions. See [2.5 \[Power Management\]](#) for which states are supported.

When a link STPCLK assertion command is received by the processor, the power management commands specified by the register with the corresponding SMAF code are invoked. When the STPCLK deassertion command is received by the processor, the processor returns into the operational state. However, had the NB COF-change command been issued (NbCofChg), the NB returns in the new NB P-state.

In multi-node systems, these registers should be programmed identically in all nodes.

Table 173: SMAF Action Definition

Register	SmafAct	ACPI state	Description
D18F3x84[31:24]	SmafAct7	C1	Initiated when a Halt instruction is executed by processor. This does not involve the interaction with the SMC, therefore the SMC is required to never send STPCLK assertion commands with SMAF=7h.
D18F3x84[23:16]	SmafAct6	S4/S5	Initiated by a processor access to the ACPI-defined PM1_CNTa register.
D18F3x84[15:8]	SmafAct5	Throttling	Occurs based upon SMC hardware-initiated throttling. Refer to section 1.5.4 [Supported Feature Variations] for package-specific support. AMD recommends using PROCHOT_L for thermal throttling and not implementing stop clock based throttling.
D18F3x84[7:0]	SmafAct4	S3	Initiated by a processor access to the ACPI-defined PM1_CNTa register.
D18F3x80[31:24]	SmafAct3	S1	Initiated by a processor access to the ACPI-defined PM1_CNTa register.
D18F3x80[23:16]	SmafAct2	-	
D18F3x80[15:8]	SmafAct1	C3, C1E, or Link init.	Initiated by an access to the ACPI-defined P_LVL3 register.
D18F3x80[7:0]	SmafAct0	C2	Initiated by a processor access to the ACPI-defined P_LVL2 register.

D18F3x80 ACPI Power State Control Low

Reset: 0000_0000h. Read-write.

Bits	Description
31:29	ClkDivisorSmafAct3. See: ClkDivisorSmafAct0.
26	NbGateEnSmafAct3. See: NbGateEnSmafAct0.

25	NbLowPwrEnSmafAct3. See: NbLowPwrEnSmafAct0.																				
24	CpuPrbEnSmafAct3. See: CpuPrbEnSmafAct0.																				
23:21	ClkDivisorSmafAct2. See: ClkDivisorSmafAct0.																				
18	NbGateEnSmafAct2. See: NbGateEnSmafAct0.																				
17	NbLowPwrEnSmafAct2. See: NbLowPwrEnSmafAct0.																				
16	CpuPrbEnSmafAct2. See: CpuPrbEnSmafAct0.																				
15:13	ClkDivisorSmafAct1. See: ClkDivisorSmafAct0.																				
10	NbGateEnSmafAct1. See: NbGateEnSmafAct0.																				
9	NbLowPwrEnSmafAct1. See: NbLowPwrEnSmafAct0.																				
8	CpuPrbEnSmafAct1. See: CpuPrbEnSmafAct0.																				
7:5	<p>ClkDivisorSmafAct0: clock divisor. Read-write. Specifies the core clock frequency while in the low-power state. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>/1</td> <td>100b</td> <td>/16</td> </tr> <tr> <td>001b</td> <td>/2</td> <td>101b</td> <td>/128</td> </tr> <tr> <td>010b</td> <td>/4</td> <td>110b</td> <td>/512</td> </tr> <tr> <td>011b</td> <td>/8</td> <td>111b</td> <td>Turn off clocks</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	Turn off clocks
Bits	Description	Bits	Description																		
000b	/1	100b	/16																		
001b	/2	101b	/128																		
010b	/4	110b	/512																		
011b	/8	111b	Turn off clocks																		
2	<p>NbGateEnSmafAct0: northbridge gate enable. Read-write. This bit does not control hardware. NbLowPwrEn is required to be set if this bit is set. Regardless of this bit, NB coarse gaters are always enabled in the low-power state and MEMCLK is always tristated when DRAM is in self-refresh mode.</p>																				
1	<p>NbLowPwrEnSmafAct0: Northbridge low-power enable. Read-write. 1=The NB clock is ramped down to the divisor specified by D18F3xD4[NbClkDiv] and DRAM is placed into self-refresh mode when LDTSTOP_L is asserted while in the low-power state.</p>																				
0	<p>CpuPrbEnSmafAct0: CPU direct probe enable. Read-write. Specifies how probes are handled while in the low-power state. 0=When the probe request comes into the NB, the core clock is brought up to the COF (based on the current P-state), all outstanding probes are completed, the core waits for a hysteresis time based on D18F3xD4[ClkRampHystSel], and then the core clock is brought down to the frequency specified by ClkDivisor. 1=The core clock does not change frequency; the probe is handled at the frequency specified by ClkDivisor; this may only be set if:</p> <ul style="list-style-type: none"> • ClkDivisor specifies a divide-by 1, 2, 4, 8, or 16 and NbCof <= 3.2 GHz • ClkDivisor specifies a divide-by 1, 2, 4, or 8 and NbCof >= 3.4 GHz <p>This bit also specifies functionality of the timer used for cache flushing during halt. See D18F3xDC[CacheFlushOnHaltTmr].</p> <ul style="list-style-type: none"> • If ((D18F3x84[CpuPrbEnSmafAct7]==0) && (D18F3xDC[IgnCpuPrbEn]==0)), only the time when the core is halted and has its clocks ramped up to service probes is counted. • If ((D18F3x84[CpuPrbEnSmafAct7]==1) or (D18F3xDC[IgnCpuPrbEn]==1)), all of the time the core is halted is counted. 																				

D18F3x84 ACPI Power State Control High

Reset: 0000_0000h. Read-write.

Bits	Description
31:29	ClkDivisorSmafAct7 . See: D18F3x80[ClkDivisorSmafAct0] .
26	NbGateEnSmafAct7 . See: D18F3x80[NbGateEnSmafAct0] .
25	NbLowPwrEnSmafAct7 . See: D18F3x80[NbLowPwrEnSmafAct0] .
24	CpuPrbEnSmafAct7 . See: D18F3x80[CpuPrbEnSmafAct0] .
23:21	ClkDivisorSmafAct6 . See: D18F3x80[ClkDivisorSmafAct0] .
18	NbGateEnSmafAct6 . See: D18F3x80[NbGateEnSmafAct0] .
17	NbLowPwrEnSmafAct6 . See: D18F3x80[NbLowPwrEnSmafAct0] .
16	CpuPrbEnSmafAct6 . See: D18F3x80[CpuPrbEnSmafAct0] .
15:13	ClkDivisorSmafAct5 . See: D18F3x80[ClkDivisorSmafAct0] .
10	NbGateEnSmafAct5 . See: D18F3x80[NbGateEnSmafAct0] .
9	NbLowPwrEnSmafAct5 . See: D18F3x80[NbLowPwrEnSmafAct0] .
8	CpuPrbEnSmafAct5 . See: D18F3x80[CpuPrbEnSmafAct0] .
7:5	ClkDivisorSmafAct4 . See: D18F3x80[ClkDivisorSmafAct0] .
2	NbGateEnSmafAct4 . See: D18F3x80[NbGateEnSmafAct0] .
1	NbLowPwrEnSmafAct4 . See: D18F3x80[NbLowPwrEnSmafAct0] . Char.Temp.BIOS: 1.
0	CpuPrbEnSmafAct4 . See: D18F3x80[CpuPrbEnSmafAct0] .

D18F3x88 NB Configuration 1 Low (NB_CFG1_LO)

Bits	Description
31:0	MSRC001_001F[31:0] , MSRC001_101F[31:0] are an alias of D18F3x88. See MSRC001_001F .

D18F3x8C NB Configuration 1 High (NB_CFG1_HI)

Bits	Description
31:0	MSRC001_001F[63:32] , MSRC001_101F[63:32] are an alias of D18F3x8C. See MSRC001_001F .

D18F3xA0 Power Control Miscellaneous

Bits	Description																				
31	CofVidProg: COF and VID of P-states programmed. Read-only. Reset: Fuse[CofVidProg]. 1=Out of cold reset, the VID, FID, and DID values of the P-state registers specified by MSRC001_0071 [StartupPstate] and D18F5x174 [StartupNbPstate] have been applied to the processor. 0=Out of cold reset, the boot VID is applied to all processor power planes, the NB clock plane is set to 800 MHz (with a FID of 00h=800 MHz and a DID of 0b) and core CPU clock planes are set to 800 MHz (with a FID of 00h=1.6 GHz and a DID of 1h). Registers containing P-state information such as FID, DID, and VID values are valid out of cold reset independent of the state of D18F3xA0 [CofVidProg]. BIOS must transition the processor to a valid P-state out of cold reset when D18F3xA0 [CofVidProg]=0. See 2.5.3.1.6 [BIOS Requirements for Core P-state Initialization and Transitions] .																				
27:16	ConfigId: Configuration identifier. Read-only. Reset: Fuse[ConfigId]. Specifies the configuration ID associated with the product. This field indicates the fuse recipe (PSDD source) used to generate the part. The ConfigId namespace is unique within a specific value for D18F4x160 [Native Die CPUID Family/Model/Stepping] .																				
14	Svi2HighFreqSel: SVI2 high frequency select. Read-write. Cold reset: 0. IF (SVI1) THEN BIOS: 0. ELSE BIOS: 1. ENDIF. 0=3.4 MHz. 1=20 MHz. Writes to this field take effect at the next SVI command boundary. If 20 MHz is supported by the VRM, BIOS should program this to 1 prior to any VID transitions. Once this bit is set, it should not be cleared until the next cold reset.																				
13:11	PllLockTime: PLL synchronization lock time. Read-write. Reset: 0. BIOS: 001b. If a P-state change occurs that applies a new FID to the PLL, this field specifies the time required for the PLL to lock to the new frequency. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>1 us</td> <td>100b</td> <td>8 us</td> </tr> <tr> <td>001b</td> <td>2 us</td> <td>101b</td> <td>16 us</td> </tr> <tr> <td>010b</td> <td>3 us</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>4 us</td> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	000b	1 us	100b	8 us	001b	2 us	101b	16 us	010b	3 us	110b	Reserved	011b	4 us	111b	Reserved
Bits	Description	Bits	Description																		
000b	1 us	100b	8 us																		
001b	2 us	101b	16 us																		
010b	3 us	110b	Reserved																		
011b	4 us	111b	Reserved																		
10	Reserved.																				
9	Reserved.																				
8	PsiVid[7]. Read-write. Reset: 0. BIOS: 2.5.1.3.1.1 . See PsiVid[6:0].																				
7	PsiVidEn: PSI_L VID enable. Read-write. Reset: 0. BIOS: 2.5.1.3.1.1 . This bit specifies how PSI_L is controlled. This signal may be used by the voltage regulator to improve efficiency while in reduced power states. 1=Control over the PSI_L signal is as specified by the PsiVid field of this register. 0=PSI_L is always high. See 2.5.1.3.1 [PSIx_L Bit] .																				
6:0	PsiVid[6:0]: PSI_L VID threshold. Read-write. Reset: 0. BIOS: 2.5.1.3.1.1 . PsiVid[7:0] = {PsiVid[7], PsiVid[6:0]}. When enabled by PsiVidEn, PsiVid[7:0] specifies the threshold value of the VID code generated by the processor, which in turn determines the state of PSI0_L. When the VID code generated by the processor is less than PsiVid[7:0] (i.e., the VID code is specifying a higher voltage level than the PsiVid-specified voltage level), then PSI0_L is high; when the VID code is greater than or equal to PsiVid[7:0], PSI0_L is driven low. See 2.5.1.3.1 [PSIx_L Bit] .																				

D18F3xA4 Reported Temperature Control

The slew rate controls in this register are used to filter processor temperature measurements. Separate controls are provided for a measured temperature, Tctlm, that is higher or lower than Tctl. The per-step timer counts as long as the measured temperature stays either above or below Tctl. Each time the measured temperature changes to the other side of Tctl, the step timer resets, and Tctl is not changed. If, for example, step times are enabled in both directions, Tctl=62.625, and the measured temperature keeps jumping quickly between 62.5 and 63.0, then (assuming the step times are long enough) Tctl would not change. However, once the measured temperature settles on one side of Tctl, Tctl can step toward the measured temperature. If the difference of measured temperature minus Tctl is greater than the value set by MaxTmpDiffUp, then Tctl is set equal to the measured temperature. See [2.10 \[Thermal Functions\]](#).

Bits	Description																											
31:21	CurTmp: current temperature. IF (D18F3xA4[CurTmpTjSel] ==11b) THEN Read-write. ELSE Read-only, updated-by-hardware. ENDIF. Reset: X. Provides the current control temperature, Tctl, after the slew-rate controls have been applied. RangeUnadjusted = ((D18F3xA4[CurTmpTjSel] !=11b) && (D18F3xA4[CurTmpRangeSel] ==0)). <table> <thead> <tr> <th>Bits</th><th>RangeUnadjusted</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000h</td><td>0</td><td>-49</td></tr> <tr> <td>001h</td><td>0</td><td>-48.875</td></tr> <tr> <td>7FEh-002h</td><td>0</td><td><(CurTmp*0.125)-49></td></tr> <tr> <td>7FFh</td><td>0</td><td>206.875</td></tr> <tr> <td>000h</td><td>1</td><td>0</td></tr> <tr> <td>001h</td><td>1</td><td>0.125</td></tr> <tr> <td>7FEh-002h</td><td>1</td><td><CurTmp*0.125></td></tr> <tr> <td>7FFh</td><td>1</td><td>255.875</td></tr> </tbody> </table>	Bits	RangeUnadjusted	Description	000h	0	-49	001h	0	-48.875	7FEh-002h	0	<(CurTmp*0.125)-49>	7FFh	0	206.875	000h	1	0	001h	1	0.125	7FEh-002h	1	<CurTmp*0.125>	7FFh	1	255.875
Bits	RangeUnadjusted	Description																										
000h	0	-49																										
001h	0	-48.875																										
7FEh-002h	0	<(CurTmp*0.125)-49>																										
7FFh	0	206.875																										
000h	1	0																										
001h	1	0.125																										
7FEh-002h	1	<CurTmp*0.125>																										
7FFh	1	255.875																										
20	Reserved.																											
17:16	CurTmpTjSel: Current temperature select. Read-write. Reset: 00. These bits may be used to provide the current temperature or control the temperature for diagnostic software. See 2.10 [Thermal Functions] . <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>CurTmp provides the read-only Tctl value.</td></tr> <tr> <td>01b</td><td>Reserved.</td></tr> <tr> <td>10b</td><td>Reserved.</td></tr> <tr> <td>11b</td><td>CurTmp is a read-write register that specifies a value used to create Tctl. The two LSB's are read-only zero (provides 0.5 degree resolution). Value in CurTmp is passed through slew control logic. That result is used for HTC and SB-TSI. However, the value reported through CurTmp is the same as the input value and is unaffected by the slew control logic.</td></tr> </tbody> </table>	Bits	Description	00b	CurTmp provides the read-only Tctl value.	01b	Reserved.	10b	Reserved.	11b	CurTmp is a read-write register that specifies a value used to create Tctl. The two LSB's are read-only zero (provides 0.5 degree resolution). Value in CurTmp is passed through slew control logic. That result is used for HTC and SB-TSI. However, the value reported through CurTmp is the same as the input value and is unaffected by the slew control logic.																	
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15:13	Reserved.																											
12:8	PerStepTimeDn: per step time down. Read-write. Cold reset: 18h. BIOS: 0Fh. Specifies the time that Tctlm must remain below Tctl before applying a 0.125 downward step. See: PerStepTimeUp.																											
7	TmpSlewDnEn: temperature slew downward enable. Read-write. Cold reset: 0. BIOS: 1. 1=Downward slewing enabled. 0=Downward slewing disabled.																											

6:5	TmpMaxDiffUp: temperature maximum difference up. Read-write. Cold reset: 00b. BIOS: 11b. Specifies the maximum difference, (Tctlm - Tctl), when Tctl immediately updates to Tctlm.										
	<table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 10%;">Bits</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">00b</td> <td>0.0 (disable upward slew)</td> </tr> <tr> <td style="text-align: left;">01b</td> <td>1.0</td> </tr> <tr> <td style="text-align: left;">10b</td> <td>3.0</td> </tr> <tr> <td style="text-align: left;">11b</td> <td>9.0</td> </tr> </tbody> </table>	Bits	Description	00b	0.0 (disable upward slew)	01b	1.0	10b	3.0	11b	9.0
Bits	Description										
00b	0.0 (disable upward slew)										
01b	1.0										
10b	3.0										
11b	9.0										
4:0	PerStepTimeUp: per 1/8th degree step time up. Read-write. Cold reset: 00h. BIOS: 0Fh. Specifies the time that Tctlm must remain above Tctl before applying a 0.125 upward step.										
	<table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 10%;">Bits</th> <th style="text-align: left;">Definition</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">1Fh-00h</td> <td>$\langle \text{PerStepTimeUp}[2:0] + 1 \rangle * 10^{\text{PerStepTimeUp}[4:3]} \text{ ms}$, ranging from 1 ms to 8000 ms.</td> </tr> </tbody> </table>	Bits	Definition	1Fh-00h	$\langle \text{PerStepTimeUp}[2:0] + 1 \rangle * 10^{\text{PerStepTimeUp}[4:3]} \text{ ms}$, ranging from 1 ms to 8000 ms.						
Bits	Definition										
1Fh-00h	$\langle \text{PerStepTimeUp}[2:0] + 1 \rangle * 10^{\text{PerStepTimeUp}[4:3]} \text{ ms}$, ranging from 1 ms to 8000 ms.										

D18F3xA8 Pop Up and Down P-states

Bits	Description
31:29	PopDownPstate. Read-write. Reset: D18F3xDC[HwPstateMaxVal]. BIOS: D18F3xDC[HwP-stateMaxVal]. Specifies the pop-down P-state number. This field uses hardware P-state numbering. See 2.5.3.2.3.3 [Core C6 (CC6) State] . This field must be set to D18F3xDC[HwPstateMaxVal]

D18F3xB8 NB Array Address

S3-check-exclude. Reset: xxxx_xxxxh. [D18F3xB8 \[NB Array Address\]](#) and [D18F3xBC \[NB Array Data Port\]](#) provide a mechanism to inject errors into DRAM and data read from internal NB arrays.

D18F3xB8 should first be written with the target array and address within the array. Read and write accesses to D18F3xBC then access the target address within the target array.

Bits	Description										
9:0	ArrayAddress. Read-write. Selects the location to access within the selected array. This format of this field is a function of ArraySelect.										
	<table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 10%;">ArraySelect</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td style="text-align: left;">1h</td> <td>LPB. See Table 450 [Format of D18F3xB8[ArrayAddress] for LPB].</td> </tr> <tr> <td style="text-align: left;">8h</td> <td>DRAM ECC. See Table 454 [Format of D18F3xB8[ArrayAddress] for DRAM ECC].</td> </tr> <tr> <td style="text-align: left;">Ah</td> <td>TCB. See Table 453 [Format of D18F3xB8[ArrayAddress] for TCB].</td> </tr> <tr> <td style="text-align: left;">All others</td> <td>Reserved</td> </tr> </tbody> </table>	ArraySelect	Description	1h	LPB. See Table 450 [Format of D18F3xB8[ArrayAddress] for LPB] .	8h	DRAM ECC. See Table 454 [Format of D18F3xB8[ArrayAddress] for DRAM ECC] .	Ah	TCB. See Table 453 [Format of D18F3xB8[ArrayAddress] for TCB] .	All others	Reserved
ArraySelect	Description										
1h	LPB. See Table 450 [Format of D18F3xB8[ArrayAddress] for LPB] .										
8h	DRAM ECC. See Table 454 [Format of D18F3xB8[ArrayAddress] for DRAM ECC] .										
Ah	TCB. See Table 453 [Format of D18F3xB8[ArrayAddress] for TCB] .										
All others	Reserved										

D18F3xBC NB Array Data Port

S3-check-exclude. See [D18F3xB8](#) for register access information. Address: D18F3xB8[ArraySelect].

Bits	Description
31:0	Data.

D18F3xBC_x8 DRAM ECC

This register controls injection of errors in writes to DRAM. See [2.14.3.1 \[DRAM Error Injection\]](#).

Bits	Description																				
31:29	Reserved.																				
28:20	ErrInjEn: enable error injection to word. Read-write. Reset: 0. Each bit in this field corresponds to a 16-bit DRAM word and enables injecting errors in that word. <table> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Data[15:0]</td></tr> <tr> <td>[1]</td><td>Data[31:16]</td></tr> <tr> <td>[2]</td><td>Data[47:32]</td></tr> <tr> <td>[3]</td><td>Data[63:48]</td></tr> <tr> <td>[4]</td><td>Data[79:64]</td></tr> <tr> <td>[5]</td><td>Data[95:80]</td></tr> <tr> <td>[6]</td><td>Data[111:96]</td></tr> <tr> <td>[7]</td><td>Data[127:112]</td></tr> <tr> <td>[8]</td><td>ECC[15:0]</td></tr> </tbody> </table>	Bit	Description	[0]	Data[15:0]	[1]	Data[31:16]	[2]	Data[47:32]	[3]	Data[63:48]	[4]	Data[79:64]	[5]	Data[95:80]	[6]	Data[111:96]	[7]	Data[127:112]	[8]	ECC[15:0]
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[5]	Data[95:80]																				
[6]	Data[111:96]																				
[7]	Data[127:112]																				
[8]	ECC[15:0]																				
19	Reserved.																				
18	DramErrEn. Read-write. Reset: 0. 1=Errors are continually injected on DRAM writes. The error injection takes place only on DRAM write accesses and should be initiated by a non-cacheable store. Errors continue to be injected on writes until this bit is cleared to a 0 by software.																				
17	EccWrReq. Read; write-1-only; cleared-by-hardware. Reset: 0. 1=Error is injected on DRAM write at the bits enabled by ErrInjEn and EccVector. A single error injection takes place on the next DRAM write access and should be initiated by a non-cacheable store. This bit is cleared by hardware after the write.																				
16	EccRdReq. Read; write-1-only; cleared-by-hardware. Reset: 0. 1=Indicates a DRAM ECC read is requested. The read takes place on the next DRAM read access and should be initiated by a non-cacheable load. The ECC bits read from DRAM are stored in EccVector. This bit is cleared by hardware after the read.																				
15:0	EccVector: error injection vector. Read-write; S3-check-exclude. Reset: x. When used in conjunction with EccWrReq, each bit of EccVector enables injecting errors to the corresponding bit within each word enabled by ErrInjEn. When used in conjunction with EccRdReq, EccVector holds the contents of the DRAM ECC bits after the read.																				

D18F3xD4 Clock Power/Timing Control 0

Bits	Description
31	NbClkDivApplyAll. Read-write. Cold reset: 0. BIOS: 1. See NbClkDiv.

30:28	<p>NbClkDiv: NB clock divisor. Read-write. Cold reset: Fuse[NbDivAltVid]. BIOS: 001b.</p> <p>Specifies the NB CLK divisor associated with D18F3x80/D18F3x84[NbLowPwrEn]. This divisor is applied while LDTSTOP_L is asserted if the corresponding core CLK divisor, D18F3x80/D18F3x84[ClkDivisor], is set to “turn off clocks” or if NBClkDivApplyAll=1; otherwise, the divisor specified by D18F3x80/D18F3x84[ClkDivisor] is applied. This divisor is relative to the current NB FID frequency, or:</p> $100 \text{ MHz} * (4 + \text{D18F5x16[C:0][NbFid]}).$ <p>If D18F5x16[C:0][NbDid] of the current NB P-state indicates a divisor that is lower than specified by this field, then no NB frequency change is made when entering the low-power state associated with this register (i.e., if this field specifies a divide-by 1 and the DID is divide-by 2, then the divisor remains 2 while in the low-power state). This field is encoded as follows:</p> <table border="1" data-bbox="279 614 1204 783"> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Divide-by 1</td><td>100b</td><td>Divide-by 16</td></tr> <tr> <td>001b</td><td>Divide-by 2</td><td>101b</td><td>Reserved Divide-by 128</td></tr> <tr> <td>010b</td><td>Divide-by 4</td><td>110b</td><td>Reserved Divide-by 512</td></tr> <tr> <td>011b</td><td>Divide-by 8</td><td>111b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	Bits	Description	000b	Divide-by 1	100b	Divide-by 16	001b	Divide-by 2	101b	Reserved Divide-by 128	010b	Divide-by 4	110b	Reserved Divide-by 512	011b	Divide-by 8	111b	Reserved																
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000b	Divide-by 1	100b	Divide-by 16																																		
001b	Divide-by 2	101b	Reserved Divide-by 128																																		
010b	Divide-by 4	110b	Reserved Divide-by 512																																		
011b	Divide-by 8	111b	Reserved																																		
27:24	<p>PowerStepUp. Read-write. Reset: 0000b. Specifies the rate at which blocks of compute unit and NB logic are gated on while the processor transitions from a quiescent state to an active state as part of a power management state transition. There are about 15 steps in this transition for each compute unit and about 5 steps for the NB for the PowerStepDown and PowerStepUp transitions. So the total transition time for a single compute unit is about 15 times the time specified by PowerStepDown and PowerStepUp and the transition time for the NB is about 5 times the time specified by PowerStepDown and PowerStepUp. Use of longer transition times may help reduce voltage transients associated with power state transitions. The bits for PowerStepUp and PowerStepDown are encoded as follows:</p> <table border="1" data-bbox="279 1100 1106 1417"> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0000b</td><td>Reserved. 400 ns</td><td>1000b</td><td>50 ns</td></tr> <tr> <td>0001b</td><td>Reserved. 300 ns</td><td>1001b</td><td>Reserved. 45 ns</td></tr> <tr> <td>0010b</td><td>Reserved. 200 ns</td><td>1010b</td><td>Reserved. 40 ns</td></tr> <tr> <td>0011b</td><td>100 ns</td><td>1011b</td><td>Reserved. 35 ns</td></tr> <tr> <td>0100b</td><td>90 ns</td><td>1100b</td><td>Reserved. 30 ns</td></tr> <tr> <td>0101b</td><td>80 ns</td><td>1101b</td><td>Reserved. 25 ns</td></tr> <tr> <td>0110b</td><td>70 ns</td><td>1110b</td><td>Reserved. 20 ns</td></tr> <tr> <td>0111b</td><td>60 ns</td><td>1111b</td><td>Reserved. 15 ns</td></tr> </tbody> </table> <ul style="list-style-type: none"> If PowerStepDown or PowerStepUp are programmed to greater than 50 ns, then the value applied to the NB is clipped to 50 ns. The compute unit steps are not clipped. PowerStepDown and PowerStepUp should always be configured to less than or equal to 50 ns in client systems. This restriction is to satisfy display refresh and isoc bandwidth requirements. BIOS: 1000b. 	Bits	Description	Bits	Description	0000b	Reserved. 400 ns	1000b	50 ns	0001b	Reserved. 300 ns	1001b	Reserved. 45 ns	0010b	Reserved. 200 ns	1010b	Reserved. 40 ns	0011b	100 ns	1011b	Reserved. 35 ns	0100b	90 ns	1100b	Reserved. 30 ns	0101b	80 ns	1101b	Reserved. 25 ns	0110b	70 ns	1110b	Reserved. 20 ns	0111b	60 ns	1111b	Reserved. 15 ns
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0111b	60 ns	1111b	Reserved. 15 ns																																		
23:20	<p>PowerStepDown. Read-write. Reset: 0000b. BIOS: 1000b. This specifies the rate at which blocks of compute unit and NB logic are gated off while the processor transitions from an active state to a quiescent state as part of a power management state transition.</p>																																				
19:18	Reserved.																																				

14	CacheFlushImmOnAllHalt: cache flush immediate on all halt. Read-write. Reset: 0. 1=Flush the caches immediately when all cores in a package have halted. One of the following conditions must be true in order for the caches to be flushed: <ul style="list-style-type: none"> • D18F4x128[CoreCstateMode]=0 and D18F4x118/D18F4x11C[CacheFlushEn]=1 for the corresponding C-state action field on all cores. • D18F4x128[CoreCstateMode]=1 and D18F3xDC[CacheFlushOnHaltCtl] !=0.
13	Reserved.
12	ClkRampHystCtl: clock ramp hysteresis control. Read-write. Reset: 0. Specifies the time base for ClkRampHystSel when (D18F4x128[CoreCstateMode] ? (D18F3x80/D18F3x84[CpuPrbEn]==0) : (D18F4x118/D18F4x11C[CpuPrbEn]==0)). 0=320 ns. 1=1.28 us.
11:8	ClkRampHystSel: clock ramp hysteresis select. Read-write. Reset: 0h. Char.BIOS: Fh. When the core(s) are in the stop-grant or halt state and a probe request is received, the core clock may need to be brought up to service the probe. <ul style="list-style-type: none"> • If (D18F4x128[CoreCstateMode] ? (D18F3x80/D18F3x84[CpuPrbEn]==0) : (D18F4x118/D18F4x11C[CpuPrbEn]==0)) then this field specifies how long the core clock is left up to service additional probes before being brought back down. Each time a probe request is received, the hysteresis timer is reset such that the period of time specified by this field must expire with no probe request before the core clock is brought back down. The hysteresis time is encoded as (the time base specified by D18F3xD4[ClkRampHystCtl]) * (1 + ClkRampHystSel). • If (D18F4x128[CoreCstateMode] ? (D18F3x80/D18F3x84[CpuPrbEn]==1) : (D18F4x118/D18F4x11C[CpuPrbEn]==1)) then this field specifies a fixed amount of time to allow for probes to be serviced after completing the transition of each core. If, for example, two cores enter stop-grant or halt at the same time, then (1) the first core would complete the transition to the low power state, (2) probe traffic would be serviced for the time specified by this field, (3) the second core would complete the transition to the low power state, and (4) probe traffic would be serviced for the time specified by this field (and afterwards, until the next power state transition). For this purpose, values range from 0h=40 ns to Fh=640 ns, encoded as 40 ns * (1 + ClkRampHystSel).
7:6	Reserved.
5:0	MaxSwPstateCpuCof: maximum software P-state core COF. Read-only. Cold reset: Fuse[MaxSwPstateCpuCof]. Specifies the maximum CPU COF supported by the processor in a software P-state. The maximum frequency is 100 MHz * MaxSwPstateCpuCof, if MaxSwPstateCpuCof is greater than zero; if MaxSwPstateCpuCof = 00h, then there is no frequency limit. Any attempt to change a software P-state CPU COF to a frequency greater than specified by this field is ignored. Processors that support core performance boost must fuse this field to the software P0 frequency or higher. See 2.5.3.1.1.1 [Software P-state Numbering] and 2.5.3.1.5 [Core P-state Transition Behavior] .

D18F3xD8 Clock Power/Timing Control 1

See [2.5.1.4 \[Voltage Transitions\]](#).

Bits	Description																																								
6:4	<p>VSRampSlamTime. Read-write. Cold reset: 000b. BIOS: 100b. Specifies the time the processor waits for voltage transitions to complete before beginning an additional voltage change or a frequency change.</p> <p>IF (SVI1) THEN Wait time = (VSRampSlamTime / 12.5mV) * ABS(destination voltage - current voltage). ELSE Wait time = (VSRampSlamTime / 15mV) * ABS(destination voltage - current voltage). ENDIF.</p> <p>IF (SVI1) THEN</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>6.25 us</td> <td>100b</td> <td>2.50 us</td> </tr> <tr> <td>001b</td> <td>5.00 us</td> <td>101b</td> <td>1.67 us</td> </tr> <tr> <td>010b</td> <td>4.17 us</td> <td>110b</td> <td>1.25 us</td> </tr> <tr> <td>011b</td> <td>3.13 us</td> <td>111b</td> <td>1.00 us</td> </tr> </tbody> </table> <p>ELSE</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>5.00 us</td> <td>100b</td> <td>2.00 us</td> </tr> <tr> <td>001b</td> <td>3.75 us</td> <td>101b</td> <td>1.50 us</td> </tr> <tr> <td>010b</td> <td>3.00 us</td> <td>110b</td> <td>1.20 us</td> </tr> <tr> <td>011b</td> <td>2.40 us</td> <td>111b</td> <td>1.00 us</td> </tr> </tbody> </table> <p>ENDIF.</p>	Bits	Description	Bits	Description	000b	6.25 us	100b	2.50 us	001b	5.00 us	101b	1.67 us	010b	4.17 us	110b	1.25 us	011b	3.13 us	111b	1.00 us	Bits	Description	Bits	Description	000b	5.00 us	100b	2.00 us	001b	3.75 us	101b	1.50 us	010b	3.00 us	110b	1.20 us	011b	2.40 us	111b	1.00 us
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010b	3.00 us	110b	1.20 us																																						
011b	2.40 us	111b	1.00 us																																						

D18F3xDC Clock Power/Timing Control 2

Bits	Description						
31:30	NbsynPtrAdjPstate[2:1]: NB/core synchronization FIFO pointer adjust P-state[2:1]. Read-write. Reset: Fuse[NumBoostStates[2:1]]. See NbsynPtrAdj.						
29:27	NbsynPtrAdjLo: NB/core synchronization FIFO pointer adjust low. Read-write. Cold reset: 000b. BIOS: 101b. See NbsynPtrAdj.						
26	IgnCpuPrbEn: ignore CPU probe enable. Read-write. Cold reset: 0. BIOS: 0. See D18F3x80/D18F3x84[CpuPrbEn] and D18F4x118/D18F4x11C[CpuPrbEn].						
25:19	CacheFlushOnHaltTmr: cache flush on halt timer. Read-write. Cold reset: 00h. IF (BatteryPower) THEN BIOS: 4h. ELSE BIOS: Fh. ENDIF. Specifies how long each core needs to stay in a C-state before it flushes its caches. See CacheFlush-OnHaltCtl, D18F3x80/D18F3x84[CpuPrbEn], [CoreCstateMode], and D18F4x118/D18F4x11C[CacheFlushTmrSel].						
	<table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>5.12 us</td> </tr> <tr> <td>7Fh-01h</td> <td>(<CacheFlushOnHaltTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushOn-HaltTmr> * 10.24 us</td> </tr> </tbody> </table>	Bits	Description	00h	5.12 us	7Fh-01h	(<CacheFlushOnHaltTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushOn-HaltTmr> * 10.24 us
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00h	5.12 us						
7Fh-01h	(<CacheFlushOnHaltTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushOn-HaltTmr> * 10.24 us						

18:16	<p>CacheFlushOnHaltCtl: cache flush on halt control. Read-write. Reset: 000b. BIOS: 000b.</p> <p>Enables cache flush on halt when ((D18F4x128[CoreCstateMode]==1) && (CacheFlushOnHaltCtl != 0)). Specifies what core clock divisor is used after the caches have been flushed, regardless of D18F4x128[CoreCstateMode]. See D18F4x118/D18F4x11C[CacheFlushTmrSel].</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>IF (D18F4x128[CoreCstateMode]) THEN Disabled. ELSE Divide-by 1. ENDIF.</td></tr> <tr> <td>001b</td><td>Divide-by 2</td></tr> <tr> <td>010b</td><td>Divide-by 4</td></tr> <tr> <td>011b</td><td>Divide-by 8</td></tr> <tr> <td>100b</td><td>Divide-by 16</td></tr> <tr> <td>101b</td><td>Reserved Divide-by 128</td></tr> <tr> <td>110b</td><td>Reserved Divide-by 512</td></tr> <tr> <td>111b</td><td>Turn off clocks</td></tr> </tbody> </table> <p>Values of /128 and /512 should be not be used. See D18F3x[84:80] and D18F4x11[C:8] for clock divisor specifications that are in effect during a C-state before the caches have been flushed. See 2.5.3.2.3.1 [C-state Probes and Cache Flushing].</p>	Bits	Description	000b	IF (D18F4x128[CoreCstateMode]) THEN Disabled. ELSE Divide-by 1. ENDIF.	001b	Divide-by 2	010b	Divide-by 4	011b	Divide-by 8	100b	Divide-by 16	101b	Reserved Divide-by 128	110b	Reserved Divide-by 512	111b	Turn off clocks
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011b	Divide-by 8																		
100b	Divide-by 16																		
101b	Reserved Divide-by 128																		
110b	Reserved Divide-by 512																		
111b	Turn off clocks																		
15	<p>NbsynPtrAdjPstate[0]: NB/core synchronization FIFO pointer adjust P-state[0]. Read-write. Reset: Fuse[NumBoostStates[0]]. See NbsynPtrAdj.</p>																		
14:12	<p>NbsynPtrAdj: NB/core synchronization FIFO pointer adjust. Read-write. Cold reset: 000b. BIOS: 110b.</p> <p>Changes to this field take effect after any of the following events :</p> <ul style="list-style-type: none"> • Warm reset. • At least one core on all compute units perform a P-state transition. • An NB P-state transition. <p>There is a synchronization FIFO between the NB clock domain and core clock domains. At cold reset, the read pointer and write pointer for each of these FIFOs is positioned conservatively, such that FIFO latency may be greater than is necessary.</p> <p>NbsynPtrAdj and NbsynPtrAdjLo may be used to position the read pointer and write pointer of each FIFO closer to each other such that latency is reduced. Each increment of NbsynPtrAdj and NbsynPtrAdjLo represents one clock cycle of whichever is the slower clock (longer period) between the NB clock and the core clock. NbsynPtrAdj is used when the core P-state is less than or equal to NbsynPtrAdjPstate, otherwise NbsynPtrAdjLo is used.</p> <p>Values less than the recommended value are allowed; values greater than the recommended value are illegal.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>6h-0h</td><td>Position the read pointer <NbsynPtrAdj, NbsynPtrAdjLo> clock cycles closer to the write pointer.</td></tr> <tr> <td>7h</td><td>Position the read pointer 7 clock cycles closer to the write pointer</td></tr> </tbody> </table>	Bits	Description	6h-0h	Position the read pointer <NbsynPtrAdj, NbsynPtrAdjLo> clock cycles closer to the write pointer.	7h	Position the read pointer 7 clock cycles closer to the write pointer												
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7h	Position the read pointer 7 clock cycles closer to the write pointer																		
11	Reserved.																		

10:8	HwPstateMaxVal: P-state maximum value. Read-write. IF ((D18F3xE8[HtcCapable]==1) && (D18F3x64[HtcTmpLmt]!=0) && (D18F3x64[HtcPstateLimit] > HwPstateMaxVal)) THEN BIOS: D18F3x64[HtcPstateLimit]. ENDIF. Cold reset: specified by the reset state of MSRC001_00[6B:64][PstateEn]; the cold reset value is the highest P-state number corresponding to the MSR in which PstateEn is set (e.g., if MSRC001_0064 and MSRC001_0065 have this bit set and the others do not, then HwPstateMaxVal=1; if MSRC001_0064 has this bit set and the others do not, then HwPstateMaxVal=0). This specifies the highest P-state value (lowest performance state) supported by the hardware. This field must not be written to a value less (higher performance) than MSRC001_0071[CurPstateLimit]. See MSRC001_0061[PstateMaxVal] . This field uses hardware P-state numbering. See 2.5.3.1.1.2 [Hardware P-state Numbering] .
7:0	Reserved.

D18F3xE4 Thermtrip Status

Bits	Description
31	SwThermtp: software THERMTRIP. Write-1-only; cleared-by-hardware. Reset: 0. Writing a 1 to this bit position induces a THERMTRIP event. This bit returns 0 when read. This is a diagnostic bit, and it should be used for testing purposes only.
5	ThermtpEn: THERMTRIP enable. Read-only. Reset: Fuse[ThermTripEn]. 1=The THERMTRIP state is supported. See 2.10.3.4 [THERMTRIP] .
4	Reserved.
3	ThermtpSense: THERMTRIP sense. Read-only. Cold reset: 0. The processor temperature could exceed the THERMTRIP value prior to cold reset. 1=The processor temperature exceeded the THERMTRIP value (regardless as to whether the THERMTRIP state is enabled). This bit is also set when the diagnostic bit SwThermtp = 1.
2	Reserved.
1	Thermtp: THERMTRIP. Read-only. Cold reset: 0. The processor temperature could exceed the THERMTRIP value prior to cold reset. 1=The processor has entered the THERMTRIP state.
0	Reserved.

D18F3xE8 Northbridge Capabilities

Read-only. Unless otherwise specified, 1=The feature is supported by the processor; 0=The feature is not supported.

Bits	Description
31:29	Reserved.
28	SUCCOR. Read-only. See CPUID Fn8000_0007_EBX[SUCCOR] . Value: 0.
27:26	Reserved.
25	Reserved.
24	MemPstateCap: memory P-state capable. Value: ~Fuse[MemPstateDis].

23:20	Reserved.
19	x2Apic: x2APIC capability. Value: 0.
18:16	Reserved.
15	Reserved.
14	MultVidPlane: multiple VID plane capable. Value: 1.
13:12	Reserved.
11	Reserved. Value: 0.
10	HtcCapable: HTC capable. Value: ~Fuse[HtcDis]. This affects D18F3x64 and D18F3x68 .
9	SvmCapable: SVM capable. Value: ~Fuse[SvmDis].
8	MctCap: memory controller (on the processor) capable. Value: (D18F5x84 [DctEn[1:0]]!=00b).
7:5	Reserved.
4	ChipKill: chipkill ECC capable. Value: ~Fuse[EccDis].
3	ECC: ECC capable. Value: ~Fuse[EccDis].
2	EightNode: Eight-node multi-processor capable. Value: (Fuse[DisableMP][2:0]==100b).
1	DualNode: Dual-node multi-processor capable. Value: (Fuse[DisableMP][2:0]==110b).
0	Reserved.

D18F3xFC CPUID Family/Model/Stepping

CPUID Fn0000_0001_EAX, CPUID Fn8000_0001_EAX are an alias of [D18F3xFC](#).

Bits	Description
31:28	Reserved.
27:20	ExtFamily: extended family. Read-only. Value: 07h.
19:16	ExtModel: extended model. Read-only. IF (Fuse[CpuIDFused]) THEN Reset: Fuse[CpuIdExt-Model[3:0]] ELSE Reset: Metal[CpuIdExtModel[3:0]] ENDIF.
15:12	Reserved.
11:8	BaseFamily. Read-only. Reset: Fh.
7:4	BaseModel. Read-only. IF (Fuse[CpuIDFused]) THEN Reset: Fuse[CpuIdModel[3:0]] ELSE Reset: Metal[CpuIdModel[3:0]] ENDIF.
3:0	Stepping. Read-only. IF (Fuse[CpuIDFused]) THEN Reset: Fuse[CpuIdStepping[3:0]] ELSE Reset: Metal[CpuIdStepping[3:0]] ENDIF.

D18F3x138 DCT0 Bad Symbol Identification

Bits	Description
31:0	Reserved.

D18F3x13C DCT1 Bad Symbol Identification

Bits	Description
31:0	Reserved.

D18F3x140 SRI to XCS Token Count

Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

[D18F3x140](#), [D18F3x144](#), and [D18F3x1\[54:48\]](#) specify the number of XCS (XBAR command scheduler) entries assigned to each virtual channel within each source port. See [2.8 \[Northbridge \(NB\)\]](#).

The default totals are:

Buffer allocation rules:

- The totals of SRI, MCT and the links must not exceed the number of XCS entries. XcsSize = 44.
 - Rule: SUM([D18F3x140\[UpReqTok, UpPreqTok, UpRspTok, DnReqTok, DnPreqTok, DnRspTok, IsocReqTok, IsocPreqTok, IsocRspTok, FreeTok\]](#)) + SUM([D18F3x144\[ProbeTok, RspTok\]](#)) + SUM([D18F3x148\[ReqTok0, PReqTok0, RspTok0, ProbeTok0, {FreeTok\[3:2\],FreeTok\[1:0\]}](#), IsocReqTok0, IsocPreqTok0, IsocRspTok0, ReqTok1, PReqTok1, RspTok1, ProbeTok1, IsocReqTok1, IsocPreqTok1, IsocRspTok1]) + SUM([D18F3x14C\[ReqTok0, PReqTok0, RspTok0, ProbeTok0, {FreeTok\[3:2\],FreeTok\[1:0\]}](#), IsocReqTok0, IsocPreqTok0, IsocRspTok0, ReqTok1, PReqTok1, RspTok1, ProbeTok1, IsocReqTok1, IsocPreqTok1, IsocRspTok1])<= XcsSize. See [D18F3x1\[54:48\]](#).

The defaults for [D18F3x140](#) and [D18F3x1\[54:48\]](#) do not allocate any tokens in the isochronous channel. If isochronous flow control mode (IFCM) is enabled ([D18F0x\[E4,C4,A4,84\]\[IsocEn\]](#)), then the XCS token counts must be changed.

- If IFCM is enabled, then [D18F3x140\[IsocReqTok, IsocRspTok\]](#) must each be non-zero. If isochronous posted requests may be generated in the system, then [D18F3x140\[IsocPreqTok\]](#) must also be non-zero. Or, in display refresh mode, [D18F3x140\[IsocReqTok, IsocRspTok\]](#) must be non-zero.

Bits	Description
31:25	Reserved.
24:20	FreeTok: free tokens. Read-write. Reset: 0Ch. BIOS: Fh. The number of free tokens must always be greater than or equal to 2 to ensure deadlock free operation.
19:18	Reserved.
17:16	IsocRspTok: isochronous response tokens. Read-write. Reset: 0. BIOS: 1.

15:14	IsocPreqTok: isochronous posted request tokens. Read-write. Reset: 0. BIOS: 0.
13:12	IsocReqTok: isochronous request tokens. Read-write. Reset: 0. BIOS: 1.
11:10	DnRspTok: downstream response tokens. Read-write. Reset: 1. BIOS: 1.
9:8	UpRspTok: upstream response tokens. Read-write. Reset: 3. BIOS: 1.
7:6	DnPreqTok: downstream posted request tokens. Read-write. Reset: 1. BIOS: 1.
5:4	UpPreqTok: upstream posted request tokens. Read-write. Reset: 1. BIOS: 2.
3:2	DnReqTok: downstream request tokens. Read-write. Reset: 1. BIOS: 1.
1:0	UpReqTok: upstream request tokens. Read-write. Reset: 3. BIOS: 2.

D18F3x144 MCT to XCS Token Count

See [D18F3x140](#).

Bits	Description
31:8	Reserved.
7:4	ProbeTok: probe tokens. Read-write. Reset: 7h. BIOS: 4h.
3:0	RspTok: response tokens. Read-write. Reset: 7h. BIOS: 7h.

D18F3x1[54:48] Link to XCS Token Count

See [D18F3x140](#).

Table 174: Register Mapping for D18F3x1[54:48]

Register	Function
D18F3x148	ONION Link
D18F3x1[54:4C]	Reserved

Bits	Description
31:30	FreeTok[3:2]: free tokens. Read-write. Cold reset: 00b. BIOS: 0. See FreeTok[1:0].
29	Reserved.
28	IsocRspTok1: isochronous response tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
27	Reserved.
26	IsocPreqTok1: isochronous posted request tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
25	Reserved.
24	IsocReqTok1: isochronous request tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
23:22	ProbeTok1: probe tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
21:20	RspTok1: response tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
19:18	PReqTok1: posted request tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
17:16	ReqTok1: request tokens sublink 1. Read-write. Cold reset: 0. BIOS: 0.
15:14	FreeTok[1:0]: free tokens. Read-write. Cold reset: 00b. FreeTok[3:0] = {FreeTok[3:2], FreeTok[1:0]}. BIOS: 00b.
13:12	IsocRspTok0: isochronous response tokens sublink 0. Read-write. Cold reset: 0. BIOS: 0.
11:10	IsocPreqTok0: isochronous posted request tokens sublink 0. Read-write. Cold reset: 0. BIOS: IF (REG==D18F3x148) THEN 1 ELSE 0 ENDIF. See D18F0x6C[ApplyIsocModeEnNow] .
9:8	IsocReqTok0: isochronous request tokens sublink 0. Read-write. Cold reset: 0. BIOS: IF (REG==D18F3x148) THEN 1 ELSE 0 ENDIF.
7:6	ProbeTok0: probe tokens sublink 0. Read-write. Cold reset: 2. BIOS: 0.
5:4	RspTok0: response tokens sublink 0. Read-write. Cold reset: 2. BIOS: IF (REG==D18F3x148) THEN 2 ELSE 0 ENDIF.
3:2	PReqTok0: posted request tokens sublink 0. Read-write. Cold reset: 2. BIOS: IF (REG==D18F3x148) THEN 2 ELSE 0 ENDIF.
1:0	ReqTok0: request tokens sublink 0. Read-write. Cold reset: 2. BIOS: IF (REG==D18F3x148) THEN 2 ELSE 3 ENDIF.

D18F3x160 NB Machine Check Misc (DRAM Thresholding) 0 (MC4_MISC0)See [2.14.1.7 \[Error Thresholding\]](#). D18F3x160 is associated with the DRAM error type. See [MSR0000_0413](#).

Bits	Description
31	Valid. Read-only. Reset: 1.
30	CntP: counter present. Read-only. Reset: 1.
29	Locked. Read-only. Reset: 0.

28:24	Reserved.
23:20	LvtOffset: LVT offset. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0h. BIOS: 1h.
19	CntEn: counter enable. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0.
18:17	IntType: interrupt type. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Cold reset: 0.
16	Ovrlf: overflow. IF (Locked) THEN Read-only; set-by-hardware. ELSE Read-write; set-by-hardware. ENDIF. Cold reset: 0.
15:12	Reserved.
11:0	ErrCnt: error counter. IF (Locked) THEN Read-only; updated-by-hardware. ELSE Read-write; updated-by-hardware. ENDIF. Cold reset: 0.

D18F3x168 NB Machine Check Misc (Link Thresholding) 1 (MC4_MISC1)

See [2.14.1.7 \[Error Thresholding\]](#). D18F3x168 is associated with the link error type. See [MSRC000_0408](#).

Bits	Description
31	Valid. Read-only. Reset: 1.
30	CntP: counter present. Read-only. Reset: 1.
29	Locked. Read-only. Reset: 0.
28:24	Reserved.
23:20	LvtOffset: LVT offset. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0h. BIOS: 1h.
19	CntEn: counter enable. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0.
18:17	IntType: interrupt type. IF (Locked) THEN Read-only. ELSE Read-write. ENDIF. Cold reset: 0.
16	Ovrlf: overflow. IF (Locked) THEN Read-only; set-by-hardware. ELSE Read-write; set-by-hardware. ENDIF. Cold reset: 0.
15:12	Reserved.
11:0	ErrCnt: error counter. IF (Locked) THEN Read-only; updated-by-hardware. ELSE Read-write; updated-by-hardware. ENDIF. Cold reset: 0.

D18F3x17C Extended Freelist Buffer Count

Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

Bits	Description
31:4	Reserved.
3:0	SPQPrbFreeCBC: XBAR to SRI Probe command buffer freelist. Reset: 8h. Read-write. BIOS: 8h.

D18F3x180 Extended NB MCA Configuration

Reset: 0000_0000h. This register is an extension of [D18F3x44 \[MCA NB Configuration\]](#).

Bits	Description
31	Reserved.
30	Reserved. Read-write.
29	Reserved. Read-write. SyncFloodOnG5CrcErr.
28	SyncFloodOnCC6DramUcErr: Read-write. BIOS: 1. 1=Enable generation of SyncFlood when we hit an Uncorrectable ECC error on C6 restore reads.
27	Reserved. Read-write.
26	ConvertUnCorToCorErrEn: convert uncorrectable error to correctable error enable. Read-write. 1=The status of uncorrectable errors is changed to appear as correctable errors; MSR0000_0411 [UC, PCC] are cleared and a machine check exception will not be raised. For uncorrectable ECC errors, MSR0000_0411 [UECC] is cleared and MSR0000_0411 [CECC] is set. Deferred errors are not affected. This field is intended for debug observability.
25	EccSymbolSize: ECC symbol size and code selection. Read-write. BIOS: See 2.14.2 [DRAM ECC Considerations] . 0=x4 symbol size and code used. 1=reserved
24	McaLogErrAddrWdtErr: log error address on WDT errors. Read-write. BIOS: 1. 1=When a watchdog timeout error occurs (see MSR0000_0410 [WDTRptEn]), the associated address is logged and MSR0000_0411 [AddrV] is set. 0=When a watchdog timeout error occurs, NB state information is saved and MSR0000_0411 [AddrV] is cleared. See D18F3x50 for details on saved information.
23	Reserved. Read-write.
22	Reserved. Read-write.
21	SyncFloodOnCpuLeakErr: sync flood on CPU leak error. Read-write. BIOS: 1. 1=Enable sync flood when one of the cores encounters an uncorrectable error which cannot be contained to the process on the core.
20	Reserved. Read-write.
19	PwP2pDatErrRmtPropDis: posted write for remote peer-to-peer data error propagation disable. Read-write. 1= A peer-to-peer posted write with a data error is not propagated to the target IO link chain if the target IO link chain is not attached to the local node (the same node as the source IO link chain). Instead, the write is dropped by the host bridge. This bit can be used in conjunction with DatWrErrDeferEn to cause a machine check exception and SyncFloodOnDeferErrToIO to cause a sync flood. The state of this field is ignored if SyncFloodOnUsPwDatErr==1.

18	PwP2pDatErrLclPropDis: posted write for local peer-to-peer data error propagation disable. Read-write. 1=A peer-to-peer posted write with a data error is not propagated to the target IO link chain if the target IO link chain is attached to the local node (the same node as the source IO link chain). Instead, the write is dropped by the host bridge. This bit can be used in conjunction with DatWrErrDeferEn to cause a machine check exception and SyncFloodOnDeferErrToIO to cause a sync flood. The state of this field is ignored if SyncFloodOnUsPwDatErr==1.
17	SyncFloodOnDeferErrToIO: convert deferred error for an IO link to sync flood enable. Read-write. BIOS: 1. 1=A deferred error which targets an IO link device is turned into a sync flood. <ul style="list-style-type: none"> When DramErrDeferEn is set and the read response is for a DMA read with a data error, setting SyncFloodOnDeferErrToIO causes a sync flood. When DatWrErrDeferEn is set and the write is peer-to-peer, setting SyncFloodOnDeferErrToIO causes a sync flood.
16	DeferDatErrNcHtMcaEn: convert deferred error for an IO link to machine check exception enable. IF (D18F3xE8 [SUCCOR]) THEN Read-write. ELSE Read-only. ENDIF. 1=A deferred error which targets an IO link device is turned into a machine check exception. <ul style="list-style-type: none"> When DramErrDeferEn is set and the read response is for a DMA read with a data error, setting DeferDatErrNcHtMcaEn causes an uncorrected error to be logged and a machine check exception to be generated. An error response is returned to the IO device irrespective of the setting of DeferDatErrNcHtMcaEn. When DatWrErrDeferEn is set and the write is peer-to-peer, setting DeferDatErrNcHtMcaEn causes an uncorrected error to be logged and a machine check exception to be generated. An error indication is sent to the target IO device irrespective of the setting of DeferDatErrNcHtMcaEn.
15	Reserved.
10	Reserved. Read-write.
9	SyncFloodOnUCNbAry: sync flood on UC NB array error. Read-write. BIOS: 1. 1=Enable sync flood on detection of an UC error in an NB array.
8	SyncFloodOnProtErr: sync flood on protocol error. Read-write. BIOS: 1. 1=Enable sync flood on detection of link protocol error, L3 protocol error, and probe filter protocol error.
7	SyncFloodOnTgtAbortErr. Read-write. BIOS: 1. 1=Enable sync flood on generated or received link responses that indicate target aborts.
6	SyncFloodOnDatErr. Read-write. BIOS: 1. 1=Enable sync flood on generated or received link responses that indicate data error.
5	DisPciCfgCpuMstAbortRsp. Read-write. BIOS: 1. 1=For master abort responses to CPU-initiated configuration accesses, disables MCA error reporting and generation of an error response to the core. It is recommended that this bit be set in order to avoid MCA exceptions being generated from master aborts for PCI configuration accesses, which are common during device enumeration.
4	ChgMstAbortToNoErr. Read-write. 1=Signal no errors instead of master abort in link response packets to IO devices on detection of a master abort condition. When ChgMstAbortToNoErr and D18F3x44 [IoMstAbortDis] are both set, ChgMstAbortToNoErr takes precedence.
3	ChgDatErrToTgtAbort. Read-write. 1=Signal target abort instead of data error in link response packets to IO devices (for Gen1 link compatibility).
2	WDTCntSel[3]: watchdog timer count select bit[3]. Read-write. See D18F3x44 [WDTCntSel].

1	SyncFloodOnUsPwDatErr: sync flood on upstream posted write data error. Read-write. BIOS: 1. 1=Enable sync flood generation when an upstream posted write data error is detected; setting of PwP2pDatErrRmtPropDis and PwP2pDatErrLclPropDis are ignored.
0	McaLogUsPwDatErrEn: MCA log of upstream posted write data error enable. Read-write. BIOS: 1. 1=Enable logging of upstream posted write data errors in MCA (if NB MCA registers are appropriately enabled and configured).

D18F3x188 NB Configuration 2 (NB_CFG2)

Same-for-all.

Bits	Description
27	DisCpuWrSzDw64ReOrd: disable streaming store reorder. Read-write. Reset: 1. BIOS: 1. 1=Disable reordering of streaming store commands.
9	DisL3HiPriFreeListAlloc. Read-write. Reset: 0. BIOS: 1. 1=Disables normal SRQ entry scheme which gives higher priority to L3 than XBAR.

D18F3x190 Downcore Control

Cold reset: 0000_0000h. See [2.4.4 \[Processor Cores and Downcoring\]](#) and [2.4.4.1 \[Software Downcoring using D18F3x190\[DisCore\]\].](#)

Bits	Description										
31:0	DisCore. Read-write; reset-applied. 0=Logical Core enabled. 1=Logical Core disabled. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Logical Core 0.</td> </tr> <tr> <td>[2:1]</td> <td>Logical Core <BIT>.</td> </tr> <tr> <td>[3]</td> <td>Logical Core 3.</td> </tr> <tr> <td>[31:4]</td> <td>Reserved.</td> </tr> </tbody> </table>	Bit	Description	[0]	Logical Core 0.	[2:1]	Logical Core <BIT>.	[3]	Logical Core 3.	[31:4]	Reserved.
Bit	Description										
[0]	Logical Core 0.										
[2:1]	Logical Core <BIT>.										
[3]	Logical Core 3.										
[31:4]	Reserved.										

D18F3x1A0 Core Interface Buffer Count

Out of cold reset, the processor allocates a minimal number of buffers that is smaller than the default values in the register. BIOS must use [D18F0x6C\[RlsLnkFullTokCntImm\]](#) or [D18F0x6C\[RlsLnkFullTokCntOnRst\]](#) for the values in the register to take effect. This is necessary even if the values are unchanged from the default values.

- The following buffer allocations rules must be satisfied:
 - CpuCmdBufCnt ≥ 2 .

Bits	Description
31	Reserved.

30:26	NbToCpuPrbLmt. Read-write. Reset: 10h. Maximum number of outstanding probes to the compute-unit. <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>02h-00h</td><td>Reserved</td></tr> <tr> <td>0Fh-03h</td><td>Maximum of <NbToCpuPrbLmt> probes.</td></tr> <tr> <td>1Fh-10h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	02h-00h	Reserved	0Fh-03h	Maximum of <NbToCpuPrbLmt> probes.	1Fh-10h	Reserved
Bits	Description								
02h-00h	Reserved								
0Fh-03h	Maximum of <NbToCpuPrbLmt> probes.								
1Fh-10h	Reserved								
25:24	Reserved.								
23:20	NbToCpuDatReqLmt. Read-write. Reset: Ch. Octword outstanding per core limit. <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>Ch-0h</td><td>Octword outstanding per core limit</td></tr> <tr> <td>Fh-Dh</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	Ch-0h	Octword outstanding per core limit	Fh-Dh	Reserved		
Bits	Description								
Ch-0h	Octword outstanding per core limit								
Fh-Dh	Reserved								
19	Reserved.								
18:16	CpuToNbFreeBufCnt. Read-write. Reset: 2h. Provides the number of tokens which can be released to each compute unit from the freelist pool. This field can be updated at any time by BIOS and does not require a warm reset to take effect. BIOS: 11b. <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>3h-0h</td><td>Number of tokens released to each compute unit from the freelist pool.</td></tr> <tr> <td>7h-4h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	3h-0h	Number of tokens released to each compute unit from the freelist pool.	7h-4h	Reserved		
Bits	Description								
3h-0h	Number of tokens released to each compute unit from the freelist pool.								
7h-4h	Reserved								
15:12	Reserved. Read-write; Reset-applied. Cold reset: 4h.								
11:10	Reserved.								
9:4	Reserved. Read-write; Reset-applied. Cold reset: IF (NumOfCompUnitsOnNode==1) THEN 1Ch ELSEIF (NumOfCompUnitsOnNode==2) THEN 18h ENDIF.								
3	Reserved.								
2:0	CpuCmdBufCnt: CPU to SRI command buffer count. Read-write; reset-applied. Each compute unit is allocated the number of buffers specified by this field. Reset: 2h. BIOS: 1h.								

D18F3x1CC IBS Control

Reset: 0000_0000h. [MSRC001_103A](#) is an alias of D18F3x1CC. D18F3x1CC is programmed by BIOS; The OS reads the LVT offset from [MSRC001_103A](#).

Bits	Description
31:9	Reserved.
8	LvtOffsetVal: local vector table offset valid. Read-write. BIOS: 1. 1=The offset in LvtOffset is valid. 0=The offset in LvtOffset is not valid and IBS interrupt generation is disabled.

7:4	Reserved.						
3:0	LvtOffset: local vector table offset. Read-write. BIOS: 0h. Specifies the address of the IBS LVT entry in the APIC registers. See APIC[530:500] . <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3h-0h</td> <td>LVT address = <500h + LvtOffset<<4></td> </tr> <tr> <td>Fh-4h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	3h-0h	LVT address = <500h + LvtOffset<<4>	Fh-4h	Reserved
Bits	Description						
3h-0h	LVT address = <500h + LvtOffset<<4>						
Fh-4h	Reserved						

D18F3x1FC Product Information Register 1

Bits	Description
31:1	Reserved. Value: Fuse[ScratchFuses[31:1]].
0	DcTdpSupport. Value: Fuse[ScratchFuses[0]]. 1=Dynamic Configurable TDP supported. See 2.5.11.8 [Dynamic Configurable TDP (DcTDP)] .

D18F3x200 Performance Mode Control Register

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:4	EnCpuSkidBufFull. Read-write. Enables optimal use of the CPU skid buffers, in the presence of multiple data movement requests from the same core. This value shouldbe set based on the number of CPU skid buffers instantiated in the design.
3	EnMcqPrbPickThrottle. Read-write. BIOS: 0. 1=Enabling throttling the MCQ to ensure the bypass path is taken by the probes instead of allocating in to the XCS.
2	EnDctOddToNcLnkDatXfr. Read-write. BIOS: 0. 1=Enables direct transfer of data from odd-numbered DRAM channels (1,3,..) to non-coherent links on the local node.
1	EnDctEvnToNcLnkDatXfr. Read-write. BIOS: 0. 1=Enables direct transfer of data from even-numbered DRAM channels (0,2,..) to non-coherent links on the local node.
0	Reserved. Read-write.

D18F3x238 DCT2 Bad Symbol Identification

Bits	Description
31:0	Reserved.

D18F3x23C DCT3 Bad Symbol Identification

Bits	Description
31:0	Reserved.

D18F3x2B4 DCT and Fuse Power Gate Control

Cold reset: 0000_0000h.

Bits	Description
31:27	Reserved.
26:12	Reserved.
11:0	Reserved.

3.13 Device 18h Function 4 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F4x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1534h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F4x04 Status/Command

Bits	Description
31:16	Status. Read-only. Reset: 0000_0000_000X_0000b. Only Status[4] may be set to indicate the existence of a PCI-defined capability block. 0=No supported links are unganged. 1=At least one link may be unganged, in which case there is a capability block associated with sublink one of the link in this function.
15:0	Command. Read-only. Value: 0000h.

D18F4x08 Class Code/Revision ID

Reset: 0600_0000h.

Bits	Description
31:8	ClassCode. Read-only. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only.

D18F4x0C Header Type

Reset: 0080_0000h.

Bits	Description
31:0	HeaderTypeReg. Read-only. These bits are fixed at their default values. The header type field indicates that there are multiple functions present in this device.

D18F4x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Value: 00h.

D18F4x110 Sample and Residency Timers

Bits	Description
31:21	Reserved.
20:13	<p>MinResTmr: minimum residency timer. IF D18F4x15C[BoostLock] THEN Read-only. ELSE Read-write. ENDIF. Cold reset: Fuse[MinResTmr].</p> <p>Specifies the minimum amount of time required between APM TDP-initiated P-state transitions. The minimum amount of time is defined as MinResTmr * CSampleTimer * FastCSampleTimer. In addition to the MinResTmr, the requirements in D18F5xB4[NodeTdpAccThrottleThreshold], D18F5xB0[NodeTdpAccBoostThreshold] or D18F5xBC[CmpUnitTdpAccThrottleThreshold] for a given compute unit must be met prior to an APM TDP-initiated P-state transition. See 2.5.9.3 [Bidirectional Application Power Management (BAPM)].</p>
12	Reserved.
11:0	<p>CSampleTimer.</p> <p>Read-write.</p> <p>Cold reset: 0.</p> <p>BIOS: 14h.</p> <p>Specifies the value that the internal CSampleTimer counter must increment to before expiring. When the internal CSampleTimer counter expires, it is reset to 0. This is the rate at which the northbridge samples the power monitor. A value of 0 disables the power monitor sampling. See FastCSampleTimer and 2.5.9 [Application Power Management (APM)].</p> <p>When the Northbridge is in a low power state (D18F3x80/D18F3x84[NbLowPwrEn]=1) and NbCof >= RefClk, the Northbridge updates power information at the following rate: $\text{CSampleTimer} * \text{FastCSampleTimer} \leq \text{Time} \leq (\text{CSampleTimer} * \text{FastCSampleTimer} + (9 * (\text{CLKIN} / \text{NbCof}) / \text{CLKIN}))$</p> <p>When the Northbridge is in a low power state and NbCof < RefClk, the Northbridge updates power information at the following rate: $\text{CSampleTimer} * \text{FastCSampleTimer} \leq \text{Time} \leq (\text{CSampleTimer} * \text{FastCSampleTimer} + (9 * (\text{CLKIN} / \text{NbCof} + 4) / \text{CLKIN}))$</p> <p>When the Northbridge is not in a low power state, the Northbridge samples the power monitor at the following rate: $\text{CSampleTimer} * \text{FastCSampleTimer} \leq \text{Time} \leq (\text{CSampleTimer} * \text{FastCSampleTimer} + (9 * (1 / \text{CLKIN})))$</p>

D18F4x11[C:8] C-state Control

D18F4x11[C:8] consist of three identical 16-bit registers, one for each C-state Action Field (CAF) associated with an IO address that is read to enter C-states. Refer to 2.5.3.2 [Core C-states].

- D18F4x118[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr].
- D18F4x118[31:16] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+1.
- D18F4x11C[15:0] specifies the actions attempted by the core when software reads from the IO address specified by MSRC001_0073[CstateAddr]+2.

D18F4x118 C-state Control 1

Bits	Description
31:30	Reserved.
29	SelfRefrEarly1 . Read-write. Reset: 0. See: SelfRefrEarly0. Temp.BIOS: 0.
28	SelfRefr1 . Read-write. Reset: 0. See: SelfRefr0. Temp.BIOS: 1.
27	NbClkGate1 . Read-write. Reset: 0. See: NbClkGate0. Temp.BIOS: 1.
26	NbPwrGate1 . Read-write. Reset: 0. See: NbPwrGate0.
25	PwrOffEnCstAct1 . Read-write; updated-by-SMU. Reset: 0. See: PwrOffEnCstAct0. BIOS: 1.
24	PwrGateEnCstAct1 . Read-write. Reset: 0. See: PwrGateEnCstAct0. Temp.BIOS: 1.
23:21	ClkDivisorCstAct1 . Read-write. Reset: 0. See: ClkDivisorCstAct0. BIOS: 000b.
20	Reserved.
19:18	CacheFlushTmrSelCstAct1 . Read-write. Reset: 0. See: CacheFlushTmrSelCstAct0. Char.Temp.BIOS: 10b.
17	CacheFlushEnCstAct1 . Read-write. Reset: 0. See: CacheFlushEnCstAct0. Char.Temp.BIOS: 1.
16	CpuPrbEnCstAct1 . Read-write. Reset: 0. See: CpuPrbEnCstAct0. Char.Temp.BIOS: 1.
15:14	Reserved.
13	SelfRefrEarly0: allow early self-refresh . Read-write. Reset: 0. Temp.BIOS: 0. 1=Allow self-refresh while cores in PC1 or CC1 are waiting for the cache flush timer to expire. 0=Wait for cache flush timer to expire before allowing self-refresh. The usage of this bit depends on D18F4x128[CoreCstateMode] . See 2.5.7.2 [DRAM Self-Refresh] and 2.5.3.2.3.1 [C-state Probes and Cache Flushing] .
12	SelfRefr0: self-refresh . Read-write. Reset: 0. Temp.BIOS: 1. 1=Allow DRAM self-refresh while in NB C-states. 0=Prevent DRAM self-refresh while in NB C-states. NbClkGate0 must be equal to SelfRefr0. The usage of this bit depends on D18F4x128[CoreCstateMode] . See 2.5.7.2 [DRAM Self-Refresh] and 2.5.4.2 [NB C-states] .
11	NbClkGate0: NB clock-gating . Read-write. Reset: 0. Temp.BIOS: 1. 1=Allow clock-gating of the NB. 0=Prevent clock-gating of the NB. NbClkGate0 must be equal to SelfRefr0. The usage of this bit depends on D18F4x128[CoreCstateMode] . See 2.5.4.2 [NB C-states] .
10	NbPwrGate0: NB power-gating . Read-write. Reset: 0. 1=Allow power-gating of the NB. 0=Prevent power-gating of the NB. NbPwrGate0 can only be programmed to 1 if NbClkGate0 and SelfRefr0 are programmed to 1. The usage of this bit depends on D18F4x128[CoreCstateMode] . See 2.5.4.2 [NB C-states] .

9	PwrOffEnCstAct0: power off enable. Read-write; updated-by-SMU. Reset: 0. Char.Temp.BIOS: 1. 1=Package power off enable. CacheFlushEnCstAct0 is required to be set if this bit is set. PwrGateEnCstAct0 is required to be set if this bit is set. See 2.5.3.2.3.4 [Package C6 (PC6) State] .
8	PwrGateEnCstAct0: power gate enable. Read-write. Reset: 0. Char.Temp.BIOS: 1. 1=Core power gating is enabled. CacheFlushEnCstAct0 is required to be set if this bit is set. See 2.5.3.2.3.3 [Core C6 (CC6) State] .

7:5	<p>ClkDivisorCstAct0: clock divisor. Read-write. Reset: 0. BIOS: 000b.</p> <p>Specifies the core clock frequency while in the low-power state before the caches are flushed. This divisor is relative to the current FID frequency, or:</p> <ul style="list-style-type: none"> • 100 MHz * (10h + MSRC001_00[6B:64][CpuFid]) of the current P-state specified by MSRC001_0063[CurPstate]. <p>If MSRC001_00[6B:64][CpuDid] of the current P-state indicates a divisor that is deeper than specified by this field, then no frequency change is made when entering the low-power state associated with this register.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>/1</td><td>100b</td><td>/16</td></tr> <tr> <td>001b</td><td>/2</td><td>101b</td><td>/128</td></tr> <tr> <td>010b</td><td>/4</td><td>110b</td><td>/512</td></tr> <tr> <td>011b</td><td>/8</td><td>111b</td><td>Turn off clocks.</td></tr> </tbody> </table> <p>See CacheFlushTmrSelCstAct0.</p>	Bits	Description	Bits	Description	000b	/1	100b	/16	001b	/2	101b	/128	010b	/4	110b	/512	011b	/8	111b	Turn off clocks.
Bits	Description	Bits	Description																		
000b	/1	100b	/16																		
001b	/2	101b	/128																		
010b	/4	110b	/512																		
011b	/8	111b	Turn off clocks.																		
4	Reserved.																				
3:2	<p>CacheFlushTmrSelCstAct0: cache flush timer select. Read-write. Reset: 0. Char.Temp.BIOS: 10b.</p> <p>Specifies the timer to use for cache flush.</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Cache flush timer</th></tr> </thead> <tbody> <tr> <td>00b</td><td>0 us</td></tr> <tr> <td>01b</td><td>D18F3xDC[CacheFlushOnHaltTmr]</td></tr> <tr> <td>10b</td><td>D18F4x128[CacheFlushTmr]</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table> <p>Each core has one timer.</p> <p>D18F3xDC[CacheFlushOnHaltCtl] specifies the core clock divisor to use after the caches are flushed. Writing values greater than 10b result in 10b. See CacheFlushEnCstAct0 and CpuPrbEnCstAct0.</p>	Bits	Cache flush timer	00b	0 us	01b	D18F3xDC[CacheFlushOnHaltTmr]	10b	D18F4x128[CacheFlushTmr]	11b	Reserved										
Bits	Cache flush timer																				
00b	0 us																				
01b	D18F3xDC[CacheFlushOnHaltTmr]																				
10b	D18F4x128[CacheFlushTmr]																				
11b	Reserved																				
1	<p>CacheFlushEnCstAct0: cache flush enable. Read-write. Reset: 0. Char.Temp.BIOS: 1. 1=Cache flush enable. The cache flush timer starts counting when the C-state is entered. See CacheFlushTmrSelCstAct0 and 2.5.3.2.3.1 [C-state Probes and Cache Flushing]. PwrGateEnCstAct0 is required to be set if this bit is set.</p>																				
0	<p>CpuPrbEnCstAct0: core direct probe enable. Read-write. Reset: 0. Char.Temp.BIOS: 1. Specifies how probes are handled while in the low-power state. 0=When the probe request comes into the NB, the core clock is brought up to the COF (based on the current P-state), all outstanding probes are completed, the core waits for a hysteresis time based on D18F3xD4[ClkRampHystSel], and then the core clock is brought down to the frequency specified by ClkDivisorCstAct0. 1=The core clock does not change frequency; the probe is handled at the frequency specified by ClkDivisorCstAct0; this may only be set if:</p> <ul style="list-style-type: none"> • ClkDivisorCstAct0 specifies a divide-by 1, 2, 4, 8, or 16 and NbCof <= 3.2 GHz • ClkDivisorCstAct0 specifies a divide-by 1, 2, 4, or 8 and NbCof >= 3.4 GHz <p>This bit also specifies functionality of the timer used for cache flushing. See CacheFlushTmrSelCstAct0.</p> <ul style="list-style-type: none"> • If CpuPrbEnCstAct0=0 and D18F3xDC[IgnCpuPrbEn]=0, only the time when the core is in a non-C0 state and has its clocks ramped up to service probes is counted. • If CpuPrbEnCstAct0=1 or D18F3xDC[IgnCpuPrbEn]=1, all of the time the core is in a non-C0 state is counted. 																				

D18F4x11C C-state Control 2

Reset: 0000_0000h. Read-write.

Bits	Description
31:14	Reserved.
13	SelfRefrEarly2 . See: D18F4x118[SelfRefrEarly0] .
12	SelfRefr2 . See: D18F4x118[SelfRefr0] .
11	NbClkGate2 . See: D18F4x118[NbClkGate0] .
10	NbPwrGate2 . See: D18F4x118[NbPwrGate0] .
9	PwrOffEnCstAct2 . See: D18F4x118[PwrOffEnCstAct0] .
8	PwrGateEnCstAct2 . See: D18F4x118[PwrGateEnCstAct0] .
7:5	ClkDivisorCstAct2 . See: D18F4x118[ClkDivisorCstAct0] .
4	Reserved.
3:2	CacheFlushTmrSelCstAct2 . See: D18F4x118[CacheFlushTmrSelCstAct0] .
1	CacheFlushEnCstAct2 . See: D18F4x118[CacheFlushEnCstAct0] .
0	CpuPrbEnCstAct2 . See: D18F4x118[CpuPrbEnCstAct0] .

D18F4x124 C-state Interrupt Control

Bits	Description
31:0	Reserved.

D18F4x128 C-state Policy Control 1

Reset: 0080_0000h.

Bits	Description										
31	CstateMsgDis: C-state messaging disable . Read-write. Specifies whether any messages are sent to the FCH when a core enters or exits a C-state. 0=Messages are sent. 1=Messages are not sent. See 2.5.3.2.4.1 [FCH Messaging] .										
24:23	CacheFlushSucMonMispredictAct: cache flush success monitor mispredict action . Read-write. Char. Temp.BIOS: 01b. Specifies the cache flush success monitor decrement when non-C0 residency is shorter than duration specified by CacheFlushSucMonTmrSel. See D18F4x130[CacheFlushSuccessMonitor] . This applies for all cores. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>reset counter to zero</td> </tr> <tr> <td>01b</td> <td>decrement by 1</td> </tr> <tr> <td>10b</td> <td>decrement by 2</td> </tr> <tr> <td>11b</td> <td>decrement by 2</td> </tr> </tbody> </table>	Bits	Description	00b	reset counter to zero	01b	decrement by 1	10b	decrement by 2	11b	decrement by 2
Bits	Description										
00b	reset counter to zero										
01b	decrement by 1										
10b	decrement by 2										
11b	decrement by 2										

22:21	CacheFlushSucMonTmrSel: cache flush success monitor timer select. Read-write. Char.Temp.BIOS: 01b. Specifies the non-C0 duration used to increment the cache flush success monitor. See D18F4x130 [CacheFlushSuccessMonitor]. This threshold applies for all cores. <table border="0"> <thead> <tr> <th><u>Bits</u></th><th><u>Duration</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>Use cache flush timer specified by D18F4x11[C:8]</td></tr> <tr> <td>01b</td><td>D18F3xDC[CacheFlushOnHaltTmr]</td></tr> <tr> <td>10b</td><td>D18F4x128[CacheFlushTmr]</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Duration</u>	00b	Use cache flush timer specified by D18F4x11[C:8]	01b	D18F3xDC [CacheFlushOnHaltTmr]	10b	D18F4x128 [CacheFlushTmr]	11b	Reserved
<u>Bits</u>	<u>Duration</u>										
00b	Use cache flush timer specified by D18F4x11[C:8]										
01b	D18F3xDC [CacheFlushOnHaltTmr]										
10b	D18F4x128 [CacheFlushTmr]										
11b	Reserved										
20:18	CacheFlushSucMonThreshold: cache flush success monitor threshold. Read-write. BIOS: 100b. Flush the caches immediately if cache flushing is enabled and the cache flush success monitor count (D18F4x130 [CacheFlushSuccessMonitor]) == CacheFlushSucMonThreshold. A value of 0 disables the cache flush success monitor. See D18F4x118/D18F4x11C [CacheFlushEn]. This threshold applies for all cores.										
17:12	Reserved. Read-write.										
11:5	CacheFlushTmr: cache flush timer. Read-write. IF (BatteryPower) THEN BIOS: 3Ch. ELSE BIOS: 7Fh. ENDIF. Specifies how long each core needs to stay in a C-state before it flushes its caches. See CoreCstateMode and D18F4x118/D18F4x11C [CacheFlushTmrSel]. <table border="0"> <thead> <tr> <th><u>Bits</u></th><th><u>Description</u></th></tr> </thead> <tbody> <tr> <td>00h</td><td><= 5.12 us</td></tr> <tr> <td>7Fh-01h</td><td>(<CacheFlushTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushTmr> * 10.24 us</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00h	<= 5.12 us	7Fh-01h	(<CacheFlushTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushTmr> * 10.24 us				
<u>Bits</u>	<u>Description</u>										
00h	<= 5.12 us										
7Fh-01h	(<CacheFlushTmr> * 10.24us) - 5.12us <= Time <= <CacheFlushTmr> * 10.24 us										
4:2	HaltCstateIndex. Read-write. Char.Temp.BIOS: 0. Specifies the IO-based C-state that is invoked by a HLT instruction. See CoreCstateMode.										
1	Reserved. Read-write.										
0	Reserved.										

D18F4x13C SMU P-state Control

Reset: 0000_0000h. Read-only, updated-by-SMU.

Bits	Description
31:4	Reserved.
3:1	SmuPstateLimit. Specifies the highest-performance P-state (lowest value) allowed. SmuPstateLimit is always bounded by MSRC001_0061 [PstateMaxVal]. This field uses hardware P-state numbering. See MSRC001_0071 [CurPstateLimit] and 2.5.3.1.1.2 [Hardware P-state Numbering].
0	SmuPstateLimitEn.

D18F4x15C Core Performance Boost Control

Bits	Description
31	<p>BoostLock. Read-only. Reset: Fuse[BoostLock]. Specifies whether the following registers are Read-write, read-only, or have special requirements related to writability. See individual register definitions for details.</p> <ul style="list-style-type: none"> • MSRC001_00[6B:64][CpuFid, CpuDid, CpuVid]. • D18F4x10C[CmpUnit0TdpLimit]. • D18F4x110[MinResTmr] • D18F4x200. • D18F4x204. • D18F4x148. • D18F4x14C. • D18F4x150. • D18F4x154. • D18F4x15C[NumBoostStates]. • D18F4x16C[CstateCnt, CstateBoost, TdpLimitDis, NodeTdpLimitEn]. • D18F5xB0[NodeTdpAccBoostThreshold] • D18F5xB4[NodeTdpAccThrottleThreshold] • D18F5xBC[CmpUnitTdpAccThrottleThreshold] • D18F5xC0[NodeTdpMarginAcc] • D18F5x[268:264,D8:C4][CmpUnitTdpMarginAcc] • D18F4x250[NodeTdpLimit].
30:9	Reserved.
8	<p>CstatePowerEn: C-state power enable. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. BIOS: 1. 1=Enable D18F4x150[CstatePowerP1, CstatePowerP2].</p>
7	<p>ApmMasterEn: APM master enable. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. BIOS: IF(D18F4x15C[NumBoostStates]==0) THEN 0. ELSE 1. ENDIF. 1=Enables the ability to turn on features associated with APM when used in conjunction with the individual feature enable bits. Enables the Northbridge-to-core power monitor request interface. This bit is the master enable bit for all APM related features. Programming this bit to 0 disables all APM related features and disables the Northbridge-to-core power monitor request interface. See 2.5.9 [Application Power Management (APM)]. BIOS must not set D18F4x15C[ApmMasterEn] until after MSRC001_1073[ConfigLocked] is set.</p>
6:5	Reserved.

4:2	NumBoostStates: number of boosted states. IF (D18F4x15C[BoostLock] ApmMasterEn D18F2x1B4[SmuCfgLock]) THEN Read-only. ELSE Read-write. ENDIF. Reset: Fuse[NumBoostStates]. Specifies the number of P-states that are considered boosted P-states. See 2.5.9 [Application Power Management (APM)] . See MSRC001_0072 [NumBoostStates].										
1:0	BoostSrc: boost source. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. BIOS: 2.5.3.1.6 . Specifies whether CPB is enabled or disabled. See 2.5.5.1.6 [Modification of P-state Requests and Visibility] . <table style="margin-top: 5px;"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Boosting disabled Sets P-state limit to NumBoostStates on all cores.</td> </tr> <tr> <td>01b</td> <td>Boosting enabled APM boosting.</td> </tr> <tr> <td>10b</td> <td>Reserved defined as SBB enable.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	Boosting disabled Sets P-state limit to NumBoostStates on all cores.	01b	Boosting enabled APM boosting.	10b	Reserved defined as SBB enable.	11b	Reserved
<u>Bits</u>	<u>Description</u>										
00b	Boosting disabled Sets P-state limit to NumBoostStates on all cores.										
01b	Boosting enabled APM boosting.										
10b	Reserved defined as SBB enable.										
11b	Reserved										

D18F4x164 Fixed Errata

Bits	Description
31:0	FixedErrata. Value: {000000h, Fuse[FixedErrata[7:0]]}. See the Revision Guide for the definition of this field. See 1.2 [Reference Documents] .

D18F4x16C APM TDP Control

Bits	Description						
31:15	Reserved.						
14	CacUpC1. IF D18F4x15C[BoostLock] THEN Read-only. ELSE Read-write. ENDIF. Reset: 1. BIOS: 0. 1=Cac interface is up on C1 (non XC6) state. 0=Cac interface is down and Cstate scalers are used in place of Cac reads.						
13	CstateCores. IF D18F4x15C[BoostLock] THEN Read-only. ELSE Read-write. ENDIF. Reset: 1. Specifies how CstateCnt determines Cstate boost conditions. <table style="margin-top: 5px;"> <thead> <tr> <th style="text-align: left;"><u>Bit</u></th> <th style="text-align: left;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>CstateCnt specifies the number of cores.</td> </tr> <tr> <td>1h</td> <td>CstateCnt specifies the number of compute units (or CPCs).</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Description</u>	0h	CstateCnt specifies the number of cores.	1h	CstateCnt specifies the number of compute units (or CPCs).
<u>Bit</u>	<u>Description</u>						
0h	CstateCnt specifies the number of cores.						
1h	CstateCnt specifies the number of compute units (or CPCs).						
11:9	CstateCnt: C-state count. IF D18F4x15C[BoostLock] THEN Read-only. ELSE Read-write. ENDIF. Reset: Fuse[CStateCnt]. Specifies the number of cores or compute units (see CstateCores) that must be in CC6 before an APM transition can occur to a boosted P-state that is higher performance than the P-state specified by CstateBoost. A value of 0 disables access to P-states above CstateBoost.						

8:6	CstateBoost. Read-write. Reset: Fuse[CstateBoost]. Specifies the P-state which requires the number of cores or compute units (see CstateCores) specified in CstateCnt to be in CC6 before a transition to a higher performance (lower numbered) boosted P-state is allowed. CstateBoost must be less than or equal to D18F4x15C[NumBoostStates] otherwise undefined behavior results. If D18F4x15C[BoostLock] =1, CstateBoost can only be written with values that are greater than or equal to the reset value. Attempts to write values less than the reset value are ignored. A value of 0 indicates that the C-state boost feature is not supported. This field uses hardware P-state numbering. See 2.5.3.1.1.2 [Hardware P-state Numbering] .
5	ApmTdpLimitSts: APM TDP limit status. Read; set-by-hardware; write-1-to-clear. Reset: 0. This bit is set by hardware when D18F5xE8[ApmTdpLimit] changes.
4	ApmTdpLimitIntEn: APM TDP limit interrupt enable. Read-write. Reset: 0. BIOS: 1. 1=Enables the generation of an interrupt using APIC330 of each core when D18F5xE8[ApmTdpLimit] changes. See ERBT-925 and ERBT-1049.
3	TdpLimitDis. IF D18F4x15C[BoostLock] THEN Read-only. ELSE Read-write. ENDIF. IF D0F0xBC_xC010408C[2]==1(Fuse[BapmDisable]). THEN BIOS:1. ENDIF. Reset: 0. 1=Disables TDP limit checking and allows the processor to transition to higher performance P-states. See 2.5.9.3 [Bidirectional Application Power Management (BAPM)] .

D18F4x1C0 Node Cac Register 1

Bits	Description
11:0	NodeCacLatest. Read-only, updated-by-hardware. Reset: 0. Specifies the sum of all instantaneous power credits on each compute unit. NodeCacLatest is reset to 0 when D18F4x15C[ApmMasterEn] =0. NodeCacLatest is the sum of all CmpUnitCacLatest values. CmpUnitCacLatest is an internal, non-software visible value.

D18F4x250 TDP Limit 8

Bits	Description
31	Reserved.
30:28	TdpLimitPstate. Read-write. Reset: 0. Specifies the highest performance P-state that has a power consumption less than or equal to the APM TDP limit. This field is programmed by BIOS and uses software P-state numbering. See 2.5.3.1.1.1 [Software P-state Numbering] and 2.5.5.1.6 [Modification of P-state Requests and Visibility] .
27:12	Reserved.
11:0	NodeTdpLimit. Read-write; Same-for-all. Reset: Fuse[ChipTdpLimit]. Specifies the maximum allowed sum of TDPS from all cores on a node. If the consumed power exceeds the NodeTdpLimit, a P-state limit is applied to all cores on the processor to reduce the power consumption so that it remains within the TDP limit. If D18F4x15C[BoostLock] =1, NodeTdpLimit can only be written with values that are less than or equal to the reset value. Attempts to write an invalid value are ignored. See D18F4x16C[NodeTdpLimitEn] and 2.5.9.2 [TDP Limiting] .

3.14 Device 18h Function 5 Configuration Registers

See 3.1 [Register Descriptions and Mnemonics]. See 2.7 [Configuration Space].

D18F5x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Value: 1535h.
15:0	VendorID: vendor ID. Read-only. Value: 1022h.

D18F5x04 Status/Command

Bits	Description
31:16	Status. Read-only. Value: 0000h.
15:0	Command. Read-only. Value: 0000h.

D18F5x08 Class Code/Revision ID

Bits	Description
31:8	ClassCode. Read-only. Value: 060000h. Provides the host bridge class code as defined in the PCI specification.
7:0	RevID: revision ID. Read-only. Value: 00h.

D18F5x0C Header Type

Bits	Description
31:0	HeaderTypeReg. Read-only. Reset: 0080_0000h. These bits are fixed at their default values. The header type field indicates that there are not multiple functions present in this device.

D18F5x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Value: 00h.

D18F5x[70,60,50,40] Northbridge Performance Event Select Low

Bits	Description
31:0	MSRC001_024[6,4,2,0][31:0] is an alias of D18F5x[70,60,50,40].

D18F5x[74,64,54,44] Northbridge Performance Event Select High

Bits	Description
31:0	MSRC001_024[6,4,2,0][63:32] is an alias of D18F5x[74,64,54,44].

D18F5x[78,68,58,48] Northbridge Performance Event Counter Low

Bits	Description
31:0	MSRC001_024[7,5,3,1][31:0] is an alias of D18F5x[78,68,58,48].

D18F5x[7C,6C,5C,4C] Northbridge Performance Event Counter High

Bits	Description
31:0	MSRC001_024[7,5,3,1][63:32] is an alias of D18F5x[7C,6C,5C,4C].

D18F5x80 Compute Unit Status 1

See [2.4.4 \[Processor Cores and Downcoreng\]](#).

Software associates logical core ID to the cores of the compute units according to the following table. All combinations not listed are reserved.

Table 175: D18F5x80[Enabled, DualCore, TripleCore, QuadCore] Definition

Enabled	DualCore	TripleCore	QuadCore	Definition
1h	xh	xh	1h	1 L2 complex is enabled; four cores of the L2 complex are enabled.
1h	xh	1h	0h	1 L2 complex is enabled; three cores of the L2 complex are enabled.
1h	1h	0h	0h	1 L2 complex is enabled; two cores of the L2 complex are enabled.
1h	0h	0h	0h	1 L2 complex is enabled; one core of the L2 complex are enabled.

Bits	Description										
31:28	Reserved.										
27:24	QuadCore: four cores of a L2 complex are enabled. Read-only. Reset: Reset is a function of Fuse[CoreDis[7:0]], D18F3x190[DisCore[7:0]] , and CLL ; In CLL mode, the reset value is 0001_0001h. 1=Four cores of a L2 complex are enabled. See Table 175 [D18F5x80[Enabled, DualCore, TripleCore, QuadCore] Definition] . <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Logical L2 complex 0</td> </tr> <tr> <td>[1]</td> <td>Reserved</td> </tr> <tr> <td>[2]</td> <td>Reserved</td> </tr> <tr> <td>[3]</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Description	[0]	Logical L2 complex 0	[1]	Reserved	[2]	Reserved	[3]	Reserved
Bit	Description										
[0]	Logical L2 complex 0										
[1]	Reserved										
[2]	Reserved										
[3]	Reserved										
23:20	Reserved.										

19:16	DualCore: two cores of a L2 complex are enabled. Read-only. Reset: Reset is a function of Fuse[CoreDis[7:0]], D18F3x190[DisCore[7:0]], and CLL ; In CLL mode, the reset value is 0001_0001h. 1=Both cores of a L2 complex are enabled. See Table 175 [D18F5x80[Enabled, Dual-Core, TripleCore, QuadCore] Definition] .										
	<table> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Logical L2 complex 0</td></tr> <tr> <td>[1]</td><td>Reserved</td></tr> <tr> <td>[2]</td><td>Reserved</td></tr> <tr> <td>[3]</td><td>Reserved</td></tr> </tbody> </table>	Bit	Description	[0]	Logical L2 complex 0	[1]	Reserved	[2]	Reserved	[3]	Reserved
Bit	Description										
[0]	Logical L2 complex 0										
[1]	Reserved										
[2]	Reserved										
[3]	Reserved										
15:12	Reserved.										
11:8	TripleCore: three cores of a L2 complex are enabled. Read-only. Reset: Reset is a function of Fuse[CoreDis[7:0]], D18F3x190[DisCore[7:0]], and CLL ; In CLL mode, the reset value is 0001_0001h. 1=Three cores of a L2 complex are enabled. See Table 175 [D18F5x80[Enabled, Dual-Core, TripleCore, QuadCore] Definition] .										
	<table> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Logical L2 complex 0</td></tr> <tr> <td>[1]</td><td>Reserved</td></tr> <tr> <td>[2]</td><td>Reserved</td></tr> <tr> <td>[3]</td><td>Reserved</td></tr> </tbody> </table>	Bit	Description	[0]	Logical L2 complex 0	[1]	Reserved	[2]	Reserved	[3]	Reserved
Bit	Description										
[0]	Logical L2 complex 0										
[1]	Reserved										
[2]	Reserved										
[3]	Reserved										
7:4	Reserved.										
3:0	Enabled: at least one core of a L2 complex is enabled. Read-only. Reset: Reset is a function of Fuse[CoreDis[7:0]], D18F3x190[DisCore[7:0]], and CLL ; In CLL mode, the reset value is 0001_0001h. 1=At least one core is enabled in a L2 complex. See Table 175 [D18F5x80[Enabled, DualCore, TripleCore, QuadCore] Definition] .										
	<table> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Logical L2 complex 0</td></tr> <tr> <td>[1]</td><td>Reserved</td></tr> <tr> <td>[2]</td><td>Reserved</td></tr> <tr> <td>[3]</td><td>Reserved</td></tr> </tbody> </table>	Bit	Description	[0]	Logical L2 complex 0	[1]	Reserved	[2]	Reserved	[3]	Reserved
Bit	Description										
[0]	Logical L2 complex 0										
[1]	Reserved										
[2]	Reserved										
[3]	Reserved										

D18F5x84 Northbridge Capabilities 2

Unless otherwise specified, 1=The feature is supported by the processor; 0=The feature is not supported.

Bits	Description
31:29	Reserved. Reserved for future expansion of DdrMaxRateEnf.
28:24	DdrMaxRateEnf: enforced maximum DDR rate. Read-only. Value: Fuse[DdrMaxRateEnf]. See: DdrMaxRate. Specifies the maximum DRAM data rate that the processor is designed to support. Writes to D18F2x94_dct[0][MemClkFreq] that specify a frequency greater than specified by DdrMaxRateEnf will result in the D18F2x94_dct[0][MemClkFreq] being set to DdrMaxRateEnf.
23:21	Reserved.
20:16	DdrMaxRate: maximum DDR rate. Read-only. Value: Fuse[DdrMaxRate]. Specifies the maximum DRAM data rate that the processor is designed to support. DdrMaxRate is defined by Table 124 [Valid Values for Memory Clock Frequency Value Definition] ; except that 00h is defined as no limit. See D18F2x94_dct[0][MemClkFreq] , and DdrMaxRateEnf.

15:12	DctEn[3:0]: DCT[3:0] enabled. Read-only. Value: ~Fuse[MemChanDis[3:0]]. Specifies which DCT controllers are enabled. 1=Enabled. 0=Disabled. <table border="1"> <thead> <tr> <th>Bit</th><th>Description</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>DCT 0</td></tr> <tr> <td>[3:1]</td><td>Reserved</td></tr> </tbody> </table>	Bit	Description	[0]	DCT 0	[3:1]	Reserved
Bit	Description						
[0]	DCT 0						
[3:1]	Reserved						
11:8	Reserved.						
7:0	CmpCap: CMP capable. Read-only. Value: (Number of physical cores on the node) - 1 - (the number of cores that are disabled by Fuse[CoreDis]). Number of fuse enabled cores on the internal node is CmpCap+1. CmpCap does not reflect cores software disabled by D18F3x190[DisCore] . See 2.4.4 [Processor Cores and Downcoring] .						

D18F5x88 NB Configuration 4 (NB_CFG4)

Bits	Description
24	DisHbNpReqBusLock. Read-write. Reset: 0. BIOS: 1. 0=While bus locks are in progress, all non-posted commands from I/O, including atomics, are blocked until the core has completed the locked transaction and releases the bus. 1=All non-posted commands except atomics do not honor bus locks and are allowed to proceed. This bit may be set to achieve better DMA performance in the presence of bus locks. This bit has no effect if MSRC001_001F[DisHbBusLock] =1.
18	EnCstateBoostBlockCC6Exit. Read-write. Reset: 0. If (EnCstateBoostBlockCC6Exit==1 && MSRC001_001F[DisCstateBoostBlockPstateUp] ==0), cores cannot exit CC6 until VDD is less than or equal to the voltage of the P-state indexed by D18F4x16C[CstateBoost] . This bit must be cleared if CC6PstateLimitMaskDis is set. This bit must be cleared if D18F3x18C[DisC6SptGntExit] is set.
14	DisHldRegRdRspChk. Read-write. Reset: 0. 1=Disable primary holding register CPU or I/O read response checks.
0	CC6PstateWakeUpDis. Read-write. Reset: 0. BIOS: 1. 1=Disable waking up cores in CC6 for P-state changes. 0=Wakeup cores in CC6 for a P-state change to the PopDownPstate, and then return the core to CC6. This is a chicken bit for the case where a core can enter CC6 and not be in the Pop-DownPstate.

D18F5x8C NB Configuration 5 (NB_CFG5)

Bits	Description
15	EnSrqAllocGt31. Read-write. Reset: 0b. BIOS: 1. 1=Enables allocation of SRA entries to above the lower 32 entries.

D18F5xE0 Processor TDP Running Average

Bits	Description
3:0	RunAvgRange: running average range. Read-write; Same-for-all. Reset: 0. BIOS: 1h. Specifies the interval over which the UNB averages power consumption estimates from the cores for boosting. Time interval = $2^{(\text{RunAvgRange} + 1)} * \text{FreeRunSampleTimer}$ rate. A value of 0 disables the TDP running average accumulator capture function. See 2.5.9 [Application Power Management (APM)] and TdpRunAvgAccCap .

D18F5xE8 TDP Limit 3

Bits	Description
31:29	Reserved.
28:16	ApmTdpLimit. Read-only; updated-by-hardware. Value: D18F4x250 [NodeTdpLimit]. If the consumed node power exceeds the ApmTdpLimit on a single node processor or the ApmTdpLimit/2 on a multi-node processor, a P-state limit is applied to all cores on all nodes to reduce the power consumption to remain within the TDP limit. See 2.5.9.2 [TDP Limiting] and MSRC001_0078 [ApmTdpLimit]. See D18F4x16C [ApmlSwTdpLimitEn].
15:10	Tdp2Watt[5:0]. Read-only. Value: 000000b. See Tdp2Watt[15:6]. Read by ucode to produce MSRC001_0077 [Tdp2Watt[5:0]].
9:0	Tdp2Watt[15:6]. Read-only. Value: Fuse[Tdp2Watt]. Specifies in watts/TDP units the conversion factor for converting TDP units to watts. Tdp2Watt[15:0] is a fixed point integer with 16 bits to the right of the decimal point and 0 bits to the left of the decimal point. E.g. Tdp2Watt[15]==0.5 W; Tdp2Watt[6]==0.976 mW; Tdp2Watt[0]==15.2 uW. Read by ucode to produce MSRC001_0077 [Tdp2Watt[15:6]].

D18F5xEC Load Step Throttle Control

Bits	Description
31:0	Reserved.

D18F5x128 Clock Power/Timing Control 3

Bits	Description
30	NbFidChgCpuOpEn. Read-write. Reset: 0b. 1=Explicitly clock gate a core prior to an NB P-state operation.
27	SprSaveRestoreEn. Read-write. Cold Reset:0. Enables SPR save/restore for non-retention NB power gating.
22	NbPllPwrDwnRegEn: NB PLL power down. Read-write. Cold reset: Fuse[NbPllPwrDnRegEn]. 1=The NB PLL is powered down when the NB is power gated and DRAM is placed into self-refresh (see 2.5.4.2 [NB C-states]). 0=The NB PLL is not powered down during NB C-states.
21	PC6Vid[7]. Read-write. Cold reset: Fuse[C6Vid[7]]. See PC6Vid[6:0].
15	CC6PwrDwnRegEn: CC6 power down regulator enable. Read-write. Cold reset: Fuse[CC6PLLpwrDnRegEn]. 1=Power down the VDDA regulator on CC6 entry. If this bit is set to 1, then CC6PwrDwnVcoEn must be 0. See PllRegTime.
14	PC6PwrDwnRegEn: PC6 power down regulator enable. Read-write. Cold reset: Fuse[C6PLLpwrDnRegEn]. 1=Power down the VDDA regulator on PC6 entry. See PllRegTime. Kabini PLL design always powers down regulator during PC6, irrespective of this setting. PC6PwrDwnRegEn=0 has no effect.

13:12	PwrGateTmr: power gate timer. Read-write. Cold reset: 01b. BIOS: Char.Temp.00b. Specifies the minimum delay time required from the power gating or ungating of one Core to the power gating or ungating of the same Core or another Core.												
	<table> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>500 ns</td><td>10b</td><td>Reserved. (5 us)</td></tr> <tr> <td>01b</td><td>1 us</td><td>11b</td><td>Reserved. (10 us)</td></tr> </tbody> </table>	Bits	Description	Bits	Description	00b	500 ns	10b	Reserved. (5 us)	01b	1 us	11b	Reserved. (10 us)
Bits	Description	Bits	Description										
00b	500 ns	10b	Reserved. (5 us)										
01b	1 us	11b	Reserved. (10 us)										
11:10	PLLVddOutUpTime. Read-write. Reset: 0. The VDD regulator may be powered down when the processor transitions to PC6. If the regulator is powered down, this field specifies the time required to initialize the core PLL logic once the regulator is powered back up.												
	<table> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>100 ns</td><td>10b</td><td>400 ns</td></tr> <tr> <td>01b</td><td>200 ns</td><td>11b</td><td>800 ns</td></tr> </tbody> </table>	Bits	Description	Bits	Description	00b	100 ns	10b	400 ns	01b	200 ns	11b	800 ns
Bits	Description	Bits	Description										
00b	100 ns	10b	400 ns										
01b	200 ns	11b	800 ns										
9	FastSlamTimeDown. Read-write. Cold reset: 0. Temp.BIOS: 1. Specifies the time the processor waits for downward voltage transitions to complete. This field only effects transitions from D18F4x16C[CstateBoost] or lower performance P-states. 0= D18F3xD8[VSRampSlamTime] or D18F3xD8[VSSlamTime] , as specified by D18F3xD8[SlamModeSelect] . 1=10 us.												
8:7	PLLRegTime: PLL regulator time. Read-write. Cold reset: 10b. The VDDA regulator may be powered down when the processor transitions to PC6 or CC6. See PC6PwrDwnRegEn and CC6PwrDwnRegEn . If CC6PwrDwnRegEn=1, the VDDA regulator is powered down during CC6. If PC6PwrDwnRegEn=1, the VDDA regulator is powered down during PC6. If the VDDA regulator is powered down during CC6 and the core transitions from CC6 to PC6, the regulator remains powered down during PC6 regardless of the PC6PwrDwnRegEn setting. This field specifies the time required for the VDDA regulator to power back up and initialize the core PLL logic that is powered by the VDDA regulator. The regulator does not support times less than 1.5us.												
	<table> <thead> <tr> <th>Bits</th><th>Description</th><th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>0.5 us</td><td>10b</td><td>1.5 us</td></tr> <tr> <td>01b</td><td>1.0 us</td><td>11b</td><td>2.0 us</td></tr> </tbody> </table>	Bits	Description	Bits	Description	00b	0.5 us	10b	1.5 us	01b	1.0 us	11b	2.0 us
Bits	Description	Bits	Description										
00b	0.5 us	10b	1.5 us										
01b	1.0 us	11b	2.0 us										
6:0	PC6Vid[6:0]: package C6 vid. Read-write. Cold reset: Fuse[C6Vid]. PC6Vid[7:0] = {PC6Vid[7], PC6Vid[6:0]}. PC6Vid[7:0] specifies the VID driven in the PC6 state. See 2.5.3.2.3.4 [Package C6 (PC6) State] and 2.5.1.3.2 [Low Power Voltages] .												

D18F5x12C Clock Power/Timing Control 4

See the *AMD Serial VID Interface 2.0 (SVI2) Specification*.

Bits	Description
31	Svi2CmdBusy. Read-only, updated-by-hardware. Cold reset: 0. 1=SVI2 command in progress. This bit is set by hardware when any SVI2 command is sent to the voltage regulator. Software must wait for this bit to clear to 0 before writing any of the following fields: D18F5x12C[CorePsi1En, CoreLoadLineTrim, CoreOffsetTrim] , D18F5x188[NbPsi1, NbLoadLineTrim, NbOffsetTrim] , D18F5x18C[CoreTfn, NbTfn] . This bit is cleared by hardware when the SVI2 command is complete. On a voltage change, this bit is cleared when the voltage transition is completed. See 2.5.1.4.1 [Hardware-Initiated Voltage Transitions] . On a telemetry or PSIx_L change, this bit is cleared as soon as the SVI2 command is sent to the voltage regulator. See 2.5.1.1.1 [SVI2 Features] and 2.5.1.3.1 [PSIx_L Bit] .

30	WaitVidCompDis: wait VID completion disable. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: 0. 0=Hardware waits for the VOTF complete indicator from the voltage regulator before clearing Svi2CmdBusy or making additional voltage change requests. 1=Hardware clears Svi2CmdBusy 500us after changes to CoreLoadLineTrim, CoreOffsetTrim, or D18F5x188[NbLoadLineTrim, NbOffsetTrim] are made; hardware clears Svi2CmdBusy and additional voltage changes are allowed after the time specified by D18F3xD8[VRampSlamTime] or D18F3xD8[VSSlamTime], as specified by D18F3xD8[SlamModeSelect]. See 2.5.1.4 [Voltage Transitions] .																				
29:6	RAZ.																				
5	CorePsi1En: Core PSI1_L enable. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Cold reset: 0. BIOS: IF (SVI1) THEN 0 ELSE 1 ENDIF. 0=PSI1_L for VDD is deasserted. 1=PSI1_L for VDD is asserted when all cores are in CC6. See 2.5.3.2.3.4 [Package C6 (PC6) State] , 2.5.1.3.1 [PSIx_L Bit] , and Svi2CmdBusy.																				
4:2	CoreLoadLineTrim: Core load line trim. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: 01b. CoreLoadLineTrim and NbLoadLineTrim specify a percentage change relative to the initial load line slope for VDD and VDDNB, respectively. See Svi2CmdBusy. <table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">000b</td> <td>Load line disabled</td> <td style="text-align: center;">100b</td> <td>+20%</td> </tr> <tr> <td style="text-align: center;">001b</td> <td>-40%</td> <td style="text-align: center;">101b</td> <td>+40%</td> </tr> <tr> <td style="text-align: center;">010b</td> <td>-20%</td> <td style="text-align: center;">110b</td> <td>+60%</td> </tr> <tr> <td style="text-align: center;">011b</td> <td>0%</td> <td style="text-align: center;">111b</td> <td>+80%</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>	000b	Load line disabled	100b	+20%	001b	-40%	101b	+40%	010b	-20%	110b	+60%	011b	0%	111b	+80%
<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>																		
000b	Load line disabled	100b	+20%																		
001b	-40%	101b	+40%																		
010b	-20%	110b	+60%																		
011b	0%	111b	+80%																		
1:0	CoreOffsetTrim: Core offset trim. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: 10b. CoreOffsetTrim and NbOffsetTrim specify a voltage offset relative to the initial load line offset for VDD and VDDNB, respectively. See Svi2CmdBusy. <table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>Load line offset disabled</td> <td style="text-align: center;">10b</td> <td>0mV</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>-25mV</td> <td style="text-align: center;">11b</td> <td>+25mV</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	<u>Bits</u>	<u>Description</u>	00b	Load line offset disabled	10b	0mV	01b	-25mV	11b	+25mV								
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00b	Load line offset disabled	10b	0mV																		
01b	-25mV	11b	+25mV																		

D18F5x16[C:0] Northbridge P-state [3:0]

Each of these registers specify the frequency and voltage associated with each of the NB P-states.

Table 176: Register Mapping for D18F5x16[C:0]

Register	Function
D18F5x160	NB P-state 0
D18F5x164	NB P-state 1
D18F5x168	NB P-state 2
D18F5x16C	NB P-state 3

The NbVid field is allowed to be different between processors in a multi-processor system. All other fields are required to be programmed to the same value for all processors in the coherent fabric. See [2.5.4.1 \[NB P-states\]](#) for more information about these registers.

Table 177: NB P-state Definitions

Term	Definition
NBCOF	NB current operating frequency in MHz. NBCOF = 100 * $(D18F5x16[C:0][NbFid] + 4h) / (2^D18F5x16[C:0][NbDid])$.
NBCOF[0]	NB current operating frequency in MHz for NB P-state 0. NBCOF[0] = (100 * (D18F5x160[NbFid] + 4h) / (2^D18F5x160[NbDid])).
NBCOF[1]	NB current operating frequency in MHz for NB P-state 1. NBCOF[1] = (100 * (D18F5x164[NbFid] + 4h) / (2^D18F5x164[NbDid])).
NBCOF[2]	NB current operating frequency in MHz for NB P-state 2. NBCOF[2] = (100 * (D18F5x168[NbFid] + 4h) / (2^D18F5x168[NbDid])).
NBCOF[3]	NB current operating frequency in MHz for NB P-state 3. NBCOF[3] = (100 * (D18F5x16C[NbFid] + 4h) / (2^D18F5x16C[NbDid])).

Bits	Description										
31:24	NbIddValue: northbridge current value. Read-write. Cold reset: Fuse[NbIddValue[3:0][1:0]]. See NbIddDiv.										
23:22	NbIddDiv: northbridge current divisor. Read-write. Cold reset: Fuse[NbIddDiv[3:0][1:0]]. After reset, NbIddDiv and NbIddValue combine to specify the expected maximum current drawn on the VDDNB power plane at a given VDDNB voltage. These values are intended to be used by 2.5.1.3.1.1 [BIOS Requirements for PSIO_L] . These values are not intended to convey final product power levels and may not match the power levels specified in the Power and Thermal Datasheet. These fields may be subsequently altered by software; they do not affect the hardware behavior. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>IddValue / 1 A, Range: 0 to 255 A.</td> </tr> <tr> <td>01b</td> <td>IddValue / 10 A, Range: 0 to 25.5 A.</td> </tr> <tr> <td>10b</td> <td>IddValue / 100 A, Range: 0 to 2.55 A.</td> </tr> <tr> <td>11b</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Description	00b	IddValue / 1 A, Range: 0 to 255 A.	01b	IddValue / 10 A, Range: 0 to 25.5 A.	10b	IddValue / 100 A, Range: 0 to 2.55 A.	11b	Reserved.
Bits	Description										
00b	IddValue / 1 A, Range: 0 to 255 A.										
01b	IddValue / 10 A, Range: 0 to 25.5 A.										
10b	IddValue / 100 A, Range: 0 to 2.55 A.										
11b	Reserved.										
21	NbVid[7]. Read-write. Cold reset: Fuse[NbVid[3:0][7]]. See NbVid[6:0].										
20	Reserved.										
19	Reserved. Reserved for expansion of MemPstate.										
18	MemPstate: Memory P-state. Read-write. Cold reset: Fuse[MemPstate[3:0]]. 1=The Northbridge P-state specified by this register maps to memory P-state 1. 0=The Northbridge P-state specified by this register maps to memory P-state 0. Memory P-states may be globally disabled by programming D18F5x170[MemPstateDis] . See 2.5.7.1 [Memory P-states] .										
17	Reserved.										
16:10	NbVid[6:0]: Northbridge VID. Read-write. Cold reset: Fuse[NbVid[3:0][6:0]]. NbVid[7:0] = {NbVid[7], NbVid[6:0]}. NbVid[7:0] specifies the Northbridge voltage.										
9:8	Reserved.										
7	NbDid: Northbridge divisor ID. Read-write. Cold reset: Fuse[NbDid[3:0]]. Specifies the Northbridge frequency divisor; see NbFid.										

6:1	NbFid[5]: Northbridge frequency ID. Read-write. Cold reset: Fuse[NbFid[3:0][5:0]]. Specifies the Northbridge frequency multiplier. The NB COF is a function of NbFid and NbDid, and defined by NBCOF. NbFid and NbDid are not changed on a write if the value written results in a frequency greater than MSRC001_0071 [MaxNbCof]. See 2.5.3.1.5 [Core P-state Transition Behavior] .
0	NbPstateEn: Northbridge P-state enable. Read-write. Cold reset: Fuse[NbPstateEn[3:0]]. 1=The Northbridge P-state specified by this register is valid. 0=The Northbridge P-state specified by this register is not valid. This bit must be set to 1 in order for the Northbridge P-state specified by this register to be programmed in D18F5x170 [NbPstateHi, NbPstateLo]. This bit controls hardware and is used to qualify the values written in D18F5x170 [NbPstateHi, NbPstateLo].

D18F5x170 Northbridge P-state Control

See also [2.5.4.1 \[NB P-states\]](#).

Bits	Description																				
31	MemPstateDis: memory P-state disable. IF (D18F3xE8 [MemPstateCap] && D18F2x1B4 [SmuCfgLock]==0) THEN Read-write, updated-by-hardware; Updated-by-SMU. ELSE Read-only, updated-by-hardware; Updated-by-SMU. Reset: Fuse[MemPstateDis]. 1=Memory P-state transitions are disabled. The current P-state is not changed by programming this bit. The memory P-state will be forced to M0 on the next NB P-state transition. On processors where memory P-states are enabled, programming this bit may result in a violation of bandwidth requirements stated in 2.5.3.1.5 (M0.MemClk-Freq>NBCOF). Software must ensure that NB P-states which violate those requirements are forced disabled. 0=Memory P-state transitions are enabled if D18F2x90_dct[0] [DisDllShutdownSR]=0.																				
30	NbPstateFidVidSbcEn. IF (D18F5x174 [NbPstateDis] D18F2x1B4 [SmuCfgLock]) THEN Read-only. ELSE Read: Write-1-only. ENDIF. Reset: 0. BIOS: 1. NB P-state transitions are blocked until this field is set to a 1. This field should only be set when all APs are launched.																				
29:27	NbPstateHiRes: NB P-state high residency timer. If D18F2x1B4 [SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. Specifies the minimum time the processor must spend in the high NB P-state before transitions to the low NB P-state are allowed. See 2.5.4.1 [NB P-states] . <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0us</td> <td>100b</td> <td>1ms</td> </tr> <tr> <td>001b</td> <td>10us</td> <td>101b</td> <td>5ms</td> </tr> <tr> <td>010b</td> <td>100us</td> <td>110b</td> <td>10ms</td> </tr> <tr> <td>011b</td> <td>500us</td> <td>111b</td> <td>50ms</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	000b	0us	100b	1ms	001b	10us	101b	5ms	010b	100us	110b	10ms	011b	500us	111b	50ms
Bits	Description	Bits	Description																		
000b	0us	100b	1ms																		
001b	10us	101b	5ms																		
010b	100us	110b	10ms																		
011b	500us	111b	50ms																		
26:24	NbPstateLoRes: NB P-state low residency timer. If D18F2x1B4 [SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. Specifies the minimum time the processor must spend in the low NB P-state before transitions to the high NB P-state are allowed. See 2.5.4.1 [NB P-states] . See: NbPstateHiRes.																				
23	NbPstateGnbSlowDis. If D18F2x1B4 [SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: 0. Specifies whether NBP-state transitions take the Gnb-Slow signal into account. 0=Take GnbSlow into account. 1=Ignore GnbSlow. See 2.5.4.1 [NB P-states] .																				
14	SwNbPstateLoDis: software NB P-state low disable. IF (D18F5x174 [NbPstateDis] D18F2x1B4 [SmuCfgLock]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=Transition to NbPstateHi and disable transitions to NbPstateLo.																				

13	NbPstateDisOnP0: NB P-state disable on P0. IF (D18F5x174[NbPstateDis] D18F2x1B4[SmuCfgLock]) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=Transition to NbPstateHi and disable transitions to NbPstateLo if any compute unit is in P0 or a boosted P-state. This field uses software P-state numbering. See 2.5.3.1.1.1 [Software P-state Numbering] .
12:9	NbPstateThreshold: NB P-state threshold. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Reset: COUNT(D18F5x80[Enabled]). Char.Temp.BIOS: COUNT(D18F5x80[Enabled]). Specifies the minimum number of compute units that must be in a P-state with MSRC001_00[6B:64] [NbPstate]=1 before transitions to lower performance NB P-states are allowed. See NbPstateLo and NbPstateHi.
8	Reserved. Reserved for future expansion of NbPstateHi.
7:6	NbPstateHi: NB P-state high. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: Fuse[NbPstateHi]. If NB P-states are enabled, this field specifies the NB P-state that is used when the number of compute units in a P-state with MSRC001_00[6B:64] [NbPstate]=1 is less than NbPstateThreshold. This field must be programmed to the same value for all processors in the coherent fabric. This field is not changed on a write if the value written is greater than the NbPstateMaxVal value written or greater than the current NbPstateLo value. See also NbPstateDisOnP0, SwNbPstateLoDis, NbPstateLo, D18F5x174[NbPstateDis] , and D18F5x16[C:0][NbPstateEn] .
5	Reserved.
4:3	NbPstateLo: NB P-state low. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: Fuse[NbPstateLo]. If NB P-states are enabled, this field specifies the NB P-state that is used when the number of compute units in a P-state with MSRC001_00[6B:64] [NbPstate]=1 is greater than or equal to NbPstateThreshold. NbPstateLo must be greater than or equal to NbPstateHi. This field must be programmed to the same value for all processors in the coherent fabric. This field is not changed on a write if the value written is greater than the NbPstateMaxVal value written or less than the current NbPstateHi value. See also NbPstateDisOnP0, SwNbPstateLoDis, D18F5x174[NbPstateDis] , and D18F5x16[C:0][NbPstateEn] .
2	Reserved.
1:0	NbPstateMaxVal: NB P-state maximum value. IF (D18F2x1B4[SmuCfgLock]) THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: specified by the reset state of D18F5x16[C:0][NbPstateEn] ; the cold reset value is the highest NB P-state number corresponding to the register in which NbPstateEn is set (e.g., if D18F5x160 and D18F5x164 have this bit set and the others do not, then NbPstateMaxVal=1; if NbPstateEn is only set in D18F5x160, then NbPstateMaxVal=0). This specifies the highest NB P-state value (lowest performance state) supported by the hardware.

D18F5x174 Northbridge P-state Status

Bits	Description
24	CurMemPstate: current memory P-state. Read-only; updated-by-hardware. Reset: 0. Specifies the current memory P-state. 1=Memory P-state 1. 0=Memory P-state 0. See 2.5.7.1 [Memory P-states] .
23	CurNbVid[7]: current northbridge voltage ID[7]. MSRC001_0071 [CurNbVid[7]] is an alias of D18F5x174[CurNbVid[7]] . VDDNB voltage.
22	CurNbPstateLo. Read-only; updated-by-hardware. Reset: 0. 1=Current NB Pstate maps to D18F5x170[NbPstateLo] . 0=Current NB Pstate maps to D18F5x170[NbPstateHi] .
21	Reserved.

20:19	CurNbPstate: current northbridge P-state. Read-only; updated-by-hardware. Reset: 0. Provides the NB P-state that corresponds to the current frequency component of the NB. The value of this field is updated when the COF transitions to a new value associated with an NB P-state.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td><td>NB P0</td></tr> <tr> <td style="text-align: center;">01b</td><td>NB P1</td></tr> <tr> <td style="text-align: center;">10b</td><td>NB P2</td></tr> <tr> <td style="text-align: center;">11b</td><td>NB P3</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	NB P0	01b	NB P1	10b	NB P2	11b	NB P3
<u>Bits</u>	<u>Description</u>										
00b	NB P0										
01b	NB P1										
10b	NB P2										
11b	NB P3										
18:12	CurNbVid[6:0]: current northbridge voltage ID. MSRC001_0071 [CurNbVid[6:0]] is an alias of D18F5x174 [CurNbVid[6:0]]. VDDNB voltage.										
11	Reserved.										
10	Reserved.										
9	CurNbDid: current northbridge divisor ID. Read-only, updated-by-hardware. Reset: 0.										
8:3	CurNbFid[5:0]: current northbridge frequency ID. Read-only, updated-by-hardware. Reset: 0.										
2:1	StartupNbPstate: startup northbridge P-state number. Read-only. Cold reset: Fuse[StartupNbPstate]. Specifies the cold reset VID, FID and DID for the Northbridge based on the NB P-state number selected. If D18F3xA0 [CofVidProg]=0, then the state of this field is ignored and the VID, FID and DID are applied to the NB as specified by that bit. Hardware verifies that D18F5x16[C:0] [NbVid, NbFid, NbDid] for the NB P-state pointed to by StartupNbPstate are programmed as specified by MSRC001_0071 [MaxNbCof]. Hardware does not verify that NbPstateEn is set.										
0	NbPstateDis: northbridge P-state disable. Read-only. Value: Fuse[NbPstateDis]. MSRC001_0071 [NbPstateDis] is an alias of D18F5x174 [NbPstateDis].										

D18F5x178 Northbridge Fusion Configuration

Bits	Description
19	SwGfxDis. Read-write. Reset: 1. BIOS: IF (GpuEnabled) THEN 0 ELSE 1 ENDIF. 1=Hardware handshakes for NB P-state transitions and DRAM self-refresh entry are ignored. See 2.5.4.1.1 [NB P-state Transitions] . See 2.5.7.2 [DRAM Self-Refresh] . Causes UNB to ignore AllowSelfRefresh, AllowNbTrans, ForceNbPs1, GnbSlow, and garlic flush.
18	CstateFusionHsDis: C-state fusion handshake disable. Read-write. Reset: 0. BIOS: 1. 1=Ignore the FCH handshake response for PC6 transitions. 0=Use the FCH handshake response for PC6 entry. See 2.5.3.2.4.1 [FCH Messaging] .
17	Dis2ndGnbAllowPsWait. Read-write. Reset: 0. BIOS: 1. 1=Do not do a second check of AllowNbTrans after quiescing the cores when transitioning NB P-states. See 2.5.4.1.1 [NB P-state Transitions] .
16	ProcHotToGnbEn. Read-write. Reset: 0. BIOS: 1. Specifies whether PROCHOT_L is distributed to GNB. See Figure 44 .
11	AllowSelfRefrS3Dis: allow self-refresh S3 disable. Read-write. Reset: 0. BIOS: 1. 1=The NB does not wait for AllowSelfRefresh assertion before placing DRAM into self-refresh (see 2.5.7.2 [DRAM Self-Refresh]) on S3 entry (see 2.5.8.1.1 [ACPI Suspend to RAM State (S3)]). 0=The NB waits for AllowSelfRefresh assertion before placing DRAM into self-refresh on S3 entry.

10	InbWakeS3Dis: InbWake S3 disable. Read-write. Reset: 0. BIOS: 1. 1= The NB does not wait for InbWake de-assertion before placing DRAM into self-refresh (see 2.5.7.2 [DRAM Self-Refresh]) on S3 entry (see 2.5.8.1.1 [ACPI Suspend to RAM State (S3)]). 0=The NB waits for InbWake de-assertion before placing DRAM into self-refresh on S3 entry.
3	CstateThreeWayHsEn: C-state three way handshake disable. Read-write. Reset: 0. 1=Enable the three way handshake with the FCH when entering a C-state. 0=Only a two way handshake with FCH is used. There is no message about the resulting package state sent to FCH. See 2.5.3.2.4.1 [FCH Messaging] .
2	CstateFusionDis: C-state fusion disable. Read-write. Reset: 0. 1>All HALT or C-state requests are forwarded to the FCH. 0=HALT and C-state requests are forwarded to the FCH when each core has made a request. See 2.5.3.2.4.1 [FCH Messaging] .

D18F5x17C Miscellaneous Voltages

Bits	Description
31	NbPsi0VidEn: Northbridge PSIO_L VID enable. Read-write. Reset: 0. This bit specifies how PSIO_L is controlled for VDDNB. See D18F3xA0[PsiVidEn] and 2.5.1.3.1 [PSIx_L Bit] .
30:23	NbPsi0Vid[7:0]: Northbridge PSIO_L VID threshold. Read-write. Reset: 0. When enabled by NbPsi0VidEn, NbPsi0Vid specifies the threshold value of the VID code generated by the Northbridge, which in turn determines the state of PSIO_L. See D18F3xA0[PsiVid[6:0]] and 2.5.1.3.1 [PSIx_L Bit] .
22:18	Reserved.
17:10	MinVid: minimum voltage. Read-only. Reset: Fuse[MinVid]. Specifies the VID code corresponding to the minimum voltage (highest VID code) that the processor drives. 00h indicates that no minimum VID code is specified. See 2.5.1 [Processor Power Planes And Voltage Control] .
9:8	Reserved.
7:0	MaxVid: maximum voltage. Read-only. Reset: Fuse[MaxVid]. Specifies the VID code corresponding to the maximum voltage (lowest VID code) that the processor drives. 00h indicates that no maximum VID code is specified. See 2.5.1 [Processor Power Planes And Voltage Control] .

D18F5x188 Clock Power/Timing Control 5

See the *AMD Serial VID Interface 2.0 (SVI2) Specification*.

Bits	Description
31:6	RAZ.
5	NbPsi1: Northbridge PSI1_L. IF D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Cold reset: 0. Specifies how PSI1_L is controlled for VDDNB. 1=PSI1_L is low. 0=PSI1_L is high. See 2.5.1.3.1 [PSIx_L Bit] .
4:2	NbLoadLineTrim: Northbridge load line trim. IF D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Cold reset: 011b. See D18F5x12C[CoreLoadLineTrim] .
1:0	NbOffsetTrim: Northbridge offset trim. IF D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. ELSE Read-write. ENDIF. Cold reset: 10b. See D18F5x12C[CoreOffsetTrim] .

D18F5x18C Clock Power/Timing Control 6

See the *AMD Serial VID Interface 2.0 (SVI2) Specification*.

Bits	Description															
31:2	RAZ. Reserved for expansion of Clock Power/Timing Control.															
1	CoreTfn: Core telemetry functionality. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF Cold reset: 0. See NbTfn.															
0	NbTfn: Northbridge telemetry functionality. If D18F2x1B4[SmuCfgLock] THEN Read-only; updated-by-hardware. (SMU) ELSE Read-write. ENDIF. Cold reset: 0. See D18F5x12C[Svi2CmdBusy]. CoreTfn and NbTfn specify the telemetry mode as follows:															
	<table> <thead> <tr> <th>CoreTfn</th> <th>NbTfn</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Telemetry enabled in voltage-only mode.</td> </tr> <tr> <td>0</td> <td>1</td> <td>Telemetry enabled in voltage and current mode.</td> </tr> <tr> <td>1</td> <td>0</td> <td>Telemetry disabled.</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved.</td> </tr> </tbody> </table>	CoreTfn	NbTfn	Description	0	0	Telemetry enabled in voltage-only mode.	0	1	Telemetry enabled in voltage and current mode.	1	0	Telemetry disabled.	1	1	Reserved.
CoreTfn	NbTfn	Description														
0	0	Telemetry enabled in voltage-only mode.														
0	1	Telemetry enabled in voltage and current mode.														
1	0	Telemetry disabled.														
1	1	Reserved.														

D18F5x194 Name String Address Port

D18F5x194 and D18F5x198 provide BIOS with a read-only (Fused) name string that may be copied to MSRC001_00[35:30] at warm reset. Each of D18F5x198_x[B:0] is read as follows:

1. Write D18F5x194[Index].
2. Read D18F5x198.

Bits	Description						
31:4	Reserved.						
3:0	Index: name string register index. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>Bh-0h</td> <td>Name String Registers. See D18F5x198_x[B:0].</td> </tr> <tr> <td>Fh-Ch</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	Bh-0h	Name String Registers. See D18F5x198_x[B:0].	Fh-Ch	Reserved
Bits	Description						
Bh-0h	Name String Registers. See D18F5x198_x[B:0].						
Fh-Ch	Reserved						

D18F5x198 Name String Data Port

See D18F5x194 for register access information. Address: D18F5x194[Index].

Bits	Description
31:0	Data.

D18F5x198_x[B:0] Name String Data

Bits	Description
31:24	NameStringByte3: name string ASCII character 3. Read-only. Value: Table 1188.
23:16	NameStringByte2: name string ASCII character 2. Read-only. Value: Table 1188.
15:8	NameStringByte1: name string ASCII character 1. Read-only. Value: Table 1188.
7:0	NameStringByte0: name string ASCII character 0. Read-only. Value: Table 1188.

D18F5x240 ECC Exclusion Base Address Low

- Transaction addresses are within the defined range if:
 $\{EccExclBaseAddr[47:6], 00_0000b\} \leq address[47:0] \leq \{EccExclLimitAddr[47:6], 00_0000b\}$.
- BIOS must quiesce all other forms of DRAM traffic when configuring this range. See [MSRC001_001F](#)[Dis-DramScrub].
- When initializing the base/limit pair, the BIOS must write the limit register before the EccExclEn bit is set. BIOS should clear EccExclEn before changing the address range.
- BIOS should take care to re-initialize memory with valid ECC when resizing this region.

Bits	Description
31:6	EccExclBaseAddr[31:6]: ECC exclusion base address register bits[31:6] . Read-write. Reset: 0. EccExclBaseAddr[47:6]={ D18F5x244 [EccExclBaseAddr[47:32]], EccExclBaseAddr[31:6]}. The ECC Exclusion Base/Limit Address registers setup a contiguous range in DRAM where ECC check and error reporting is disabled. BIOS configures the ECC exclusion range code to cover the frame buffer region in ECC UMA systems with internal GPUs. The GPU is configured as MC_SHARED:MC_VM_STEERING [DEFAULT_STEERING]=1 (system traffic to onion).
5:1	Reserved.
0	EccExclEn . Read-write. Reset: 0. 1=Enable ECC Exclusion Range. See D18F5x240 [EccExclBase-Addr].

D18F5x244 ECC Exclusion Base Address High

Bits	Description
31:16	Reserved.
15:0	EccExclBaseAddr[47:32]: ECC exclusion base address register bits[47:32] . Read-write. Reset: 0. See D18F5x240 [EccExclBaseAddr].

D18F5x248 ECC Exclusion Limit Address Low

Bits	Description
31:6	EccExclLimitAddr[31:6]: ECC exclusion limit address register bits[31:6] . Read-write. Reset: 0. EccExclLimitAddr[47:6]={ D18F5x24C [EccExclLimitAddr[47:32]], EccExclLimitAddr[31:6]}. See D18F5x240 [EccExclBaseAddr].
5:0	Reserved.

D18F5x24C ECC Exclusion Limit Address High

Bits	Description
31:16	Reserved.
15:0	EccExclLimitAddr[47:32]: ECC exclusion limit address register bits[47:32] . Read-write. Reset: 0. See D18F5x240 [EccExclBaseAddr].

D18F5x260 Clock Power/Timing Control 8

Bits	Description
31:4	Reserved.
3:0	Reserved.

3.15 GPU Memory Mapped Registers

3.16 Northbridge IOAPIC Registers

The Northbridge IOAPIC is accessed through the Northbridge IOAPIC base address specified by [D0F0xFC_x01 \[IOAPIC Base Address Lower\]](#) and [D0F0xFC_x02 \[IOAPIC Base Address Upper\]](#).

NBIOAPICx00 IO Register Select

Bits	Description
31:8	Reserved.
7:0	IndirectAddressOffset. Read-write. Reset: 0. Specifies the indexed register accessed via NBIOAPICx10 [IO Window] .

NBIOAPICx10 IO Window

Bits	Description
31:0	IoapicData.

NBIOAPICx10_x00 IOAPIC ID

This register is not used in IOxAPIC PCI bus delivery mode.

Bits	Description
31:28	ExtendID: extended IOAPIC device ID. IF (D0F0xFC_x00[IoapicIdExtEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0.
27:24	ID: IOAPIC device ID. Read-write. Reset: 0.
23:0	Reserved.

NBIOAPICx10_x01 IOAPIC Version

Bits	Description
31:24	Reserved.
23:16	MaxRedirectionEntries. Value: 1Fh. Indicates 32 entries [31:0].
15	PRQ. Value: 1. IRQ pin assertion supported
14:8	Reserved.
7:0	Version. Value: 21h. PCI 2.2 compliant

NBIOAPICx10_x02 IOAPIC Arbitration

Bits	Description
31:28	Reserved.

27:24	ArbitrationID . Read-only. Reset: 0.
23:0	Reserved.

NBIOAPICx10_x[4E:10:step2] Redirection Table Entry [31:0]

Bits	Description																				
63:56	DestinationID . Read-write. Reset: 0. Bits [19:12] of the address field of the interrupt message.																				
55:32	Reserved.																				
31:17	Reserved.																				
16	Mask . Read-write. Reset: 1. 1=Mask the interrupt injection at the input of this device. 0=Unmask.																				
15	TriggerMode . Read-write. Reset: 0. 0=Edge. 1=Level																				
14	RemoteIRR . Read-only. Reset: 0. Used for level triggered interrupts only. It is cleared by EOI special cycle transaction or write to EOI register. 1=Interrupt message is delivered.																				
13	InterruptPinPolarity . Read-write. Reset: 0. 0=High. 1=Low.																				
12	DeliveryStatus . Read-only. Reset: 0. 0=Idle. 1=Send Pending.																				
11	DestinationMode . Read-write. Reset: 0. 0=Physical. 1=Logical																				
10:8	DeliveryMode . Read-write. Reset: 0. <table border="0"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>000b</td> <td>Fixed</td> <td>100b</td> <td>NMI</td> </tr> <tr> <td>001b</td> <td>Lowest Priority</td> <td>101b</td> <td>INIT</td> </tr> <tr> <td>010b</td> <td>SMI/PMI</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>Reserved</td> <td>111b</td> <td>ExtINT</td> </tr> </table>	Bits	Definition	Bits	Definition	000b	Fixed	100b	NMI	001b	Lowest Priority	101b	INIT	010b	SMI/PMI	110b	Reserved	011b	Reserved	111b	ExtINT
Bits	Definition	Bits	Definition																		
000b	Fixed	100b	NMI																		
001b	Lowest Priority	101b	INIT																		
010b	SMI/PMI	110b	Reserved																		
011b	Reserved	111b	ExtINT																		
7:0	Vector . Read-write. Reset: 0. Interrupt vector associated with this interrupt input																				

NBIOAPICx20 IRQ Pin Assertion

Bits	Description
31:8	Reserved.
7:0	InputIRQ . Read-write. Reset: 0. IRQ number for the requested interrupt. A write to this register will trigger an interrupt associated with the redirection table entry referenced by the IRQ number. Currently the redirection table has 24 entries. Writes with IRQ number greater than 17h have no effect.

NBIOAPICx40 EOI

Bits	Description
31:8	Reserved.
7:0	Vector . Write-only. Reset: 0. Interrupt vector. A write to this register will clear the remote IRR bit in the redirection table entry found matching the interrupt vector. This provides an alternate mechanism other than PCI special cycle for EOI to reach IOxAPIC.

3.17 APIC Registers

See [2.4.8.1.2 \[APIC Register Space\]](#).

MMIO local APIC space is accessible in xAPIC mode.

APIC20 APIC ID

Bits	Description
31:24	ApicId: APIC ID. Read-write. Reset: Varies based on core number. • The initial value of APIC20[ApicId[7:0]] is {0000b, CpuCoreNum[3:0]}. See 2.4.8.1.3 [ApicId Enumeration Requirements] . See 2.4.4 [Processor Cores and Downcoring] . Intel defines as Read-only on some processors.
23:0	Reserved.

APIC30 APIC Version

Bits	Description
31	ExtApicSpace: extended APIC register space present. Read-only. Reset: 1. 1=Indicates the presence of extended APIC register space starting at APIC400 . Reserved on Intel processors.
30:25	RAZ.
24	DirectedEoiSupport: directed EOI support. Read-only. Reset: 0. 0=Directed EOI capability not supported.
23:16	MaxLvtEntry. Read-only. Reset: IF (Fuse[HtcDis] MSRC001_001F[DisApicThermLVT]) THEN 04h ELSE 05h ENDIF. Specifies the number of entries in the local vector table minus one.
15:8	RAZ.
7:0	Version. Read-only. Reset: 10h. Indicates the version number of this APIC implementation.

APIC80 Task Priority (TPR)

Bits	Description
31:8	RAZ.
7:0	Priority. Read-write. Reset: 0. This field is assigned by software to set a threshold priority at which the core is interrupted.

APIC90 Arbitration Priority (APR)

Bits	Description
31:8	RAZ.
7:0	Priority. Read-only. Reset: 0. Indicates the current priority for a pending interrupt, or a task or interrupt being serviced by the core. The priority is used to arbitrate between cores to determine which accepts a lowest-priority interrupt request.

APICA0 Processor Priority (PPR)

Bits	Description
31:8	RAZ.
7:0	Priority. Reset: 0. Read-only. Indicates the core's current priority servicing a task or interrupt, and is used to determine if any pending interrupts should be serviced. It is the higher value of the task priority value and the current highest in-service interrupt.

APICB0 End of Interrupt

This register is written by the software interrupt handler to indicate the servicing of the current interrupt is complete.

Bits	Description
31:0	Unused. Write-only.

APICC0 Remote Read

Bits	Description
31:0	RemoteReadData. Read-only. Reset: 0. The data resulting from a valid completion of a remote read inter-processor interrupt.

APICD0 Logical Destination (LDR)

Bits	Description
31:24	Destination. Read-write. Reset: 0. This APIC's destination identification. Used to determine which interrupts should be accepted.
23:0	Reserved.

APICE0 Destination Format

Only supported in xAPIC mode.

Bits	Description								
31:28	Format. Read-write. Reset: Fh. Controls which format to use when accepting interrupts with a logical destination mode. <table border="0" style="margin-left: 20px;"> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> <tr> <td>0h</td> <td>Cluster destinations are used</td> </tr> <tr> <td>Eh-1h</td> <td>Reserved</td> </tr> <tr> <td>Fh</td> <td>Flat destinations are used</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	0h	Cluster destinations are used	Eh-1h	Reserved	Fh	Flat destinations are used
<u>Bits</u>	<u>Definition</u>								
0h	Cluster destinations are used								
Eh-1h	Reserved								
Fh	Flat destinations are used								
27:0	Reserved. Reset: FFF_FFFFh.								

APICF0 Spurious-Interrupt Vector (SVR)

Bits	Description
31:13	RAZ.
12	EoiBroadcastDisable: EOI broadcast disable. Read-only. Reset: 0. AMD-specific: Added by Intel with x2APIC, not added by AMD.
11:10	RAZ.
9	FocusDisable. Read-write. Reset: 0. 1=Disable focus core checking during lowest-priority arbitrated interrupts. AMD-specific: Deprecated by Intel with x2APIC, not deprecated by AMD.
8	APICSWEn: APIC software enable. Read-write. Reset: 0. 0=SMI, NMI, INIT, LINT[1:0], and Startup interrupts may be accepted; pending interrupts in APIC[170:100] and APIC[270:200] are held, but further fixed, lowest-priority, and ExtInt interrupts are not accepted. All LVT entry mask bits are set and cannot be cleared. See MSRC001_001F[DisApicSwEnFix] .
7:0	Vector. Read-write. Reset: FFh. The vector that is sent to the core in the event of a spurious interrupt. The behavior of bits 3:0 are controlled as specified by D18F0x68[ApicExtSpur] .

APIC[170:100] In-Service (ISR)

The in-service registers provide a bit per interrupt to indicate that the corresponding interrupt is being serviced by the core. APIC100[15:0] are reserved. Interrupts are mapped as follows:

Table 178: Register Mapping for APIC[170:100]

Register	Function
APIC100	Interrupts [31:16]
APIC110	Interrupts [63:32]
APIC120	Interrupts [95:64]
APIC130	Interrupts [127:96]
APIC140	Interrupts [159:128]
APIC150	Interrupts [191:160]
APIC160	Interrupts [223:192]
APIC170	Interrupts [255:224]

Bits	Description
31:0	InServiceBits. Reset: 0. Read-only. These bits are set when the corresponding interrupt is being serviced by the core.

APIC[1F0:180] Trigger Mode (TMR)

The trigger mode registers provide a bit per interrupt to indicate the assertion mode of each interrupt. APIC180[15:0] are reserved. Interrupts are mapped as follows:

Table 179: Register Mapping for APIC[1F0:180]

Register	Function
APIC180	Interrupts [31:16]
APIC190	Interrupts [63:32]
APIC1A0	Interrupts [95:64]
APIC1B0	Interrupts [127:96]
APIC1C0	Interrupts [159:128]
APIC1D0	Interrupts [191:160]
APIC1E0	Interrupts [223:192]
APIC1F0	Interrupts [255:224]

Bits	Description
31:0	TriggerModeBits. Reset: 0. Read-only. The corresponding trigger mode bit is updated when an interrupt is accepted. The values are: 0=Edge-triggered interrupt. 1=Level-triggered interrupt.

APIC[270:200] Interrupt Request (IRR)

The interrupt request registers provide a bit per interrupt to indicate that the corresponding interrupt has been accepted by the APIC. APIC200[15:0] are reserved. Interrupts are mapped as follows:

Table 180: Register Mapping for APIC[270:200]

Register	Function
APIC200	Interrupts [31:16]
APIC210	Interrupts [63:32]
APIC220	Interrupts [95:64]
APIC230	Interrupts [127:96]
APIC240	Interrupts [159:128]
APIC250	Interrupts [191:160]
APIC260	Interrupts [223:192]
APIC270	Interrupts [255:224]

Bits	Description
31:0	RequestBits. Read-only. Reset: 0. The corresponding request bit is set when the an interrupt is accepted by the APIC.

APIC280 Error Status

Writes to this register trigger an update of the register state. The value written by software is arbitrary. Each write causes the internal error state to be loaded into this register, clearing the internal error state. Consequently, a second write prior to the occurrence of another error causes the register to be overwritten with cleared data.

Bits	Description
31:8	RAZ.

7	IllegalRegAddr: illegal register address. Read-write. Reset: 0. This bit indicates that an access to a nonexistent register location within this APIC was attempted. Can only be set in xAPIC mode. Illegal register accesses in x2APIC mode cause #GP fault.
6	RevdIllegalVector: received illegal vector. Read-write. Reset: 0. This bit indicates that this APIC has received a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts).
5	SentIllegalVector. Read-write. Reset: 0. This bit indicates that this APIC attempted to send a message with an illegal vector (00h to 0Fh for fixed and lowest priority interrupts).
4	RAZ. Intel defined as Redirectable IPI. Intel dropped redirectable IPI with the addition of x2APIC. Redirectable not deprecated by AMD.
3	RevAcceptError: receive accept error. Read-write. Reset: 0. This bit indicates that a message received by this APIC was not accepted by this or any other APIC. AMD-specific: Deprecated by Intel with x2APIC, not deprecated by AMD.
2	SendAcceptError. Read-write. Reset: 0. This bit indicates that a message sent by this APIC was not accepted by any APIC. AMD-specific: Deprecated by Intel with x2APIC, not deprecated by AMD.
1:0	RAZ. [1]: Previously defined as Receive Checksum Error. Only used by 3-wire interface. [0]: Previously defined as Send Checksum Error. Only used by 3-wire interface.

APIC300 Interrupt Command Low (ICR Low)

Not all combinations of ICR fields are valid. Only the following combinations are valid:

Table 181: ICR valid combinations

Message Type	Trigger Mode	Level	Destination Shorthand
Fixed	Edge	x	x
	Level	Assert	x
Lowest Priority, SMI, NMI, INIT	Edge	x	Destination or all excluding self.
	Level	Assert	Destination or all excluding self
Startup	x	x	Destination or all excluding self

Note: x indicates a don't care.

Bits	Description
31:20	RAZ.

19:18	<p>DestShrthnd: destination shorthand. Read-write. Reset: 0. Provides a quick way to specify a destination for a message.</p> <table border="0"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>No shorthand (Destination field)</td></tr> <tr> <td>01b</td><td>Self</td></tr> <tr> <td>10b</td><td>All including self</td></tr> <tr> <td>11b</td><td>All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)</td></tr> </tbody> </table> <p>If all including self or all excluding self is used, then destination mode is ignored and physical is automatically used.</p>	Bits	Description	00b	No shorthand (Destination field)	01b	Self	10b	All including self	11b	All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)								
Bits	Description																		
00b	No shorthand (Destination field)																		
01b	Self																		
10b	All including self																		
11b	All excluding self (This sends a message with a destination encoding of all 1s, so if lowest priority is used the message could end up being reflected back to this APIC.)																		
17:16	<p>RemoteRdStat: remote read status. Read-only. Reset: 0. Deprecated by Intel.</p> <table border="0"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Read was invalid</td></tr> <tr> <td>01b</td><td>Delivery pending</td></tr> <tr> <td>10b</td><td>Delivery complete and access was valid</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	00b	Read was invalid	01b	Delivery pending	10b	Delivery complete and access was valid	11b	Reserved								
Bits	Description																		
00b	Read was invalid																		
01b	Delivery pending																		
10b	Delivery complete and access was valid																		
11b	Reserved																		
15	<p>TM: trigger mode. Read-write. Reset: 0. Indicates how this interrupt is triggered. 0=Edge triggered. 1=Level triggered.</p>																		
14	<p>Level. Read-write. Reset: 0. 0=Deasserted. 1=Asserted.</p>																		
13	<p>RAZ.</p>																		
12	<p>DS: interrupt delivery status. Read-only. Reset: 0. In xAPIC mode this bit is set to indicate that the interrupt has not yet been accepted by the destination core(s). 0=Idle. 1=Send pending. Reserved in x2APIC mode. Software may repeatedly write ICRL without polling the DS bit; all requested IPIs will be delivered.</p>																		
11	<p>DM: destination mode. Read-write. Reset: 0. 0=Physical. 1=Logical.</p>																		
10:8	<p>MsgType. Read-write. Reset: 0. The message types are encoded as follows:</p> <table border="0"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Fixed</td></tr> <tr> <td>001b</td><td>Lowest Priority. Deprecated by Intel with x2APIC.</td></tr> <tr> <td>010b</td><td>SMI</td></tr> <tr> <td>011b</td><td>Remote read. Deprecated by Intel with x2APIC.</td></tr> <tr> <td>100b</td><td>NMI</td></tr> <tr> <td>101b</td><td>INIT</td></tr> <tr> <td>110b</td><td>Startup</td></tr> <tr> <td>111b</td><td>External interrupt. Deprecated by Intel with x2APIC.</td></tr> </tbody> </table>	Bits	Description	000b	Fixed	001b	Lowest Priority. Deprecated by Intel with x2APIC.	010b	SMI	011b	Remote read. Deprecated by Intel with x2APIC.	100b	NMI	101b	INIT	110b	Startup	111b	External interrupt. Deprecated by Intel with x2APIC.
Bits	Description																		
000b	Fixed																		
001b	Lowest Priority. Deprecated by Intel with x2APIC.																		
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011b	Remote read. Deprecated by Intel with x2APIC.																		
100b	NMI																		
101b	INIT																		
110b	Startup																		
111b	External interrupt. Deprecated by Intel with x2APIC.																		
7:0	<p>Vector. Read-write. Reset: 0. The vector that is sent for this interrupt source.</p>																		

APIC310 Interrupt Command High (ICR High)

Bits	Description
31:24	<p>DestinationField. Read-write. Reset: 0. The destination encoding used when APIC300[DestShrthnd] is 00b.</p>
23:0	<p>RAZ.</p>

APIC320 LVT Timer

Bits	Description
31:18	RAZ.
17	Mode. Read-write. Reset: 0. 0=One-shot. 1=Periodic.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	RAZ.
12	DS: interrupt delivery status. Read-only; updated-by-hardware. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. Read-write. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APIC330 LVT Thermal Sensor

Interrupts for this local vector table are caused by changes in [MSRC001_0061](#)[CurPstateLimit] due to SB-RMI or HTC. This register is accessible if (([MSRC001_001F](#)[DisApicThermLVT]==0) && (FUSE[HtcDis]==0)).

Bits	Description
31:17	RAZ.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	RAZ.
12	DS: interrupt delivery status. Read-only; updated-by-hardware. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. Read-write. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APIC340 LVT Performance Monitor

Interrupts for this local vector table are caused by overflows of:

- [MSRC001_00\[07:04\]](#) [Performance Event Counter (PERF_CTR[3:0])].
- [MSRC001_024\[7,5,3,1\]](#) [Northbridge Performance Event Counter (NB_PERF_CTR[3:0])].

Bits	Description
31:17	RAZ.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	RAZ.
12	DS: interrupt delivery status. Read-only; updated-by-hardware. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. Read-write. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APIC3[60:50] LVT LINT[1:0]

Table 182: Register Mapping for APIC3[60:50]

Register	Function
APIC350	LINT 0
APIC360	LINT 1

Bits	Description
31:17	RAZ.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15	TM: trigger mode. Read-write. Reset: 0. 0=Edge. 1=Level.
14	RmtIRR. Read-only; updated-by-hardware. Reset: 0. If trigger mode is level, remote IRR is set when the interrupt has begun service. Remote IRR is cleared when the end of interrupt has occurred.
13	Reserved. Read-write. Reset: 0. Intel defined as pin polarity. Not used by AMD because LINT interrupts are delivered by link messages instead of individual pins.
12	DS: interrupt delivery status. Read-only; updated-by-hardware. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. Read-write. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APIC370 LVT Error

Bits	Description
31:17	RAZ.
16	Mask. Read-write. Reset: 1. 0=Not masked. 1=Masked.
15:13	Reserved.
12	DS: interrupt delivery status. Read-only; updated-by-hardware. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. Read-write. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. Read-write. Reset: 00h. Interrupt vector number.

APIC380 Timer Initial Count

Bits	Description
31:0	Count. Read-write. Reset: 0. The value copied into the current count register when the timer is loaded or reloaded.

APIC390 Timer Current Count

Bits	Description
31:0	Count. Read-only. Reset: 0. The current value of the counter.

APIC3E0 Timer Divide Configuration

The Div bits are encoded as follows:

Table 183: Div[3,1:0] Value Table

Div[3]	Div[1:0]	Resulting Timer Divide
0	00b	2
0	01b	4
0	10b	8
0	11b	16
1	00b	32
1	01b	64
1	10b	128
1	11b	1

Bits	Description
31:4	RAZ.
3	Div[3]. Read-write. Reset: 0. See Table 183 .
2	RAZ.
1:0	Div[1:0]. Read-write. Reset: 0. See Table 183 .

APIC400 Extended APIC Feature

Bits	Description
31:24	RAZ.
23:16	ExtLvtCount: extended local vector table count. Read-only. Reset: 04h. This specifies the number of extended LVT registers (APIC[530:500]) in the local APIC.
15:3	RAZ.
2	ExtApicIdCap: extended APIC ID capable. Read-only. Reset: 1. 1=The processor is capable of supporting an 8-bit APIC ID, as controlled by APIC410[ExtApicIdEn] .
1	SeoiCap: specific end of interrupt capable. Read-only. Reset: 1. 1=The APIC420 [Specific End Of Interrupt] is present.
0	IerCap: interrupt enable register capable. Read-only. Reset: 1. This bit indicates that the APIC[4F0:480] [Interrupt Enable] are present. See 2.4.8.1.8 [Interrupt Masking] .

APIC410 Extended APIC Control

Bits	Description
31:3	RAZ.
2	ExtApicIdEn: extended APIC ID enable. Read-write. Reset: 0. 1=Enable 8-bit APIC ID; APIC20[ApicId] supports an 8-bit value; an interrupt broadcast in physical destination mode requires that the IntDest[7:0]=1111_1111b (instead of xxxx_1111b); a match in physical destination mode occurs when (IntDest[7:0] == ApicId[7:0]) instead of (IntDest[3:0] == ApicId[3:0]). 4-bit APIC ID support deprecated only when x2APIC mode is added. If ExtApicIdEn=1 then program D18F0x68[ApicExtId]=1 and D18F0x68[ApicExtBrdCst]=1.
1	SeoiEn. Read-write. Reset: 0. 1=Enable SEOI generation when a write to APIC420 [Specific End Of Interrupt] is received.
0	IerEn. Read-write. Reset: 0. 1=Enable writes to the interrupt enable registers.

APIC420 Specific End Of Interrupt

Bits	Description
31:8	RAZ.
7:0	EoVec: end of interrupt vector. Read-write. Reset: 0. A write to this field causes an end of interrupt cycle to be performed for the vector specified in this field. The behavior is undefined if no interrupt is pending for the specified interrupt vector.

APIC[4F0:480] Interrupt Enable

AMD-Specific. Interrupt enables range is mapped as follows:

Table 184: Register Mapping for APIC[4F0:480]

Register	Function
APIC480	IntEn[31:0]
APIC490	IntEn[63:32]
APIC4A0	IntEn[95:64]
APIC4B0	IntEn[127:96]
APIC4C0	IntEn[159:128]
APIC4D0	IntEn[191:160]
APIC4E0	IntEn[223:192]
APIC4F0	IntEn[255:224]

Bits	Description
31:0	InterruptEnableBits. Read-write. Reset: FFFF_FFFFh. The interrupt enable bits can be used to enable each of the 256 interrupts. See above table.

APIC[530:500] Extended Interrupt [3:0] Local Vector Table

AMD-Specific. APIC500 provides a local vector table entry for IBS; See D18F3x1CC. APIC510 provides a

local vector table entry for error thresholding. The APIC[530:520] registers are unused. [APIC\[530:500\]](#) interrupts disabled by ([MSRC001_001F\[DisApicExtReg\]==1](#)).

Table 185: Register Mapping for APIC[530:500]

Register	Function
APIC500	Extended Interrupt 0 (IBS)
APIC510	Extended Interrupt 1 (Thresholding)
APIC520	Extended Interrupt 2
APIC530	Extended Interrupt 3

Bits	Description
31:17	RAZ.
16	Mask. IF (MSRC001_001F[DisApicExtReg]==1) THEN RAZ. ELSE Read-write. ENDIF. Reset: 1. 0=Not masked. 1=Masked.
15:13	RAZ.
12	DS: interrupt delivery status. IF (MSRC001_001F[DisApicExtReg]==1) THEN RAZ. ELSE Read-only; updated-by-hardware. ENDIF. Reset: 0. 0=Idle. 1=Send pending. (Indicates that the interrupt has not yet been accepted by the core.)
11	RAZ.
10:8	MsgType: message type. IF (MSRC001_001F[DisApicExtReg]==1) THEN RAZ. ELSE Read-write. ENDIF. Reset: 000b. See 2.4.8.1.14 [Generalized Local Vector Table] .
7:0	Vector. IF (MSRC001_001F[DisApicExtReg]==1) THEN RAZ. ELSE Read-write. ENDIF. Reset: 00h. Interrupt vector number.

3.18 CPUID Instruction Registers

Processor feature capabilities and configuration information are provided through the CPUID instruction. The information is accessed by (1) selecting the CPUID function setting EAX and optionally ECX for some functions, (2) executing the CPUID instruction, and (3) reading the results in the EAX, EBX, ECX, and EDX registers. The syntax *CPUID FnXXXX_XXXX_EiX/_xYYY* refers to the function where EAX==X, and optionally ECX==Y, and the registers specified by EiX. EiX can be any single register such as {EAX, EBX, ECX, and EDX}, or a range of registers, such as E[C,B,A]X. Undefined function numbers return 0's in all 4 registers. See [2.4.10 \[CPUID Instruction\]](#).

Unless otherwise specified, single-bit feature fields are encoded as 1=Feature is supported by the processor; 0=Feature is not supported by the processor.

The following provides processor specific details about CPUID.

CPUID Fn0000_0000_EAX Processor Vendor and Largest Standard Function Number

Bits	Description
31:0	LFuncStd: largest standard function. Value: 0000_000Dh. The largest CPUID standard function input value supported by the processor implementation.

CPUID Fn0000_0000_E[D,C,B]X Processor Vendor

[CPUID Fn0000_0000_E\[D,C,B\]X](#) and [CPUID Fn8000_0000_E\[D,C,B\]X](#) return the same value.

Table 186: Reset Mapping for CPUID Fn8000_0000_E[D,C,B]X

Register	Value	Description
CPUID Fn0000_0000_EBX	6874_7541h	The ASCII characters “h t u A”.
CPUID Fn0000_0000_ECX	444D_4163h	The ASCII characters “D M A c”.
CPUID Fn0000_0000_EDX	6974_6E65h	The ASCII characters “i t n e”.

Bits	Description
31:0	Vendor. The 12 8-bit ASCII character codes to create the string “AuthenticAMD”.

CPUID Fn0000_0001_EAX Family, Model, Stepping Identifiers

Also see [CPUID Fn8000_0001_EAX \[Family, Model, Stepping Identifiers\]](#).

Family is an 8-bit value and is defined as: **Family[7:0]** = ({0000b,BaseFamily[3:0]} + ExtendedFamily[7:0]). E.g. If BaseFamily[3:0]=Fh and ExtendedFamily[7:0]=07h, then Family[7:0]=16h.

Model is an 8-bit value and is defined as: **Model[7:0]** = {ExtendedModel[3:0], BaseModel[3:0]}. E.g. If ExtendedModel[3:0]=Eh and BaseModel[3:0]=8h, then Model[7:0] = E8h. Model numbers vary with product.

Bits	Description
31:28	Reserved.
27:20	ExtFamily: extended family. CPUID Fn0000_0001_EAX [ExtFamily] is an alias of D18F3xFC [ExtFamily].
19:16	ExtModel: extended model. CPUID Fn0000_0001_EAX [ExtModel] is an alias of D18F3xFC [ExtModel].
15:12	Reserved.
11:8	BaseFamily. CPUID Fn0000_0001_EAX [BaseFamily] is an alias of D18F3xFC [BaseFamily].
7:4	BaseModel. CPUID Fn0000_0001_EAX [BaseModel] is an alias of D18F3xFC [BaseModel].
3:0	Stepping. CPUID Fn0000_0001_EAX [Stepping] is an alias of D18F3xFC [Stepping].

CPUID Fn0000_0001_EBX LocalApicId, LogicalProcessorCount, CLFlush

Bits	Description
31:24	LocalApicId: initial local APIC physical ID. Value: The initial APIC20 [ApicId] value. See 2.4.4 [Processor Cores and Downcore].
23:16	LogicalProcessorCount: logical processor count. Specifies the number of cores in the processor as CPUID Fn8000_0008_ECX [NC] + 1. Value: CPUID Fn8000_0008_ECX [NC] + 1.
15:8	CLFlush: CLFLUSH size in quadwords. Value: 08h.
7:0	8BitBrandId: 8 bit brand ID. Value: 00h. Indicates that the brand ID is in CPUID Fn8000_0001_EBX .

CPUID Fn0000_0001_ECX Feature Identifiers

These values can be over-written by [MSRC001_1004](#).

Bits	Description
31	RAZ. Reserved for use by hypervisor to indicate guest status.
30	RDRAND: RDRAND instruction support. Value: 0.
29	F16C: half-precision convert instruction support. Value: ~(Fuse[XCoreLateBits[88]] MSRC001_102E [DisF16c]).
28	AVX: AVX instruction support. Value: 1. Value: ~(Fuse[XCoreLateBits[87]] MSRC001_102E [DisAvx]).
27	OSXSAVE: OS enabled support for XGETBV/XSETBV. Value: CR4[OSXSAVE]. 1=The OS has enabled support for XGETBV/XSETBV instructions to query processor extended states.
26	XSAVE: XSAVE (and related) instruction support. Value: ~(Fuse[XCoreLateBits[85]] MSRC001_102E [DisXsave]). 1=Support provided for the XSAVE, XRSTOR, XSETBV, and XGETBV instructions and the XFEATURE_ENABLED_MASK register.
25	AES: AES instruction support. Value: ~(Fuse[XCoreLateBits[84]] MSRC001_102E [DisAes]).
24	Reserved.
23	POPCNT: POPCNT instruction. Value: 1.
22	MOVBE: MOVBE instruction support. Value: ~(Fuse[XCoreLateBits[83]] MSRC001_102E [DisMovbe]).
21	x2APIC: x2APIC capability. Value: 0.
20	SSE42: SSE4.2 instruction support. Value: ~(Fuse[XCoreLateBits[82]] MSRC001_102E [DisSse4p2]).
19	SSE41: SSE4.1 instruction support. Value: ~(Fuse[XCoreLateBits[81]] MSRC001_102E [DisSse4p1]).
18	Reserved.
17	PCID: process context identifiers support. Value: 0.
16:14	Reserved.
13	CMPXCHG16B: CMPXCHG16B instruction. Value: 1.

12	FMA: FMA instruction support. Value: 0.
11:10	Reserved.
9	SSSE3: supplemental SSE3 extensions. Value: 1.
8:4	Reserved.
3	Monitor: Monitor/Mwait instructions. Value: ~MSRC001_0015[MonMwaitDis].
2	Reserved.
1	PCLMULQDQ: PCLMULQDQ instruction support. Value: ~(Fuse[XCoreLateBits[84]] MSRC001_102E[DisPcmulqdq]).
0	SSE3: SSE3 extensions. Value: 1.

CPUID Fn0000_0001_EDX Feature IdentifiersThese values can be over-written by [MSRC001_1004](#).

Bits	Description
31:29	Reserved.
28	HTT: hyper-threading technology. Value: CPUID Fn8000_0008_ECX[NC]!=0. 1=Multi core product (CPUID Fn8000_0008_ECX[NC] != 0). 0=Single core product (CPUID Fn8000_0008_ECX[NC]==0).
27	Reserved.
26	SSE2: SSE2 extensions. Value: 1.
25	SSE: SSE extensions. Value: 1.
24	FXSR: FXSAVE and FXRSTOR instructions. Value: 1.
23	MMX: MMX™ instructions. Value: 1.
22:20	Reserved.
19	CLFLSH: CLFLUSH instruction. Value: 1.
18	Reserved.
17	PSE36: page-size extensions. Value: 1.
16	PAT: page attribute table. Value: 1.
15	CMOV: conditional move instructions, CMOV, FCOMI, FCMOV. Value: 1.
14	MCA: machine check architecture, MCG_CAP. Value: 1.
13	PGE: page global extension, CR4.PGE. Value: 1.
12	MTRR: memory-type range registers. Value: 1.
11	SysEnterSysExit: SYSENTER and SYSEXIT instructions. Value: 1.
10	Reserved.
9	APIC: advanced programmable interrupt controller (APIC) exists and is enabled. Value: MSR0000_001B[ApicEn].
8	CMPXCHG8B: CMPXCHG8B instruction. Value: 1.
7	MCE: machine check exception, CR4.MCE. Value: 1.

6	PAE: physical-address extensions (PAE). Value: 1.
5	MSR: AMD model-specific registers (MSRs), with RDMSR and WRMSR instructions. Value: 1.
4	TSC: time stamp counter, RDTSC/RDTSCP instructions, CR4.TSD. Value: 1.
3	PSE: page-size extensions (4 MB pages). Value: 1.
2	DE: debugging extensions, IO breakpoints, CR4.DE. Value: 1.
1	VME: virtual-mode enhancements. Value: 1.
0	FPU: x87 floating point unit on-chip. Value: 1.

CPUID Fn0000_000[4:2] Reserved

Bits	Description
31:0	Reserved.

CPUID Fn0000_0005_EAX Monitor/MWait

Bits	Description
31:16	Reserved.
15:0	MonLineSizeMin: smallest monitor-line size in bytes. Value: 40h.

CPUID Fn0000_0005_EBX Monitor/MWait

Bits	Description
31:16	Reserved.
15:0	MonLineSizeMax: largest monitor-line size in bytes. Value: 40h.

CPUID Fn0000_0005_ECX Monitor/MWait

Bits	Description
31:2	Reserved.
1	IBE: interrupt break-event. Value: 1.
0	EMX: enumerate MONITOR/MWAIT extensions. Value: 1.

CPUID Fn0000_0005_EDX Monitor/MWait

Bits	Description
31:0	Reserved.

CPUID Fn0000_0006_EAX Thermal and Power Management

Bits	Description
31:3	Reserved.
2	ARAT: always running APIC timer. Value: 0. 1=Indicates support for APIC timer always running feature.
1:0	Reserved.

CPUID Fn0000_0006_EBX Thermal and Power Management

Bits	Description
31:0	Reserved.

CPUID Fn0000_0006_ECX Thermal and Power Management

Bits	Description
31:1	Reserved.
0	EffFreq: effective frequency interface. Value: 1. 1=Indicates presence of MSR0000_00E7 [Max Performance Frequency Clock Count (MPERF)] and MSR0000_00E8 [Actual Performance Frequency Clock Count (APERF)] .

CPUID Fn0000_0006_EDX Thermal and Power Management

Bits	Description
31:0	Reserved.

CPUID Fn0000_0007_EAX_x0 Structured Extended Feature Identifiers (ECX=0)

Bits	Description
31:0	Reserved.

CPUID Fn0000_0007_EBX_x0 Structured Extended Feature Identifiers (ECX=0)

Bits	Description
31:11	Reserved.
10	INVPCID: invalidate processor context ID. Value: 0.

8	BMI2: bit manipulation group 2 instruction support. Value: 0.
7	SMEP: supervisor mode execution protection. Value: 0.
6	Reserved.
5	AVX2: AVX extension support. Value: 0.
4	Reserved.
3	BMI1: bit manipulation group 1 instruction support. Value: ~(Fuse[XCoreLateBits[89]] (MSRC001_102E [DisBmi])).
2:1	Reserved.
0	FSGSBASE: FS and GS base read write instruction support. Value: 0.

CPUID Fn0000_0007_EDX_x0 Structured Extended Feature Identifiers (ECX=0)

Bits	Description
31:0	Reserved.

CPUID Fn0000_0007_EDX_x0 Structured Extended Feature Identifiers (ECX=0)

Bits	Description
31:0	Reserved.

CPUID Fn0000_000[A:8] Reserved

Bits	Description
31:0	Reserved.

CPUID Fn0000_000B Reserved

Bits	Description
31:0	Reserved.

CPUID Fn0000_000C Reserved

Bits	Description
31:0	Reserved.

CPUID Fn0000_000D_EAX_x0 Processor Extended State Enumeration (ECX=0)

Bits	Description
31:0	XFeatureSupportedMask[31:0] . Value: 0000_0007h.

CPUID Fn0000_000D_EBX_x0 Processor Extended State Enumeration (ECX=0)

Bits	Description
31:0	<p>XFeatureEnabledSizeMax. Size in bytes of XSAVE/XRSTOR area for the currently enabled features in XCR0.</p> <p>Value: $512 + 64 + (\text{IF } (\text{XCR0[AVX]}) \text{ THEN } 256 \text{ ELSE } 0 \text{ ENDIF})$.</p> <p>The components of this sum are described as follows:</p> <ul style="list-style-type: none"> • 512: FPU/SSE save area (needed even if XCR0[SSE]=0) • 64: Header size (always needed). • Size of YMM area if YMM enabled.

CPUID Fn0000_000D_ECX_x0 Processor Extended State Enumeration (ECX=0)

Bits	Description
31:0	<p>XFeatureSupportedSizeMax. Size in bytes of XSAVE/XRSTOR area for all features that the core supports. See XFeatureEnabledSizeMax.</p> <p>Value: 0000_0340h. (512+64+256)</p>

CPUID Fn0000_000D_EDX_x0 Processor Extended State Enumeration (ECX=0)

Bits	Description
31:0	<p>XFeatureSupportedMask[63:32].</p> <p>Value: 0000_0000h.</p>

CPUID Fn0000_000D_EAX_x1 Processor Extended State Enumeration (ECX=1)

Bits	Description

31:1	Reserved.
0	XSAVEOPT: XSAVEOPT is available. Value: ~(Fuse[XCoreLateBits[86]] MSRC001_102E[DisXsaveopt]).

CPUID Fn0000_000D_E[D,C,B]X_x1 Processor Extended State Enumeration (ECX=1)

Bits	Description
31:0	Reserved.

CPUID Fn0000_000D_EAX_x2 Processor Extended State Enumeration (ECX=2)

Bits	Description
31:0	YmmSaveStateSize: YMM save state byte size. Value: 0000_0100h.

CPUID Fn0000_000D_EBX_x2 Processor Extended State Enumeration (ECX=2)

Bits	Description
31:0	YmmSaveStateOffset: YMM save state byte offset. Value: 0000_0240h.

CPUID Fn0000_000D_ECX_x2 Processor Extended State Enumeration (ECX=2)

Bits	Description
31:0	Reserved.

CPUID Fn0000_000D_EDX_x2 Processor Extended State Enumeration (ECX=2)

Bits	Description
31:0	Reserved.

For CPUID Fn0000_000D, if ECX>2 then EAX/EBX/ECX/EDX will return 0.

CPUID Fn8000_0000_EAX Largest Extended Function Number

Bits	Description
31:0	LFuncExt: largest extended function. Value: 8000_001Eh. The largest CPUID extended function input value supported by the processor implementation.

CPUID Fn8000_0000_E[D,C,B]X Processor Vendor

CPUID Fn0000_0000_E[D,C,B]X and CPUID Fn8000_0000_E[D,C,B]X return the same value.

Table 187: CPUID Fn8000_0000_E[B,C,D]X Value

Register	Value	Description
CPUID Fn8000_0000_EBX	6874_7541h	The ASCII characters “h t u A”.
CPUID Fn8000_0000(ECX	444D_4163h	The ASCII characters “D M A c”.
CPUID Fn8000_0000_EDX	6974_6E65h	The ASCII characters “i t n e”.

Bits	Description
31:0	Vendor. The 12 8-bit ASCII character codes to create the string “AuthenticAMD”.

CPUID Fn8000_0001_EAX Family, Model, Stepping IdentifiersAlso see [CPUID Fn0000_0001_EAX \[Family, Model, Stepping Identifiers\]](#).

Bits	Description
31:28	Reserved.
27:20	ExtFamily: extended family. CPUID Fn8000_0001_EAX[ExtFamily] is an alias of D18F3xFC [ExtFamily].
19:16	ExtModel: extended model. CPUID Fn8000_0001_EAX[ExtModel] is an alias of D18F3xFC [ExtModel].
15:12	Reserved.
11:8	BaseFamily. CPUID Fn8000_0001_EAX[BaseFamily] is an alias of D18F3xFC [BaseFamily].
7:4	BaseModel. CPUID Fn8000_0001_EAX[BaseModel] is an alias of D18F3xFC [BaseModel].
3:0	Stepping. CPUID Fn8000_0001_EAX[Stepping] is an alias of D18F3xFC [Stepping].

CPUID Fn8000_0001_EBX BrandId Identifier

Bits	Description								
31:28	PkgType: package type. Specifies the package type. Value: 0h. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>FT3 (BGA)</td> </tr> <tr> <td>1h</td> <td>FS1b</td> </tr> <tr> <td>Fh-2h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	0h	FT3 (BGA)	1h	FS1b	Fh-2h	Reserved
Bits	Description								
0h	FT3 (BGA)								
1h	FS1b								
Fh-2h	Reserved								

CPUID Fn8000_0001_ECX Feature IdentifiersThese values can be over-written by [MSRC001_1005](#).

Bits	Description
31:30	Reserved.
29	Reserved.

28	PerfCtrExtL2I: L2I performance counter extensions support. Value: 1. Indicates support for MSRC001_023[6,4,2,0] and MSRC001_023[7,5,3,1] .
27	PerfTsc: performance time-stamp counter supported. Value: 0. Indicates support for MSRC001_0280 [Performance Time Stamp Counter (CU_PTSC)].
26	DataBreakpointExtension. Value: 1. Indicates data breakpoint support for MSRC001_1027 and MSRC001_101[B:9] .
25	Reserved.
24	PerfCtrExtNB: NB performance counter extensions support. Value: 1. Indicates support for MSRC001_024[6,4,2,0] and MSRC001_024[7,5,3,1] .
23	PerfCtrExtCore: core performance counter extensions support. Value: 0. Indicates support for MSRC001_020[A,8,6,4,2,0] and MSRC001_020[B,9,7,5,3,1].
22	TopologyExtensions: topology extensions support. Value: 1. Indicates support for CPUID Fn8000_001D_EAX_x0-CPUID Fn8000_001E_EDX .
21	TBM: trailing bit manipulation instruction support. Value: 0.
18	Reserved.
17	TCE: translation cache extension. Value: 0.
16	FMA4: 4-operand FMA instruction support. Value: 0.
15	LWP: lightweight profiling support. Value: 0.
14	Reserved.
13	WDT: watchdog timer support. Value: 1.
12	SKINIT: SKINIT and STGI support. Value: 1.
11	XOP: extended operation support. Value: 0.
10	IBS: Instruction Based Sampling. Value: 1.
9	OSVW: OS Visible Work-around support. Value: 1.
8	3DNowPrefetch: Prefetch and PrefetchW instructions. Value: 1.
7	MisAlignSse: Misaligned SSE Mode. Value: 1.
6	SSE4A: EXTRQ, INSERTQ, MOVNTSS, and MOVNTSD instruction support. Value: 1.
5	ABM: advanced bit manipulation. Value: 1. LZCNT instruction support.
4	AltMovCr8: LOCK MOV CR0 means MOV CR8. Value: 1.

3	ExtApicSpace: extended APIC register space. Value: 1.
2	SVM: Secure Virtual Mode feature. Value: ~Fuse[SvmDis]. Indicates support for the remaining SVM instructions, not covered by SKINIT: VMRUN, VMLOAD, VMSAVE, CLGI, VMMCALL, and INVLPGA.
1	CmpLegacy: core multi-processing legacy mode. Value: (CPUID Fn8000_0008_ECX[NC]>0). 1=Multi core product (CPUID Fn8000_0008_ECX[NC] != 0). 0=Single core product (CPUID Fn8000_0008_ECX[NC] == 0).
0	LahfSahf: LAHF/SAHF instructions. Value: 1.

CPUID Fn8000_0001_EDX Feature IdentifiersThese values can be over-written by [MSRC001_1005](#).

Bits	Description
31	3DNow: 3DNow!TM instructions. Value: 0.
30	3DNowExt: AMD extensions to 3DNow!TM instructions. Value: 0.
29	LM: long mode. Value: 1. LongModeDis tied to 0b at the SOC level.
28	Reserved.
27	RDTSCP: RDTSCP instruction. Value: 1.
26	Page1GB: one GB large page support. Value: 1.
25	FFXSR: FXSAVE and FXRSTOR instruction optimizations. Value: 1.
24	FXSR: FXSAVE and FXRSTOR instructions. Value: 1.
23	MMX: MMXTM instructions. Value: 1.
22	MmxExt: AMD extensions to MMX instructions. Value: 1.
21	Reserved.
20	NX: no-execute page protection. Value: 1.
19:18	Reserved.
17	PSE36: page-size extensions. Value: 1.
16	PAT: page attribute table. Value: 1.
15	CMOV: conditional move instructions, CMOV, FCOMI, FCMOV. Value: 1.
14	MCA: machine check architecture, MCG_CAP. Value: 1.
13	PGE: page global extension, CR4.PGE. Value: 1.
12	MTRR: memory-type range registers. Value: 1.
11	SysCallSysRet: SYSCALL and SYSRET instructions. Value: 1.
10	Reserved.
9	APIC: advanced programmable interrupt controller (APIC) exists and is enabled. Value: MSR0000_001B [ApicEn].
8	CMPXCHG8B: CMPXCHG8B instruction. Value: 1.
7	MCE: machine check exception, CR4.MCE. Value: 1.
6	PAE: physical-address extensions (PAE). Value: 1.

5	MSR: model-specific registers (MSRs), with RDMSR and WRMSR instructions. Value: 1.
4	TSC: time stamp counter, RDTSC/RDTSCP instructions, CR4.TSD. Value: 1.
3	PSE: page-size extensions (4 MB pages). Value: 1.
2	DE: debugging extensions, IO breakpoints, CR4.DE. Value: 1.
1	VME: virtual-mode enhancements. Value: 1.
0	FPU: x87 floating point unit on-chip. Value: 1.

CPUID Fn8000_000[4:2]_E[D,C,B,A]X Processor Name String Identifier

Table 188: Valid Values for CPUID Fn8000_000[4:2]_E[D,C,B,A]X

Register	Value
CPUID Fn8000_0002_EAX	MSRC001_0030[31:0]
CPUID Fn8000_0002_EBX	MSRC001_0030[63:32]
CPUID Fn8000_0002_ECX	MSRC001_0031[31:0]
CPUID Fn8000_0002_EDX	MSRC001_0031[63:32]
CPUID Fn8000_0003_EAX	MSRC001_0032[31:0]
CPUID Fn8000_0003_EBX	MSRC001_0032[63:32]
CPUID Fn8000_0003_ECX	MSRC001_0033[31:0]
CPUID Fn8000_0003_EDX	MSRC001_0033[63:32]
CPUID Fn8000_0004_EAX	MSRC001_0034[31:0]
CPUID Fn8000_0004_EBX	MSRC001_0034[63:32]
CPUID Fn8000_0004_ECX	MSRC001_0035[31:0]
CPUID Fn8000_0004_EDX	MSRC001_0035[63:32]

Bits	Description
31:0	ProcName: processor name. These return the ASCII string corresponding to the processor name, stored in MSRC001_00[35:30] [Processor Name String].

CPUID Fn8000_0005_EAX L1 TLB 2M/4M Identifiers

This function provides the processor's first level cache and TLB characteristics for each core.

Bits	Description
31:24	L1DTlb2and4MAssoc: data TLB associativity for 2 MB and 4 MB pages. Value: FFh. See: CPUID Fn8000_0005(ECX)[L1DcAssoc].
23:16	L1DTlb2and4MSize: data TLB number of entries for 2 MB and 4 MB pages. Value: 8. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.

15:8	L1ITlb2and4MAssoc: instruction TLB associativity for 2 MB and 4 MB pages. Value: FFh. See: CPUID Fn8000_0005_ECX [L1DcAssoc].
7:0	L1ITlb2and4MSize: instruction TLB number of entries for 2 MB and 4 MB pages. Value: 8. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.

CPUID Fn8000_0005_EBX L1 TLB 4K IdentifiersSee: [CPUID Fn8000_0005_EAX](#).

Bits	Description
31:24	L1DTlb4KAssoc: data TLB associativity for 4 KB pages. Value: FFh. See: CPUID Fn8000_0005_ECX [L1DcAssoc].
23:16	L1DTlb4KSize: data TLB number of entries for 4 KB pages. Value: 40.
15:8	L1ITlb4KAssoc: instruction TLB associativity for 4 KB pages. Value: FFh. ITLB associativity for 4 KB pages is reported by CPUID Fn8000_0006_EBX [L2ITlb4KAssoc].
7:0	L1ITlb4KSize: instruction TLB number of entries for 4 KB pages. Value: 32. ITLB size for 4 KB pages is reported by CPUID Fn8000_0006_EBX [L2ITlb4KSize].

CPUID Fn8000_0005_ECX L1 Data Cache Identifiers

This function provides first level cache characteristics for each core.

Bits	Description														
31:24	L1DcSize: L1 data cache size in KB. Value: 32.														
23:16	L1DcAssoc: L1 data cache associativity. Value: 8. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved</td> </tr> <tr> <td>01h</td> <td>1 way (direct mapped)</td> </tr> <tr> <td>02h</td> <td>2 way</td> </tr> <tr> <td>03h</td> <td>3 way</td> </tr> <tr> <td>FEh-04h</td> <td>[L1IcAssoc] way</td> </tr> <tr> <td>FFh</td> <td>Fully associative</td> </tr> </tbody> </table>	Bits	Description	00h	Reserved	01h	1 way (direct mapped)	02h	2 way	03h	3 way	FEh-04h	[L1IcAssoc] way	FFh	Fully associative
Bits	Description														
00h	Reserved														
01h	1 way (direct mapped)														
02h	2 way														
03h	3 way														
FEh-04h	[L1IcAssoc] way														
FFh	Fully associative														
15:8	L1DcLinesPerTag: L1 data cache lines per tag. Value: 1.														
7:0	L1DcLineSize: L1 data cache line size in bytes. Value: 64.														

CPUID Fn8000_0005_EDX L1 Instruction Cache Identifiers

This function provides first level cache characteristics for each core.

Bits	Description
31:24	L1IcSize: L1 instruction cache size KB. Value: 32.
23:16	L1IcAssoc: L1 instruction cache associativity. Value: 2. See: CPUID Fn8000_0005(ECX)[L1DcAssoc] .
15:8	L1IcLinesPerTag: L1 instruction cache lines per tag. Value: 1.
7:0	L1IcLineSize: L1 instruction cache line size in bytes. Value: 64.

CPUID Fn8000_0006_EAX L2 TLB 2M/4M Identifiers

This function provides the processor's second level cache and TLB characteristics for each core.

Bits	Description
31:28	L2DTlb2and4MAssoc: L2 data TLB associativity for 2 MB and 4 MB pages. Value: 2. See: CPUID Fn8000_0006(ECX)[L2Assoc] .
27:16	L2DTlb2and4MSize: L2 data TLB number of entries for 2 MB and 4 MB pages. Value: 256. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.
15:12	L2ITlb2and4MAssoc: L2 instruction TLB associativity for 2 MB and 4 MB pages. Value: 0. See: CPUID Fn8000_0006(ECX)[L2Assoc] .
11:0	L2ITlb2and4MSize: L2 instruction TLB number of entries for 2 MB and 4 MB pages. Value: 0. The value returned is for the number of entries available for the 2 MB page size; 4 MB pages require two 2 MB entries, so the number of entries available for the 4 MB page size is one-half the returned value.

CPUID Fn8000_0006_EBX L2 TLB 4K Identifiers

This function provides second level TLB characteristics for 4K pages shared by each core on a L2 complex.

Bits	Description
31:28	L2DTlb4KAssoc: L2 data TLB associativity for 4 KB pages. Value: 4. See: CPUID Fn8000_0006(ECX)[L2Assoc] .
27:16	L2DTlb4KSize: L2 data TLB number of entries for 4 KB pages. Value: 512.

15:12	L2ITlb4KAssoc: L2 instruction TLB associativity for 4 KB pages. Value: 4. See: CPUID Fn8000_0006_ECX [L2Assoc].
11:0	L2ITlb4KSize: L2 instruction TLB number of entries for 4 KB pages. Value: 512.

CPUID Fn8000_0006_ECX L2 Cache Identifiers

Bits	Description																																							
31:16	L2Size: L2 cache size in KB. Value: IF (Fuse[IL2Region[2:0]]==000b) THEN 0800h. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>03FFh-0000h</td> <td>Reserved</td> </tr> <tr> <td>0400h</td> <td>1 MB</td> </tr> <tr> <td>07FFh-0401h</td> <td>Reserved</td> </tr> <tr> <td>0800h</td> <td>2 MB</td> </tr> <tr> <td>FFFFh-0801h</td> <td>Reserved</td> </tr> </tbody> </table> <table> <thead> <tr> <th>IL2Region</th> <th>Size</th> <th>Active Banks</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>2 MB</td> <td>bank[3:0]</td> </tr> <tr> <td>001b</td> <td>1 MB</td> <td>1 MB bank[1,0]</td> </tr> <tr> <td>010b</td> <td>1 MB</td> <td>1 MB bank[2,0]</td> </tr> <tr> <td>011b</td> <td>1 MB</td> <td>1 MB bank[3,0]</td> </tr> <tr> <td>100b</td> <td>1 MB</td> <td>1 MB bank[2,1]</td> </tr> <tr> <td>101b</td> <td>1 MB</td> <td>1 MB bank[3,1]</td> </tr> <tr> <td>110b</td> <td>1 MB</td> <td>1 MB bank[3,2]</td> </tr> <tr> <td>111b</td> <td>Reserved</td> <td></td> </tr> </tbody> </table>	Bits	Description	03FFh-0000h	Reserved	0400h	1 MB	07FFh-0401h	Reserved	0800h	2 MB	FFFFh-0801h	Reserved	IL2Region	Size	Active Banks	000b	2 MB	bank[3:0]	001b	1 MB	1 MB bank[1,0]	010b	1 MB	1 MB bank[2,0]	011b	1 MB	1 MB bank[3,0]	100b	1 MB	1 MB bank[2,1]	101b	1 MB	1 MB bank[3,1]	110b	1 MB	1 MB bank[3,2]	111b	Reserved	
Bits	Description																																							
03FFh-0000h	Reserved																																							
0400h	1 MB																																							
07FFh-0401h	Reserved																																							
0800h	2 MB																																							
FFFFh-0801h	Reserved																																							
IL2Region	Size	Active Banks																																						
000b	2 MB	bank[3:0]																																						
001b	1 MB	1 MB bank[1,0]																																						
010b	1 MB	1 MB bank[2,0]																																						
011b	1 MB	1 MB bank[3,0]																																						
100b	1 MB	1 MB bank[2,1]																																						
101b	1 MB	1 MB bank[3,1]																																						
110b	1 MB	1 MB bank[3,2]																																						
111b	Reserved																																							
15:12	L2Assoc: L2 cache associativity. Value: 8. <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Disabled.</td> <td>8h</td> <td>16 ways</td> </tr> <tr> <td>1h</td> <td>1 way (direct mapped)</td> <td>9h</td> <td>Reserved</td> </tr> <tr> <td>2h</td> <td>2 ways</td> <td>Ah</td> <td>32 ways</td> </tr> <tr> <td>3h</td> <td>Reserved</td> <td>Bh</td> <td>48 ways</td> </tr> <tr> <td>4h</td> <td>4 ways</td> <td>Ch</td> <td>64 ways</td> </tr> <tr> <td>5h</td> <td>Reserved</td> <td>Dh</td> <td>96 ways</td> </tr> <tr> <td>6h</td> <td>8 ways</td> <td>Eh</td> <td>128 ways</td> </tr> <tr> <td>7h</td> <td>Reserved</td> <td>Fh</td> <td>Fully associative</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	0h	Disabled.	8h	16 ways	1h	1 way (direct mapped)	9h	Reserved	2h	2 ways	Ah	32 ways	3h	Reserved	Bh	48 ways	4h	4 ways	Ch	64 ways	5h	Reserved	Dh	96 ways	6h	8 ways	Eh	128 ways	7h	Reserved	Fh	Fully associative			
Bits	Description	Bits	Description																																					
0h	Disabled.	8h	16 ways																																					
1h	1 way (direct mapped)	9h	Reserved																																					
2h	2 ways	Ah	32 ways																																					
3h	Reserved	Bh	48 ways																																					
4h	4 ways	Ch	64 ways																																					
5h	Reserved	Dh	96 ways																																					
6h	8 ways	Eh	128 ways																																					
7h	Reserved	Fh	Fully associative																																					
11:8	L2LinesPerTag: L2 cache lines per tag. Value: 1.																																							
7:0	L2LineSize: L2 cache line size in bytes. Value: 64.																																							

CPUID Fn8000_0006_EDX L3 Cache Identifiers

This function provides third level cache characteristics shared by all cores of a node.

Bits	Description
31:18	L3Size: L3 cache size. Value: 0.
17:16	Reserved.
15:12	L3Assoc: L3 cache associativity. Value: 0.

11:8	L3LinesPerTag: L3 cache lines per tag. Value: 0.
7:0	L3LineSize: L3 cache line size in bytes. Value: 0.

CPUID Fn8000_0007_EAX Processor Feedback Capabilities

Bits	Description								
31:16	MaxWrapTime. Value: 0D6Bh. (3435 ms) Specifies the maximum time between reads that software should use to avoid two wraps. A read of at least once every MaxWrapTime seconds will result in either zero or one wrap during that interval.								
15:8	Version. Value: 01h. Specifies the processor feedback capabilities version.								
7:0	NumberOfMonitors. Value: 01h. Specifies the number of processor feedback MSR pairs supported, from MSRC001_0080 to MSRC001_0088 [0+((NumberOfMonitors-1)*2)+1]. <table border="1"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Reserved.</td> </tr> <tr> <td>01h</td> <td>MSRC001_0080 to MSRC001_0081 supported.</td> </tr> <tr> <td>FFh-02h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Description	00h	Reserved.	01h	MSRC001_0080 to MSRC001_0081 supported.	FFh-02h	Reserved.
Bits	Description								
00h	Reserved.								
01h	MSRC001_0080 to MSRC001_0081 supported.								
FFh-02h	Reserved.								

CPUID Fn8000_0007_EBX RAS Capabilities

Bits	Description
31:3	Reserved.
2	HWA: hardware assert supported. 1=Indicates support for MSRC001_10 [DF:C0]. Value: 0.
1	SUCCOR: Software uncorrectable error containment and recovery capability. Value: 0.
0	McaOverflowRecov: MCA overflow recovery support. Value: 1. 1=MCA overflow conditions (MCi_STATUS[Overflow]=1) are not fatal; software may safely ignore such conditions. 0=MCA overflow conditions require software to shut down the system. See 2.14.1.6 [Handling Machine Check Exceptions] .

CPUID Fn8000_0007_ECX Advanced Power Management Information

Bits	Description
31:0	Reserved.

CPUID Fn8000_0007_EDX Advanced Power Management Information

This function provides advanced power management feature identifiers.

Bits	Description
12	Reserved. Reserved for indicating Power Accumulator MSR C001_007A UBTS-412132
11	ProcFeedbackInterface: processor feedback interface. Value: 1. 1=Indicates support for processor feedback interface; CPUID Fn8000_0007_EAX .
10	EffFreqRO: read-only effective frequency interface. Value: 0. 1=Indicates presence of MSRC000_00E7 [Read-Only Max Performance Frequency Clock Count (MPerfReadOnly)] and MSRC000_00E8 [Read-Only Actual Performance Frequency Clock Count (APerfReadOnly)].
9	CPB: core performance boost. Value: (D18F4x15C [NumBoostStates]>0). 1= Indicates presence of MSRC001_0015 [CpbDis] and support for core performance boost. See 2.5.9 [Application Power Management (APM)] .
8	TscInvariant: TSC invariant. Value: 1. The TSC rate is invariant.
7	HwPstate: hardware P-state control. Value: 1. MSRC001_0061 [P-state Current Limit], MSRC001_0062 [P-state Control] and MSRC001_0063 [P-state Status] exist.
6	100MHzSteps: 100 MHz multiplier Control. Value: 1.
5	Reserved.
4	TM: hardware thermal control (HTC). Value: ~Fuse[HtcDis].
3	TTP: THERMTRIP. Value: Fuse[ThermTripEn].
2	VID: Voltage ID control. Value: 0. Function replaced by HwPstate.
1	FID: Frequency ID control. Value: 0. Function replaced by HwPstate.
0	TS: Temperature sensor. Value: 1.

CPUID Fn8000_0008_EAX Long Mode Address Size Identifiers

This provides information about the maximum physical and linear address width supported by the processor.

Bits	Description
31:24	Reserved.
23:16	GuestPhysAddrSize: maximum guest physical byte address size in bits. Value: 0. 0=The maximum guest physical address size defined by PhysAddrSize.
15:8	LinAddrSize: Maximum linear byte address size in bits. Value: IF (CPUID Fn8000_0001_EDX [LM]) THEN 30h ELSE 20h ENDIF.
7:0	PhysAddrSize: Maximum physical byte address size in bits. Value: 28h.

CPUID Fn8000_0008_EBX Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_0008_ECX Size Identifiers

This provides information about the number of logical cores supported by the processor.

Bits	Description										
31:18	Reserved.										
17:16	PerfTscSize: performance time-stamp counter size. Value: 00b. Indicates the size of MSRC001_0280[PTSC]. Valid only when (CPUID Fn8000_0001_ECX[PerfTsc]==1).										
	<table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>40 bits</td> </tr> <tr> <td>01b</td> <td>48 bits</td> </tr> <tr> <td>10b</td> <td>56 bits</td> </tr> <tr> <td>11b</td> <td>64 bits</td> </tr> </tbody> </table>	Bits	Description	00b	40 bits	01b	48 bits	10b	56 bits	11b	64 bits
Bits	Description										
00b	40 bits										
01b	48 bits										
10b	56 bits										
11b	64 bits										
15:12	ApicIdCoreIdSize: APIC ID size. Value: 3h. The number of bits in the initial APIC20[ApicId] value that indicate core ID within a processor.										
11:8	Reserved.										
7:0	NC: number of cores - 1. The number of cores in the processor is NC+1 (e.g., if NC=0, then there is one core). See 2.4.4 [Processor Cores and Downcoreing] . Value: D18F5x84[CmpCap]-NumOnes(D18F3x190[DisCore]).										

CPUID Fn8000_0008_EDX Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_0009 Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_000A_EAX SVM Revision and Feature Identification

This provides SVM revision. If ([CPUID Fn8000_0001_ECX\[SVM\]==0](#)) then [CPUID Fn8000_000A_EAX](#) is reserved.

Bits	Description
31:8	Reserved.
7:0	SvmRev: SVM revision. Value: 01h.

CPUID Fn8000_000A_EBX SVM Revision and Feature Identification

This provides SVM revision and feature information. If ([CPUID Fn8000_0001_ECX\[SVM\]==0](#)) then [CPUID Fn8000_000A_EBX](#) is reserved.

Bits	Description
31:0	NASID: number of address space identifiers (ASID). Value: 8h.

CPUID Fn8000_000A(ECX) SVM Revision and Feature Identification

Bits	Description
31:0	Reserved.

CPUID Fn8000_000A(EDX) SVM Revision and Feature Identification

This provides SVM feature information. If (CPUID Fn8000_0001(ECX)[SVM]==0) then CPUID Fn8000_000A(EDX) is reserved.

Bits	Description
31:14	Reserved.
13	AVIC: AMD virtual interrupt controller. Value: 0. 1=Support indicated for SVM mode virtualized interrupt controller; Indicates support for MSRC001_011B [AVIC Doorbell].
12	PauseFilterThreshold: PAUSE filter threshold. Value: 1.
10	PauseFilter: pause intercept filter. Value: 1.
7	DecodeAssists: decode assists. Value: 1.
6	FlushByAsid: flush by ASID. Value: 1.
5	VmcbClean: VMCB clean bits. Value: 0.
4	TscRateMsr: MSR based TSC rate control. Value: 1. 1=Indicates support for TSC ratio MSRC000_0104.
3	NRIPS: NRIP Save. Value: 1.
2	SVML: SVM lock. Value: 1.
1	LbrVirt: LBR virtualization. Value: 1.
0	NP: nested paging. Value: 1.

CPUID Fn8000_00[18:0B] Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_0019(EAX) L1 TLB 1G Identifiers

This function provides first level TLB characteristics for 1G pages shared by each core on a L2 complex.

Bits	Description
31:28	L1DTlb1GAssoc: L1 data TLB associativity for 1 GB pages. See: CPUID Fn8000_0006_ECX [L2Assoc]. Value: 0.
27:16	L1DTlb1GSize: L1 data TLB number of entries for 1 GB pages. Value: 0.
15:12	L1ITlb1GAssoc: L1 instruction TLB associativity for 1 GB pages. See: CPUID Fn8000_0006_ECX [L2Assoc]. Value: 0.
11:0	L1ITlb1GSize: L1 instruction TLB number of entries for 1 GB pages. Value: 0.

CPUID Fn8000_0019_EBX L2 TLB 1G Identifiers

This provides 1 GB paging information. The *associativity* fields are defined by [CPUID Fn8000_0006_EAX](#), [CPUID Fn8000_0006_EBX](#), [CPUID Fn8000_0006_ECX](#) and [CPUID Fn8000_0006_EDX](#).

Bits	Description
31:28	L2DTlb1GAssoc: L2 data TLB associativity for 1 GB pages. See: CPUID Fn8000_0006_ECX [L2Assoc]. Value: 0.
27:16	L2DTlb1GSize: L2 data TLB number of entries for 1 GB pages. Value: 0.
15:12	L2ITlb1GAssoc: L2 instruction TLB associativity for 1 GB pages. See: CPUID Fn8000_0006_ECX [L2Assoc]. Value: 0.
11:0	L2ITlb1GSize: L2 instruction TLB number of entries for 1 GB pages. Value: 0.

CPUID Fn8000_0019_E[D,C]X Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_001A_EAX Performance Optimization Identifiers

This function returns performance related information. For more details on how to use these bits to optimize software, see the optimization guide.

Bits	Description
31:3	Reserved.
2	FP256. Value: 0.
1	MOVU. Value: 1.
0	FP128. Value: 1.

CPUID Fn8000_001A_E[D,C,B]X Reserved

Bits	Description
31:0	Reserved.

CPUID Fn8000_001B_EAX Instruction Based Sampling Identifiers

This function returns IBS feature information.

Bits	Description
31:11	Reserved.
10	IbsOpData4: IBS op data 4 MSR supported. Value: 0. See MSRC001_103D [IBS Op Data 4 (DC_IBS_DATA2)].
9	IbsFetchCtlExtd: IBS fetch control extended MSR supported. Value: 0. 1=Indicates support for MSRC001_103C [IBS Fetch Control Extended (IC_IBS_EXTD_CTL)].
8	OpBrnFuse: fused branch micro-op indication supported. Value: 0. 1=Indicates support for MSRC001_1035 [IbsOpBrnFuse].
7	RipInvalidChk: invalid RIP indication supported. Value: 1. 1=Indicates support for MSRC001_1035 [IbsRipInvalid].
6	OpCntExt: IbsOpCurCnt and IbsOpMaxCnt extend by 7 bits. Value: 1. 1=Indicates support for MSRC001_1033 [IbsOpCurCnt[26:20], IbsOpMaxCnt[26:20]].
5	BrnTrgt: branch target address reporting supported. Value: 1.
4	OpCnt: op counting mode supported. Value: 1.
3	RdWrOpCnt: read write of op counter supported. Value: 1.
2	OpSam: IBS execution sampling supported. Value: 1.
1	FetchSam: IBS fetch sampling supported. Value: 1.
0	IBSFFV: IBS feature flags valid. Value: 1.

CPUID Fn8000_001B_E[D,C,B]X Instruction Based Sampling Identifiers

Bits	Description
31:0	Reserved.

CPUID Fn8000_001C_EAX Lightweight Profiling Capabilities 0

This function returns IBS feature information; see the Lightweight Profiling Specification section titled “Detecting LWP”. If ([CPUID Fn8000_0001_ECX\[LWP\]==0](#)) then CPUID Fn8000_001C_E[D,C,B,A]X is reserved.

Bits	Description
31:0	Reserved.

CPUID Fn8000_001C_EBX Lightweight Profiling Capabilities 0

See [CPUID Fn8000_001C_EAX](#).

Bits	Description
31:0	Reserved.

CPUID Fn8000_001C_ECX Lightweight Profiling Capabilities 0

See [CPUID Fn8000_001C_EAX](#).

Bits	Description
31:0	Reserved.

CPUID Fn8000_001C_EDX Lightweight Profiling Capabilities 0

See [CPUID Fn8000_001C_EAX](#).

Bits	Description
31:0	Reserved.

CPUID Fn8000_001D_EAX_x0 Cache Properties

CPUID Fn8000_001D_EAX_x0 reports topology information for the DC.

If ([CPUID Fn8000_0001_ECX\[TopologyExtensions\]==0](#)) then CPUID Fn8000_001D_E[D,C,B,A]X is reserved.

Table 189: ECX mapping to Cache Type for CPUID Fn8000_001D_E[D,C,B,A]X

ECX	Cache Type
0	DC
1	IC
2	L2
3	Null

Bits	Description												
31:26	Reserved. Intel defines this field as MaxCores.												
25:14	NumSharingCache: number of cores sharing cache. Value: 000h. The number of cores sharing this cache is NumSharingCache+1.												
13:10	Reserved.												
9	FullyAssociative: fully associative cache. Value: 0. 1=Cache is fully associative.												
8	SelfInitialization: cache is self-initializing. Value: 1. 1=Cache is self initializing; cache does not need software initialization.												
7:5	CacheLevel: cache level. Identifies the cache level. Value: 001b. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Reserved.</td> </tr> <tr> <td>001b</td> <td>Level 1</td> </tr> <tr> <td>010b</td> <td>Level 2</td> </tr> <tr> <td>011b</td> <td>Level 3</td> </tr> <tr> <td>111b-100b</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Description	000b	Reserved.	001b	Level 1	010b	Level 2	011b	Level 3	111b-100b	Reserved.
Bits	Description												
000b	Reserved.												
001b	Level 1												
010b	Level 2												
011b	Level 3												
111b-100b	Reserved.												
4:0	CacheType: cache type. Identifies the type of cache. Value: 01h. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Null; no more caches.</td> </tr> <tr> <td>01h</td> <td>Data cache</td> </tr> <tr> <td>02h</td> <td>Instruction cache</td> </tr> <tr> <td>03h</td> <td>Unified cache</td> </tr> <tr> <td>1Fh-04h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Description	00h	Null; no more caches.	01h	Data cache	02h	Instruction cache	03h	Unified cache	1Fh-04h	Reserved.
Bits	Description												
00h	Null; no more caches.												
01h	Data cache												
02h	Instruction cache												
03h	Unified cache												
1Fh-04h	Reserved.												

CPUID Fn8000_001D_EAX_x1 Cache Properties

CPUID Fn8000_001D_EAX_x1 reports topology information for the IC. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of cores sharing cache. See: CPUID Fn8000_001D_EAX_x0 [NumSharingCache]. Value: 000h.
13:10	Reserved.
9	FullyAssociative: fully associative cache. Value: 0. See: CPUID Fn8000_001D_EAX_x0 [FullyAssociative].
8	SelfInitialization: cache is self-initializing. Value: 1. See: CPUID Fn8000_001D_EAX_x0 [SelfInitialization].
7:5	CacheLevel: cache level. Identifies the cache level. Value: 001b. See: CPUID Fn8000_001D_EAX_x0 [CacheLevel].
4:0	CacheType: cache type. Value: 02h. See: CPUID Fn8000_001D_EAX_x0 [CacheType].

CPUID Fn8000_001D_EAX_x2 Cache Properties

CPUID Fn8000_001D_EAX_x2 reports topology information for the L2. See [CPUID](#)

Fn8000_001D_EAX_x0.

Bits	Description
31:26	Reserved.
25:14	NumSharingCache: number of cores sharing cache. See: CPUID Fn8000_001D_EAX_x0[NumSharingCache] . Value: CPUID Fn8000_001E_EBX [ThreadsPerComputeUnit].
13:10	Reserved.
9	FullyAssociative: fully associative cache. Value: 0. See: CPUID Fn8000_001D_EAX_x0[FullyAssociative] .
8	SelfInitialization: cache is self-initializing. Value: 1. See: CPUID Fn8000_001D_EAX_x0[SelfInitialization] .
7:5	CacheLevel: cache level. Identifies the cache level. Value: 010b. See: CPUID Fn8000_001D_EAX_x0[CacheLevel] .
4:0	CacheType: cache type. Value: 03h. See: CPUID Fn8000_001D_EAX_x0[CacheType] .

CPUID Fn8000_001D_EAX_x3 Cache Properties

CPUID Fn8000_001D_EAX_x3 reports done/null. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:5	Reserved.
4:0	CacheType: cache type. Value: 00h. See: CPUID Fn8000_001D_EAX_x0[CacheType] .

CPUID Fn8000_001D_EBX_x0 Cache Properties

CPUID Fn8000_001D_EBX_x0 reports topology information for the DC. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:22	CacheNumWays: cache number of ways. Cache number of ways is CacheNumWays+1. Value: 007h.
21:12	CachePhysPartitions: cache physical line partitions. Value: 000h. Cache partitions is CachePhysPartitions+1.
11:0	CacheLineSize: cache line size in bytes. Value: 03Fh. Cache line size in bytes is CacheLineSize+1.

CPUID Fn8000_001D_EBX_x1 Cache Properties

CPUID Fn8000_001D_EBX_x1 reports topology information for the IC. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:22	CacheNumWays: cache number of ways. See: CPUID Fn8000_001D_EBX_x0[CacheNumWays] . Value: 001h.

21:12	CachePhysPartitions: cache physical line partitions. Value: 000h. See: CPUID Fn8000_001D_EBX_x0[CachePhysPartitions] .
11:0	CacheLineSize: cache line size in bytes. Value: 03Fh. See: CPUID Fn8000_001D_EBX_x0[CacheLineSize] .

CPUID Fn8000_001D_EBX_x2 Cache Properties

CPUID Fn8000_001D_EBX_x2 reports topology information for the L2. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:22	CacheNumWays: cache number of ways. Value: 00Fh. See: CPUID Fn8000_001D_EBX_x0[CacheNumWays] .
21:12	CachePhysPartitions: cache physical line partitions. Value: 000h. See: CPUID Fn8000_001D_EBX_x0[CachePhysPartitions] .
11:0	CacheLineSize: cache line size in bytes. Value: 03Fh. See: CPUID Fn8000_001D_EBX_x0[CacheLineSize] .

CPUID Fn8000_001D_EBX_x3 Cache Properties

CPUID Fn8000_001D_EAX_x3 reports done/null. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:22	CacheNumWays: cache number of ways. Value: 0. See: CPUID Fn8000_001D_EBX_x0[CacheNumWays] .
21:12	CachePhysPartitions: cache physical line partitions. Value: 000h. See: CPUID Fn8000_001D_EBX_x0[CachePhysPartitions] .
11:0	CacheLineSize: cache line size in bytes. Value: 0. See: CPUID Fn8000_001D_EBX_x0[CacheLineSize] .

CPUID Fn8000_001D_ECX_x0 Cache Properties

CPUID Fn8000_001D_ECX_x0 reports topology information for the DC. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:0	CacheNumSets: cache number of sets. Cache number of sets is CacheNumSets+1. Reports number of indexes. Value: 0000_003Fh.

CPUID Fn8000_001D(ECX_x1) Cache Properties

CPUID Fn8000_001D(ECX_x1) reports topology information for the IC. See [CPUID Fn8000_001D\(EAX_x0\)](#).

Bits	Description
31:0	CacheNumSets: cache number of sets. See: CPUID Fn8000_001D(ECX_x0)[CacheNumSets] . Value: 0000_00FFh.

CPUID Fn8000_001D(ECX_x2) Cache Properties

CPUID Fn8000_001D(ECX_x2) reports topology information for the L2. See [CPUID Fn8000_001D\(EAX_x0\)](#).

Bits	Description								
31:0	CacheNumSets: cache number of sets. Value: Product-specific. See: CPUID Fn8000_001D(ECX_x0)[CacheNumSets] . <table> <thead> <tr> <th>L2 Size</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>512 KB</td> <td>0000_01FFh.</td> </tr> <tr> <td>1 MB</td> <td>0000_03FFh.</td> </tr> <tr> <td>2 MB</td> <td>0000_07FFh.</td> </tr> </tbody> </table>	L2 Size	Value	512 KB	0000_01FFh.	1 MB	0000_03FFh.	2 MB	0000_07FFh.
L2 Size	Value								
512 KB	0000_01FFh.								
1 MB	0000_03FFh.								
2 MB	0000_07FFh.								

CPUID Fn8000_001D(ECX_x3) Cache Properties

CPUID Fn8000_001D(EAX_x3) reports done/null. See [CPUID Fn8000_001D\(EAX_x0\)](#).

Bits	Description
31:0	Reserved. Value: 0000_0000h.

CPUID Fn8000_001D(EDX_x0) Cache Properties

CPUID Fn8000_001D(EDX_x0) reports topology information for the DC. See [CPUID Fn8000_001D\(EAX_x0\)](#).

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Value: 0. 0=Cache is not inclusive of lower cache levels, as indicated by starthere1. 1=Cache is inclusive of lower cache levels.
0	WBINVD: Write-Back Invalidate/Invalidate. Value: 0. 0=WBINVD/INVD invalidates all lower level caches of non-originating cores sharing this cache. 1=WBINVD/INVD not ensured to invalidate all lower level caches of non-originating cores sharing this cache.

CPUID Fn8000_001D(EDX_x1) Cache Properties

CPUID Fn8000_001D(EDX_x1) reports topology information for the IC. See [CPUID Fn8000_001D\(EAX_x0\)](#).

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. Value: 0. See: CPUID Fn8000_001D_EDX_x0[CacheInclusive] .
0	WBINVD: Write-Back Invalidate/Invalidate. Value: 0. See: CPUID Fn8000_001D_EDX_x0[WBINVD] .

CPUID Fn8000_001D_EDX_x2 Cache Properties

CPUID Fn8000_001D_EDX_x2 reports topology information for the L2. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:2	Reserved.
1	CacheInclusive: cache inclusive. See: CPUID Fn8000_001D_EDX_x0[CacheInclusive] . Value: 1.
0	WBINVD: Write-Back Invalidate/Invalidate. Value: 0. See: CPUID Fn8000_001D_EDX_x0[WBINVD] .

CPUID Fn8000_001D_EDX_x3 Cache Properties

CPUID Fn8000_001D_EAX_x3 reports done/null. See [CPUID Fn8000_001D_EAX_x0](#).

Bits	Description
31:0	Reserved. Value: 0000_0000h.

CPUID Fn8000_001E_EAX Extended APIC ID

If [CPUID Fn8000_0001_ECX\[TopologyExtensions\]==0](#) then CPUID Fn8000_001E_E[D,C,B,A]X is reserved. If ([MSR0000_001B\[ApicEn\]==0](#)) then [CPUID Fn8000_001E_EAX\[ExtendedApicId\]](#) is reserved.

Bits	Description
31:0	ExtendedApicId: extended APIC ID. Value: IF (MSR0000_001B[ApicEn]==0) THEN 0000_0000h ELSE APIC20[31:0] ENDIF.

CPUID Fn8000_001E_EBX Compute Unit Identifiers

See [CPUID Fn8000_001E_EAX](#).

Bits	Description
31:16	Reserved.

15:8	ThreadsPerComputeUnit: threads per compute unit. The number of threads per compute unit is ThreadsPerComputeUnit+1. Value: 0.
7:0	ComputeUnitId: compute unit ID. Identifies the processor compute unit ID. Value: D18F3x12C[CpuNum].

CPUID Fn8000_001E(ECX) Node Identifiers

See [CPUID Fn8000_001E_EAX](#).

Bits	Description
31:0	Reserved.

CPUID Fn8000_001E_EDX Reserved

See [CPUID Fn8000_001E_EAX](#).

Bits	Description
31:0	Reserved.

3.19 MSRs - MSR0000_xxxx

See [3.1 \[Register Descriptions and Mnemonics\]](#) for a description of the register naming convention. MSRs are accessed through x86 WRMSR and RDMSR instructions.

MSR0000_0000 Load-Store MCA Address

Bits	Description
63:0	Alias of MSR0000_0402 .

MSR0000_0001 Load-Store MCA Status

Bits	Description
63:0	Alias of MSR0000_0401 .

MSR0000_0010 Time Stamp Counter (TSC)

Reset: 0000_0000_0000_0000h. [MSR0000_0010](#)[31:0] is derived from [D18F3x130](#)[TSC[31:0]]. [MSR0000_0010](#)[63:32] is derived from [D18F3x134](#)[TSC[63:32]].

Bits	Description
63:32	TSC[63:32]: time stamp counter high. See: TSC[31:0].
31:0	TSC[31:0]: time stamp counter low. Read-write; updated-by-hardware; S3-check-exclude. TSC[63:0] = {TSC[63:32],TSC[31:0]}. The TSC increments at the P0 frequency. This field uses software P-state numbering. See 2.5.3.1.1.1 [Software P-state Numbering] . The TSC counts at the same rate in all P-states, all C states, S0, or S1. A read of this MSR in guest mode is affected by MSRC000_0104 [Time Stamp Counter Ratio (TscRateMsr)] . The value (TSC/TSCRatio) is the TSC P0 frequency based value (as if TSCRatio==1.0) when (TSCRatio!=1.0).

MSR0000_001B APIC Base Address (APIC_BAR)

Bits	Description
63:40	MBZ.
39:12	ApicBar[39:12]: APIC base address register. Read-write. Reset: 00_FEE0_0h. Specifies the base address, physical address [39:12], for the APICXX register set in xAPIC mode. See 2.4.8.1.2 [APIC Register Space] .
11	ApicEn: APIC enable. Read-write. Reset: 0. See 2.4.8.1.2 [APIC Register Space] . 1=Local APIC is enabled in xAPIC mode. Intel warm reset state. MSR0000_001B [ApicEn] is aliased to D18F3x108 [ApicEn].
10	MBZ.
9	MBZ.
8	BSC: boot strap core. Read-write; updated-by-hardware. Reset: x. 1=The core is the boot core of the BSP. 0=The core is not the boot core of the BSP.
7:0	MBZ.

MSR0000_002A Cluster ID (EBL_CR_POWERON)

Read; GP-write. Writes to this register result in a GP fault with error code 0.

Bits	Description
63:18	MBZ.
17:16	ClusterID . Reset: 00b. The field does not affect hardware. MSR0000_002A [ClusterID] is an alias of MSRC001_1001 [ClusterID].
15:0	MBZ.

MSR0000_00E7 Max Performance Frequency Clock Count (MPERF)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	MPERF: maximum core clocks counter . Read-write; Updated-by-hardware . Incremented by hardware at the P0 frequency while the core is in C0. This register does not increment when the core is in the stop-grant state. In combination with MSR0000_00E8 , this is used to determine the effective frequency of the core. A read of this MSR in guest mode is affected by MSRC000_0104 [Time Stamp Counter Ratio (TscRateMsr)]. This field uses software P-state numbering. See MSRC001_0015 [Eff-FreqCntMwait], 2.5.3.3 [Effective Frequency], and 2.5.3.1.1.1 [Software P-state Numbering].

MSR0000_00E8 Actual Performance Frequency Clock Count (APERF)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	APERF: actual core clocks counter . Read-write; Updated-by-hardware . This register increments in proportion to the actual number of core clocks cycles while the core is in C0. The register does not increment when the core is in the stop-grant state. See MSR0000_00E7 .

MSR0000_00FE MTRR Capabilities (MTRRcap)

Read; GP-write. Reset: 0000_0000_0000_0508h.

Bits	Description
63:11	Reserved.
10	MtrrCapWc: write-combining memory type . 1=The write combining memory type is supported.
9	Reserved.
8	MtrrCapFix: fixed range register . 1=Fixed MTRRs are supported.
7:0	MtrrCapVCnt: variable range registers count . Specifies the number of variable MTRRs supported.

MSR0000_0174 SYSENTER CS (SYSENTER_CS)

Bits	Description
63:32	RAZ.

31:16	Reserved. Read-write.
15:0	SysEnterCS: SYSENTER target CS. Read-write. Reset: 0000h. Holds the called procedure code segment.

MSR0000_0175 SYSENTER ESP (SYSENTER_ESP)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:32	Reserved.
31:0	SysEnterESP: SYSENTER target SP. Read-write. Holds the called procedure stack pointer.

MSR0000_0176 SYSENTER EIP (SYSENTER_EIP)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:32	Reserved.
31:0	SysEnterEIP: SYSENTER target IP. Read-write. Holds the called procedure instruction pointer.

MSR0000_0179 Global Machine Check Capabilities (MCG_CAP)

Read; GP-write.

Bits	Description
63:9	Reserved.
8	McgCtlP: MCG_CTL register present. Value: 1. 1=The machine check control registers (MCi_CTL) are present. See 2.14.1 [Machine Check Architecture]
7:0	Count. Value: 06h. Indicates the number of error reporting banks visible to each core. 06h=Error-reporting banks 0 through 5. See 2.14.1.1 [Machine Check Registers] .

MSR0000_017A Global Machine Check Status (MCG_STAT)Reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#).

Bits	Description
63:3	Reserved.
2	MCIP: machine check in progress. Read-write; set-by-hardware. 1=A machine check is in progress.
1	EIPV: error instruction pointer valid. Read-write; Updated-by-hardware. 1=The instruction pointer that was pushed onto the stack by the machine check mechanism references the instruction that caused the machine check error.
0	RIPV: restart instruction pointer valid. Read-write; Updated-by-hardware. 1=Program execution can be reliably restarted at the EIP address on the stack. 0=The interrupt was not precise and/or the process (task) context may be corrupt; continued operation of this process may not be possible without intervention, however system processing or other processes may be able to continue with appropriate software clean up.

MSR0000_017B Global Machine Check Exception Reporting Control (MCG_CTL)

Read-write. Not shared. Reset: 0000_0000_0000_0000h. This register controls enablement of the individual error reporting banks; see [2.14.1 \[Machine Check Architecture\]](#). When a machine check register bank is not enabled in MCG_CTL, errors for that bank are not logged or reported, and actions enabled through the MCA are not taken; each MCi_CTL register identifies which errors are still corrected when MCG_CTL[i] is disabled.

Bits	Description
63:7	Unused.
6	Unused.
5	MC5En: MC5 register bank enable. 1=The MC5 machine check register bank is enabled.
4	MC4En: MC4 register bank enable. 1=The MC4 machine check register bank is enabled for all cores of the node. MSR0000_017B[MC4En] is an alias of D18F3x108[MceEn] .
3	Unused.
2	MC2En: MC2 register bank enable. 1=The MC2 machine check register bank is enabled.
1	MC1En: MC1 register bank enable. 1=The MC1 machine check register bank is enabled.
0	MC0En: MC0 register bank enable. 1=The MC0 machine check register bank is enabled.

MSR0000_01D9 Debug Control (DBG_CTL_MSR)

Bits	Description
63:7	Reserved.
6	MBZ.
5:2	PB: performance monitor pin control. Read-write. Reset: 0. This field does not control any hardware.
1	BTF. Read-write. Reset: 0. 1=Enable branch single step. See MSRC001_1010[TEN] .
0	LBR. Read-write. Reset: 0. 1=Enable last branch record.

MSR0000_01DB Last Branch From IP (BR_FROM)

Read; GP-write; [Not-same-for-all](#), [Updated-by-hardware](#). Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	LastBranchFromIP. Loaded with the segment offset of the branch instruction.

MSR0000_01DC Last Branch To IP (BR_TO)

Read; GP-write; [Not-same-for-all](#), [Updated-by-hardware](#). Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	LastBranchToIP. Holds the target RIP of the last branch that occurred before an exception or interrupt.

MSR0000_01DD Last Exception From IP

Read; GP-write; Not-same-for-all, Updated-by-hardware. Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	LastIntFromIP . Holds the source RIP of the last branch that occurred before the exception or interrupt.

MSR0000_01DE Last Exception To IP

Read; GP-write; Not-same-for-all, Updated-by-hardware. Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	LastIntToIP . Holds the target RIP of the last branch that occurred before the exception or interrupt.

MSR0000_020[F:0] Variable-Size MTRRs Base/Mask

Each MTRR (MSR0000_020[F:0] [Variable-Size MTRRs Base/Mask], MSR0000_02[6F:68,59:58,50], or MSR0000_02FF [MTRR Default Memory Type (MTRRdefType)]) specifies a physical address range and a corresponding memory type (MemType) associated with that range. Setting the memory type to an unsupported value results in a #GP.

The variable-size MTRRs come in pairs of base and mask registers (MSR0000_0200 and MSR0000_0201 are the first pair, etc.). Variables MTRRs are enabled through MSR0000_02FF[MtrrDefTypeEn]. A core access--with address CPUAddr--is determined to be within the address range of a variable-size MTRR if the following equation is true:

$$\text{CPUAddr}39:12 \& \text{PhyMask}[39:12] == \text{PhyBase}[39:12] \& \text{PhyMask}[39:12].$$

For example, if the variable MTRR spans 256 KB and starts at the 1 MB address. The PhyBase would be set to 0_0010_0000h and the PhyMask to F_FFFC_0000h (with zeros filling in for bits[11:0]). This results in a range from 0_0010_0000h to 0_0013_FFFF.

MSR0000_020[E,C,A,8,6,4,2,0] Variable-Size MTRRs Base

Table 190: Register Mapping for MSR0000_020[E,C,A,8,6,4,2,0]

Register	Function
MSR0000_0200	Range 0
MSR0000_0202	Range 1
MSR0000_0204	Range 2
MSR0000_0206	Range 3
MSR0000_0208	Range 4
MSR0000_020A	Range 5
MSR0000_020C	Range 6
MSR0000_020E	Range 7

Table 191: Valid Values for Memory Type Definition

Bits	Description
000b	UC or uncacheable.
001b	WC or write combining.
011b-010b	Reserved
100b	WT or write through.
101b	WP or write protect.
110b	WB or write back.
111b	Reserved

Bits	Description
63:40	MBZ.
39:12	PhyBase: base address. Read-write. Reset: 0.
11:3	MBZ.
2:0	MemType: memory type. Read-write. Reset: 0. Address range from 00000h to 0FFFFh. See: Table 191 [Valid Values for Memory Type Definition] .

MSR0000_020[F,D,B,9,7,5,3,1] Variable-Size MTRRs Mask

Table 192: Register Mapping for MSR0000_020[F,D,B,9,7,5,3,1]

Register	Function
MSR0000_0201	Range 0
MSR0000_0203	Range 1
MSR0000_0205	Range 2
MSR0000_0207	Range 3
MSR0000_0209	Range 4
MSR0000_020B	Range 5
MSR0000_020D	Range 6
MSR0000_020F	Range 7

Bits	Description
63:40	MBZ.
39:12	PhyMask: address mask. Read-write. Reset: 0.
11	Valid: valid. Read-write. Reset: 0. 1=The variable-size MTRR pair is enabled.
10:0	MBZ.

MSR0000_02[6F:68,59:58,50] Fixed-Size MTRRs

See [MSR0000_020\[F:0\]](#) for general MTRR information. Fixed MTRRs are enabled through [MSR0000_02FF\[MtrrDefTypeFixEn, MtrrDefTypeEn\]](#). For addresses below 1MB, the appropriate Fixed MTRRs override the default access destination. Each fixed MTRR includes two bits, RdDram and WrDram,

that determine the destination based on the access type.

See [2.4.6.1.2 \[Determining The Access Destination for Core Accesses\]](#).

Table 193: Register Mapping for [MSR0000_02\[6F:68,59:58,50\]](#)

Register	Function
MSR0000_0250	64K Range
MSR0000_0258	16K_0 Range
MSR0000_0259	16K_1 Range
MSR0000_0268	4K_0 Range
MSR0000_0269	4K_1 Range
MSR0000_026A	4K_2 Range
MSR0000_026B	4K_3 Range
MSR0000_026C	4K_4 Range
MSR0000_026D	4K_5 Range
MSR0000_026E	4K_6 Range
MSR0000_026F	4K_7 Range

Table 194: Field Mapping for [MSR0000_02\[6F:68,59:58,50\]](#)

Register	Bits							
	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
MSR0000_0250	64K_70000	64K_60000	64K_50000	64K_40000	64K_30000	64K_20000	64K_10000	64K_00000
MSR0000_0258	16K_9C000	16K_98000	16K_94000	16K_90000	16K_8C000	16K_88000	16K_84000	16K_80000
MSR0000_0259	16K_BC000	16K_B8000	16K_B4000	16K_B0000	16K_AC000	16K_A8000	16K_A4000	16K_A0000
MSR0000_0268	4K_C7000	4K_C6000	4K_C5000	4K_C4000	4K_C3000	4K_C2000	4K_C1000	4K_C0000
MSR0000_0269	4K_CF000	4K_CE000	4K_CD000	4K_CC000	4K_CB000	4K_CA000	4K_C9000	4K_C8000
MSR0000_026A	4K_D7000	4K_D6000	4K_D5000	4K_D4000	4K_D3000	4K_D2000	4K_D1000	4K_D0000
MSR0000_026B	4K_DF000	4K_DE000	4K_DD000	4K_DC000	4K_DB000	4K_DA000	4K_D9000	4K_D8000
MSR0000_026C	4K_E7000	4K_E6000	4K_E5000	4K_E4000	4K_E3000	4K_E2000	4K_E1000	4K_E0000
MSR0000_026D	4K_EF000	4K_EE000	4K_ED000	4K_EC000	4K_EB000	4K_EA000	4K_E9000	4K_E8000
MSR0000_026E	4K_F7000	4K_F6000	4K_F5000	4K_F4000	4K_F3000	4K_F2000	4K_F1000	4K_F0000
MSR0000_026F	4K_FF000	4K_FE000	4K_FD000	4K_FC000	4K_FB000	4K_FA000	4K_F9000	4K_F8000

Bits	Description
63:61	MBZ.
60	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
59	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
58:56	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
55:53	MBZ.
52	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
51	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
50:48	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
47:45	MBZ.

44	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
43	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
42:40	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
39:37	MBZ.
36	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
35	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
34:32	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
31:29	MBZ.
28	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
27	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
26:24	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
23:21	MBZ.
20	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
19	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
18:16	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
15:13	MBZ.
12	RdDram: read DRAM. See: MSR0000_02[6F:68,59:58,50][4] .
11	WrDram: write DRAM. See: MSR0000_02[6F:68,59:58,50][3] .
10:8	MemType: memory type. See: MSR0000_02[6F:68,59:58,50][2:0] .
7:5	MBZ.
4	RdDram: read DRAM. IF (MSRC001_0010[MtrrFixDramModEn]) THEN Read-write. ELSE MBZ. ENDIF. Reset: 0. 0=Read accesses to the range are marked as MMIO. 1=Read accesses to the range are marked as destined for DRAM. Address range from 00000h to 0FFFFh. See: MSRC001_0010[MtrrFixDramEn, MtrrFixDramModEn] .
3	WrDram: write DRAM. IF (MSRC001_0010[MtrrFixDramModEn]) THEN Read-write. ELSE MBZ. ENDIF. Reset: 0. 0=Write accesses to the range are marked as MMIO. 1=Write accesses to the range are marked as destined for DRAM. Address range from 00000h to 0FFFFh. See: MSRC001_0010[MtrrFixDramEn, MtrrFixDramModEn] .
2:0	MemType: memory type. Read-write. Reset: 0. Address range from 00000h to 0FFFFh. See: Table 191 [Valid Values for Memory Type Definition] .

MSR0000_0277 Page Attribute Table (PAT)

This register specifies the memory type based on the PAT, PCD, and PWT bits in the virtual address page tables.

Bits	Description
63:59	MBZ.
58:56	PA7MemType. See: PA0MemType. Reset: 0h. Default UC. MemType for {PAT, PCD, PWT} = 7h.
55:51	MBZ.
50:48	PA6MemType. See: PA0MemType. Reset: 7h. Default UC-. MemType for {PAT, PCD, PWT} = 6h.
47:43	MBZ.

42:40	PA5MemType . See: PA0MemType. Reset: 4h. Default WT. MemType for {PAT, PCD, PWT} = 5h.																				
39:35	MBZ.																				
34:32	PA4MemType . See: PA0MemType. Reset: 6h. Default WB. MemType for {PAT, PCD, PWT} = 4h.																				
31:27	MBZ.																				
26:24	PA3MemType . See: PA0MemType. Reset: 0h. Default UC. MemType for {PAT, PCD, PWT} = 3h.																				
23:19	MBZ.																				
18:16	PA2MemType . See: PA0MemType. Reset: 7h. Default UC-. MemType for {PAT, PCD, PWT} = 2h.																				
15:11	MBZ.																				
10:8	PA1MemType . See: PA0MemType. Reset: 4h. Default WT. MemType for {PAT, PCD, PWT} = 1h.																				
7:3	MBZ.																				
2:0	PA0MemType . Read-write. Reset: 6h. MemType for {PAT, PCD, PWT} = 0h. <table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>UC or uncacheable.</td> <td>4h</td> <td>WT or write through.</td> </tr> <tr> <td>1h</td> <td>WC or write combining.</td> <td>5h</td> <td>WP or write protect.</td> </tr> <tr> <td>2h</td> <td>MBZ.</td> <td>6h</td> <td>WB or write back.</td> </tr> <tr> <td>3h</td> <td>MBZ.</td> <td>7h</td> <td>UC- or uncacheable (overridden by WC state).</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	0h	UC or uncacheable.	4h	WT or write through.	1h	WC or write combining.	5h	WP or write protect.	2h	MBZ.	6h	WB or write back.	3h	MBZ.	7h	UC- or uncacheable (overridden by WC state).
Bits	Description	Bits	Description																		
0h	UC or uncacheable.	4h	WT or write through.																		
1h	WC or write combining.	5h	WP or write protect.																		
2h	MBZ.	6h	WB or write back.																		
3h	MBZ.	7h	UC- or uncacheable (overridden by WC state).																		

MSR0000_02FF MTRR Default Memory Type (MTRRdefType)See [MSR0000_020\[F:0\]](#) for general MTRR information.

Bits	Description
63:12	MBZ.
11	MtrrDefTypeEn: variable and fixed MTRR enable . Read-write. Reset: 0. 1= MSR0000_020[F:0] [Variable-Size MTRRs Base/Mask], and MSR0000_02[6F:68,59:58,50] [Fixed-Size MTRRs] are enabled. 0=Fixed and variable MTRRs are not enabled.
10	MtrrDefTypeFixEn: fixed MTRR enable . Read-write. Reset: 0. 1= MSR0000_02[6F:68,59:58,50] [Fixed-Size MTRRs] are enabled. This field is ignored (and the fixed MTRRs are not enabled) if MSR0000_02FF[MtrrDefTypeEn]=0 .
9:8	MBZ.
7:0	MemType: memory type . Read-write. Reset: 0. If MtrrDefTypeEn==1 then MemType specifies the memory type for memory space that is not specified by either the fixed or variable range MTRRs. If MtrrDefTypeEn==0 then the default memory type for all of memory is UC. Valid encodings are {00000b, MSR0000_02[6F:68,59:58,50][2:0] }.

MSR0000_0400 MC0 Machine Check Control (MC0_CTL)Read-write. Reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0044 \[DC Machine Check Control Mask \(MC0_CTL_MASK\)\]](#)

Bits	Description
63:12	Unused.
11	SRDE_ALL: all system read data errors . Report system read data errors for any operation including a DC/IC fetch, hardware prefetch, or TLB reload.

10	SRDET: read data errors on TLB reload. Report system read data errors on a TLB reload if MSR0000_0400[SRDE_ALL] = 1.
9	SRDES: read data errors on store. Report system read data errors on a store if MSR0000_0400[SRDE_ALL] = 1.
8	SRDEL: read data errors on load. Report system read data errors on a load if MSR0000_0400[SRDE_ALL] = 1.
7	TLB2M: L2DTLB multi-hit errors. Report L2DTLB multi-hit errors.
6	TLB2P: L2DTLB parity errors. Report TLB parity and multimatch errors.
5	TLB1M: L1DTLB multi-hit errors. Report L1DTLB multi-hit errors.
4	Unused.
3	DTP: tag array parity errors. Report data cache tag array parity errors.
2	DDP: data array parity errors. Report data cache data array parity errors.
1:0	Unused.

MSR0000_0401 MC0 Machine Check Status (MC0_STATUS)

See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0015](#)[McStatusWrEn]. Table 196 describes the error codes and status register settings for each error type. [MSR0000_0001](#) is an alias of [MSR0000_0401](#).

Bits	Description
63	Val: error valid. Read-write; set-by-hardware. Cold reset: 0. 1=This bit indicates that a valid error has been detected. This bit should be cleared to 0 by software after the register has been read.
62	Overflow: error overflow. Read-write; set-by-hardware. Cold reset: 0. 1=An error was detected while the valid bit (Val) was set; at least one error was not logged. Overflow is set independently of whether the existing error is overwritten. The following hierarchy identifies the error logging priorities. 1. Uncorrectable errors 2. Correctable errors The machine check mechanism handles the contents of MC <i>i</i> _STATUS during overflow as follows: <ul style="list-style-type: none">• Higher priority errors overwrite lower priority errors.• New errors of equal or lower priority do not overwrite existing errors.• Uncorrectable errors which are not logged due to overflow result in setting PCC, unless the new uncorrectable error is of the same type and in the same reportable address range as the existing error. Implementation note: Uncorrectable errors require software intervention. When an uncorrectable error occurs, the software must take action to prevent possible data corruption. However, if software cannot obtain the details of the error, it must behave pessimistically. Lost uncorrectable errors are signaled by Overflow and PCC; when software sees PCC, it considers the situation as fatal to the system. New uncorrectable errors of the same type and in the same reportable address range as existing errors may avoid setting PCC, even when setting Overflow.
61	UC: error uncorrected. Read-write; Updated-by-hardware. Cold reset: 0. 1=The error was not corrected by hardware.
60	En: error enable. Read-write; Updated-by-hardware. Cold reset: 0. 1=MCA error reporting is enabled for this error, as indicated by MC <i>i</i> _CTL.

59	MiscV: miscellaneous error register valid. Value: 0. 1=Valid thresholding in MSR0000_0403 .																				
58	AddrV: error address valid. Read-write; Updated-by-hardware. Cold reset: 0. 1=MCi_ADDR contains address information associated with the error.																				
57	PCC: processor context corrupt. Read-write; Updated-by-hardware. Cold reset: 0. 1=Hardware context held by the processor may have been corrupted. Continued operation of the system may have unpredictable results. The error is not recoverable or survivable, and the system should be reinitialized. See 2.14.1.6.1 [Differentiation Between System-Fatal and Process-Fatal Errors] . Implementation note 1: PCC errors are fatal to the system. Therefore, it is important not to set PCC unnecessarily. If the error results in global processor state which is no longer reliable or which may contain incorrect global information (e.g., corrupted cache tag, corrupted address), then PCC should be set to prevent random corruption. If the error affects only a single or known set of processes (e.g., corrupted data with good address and tags), then PCC should not be set. Implementation note 2: Errors which are imprecise do not automatically require PCC; as long as the error can be confined to a process, system operation can be salvaged and PCC should not be set. An imprecise interrupt is signalled by RIPV=0. Implementation note 3: Hardware must consider the effects of CPL when setting PCC. Hardware must ensure that the CPL reported on the MCA interrupt stack is the same as when the error occurred; if the value of CPL changes between the error and the MCE, the error was not contained and PCC should be set to 1. It is sufficient to ensure that the CPL has not changed from supervisor to user, as it is most important to identify if the error happened when the kernel was running.																				
56:45	Reserved.																				
44	Deferred: deferred error. Value: 0. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; the data is poisoned and an exception is deferred until the data is loaded by a core.																				
43	Poison: poison error. Value: 0. 1=The error was the result of attempting to consume poisoned data. This indicator does not apply to MSR0000_0411 [MC4 Machine Check Status (MC4_STATUS)] .																				
42:40	Reserved.																				
39	Reserved.																				
38:36	Way: cache way in error. Read-write; Updated-by-hardware. Cold reset: 0. Indicates the cache way for parity error only.																				
	<table> <thead> <tr> <th>Bits</th> <th>Description</th> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Way 0</td> <td>4h</td> <td>Way 4</td> </tr> <tr> <td>1h</td> <td>Way 1</td> <td>5h</td> <td>Way 5</td> </tr> <tr> <td>2h</td> <td>Way 2</td> <td>6h</td> <td>Way 6</td> </tr> <tr> <td>3h</td> <td>Way 3</td> <td>7h</td> <td>Way 7</td> </tr> </tbody> </table>	Bits	Description	Bits	Description	0h	Way 0	4h	Way 4	1h	Way 1	5h	Way 5	2h	Way 2	6h	Way 6	3h	Way 3	7h	Way 7
Bits	Description	Bits	Description																		
0h	Way 0	4h	Way 4																		
1h	Way 1	5h	Way 5																		
2h	Way 2	6h	Way 6																		
3h	Way 3	7h	Way 7																		

35:21	Reserved.
20:16	ErrorCodeExt: extended error code. Read-write; Updated-by-hardware. Cold reset: 0. Logs an extended error code when an error is detected. This model-specific field is used in conjunction with ErrorCode to identify the error sub-type for root cause analysis (see 2.14.1.5 [Error Code]). See Table 196 for expected values.
15:0	ErrorCode: error code. Read-write; Updated-by-hardware. Cold reset: 0. See 2.14.1.5 [Error Code] for details on decoding this field. See Table 196 for expected values.

Table 195: MC0 Error Descriptions

Error Type	Error Sub-type	Description ¹	CTL ²	EAC ³
Data Parity		A DC data parity error for a tag hit occurred during an LS access to the DC.	DDP	E
Tag Parity		A DC tag array parity error for a data hit occurred during an LS access to the DC.	DTP	E
Copyback Parity		A DC data or tag array parity error for a tag miss occurred during an LS access to the DC.	DDP, DTP	E
Tag Snoop Parity		A tag parity error was encountered during snoop. Data array parity check enabled only for tag hit.	DDP, DTP	E
L2 TLB Error	TLB parity	Parity error in BTLB. Regardless of whether this error is masked from logging, it will invalidate the lookup index (for both 4k and 2M storage) where the error occurred and an L2DTLB miss will be generated.	TLB2P	E
L1 TLB Error ⁴	TLB multimatch	Hit multiple entries. Regardless of whether this error is masked from logging or enabled for SyncFlood generation, the L1DTLB will be flushed.	TLB1M	E
L2 TLB Error ⁴	TLB multimatch	Hit multiple entries. (linear tags) Regardless of whether this error is masked from logging, it will invalidate the lookup index (for both 4k and 2M storage) where the error occurred and an L2DTLB miss will be generated.	TLB2M	E
System Read Data Error	TLB Reload	System read data error occurred on a TLB reload.	SRDET	E
	Store	System read data error occurred on a store.	SRDES	E
	Load	System read data error occurred on a load or hardware prefetch.	SRDEL	E

1. CID: core ID. All LS errors are reported to the affected core; see [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).
2. See [MSR0000_0400](#).
3. EAC: D=Error action taken if detected. E=Error action taken if MCA bank enabled. See [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).

Table 196: MC0 Error Signatures

Error Type	Error	Error Code Ext	Error Code						UC	ADDRV	PCC
			Type	UU/PP	T	RRRR	II/TT	LL			
Data Parity	Load,	0h	MEM	-	-	DRD	Data	L1	1	1	0
	Store	0h		-	-	DWR	Data	L1	1	1	1
Tag Parity	Load,	10h		-	-	DRD	Data	L1	1	1	1
	Store	10h		-	-	DWR	Data	L1	1	1	1
Copyback Parity	-	0h		-	-	Evict	Data	L1	1	1	1
Tag Snoop Parity	-	10h		-	-	Snoop	Data	L1	1	1	1
L2DTLB Parity	-	0h	TLB	-	-	-	Data	L2	0	1	0
L1DTLB Multimatch	-	1h		-	-	-	Data	L1	0 ¹	1	0 ¹
L2DTLB Multimatch	-	1h		-	-	-	Data	L2	0	1	0
Read Data Error on TLB Reload	-	0h	BUS	SRC	0	RD	MEM/I O	LG	1	1	1
Read Data Error on Store	-	0h		SRC	0	DWR	MEM/I O	LG	1	1	1
Read Data Error on Load	-	0h		SRC	0	DRD	MEM/I O	LG	1	1	1
1. If an MCA error causes an unlocking store to miss in both the L1DTLB and L2DTLB, the error is uncorrectable. Both PCC and UC will be set to '1'.											

MSR0000_0402 MC0 Machine Check Address (MC0_ADDR)

Read-write; Updated-by-hardware. Cold reset: 0000_0000_0000_0000h. The MCi_ADDR register contains valid data if indicated by MCi_STATUS[AddrV]. See 2.14.1 [Machine Check Architecture]. [MSR0000_0000](#) is an alias of [MSR0000_0402](#).

Bits	Description
63:0	ADDR: Address. See Table 197 .

Table 197: MC0 Address Register

Error Type	Error Sub-type	Bits	Description
Data or Tag Parity	Load, Store, HW Prefetch	39:4	PhysAddr[39:4].
Copyback Parity		11:6	PhysAddr[11:6].
Tag Snoop Parity		39:6	PhysAddr[39:6].
BTLB Parity		47:12	LinAddr[47:12].
BTLB Multimatch			
Read Data Error	TLB Reload, Load, or Store	39:4	PhysAddr[39:4].

MSR0000_0403 MC0 Machine Check Miscellaneous (MC0_MISC)

Bits	Description
63:0	Reserved.

MSR0000_0404 MC1 Machine Check Control (MC1_CTL)

Read-write.

Reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#).

Bits	Description
63:13	Unused.
12	Unused.
11:10	Unused.
9	SRDE: read data errors. Report system read data errors for an instruction cache fetch if MSR0000_0400[SRDE_ALL] = 1.
8:7	Unused.
6	TLBP: TLB parity errors. Report TLB parity errors. BTLB Parity and Multimatch.
5	Unused.
4	ISTP: snoop tag array parity errors. Report instruction cache snoop tag array parity errors which occur during snoop.
3	ITP: tag array parity errors. Report instruction cache tag array parity errors.
2	IDP: data array parity errors. Report instruction cache data array parity errors.
1	IVP: victim parity errors. Report victim parity errors.
0	PRPE: ME patch RAM parity error. Report patch ram parity errors.

MSR0000_0405 MC1 Machine Check Status (MC1_STATUS)See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0015\[McStatusWrEn\]](#). [Table 198](#) describes each error type. [Table 199](#) describes the error codes and status register settings for each error type.

Bits	Description
63	Val: error valid. See: MSR0000_0401[Val] .
62	Overflow: error overflow. See: MSR0000_0401[Overflow] .
61	UC: error uncorrected. See: MSR0000_0401[UC] .
60	En: error enable. See: MSR0000_0401[En] .
59	MiscV: miscellaneous error register valid. Value: 0. See: MSR0000_0401[MiscV] . 1=Valid thresholding in MSR0000_0407 .
58	AddrV: error address valid. See: MSR0000_0401[AddrV] .
57	PCC: processor context corrupt. See: MSR0000_0401[PCC] .
56:40	Reserved.

39:36	Way: cache way in error. Read-write; Updated-by-hardware. Cold reset: 0. Indicates the cache way in error. <table border="1"> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Way 0</td></tr> <tr> <td>1h</td><td>Way 1</td></tr> <tr> <td>Fh-2h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	0h	Way 0	1h	Way 1	Fh-2h	Reserved
Bits	Description								
0h	Way 0								
1h	Way 1								
Fh-2h	Reserved								
35:28	Reserved.								
27:24	PRParity[3:0]: ME Patch Ram Parity [3:0]. Read-write; updated-by-hardware. Cold reset: 0.								
23:21	Reserved.								
20:16	ErrorCodeExt: extended error code. Read-write; updated-by-hardware. Cold reset: 0. See Table 199 for expected values.								
15:0	ErrorCode: error code. Read-write; updated-by-hardware. Cold reset: 0. See 2.14.1.5 [Error Code] for details on decoding this field. See Table 199 for expected values.								

Table 198: MC1 Error Descriptions

Error Type	Error	Description	CTL ³	CID ²	EAC ¹
Read Data Error		An error occurred during an attempted read of data from the NB. Possible reasons include master abort and target abort.	SRDE		
Data or Tag Parity		An IC data or tag array parity error for a tag hit occurred during instruction fetch from the IC. The data is discarded from the IC, the data array and all tag arrays are cleared, and the line is refetched. IC parity errors may occur on non-cacheable instructions. Non-cacheable instructions pass through the instruction cache but are not marked as valid cache lines.	IDP, ITP		
Tag Snoop		A tag error was encountered during snoop or victimization.	ISTP		
Victim Parity		IC Tag parity error as a result of victim cast-out.	IVP		
BTLB Parity		Parity error in BTLB.	TLBP		
BTLB Multimatch		Hit multiple entries (linear tags).	TLBP		
PRPE PatchRam Parity		Microcode Patch RAM Parity Error	PRPE		

1. EAC: D=Error action taken if detected. E=Error action taken if MCA bank enabled. See [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).
2. CID: core ID. A=Error reported to the affected core. 0=Error reported to core 0 of the L2 complex. B=Error reported to all cores of the L2 complex. See [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).
3. See [MSR0000_0404](#).

Table 199: MC1 Error Signatures

Error Type	Error	Error Code Ext	Error Code						UC	ADDRV	PCC
			Type	PP	TT	RRRR	II/TT	LL			
Read Data Error		0h	BUS	SRC	0	IRD	MEM	LG	1	1	0
Data Parity		0h	MEM	-	-	IRD	Instr	L1	0 ¹	1	0
Tag Parity		1h	MEM	-	-	IRD	Instr	L1	0 ¹	1	0
Tag Snoop		0h	MEM	-	-	Snoop	Instr	L1	1	1	1
Victim Parity		0h	MEM	-	-	-	Instr	L1	0 ³	1	0
BTLB Parity		0h	TLB	-	-	-	Instr	L2	0 ²	1	0
BTLB Multimatch		1h	TLB	-	-	-	Instr	L2	0 ²	1	0
PRPE PatchRam Parity		2h	MEM	-	-	-	Instr	LG	1	1	0

MSR0000_0406 MC1 Machine Check Address (MC1_ADDR)

Read-write; Updated-by-hardware. Cold reset: 0000_0000_0000_0000h. The MCi_ADDR register contains valid data if indicated by MCi_STATUS[AddrV]. See [2.14.1 \[Machine Check Architecture\]](#).

Bits	Description
63:0	ADDR: Address. See Table 200 .

The following table defines the address register as a function of error type.

Table 200: MC1 Address Register

Error Type	Error Sub-Type	Bits	Description
IC Data and Tag Parity		47:4	Linear address
Tag Snoop		39:6	Physical address
Victim Parity		47:6	Linear Address
BTLB Parity		47:4	Linear address
BTLB Multimatch			
PRPE PatchRam ParityError		12:0	Patch Ram Address
BU Read Data Error	-	63:40	Reserved.
		39:6	PhysAddr[47:6].
		5:0	Reserved.

MSR0000_0407 MC1 Machine Check Miscellaneous (MC1_MISC)

Bits	Description
63:0	Reserved.

MSR0000_0408 MC2 Machine Check Control (MC2_CTL)

Read-write; [Per-L2](#); not-same-for-all.

Reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0046 \[BU Machine Check Control Mask \(MC2_CTL_MASK\)\]](#).

Bits	Description
63:14	Unused.
13	AttrParity: attribute parity errors.
12:9	Unused.
8	DataUncor: uncorrectable data errors.
7	DataCor: correctable data errors.
6	DataParity: data parity errors.
5	TagUncor: uncorrectable tag errors.
4	TagCor: correctable tag errors.
3	Unused.
2	IBUFF: NB read response error due to a fill.
1	OBUFF: NB read response error due to a write/victim.
0	Unused.

MSR0000_0409 MC2 Machine Check Status (MC2_STATUS)

IF ([MSRC001_10A0\[McaToMstCoreEn\]](#)) THEN [Per-L2](#); not-same-for-all. ENDIF. See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0015\[McStatusWrEn\]](#). [Table 201](#) describes each error type. [Table 202](#) describes the error codes and status register settings for each error type. See [MSRC001_10A0\[McaToMstCoreEn\]](#).

Bits	Description
63	Val: error valid. See: MSR0000_0401[Val] .
62	Overflow: error overflow. See: MSR0000_0401[Overflow] . Errors in the L2 data array are only corrected with scrub (read-modify-write) operations. As a result, the same L2 data error may be detected and logged multiple times causing MSR0000_0409[Overflow] to be set. Errors in the L2 tag array are typically corrected when the tags are accessed but there are scenarios when the error is not corrected. As a result the same L2 tag error may be detected and logged multiple times causing MSR0000_0409[Overflow] to be set. Some combinations of MSRC001_0046 [BU Machine Check Control Mask (MC2_CTL_MASK)] partial masks will result in MSR0000_0409[Overflow] being set without an overflow condition.
61	UC: error uncorrected. See: MSR0000_0401[UC] .
60	En: error enable. See: MSR0000_0401[En] .

59	MiscV: miscellaneous error register valid. Value: 0. See: MSR0000_0401 [MiscV]. 1=Valid thresholding in MSR0000_040B .								
58	AddrV: error address valid. See: MSR0000_0401 [AddrV].								
57	PCC: processor context corrupt. See: MSR0000_0401 [PCC].								
56	ErrCoreIdVal. Read-write; Updated-by-hardware. Cold reset: 0. 1=The ErrCoreId field is valid. ErrCoreIdVal is not set for L2I Rinse or Scrub operations.								
55	Reserved.								
54:47	<p>Syndrome[7:0]. Read-write; Updated-by-hardware. Cold reset: 0. The syndrome bits when an ECC error is detected. See Table 202 for when Syndrome is valid. Syndrome[15:0] = {Syndrome[15:8], Syndrome[7:0]}.</p> <table> <thead> <tr> <th>Array</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>L2 Tag</td> <td>Syndrome[7:0]. (Syndrome[15:8] is 0)</td> </tr> <tr> <td>L2 Data</td> <td>Syndrome[8:0]. (Syndrome[15:9] is 0)</td> </tr> <tr> <td>NbRead, NbFill</td> <td>Syndrome[15:0]. Even parity.</td> </tr> </tbody> </table> <p>Syndrome[15:0] even parity calculation:</p> <ul style="list-style-type: none"> • Par[0] = Dat[0] ^ Dat[8] ^ Dat[16] ^ Dat[24] ^ Dat[32] ^ Dat[40] ^ Dat[48] ^ Dat[56] • Par[1] = Dat[1] ^ Dat[9] ^ Dat[17] ^ Dat[25] ^ Dat[33] ^ Dat[41] ^ Dat[49] ^ Dat[57] • ... • Par[7] = Dat[7] ^ Dat[15] ^ Dat[23] ^ Dat[31] ^ Dat[39] ^ Dat[47] ^ Dat[55] ^ Dat[63] • Par[8] = Dat[64] ^ Dat[72] ^ Dat[80] ^ Dat[88] ^ Dat[96] ^ Dat[104] ^ Dat[112] ^ Dat[120] • Par[9] = Dat[65] ^ Dat[73] ^ Dat[81] ^ Dat[89] ^ Dat[97] ^ Dat[105] ^ Dat[113] ^ Dat[121] • ... • Par[15] = Dat[71] ^ Dat[79] ^ Dat[87] ^ Dat[95] ^ Dat[103] ^ Dat[111] ^ Dat[119] ^ Dat[127] <p>In rare instances, an error that sets UECC=1 will log a correctable error syndrome. This is due to detection of a single-bit ECC error with no corresponding parity error, which can indicate the presence of a multi-bit ECC error, or a single-bit ECC error and an error in the parity bit. This can only happen on a write of attributes from L1 to L2.</p>	Array	Description	L2 Tag	Syndrome[7:0]. (Syndrome[15:8] is 0)	L2 Data	Syndrome[8:0]. (Syndrome[15:9] is 0)	NbRead, NbFill	Syndrome[15:0]. Even parity.
Array	Description								
L2 Tag	Syndrome[7:0]. (Syndrome[15:8] is 0)								
L2 Data	Syndrome[8:0]. (Syndrome[15:9] is 0)								
NbRead, NbFill	Syndrome[15:0]. Even parity.								
46	CECC: correctable ECC error. Read-write; Updated-by-hardware. Cold reset: 0. 1=The error was a correctable ECC error.								
45	UECC: uncorrectable ECC error. Read-write; updated-by-hardware. Cold reset: 0. 1=The error was an uncorrectable ECC error.								
44	Deferred: deferred error. See: MSR0000_0401 [Deferred].								
43	Poison: poison error. See: MSR0000_0401 [Poison].								
42	Reserved.								

41:36	<p>Way: cache way/entry in error. Read-write; Updated-by-hardware. Cold reset: 0. Indicates the cache way in error. See Table 202 for when Way is valid and what ways are valid.</p> <pre> IF ((ErrorCodeExt==00100b)) THEN CRQ IBUFF error location specified by {Way, MSR0000_040A[5:4]}. ELSEIF ((ErrorCodeExt==00101b)) THEN CRQ OBUFF error location specified by {Way, MSR0000_040A[5:4]}. ELSE Bits Description 00h Way 0 01h Way 1 0Eh-02h Way <Way> 0Fh Way 15 ENDIF </pre>
35:32	ErrCoreId. Read-write; Updated-by-hardware. Cold reset: 0. When ErrCoreIdVal=1, this field indicates which core within the processor is associated with the error; Otherwise this field is reserved.
31:24	Syndrome[15:8]. See: MSR0000_0409 [Syndrome[7:0]].
23:21	Reserved.
20:16	ErrorCodeExt: extended error code. Read-write; updated-by-hardware. Cold reset: 0. See MSR0000_0401 [ErrorCodeExt]. See Table 202 for expected values.
15:0	ErrorCode: error code. Read-write; Updated-by-hardware. Cold reset: 0. See 2.14.1.5 [Error Code] for details on decoding this field. See Table 202 for expected values.

Table 201: MC2 Error Descriptions

Error Type	Error	Description	CTL ³	CID ²	EAC ¹
NB	IBUFF	A parity error occurred in the IBUFF.	IBUFF	-	E ¹
NB	OBUFF	Aparity error occurred in the OBUFF.	OBUFF	-	E ¹
L2 Cache	L2Tag	A correctable or uncorrectable ECC error was seen in the L2 tag.	TagCor, TagUncor	-	E ¹
L2 Cache	L2Data	A correctable or uncorrectable ECC error was seen in the L2 data array.	DataParity, DataCor, DataUncor.	-	E ¹
Attribute Parity	Par	A parity error was seen in the L2 attribute bits. This error was corrected by hardware.	AttrParity	A ²	E ¹

1. EAC: The error action is taken if detected for all CU errors. D=Error action taken if detected. E=Error action taken if MCA bank enabled. See [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#). If any core in the L2 complex has MCG_CTL[2] asserted, the MCA logic in the L2I is enabled.
2. CID: core ID. A=Error reported to the affected core. 0=Error reported to core 0 of the L2 complex; see [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).
3. See [MSR0000_0408](#).
4. Error Action: Sync flood=Take sync flood if PCC=1. None=No action other than that specified by MCA.

Table 202: MC2 Error Signatures

Error Type	Error Sub-Type	Sub	ErrorCodeExt	Error Code						UC	ADDRV	PCC	Syndrome	Way	CECC	UECC	ErrCoreIdVal
				Type	PP	T	RRRR	II/TT	LL								
NB	IBUFF	-	04h	MEM	-	-	RD	G	L2	1	1	1	15:0	5:0	0	0	0
	OBUFF		05h				WR										
Tag	Cor	BankReq	09h	MEM	-	-	GEN	G	L2	0/1 ¹	1	0/UC ¹	7:0	3:0	1/0	0/1 ¹	1
		Prb	0Ah				Probe										
		Fill	0Bh				RD										
Tag	Uncor	BankReq	0Dh	MEM	-	-	GEN	G	L2	1	1	1	7:0	3:0	0	1	1
		Prb	0Eh				Probe										
		Fill	0Fh				RD										
Data	Cor	Hit	10h	MEM	-	-	RD	G	L2	0/1 ²	1	0/UC ²	8:0	3:0	1/0	0/1 ²	1
		Attr	11h				GEN										
		Vict	12h				Evict										
		Fill	13h				RD										
Data	Uncor	Hit	14h	MEM	-	-	RD	G	L2	1	1	1	8:0	3:0	0	1	1
		Attr	15h				GEN										
		Vict	16h				Evict										
		Fill	17h				RD										
Data	Par	Hit	18h	MEM	-	-	RD	G	L2	0	1	0	-	3:0	0	0	1
		Attr	19h				GEN										
		Fill	1Bh				IRD										
Attr	Par	Hit	1Ch	MEM	-	-	RD	G	L2	0	1	0	-	3:0	0	0	1
		Attr	1Dh				GEN										
		Fill	1Fh				IRD										

MSR0000_040A MC2 Machine Check Address (MC2_ADDR)

Read-write; Updated-by-hardware. Cold reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). The following table defines the address register as a function of error type.

This register is shared by all cores of the L2 complex when the [MSRC001_10A0\[McaToMstCoreEn\]==0](#).

When ([MSRC001_10A0\[McaToMstCoreEn\]==1](#)), only the lowest enabled core in the complex can read/write this register. All other cores will read all 0s and writes will be ignored.

Bits	Description
63:40	Reserved.
39:4	ADDR . Read-write; updated-by-hardware. See Table 203 .
3:0	Reserved.

Table 203: MC2 Address Register

Error Type	Error Sub-Type	Bits	Description
L2 Tag	ErrorCodeExt=0 9h to 0Fh.	63:17	Reseved.
		16:6	PhysAddr[16:6].
		5:0	Reseved.
Data, Attr, NB	ErrorCodeExt=0 4h to 05h, 10h to 1Fh.	63:40	RAZ
		39:4	PhysAddr[39:4].
		3:0	RAZ

MSR0000_040B MC2 Machine Check Miscellaneous (MC2_MISC)

Bits	Description
63:0	Reserved.

MSR0000_040C MC3 Machine Check Control (MC3_CTL)

Reset: 0000_0000_0000_0000h. Read-only.

Bits	Description
63:0	Unused.

MSR0000_040D MC3 Machine Check Status (MC3_STATUS)Reset: 0. See [MSRC001_0015](#)[McStatusWrEn].

Bits	Description
63:0	Reserved.

MSR0000_040E MC3 Machine Check Address (MC3_ADDR)

Reset: 0000_0000_0000_0000h. Read-only.

Bits	Description
63:0	Reserved.

MSR0000_040F MC3 Machine Check Miscellaneous (MC3_MISC)

Reset: 0000_0000_0000_0000h. Read-only.

Bits	Description
63:0	Reserved.

MSR0000_0410 MC4 Machine Check Control (MC4_CTL)Read-write; [Not-same-for-all](#). Reset: 0000_0000_0000_0000h.

MSR0000_0410[31:0] is an alias of **D18F3x40**, which is accessible through PCI configuration space. Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#). Accessibility of this register by non-NBC cores is affected by **D18F3x44**[NbMcaToMstCpuEn].

See **D18F3x44** [[MCA NB Configuration](#)] for further NB MCA configuration controls. See [2.14.1 \[Machine Check Architecture\]](#) for a general description of the machine check architecture. See [MSRC001_0048](#) [[NB Machine Check Control Mask \(MC4_CTL_MASK\)](#)] for the corresponding error mask register.

Bits	Description
63:32	Unused.
31	McaCpuDatErrEn: L2 complex data error. 1=Enables MCA reporting of CPU data errors sent to the NB.
29:28	Unused. Read-write.
27	Unused. Read-write.
26	NbArrayParEn: northbridge array parity error reporting enable. 1=Enables reporting of parity errors in the NB arrays.
25	UsPwDatErrEn: upstream data error enable. Read-write. 1=Enables MCA reporting of upstream posted writes in which the EP bit is set as indicated by the ONION error bits.
24:18	Unused. Read-write.
17	CpPktDatEn: completion packet error reporting enable. Read-write. 1=Enables MCA reporting of completion packets with the EP bit set. Any response packet with data errors detected by ONION will generate this error.
16	NbIntProtEn: northbridge internal bus (ONION) protocol error reporting enable. Read-write. 1=Enables MCA reporting of protocol errors detected on the northbridge internal bus (ONION). When possible, this enable should be cleared before initiating a warm reset to avoid logging spurious errors due to RESET_L signal skew.
15:13	Unused. Read-write.
12	WDTRptEn: watchdog timer error reporting enable. 1=Enables MCA reporting of watchdog timer errors. The watchdog timer checks for NB system accesses for which a response is expected but no response is received. See D18F3x44 [MCA NB Configuration] for information regarding configuration of the watchdog timer duration. This bit does not affect operation of the watchdog timer in terms of its ability to complete an access that would otherwise cause a system hang. This bit only affects whether such errors are reported through MCA.
11	AtomicRMWEn: atomic read-modify-write error reporting enable. 1=Enables MCA reporting of atomic read-modify-write (RMW) commands received from an IO link. Atomic RMW commands are not supported. An atomic RMW command results in a link error response being generated back to the requesting IO device. The generation of the link error response is not affected by this bit.
10	Unused. Read-write.
9	TgtAbortEn: target abort error reporting enable. 1=Enables MCA reporting of target aborts to a link. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of this bit.
8	MstrAbortEn: master abort error reporting enable. 1=Enables MCA reporting of master aborts to a link. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of this bit.
7:6	Unused. Read-write.

5	SyncPktEn: link sync packet error reporting enable. 1=Enables MCA reporting of link-defined sync error packets detected on link. The NB floods its outgoing link with sync packets after detecting a sync packet on the incoming link independent of the state of this bit.
4:2	Unused. Read-write.
1	UECCEn: uncorrectable ECC error reporting enable. 1=Enables MCA reporting of DDR3 DRAM uncorrectable ECC errors which are detected in the NB. In some cases data may be forwarded to the core prior to checking ECC in which case the check takes place in one of the other error reporting banks.
0	CECCEn: correctable ECC error reporting enable. 1=Enables MCA reporting of DDR3 DRAM correctable ECC errors which are detected in the NB.

MSR0000_0411 MC4 Machine Check Status (MC4_STATUS)

Not-same-for-all. Cold reset: 0000_0000_0000_0000h.

MSR0000_0411[63:32] is an alias of D18F3x4C, and MSR0000_0411[31:0] is an alias of D18F3x48. Only one of these registers exists in multi-core devices; see 3.1.1 [Northbridge MSRs In Multi-Core Products]. Accessibility of this register by non-NBC cores is affected by D18F3x44[NbMcaToMstCpuEn]. See MSRC001_0015[McStatusWrEn] for information on writing to this register. See 2.14.1 [Machine Check Architecture] for machine check architecture background.

Table 204 describes each error type. Table 205 and Table 206 describe the error codes and status register settings for each error type.

Bits	Description
63	Val: valid. See: MSR0000_0401[Val] .
62	Overflow: error overflow. See: MSR0000_0401[Overflow] .
61	UC: error uncorrected. See: MSR0000_0401[UC] .
60	En: error enable. See: MSR0000_0401[En] .
59	MiscV: miscellaneous error register valid. See: MSR0000_0401[MiscV] . 1=Valid thresholding in MSR0000_0413 or MSRC000_0408 .
58	AddrV: error address valid. See: MSR0000_0401[AddrV] .
57	PCC: processor context corrupt. See: MSR0000_0401[PCC] .
56	ErrCoreIdVal: error core ID is valid. Read-write; set-by-hardware. 1=The ErrCoreId field is valid.
55	Reserved. Placeholder for TCC.
54:47	Syndrome[7:0]. Read-write. Syndrome[15:0] = {Syndrome[15:8], Syndrome[7:0]}. The syndrome bits when an ECC error is detected. See Table 206 Valid Syndrome column for which bits are valid for each error.
46	CECC: correctable ECC error. Read-write; Updated-by-hardware. 1=The error was a correctable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. If CECC is set with UECC, indicates that an error was detected by the hardware-managed history scheme.
45	UECC: uncorrectable ECC error. Read-write; Updated-by-hardware. 1=The error was an uncorrectable ECC error according to the restrictions of the ECC algorithm. UC indicates whether the error was actually corrected by the processor. If UECC is set with CECC, indicates that an error was detected by the hardware-managed history scheme.

44	Deferred: deferred error. Read-write; Updated-by-hardware. 1=A deferred error was created. A deferred error is the result of an uncorrectable data error which did not immediately cause a processor exception; the data is poisoned and an exception is deferred until the data is consumed.
43:42	Reserved.
41	SubLink: sublink. Read-write; set-by-hardware. For errors associated with a link, this bit indicates if the error was associated with the upper or lower byte of the link. 0=Sublink [7:0]. 1=Sublink [15:8].
40	Scrub: error detected on a scrub. Read-write; Set-by-hardware.
35:32	ErrCoreId: error associated with core N. Read-write; updated-by-hardware. When ErrCoreIdVal=1 this field indicates which core within the processor is associated with the error; Otherwise this field is reserved. All values greater than D18F5x84[CmpCap] are reserved.
31:24	Reserved. Read-write.
23:21	Reserved.
20:16	ErrorCodeExt: extended error code. Read-write; Updated-by-hardware. See MSR0000_0401[ErrorCodeExt] . See Table 205 for values.
15:0	ErrorCode: error code. Read-write; Updated-by-hardware. See 2.14.1.5 [Error Code] .

Table 204: MC4 Error Descriptions

Error Type	Description	CTL ¹	ETG ²	EAC ⁴
Sync Error	Link-defined sync error packets detected on link. The NB floods its outgoing links with sync packets after detecting a sync packet on an incoming link independent of the state of the control bits.	SyncPktEn	L	D
Master Abort	Master abort seen as result of link operation. Reasons for this error include requests to non-existent addresses. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of the control bit.	MstrAbortEn	L	D
Target Abort	Target abort seen as result of link operation. The NB returns an error response back to the requestor with any associated data all 1s independent of the state of the control bit.	TgtAbortEn	L	D
RMW Error	An atomic read-modify-write (RMW) command was received from an IO link. Atomic RMW commands are not supported. An atomic RMW command results in a link error response being generated back to the requesting IO device. The generation of the link error response is not affected by the control bit.	AtomicRMWEn	L	D
WDT Error	NB WDT timeout due to lack of progress. The NB WDT monitors transaction completions. A transaction that exceeds the programmed time limit reports errors via the MCA. The cause of error may be another node or device which failed to respond.	WDTRptEn	L	D
DRAM ECC Error	A DRAM ECC error detected.	CECCEn, UECCEn	D	D
DRAM CRC Error	A DRAM CRC error was detected.	CCRCEn, UCRCEn	D	D

Table 204: MC4 Error Descriptions

Error Type	Description	CTL ¹	ETG ²	EAC ⁴
Link Data Error	Data error detected on link. If enabled for reporting and the request is sourced from a core, then PCC is set. (If not enabled for reporting, PCC is not set. If configured to allow an error response to be returned to the core, this could allow error containment to a scope smaller than the entire system.)	McaUsPwDat ErrEn, CpPktDatEn	L	D
Protocol Error	Protocol error detected by link. Additional hardware assertion protocol errors may be enabled via D18F3x18C[EnHwAssertProtErr] for debug purposes. These errors are distinguished from each other by the value in MSR0000_0412[ErrAddr] . See Table 208 . For protocol errors, the system cannot continue operation. Protocol errors can be caused by other subcomponents than the one reporting the error. For diagnosis, collect and examine MCA registers from other banks, cores, and processors in the system.	NbIntProtEn	L ³	D
NB Array Error	A parity error was detected in the NB internal arrays.	NbArrayParEn	-	D
L2 complex Data Error	NB received a data error from a core and this error could not be contained. For the cause of the data error, examine the core MCA registers for deferred errors. This error may occur for the following types of data writes: <ul style="list-style-type: none">• APIC• Configuration space (IO and MMIO) For these errors, sync flood will occur if D18F3x180[SyncFloodOnCpuLeakErr] is set.	McaCpuDatEr rEn	-	D

1. CTL: See [MSR0000_0410](#).
 2. ETG: error threshold group. See [2.14.1.7 \[Error Thresholding\]](#).
 • L=Link.
 • D=DRAM.
 3. The error thresholding group is Link if link protocol error; none for non-link protocol error.
 4. EAC: D=Error action taken if detected. E=Error action taken if MCA bank enabled.

The NB is capable of reporting the following errors:

Table 205: MC4 Error Signatures, Part 1

Error Type	ErrorCode-Ext	Error Code						
		Type	PP	T	RRRR	II/TT	LL	
Reserved	00h	-	-	-	-	-	-	
Reserved	01h	-	-	-	-	-	-	
Sync Error	02h	BUS	OBS	0	GEN	GEN	LG	
Mst Abort	03h	BUS	SRC/OBS	0	RD/WR	MEM/IO ¹	LG	
Tgt Abort	04h	BUS	SRC/OBS	0	RD/WR	MEM/IO ¹	LG	
RMW Error	06h	BUS	OBS	0	GEN	IO	LG	
WDT Error	07h	BUS	GEN	1	GEN	GEN	LG	

Table 205: MC4 Error Signatures, Part 1

Error Type	ErrorCode-Ext	Error Code					
		Type	PP	T	RRRR	II/TT	LL
ECC Error	08h	BUS	SRC/RES	0	RD/WR	MEM	LG
Link Data Error	0Ah	BUS	SRC/OBS	0	RD/WR/DWR	MEM/IO	LG
NB Protocol Error	0Bh		OBS	0	GEN	GEN	LG
NB Array Error	0Ch		OBS	0	GEN	GEN	LG
L2 complex Data Error	19h	MEM	-	-	WR	Data	LG

1. Indicates the type of link attached to the reporting NB, not the instruction type. MEM indicates coherent link, IO indicates IO link.

Table 206: MC4 Error Signatures, Part 2

Error Type	UC	AddrV	PCC	Syndrome Valid	CECC	UECC	Deferred	Scrub	Link	Err CoreId
Sync Error	1	0	1	-	0	0	0	0	Y	-
Mst Abort	1	1	Core ¹⁰	-	0	0	0	0	Y	Y
Tgt Abort	1	1	Core ¹⁰	-	0	0	0	0	Y	Y
RMW Error	1	1	0	-	0	0	0	0	Y	-
WDT Error	1	0 ¹	1	-	0	0	0	0	-	-
ECC Error	MS ⁶	1	MS ⁶ & Core	15:0	~MS ⁶	MS ⁶	0	1/0	-	-
Link Data Error	~Deferred ¹¹	1	0	-	0	0	0/1	0	Y	-
NB Protocol Error	1	1/0 ²	1	-	0	0	0	0	Y	-
NB Array Error	~Deferred ¹¹	1 ⁴	~Deferred ¹¹	-	0	0	0/1	0	-	-
L2 complex Data Error	1	0	1	-	0	0	0	0	-	Y

1. See [Table 212 \[Format of MSR0000_0412\[ErrAddr\[47:1\]\] for Watchdog Timer Errors\]](#).
2. See [Table 208 \[Format of MSR0000_0412\[ErrAddr\[47:1\]\] for Protocol Errors\]](#).
3. See [Table 211 \[Valid Values for ArrayErrorType\]](#).
4. MS: multi-symbol. 1=Multi-symbol. 0=Not multi-symbol.
5. Core: source is core. 1=Source is core. 0=Source is not core.
6. Deferred: error is deferred. 1=Error is deferred. 0=Error is not deferred.

MSR0000_0412 MC4 Machine Check Address (MC4_ADDR)

IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSE Read-write; Per-node; not-same-for-all. ENDIF. Cold reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). MSR0000_0412[31:0] is an alias of D18F3x50. MSR0000_0412[63:32] is an alias of D18F3x54.

Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#). ErrAddr[47:1] carries supplemental information associated with a machine check error, generally the address being accessed. Accessibility of this register by non-NBC cores is affected by [D18F3x44\[NbMcaToMstCpuEn\]](#). The format of ErrAddr[47:1] is a function of [MSR0000_0411\[ErrorCodeExt\]](#); See ErrAddr[47:1].

Bits	Description
63:48	Reserved. Value: 00h.
47:32	ErrAddr[47:32]: Error Address Bits[47:32] . See: ErrAddr[31:1].
31:1	ErrAddr[31:1]: Error Address Bits[31:1] . ErrAddr[47:0] = { MSR0000_0412[ErrAddr[47:32]] , MSR0000_0412[ErrAddr[31:1]] , MSR0000_0412[ErrAddr[0]] }. See the tables below for the encoding.
0	ErrAddr[0]: Error Address Bit[0] .

The register format depends on the type of error being logged:

- Protocol errors contain the error reason code, may contain the physical address, and are formatted according to [Table 208](#).
- NB array errors indicate the array in error, and are formatted according to [Table 210](#).
- NB Watchdog timer errors depend on the mode selected by [D18F3x180\[McaLogErrAddrWdtErr\]](#), and the format is indicated by D18F3x4C[AddrV]. If D18F3x4C[AddrV] is indicated, errors are formatted according to [Table 207](#). If D18F3x4C[AddrV] is not indicated, errors are formatted according to [Table 212](#).
- All other NB errors which indicate D18F3x4C[AddrV] are formatted according to [Table 207](#).

Table 207: Format of [MSR0000_0412\[ErrAddr\[47:1\]\]](#) for All Other Errors

Bits	Description
47:1	PhysAddr[47:1] .

Table 208: Format of [MSR0000_0412\[ErrAddr\[47:1\]\]](#) for Protocol Errors

Bits	Description
47:6	PhysAddr[47:6] . Valid of (MSR0000_0411[AddrV]==1); otherwise reserved.
5:1	ProtocolErrorType . See Table 209 [Valid Values for ProtocolErrorType] .

Table 209: Valid Values for ProtocolErrorType

Bits	Description
00h	Link: SRQ Read Response without matching request
01h	Link: Probe Response without matching request
02h	Link: TgtDone without matching request
03h	Link: TgtStart without matching request
04h	Link: Command buffer overflow
05h	Link: Data buffer overflow
06h	Link: Link retry packet count acknowledge overflow
07h	Link: Data command in the middle of a data transfer
08h	Link: Link address extension command followed by a packet other than a command with address. However, in coherent links it may be followed by a response packet.

Table 209: Valid Values for ProtocolErrorType

Bits	Description
09h	Link: A specific coherent-only packet from a CPU(cache block command) was issued to an IO link.
0Ah	Link: A command with invalid encoding was received. This error occurs when: 1. Any invalid command is received (including a command with no valid encoding or a coherent link command over an IO link or vice versa) while not in retry mode. 2. Any illegal command is received in which the CRC is correct while in retry mode (including any upstream broadcast command (link command encoding = 11101xb)).
0Bh	Link: Link CTL deassertion occurred when a data phase was not pending. This error condition may only occur when error-retry mode is not enabled (if it is enabled, this condition triggers a retry).
1Fh-10h	Reserved

Table 210: Format of [MSR0000_0412\[ErrAddr\[47:1\]\]](#) for NB Array Errors

Bits	Description
47:6	Reserved.
5:1	ArrayErrorType . See Table 211 [Valid Values for ArrayErrorType] .

Table 211: [Valid Values for ArrayErrorType](#)

Bits	Description
00h	SRA: System request address.
01h	SRD: System request data.
02h	SPB: System packet buffer.
03h	MCD: Memory controller data.
04h	MPB: Memory packet buffer.
05h	LPB0: Link 0 packet buffer.
08h-06h	Reserved.
09h	MPBC: Memory controller command packet buffer.
0Ah	MCDBM: Memory controller byte mask.
0Bh	MCACAM: Memory controller address array.
0Ch	DMAP: Extended DRAM address map.
0Dh	MMAP: Extended MMIO address map.
0Eh	X86MAP: Extended PCI/IO address map.
0Fh	CFGMAP: Extended config address map.
17h-10h	Reserved.
18h	SRIMCTRTE: SRI/MCT extended routing table.
1Ch-19h	Reserved
1Dh	TCB: TCB array.
1Fh-1Eh	Reserved

Table 212: Format of [MSR0000_0412\[ErrAddr\[47:1\]\]](#) for Watchdog Timer Errors

Bits	Description
47:40	CoreId. Indicates the core ID if the SourcePointer specifies Core. <u>Bits</u> <u>Description</u> 07h-00h Logical CoreId FFh-08h Reserved
39:36	SystemResponseCount. This field records unspecified, implementation-specific information.
35:31	WaitCode. records unspecified, implementation-specific information (all zeroes means no waiting condition).
30	WaitForPostedWrite.
29:27	DestinationNode. Records the Node ID of the node addressed by the transaction.
26:25	DestinationUnit. <u>Bits</u> <u>Description</u> 00b Core 01b Extended Core 10b Memory Controller 11b Host
24:22	SourceNode. Records the Node ID of the node originating the transaction.
21:20	SourceUnit. (same encoding as Destination Unit)
19:15	SourcePointer. Identifies crossbar source: <u>Bits</u> <u>Description</u> 00h SRI HostBridge 03h-01h Reserved 04h Core/L3 victim. See CoreId. See OpType. 07h-05h Reserved 08h Memory controller. 0Fh-09h Reserved 1Fh-10h Link. Link HH; sublink N (where N=0b for ganged links). All unused codes are reserved.
14:11	SrqEntryState. Records unspecified, implementation-specific information (all zeroes means idle).
10:7	OpType. Records unspecified, implementation-specific information.
6:1	LinkCommand. When the NB WDT expires, the link command of the transaction that timed out is captured here. This field is encoded identically to the “Code” field for link transactions defined in the link specification.

MSR0000_0413 NB Machine Check Misc 4 (DRAM Thresholding) 0 (MC4_MISC0)

[MSR0000_0413](#) is the first of the NB machine check miscellaneous registers. [MSR0000_0413](#) is associated with the DRAM error type. To see the remaining NB machine check miscellaneous registers, refer to [MSR0000_0408](#). Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#).

Bits	Description
------	-------------

63	Valid. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Reset: 1. ENDIF. 1=The CntP field is present.										
62	CntP: counter present. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Reset: 1. ENDIF. 1=A valid threshold counter is present.										
61	Locked. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Reset: 0. ENDIF. BIOS: IF (IntType==10b) THEN 1. ELSE 0. ENDIF. 1=Writes to bits [55:32] of this register are ignored. Set by BIOS to indicate that this register is not available for OS use. When MSRC001_0015[McStatusWrEn] is set, MSR writes to this register update all bits, regardless of the state of the Locked bit.										
60:56	Reserved.										
55:52	LvtOffset: LVT offset. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~MSR0000_0413[Locked]) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Reset: 0h. ENDIF. Specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see APIC[530:500]). <table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">3h-0h</td> <td>See APIC[530:500].</td> </tr> <tr> <td style="text-align: center;">Fh-4h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	3h-0h	See APIC[530:500].	Fh-4h	Reserved				
<u>Bits</u>	<u>Description</u>										
3h-0h	See APIC[530:500].										
Fh-4h	Reserved										
51	CntEn: counter enable. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Reset: 0. ENDIF. 1=Count thresholding errors. See 2.14.1.7 [Error Thresholding].										
50:49	IntType: interrupt type. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~MSR0000_0413[Locked]) THEN Read-write; Per-node ; not-same-for-all. ELSE Read-only; Per-node ; not-same-for-all. Cold reset: 0. ENDIF. Specifies the type of interrupt signaled when Ovrlfw is set. <table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Description</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">00b</td> <td>No Interrupt.</td> </tr> <tr> <td style="text-align: center;">01b</td> <td>APIC. APIC based interrupt (see LvtOffset above) to all cores.</td> </tr> <tr> <td style="text-align: center;">10b</td> <td>SMI. SMI trigger event (always routed to CpuCoreNum 0, as defined in 2.4.4 [Processor Cores and Downcoring]); see 2.4.10.2.3 [SMI Sources And Delivery].</td> </tr> <tr> <td style="text-align: center;">11b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	00b	No Interrupt.	01b	APIC. APIC based interrupt (see LvtOffset above) to all cores.	10b	SMI. SMI trigger event (always routed to CpuCoreNum 0, as defined in 2.4.4 [Processor Cores and Downcoring]); see 2.4.10.2.3 [SMI Sources And Delivery].	11b	Reserved
<u>Bits</u>	<u>Description</u>										
00b	No Interrupt.										
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11b	Reserved										
48	Ovrlfw: overflow. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node ; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node ; not-same-for-all; set-by-hardware. ELSE Read-only; Per-node ; not-same-for-all; set-by-hardware. Cold reset: 0. ENDIF. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this bit is set, the interrupt selected by the IntType field is generated.										
47:44	Reserved.										

43:32	ErrCnt: error counter. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node; not-same-for-all; updated-by-hardware. ELSE Read-only; Per-node; not-same-for-all; updated-by-hardware. Cold reset: 0. ENDIF. Written by software to set the starting value of the error counter. Incremented by hardware when errors are logged. Saturates at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)).
31:24	BlkPtr: Block pointer for additional MISC registers. Read-only. Value: 01h. 01h=Extended MC4_MISC MSR block is valid. See MSRC000_0408 .
23:0	Reserved.

MSR0000_0414 MC5 Machine Check Control (MC5_CTL)

Read-write. Reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0049 \[FR Machine Check Control Mask \(MC5_CTL_MASK\)\]](#).

Bits	Description
63:1	Unused.
0	WDT: core watchdog timer. See MSRC001_0074 [CPU Watchdog Timer (CpuWdtCfg)] .

MSR0000_0415 MC5 Machine Check Status (MC5_STATUS)

Cold reset: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSRC001_0015\[McStatusWrEn\]](#). Table 213 describes each error type. Table 214 describes the error codes and status register settings for each error type.

Bits	Description
63	Val: error valid. See: MSR0000_0401[Val] .
62	Overflow: error overflow. See: MSR0000_0401[Overflow] .
61	UC: error uncorrected. See: MSR0000_0401[UC] .
60	En: error enable. See: MSR0000_0401[En] .
59	MiscV: miscellaneous error register valid. Read-write; Updated-by-hardware. See: MSR0000_0401[MiscV] . 1= MSR0000_0417 is valid.
58	AddrV: error address valid. See: MSR0000_0401[AddrV] . 1=Valid address in MSR0000_0416 .
57	PCC: processor context corrupt. See: MSR0000_0401[PCC] .
56:16	Reserved.
15:0	ErrorCode: error code. Read-write; Updated-by-hardware. See 2.14.1.5 [Error Code] See Table 214 .

Table 213: MC5 Error Descriptions

Error Type	Error Sub-type	Description	CTL ¹	EAC ³
WDT error	-	The WDT timer has expired. See MSRC001_0074 [CPU Watchdog Timer (CpuWdtCfg)] .	WDT	E

1. CTL: See [MSR0000_0414](#).
 2. CID: core ID. All EX errors are reported to the affected core; see [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).
 3. EAC: D=Error action taken if detected. E=Error action taken if MCA bank enabled. See [2.14.1.3 \[Error Detection, Action, Logging, and Reporting\]](#).

Table 214: MC5 Error Signatures

Error Type	Error Sub-Type	ErrorCodeExt	Error Code							UC	ADDRV	MISCV	PCC	CECC	UECC
			Type	UU/P P	TT	RRRR	II/TT	LL							
WDT error	-	00h	BUS	GEN	1	GEN	GEN	LG	1	1	1	1	1	0	0
1. Causes shutdown. See 2.14.1.3.1 [MCA conditions that cause Shutdown] . PRNF errors will hang the core. 2. Causes shutdown if UC=1. See 2.14.1.3.1 [MCA conditions that cause Shutdown] . 3. STATQ sets PCC=1 if a store retired in last 3 cycles or FpTokenRet bits mismatch.															

MSR0000_0416 MC5 Machine Check Address (MC5_ADDR)

Read-write; Updated-by-hardware. Cold reset: 0000_0000_0000_0000h. The MCi_ADDR register contains valid data if indicated by MCi_STATUS[AddrV]. See [2.14.1 \[Machine Check Architecture\]](#). The register format depends on the type of error being logged.

Bits	Description
63:0	ADDR . See Table 215 .

The following tables define the address register as a function of error type.

Table 215: MC5 Address Register

Error Type	Error Sub-Type	Bits	Description
WDT	- (ErrorCodeExt=00h)	63:48	Reserved
		48:0	LogAddr[48:0] . Logical canonical address of the next instruction after the last instruction retired.

MSR0000_0417 MC5 Machine Check Miscellaneous (MC5_MISC)

Cold reset: 0000_0000_0000_0000h.

Bits	Description																		
63:8	Reserved.																		
7:0	FrCompl . Read-write. When the WDT expires, these bits are loaded with the state of the valid and completion bits. <table><thead><tr><th>Bit</th><th>Definition</th></tr></thead><tbody><tr><td>[7]</td><td>FpComplete1: The COP at ROB next-to-bottom has FP completion.</td></tr><tr><td>[6]</td><td>LsComplete1: The COP at ROB next-to-bottom has LS completion.</td></tr><tr><td>[5]</td><td>ExComplete1: The COP at ROB next-to-bottom has EX completion.</td></tr><tr><td>[4]</td><td>RobOpValid1: The COP at ROB next-to-bottom is valid.</td></tr><tr><td>[3]</td><td>FpComplete0: The COP at ROB bottom has FP completion.</td></tr><tr><td>[2]</td><td>LsComplete0: The COP at ROB bottom has LS completion.</td></tr><tr><td>[1]</td><td>ExComplete0: The COP at ROB bottom has EX completion.</td></tr><tr><td>[0]</td><td>RobOpValid0: The COP at ROB bottom is valid.</td></tr></tbody></table>	Bit	Definition	[7]	FpComplete1: The COP at ROB next-to-bottom has FP completion.	[6]	LsComplete1: The COP at ROB next-to-bottom has LS completion.	[5]	ExComplete1: The COP at ROB next-to-bottom has EX completion.	[4]	RobOpValid1: The COP at ROB next-to-bottom is valid.	[3]	FpComplete0: The COP at ROB bottom has FP completion.	[2]	LsComplete0: The COP at ROB bottom has LS completion.	[1]	ExComplete0: The COP at ROB bottom has EX completion.	[0]	RobOpValid0: The COP at ROB bottom is valid.
Bit	Definition																		
[7]	FpComplete1: The COP at ROB next-to-bottom has FP completion.																		
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[1]	ExComplete0: The COP at ROB bottom has EX completion.																		
[0]	RobOpValid0: The COP at ROB bottom is valid.																		

3.20 MSRs - MSRC000_0xxx

MSRC000_0080 Extended Feature Enable (EFER)

SKINIT Execution: 0000_0000_0000_0000h.

Bits	Description
63:16	MBZ.
15	MBZ.
14	FFXSE: fast FXSAVE/FRSTOR enable. Read-write. Reset: 0. 1=Enables the fast FXSAVE/FRSTOR mechanism. A 64-bit operating system may enable the fast FXSAVE/FRSTOR mechanism if (CPUID Fn8000_0001_EDX[FFXSR]==1). This bit is set once by the operating system and its value is not changed afterwards.
13	LMSLE: long mode segment limit enable. Read-write. Reset: 0. 1=Enables the long mode segment limit check mechanism.
12	SVME: secure virtual machine (SVM) enable. IF (MSRC001_0114[SvmeDisable]==1) THEN MBZ. ELSE Read-write. ENDIF. Reset: 0. 1=SVM features are enabled.
11	NXE: no-execute page enable. Read-write. Reset: 0. 1=The no-execute page protection feature is enabled.
10	LMA: long mode active. Read-only. Reset: 0. 1=Indicates that long mode is active.
9	MBZ.
8	LME: long mode enable. Read-write. Reset: 0. 1=Long mode is enabled.
7:1	RAZ.
0	SYSCALL: system call extension enable. Read-write. Reset: 0. 1=SYSCALL and SYSRET instructions are enabled. This adds the SYSCALL and SYSRET instructions which can be used in flat addressed operating systems as low latency system calls and returns.

MSRC000_0081 SYSCALL Target Address (STAR)

Reset: 0000_0000_0000_0000h. This register holds the target address used by the SYSCALL instruction and the code and stack segment selector bases used by the SYSCALL and SYSRET instructions.

Bits	Description
63:48	SysRetSel: SYSRET CS and SS. Read-write.
47:32	SysCallSel: SYSCALL CS and SS. Read-write.
31:0	Target: SYSCALL target address. Read-write.

MSRC000_0082 Long Mode SYSCALL Target Address (STAR64)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	LSTAR: long mode target address. Read-write. Target address for 64-bit mode calling programs. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0083 Compatibility Mode SYSCALL Target Address (STARCOMPAT)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	CSTAR: compatibility mode target address. Read-write. Target address for compatibility mode. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0084 SYSCALL Flag Mask (SYSCALL_FLAG_MASK)

Bits	Description
63:32	RAZ.
31:0	Mask: SYSCALL flag mask. Read-write. Reset: 0000_0000h. This register holds the EFLAGS mask used by the SYSCALL instruction. 1=Clear the corresponding EFLAGS bit when executing the SYSCALL instruction.

MSRC000_0100 FS Base (FS_BASE)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	FSBase: expanded FS segment base. Read-write; not-same-for-all. This register provides access to the expanded 64-bit FS segment base. The address stored in this register must be in canonical form (if not canonical, a #GP fault fill occurs).

MSRC000_0101 GS Base (GS_BASE)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	GSSBase: expanded GS segment base. Read-write; not-same-for-all. This register provides access to the expanded 64-bit GS segment base. The address stored in this register must be in canonical form (if not canonical, a #GP fault fill occurs).

MSRC000_0102 Kernel GS Base (KernelGSbase)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	KernelGSBase: kernel data structure pointer. Read-write. This register holds the kernel data structure pointer which can be swapped with the GS_BASE register using the SwapGS instruction. The address stored in this register must be in canonical form (if not canonical, a #GP fault occurs).

MSRC000_0103 Auxiliary Time Stamp Counter (TSC_AUX)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:32	Reserved.
31:0	TscAux: auxiliary time stamp counter data. Read-write. It is expected that this is initialized by privileged software to a meaningful value, such as a processor ID. This value is returned in the RDTSCP instruction.

MSRC000_0104 Time Stamp Counter Ratio (TscRateMsr)

[MSRC000_0104](#) [Time Stamp Counter Ratio (TscRateMsr)] allows the hypervisor to control the guest's view of the Time Stamp Counter. It provides a multiplier that scales the value returned when [MSR0000_0010](#)[TSC] and [MSR0000_00E7](#)[MPERF] are read by a guest running under virtualization. This allows the hypervisor to provide a consistent TSC and MPERF rate for a guest process when moving that process between cores that have a differing P0 rate. The TSC Ratio MSR does not affect the value read from the TSC and MPERF MSRs when read when in host mode or when virtualization is not being used or when accessed by code executed in system management mode (SMM) unless the SMM code is executed within a guest container. The TSC Ratio value does not affect the rate of the underlying TSC and MPERF counters, or the value that gets written to the TSC and MPERF MSRs counters on a write by either the host or the guest. The TSC Ratio MSR contains a fixed-point number in 8.32 format, which is 8 bits of integer and 32 bits of fraction. This number is the ratio of the desired P0 frequency to the P0 frequency of the core. The reset value of the TSC Ratio MSR is 1.0, which results in a guest frequency matches the core P0 frequency.

Bits	Description
63:40	MBZ.
39:32	TscRateMsrInt: time stamp counter rate integer. Read-write. Reset: 01h. Specifies the integer part of the MSR TSC ratio value.
31:0	TscRateMsrFrac: time stamp counter rate fraction. Read-write. Reset: 0000_0000h. Specifies the fractional part of the MSR TSC ratio value.

MSRC000_0408 NB Machine Check Misc 4 (Link Thresholding) 1 (MC4_MISC1)

Per-node. [MSRC000_0408](#) is associated with the link error type. See [2.14.1.7](#) [Error Thresholding]. Accessibility of this register by non-NBC cores is affected by [D18F3x44](#)[NbMcaToMstCpuEn].

[MSRC000_0408](#)[63:32] is an alias of [D18F3x168](#).

Bits	Description
63	Valid. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Reset: 1. ENDIF. 1=The CntP field is present.
62	CntP: counter present. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Reset: 1. ENDIF. 1=A valid threshold counter is present.
61	Locked. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn]) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Reset: 0. ENDIF. BIOS: IF (IntType==10b) THEN 1. ELSE 0. ENDIF. 1=Writes to bits [55:32] of this register are ignored. Set by BIOS to indicate that this register is not available for OS use. When MSRC001_0015[McStatusWrEn] is set, MSR writes to this register update all bits, regardless of the state of the Locked bit.

60:56	Reserved.										
55:52	<p>LvtOffset: LVT offset. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~MSRC000_0408[Locked]) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Reset: 0h. ENDIF. Specifies the address of the LVT entry in the APIC registers as follows: LVT address = (LvtOffset shifted left 4 bits) + 500h (see APIC[530:500]).</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3h-0h</td> <td>See APIC[530:500].</td> </tr> <tr> <td>Fh-4h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	3h-0h	See APIC[530:500].	Fh-4h	Reserved				
Bits	Description										
3h-0h	See APIC[530:500].										
Fh-4h	Reserved										
51	<p>CntEn: counter enable. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Reset: 0. ENDIF. 1=Count thresholding errors. See 2.14.1.7 [Error Thresholding].</p>										
50:49	<p>IntType: interrupt type. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~MSRC000_0408[Locked]) THEN Read-write; Per-node; not-same-for-all. ELSE Read-only; Per-node; not-same-for-all. Cold reset: 0. ENDIF. Specifies the type of interrupt signaled when Ovrlfw is set.</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No Interrupt.</td> </tr> <tr> <td>01b</td> <td>APIC. APIC based interrupt (see LvtOffset above) to all cores.</td> </tr> <tr> <td>10b</td> <td>SMI. SMI trigger event (always routed to CpuCoreNum 0, as defined in 2.4.4 [Processor Cores and Downcore]); see 2.4.8.2.3 [SMI Sources And Delivery].</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	No Interrupt.	01b	APIC. APIC based interrupt (see LvtOffset above) to all cores.	10b	SMI. SMI trigger event (always routed to CpuCoreNum 0, as defined in 2.4.4 [Processor Cores and Downcore]); see 2.4.8.2.3 [SMI Sources And Delivery].	11b	Reserved
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11b	Reserved										
48	<p>Ovrlfw: overflow. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node; not-same-for-all; set-by-hardware. ELSE Read-only; Per-node; not-same-for-all; set-by-hardware. Cold reset: 0. ENDIF. Set by hardware when ErrCnt transitions from FFEh to FFFh. When this bit is set, the interrupt selected by the IntType field is generated.</p>										
47:44	Reserved.										
43:32	<p>ErrCnt: error counter. IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ; Per-node; not-same-for-all. ELSIF (MSRC001_0015[McStatusWrEn] ~Locked) THEN Read-write; Per-node; not-same-for-all; updated-by-hardware. ELSE Read-only; Per-node; not-same-for-all; updated-by-hardware. Cold reset: 0. ENDIF. Written by software to set the starting value of the error counter. Incremented by hardware when errors are logged. Saturates at FFFh (no rollover). The threshold value, written by software, is (FFFh - the desired error count (the number of errors necessary in order for an interrupt to be taken)).</p>										
31:0	Reserved. Read-only. Reset: 0100_0000h.										

MSRC000_0409 Reserved

Bits	Description
63:0	RAZ.

MSRC000_040[F:A] Reserved

Bits	Description
63:0	RAZ.

3.21 MSRs - MSRC001_0xx

MSRC001_00[03:00] Performance Event Select (PERF_CTL[3:0])

Reset: 0000_0000_0000_0000h. See 2.6.1 [Performance Monitor Counters].

Table 216: Register Mapping for MSRC001_00[03:00]

Register	Function
MSRC001_0000	Counter 0
MSRC001_0001	Counter 1
MSRC001_0002	Counter 2
MSRC001_0003	Counter 3

Bits	Description								
63:42	Reserved.								
41	HostOnly: host only counter. Read-write. 1=Events are only counted when the processor is in host mode.								
40	GuestOnly: guest only counter. Read-write. 1=Events are only counted when the processor is in guest mode.								
39:36	Reserved.								
35:32	EventSelect[11:8]: performance event select. Read-write. See: EventSelect[7:0].								
31:24	CntMask: counter mask. Read-write. Controls the number of events counted per clock cycle. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>The corresponding PERF_CTR[3:0] register is incremented by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 3.</td> </tr> <tr> <td>03h-01h</td> <td>When Inv = 0, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv = 1, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is less than CntMask value.</td> </tr> <tr> <td>FFh-04h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	00h	The corresponding PERF_CTR[3:0] register is incremented by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 3.	03h-01h	When Inv = 0, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv = 1, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is less than CntMask value.	FFh-04h	Reserved.
Bits	Definition								
00h	The corresponding PERF_CTR[3:0] register is incremented by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 3.								
03h-01h	When Inv = 0, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is greater than or equal to the CntMask value. When Inv = 1, the corresponding PERF_CTR[3:0] register is incremented by 1 if the number of events occurring in a clock cycle is less than CntMask value.								
FFh-04h	Reserved.								
23	Inv: invert counter mask. Read-write. See CntMask.								
22	En: enable performance counter. Read-write. 1= Performance event counter is enabled.								
21	Reserved.								
20	Int: enable APIC interrupt. Read-write. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt when the performance counter overflows.								
18	Edge: edge detect. Read-write. 0=Level detect. 1=Edge detect. The edge count mode increments the counter when a transition happens on the monitored event. If the event selected is changed without disabling the counter, an extra edge is falsely detected when the first event is a static 0 and the second event is a static one. To avoid this false edge detection, disable the counter when changing the event and then enable the counter with a second MSR write.								
17	OS: OS mode. Read-write. 1=Events are only counted when CPL=0.								
16	User: user mode. Read-write. 1=Events only counted when CPL>0.								

15:8	UnitMask: event qualification. Read-write. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is not applicable and may be set to zeros.																		
7:0	<p>EventSelect[7:0]: event select. Read-write. This field, along with EventSelect[11:8] above, combine to form the 12-bit event select field, EventSelect[11:0]. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CNT[3:0] register. The events are specified in section 3.23 [Core Performance Counter Events]. Some events are reserved; when a reserved event is selected, the results are undefined.</p> <p>EventSelect[7:5] are used internally to encode the TLM that controls the performance counter.</p> <table style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; width: 15%;">Bits</th> <th style="text-align: left;">Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>FP</td> </tr> <tr> <td>001b</td> <td>LS</td> </tr> <tr> <td>010b</td> <td>DC</td> </tr> <tr> <td>011b</td> <td>BU</td> </tr> <tr> <td>100b</td> <td>IC</td> </tr> <tr> <td>101b</td> <td>ME</td> </tr> <tr> <td>110b</td> <td>FR</td> </tr> <tr> <td>111b</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	000b	FP	001b	LS	010b	DC	011b	BU	100b	IC	101b	ME	110b	FR	111b	Reserved.
Bits	Definition																		
000b	FP																		
001b	LS																		
010b	DC																		
011b	BU																		
100b	IC																		
101b	ME																		
110b	FR																		
111b	Reserved.																		

MSRC001_00[07:04] Performance Event Counter (PERF_CTR[3:0])

The core provides four 48-bit performance counters. Each counter can monitor a different event specified by [MSRC001_00\[03:00\] \[Performance Event Select \(PERF_CTL\[3:0\]\)\]](#). The accuracy of the counters is not ensured.

Performance counters are used to count specific processor events, such as data-cache misses, or the duration of events, such as the number of clocks it takes to return data from memory after a cache miss. During event counting, the processor increments the counter when it detects an occurrence of the event. During duration measurement, the processor counts the number of processor clocks it takes to complete an event. Each performance counter can be used to count one event, or measure the duration of one event at a time.

In addition to the RDMSR instruction, the PERF_CNT[3:0] registers can be read using a special read performance-monitoring counter instruction, RDPMC. The RDPMC instruction loads the contents of the PERF_CTR[3:0] register specified by the ECX register, into the EDX register and the EAX register.

Writing the performance counters can be useful if there is an intention for software to count a specific number of events, and then trigger an interrupt when that count is reached. An interrupt can be triggered when a performance counter overflows. Software should use the WRMSR instruction to load the count as a two's-complement negative number into the performance counter. This causes the counter to overflow after counting the appropriate number of times.

The performance counters are not assured of producing identical measurements each time they are used to measure a particular instruction sequence, and they should not be used to take measurements of very small instruction sequences. The RDPMC instruction is not serializing, and it can be executed out-of-order with respect to other instructions around it. Even when bound by serializing instructions, the system environment at

the time the instruction is executed can cause events to be counted before the counter value is loaded into EDX:EAX.

Table 217: Register Mapping for MSRC001_00[07:04]

Register	Function
MSRC001_0004	Counter 0
MSRC001_0005	Counter 1
MSRC001_0006	Counter 2
MSRC001_0007	Counter 3

Bits	Description
63:48	RAZ.
47:0	CTR: performance counter value. Read-write. Reset: 0. Returns the current value of the event counter.

MSRC001_0010 System Configuration (SYS_CFG)

Bits	Description
63:23	Reserved.
22	Tom2ForceMemTypeWB: top of memory 2 memory type write back. Read-write. Reset: 0. 1=The default memory type of memory between 4GB and TOM2 is write back instead of the memory type defined by MSR0000_02FF[MemType] . For this bit to have any effect, MSR0000_02FF[MtrrDefTypeEn] must be 1. MTRRs and PAT can be used to override this memory type.
21	MtrrTom2En: MTRR top of memory 2 enable. Read-write. Reset: 0. 0= MSRC001_001D [Top Of Memory 2 (TOM2)] is disabled. 1=This register is enabled. See D0F0x64_x19[TomEn] .
20	MtrrVarDramEn: MTRR variable DRAM enable. Read-write. Reset: 0. BIOS: 1. 0= MSRC001_001A [Top Of Memory (TOP_MEM)] and IORRs are disabled. 1=These registers are enabled.
19	MtrrFixDramModEn: MTRR fixed RdDram and WrDram modification enable. Read-write. Reset: 0. Controls access to MSR0000_02[6F:68,59:58,50][RdDram, WrDram] . 0=Access type is MBZ; writing 00b does not change the hidden value of MSR0000_02[6F:68,59:58,50][RdDram, WrDram] . 1=Access type is Read-write. BIOS: This bit should be set to 1 during BIOS initialization of the fixed MTRRs, then cleared to 0 for operation.
18	MtrrFixDramEn: MTRR fixed RdDram and WrDram attributes enable. Read-write. Reset: 0. BIOS: 1. 1=Enables the RdDram and WrDram attributes in MSR0000_02[6F:68,59:58,50] .
17	SysUcLockEn: system lock command enable. Read-write. Reset: 1. 0=Coherent fabric does not support bus lock transactions. This bit must be set on multi-core processors. There is no need to set this on single core processors. When this bit is clear, bus locks are never used by the processor core. When this bit is set, cache locks are still used by the processor core as much as possible, but bus locks are sent in necessary cases.
16	Reserved.
15:0	Reserved.

MSRC001_0015 Hardware Configuration (HWCR)

Bits	Description
63:32	Reserved.
31:30	Reserved. Read-write.
29	Reserved. Read-write.
28	Reserved. Read-write.
27	Reserved. Read-write.
26	EffFreqCntMwait: effective frequency counting during mwait. Read-write. Reset: 0. Specifies whether MSR0000_00E7 [Max Performance Frequency Clock Count (MPERF)] and MSR0000_00E8 [Actual Performance Frequency Clock Count (APERF)] increment while the core is in the monitor event pending state (when the mwait instruction has been executed). 0=The registers do not increment. 1=The registers increment. See 2.5.3.3 [Effective Frequency] .
25	CpbDis: core performance boost disable. Read-write. Reset: 0. Specifies whether core performance boost is requested to be enabled or disabled. 0=CPB is requested to be enabled. 1=CPB is disabled. See 2.5.9 [Application Power Management (APM)] . If this bit is set on any core, then CPB is disabled on all cores in the processor. If core performance boost is disabled while a core is in a boosted P-state, the core will automatically transition to the highest performance non-boosted P-state. A write to MSRC001_0015[CpbDis] is aliased to D18F4x114[CpbDis] . A read of MSRC001_0015[CpbDis] returns the last value written to MSRC001_0015[CpbDis] . When D18F4x114[CpbDis] is set on any core, the NB initiates a P-state limit on all cores. The P-state limit is set to the highest performance non-boosted P-state. See 2.5.5.1.6 [Modification of P-state Requests and Visibility] .
24	TscFreqSel: TSC frequency select. Read-only. Reset: 1. 1=The TSC increments at the P0 frequency. This field uses software P-state numbering. See 2.5.3.1.1.1 [Software P-state Numbering] .
23	ForceRdWrSzPrb: force probes for RdSized and WrSized. Read-write. MSRC001_0015[ForceRdWrSzPrb] is an alias of D18F3xEC[ForceRdWrSzPrb] . Reset: 0. A read returns a 1 if this field is set on any core of the node. 1=Forces probes on read-sized and write-sized transactions, except those that are display refresh.
22	Reserved. Read-write.
21	MisAlignSseDis: misaligned SSE mode disable. Read-write. Reset: 0. 1=Disables misaligned SSE mode. If this is set, then CPUID Fn8000_0001(ECX)[MisAlignSse] is 0.
20	IoCfgGpFault: IO-space configuration causes a GP fault. Read-write. Reset: 0. 1=IO-space accesses to configuration space cause a GP fault. The fault is triggered if any part of the IO read/write address range is between CF8h and CFFh, inclusive. These faults only result from single IO instructions, not to string and REP IO instructions. This fault takes priority over the IO trap mechanism described by MSRC001_0054 [IO Trap Control (SMI_ON_IO_TRAP_CTL_STS)] .
19	Reserved. Read-write.

18	McStatusWrEn: machine check status write enable. Read-write. Reset: 0. McStatusWrEn can be used to debug machine check exception and interrupt handlers. See 2.14.3 [Error Injection and Simulation] . See 2.14.1 [Machine Check Architecture] . <ul style="list-style-type: none"> • 1=Writes by software to MCi_STATUS (see 2.14.1 [Machine Check Architecture]) do not cause general protection faults; such writes update all implemented bits in these registers. • 0=MCi_STATUS registers are readable; writing a non-zero pattern to these registers causes a general protection fault. • The MCi_STATUS registers are: MSR0000_0401, MSR0000_0405, MSR0000_0409, MSR0000_040D, MSR0000_0411, MSR0000_0415. McStatusWrEn does not affect the writability of MSR0000_0001; MSR0000_0001 is always writable.
17	Wrap32Dis: 32-bit address wrap disable. Read-write. Reset: 0. 1=Disable 32-bit address wrapping. Software can use Wrap32Dis to access physical memory above 4 Gbytes without switching into 64-bit mode. To do so, software should write a greater-than 4 Gbyte address to MSRC000_0100 [FS Base (FS_BASE)] and MSRC000_0101 [GS Base (GS_BASE)] . Then it would address ± 2 Gbytes from one of those bases using normal memory reference instructions with a FS or GS override prefix. However, the INVLPG, FST, and SSE store instructions generate 32-bit addresses in legacy mode, regardless of the state of Wrap32Dis.
16:15	Reserved. Read-write.
14	RsmSpCycDis: RSM special bus cycle disable. IF MSRC001_0015 [SmmLock] THEN Read-only ELSE Read-write ENDIF. Reset: 0. 0=A link special bus cycle, SMIACK, is generated on a resume from SMI.
13	SmiSpCycDis: SMI special bus cycle disable. IF MSRC001_0015 [SmmLock] THEN Read-only ELSE Read-write ENDIF. Reset: 0. 0=A link special bus cycle, SMIACK, is generated when an SMI interrupt is taken.
12	Reserved. Read-write.
11	Reserved. Read-write. Previously defined as LimitCpuidStdMaxVal.
10	MonMwaitUserEn: MONITOR/MWAIT user mode enable. Read-write. Reset: 0. 1=The MONITOR and MWAIT instructions are supported in all privilege levels. 0=The MONITOR and MWAIT instructions are supported only in privilege level 0; these instructions in privilege levels 1 to 3 cause a #UD exception. The state of this bit is ignored if MonMwaitDis is set.
9	MonMwaitDis: MONITOR and MWAIT disable. Read-write. Reset: 0. 1=The MONITOR and MWAIT opcodes become invalid. This affects what is reported back through CPUID Fn0000_0001_ECX [Monitor].
8	IgnneEm: IGNNE port emulation enable. Read-write. Reset: 0. 1=Enable emulation of IGNNE port.
7:6	Reserved. Read-write.
4	INVDWBINVD: INVD to WBINVD conversion. Read-write. Reset: 0. 1=Convert INVD to WBINVD. BIOS: See 2.3.3 [Using L2 Cache as General Storage During Boot] . This bit is required to be set for normal operation when two or more cores of a L2 complex are enabled, and thus share the L2 cache.

3	TlbCacheDis: cacheable memory disable. Read-write. Reset: 0. 1=Disable performance improvement that assumes that the PML4, PDP, PDE and PTE entries are in cacheable WB DRAM. Operating systems that maintain page tables in any other memory type must set the TlbCacheDis bit to insure proper operation. <ul style="list-style-type: none"> • TlbCacheDis does not override the memory type specified by the SMM ASeg and TSeg memory regions. See 2.4.8.2.7 [The Protected ASeg and TSeg Areas]. • Non-SMM mode page table walks page fault using the reserved error code if directed to the ASeg or TSeg memory regions.
1	Reserved. Read-write.
0	SmmLock: SMM code lock. Read; write-1-only. Reset: 0. SBIOS: 1. 1=SMM code in the ASeg and TSeg range and the SMM registers are read-only and SMI interrupts are not intercepted in SVM. See 2.4.8.2.9 [Locking SMM] .

MSRC001_00[18,16] IO Range Base (IORR_BASE[1:0])

Reset: 0000_0000_0000_0000h. MSRC001_0016 and MSRC001_0017 combine to specify the first IORR range and MSRC001_0018 and MSRC001_0019 combine to specify the second IORR range. A core access, with address CPUAddr, is determined to be within IORR address range if the following equation is true:
 $CPUAddr[39:12] \& PhyMask[39:12] == PhyBase[39:12] \& PhyMask[39:12]$.

BIOS can use the IORRs to create an IO hole within a range of addresses that would normally be mapped to DRAM. It can also use the IORRs to re-assert a DRAM destination for a range of addresses that fall within a bigger IO hole that overlays DRAM. See [2.4.6.1.2 \[Determining The Access Destination for Core Accesses\]](#).

Bits	Description
63:40	RAZ.
39:12	PhyBase: physical base address. Read-write.
11:5	RAZ.
4	RdMem: read from memory. Read-write. 1=Read accesses to the range are directed to system memory. 0=Read accesses to the range are directed to IO.
3	WrMem: write to memory. Read-write. 1=Write accesses to the range are directed to system memory. 0=Write accesses to the range are directed to IO.
2:0	RAZ.

MSRC001_00[19,17] IO Range Mask (IORR_MASK[1:0])

Reset: 0000_0000_0000_0000h. See [MSRC001_00\[18,16\]](#).

Bits	Description
63:40	RAZ.
39:12	PhyMask: physical address mask. Read-write.
11	Valid. Read-write. 1=The pair of registers that specifies an IORR range is valid.
10:0	RAZ.

MSRC001_001A Top Of Memory (TOP_MEM)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:40	RAZ.
39:23	TOM[39:23]: top of memory. Read-write. Specifies the address that divides between MMIO and DRAM. This value is normally placed below 4G. From TOM to 4G is MMIO; below TOM is DRAM. See 2.4.6 [System Address Map] and 2.9.11 [DRAM CC6/PC6 Storage] .
22:0	RAZ.

MSRC001_001D Top Of Memory 2 (TOM2)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:40	RAZ.
39:23	TOM2[39:23]: second top of memory. Read-write. Specifies the address divides between MMIO and DRAM. This value is normally placed above 4G. From 4G to TOM2 - 1 is DRAM; TOM2 and above is MMIO. See 2.4.6 [System Address Map] and 2.9.11 [DRAM CC6/PC6 Storage] . This register is enabled by MSRC001_0010[MtrrTom2En] .
22:0	RAZ.

MSRC001_001F Northbridge Configuration 1 (NB_CFG1)

Read-write; Per-node. Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#). [MSRC001_001F\[31:0\]](#), [MSRC001_101F\[31:0\]](#) are an alias of [D18F3x88](#). [MSRC001_001F\[63:32\]](#), [MSRC001_101F\[63:32\]](#) are an alias of [D18F3x8C](#).

Bits	Description
62	DisStpClkAbortFlush. Reset: 0. BIOS: 1. 1=Disable aborting flush for core when the other core has a pending architectural interrupt.
55	EnaDiv1CpuLowPwr. Reset: 0. BIOS: 1. Enables power management actions in the core even when the requested clock divisor is /1. Normally a /1 clock divisor does not generate power management actions.
54	InitApicIdCpuIdLo. Reset: 0. BIOS: 1. 0=Reserved. 1=Selects the format for ApicId; see APIC20 .
51	DisDatFwdVic. Reset: 0. BIOS: 1. 1=Disables data forwarding from victims to reads.
50	DisOrderRdRsp. Reset: 0. 1=Disables ordered responses to IO link read requests.
46	EnableCf8ExtCfg: enable CF8 extended configuration cycles. Reset: 0. 1=Allows the IO configuration space access method, IOCF8 and IOCFC , to be used to generate extended configuration cycles by enabling IOCF8[27:24] .

45	DisUsSysMgtReqToNcHt: disable upstream system management request to link. Reset: 0. 1=Disables downstream reflection of upstream STPCLK and x86 legacy input system management commands (in order to work around potential deadlock scenarios related to reflection regions).
36	DisDatMsk: disable data mask. Reset: 0. BIOS: IF (DataMaskMbType!=1) THEN 1 ELSE 0 ENDIF. 1=Disables DRAM data masking function; all write requests that are less than one cacheline, a DRAM read is performed before writing the data. Data masking is supported in ECC mode; the NB performs a minimum write size of 16B. Note that when this feature is disabled, the DCT will drive the DM pins low during MCT writes to x8 DIMMs. See also TriDM.
31	DisCohLdtCfg: disable coherent link configuration accesses. Reset: 0. 1=Disables automatic routing of PCI configuration accesses to the processor configuration registers; PCI configuration space accesses which fall within the hard-coded range reserved for processor configuration-space registers are instead routed to the IO link specified by D18F1x[1DC:1D0,EC:E0] [Configuration Map]. This can be used to effectively hide the configuration registers from software. It can also be used to provide a means for an external chip to route processor configuration accesses according to a scheme other than the hard-coded version. When used, this bit needs to be set on all processors in a system. PCI configuration accesses should not be generated if this bit is not set on all processors.
27	DisDramScrub. Reset: 0. 1=Disable DRAM ECC scrubbing; this overrides the settings in D18F3x58 [Scrub Rate Control], D18F3x5C [DRAM Scrub Address Low].
18	DisCstateBoostBlockPstateUp. Read-write. Reset: 0. BIOS: D18F5x88 [EnCstateBoostBlockCC6Exit]. 1=Allow cores that are waking up out of a non-C0 C-state to transition to the last requested Pstate without having to wait for cores in the boosted P-state to transition out of the boosted P-state.

MSRC001_0022 Machine Check Exception Redirection

Reset: 0000_0000_0000_0000h. This register can be used to redirect machine check exceptions (MCEs) to SMIs or vectored interrupts. If both RedirSmiEn and RedirVecEn are set, then undefined behavior results.

Bits	Description
63:32	Reserved.
31:10	Reserved. Read-write.
9	RedirSmiEn. Read-write. 1=Redirect MCEs (that are directed to this core) to generate an SMI-trigger IO cycle via MSRC001_0056 . The status is stored in SMMFEC4 [MceRedirSts].
8	RedirVecEn. Read-write. 1=Redirect MCEs (that are directed to this core) to generate a vectored interrupt, using the interrupt vector specified in RedirVector.
7:0	RedirVector. Read-write. See RedirVecEn.

MSRC001_00[35:30] Processor Name String

Reset: 0000_0000_0000_0000h. BIOS: [Table 219](#). These registers holds the CPUID name string in ASCII. The state of these registers are returned by CPUID instructions, [CPUID Fn8000_000\[4:2\]_E\[D,C,B,A\]X](#). BIOS should set these registers to the product name for the processor as provided by AMD. Each register contains a block of 8 ASCII characters; the least byte corresponds to the first ASCII character of the block; the most-significant byte corresponds to the last character of the block. MSRC001_0030 contains the first block of

the name string; MSRC001_0035 contains the last block of the name string.

Table 218: Register Mapping for MSRC001_00[35:30]

Register	Function
MSRC001_0030	Characters 7-0
MSRC001_0031	Characters 15-8
MSRC001_0032	Characters 23-16
MSRC001_0033	Characters 31-24
MSRC001_0034	Characters 39-32
MSRC001_0035	Characters 47-40

See [D18F5x194](#) for the access method to [D18F5x198_x\[B:0\]](#).

Table 219: BIOS Recommendations for MSRC001_00[35:30]

Register	BIOS
MSRC001_0030	{D18F5x198_x1, D18F5x198_x0}
MSRC001_0031	{D18F5x198_x3, D18F5x198_x2}
MSRC001_0032	{D18F5x198_x5, D18F5x198_x4}
MSRC001_0033	{D18F5x198_x7, D18F5x198_x6}
MSRC001_0034	{D18F5x198_x9, D18F5x198_x8}
MSRC001_0035	{D18F5x198_xB, D18F5x198_xA}

Bits	Description
63:0	CpuNameString . Read-write.

MSRC001_003E Hardware Thermal Control (HTC)

Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#).
Uses hardware P-state numbering. See [2.5.3.1.1.2 \[Hardware P-state Numbering\]](#).

Bits	Description
63:32	Reserved.
31	Reserved.
30:28	HtcPstateLimit: HTC P-state limit select. MSRC001_003E[HtcPstateLimit] is an alias of D18F3x64[HtcPstateLimit] . MSRC001_003E[HtcPstateLimit] is an alias of D18F3x64[HtcPstateLimit] .

27:24	HtcHystLmt: HTC hysteresis. MSRC001_003E [HtcHystLmt] is an alias of D18F3x64 [HtcHystLmt].
23	HtcSlewSel: HTC slew-controlled temperature select. MSRC001_003E [HtcSlewSel] is an alias of D18F3x64 [HtcSlewSel].
22:16	HtcTmpLmt: HTC temperature limit. MSRC001_003E [HtcTmpLmt] is an alias of D18F3x64 [HtcTmpLmt].
7	PslApicLoEn: P-state limit lower value change APIC interrupt enable. MSRC001_003E [PslApicLoEn] is an alias of D18F3x64 [PslApicLoEn].
6	PslApicHiEn: P-state limit higher value change APIC interrupt enable. MSRC001_003E [PslApicHiEn] is an alias of D18F3x64 [PslApicHiEn].
5	HtcActSts: HTC-active status. MSRC001_003E [HtcActSts] is an alias of D18F3x64 [HtcActSts].
4	HtcAct: HTC-active state. MSRC001_003E [HtcAct] is an alias of D18F3x64 [HtcAct].
0	HtcEn: HTC enable. MSRC001_003E [HtcEn] is an alias of D18F3x64 [HtcEn].

MSRC001_0044 DC Machine Check Control Mask (MC0_CTL_MASK)

Read-write. Reset: 0000_0000_0000_0000h. BIOS: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSR0000_0400 \[MC0 Machine Check Control \(MC0_CTL\)\]](#).

Bits	Description
63:12	Reserved.
11	SRDE_ALLMsk: all system read data errors mask. Read-write. See DDPMsk.
10	SRDETMsk: read data errors on TLB reload mask. Read-write. See DDPMsk.
9	SRDESMSk: read data errors on store mask. Read-write. See DDPMsk.
8	SRDELMSk: read data errors on load mask. Read-write. See DDPMsk.
7	TLB2MMsk: L2DTLB multi-hit mask. Read-write. 1=Disable detection. See DDPMsk.
6	TLB2PMsk: L2DTLB parity mask. Read-write. 1=Disable detection. See DDPMsk.
5	TLB1MMsk: L1DTLB multi-hit mask. Read-write. 1=Disable detection. See DDPMsk.
4	Reserved.
3	DTPMSk: tag array parity errors mask. Read-write. See DDPMsk.
2	DDPMsk: data array parity errors mask. Read-write. 1=Disable error logging in MSR0000_0401 [MC0 Machine Check Status (MC0_STATUS)] and MSR0000_0402 [MC0 Machine Check Address (MC0_ADDR)] for errors represented by this bit. This bit also disables error detection, and prevents error responses. See 2.14.1 [Machine Check Architecture] and MSR0000_0400 [MC0 Machine Check Control (MC0_CTL)] .
1:0	Reserved.

MSRC001_0045 IC Machine Check Control Mask (MC1_CTL_MASK)

Reset: 0000_0000_0000_0000h. BIOS: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSR0000_0404 \[MC1 Machine Check Control \(MC1_CTL\)\]](#).

Bits	Description
63:10	Reserved.

9	SRDEMsK: read data errors mask. Read-write. See: IDPMsk.
8:7	Reserved.
6	TLBPMsk: TLB parity errors mask. Read-write. See: IDPMsk.
5	Reserved.
4	ISTPMsk: snoop tag array parity errors mask. Read-write. See: IDPMsk.
3	ITPMsk: tag array parity errors mask. Read-write. See: IDPMsk.
2	IDPMsk: data array parity errors mask. Read-write. 1=Disable error logging in MSR0000_0405 [MC1 Machine Check Status (MC1_STATUS)] and MSR0000_0406 [MC1 Machine Check Address (MC1_ADDR)] for errors represented by this bit. This bit also disables error detection, and prevents error responses. See 2.14.1 [Machine Check Architecture] and MSR0000_0404 [MC1 Machine Check Control (MC1_CTL)] .
1	IVPMsk: victim parity error mask. Read-write. 1=Disable logging victim parity errors.
0	PRPEMsk: ME patch RAM parity error mask. Read-write. 1=Disable logging patch ram parity errors.

MSRC001_0046 BU Machine Check Control Mask (MC2_CTL_MASK)

Read-write. Reset: 0000_0000_0000_0000h. BIOS: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSR0000_0408 \[MC2 Machine Check Control \(MC2_CTL\)\]](#).

Bits	Description
63:14	Reserved.
13	AttrParity: report attribute parity errors.
12:9	Reserved.
8	DataUncor: report uncorrectable data errors.
7	DataCor: report correctable data errors.
6	DataParity: report data parity errors.
5	TagUncor: report uncorrectable tag errors.
4	TagCor: report correctable tag errors.
3	Reserved.
2	NbFill: NB read response error due to a fill.
1	NbRead: NB read response error due to a write/victim.
0	Reserved.

MSRC001_0047 Reserved (MC3_CTL_MASK)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	Reserved.

MSRC001_0048 NB Machine Check Control Mask (MC4_CTL_MASK)

IF (D18F3x44[NbMcaToMstCpuEn] && !NBC) THEN RAZ. ELSE Read-write; Per-node. Reset: 0000_0000_0400_0000h. BIOS: 0000_0000_0400_0000h. ENDIF. The format of MC4_CTL_MASK corresponds to [MSR0000_0410 \[MC4 Machine Check Control \(MC4_CTL\)\]](#). For each defined bit position, 1=Disable logging. Only one of these registers exists in multi-core devices; see [3.1.1 \[Northbridge MSRs In Multi-Core Products\]](#). See [2.14.1 \[Machine Check Architecture\]](#). Accessibility of this register by non-NBC cores is affected by D18F3x44[NbMcaToMstCpuEn]. MSRC001_0048[31:0] is an alias of D18F3x198. See [MSR0000_0410 \[MC4 Machine Check Control \(MC4_CTL\)\]](#).

Bits	Description
63:32	Reserved.
31	McaCpuDatErrEn.
29	UCRCEn.
28	CCRCEn.
27	Reserved. Read-write.
26	NbArrayParEn. Parity error checking may be enabled if NB power gating is disabled.
25	UsPwDatErrEn.
24:18	Reserved. Read-write.
17	CpPktDatEn.
16	NbIntProtEn.
15:13	Reserved. Read-write.
12	WDTRptEn.
11	AtomicRMWEn.
10	Reserved. Read-write.
9	TgtAbortEn.
8	MstrAbortEn.
7:6	Reserved. Read-write.
5	SyncPktEn.
4:2	Reserved. Read-write.
1	UECCEn.
0	CECCEn.

MSRC001_0049 FR Machine Check Control Mask (MC5_CTL_MASK)

Reset: 0000_0000_0000_0000h. BIOS: 0000_0000_0000_0000h. See [2.14.1 \[Machine Check Architecture\]](#). See [MSR0000_0414 \[MC5 Machine Check Control \(MC5_CTL\)\]](#).

Bits	Description

63:1	Reserved.
0	CPUWDTMsk: CPU watchdog timer mask. Read-write. 1=Disable error logging in MSR0000_0415 [MC5 Machine Check Status (MC5_STATUS)] and MSR0000_0416 [MC5 Machine Check Address (MC5_ADDR)] for errors represented by this bit. This bit also disables error detection, and prevents error responses. See 2.14.1 [Machine Check Architecture] and MSR0000_0414 [MC5 Machine Check Control (MC5_CTL)] .

MSRC001_00[53:50] IO Trap (SMI_ON_IO_TRAP_[3:0])

Reset: 0000_0000_0000_0000h.

[MSRC001_00\[53:50\]](#) and [MSRC001_0054](#) provide a mechanism for executing the SMI handler if a an access to one of the specified addresses is detected. Access address and access type checking is performed before IO instruction execution. If the access address and access type match one of the specified IO address and access types, then: (1) the IO instruction is not executed; (2) any breakpoint, other than the single-step breakpoint, set on the IO instruction is not taken (the single-step breakpoint is taken after resuming from SMM); and (3) the SMI-trigger IO cycle specified by [MSRC001_0056](#). The status is stored in [SMMFEC4\[IoTrapSts\]](#).

IO-space configuration accesses are special IO accesses. An IO access is defined as an IO-space configuration access when IO instruction address bits[31:0] are CFCh, CFDh, CFEh, or CFFh when IO-space configuration is enabled ([IOCF8\[ConfigEn\]](#)). The access address for a configuration space access is the current value of [IOCF8\[BusNo, Device, Function, RegNo\]](#). The access address for an IO access that is not a configuration access is equivalent to the IO instruction address, bits[31:0].

The access address is compared with SmiAddr, and the instruction access type is compared with the enabled access types defined by ConfigSMI, SmiOnRdEn, and SmiOnWrEn. Access address bits[23:0] can be masked with SmiMask.

IO and configuration space trapping to SMI applies only to single IO instructions; it does not apply to string and REP IO instructions.

The conditional GP fault described by [MSRC001_0015\[IoCfgGpFault\]](#) takes priority over this trap.

Table 220: Register Mapping for [MSRC001_00\[53:50\]](#)

Register	Function
MSRC001_0050	Range 0
MSRC001_0051	Range 1
MSRC001_0052	Range 2
MSRC001_0053	Range 3

Bits	Description
63	SmiOnRdEn: enable SMI on IO read. Read-write. 1=Enables SMI generation on a read access.
62	SmiOnWrEn: enable SMI on IO write. Read-write. 1=Enables SMI generation on a write access.
61	ConfigSmi: configuration space SMI. Read-write. 1=Configuration access. 0=IO access (that is not an IO-space configuration access).
60:56	Reserved. Read-write.

55:32	SmiMask[23:0] . Read-write. SMI IO trap mask. 0=Mask address bit. 1=Do not mask address bit.
31:0	SmiAddr[31:0] . Read-write. SMI IO trap address.

MSRC001_0054 IO Trap Control (SMI_ON_IO_TRAP_CTL_STS)

For each of the SmiEn bits below, 1=The trap specified by the corresponding MSR is enabled. See [MSRC001_00\[53:50\]](#).

Bits	Description
63:32	RAZ.
31:16	Reserved. Read-write.
15	IoTrapEn: IO trap enable . Read-write. Reset: 0. 1=Enable IO and configuration space trapping specified by MSRC001_00[53:50] and MSRC001_0054 .
14:8	Reserved. Read-write.
7	SmiEn3: SMI enable for the trap specified by MSRC001_0053 . Read-write. Reset: 0.
6	Reserved. Read-write.
5	SmiEn2: SMI enable for the trap specified by MSRC001_0052 . Read-write. Reset: 0.
4	Reserved. Read-write.
3	SmiEn1: SMI enable for the trap specified by MSRC001_0051 . Read-write. Reset: 0.
2	Reserved. Read-write.
1	SmiEn0: SMI enable for the trap specified by MSRC001_0050 . Read-write. Reset: 0.
0	Reserved. Read-write.

MSRC001_0055 Interrupt Pending

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	RAZ.

MSRC001_0056 SMI Trigger IO Cycle

Not-same-for-all; S3-check-exclude. Reset: 0000_0000_0000_0000h. See [2.4.8.2.3 \[SMI Sources And Delivery\]](#). This register specifies an IO cycle that may be generated when a local SMI trigger event occurs. If IoCycleEn is set and there is a local SMI trigger event, then the IO cycle generated is a byte read or write, based on IoRd, to address IoPortAddress. If the cycle is a write, then IoData contains the data written. If the cycle is a read, the value read is discarded. If IoCycleEn is clear and a local SMI trigger event occurs, then undefined behavior results.

Bits	Description
63:32	Reserved.
31:27	Reserved. Read-write.
26	IoRd: IO Read . Read-write. 1=IO read; 0=IO write.

25	IoCycleEn: IO cycle enable. Read-write. 1=The SMI trigger IO cycle is enabled to be generated.
24	Reserved. Read-write.
23:16	IoData. Read-write.
15:0	IoPortAddress. Read-write.

MSRC001_0058 MMIO Configuration Base Address

Same-for-all. See [2.7 \[Configuration Space\]](#) for a description of MMIO configuration space.

Bits	Description																								
63:40	RAZ.																								
39:20	MmioCfgBaseAddr[39:20]: MMIO configuration base address bits[39:20]. Read-write. Reset: 0. Specifies the base address of the MMIO configuration range. The size of the MMIO configuration-space address range is specified by SegBusRange as follows. All lower order undefined bits must be 0. <table> <thead> <tr> <th><u>BusRange</u></th> <th><u>MmioCfgBaseAddr</u></th> <th><u>BusRange</u></th> <th><u>MmioCfgBaseAddr</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>[39:20]</td> <td>5h</td> <td>[39:25]</td> </tr> <tr> <td>1h</td> <td>[39:21]</td> <td>6h</td> <td>[39:26]</td> </tr> <tr> <td>2h</td> <td>[39:22]</td> <td>7h</td> <td>[39:27]</td> </tr> <tr> <td>3h</td> <td>[39:23]</td> <td>8h</td> <td>[39:28]</td> </tr> <tr> <td>4h</td> <td>[39:24]</td> <td>Fh-9h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>BusRange</u>	<u>MmioCfgBaseAddr</u>	<u>BusRange</u>	<u>MmioCfgBaseAddr</u>	0h	[39:20]	5h	[39:25]	1h	[39:21]	6h	[39:26]	2h	[39:22]	7h	[39:27]	3h	[39:23]	8h	[39:28]	4h	[39:24]	Fh-9h	Reserved
<u>BusRange</u>	<u>MmioCfgBaseAddr</u>	<u>BusRange</u>	<u>MmioCfgBaseAddr</u>																						
0h	[39:20]	5h	[39:25]																						
1h	[39:21]	6h	[39:26]																						
2h	[39:22]	7h	[39:27]																						
3h	[39:23]	8h	[39:28]																						
4h	[39:24]	Fh-9h	Reserved																						
19:6	RAZ.																								
5:2	BusRange: bus range identifier. Read-write. Reset: 0. Specifies the number of buses in the MMIO configuration space range. The size of the MMIO configuration space is 1 MB times the number of buses. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Description</u></th> <th><u>Bits</u><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>1</td> <td>5h32</td> </tr> <tr> <td>1h</td> <td>2</td> <td>6h64</td> </tr> <tr> <td>2h</td> <td>4</td> <td>7h128</td> </tr> <tr> <td>3h</td> <td>8</td> <td>8h256</td> </tr> <tr> <td>4h</td> <td>16</td> <td>Fh-9hReserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	<u>Bits</u> <u>Description</u>	0h	1	5h32	1h	2	6h64	2h	4	7h128	3h	8	8h256	4h	16	Fh-9hReserved						
<u>Bits</u>	<u>Description</u>	<u>Bits</u> <u>Description</u>																							
0h	1	5h32																							
1h	2	6h64																							
2h	4	7h128																							
3h	8	8h256																							
4h	16	Fh-9hReserved																							
0	Enable. Read-write. Reset: 0. 1=MMIO configuration space is enabled.																								

MSRC001_0060 BIST Results

Read; GP-write. Reset: 0000_0000_xxxx_xxxxh. This register provides BIST results after each reset. The results provided here are identical to the values provided in EAX. If ([MSRC001_0060](#)[29:0]=0000_0000h) then no BIST failures were detected. Bits[31:0] below provide the BIST test name; 1=A failure was detected on that test.

Bits	Description
63:32	Reserved.

MSRC001_0061 P-state Current Limit

Read; GP-write; updated-by-hardware. See [2.5.3 \[CPU Power Management\]](#).

Bits	Description
63:7	RAZ.
6:4	PstateMaxVal: P-state maximum value. Specifies the lowest-performance non-boosted P-state (highest non-boosted value) allowed. Attempts to change MSRC001_0062[PstateCmd] to a lower-performance P-state (higher value) are clipped to the value of this field. This clipping is enforced by microcode, see MSRC001_0062[PstateCmd] . This field uses software P-state numbering. See 2.5.3.1.1.1 [Software P-state Numbering] . The state of this field is controlled through D18F3xDC[HwPstateMaxVal] .
3	RAZ.
2:0	CurPstateLimit: current P-state limit. Specifies the highest-performance non-boosted P-state (lowest value) allowed. CurPstateLimit is always bounded by MSRC001_0061[PstateMaxVal] . Attempts to change the CurPstateLimit to a value greater (lower performance) than MSRC001_0061[PstateMaxVal] leaves CurPstateLimit unchanged. This field uses software P-state numbering. See MSRC001_0071[CurPstateLimit] and 2.5.3.1.1.1 [Software P-state Numbering] . CurPstateLimit = Max { (D18F3x64[HtcAct] =1, (D18F3x68[SwPstateLimit] - D18F4x15C[NumBoostStates]) if D18F3x64[HtcAct] =1, (D18F3x68[SwPstateLimitEn] =1}.

MSRC001_0062 P-state Control

Bits	Description
63:3	MBZ.
2:0	PstateCmd: P-state change command. Read-write; Not-same-for-all. Cold reset value varies by product; after a warm reset, value initializes to the P-state the core was in prior to the reset; copied from MSRC001_0071[CurPstate] after all resets. Writes to this field cause the core to change to the indicated non-boosted P-state number, specified by MSRC001_00[6B:64] . 0=P0, 1=P1, etc. P-state limits are applied to any P-state requests made through this register. Reads from this field return the last written value, regardless of whether any limits are applied. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering] . Writes to this field that do not change MSRC001_0063[CurPstate] cause VID changes but do not cause COF updates if the corresponding MSRC001_00[6B:64] have changed.

MSRC001_0063 P-state Status

Read; GP-write; Updated-by-hardware.

Bits	Description
63:3	RAZ.
2:0	CurPstate: current P-state. Cold reset: MSRC001_0071 [CurPstate]. This field provides the frequency component of the current non-boosted P-state of the core (regardless of the source of the P-state change, including MSRC001_0062 [PstateCmd] and D18F3xC4 [SBI P-state Limit] ; see 2.5.3.1.5 [Core P-state Transition Behavior] for information on how these interact). 0=P0, 1=P1, etc. The value of this field is updated when the COF transitions to a new value associated with a P-state. This field uses software P-state numbering. See 2.5.3 [CPU Power Management] and 2.5.3.1.1.1 [Software P-state Numbering] . This field is transported from D18F3xC8 after the value is modified as specified by 2.5.5.1.6 [Modification of P-state Requests and Visibility] .

MSRC001_00[6B:64] P-state [7:0]

Per-node. Cold reset:[D18F4x1\[FC:E0\]](#). Each of these registers specify the frequency and voltage associated with each of the core P-states.

Table 221: Register Mapping for MSRC001_00[6B:64]

Register	Function
MSRC001_0064	P-state 0
MSRC001_0065	P-state 1
MSRC001_0066	P-state 2
MSRC001_0067	P-state 3
MSRC001_0068	P-state 4
MSRC001_0069	P-state 5
MSRC001_006A	P-state 6
MSRC001_006B	P-state 7

The CpuVid field in these registers is required to be programmed to the same value in all cores of a processor, but are allowed to be different between processors in a multi-processor system. All other fields in these registers are required to be programmed to the same value in each core of the coherent fabric. See [2.5.3 \[CPU Power Management\]](#).

When [D18F4x15C](#)[BoostLock]=1, [MSRC001_00\[6B:64\]](#)[CpuVid, CpuDid, CpuFid] have special write requirements associated with them. These requirements are enforced by the Northbridge prior to writing [D18F4x1\[FC:E0\]](#). Microcode transports this register to [D18F4x1\[FC:E0\]](#).

Table 222: P-state Definitions

Term	Definition
CoreCOF	Core current operating frequency in MHz. CoreCOF = 100 * (MSRC001_00[6B:64] [CpuFid] + 10h) / (2^ MSRC001_00[6B:64] [CpuDid]).

Bits	Description										
63	PstateEn. Read-write. 1=The P-state specified by this MSR is valid. 0=The P-state specified by this MSR is not valid. The purpose of this register is to indicate if the rest of the P-state information in the register is valid after a reset; it controls no hardware. Alias of D18F4x1[FC:E0][PstateEn] .										
62:42	RAZ.										
41:40	IddDiv: current divisor. Read-write. See IddValue. Alias of D18F4x1[FC:E0][IddDiv] .										
39:32	IddValue: current value. Read-write. After a reset, IddDiv and IddValue combine to specify the expected maximum current dissipation of a single core that is in the P-state corresponding to the MSR number. These values are intended to be used to create ACPI-defined _PSS objects (see 2.5.3.1.8.3 [ACPI Processor P-state Objects]) and to perform the 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check] . The values are expressed in amps; they are not intended to convey final product power levels; they may not match the power levels specified in the Power and Thermal Datasheets. Alias of D18F4x1[FC:E0][IddValue] . These fields are encoded as follows: <table> <thead> <tr> <th><u>IddDiv</u></th> <th><u>Description</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>IddValue / 1 A, Range: 0 to 255 A.</td> </tr> <tr> <td>01b</td> <td>IddValue / 10 A, Range: 0 to 25.5 A.</td> </tr> <tr> <td>10b</td> <td>IddValue / 100 A, Range: 0 to 2.55 A.</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>IddDiv</u>	<u>Description</u>	00b	IddValue / 1 A, Range: 0 to 255 A.	01b	IddValue / 10 A, Range: 0 to 25.5 A.	10b	IddValue / 100 A, Range: 0 to 2.55 A.	11b	Reserved
<u>IddDiv</u>	<u>Description</u>										
00b	IddValue / 1 A, Range: 0 to 255 A.										
01b	IddValue / 10 A, Range: 0 to 25.5 A.										
10b	IddValue / 100 A, Range: 0 to 2.55 A.										
11b	Reserved										
31:23	RAZ.										
22	NbPstate: Northbridge P-state. IF (MSRC001_0071[NbPstateDis]) THEN Read-only. ELSE Read-write. ENDIF. 1=Low performance NB P-state. 0=High performance NB P-state. If this bit is set in any given P-state register, then it must also be set in all enabled lower performance P-state registers as well. Equivalent P-states in each core must program this bit to the same value. See 2.5.4.1 [NB P-states] and D18F5x170[NbPstateThreshold, NbPstateLo, NbPstateHi] . Alias of D18F4x1[FC:E0][NbPstate] .										
21	RAZ.										
20:17	RAZ.										
16	CpuVid[7]: core VID bit[7]. Read-write. Except as required by 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check] , software should not modify this field. See CpuVid[6:0]. Alias of D18F4x1[FC:E0][CpuVid[7]] .										
15:9	CpuVid[6:0]: core VID. Read-write. Except as required by 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check] , software should not modify this field. See 2.5.1 [Processor Power Planes And Voltage Control] . If (D18F4x15C[BoostLock]==1), then CpuVid for boosted P-states can only be written with values that are greater than (lower voltages than) or equal to the reset value in CpuVid. Alias of D18F4x1[FC:E0][CpuVid[6:0]] .										

8:6	<p>CpuDid: core divisor ID. Read-write. Except as required by 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check], software should not modify this field. Specifies the core frequency divisor; see CpuFid. Writes of reserved values are ignored. Alias of D18F4x1[FC:E0][CpuDid].</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: left; padding-bottom: 2px;"><u>Bits</u></th><th style="text-align: left; padding-bottom: 2px;"><u>Description</u></th></tr> </thead> <tbody> <tr> <td style="padding-top: 2px;">0h</td><td>Divide-by 1</td></tr> <tr> <td style="padding-top: 2px;">1h</td><td>Divide-by 2</td></tr> <tr> <td style="padding-top: 2px;">2h</td><td>Divide-by 4</td></tr> <tr> <td style="padding-top: 2px;">3h</td><td>Divide-by 8</td></tr> <tr> <td style="padding-top: 2px;">4h</td><td>Divide-by 16</td></tr> <tr> <td style="padding-top: 2px;">7h-5h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Description</u>	0h	Divide-by 1	1h	Divide-by 2	2h	Divide-by 4	3h	Divide-by 8	4h	Divide-by 16	7h-5h	Reserved
<u>Bits</u>	<u>Description</u>														
0h	Divide-by 1														
1h	Divide-by 2														
2h	Divide-by 4														
3h	Divide-by 8														
4h	Divide-by 16														
7h-5h	Reserved														
5:0	<p>CpuFid[5:0]: core frequency ID. Read-write. Except as required by 2.5.3.1.7 [Processor-Systemboard Power Delivery Compatibility Check], software should not modify this field. Specifies the core frequency multiplier. The core COF is a function of CpuFid and CpuDid, and defined by CoreCOF. CpuFid and CpuDid must be programmed to the requirements specified in MSRC001_0071[MaxCpuCof] and D18F3xD4[MaxSwPstateCpuCof]. Writes to a non-boosted P-state with frequencies greater than D18F3xD4[MaxSwPstateCpuCof] are ignored. Writes to a boosted P-state with frequencies greater than MSRC001_0071[MaxCpuCof] are ignored. If D18F4x15C[BoostLock]=1, then CpuDid for boosted P-states can only be written with values that are greater than or equal to the reset value in CpuDid. If D18F4x15C[BoostLock]=1, then CpuFid for boosted P-states can only be written with values that are less than or equal to the reset value in CpuFid. See 2.5.3.1.5 [Core P-state Transition Behavior]. Alias of D18F4x1[FC:E0][CpuFid].</p>														

MSRC001_0070 COFVID Control

Cold reset: Product-specific. There is one register implemented for each core. This register includes several fields that are identical to [MSRC001_00\[6B:64\]](#). It is controlled by hardware for P-state transitions. It may also be used by software to directly control the current COF or VID. Alias of [D18F3xC0](#).

Accesses to this register that result in invalid COFs or VIDs are ignored. See [2.5.3 \[CPU Power Management\]](#).

Bits	Description
63:32	RAZ.
31:24	NbVid: Northbridge VID. IF (MSRC001_0071[NbPstateDis] IgnoreVidDidFid) THEN Read-only. ELSE Read-write. ENDIF. See D18F5x16[C:0][NbVid] . On a warm reset this field reflects the current VDDNB voltage.
23	RAZ.
22	NbPstate: Northbridge P-state. IF (MSRC001_0071[NbPstateDis]) THEN Read-only. ELSE Read-write. ENDIF. See MSRC001_00[6B:64][NbPstate] . On a warm reset this field reflects the current NB P-state and may not match MSRC001_00[6B:64][NbPstate] indexed by MSRC001_0071[CurPstate] .
21	RAZ.
20	CpuVid[7]. Read-write. See CpuVid[6:0] .

18:16	PstateId: P-state identifier. Read-write. Cold reset: Fuse[StartupPstate]. This field is required to provide the P-state number that is associated with the values of the other fields in this register. This value is used by the logic to determine if the P-state is increasing or decreasing. This field uses hardware P-state numbering. See 2.5.3.1.1.2 [Hardware P-state Numbering] .
15:9	CpuVid[6:0]: core VID. Read-write. See MSRC001_00[6B:64][CpuVid] . CpuVid[7:0] = {CpuVid[7], CpuVid[6:0]}. On a warm reset this field reflects the current VDD voltage and may not match MSRC001_00[6B:64][CpuVid] indexed by MSRC001_0071[CurPstate] .
8:6	CpuDid: core divisor ID. Read-write. See MSRC001_00[6B:64][CpuDid] . The PstateId field must be updated to cause a new CpuDid value to take effect.
5:0	CpuFid[5:0]: core frequency ID. Read-write. See MSRC001_00[6B:64][CpuFid] . The PstateId field must be updated to cause a new CpuFid value to take effect.

MSRC001_0071 COFVID StatusRead-only. See [2.5.3 \[CPU Power Management\]](#).

Bits	Description
63:59	MaxNbCof: maximum NB COF. Cold reset: Fuse[MaxNbCof]. Specifies the maximum NB COF supported by the processor. If MaxNbCof is greater than zero, the maximum frequency is 100 MHz * MaxNbCof; if MaxNbCof = 00h, then there is no frequency limit. Any attempt to change the NB COF to a frequency greater than specified by this field is ignored.
58:56	CurPstateLimit: current P-state limit. Updated-by-hardware. Provides the current lowest-performance P-state limit number. This register uses hardware P-state numbering. See MSRC001_0061[CurPstateLimit] and 2.5.3.1.1.2 [Hardware P-state Numbering] . Value: MAX(IF (D18F3x64[HtcAct]) THEN (D18F3x64[HtcPstateLimit]) ELSE 0 ENDIF, IF (D18F3x68[SwPstateLimitEn]) THEN D18F3x68[SwPstateLimit] ELSE 0 ENDIF, IF (D18F3xC4[PstateLimitEn]) THEN D18F3xC4[PstateLimit] ELSE 0 ENDIF, IF (D18F4x13C[SmuPstateLimitEn]) THEN D18F4x13C[SmuPstateLimit] ELSE 0 ENDIF, IF (ApmPstateLimitEn) THEN ApmPstateLimit ELSE D18F4x15C[NumBoostStates] ENDIF). ApmPstateLimit and ApmPstateLimitEn are internal, non-software visible registers. See 2.5.9.3 [Bidirectional Application Power Management (BAPM)] for details on ApmPstateLimit and ApmPstateLimitEn.
55	Reserved.
54:49	MaxCpuCof: maximum core COF. Cold reset: Fuse[MaxCpuCof]. Specifies the maximum CPU COF supported by the processor. The maximum frequency is 100 MHz * MaxCpuCof, if MaxCpuCof is greater than zero; if MaxCpuCof = 00h, then there is no frequency limit. Any attempt to change a CPU COF to a frequency greater than specified by this field is ignored. Processors that support core performance boost must fuse this field to the maximum boosted P-state frequency or higher.
48:35	Reserved.

34:32	StartupPstate: startup P-state number. Cold reset: Fuse[StartupPstate]. Specifies the cold reset VID, FID and DID for the core based on the P-state number selected. StartupPstate uses hardware P-state numbering. See MSRC001_00[6B:64] and 2.5.3.1.1.2 [Hardware P-state Numbering] . If D18F3xA0[CoFVidProg]=0, then the state of this field is ignored and the VID, FID and DID are applied to the core as specified by that bit. Hardware verifies that MSRC001_00[6B:64] [CpuVid, CpuFid, CpuDid] for the P-state pointed to by StartupPstate are programmed as specified by MSRC001_0071 [MaxCpuCof]. Hardware does not verify that PstateEn is set. See 2.5.3.1.5 [Core P-state Transition Behavior] .
31:24	CurNbVid[7:0]: current NB VID. Read-only; updated-by-hardware. Cold reset: Fuse[NbVid[Fuse[StartupNbPstate]][7:0]]. This field specifies the current VDDNB voltage. MSRC001_0071 [CurNbVid[7:0]] is an alias of D18F5x174 [CurNbVid[7:0]].
23	NbPstateDis: NB P-states disabled. Value: D18F5x174 [NbPstateDis]. MSRC001_0071 [NbPstateDis] is an alias of D18F5x174 [NbPstateDis]. 0=NB P-state frequency and voltage changes are supported. See D18F5x170 [SwNbPstateLoDis, NbPstateDisOnP0]. 1=NB P-state frequency and voltage changes are disabled.
22	Reserved.
21	Reserved.
20	CurCpuVid[7]. Cold reset: Fuse[CpuVid[Fuse[StartupPstate]][7]]. See CurCpuVid[6:0].
19	Reserved. Reserved for future expansion of CurPstate.
18:16	CurPstate: current P-state. Cold reset: Fuse[StartupPstate]. Specifies the current P-state requested by the core. This field uses hardware P-state numbering. See MSRC001_0063 [CurPstate] and 2.5.3.1.1.2 [Hardware P-state Numbering] . When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.
15:9	CurCpuVid[6:0]: current core VID. Cold reset: Fuse[CpuVid[Fuse[StartupPstate]][6:0]]. CurCpuVid = {CurCpuVid[7], CurCpuVid[6:0]}. This field specifies the current VDD voltage.
8:6	CurCpuDid: current core divisor ID. Cold reset: Fuse[CpuDid[Fuse[StartupPstate]][2:0]]. Specifies the current CpuDid of the core. See MSRC001_00[6B:64] . When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.
5:0	CurCpuFid: current core frequency ID. Cold reset: Fuse[CpuFid[Fuse[StartupPstate]][5:0]]. Specifies the current CpuFid of the core. See MSRC001_00[6B:64] . When a P-state change is requested, the value in this field is updated once all required frequency and voltage transitions are completed.

MSRC001_0073 C-state Base Address

Reset: 0000_0000_0000_0000h.

Bits	Description
63:32	Reserved.
31:16	Reserved. Read-write.
15:0	CstateAddr: C-state address. Read-write. Specifies the IO addresses trapped by the core for C-state entry requests. A value of 0 in this field specifies that the core does not trap any IO addresses for C-state entry. Writing values greater than FF8h into this field result in undefined behavior. All other values cause the core to trap IO addresses CstateAddr through CstateAddr+7. See 2.5.3.2.2 [C-state Request Interface] , D18F4x11 [C:8], and D18F4x11C .

MSRC001_0074 CPU Watchdog Timer (CpuWdtCfg)Read-write; [Same-for-all](#). Reset: 0000_0000_0000_0000h.

The CPU watchdog timer (WDT) is implemented as a counter that counts out the time periods specified. The counter starts counting when CpuWdtEn is set. The counter does not count during halt or stop-grant. It restarts the count each time an operation of an instruction completes. If no operation completes by the specified time period, then a machine check error may be recorded if enabled (see [MSR0000_0414](#) through [MSR0000_0417](#)). If a watchdog timer error overflow occurs ([MSR0000_0415](#)[Overflow]), a sync flood can be generated if enabled in [D18F3x180](#)[SyncFloodOnCpuLeakErr].

The CPU watchdog timer must be set higher than the NB watchdog timer ([D18F3x44](#) [MCA NB Configuration]) in order to allow remote requests to complete. The CPU watchdog timer must be set the same for all CPUs in a system.

Bits	Description																												
63:7	Reserved.																												
6:3	CpuWdtCountSel: CPU watchdog timer count select. CpuWdtCountSel and CpuWdtTimeBase together specify the time period required for the WDT to expire. The time period is ((the multiplier specified by CpuWdtCountSel) * (the time base specified by CpuWdtTimeBase)). The actual timeout period may be anywhere from zero to one increments less than the values specified, due to non-deterministic behavior. <table> <thead> <tr> <th>Bits</th> <th>Multiplier</th> <th>Bits</th> <th>Multiplier</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>4095</td> <td>6h63</td> <td></td> </tr> <tr> <td>1h</td> <td>2047</td> <td>7h31</td> <td></td> </tr> <tr> <td>2h</td> <td>1023</td> <td>8h8191</td> <td></td> </tr> <tr> <td>3h</td> <td>511</td> <td>9h16383</td> <td></td> </tr> <tr> <td>4h</td> <td>255</td> <td>Fh-AhReserved</td> <td></td> </tr> <tr> <td>5h</td> <td>127</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Multiplier	Bits	Multiplier	0h	4095	6h63		1h	2047	7h31		2h	1023	8h8191		3h	511	9h16383		4h	255	Fh-AhReserved		5h	127		
Bits	Multiplier	Bits	Multiplier																										
0h	4095	6h63																											
1h	2047	7h31																											
2h	1023	8h8191																											
3h	511	9h16383																											
4h	255	Fh-AhReserved																											
5h	127																												
2:1	CpuWdtTimeBase: CPU watchdog timer time base. Specifies the time base for the timeout period specified in CpuWdtCountSel. MSRC001_0074 [CpuWdtTimeBase] is an alias of D18F3x108 [CpuWdtTimeBase]. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.31 ms</td> </tr> <tr> <td>01b</td> <td>1.28 us</td> </tr> <tr> <td>10b</td> <td>Reserved (5 ns)</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00b	1.31 ms	01b	1.28 us	10b	Reserved (5 ns)	11b	Reserved																		
Bits	Description																												
00b	1.31 ms																												
01b	1.28 us																												
10b	Reserved (5 ns)																												
11b	Reserved																												
0	CpuWdtEn: CPU watchdog timer enable. 1=The WDT is enabled.																												

MSRC001_0080 Frequency Sensitivity Feedback Monitor Actual Count 0

GP-write. See [2.7.3 \[Frequency Sensitivity\]](#).

Bits	Description								
63:56	ClassCode. Read; GP-write. Value: 01h. Specifies the core frequency sensitivity class for this feedback monitor. <table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00h</td><td>Reserved</td></tr> <tr> <td>01h</td><td>Core frequency sensitivity.</td></tr> <tr> <td>FFh-02h</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	00h	Reserved	01h	Core frequency sensitivity.	FFh-02h	Reserved
Bits	Description								
00h	Reserved								
01h	Core frequency sensitivity.								
FFh-02h	Reserved								
55:0	ActualCount. Read; GP-write; updated-by-hardware. Reset: 0. Specifies the actual count of this feedback monitor. See CPUID Fn8000_0007_EAX[MaxWrapTime] .								

MSRC001_0081 Frequency Sensitivity Feedback Monitor Reference Count 0

GP-write. See [2.7.3 \[Frequency Sensitivity\]](#).

Bits	Description
63:56	ClassCode. Value: 01h. See: MSRC001_0080 [ClassCode]. Specifies the core frequency sensitivity class for this feedback monitor.
55:0	RefCount. Read-only; updated-by-hardware. Reset: 0. Specifies the reference count of this feedback monitor. See CPUID Fn8000_0007_EAX[MaxWrapTime] .

MSRC001_0111 SMM Base Address (SMM_BASE)

Reset: 0000_0000_0003_0000h. This holds the base of the SMM memory region. The value of this register is stored in the save state on entry into SMM (see [2.4.8.2.5 \[SMM Save State\]](#)) and it is restored on returning from SMM. The 16-bit CS (code segment) selector is loaded with SmmBase[19:4] on entering SMM.

SmmBase[3:0] is required to be 0. The SMM base address can be changed in two ways:

- The SMM base address, at offset FF00h in the SMM state save area, may be changed by the SMI handler. The RSM instruction updates SmmBase with the new value.
- Normal WRMSR access to this register.

Bits	Description
63:32	Reserved.
31:0	SmmBase. IF MSRC001_0015 [SmmLock] THEN Read-only; Not-same-for-all. ELSE Read-write; Not-same-for-all. ENDIF.

MSRC001_0112 SMM TSeg Base Address (SMMAddr)

Reset: 0000_0000_0000_0000h.

See [2.4.8.2 \[System Management Mode \(SMM\)\]](#) and [2.4.6.1 \[Memory Access to the Physical Address Space\]](#). See [MSRC001_0113](#) for more information about the ASeg and TSeg address ranges.

Each CPU access, directed at CPUAddr, is determined to be in the TSeg range if the following is true:

CPUAddr[39:17] & TSegMask[39:17] == TSegBase[39:17] & TSegMask[39:17].

For example, if TSeg spans 256 KB and starts at the 1 MB address. The [MSRC001_0112](#)[TSegBase] would be set to 0010_0000h and the [MSRC001_0113](#)[TSegMask] to FFFC_0000h (with zeros filling in for bits[16:0]). This results in a TSeg range from 0010_0000 to 0013_FFFFh.

Bits	Description
63:40	Reserved.
39:17	TSegBase[39:17]: TSeg address range base. IF MSRC001_0015 [SmmLock] THEN Read-only ELSE Read-write ENDIF.
16:0	Reserved.

MSRC001_0113 SMM TSeg Mask (SMMMask)

Reset: 0000_0000_0000_0000h. See [2.4.8.2 \[System Management Mode \(SMM\)\]](#).

The ASeg address range is located at a fixed address from A0000h–BFFFFh. The TSeg range is located at a variable base (specified by [MSRC001_0112](#)[TSegBase]) with a variable size (specified by [MSRC001_0113](#)[TSegMask]). These ranges provide a safe location for SMM code and data that is not readily accessible by non-SMM applications. The SMI handler can be located in one of these two ranges, or it can be located outside these ranges. These ranges must never overlap each other.

This register specifies how accesses to the ASeg and TSeg address ranges are controlled as follows:

- If [A,T]Valid=1, then:
 - If in SMM, then:
 - If [A, T]Close=0, then the accesses are directed to DRAM with memory type as specified in [A, T]MTTypeDram.
 - If [A, T]Close=1, then instruction accesses are directed to DRAM with memory type as specified in [A, T]MTTypeDram and data accesses are directed at MMIO space and with attributes based on [A, T]MTTypeIoWc.
 - If not in SMM, then the accesses are directed at MMIO space with attributes based on [A,T]MTTypeIoWc.
- See [2.4.6.1.1 \[Determining Memory Type\]](#).

Bits	Description
63:40	Reserved.
39:17	TSegMask[39:17]: TSeg address range mask. IF MSRC001_0015 [SmmLock] THEN Read-only ELSE Read-write ENDIF. See MSRC001_0112 .
16:15	Reserved.
14:12	TMTTypeDram: TSeg address range memory type. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. Specifies the memory type for SMM accesses to the TSeg range that are directed to DRAM. See: Table 191 [Valid Values for Memory Type Definition] .
11	Reserved.
10:8	AMTypeDram: ASeg Range Memory Type. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. Specifies the memory type for SMM accesses to the ASeg range that are directed to DRAM. See: Table 191 [Valid Values for Memory Type Definition] .
7:6	Reserved.

5	TMTTypeIoWc: non-SMM TSeg address range memory type. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. Specifies the attribute of TSeg accesses that are directed to MMIO space. 0=UC (uncacheable). 1=WC (write combining).
4	AMTypeIoWc: non-SMM ASeg address range memory type. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. Specifies the attribute of ASeg accesses that are directed to MMIO space. 0=UC (uncacheable). 1=WC (write combining).
3	TClose: send TSeg address range data accesses to MMIO. Read-write. 1=When in SMM, direct data accesses in the TSeg address range to MMIO space. See ACclose.
2	AClose: send ASeg address range data accesses to MMIO. Read-write. 1=When in SMM, direct data accesses in the ASeg address range to MMIO space. [A, T]Close allows the SMI handler to access the MMIO space located in the same address region as the [A, T]Seg. When the SMI handler is finished accessing the MMIO space, it must clear the bit. Failure to do so before resuming from SMM causes the CPU to erroneously read the save state from MMIO space.
1	TValid: enable TSeg SMM address range. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. 1=The TSeg address range SMM enabled.
0	AValid: enable ASeg SMM address range. IF MSRC001_0015 [SmmLock] THEN Read-only. ELSE Read-write. ENDIF. 1=The ASeg address range SMM enabled.

MSRC001_0114 Virtual Machine Control (VM_CR)

Bits	Description
63:32	Reserved.
31:5	MBZ.
4	SvmeDisable: SVME disable. See Lock for the access type of this field. Reset: 0. 1= MSRC000_0080 [SVME] is MBZ. 0= MSRC000_0080 [SVME] is read-write. Attempting to set this field when (MSRC000_0080 [SVME]==1) causes a #GP fault, regardless of the state of Lock. See the APM2 section titled “Enabling SVM” for software use of this field.
3	Lock: SVM lock. Read-only; write-1-only; cleared-by-hardware. Reset: 0. See MSRC001_0118 [SvmLockKey] for the condition that causes hardware to clear this field. 1=SvmeDisable is read-only. 0=SvmeDisable is read-write.
2	DisA20m: disable A20 masking. Read-write; set-by-hardware. Reset: 0. 1=Disables A20 masking. This bit is set by hardware when the SKINIT instruction is executed.
1	InterceptInit: intercept INIT. Read-write; set-by-hardware. Reset: 0. This bit controls how INIT is delivered in host mode. This bit is set by hardware when the SKINIT instruction is executed. 0=INIT delivered normally. 1=INIT translated into a SX interrupt.
0	DPD: debug port disable. Read-write; set-by-hardware. Reset: 0. Set by hardware when the SKINIT instruction is executed. This bit controls if debug facilities such as JTAG and HDT have access to the processor state information. 1=HDT is disabled; SB-IAI is disabled; see D18F3x1E4 [SbIaiDis]; functional chain fuses override disabled; RMW and Redundancy chain overrides (including cache size and core disable bits) are unaffected. 0=HDT may be enabled; SB-IAI may be enabled; see D18F3x1E4 [SwIaiDis]=0. Core DSM is automatically disabled when DPD transitions from 0 to 1.

MSRC001_0115 IGNNE

Bits	Description
63:32	Reserved.
31:1	MBZ.
0	IGNNE: current IGNNE state. Read-write. Reset: 0. This bit controls the current state of the processor internal IGNNE signal.

MSRC001_0116 SMM Control (SMM_CTL)

IF ([MSRC001_0015](#)[SmmLock]) THEN GP-read-write. ELSE GP-read; write-only. ENDIF.

The bits in this register are processed in the order of: SmmEnter, SmiCycle, SmmDismiss, RsmCycle and SmmExit. However, only the following combination of bits may be set in a single write (all other combinations result in undefined behavior):

- SmmEnter and SmiCycle.
- SmmEnter and SmmDismiss.
- SmmEnter, SmiCycle and SmmDismiss.
- SmmExit and RsmCycle.

Software is responsible for ensuring that SmmEnter and SmmExit operations are properly matched and are not nested.

Bits	Description
63:5	MBZ.
4	RsmCycle: send RSM special cycle. 1=Send a RSM special cycle.
3	SmmExit: exit SMM. 1=Exit SMM.
2	SmiCycle: send SMI special cycle. 1=Send a SMI special cycle.
1	SmmEnter: enter SMM. 1=Enter SMM.
0	SmmDismiss: clear SMI. 1=Clear the SMI pending flag.

MSRC001_0117 Virtual Machine Host Save Physical Address (VM_HSAVE_PA)

Bits	Description
63:40	MBZ.
39:12	VM_HSAVE_PA: physical address of host save area. Read-write. Reset: 0. This register contains the physical address of a 4-KB region where VMRUN saves host state and where vm-exit restores host state from. Writing this register causes a #GP if (FF_FFFF_Fh>=VM_HSAVE_PA>=FD_0000_0h).
11:0	MBZ.

MSRC001_0118 SVM Lock Key

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	SvmLockKey: SVM lock key. RAZ; write. Writes to this register when MSRC001_0114[Lock]==0 modify SvmLockKey. If ((MSRC001_0114[Lock]==1) && (SvmLockKey!=0) && (The write value==The value stored in SvmLockKey)) for a write to this register then hardware updates MSRC001_0114[Lock]=0 . If ((MSRC001_0114[Lock]==1) && ((SvmLockKey==0) ((SvmLockKey!=0) && (The write value!=The value stored in SvmLockKey))) for a write to this register then the write will be silently ignored and MSRC001_0114[Lock] is unmodified.

MSRC001_011A Local SMI Status

Reset: 0000_0000_0000_0000h. This registers returns the same information that is returned in [SMMFEC4 \[Local SMI Status\]](#) portion of the SMM save state. The information in this register is only updated when [MSRC001_0116\[SmmDismiss\]](#) is set by software.

Bits	Description
63:32	Reserved.
31:0	See SMMFEC4 [Local SMI Status] .

MSRC001_0140 OS Visible Work-around MSR0 (OSVW_ID_Length)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:16	Reserved. Read-write.
15:0	OSVWIdLength: OS visible work-around ID length. Read-write. See the Revision Guide for the definition of this field; see 1.2 [Reference Documents] .

MSRC001_0141 OS Visible Work-around MSR1 (OSVW_Status)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	OsvwStatusBits: OS visible work-around status bits. Read-write. See the Revision Guide for the definition of this field; see 1.2 [Reference Documents] .

MSRC001_023[6,4,2,0] L2I Performance Event Select (L2I_PERF_CTL[3:0])

Per-L2. Reset: 0000_0000_0000_0000h. See [2.6.1 \[Performance Monitor Counters\]](#).

Table 223: Register Mapping for MSRC001_023[6,4,2,0]

Register	Function
MSRC001_0230	Counter 0
MSRC001_0232	Counter 1
MSRC001_0234	Counter 2
MSRC001_0236	Counter 3

Bits	Description										
63:60	Reserved.										
59:56	ThreadMask[3:0] . Read-write. 0=Count events from the specified thread. 1=Mask count events from the specified thread. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Thread 0</td> </tr> <tr> <td>[1]</td> <td>Thread 1</td> </tr> <tr> <td>[2]</td> <td>Thread 2</td> </tr> <tr> <td>[3]</td> <td>Thread 3</td> </tr> </tbody> </table>	Bit	Description	[0]	Thread 0	[1]	Thread 1	[2]	Thread 2	[3]	Thread 3
Bit	Description										
[0]	Thread 0										
[1]	Thread 1										
[2]	Thread 2										
[3]	Thread 3										
55:52	Reserved.										
51:48	BankMask[3:0] . Read-write. 0=Count events from the specified bank. 1=Mask count events from the specified bank. <table> <thead> <tr> <th>Bit</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Bank 0</td> </tr> <tr> <td>[1]</td> <td>Bank 1</td> </tr> <tr> <td>[2]</td> <td>Bank 2</td> </tr> <tr> <td>[3]</td> <td>Bank 3</td> </tr> </tbody> </table>	Bit	Description	[0]	Bank 0	[1]	Bank 1	[2]	Bank 2	[3]	Bank 3
Bit	Description										
[0]	Bank 0										
[1]	Bank 1										
[2]	Bank 2										
[3]	Bank 3										
47:41	Reserved.										
40:37	IntCoreSel: interrupt to core select . Read-write. Specifies the logical core of the L2 complex to direct the interrupt.										
36	IntCoreEn: interrupt to core enable . Read-write. 1=Interrupt to a single core specified by IntCoreSel. 0=Interrupt to all cores.										
35:32	EventSelect[11:8]: performance event select . See: EventSelect[7:0].										
31:24	CntMask: counter mask . Read-write. Controls the number of events counted per clock cycle. <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>The corresponding L2I_PERF_CTL[3:0] register increments by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 4.</td> </tr> <tr> <td>03h-01h</td> <td>When Inv = 0, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value.</td> </tr> <tr> <td>FFh-04h</td> <td>When Inv = 1, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.</td> </tr> <tr> <td>FFh-04h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	00h	The corresponding L2I_PERF_CTL[3:0] register increments by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 4.	03h-01h	When Inv = 0, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value.	FFh-04h	When Inv = 1, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.	FFh-04h	Reserved
Bits	Description										
00h	The corresponding L2I_PERF_CTL[3:0] register increments by the number of events occurring in a clock cycle. Maximum number of events in one cycle is 4.										
03h-01h	When Inv = 0, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is greater than or equal to the CntMask value.										
FFh-04h	When Inv = 1, the corresponding L2I_PERF_CTL[3:0] register increments by 1, if the number of events occurring in a clock cycle is less than CntMask value.										
FFh-04h	Reserved										
23	Inv: invert counter mask . Read-write. See CntMask.										
22	En: enable performance counter . Read-write. 1= Performance event counter is enabled.										
21	Reserved.										
20	Int: enable APIC interrupt . Read-write. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via APIC340 [LVT Performance Monitor] when the performance counter overflows.										
18:16	Reserved.										

15:8	UnitMask: event qualification. Read-write. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused .
7:0	EventSelect[7:0]: event select. Read-write. This field, along with EventSelect[11:8] above, combine to form the 12-bit event select field, EventSelect[11:0]. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding PERF_CNT[3:0] register. The events are specified in section 3.23 [Core Performance Counter Events] . Some events are reserved; when a reserved event is selected, the results are undefined.

MSRC001_023[7,5,3,1] L2I Performance Event Counter (L2I_PERF_CTR[3:0])Per-L2. See [MSRC001_023\[6,4,2,0\] \[L2I Performance Event Select \(L2I_PERF_CTL\[3:0\]\)\]](#).

Table 224: Register Mapping for MSRC001_023[7,5,3,1]

Register	Function
MSRC001_0231	Counter 0
MSRC001_0233	Counter 1
MSRC001_0235	Counter 2
MSRC001_0237	Counter 3

Bits	Description
63:48	RAZ.
47:0	CTR: performance counter value. Read-write. Reset: 0.

MSRC001_024[6,4,2,0] Northbridge Performance Event Select (NB_PERF_CTL[3:0])Per-node. See [2.6.1 \[Performance Monitor Counters\]](#). MSRC001_024[6,4,2,0][31:0] is an alias of D18F5x[70,60,50,40]. MSRC001_024[6,4,2,0][63:32] is an alias of D18F5x[74,64,54,44].

Table 225: Register Mapping for MSRC001_024[6,4,2,0]

Register	Function
MSRC001_0240	Counter 0
MSRC001_0242	Counter 1
MSRC001_0244	Counter 2
MSRC001_0246	Counter 3

Bits	Description
35:32	EventSelect[11:8]: performance event select. Read-write. Reset: 0. See EventSelect[7:0].
31:23	Reserved.
22	En: enable performance counter. Read-write. Reset: 0. 1= Performance event counter is enabled.
21	Reserved.

20	Int: enable APIC interrupt. Read-write. Reset: 0. 1=APIC performance counter LVT interrupt is enabled to generate an interrupt via APIC340 [LVT Performance Monitor] to all or a single local APIC's on this node, based on IntCoreEn, when the performance counter overflows.
18:16	Reserved.
15:8	UnitMask: event qualification. Read-write. Reset: 0. Each UnitMask bit further specifies or qualifies the event specified by EventSelect. All events selected by UnitMask are simultaneously monitored. Unless otherwise stated, the UnitMask values shown may be combined (logically ORed) to select any desired combination of the sub-events for a given event. In some cases, certain combinations can result in misleading counts, or the UnitMask value is an ordinal rather than a bit mask. These situations are described where applicable, or should be obvious from the event descriptions. For events where no UnitMask table is shown, the UnitMask is Unused .
7:0	EventSelect[7:0]: event select. Read-write. Reset: 0. This field, along with EventSelect[11:8] above, combine to form the 12-bit event select field, EventSelect[11:0]. EventSelect specifies the event or event duration in a processor unit to be counted by the corresponding NB_PERF_CTR[3:0] register. The events are specified in 3.25 [NB Performance Counter Events] . Some events are reserved; when a reserved event is selected, the results are undefined.

MSRC001_024[7,5,3,1] Northbridge Performance Event Counter (NB_PERF_CTR[3:0])

Per-node. See [MSRC001_024\[6,4,2,0\] \[Northbridge Performance Event Select \(NB_PERF_CTL\[3:0\]\)\]](#).

[MSRC001_024\[7,5,3,1\]\[31:0\]](#) is an alias of D18F5x[78,68,58,48]. [MSRC001_024\[7,5,3,1\]\[63:32\]](#) is an alias of [D18F5x\[7C,6C,5C,4C\]](#).

Table 226: Register Mapping for MSRC001_024[7,5,3,1]

Register	Function
MSRC001_0241	Counter 0
MSRC001_0243	Counter 1
MSRC001_0245	Counter 2
MSRC001_0247	Counter 3

Bits	Description
63:48	RAZ.
47:32	CTR[47:32]: performance counter value[47:32]. See: CTR[31:0].
31:0	CTR[31:0]: performance counter value[31:0]. Read-write. Reset: 0. CTR[47:0] = {CTR[47:32], CTR[31:0]}. Returns the current value of the event counter.

3.22 MSRs - MSRC001_1xxx

MSRC001_1004 CPUID Features (Features)

Read-write. Reset: {CPUID Fn0000_0001_ECX, CPUID Fn0000_0001_EDX}. MSRC001_1004[63:32] provides back-door control over values read from CPUID Fn0000_0001_ECX; MSRC001_1004[31:0] provides back-door control over values read from CPUID Fn0000_0001_EDX.

Bits	Description
63	Reserved. Read-write. [63] is reserved for hypervisor.
62	RDRAND.
61	F16C.
60	AVX.
59	OSXSAVE. Modifies CPUID Fn0000_0001_ECX[OSXSAVE] only if CR4[OSXSAVE].
58	XSAVE.
57	AES. Modifies CPUID Fn0000_0001_ECX[AES] only if the reset value is 1 (~Fuse[AesDis]).
56	Reserved. Read-write.
55	POPCNT.
54	MOVBE.
53	x2APIC.
52	SSE42.
51	SSE41.
50:46	Reserved. Read-write.
45	CMPXCHG16B.
44:42	Reserved. Read-write.
41	SSSE3.
40:36	Reserved. Read-write.
35	Monitor. Modifies CPUID Fn0000_0001_ECX[Monitor] only if ~MSRC001_0015[MonMwaitDis].
34	Reserved. Read-write.
33	PCLMULQDQ. Modifies CPUID Fn0000_0001_ECX[PCLMULQDQ] only if the reset value is 1 (~Fuse[AesDis])
32	SSE3.
31:29	Reserved. Read-write.
28	HTT.
27	Reserved. Read-write.
26	SSE2.
25	SSE.
24	FXSR.
23	MMX.
22:20	Reserved. Read-write.

19	CLFSH.
18	Reserved. Read-write.
17	PSE36.
16	PAT.
15	CMOV.
14	MCA.
13	PGE.
12	MTRR.
11	SysEnterSysExit.
10	Reserved. Read-write.
9	APIC. Modifies CPUID Fn0000_0001_EDX [APIC] only if MSR0000_001B [ApicEn].
8	CMPXCHG8B.
7	MCE.
6	PAE.
5	MSR.
4	TSC.
3	PSE.
2	DE.
1	VME.
0	FPU.

MSRC001_1005 Extended CPUID Features (ExtFeatures)

Read-write. Reset: [{CPUID Fn8000_0001_ECX, CPUID Fn8000_0001_EDX}](#). MSRC001_1005[63:32] provides back-door control over values read from [CPUID Fn8000_0001_ECX](#); MSRC001_1005[31:0] provides back-door control over values read from [CPUID Fn8000_0001_EDX](#).

Bits	Description
63:61	Reserved. Read-write.
60	PerfCtrExtL2I.
59	PerfTsc.
58	DataBreakpointExtension.
56	PerfCtrExtNB.
55	PerfCtrExtCore.
54	TopologyExtensions.
53	TBM.
51	NodeId.
50	Reserved. Read-write.
48	FMA4.
47	LWP.

46	Reserved. Read-write.
45	WDT.
44	SKINIT.
43	XOP.
42	IBS.
41	OSVW.
40	3DNowPrefetch.
39	MisAlignSse.
38	SSE4A.
37	ABM.
36	AltMovCr8.
35	ExtApicSpace.
34	SVM. Modifies CPUID Fn8000_0001_ECX[SVM] only if D18F3xE8[SvmCapable].
33	CmpLegacy.
32	LahfSahf.
31	3DNow.
30	3DNowExt.
29	LM. Read-write.
28	Reserved. Read-write.
27	RDTSCP.
26	Page1GB.
25	FFXSR.
24	FXSR.
23	MMX.
22	MmxExt.
21	Reserved. Read-write.
20	NX.
19:18	Reserved. Read-write.
17	PSE36.
16	PAT.
15	CMOV.
14	MCA.
13	PGE.
12	MTRR.
11	SysCallSysRet.
10	Reserved. Read-write.
9	APIC.
8	CMPXCHG8B.

7	MCE.
6	PAE.
5	MSR.
4	TSC.
3	PSE.
2	DE.
1	VME.
0	FPU.

MSRC001_101[B:9] Address Mask For DR[3:1] Breakpoints

Reset: 0000_0000_0000_0000h. Support indicated by [CPUID Fn8000_0001_ECX](#)[DataBreakpointExtension]. See [MSRC001_1027](#).

Table 227: Register Mapping for MSRC001_101[B:9]

Register	Function
MSRC001_1019	DR1_ADDR_MASK
MSRC001_101A	DR2_ADDR_MASK
MSRC001_101B	DR3_ADDR_MASK

Table 228: Field Mapping for MSRC001_101[B:9]

Register	Bits
	31:0
MSRC001_1019	DR1
MSRC001_101A	DR2
MSRC001_101B	DR3

Bits	Description
63:32	Reserved.
31:0	AddrMask: mask for DR linear address data breakpoint. Read-write. This field qualifies the DR linear address data breakpoint, allowing the DR[3:1] data breakpoint on a range of addresses in memory. The mask bits are active high; 0=Include bit into address compare; 1=Exclude bit into address compare. AddrMask is always used, and it can be used in conjunction with any debug function that uses DR[3:1]. The legacy DR breakpoint function is provided by AddrMask[31:0]==0000_0000h).

MSRC001_1020 Load-Store Configuration (LS_CFG)

Bits	Description
63:53	Reserved. Read-write.
52	Reserved.

51	Reserved.
50:45	Reserved. Read-write.
26	DisHitCurPageOpt. Read-write. Reset: 0. BIOS: 1. 1=Disable current table-walk page hit optimization.
24	Reserved.

MSRC001_1021 Instruction Cache Configuration (IC_CFG)

Bits	Description
26	DIS_WIDEREAD_PWR_SAVE. Read-write; Same-for-all . Reset: 0. BIOS: 1. 1=Disable wide read power mgmt feature for read accesses to IC data array. See 2.3.4 [Instruction Cache Configuration Register Usage Requirements] .
9	DisSpecTlbRld. Read-write; Same-for-all . Reset: 0. BIOS: See 2.3.3 [Using L2 Cache as General Storage During Boot] . 1=Disable speculative TLB reloads. See 2.3.4 [Instruction Cache Configuration Register Usage Requirements] .

MSRC001_1022 Data Cache Configuration (DC_CFG)

Bits	Description
13	DisHwPf. Read-write. Reset: 0. BIOS: See 2.3.3 . 1=Disable hardware prefetches.
12:5	Reserved.
4	DisSpecTlbWalk. Read-write. Reset: 0. BIOS: See 2.3.3 . 1=Disable speculative table-walks.

MSRC001_1023 Bus Unit Configuration (BU_CFG)

Bits	Description

MSRC001_1027 Address Mask For DR0 Breakpoints (DR0_ADDR_MASK)

Reset: 0000_0000_0000_0000h. Support for AddrMaskDR0[31:12] is indicated by CPUID Fn8000_0001_ECX[DataBreakpointExtension]. See [MSRC001_101\[B:9\]](#).

Bits	Description
63:32	Reserved.
31:0	AddrMaskDR0: mask for DR0 linear address data breakpoint. Read-write. This field qualifies the DR0 linear address data breakpoint, allowing the DR0 data breakpoint on a range of addresses in memory. AddrMaskDR0[11:0] also qualifies the DR0 linear address instruction breakpoint, allowing the DR0 instruction breakpoint on a range of addresses in memory. The mask bits are active high; 0=Include bit into address compare; 1=Exclude bit into address compare. AddrMaskDR0 is always used, and it can be used in conjunction with any debug function that uses DR0. AddrMaskDR0[31:12] is only valid for data breakpoints. The legacy DR0 breakpoint function is provided by AddrMaskDR0[31:0]==0000_0000h).

MSRC001_1028 Floating Point Configuration (FP_CFG)

Bits	Description
------	-------------

MSRC001_102A Bus Unit Configuration 2 (BU_CFG2)

Bits	Description
15	CILinesToL2Dis. Read-write. Reset: 1. BIOS: See 2.3.3 [Using L2 Cache as General Storage During Boot] . 1=Clean victims and clean forced victims are not sent to the L2. When this bit is set, clean DC evictions and all IC evictions are discarded by the BU (not sent to L2I).
14:0	Reserved.

MSRC001_1030 IBS Fetch Control (IbsFetchCtl)

Reset: 0000_0000_0000_0000h. See [2.6.2 \[Instruction Based Sampling \(IBS\)\]](#).

The IBS fetch sampling engine is described as follows:

- The periodic fetch counter is an internal 20-bit counter:
 - The periodic fetch counter [19:4] is set to IbsFetchCnt[19:4] and the periodic fetch counter [3:0] is set according to IbsRandEn when IbsFetchEn is changed from 0 to 1.
 - It increments for every fetch cycle that completes when IbsFetchEn=1 and IbsFetchVal=0.
 - The periodic fetch counter is undefined when IbsFetchEn=0 or IbsFetchVal=1.
 - When IbsFetchCnt[19:4] is read it returns the current value of the periodic fetch counter [19:4].
- When the periodic fetch counter reaches {IbsFetchMaxCnt[19:4],0h} and the selected instruction fetch completes or is aborted:
 - IbsFetchVal is set to 1.
 - Drivers can't assume that IbsFetchCnt[19:4] is 0 when IbsFetchVal==1.
 - The status of the operation is written to the IBS fetch registers (this register, [MSRC001_1031](#) and [MSRC001_1032](#)).
 - An interrupt is generated as specified by [MSRC001_103A](#). The interrupt service routine associated with this interrupt is responsible for saving the performance information stored in IBS execution registers.

Bits	Description
63:59	Reserved.
58	Reserved.
57	IbsRandEn: random instruction fetch tagging enable. Read-write. 1=Bits[3:0] of the fetch counter are randomized when IbsFetchEn is set to start the fetch counter; the "random" value is taken from a free-running 4-bit counter. 0=Bits[3:0] of the fetch counter are set to 0h when IbsFetchEn is set to start the fetch counter.
56	IbsL2TlbMiss: instruction cache L2TLB miss. Read-write; set-by-hardware. 1=The instruction fetch missed in the L2 TLB.
55	IbsL1TlbMiss: instruction cache L1TLB miss. Read-write; set-by-hardware. 1=The instruction fetch missed in the L1 TLB.

54:53	IbsL1TlbPgSz: instruction cache L1TLB page size. Read-write; updated-by-hardware. Indicates the page size of the translation in the L1 TLB. This field is only valid if IbsPhyAddrValid==1.										
	<table> <thead> <tr> <th>Bits</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00b</td><td>4 KB</td></tr> <tr> <td>01b</td><td>2 MB</td></tr> <tr> <td>10b</td><td>Reserved</td></tr> <tr> <td>11b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Description	00b	4 KB	01b	2 MB	10b	Reserved	11b	Reserved
Bits	Description										
00b	4 KB										
01b	2 MB										
10b	Reserved										
11b	Reserved										
52	IbsPhyAddrValid: instruction fetch physical address valid. Read-write; set-by-hardware. 1=The physical address in MSRC001_1032 and the IbsL1TlbPgSz field are valid for the instruction fetch.										
51	IbsIcMiss: instruction cache miss. Read-write; set-by-hardware. 1=The instruction fetch missed in the instruction cache.										
50	IbsFetchComp: instruction fetch complete. Read-write; set-by-hardware. 1=The instruction fetch completed and the data is available for use by the instruction decoder.										
49	IbsFetchVal: instruction fetch valid. Read-write; set-by-hardware. 1>New instruction fetch data available. When this bit is set, the fetch counter stops counting and an interrupt is generated as specified by MSRC001_103A . This bit must be cleared for the fetch counter to start counting. When clearing this bit, software can write 0000h to IbsFetchCnt[19:4] to start the fetch counter at IbsFetchMaxCnt[19:4].										
48	IbsFetchEn: instruction fetch enable. Read-write. 1=Instruction fetch sampling is enabled.										
47:32	IbsFetchLat: instruction fetch latency. Read-write; set-by-hardware. Indicates the number of clock cycles from when the instruction fetch was initiated to when the data was delivered to the core. If the instruction fetch is abandoned before the fetch completes, this field returns the number of clock cycles from when the instruction fetch was initiated to when the fetch was abandoned.										
31:16	IbsFetchCnt[19:4]. Read-write; updated-by-hardware. Provides read/write access to bits[19:4] of the periodic fetch counter. Programming this field to a value greater than or equal to IbsFetchMaxCnt[19:4] results in undefined behavior.										
15:0	IbsFetchMaxCnt[19:4]. Read-write. Specifies bits[19:4] of the maximum count value of the periodic fetch counter. Programming this field to 0000h and setting IbsFetchEn results in undefined behavior. Bits[3:0] of the maximum count are always 0000b.										

MSRC001_1031 IBS Fetch Linear Address (IbsFetchLinAd)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	IbsFetchLinAd: instruction fetch linear address. Read-write; updated-by-hardware. Provides the linear address in canonical form for the tagged instruction fetch.

MSRC001_1032 IBS Fetch Physical Address (IbsFetchPhysAd)

Reset: 0000_0000_0000_0000h.

Bits	Description

63:40	Reserved.
39:0	IbsFetchPhysAd: instruction fetch physical address. Read-write; updated-by-hardware. Provides the physical address for the tagged instruction fetch. The lower 12 bits are not modified by address translation, so they are always the same as the linear address. This field contains valid data only if MSRC001_1030 [IbsPhyAddrValid] is asserted.

MSRC001_1033 IBS Execution Control (IbsOpCtl)

Reset: 0000_0000_0000_0000h. See [2.6.2 \[Instruction Based Sampling \(IBS\)\].](#)

The IBS execution sampling engine is described as follows for IbsOpCntCtl==1. If IbsOpCntCtl==1n then references to “periodic op counter” mean “periodic cycle counter”.

- The periodic op counter is an internal 27-bit counter:
 - It is set to IbsOpCurCnt[26:0] when IbsOpEn is changed from 0 to 1.
 - It increments every dispatched op when IbsOpEn=1 and IbsOpVal=0.
 - The periodic op counter is undefined when IbsOpEn=0 or IbsOpVal=1.
 - When IbsOpCurCnt[26:0] is read then it returns the current value of the periodic micro-op counter [26:0].
- When the periodic micro-op counter reaches IbsOpMaxCnt:
 - The next dispatched micro-op is tagged if IbsOpCntCtl==1. A valid op in the next dispatched line is tagged if IbsOpCntCtl==0. See IbsOpCntCtl.
 - The periodic micro-op counter [26:7]=0; [6:0] is randomized by hardware.
- The periodic micro-op counter is not modified when a tagged micro-op is flushed.
- When a tagged micro-op is retired:
 - IbsOpVal is set to 1.
 - Drivers can't assume that IbsOpCurCnt is 0 when IbsOpVal==1.
 - The status of the operation is written to the IBS execution registers (this register, [MSRC001_1034](#), [MSRC001_1035](#), [MSRC001_1036](#), [MSRC001_1037](#), [MSRC001_1038](#) and [MSRC001_1039](#)).
 - An interrupt is generated as specified by [MSRC001_103A](#). The interrupt service routine associated with this interrupt is responsible for saving the performance information stored in IBS execution registers.

Bits	Description
63:59	Reserved.
58:32	IbsOpCurCnt[26:0]: periodic op counter current count. Read-write; updated-by-hardware. Returns the current value of the periodic op counter.
31:27	Reserved.
26:20	IbsOpMaxCnt[26:20]: periodic op counter maximum count. Read-write. See IbsOpMaxCnt[19:4].
19	IbsOpCntCtl: periodic op counter count control. Read-write. 1=Count dispatched Micro-ops; when a roll-over occurs, the counter is preloaded with a pseudorandom 7 bit value between 1 and 127. 0=Count clock cycles; a 1-of-4 round robin counter selects an op in the next dispatch line; if the op pointed to by the round robin counter is invalid, then the next younger valid op is selected.
18	IbsOpVal: micro-op sample valid. Read-write; set-by-hardware. 1>New instruction execution data available; the periodic op counter is disabled from counting. An interrupt may be generated when this bit is set as specified by MSRC001_103A [LvtOffset].
17	IbsOpEn: micro-op sampling enable. Read-write. 1=Instruction execution sampling enabled.

16	Reserved.						
15:0	<p>IbsOpMaxCnt[19:4]: periodic op counter maximum count. Read-write. IbsOpMaxCnt[26:0] = {IbsOpMaxCnt[26:20], IbsOpMaxCnt[19:4], 0000b}. Specifies maximum count value of the periodic op counter. Bits [3:0] of the maximum count are always 0000b. Must be >=20h</p> <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>001Fh-0000h</td> <td>Reserved</td> </tr> <tr> <td>FFFFh-0020h</td> <td><IbsOpMaxCnt[19:4]*16> Micro-ops</td> </tr> </tbody> </table>	Bits	Description	001Fh-0000h	Reserved	FFFFh-0020h	<IbsOpMaxCnt[19:4]*16> Micro-ops
Bits	Description						
001Fh-0000h	Reserved						
FFFFh-0020h	<IbsOpMaxCnt[19:4]*16> Micro-ops						

MSRC001_1034 IBS Op Logical Address (IbsOpRip)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	IbsOpRip: micro-op linear address. Read-write; updated-by-hardware. Linear address in canonical form for the instruction that contains the tagged micro-op.

MSRC001_1035 IBS Op Data (IbsOpData)

Bits	Description
63:41	Reserved.
40	<p>IbsOpMicrocode. Value: 0. 1=Tagged operation from microcode. Added XV</p>
39	<p>IbsOpBrnFuse: fused branch micro-op. Value: 0. 1=Tagged operation was a fused branch micro-op. Support indicated by CPUID Fn8000_001B_EAX[OpBrnFuse]. Added SR</p>
38	<p>IbsRipInvalid: RIP is invalid. Read-write; updated-by-hardware. Reset: 0. 1=Tagged operation RIP is invalid. Support indicated by CPUID Fn8000_001B_EAX[RipInvalidChk]. Added LN</p>
37	<p>IbsOpBrnRet: branch micro-op retired. Read-write; updated-by-hardware. Reset: 0. 1=Tagged operation was a branch micro-op that retired. Not set for a branch micro-op that is not an ISA-level control transfer instruction.</p>
36	<p>IbsOpBrnMisp: mispredicted branch micro-op. Read-write; updated-by-hardware. Reset: 0. 1=Tagged operation was a branch micro-op that was mispredicted. Qualified by IbsOpBrnRet==1.</p>
35	<p>IbsOpBrnTaken: taken branch micro-op. Read-write; updated-by-hardware. Reset: 0. 1=Tagged operation was a branch micro-op that was taken. Qualified by IbsOpBrnRet==1.</p>
34	<p>IbsOpReturn: return micro-op. Read-write; updated-by-hardware. Reset: 0. 1=Tagged operation was return micro-op. Qualified by (IbsOpBrnRet==1).</p>
33:32	Reserved. Read-write; updated-by-hardware.

31:16	IbsTagToRetCtr: micro-op tag to retire count. Read-write; updated-by-hardware. Reset: 0. This field returns the number of cycles from when the micro-op was tagged to when the micro-op was retired. This field is equal to IbsCompToRetCtr when the tagged micro-op is a NOP.
15:0	IbsCompToRetCtr: micro-op completion to retire count. Read-write; updated-by-hardware. Reset: 0. This field returns the number of cycles from when the micro-op was completed to when the micro-op was retired.

MSRC001_1036 IBS Op Data 2 (IbsOpData2)

Reset: 0000_0000h. **MSRC001_1036**[31:0] is an alias of **D18F3x1D0**. Northbridge data is only valid for load operations that miss both the L1 data cache and the L2 cache. If a load operation crosses a cache line boundary, the data returned in this register is the data for the access to the lower cache line.

Bits	Description																		
63:32	Reserved.																		
31:6	Reserved. Read-write.																		
5	Reserved. Read-write.																		
4	Reserved. Read-write.																		
3	Reserved. Read-write.																		
2:0	NbIbsReqSrc: northbridge IBS request data source. Read-write. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No valid status</td></tr> <tr> <td>1h</td> <td>Reserved</td></tr> <tr> <td>2h</td> <td>Cache: data returned from another compute-unit cache.</td></tr> <tr> <td>3h</td> <td>DRAM: data returned from DRAM</td></tr> <tr> <td>4h</td> <td>Reserved for remote cache</td></tr> <tr> <td>5h</td> <td>Reserved</td></tr> <tr> <td>6h</td> <td>Reserved</td></tr> <tr> <td>7h</td> <td>Other: data returned from MMIO/Config/PCI/APIC</td></tr> </tbody> </table>	Bits	Description	0h	No valid status	1h	Reserved	2h	Cache: data returned from another compute-unit cache.	3h	DRAM: data returned from DRAM	4h	Reserved for remote cache	5h	Reserved	6h	Reserved	7h	Other: data returned from MMIO/Config/PCI/APIC
Bits	Description																		
0h	No valid status																		
1h	Reserved																		
2h	Cache: data returned from another compute-unit cache.																		
3h	DRAM: data returned from DRAM																		
4h	Reserved for remote cache																		
5h	Reserved																		
6h	Reserved																		
7h	Other: data returned from MMIO/Config/PCI/APIC																		

MSRC001_1037 IBS Op Data 3 (IbsOpData3)

Reset: 0000_0000_0000_0000h. If a load or store operation crosses a 128-bit boundary, the data returned in this register is the data for the access to the data below the 128-bit boundary.

Bits	Description
63:48	IbsTlbRefillLat: L1 DTLB refill latency. Read-only. Value: 0. The number of cycles from when a L1 DTLB refill is triggered by a tagged op to when the L1 DTLB fill has been completed.

47:32	IbsDcMissLat: data cache miss latency. Read-write; updated-by-hardware. Indicates the number of clock cycles from when a miss is detected in the data cache to when the data was delivered to the core. The value returned by this counter is not valid for data cache writes or prefetch instructions.																
31:26	IbsOpDcMissOpenMemReqs: outstanding memory requests on DC fill. Read-only. Value: 0. The number of allocated, valid DC MABs when the MAB corresponding to a tagged DC miss op is deallocated. Includes the MAB allocated by the sampled op. 00000b=No information provided.																
25:22	IbsOpMemWidth: load/store size in bytes. Read-only. Value: 0. Report the number of bytes the load or store is attempting to access. <table> <thead> <tr> <th style="text-align: left;">Bits</th> <th style="text-align: left;">Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>No information provided.</td> </tr> <tr> <td>1h</td> <td>Byte</td> </tr> <tr> <td>2h</td> <td>Word</td> </tr> <tr> <td>3h</td> <td>DW</td> </tr> <tr> <td>4h</td> <td>QW</td> </tr> <tr> <td>5h</td> <td>OW</td> </tr> <tr> <td>Fh-6h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Description	0h	No information provided.	1h	Byte	2h	Word	3h	DW	4h	QW	5h	OW	Fh-6h	Reserved
Bits	Description																
0h	No information provided.																
1h	Byte																
2h	Word																
3h	DW																
4h	QW																
5h	OW																
Fh-6h	Reserved																
21	IbsSwPf: software prefetch. Read-only. Value: 0. 1=The op is a software prefetch.																
20	IbsL2Miss: L2 cache miss for the sampled operation. Read-only. Value: 0. 1=The operation missed in the L2, regardless of whether the op initiated the request to the L2.																
19	IbsDcL2TlbHit1G: data cache L2TLB hit in 1G page. Read-only. Value: 0. 1=The physical address for the tagged load or store operation was present in a 1G page table entry in the data cache L2TLB.																
18	IbsDcPhyAddrValid: data cache physical address valid. Read-write; updated-by-hardware. 1=The physical address in MSRC001_1039 is valid for the load or store operation.																
17	IbsDcLinAddrValid: data cache linear address valid. Read-write; updated-by-hardware. 1=The linear address in MSRC001_1038 is valid for the load or store operation.																
16	DcMissNoMabAlloc: DC miss with no MAB allocated. Read-write; updated-by-hardware. 1=The tagged load or store operation hit on an already allocated MAB.																
15	IbsDcLockedOp: locked operation. Read-write; updated-by-hardware. 1=Tagged load or store operation is a locked operation.																
14	IbsDcUcMemAcc: UC memory access. Read-write; updated-by-hardware. 1=Tagged load or store operation accessed uncacheable memory.																
13	IbsDcWcMemAcc: WC memory access. Read-write; updated-by-hardware. 1=Tagged load or store operation accessed write combining memory.																
12	Reserved. Read-write.																
11	IbsDcStToLdFwd: data forwarded from store to load operation. Read-write; updated-by-hardware. 1=Data for tagged load operation was forwarded from a store operation. If this bit is set and Ibs-DcStToLdCan=1, then the data for the load operation forwarded from a store operation but the data was not forwarded immediately.																

10	Reserved. Read-write.
9	Reserved. Read-write; updated-by-hardware.
8	IbsDcMisAcc: misaligned access. Read-write; updated-by-hardware. 1=The tagged load or store operation crosses a 128 bit address boundary.
7	IbsDcMiss: data cache miss. Read-write; updated-by-hardware. 1=The cache line used by the tagged load or store was not present in the data cache.
6	IbsDcL2tlbHit2M: data cache L2TLB hit in 2M page. Read-write; updated-by-hardware. 1=The physical address for the tagged load or store operation was present in a 2M page table entry in the data cache L2TLB.
5	Reserved. Read-write.
4	IbsDcL1TlbHit2M: data cache L1TLB hit in 2M page. Read-write; updated-by-hardware. 1=The physical address for the tagged load or store operation was present in a 2M page table entry in the data cache L1TLB.
3	IbsDcL2TlbMiss: data cache L2TLB miss. Read-write; updated-by-hardware. 1=The physical address for the tagged load or store operation was not present in the data cache L2TLB.
2	IbsDcL1TlbMiss: data cache L1TLB miss. Read-write; updated-by-hardware. 1=The physical address for the tagged load or store operation was not present in the data cache L1TLB.
1	IbsStOp: store op. Read-write; updated-by-hardware. 1=Tagged operation is a store operation.
0	IbsLdOp: load op. Read-write; updated-by-hardware. 1=Tagged operation is a load operation.

MSRC001_1038 IBS DC Linear Address (IbsDcLinAd)

Reset: 0000_0000_0000_0000h.

Bits	Description
63:0	IbsDcLinAd. Read-write; updated-by-hardware. Provides the linear address in canonical form for the tagged load or store operation. This field contains valid data only if MSRC001_1037 [IbsDcLinAddrValid] is asserted.

MSRC001_1039 IBS DC Physical Address (IbsDcPhysAd)

Bits	Description
63:40	RAZ.
39:0	IbsDcPhysAd: load or store physical address. Read-write; updated-by-hardware. Reset: 0. Provides the physical address for the tagged load or store operation. The lower 12 bits are not modified by address translation, so they are always the same as the linear address. This field contains valid data only if MSRC001_1037 [IbsDcPhyAddrValid] is asserted.

MSRC001_103A IBS Control

GP-write.

Bits	Description
63:32	Reserved.
31:9	Reserved.
8	LvtOffsetVal: local vector table offset valid. MSRC001_103A [LvtOffsetVal] is an alias of D18F3x1CC [LvtOffsetVal].
7:4	Reserved.
3:0	LvtOffset: local vector table offset. MSRC001_103A [LvtOffset] is an alias of D18F3x1CC [LvtOffset].

MSRC001_103B IBS Branch Target Address (BP_IBSTGT_RIP)Reset: 0000_0000_0000_0000h. Support for this register indicated by [CPUID Fn8000_001B_EAX](#)[BrnTrgt].

Bits	Description
63:0	IbsBrTarget. Read-write; updated-by-hardware. The logical address in canonical form for the branch target. Contains a valid target if non-0. Qualified by MSRC001_1035 [IbsOpBrnRet]==1.

MSRC001_1090 Processor Feedback Constants 0 (CU_PROCFB_SCALE_0)Read-write. See [2.7.3 \[Frequency Sensitivity\]](#).

Bits	Description
63:32	Reserved.
31:16	Reserved.
15:8	RefCountScale. Reset: Fuse[XCoreLateBits[97:90]]. BIOS: 64h.
7:0	ActualCountScale. Reset: Fuse[XCoreLateBits[105:98]]. BIOS: A5h.

MSRC001_10A0 L2I Configuration (L2I_CFG)

Per-L2.

Bits	Description				
56:45	L2ScrubberInterval: L2 background scrubber interval [11:0]. Read-write. Reset: 0. BIOS: 100h. If (L2ScrubberDis==0), the background error scrubber will wake up and perform one scrub every (N+1)*64 clock CClks. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Scrubber Interval</th> </tr> <tr> <td>FFh-00h</td> <td><L2ScrubberInterval>+1) * 64 CClks</td> </tr> </table>	Bits	Scrubber Interval	FFh-00h	<L2ScrubberInterval>+1) * 64 CClks
Bits	Scrubber Interval				
FFh-00h	<L2ScrubberInterval>+1) * 64 CClks				
44	PbDisobeysThrottleNb: probes disobey NB throttling. Read-write. Reset: 0. BIOS: 1. 1=Probe responses do not obey the ThrottleNbInterface field, but can be sent to the NB on any valid (non-skipped) CClk.				

43:40	<p>ThrottleNbInterface: NB Interface Request Throttling [3:0]. Read-write. Reset: Fh. BIOS: NumOfCompUnitsOnNode-1. If (PbDisObeysThrottleNb==1), Specifies how many clocks the CU needs to wait before sending the next packet of information to the NB. This applies to the CU->NB request interface and the CU->NB probe response interface. This is how many clocks the BU needs to wait before sending the next packet of information to the NB. This applies to the BU->NB request interface and the BU->NB probe response interface.</p> <p>This field must be programmed to a value greater than or equal to the number of L2 complexes in the node that have at least one enabled core minus 1. Rule: MSRC001_10A0[ThrottleNbInterface] >=NumOfCompUnitsOnNode-1. See 2.4.4 [Processor Cores and Downcoreing].</p> <p>If (PbDisObeysThrottleNb==0), probe responses must also obey the same throttling rule.</p> <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 10%;"><u>Bits</u></td><td style="width: 10%; text-align: center;"><u>Throttling Interval</u></td></tr> <tr> <td>Fh-0h</td><td style="text-align: center;"><ThrottleNbInterface>+1 CClks</td></tr> </table>	<u>Bits</u>	<u>Throttling Interval</u>	Fh-0h	<ThrottleNbInterface>+1 CClks
<u>Bits</u>	<u>Throttling Interval</u>				
Fh-0h	<ThrottleNbInterface>+1 CClks				
21	L2ScrubberDis: L2 Scrubber Disable . Read-write. Reset: 0. 1=Do not search for and repair single bit errors in the background.				
20	<p>L2RinserDis: L2 rinser disable. Read-write. Reset: 0.</p> <p>BIOS: 1.</p> <p>1=Disable background copy of dirty lines to the NB. See L2RinserInterval.</p>				
19	<p>McaToMstCoreEn: route machine check events to master Core. Read-write. Reset: 0. BIOS: 1.</p> <p>1=Errors are logged and reported to the L2 complex Master Core, which is the lowest physically numbered core in the L2 complex that is not fused off.</p> <p>When (McaToMstCoreEn==1), an MCE may not be delivered in the following circumstance:</p> <ul style="list-style-type: none"> • An MCE occurs in the L2I when the MCA Master Core is in CC6. • L2I enters XC6 before the MCA Master Core exits CC6. <p>The event that triggered the MCE will still be properly logged in the MCA registers. L2I uncorrected errors also generate a sync flood, therefore the missed MCE should not affect error containment, recovery, or diagnosis. The major impact is when (L2ICfg[FlagMcaCorrErr]==1), in which case a corrected-error MCE (that does not generate a sync flood) may never get delivered.</p> <p>0=Errors are logged and reported to the core whose behavior triggered the error, if that can be determined. If it cannot be determined (e.g. for NB probes) then they are logged and reported to the L2 complex Master Core.</p>				
7	PrefetcherDis . Read-write. Reset: 0. BIOS: See 2.3.3 [Using L2 Cache as General Storage During Boot] . 1=Disable the L2 prefetcher.				
3	CacheIcAttrDis . Read-write. Reset: 0. BIOS: See 2.3.3 [Using L2 Cache as General Storage During Boot] . 1=Disable inserting IC attributes into the L2.				

3.23 Core Performance Counter Events

This section provides the performance counter events that may be selected through [MSRC001_00\[03:00\]\[EventSelect,UnitMask\]](#). See [MSRC001_00\[03:00\]](#) and [MSRC001_00\[07:04\] \[Performance Event Counter \(PERF_CTR\[3:0\]\)\]](#).

For L2I performance counter events see [2.6.1.2 \[L2I Performance Monitor Counters\]](#) and [3.24 \[L2I Performance Counter Events\]](#).

For NB performance counter events see [2.6.1.3 \[NB Performance Monitor Counters\]](#) and [3.25 \[NB Performance Counter Events\]](#).

3.23.1 PMCx0[1F:00] Events (FP)

PMCx000 Dispatched FPU Operations

The number of operations (uops) dispatched to the FPU execution pipelines. This includes all operations done by x87, MMX™ and SSE instructions, including moves. This event is a speculative event. (See PMCx0CB). Since this event includes non-numeric operations it is not suitable for measuring MFLOPs. Pure FP loads do not use an FP execution pipe and are counted with UnitMask 7.

UnitMask	Description
1	Pipe1 dispatches. (Float mul/div/sqrt, store/convert, vec-int add/sub/logical)
0	Pipe0 dispatches. (Float add/sub, vec-int mul, vec-int add/sub/logical)

PMCx001 FP Scheduler Empty

The number of cycles in which the FPU is empty. Invert this ([MSRC001_00\[03:00\]\[Inv\]==1](#)) to count cycles in which at least one FPU operation is present in the FPU.

PMCx002 Dispatched Fast Flag FPU Operations

The number of FPU operations that use the fast flag interface (e.g. FCOMI, COMISS, COMISD, UCOMISS, UCOMISD, MOVD, CVTSD2SI). This event is a speculative event.

PMCx003 Retired SSE/AVX Operations

The number of SSE/AVX operations retired. The number of events logged per cycle can vary from 0 to 8.

UnitMask	Description
7	Reserved.
6	Double precision divide/square root FLOPS.
5	Double precision multiply FLOPS.
4	Double precision add/subtract FLOPS.
3	Reserved.
2	Single-precision divide/square root FLOPS.
1	Single-precision multiply FLOPS.

0	Single-precision add/subtract FLOPS.
---	--------------------------------------

PMCx005 Retired Serializing Ops

The number of serializing uops retired. A bottom-executing uop is not issued until it is the oldest non-retired uop in the FPU. A control-renaming uop requires a rename from a limited pool of control renames.

UnitMask	Description
7:4	Reserved.
3	x87 control-renaming uops retired.
2	x87 bottom-executing uops retired.
1	SSE control-renaming uops retired.
0	SSE bottom-executing uops retired.

PMCx011 Retired x87 Floating Point Operations

The number of x87 floating point ops that have retired.

UnitMask	Description
7:3	Reserved.
2	Divide and fsqrt ops.
1	Multiply ops.
0	Add/subtract ops.

3.23.2 PMCx0[3F:20] Events (LS)**PMCx020 Segment Register Loads**

The number of segment register loads performed.

UnitMask	Description
7	Reserved.
6	HS
5	GS
4	FS
3	DS
2	SS
1	CS
0	ES

PMCx021 Pipeline Restart Due to Self-Modifying Code

The number of pipeline restarts that were caused by self-modifying code (a store that hits any instruction that's been fetched for execution beyond the instruction doing the store).

PMCx022 Pipeline Restart Due to Probe Hit

The number of pipeline restarts caused by invalidating probes that hit load out-of-order with respect to other load.

UnitMask	Description
7:2	Reserved.
1	Restarts due to evictions caused by fills.
0	Restarts due to evictions caused by invalidating probes.

PMCx024 Locked Operations

This event covers locked operations performed and their execution time. The execution time represented by the cycle counts is typically overlapped to a large extent with other instructions. The non-speculative cycles event is suitable for event-based profiling of lock operations that tend to miss in the cache.

UnitMask	Description
7:3	Reserved.
2	The number of cycles to unlock \$line (not including cache miss)
1	The number cycles to acquire bus lock
0	The number of locked instructions executed

PMCx026 Retired CLFLUSH Instructions

The number of CLFLUSH instructions retired.

PMCx027 Retired CPUID Instructions

The number of CPUID instructions retired.

PMCx029 LS Dispatch

Counts the number of transactions dispatched to load-store unit.

UnitMask	Description
7:3	Reserved.
2	Load-op-Stores.
1	Stores.
0	Loads.

PMCx02A Canceled Store to Load Forward Operations

Counts the number of missed store to load forward opportunities which resulted in blocks.

UnitMask	Description
2	Block due to store being misaligned.

1	Block due to store being smaller than the load.
0	Block due to address mismatch (starting byte not the same).

3.23.3 PMCx0[5F:40] Events (DC)

PMCx040 Data Cache Accesses

The number of accesses to the data cache for load and store references. This may include certain microcode scratchpad accesses, although these are generally rare. Each increment represents an eight-byte access, although the instruction may only be accessing a portion of that. This event is a speculative event. This event counts all loads and stores that access the cache, that are not prefetch requests, regardless of hit or miss. You can determine data cache hit by looking at event [PMCx041](#) that is the number of data cache misses. MAB hit is not contained.

PMCx041 Data Cache Misses

The number of data cache references which miss in the data cache and allocate a MAB. This event is a speculative event. This event counts the number of MAB allocations caused by DC misses. This event does not count MAB allocations for state change requests or prefetch requests.

PMCx042 Data Cache Refills from L2 or Northbridge

The number of data cache refills satisfied from the L2 cache (and/or the northbridge), per the UnitMask. This event includes refills for prefetch requests and data returned from state change operations. The UnitMask selects lines in one or more specific coherency states. Each increment reflects a 64-byte transfer. If Unit-Mask[0] is selected it might be less than 64-bytes. This event is a speculative event.

UnitMask	Description
7:5	Reserved.
4	Modified
3	Owned
2	Exclusive
1	Shared
0	Non-cacheable return of data.

PMCx043 Data Cache Refills from the northbridge

The number of L1 cache refills satisfied from the northbridge (DRAM or another processor's cache), as opposed to the L2. The UnitMask selects lines in one or more specific coherency states. Each increment reflects a 64-byte transfer. This event is a speculative event.

UnitMask	Description
7:5	Reserved.
4	Modified
3	Owned
2	Exclusive
1	Shared

0	Non-cacheable read data.
---	--------------------------

PMCx044 Data Cache Lines Evicted

The UnitMask may be used to count only victims in specific coherency states. Each increment represents a 64-byte transfer. Lines brought into the data cache by PrefetchNTA instructions are evicted directly to system memory (if dirty) or invalidated (if clean). This event is a speculative event.

UnitMask	Description
7:5	Reserved.
4	Modified eviction
3	Owned eviction
2	Exclusive eviction
1	Shared eviction
0	Evicted from probe

PMCx045 L1 DTLB Miss and L2 DTLB Hit

The number of data cache accesses that miss in the L1 DTLB and hit in the L2 DTLB. This event is a speculative event.

PMCx046 DTLB Miss

The number of data cache accesses that miss in both the L1 and L2 DTLBs. This event is a speculative event.

UnitMask	Description
7:4	Reserved.
3	Count loads that miss L2TLB.
2	Count stores that miss L2TLB.
1	Count loads that miss L1TLB.
0	Count stores that miss L1TLB.

PMCx047 Misaligned Accesses

The number of data cache accesses that are misaligned. These are accesses which cross the boundary as specified by UnitMask. Misaligned accesses incur at least an extra cache access and an extra cycle of latency on reads. This event is a speculative event.

UnitMask	Description
7:2	Reserved.
1	Number of misaligns that cross a 4kb boundary
0	Number of misaligns that cross a 16-byte boundary

PMCx04B Prefetch Instructions Dispatched

The number of prefetch instructions dispatched by the decoder. Such instructions may or may not cause a cache

line transfer. All Dcache and L2 accesses, hits and misses by prefetch instructions, except for prefetch instructions that collide with an outstanding hardware prefetch, are included in these events. This event is a speculative event.

UnitMask	Description
7:3	Reserved.
2	NTA (PrefetchNTA)
1	Store (PrefetchW)
0	Load (Prefetch, PrefetchT0/T1/T2)

PMCx04C DCACHE Misses by Locked Instructions

The number of cacheable locked operations that miss in the data cache. Cacheable locks are defined as locks that hit write back memory space and are not misaligned.

PMCx04D L1 DTLB Hit

The number of data cache accesses that hit in the L1 DTLB. This event is a speculative event.

UnitMask	Description
7:2	Reserved.
1	L1 2M TLB hit
0	L1 4K TLB hit

PMCx052 Ineffective Software Prefetches

The number of software prefetches that do not cause an actual data cache refill. The unit mask may be used to determine the specific cause.

UnitMask	Description
7:4	Reserved.
3	SW Prefetch hit in L2.
2	SW prefetches that don't get a MAB and don't cause PMCx052[1,0] .
1	Software prefetch hit a pending fill.
0	Software prefetch hit in the data cache.

PMCx054 Global Page Invalidations

This event counts TLB flushes that flush TLB entries that have the global bit set.

3.23.4 PMCx[8,1:0][7F:60] Events (BU)

PMCx062 Command Related to Read Block Operations

UnitMask	Description
7	Reserved.

6	Read Block Speculative Shared.
5	RdBlkSpecMod.
4	RdBlkSpec.
3	Reserved.
2	Read Block Shared.
1	RdBlkMod.
0	Read Block.

PMCx063 Command Related to Change to Dirty Operations

UnitMask	Description
7:5	Reserved.
4	Change to Dirty.
3:0	Reserved.

PMCx065 Memory Requests by Type

These events reflect accesses to memory of each region type (as defined by MTRR or PAT settings). Unit-Mask[1] and UnitMask[7] reflect full 64 byte writes or full or partial 32 byte writes.

UnitMask	Description
7	Streaming store (SS) requests.
1	Request to write-combining (WC) memory.
0	Requests to non-cacheable (UC) memory.

PMCx067 Data Cache Prefetches

UnitMask	Description
7:4	Reserved.
3	Prefetch hits on MAB.
2	Reserved.
1	Prefetch attempts.
0	Reserved.

PMCx068 MAB Requests

These events reflect utilization of the Miss Address Buffers (MABs), which handle L1 cache misses. The UnitMask is an encoded value which selects one of the IC or DC miss buffers. EventSelect 68h counts the number of misses handled by the selected MAB; EventSelect 69h counts the number of cycles the selected MAB is busy waiting for the refill response.

When used together, these two events provide a measure of the average refill latency seen by the selected MAB, which is the number of cycles spent waiting (EventSelect 69h) divided by the number of requests (EventSelect 68h). This calculation gives the most direct indication of average system latency for Dcache and Icache refills, respectively. For other entries this value typically includes queuing delays caused by resource contention with prior refills.

UnitMask	Description
7:0	BufferN. where N = 00h to 0Ch. <u>Bits</u> <u>Definition</u> 07h-00h DC miss buffers 0 to 7 0Ah-08h IC miss buffers 0 to 2 0Bh Any DC miss buffer 0Ch Any IC miss buffer FFh-0Dh Reserved

PMCx069 MAB Wait Cycles

See [PMCx068](#).

UnitMask	Description
7:0	BufferID. See: PMCx068 [BufferN].

PMCx06C System Response by Coherence State

The number of responses from the L2I for cache refill requests. The UnitMask may be used to select specific cache coherency states. Each of {Exclusive, Modified, Shared} represents one 64-byte cache line transferred from the L2I (DRAM, L2 cache, or the L1 cache of another core) to the data cache or instruction cache.

- Modified responses may be for Dcache store miss refills, PrefetchW software prefetches, or Change-to-Dirty requests that get a dirty probe hit in another cache.
- Exclusive responses may be for:
 - Dcache load miss refill.
 - Software prefetches.
- Shared responses may be for:
 - Icache refill.
 - Any request that hits a clean line in another cache.
- Change-to-Dirty success response is for a Dcache upgrade request (store hit to a shared line).
- Uncacheable response is for all uncacheable system requests.

UnitMask	Description
7	Reserved.

6	Uncacheable.
5	Change-to-Dirty success.
4	Data Error.
3	Owned.
2	Shared.
1	Modified.
0	Exclusive.

PMCx06D Data Written to System

The number of 16-byte data transfers from the processor to the system. Note that a dirty cache line writeback would cause four increments. An IO write would cause two increments: one for the mask and one for the data.

UnitMask	Description
7:6	Reserved.
5	Data for Write Combine context flush.
4	Byte Enable Mask for Write Combine context flush.
3	Data for uncacheable or IO store.
2	Byte Enable Mask for uncacheable or IO store.
1	Instruction attribute evictions.
0	Data line evictions.

PMCx075 Cache Cross-invalidates

These reflect internal probes for Icache or Dcache misses that hit in the Dcache or Icache, causing the line to be invalidated. These may result from code modification, data being located too close to code, or virtual address aliasing. The aliasing cases arise when a physical memory location is referenced via two or more virtual addresses which differ in bits 14:12. Such aliasing cases are generally uncommon.

UnitMask	Description
7	Reserved.
6	DC probe rejected late.
5	DC probe rejected early.
4	IC hits DC Clean Line (reading code).
3	IC Invalidates DC Dirty Line (execution of recently modified code, or modified data too close to code).
2	IC Invalidates IC (aliasing).
1	DC Invalidates DC (CD or WBINVD).
0	DC Invalidates IC (modification of cached instructions, or of data located too close to code).

PMCx076 CPU Clocks not Halted

The number of clocks that the CPU is not in a halted state (due to STPCLK or a HLT instruction). Note: this

event allows system idle time to be automatically factored out from IPC (or CPI) measurements, providing the OS halts the CPU when going idle. If the OS goes into an idle loop rather than halting, such calculations are influenced by the IPC of the idle loop.

PMCx07D: Reserved. See [L2IPMCx07D \[Requests to L2 Cache\]](#).

PMCx07E: Reserved. See [L2IPMCx07E \[L2 Cache Misses\]](#).

PMCx07F: Reserved. See [L2IPMCx07F \[L2 Fill/Writeback\]](#).

PMCx162 PDC Miss

Counts the number of PDC miss events specified by the UnitMask.

UnitMask	Description
7	Reserved.
6	Guest: PML4E Level.
5	Guest: PDPE Level.
4	Guest: PDE Level.
3	Reserved.
2	Host: PML4E Level.
1	Host: PDPE Level.
0	Host: PDE Level.

3.23.5 PMCx[1:0][9F:80] Events (IC)

Note: All instruction cache events are speculative events unless specified otherwise.

PMCx080 Instruction Cache Fetches

The number of successful instruction cache accesses by the instruction fetcher that result in data being sent to the decoder. Each access is an aligned 32 byte read, from which a varying number of instructions may be decoded.

PMCx081 Instruction Cache Misses

The number of instruction fetches and prefetch requests that miss in the instruction cache. This is typically equal to or very close to the sum of events 82h and 83h. Each miss results in a 64-byte cache line refill.

PMCx082 Instruction Cache Refills from L2

The number of instruction cache refills satisfied from the L2 cache. Each increment represents one 64-byte cache line transfer.

PMCx083 Instruction Cache Refills from System

The number of instruction cache refills from system memory (or another cache). Each increment represents one 64-byte cache line transfer.

PMCx084 L1 ITLB Miss, L2 ITLB Hit

The number of instruction fetches that miss in the L1 ITLB but hit in the L2 ITLB.

PMCx085 ITLB Miss

The number of instruction fetches that miss in the 4K ITLB and 2M ITLB.

UnitMask	Description
7:2	Reserved.
1	Instruction fetches to a 2M page.
0	Instruction fetches to a 4K page.

PMCx087 Instruction Fetch Stall

The number of cycles the instruction fetcher is stalled. This may be for a variety of reasons such as branch predictor updates, unconditional branch bubbles, far jumps and cache misses, among others. May be overlapped by instruction dispatch stalls or instruction execution, such that these stalls don't necessarily impact performance.

PMCx088 Return Stack Hits

The number of near return instructions (RET or RET Iw) that get their return address from the return address stack (i.e. where the stack has not gone empty). This may include cases where the address is incorrect (return mispredicts). This may also include speculatively executed false-path returns. Return mispredicts are typically caused by the return address stack underflowing, however they may also be caused by an imbalance in calls vs. returns, such as doing a call but then popping the return address off the stack.

This event cannot be reliably compared with events C9h and CAh (such as to calculate percentage of return mispredicts due to an empty return address stack), since it may include speculatively executed false-path returns that are not included in those retire-time events.

PMCx089 Return Stack Overflows

The number of (near) call instructions that cause the return address stack to overflow. When this happens, the oldest entry is discarded. This count may include speculatively executed calls.

PMCx08B Instruction Cache Victims

The number of cachelines evicted from the instruction cache to the L2.

PMCx08C Instruction Cache Lines Invalidated

The number of instruction cache lines invalidated.

UnitMask	Description
7:2	Reserved.
1	IC invalidate due to a BU probe.

0	IC invalidate due to an LS probe.
---	-----------------------------------

PMCx099 ITLB Reloads

The number of ITLB reload requests.

PMCx09A ITLB Reloads Aborted

The number of ITLB reloads aborted.

PMCx19A Retired Indirect Branch Info

UnitMask	Description
7:2	Reserved.
1	Retired Mispredicted Indirect Branch Instruction. Retired Mispredicted Near Unconditional jump with target specified in Register or Memory. This event is non-speculative.
0	Retired Indirect branch Instruction. Retired Near Unconditional jump with target specified in Register or Memory. This event is non-speculative.

3.23.6 PMCx[1,0][DF:C0] Events (EX, DE)**PMCx0C0 Retired Instructions**

The number of instructions retired (execution completed and architectural state updated). This count includes exceptions and interrupts - each exception or interrupt is counted as one instruction.

PMCx0C1 Retired uops

The number of micro-ops retired. This includes all processor activity (instructions, exceptions, interrupts, microcode assists, etc.).

PMCx0C2 Retired Branch Instructions

The number of branch instructions retired. This includes all types of architectural control flow changes, including exceptions and interrupts.

PMCx0C3 Retired Mispredicted Branch Instructions

The number of branch instructions retired, of any type, that were not correctly predicted in either target or direction. This includes those for which prediction is not attempted (far control transfers, exceptions and interrupts), and excludes resyncs.

PMCx0C4 Retired Taken Branch Instructions

The number of taken branches that were retired. This includes all types of architectural control flow changes, including exceptions and interrupts, and excludes resyncs.

PMCx0C5 Retired Taken Branch Instructions Mispredicted

The number of retired taken branch instructions that were mispredicted, and excludes resyncs.

PMCx0C6 Retired Far Control Transfers

The number of far control transfers retired including far call/jump/return, IRET, SYSCALL and SYSRET, plus exceptions and interrupts, and excludes resyncs. Far control transfers are not subject to branch prediction.

PMCx0C7 Retired Branch Resyncs

The number of resync branches. These reflect pipeline restarts due to certain microcode assists and events such as writes to the active instruction stream, among other things. Each occurrence reflects a restart penalty similar to a branch mispredict. This is relatively rare.

PMCx0C8 Retired Near Returns

The number of near return instructions (RET or RET Iw) retired.

PMCx0C9 Retired Near Returns Mispredicted

A near return instruction was retired that mispredicted in either target or direction.

PMCx0CA Retired Mispredicted Taken Branch Instructions due to Target Mismatch

A taken branch instruction was retired that mispredicted in target address (but not in direction).

PMCx0CB Retired MMX/FP Instructions

A floating point (x87, MMX, or SSE) instruction was retired. The UnitMask allows the distinction between x87/MMX and SSE instructions. Since this event includes non-numeric instructions it is not suitable for measuring MFLOPS.

UnitMask	Description
7:2	Reserved.
1	SSE floating point instruction was retired (SSE, SSE2, SSE3, MNI)
0	x87 or MMX™ instruction was retired

PMCx0CD Interrupts-Masked Cycles

The number of processor cycles where interrupts are masked (EFLAGS.IF = 0). Using edge-counting with this event gives the number of times IF is cleared; dividing the cycle-count value by this value gives the average length of time that interrupts are disabled on each instance. Compare the edge count with [PMCx0CF](#) to determine how often interrupts are disabled for interrupt handling vs. other reasons (e.g. critical sections).

PMCx0CE Interrupts-Masked Cycles with Interrupt Pending

The number of processor cycles where interrupts are masked (EFLAGS.IF = 0) and an interrupt is pending.

Using edge-counting with this event and comparing the resulting count with the edge count for **PMCx0CD** gives the proportion of interrupts for which handling is delayed due to prior interrupts being serviced, critical sections, etc. The cycle count value gives the total amount of time for such delays. The cycle count divided by the edge count gives the average length of each such delay.

PMCx0CF Interrupts Taken

The number of hardware interrupts taken. This does not include software interrupts (INT n instruction).

PMCx0DB FPU Exceptions

The number of floating point unit exceptions for microcode assists. The UnitMask may be used to isolate specific types of exceptions.

UnitMask	Description
7:4	Reserved.
3	SSE and x87 microtraps
2	SSE reclass microfaults
1	SSE retype microfaults
0	x87 reclass microfaults

PMCx0D[F:C] DR[3:0] Breakpoint Matches

Table 229: Register Mapping for PMCx0D[F:C]

Register	Function
PMCx0DC	DR0
PMCx0DD	DR1
PMCx0DE	DR2
PMCx0DF	DR3

The number of matches on the address in breakpoint register DR0, per the breakpoint type specified in DR7. The breakpoint does not have to be enabled. Each instruction breakpoint match incurs an overhead of about 120 cycles; load/store breakpoint matches do not incur any overhead.

PMCx1CF Tagged IBS Ops

Number of ops tagged by IBS.

PMCx1D0 Tagged IBS Ops Retired

The number of retired tagged IBS operations.

3.24 L2I Performance Counter Events

L2IPMCx060 Command Related to Victim Buffers

UnitMask	Description
7	Lock.
6:5	Reserved.
4	ClVicBlk: clean victim command.
3	WrVicBlkNR: write victim block non-rinsing.
2	WrVicBlkR: write victim block rinsing.
1:0	Reserved.

L2IPMCx061 Command Related to Masked Operations

Count Masked Byte and DW reads and writes to the NB. Byte sized read and write commands can request the transfer of up to 32 bytes. DW sized read and write commands can request the transfer of up to 32 DW's. Combining of the WC memory type can cause 1 B/DW write to represent multiple stores.

UnitMask	Description
7:6	Reserved.
5	WrDWord: write double-word.
4	WrByte: write byte.
3	Reserved.
2	RdDWord: read double-word.
1	Reserved.
0	RdByte: read-byte.

L2IPMCx062 Command Related to Read Block Operations

UnitMask	Description
7:3	Reserved.
2	RdBlkS: read block shared.
1	RdBlkM: read block modified.
0	RdBlk: read block.

L2IPMCx063 Command Related to Change to Dirty Operations

UnitMask	Description
7:5	Reserved.
4	ChgToDirty: change to dirty.
3:0	Reserved.

L2IPMCx06C Response From System on Cache Refills

The number of responses from the system for cache refill requests. The UnitMask may be used to select specific cache coherency states. Each increment represents one 64 B cache line transferred from the system (DRAM or another cache, including another core on the same node) to the data cache, instruction cache or L2 cache (for data prefetcher and TLB table walks). Modified-state responses may be for Dcache store miss refills, PrefetchW software prefetches, hardware prefetches for a store-miss stream, or Change-to-Dirty requests that get a dirty (Owned) probe hit in another cache. Exclusive responses may be for any Icache refill, Dcache load miss refill, other software prefetches, hardware prefetches for a load-miss stream, or TLB table walks that miss in the L2 cache; Shared responses may be for any of those that hit a clean line in another cache.

UnitMask	Description
7	Reserved.
6	Uncacheable.
5	ChgToDirtySuccess.
4	DataError.
3	Owned.
2	Shared.
1	Modified.
0	Exclusive.

L2IPMCx07D Requests to L2 Cache

UnitMask	Description
7	Reserved.
6	PrefReq. L2 cache prefetcher request.
5:4	Reserved.
3	NbPrbReq. NB probe request.
2	Reserved.
1	DcFill. DC fill.
0	IcFill. IC fill.

L2IPMCx07E L2 Cache Misses

The number of requests that miss in the L2 cache. This may include some amount of speculative activity. The IC-fill-miss and DC-fill-miss events tend to mirror the Icache and Dcache refill-from-system [PMCx083](#) and [PMCx043](#), and tend to include more speculative activity than those events.

UnitMask	Description
7:5	Reserved.
4	L2PrefReq. L2 Cache Prefetcher request
3:2	Reserved.
1	DcFill.
0	IcFill.

L2IPMCx07F L2 Fill/Writeback

UnitMask	Description
7:3	Reserved.
2	L2CleanWritebacks . L2 Clean Writebacks to system.
1	L2Writebacks . L2 Writebacks to system (Clean and Dirty).
0	L2Fills . L2 fills from system. Note: Fills for non-temporal software prefetch and WP-memtype fills also are counted in this event even though they don't get cached in L2.

3.25 NB Performance Counter Events

This section provides the performance counter events that may be selected through [MSRC001_024\[6,4,2,0\]\[EventSelect,UnitMask\]](#). See that register and [MSRC001_024\[7,5,3,1\] \[Northbridge Performance Event Counter \(NB_PERF_CTR\[3:0\]\)\]](#).

3.25.1 PMCx0E[7:4] Events (Memory Controller)**NBPMCx0E4 Memory Controller Bypass Counter Saturation and DCQ Occupancy**

UnitMask	Description																		
5	DCQ Bypass Saturated. The DCT is selected by the field NBPMCx0E4[4:2].																		
4:2	Select DCQ bypass: <table> <thead> <tr> <th>Bits</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Select DCT0 DCQ bypass</td> </tr> <tr> <td>001b</td> <td>Select DCT1 DCQ bypass</td> </tr> <tr> <td>010b</td> <td>Select DCT2 DCQ bypass</td> </tr> <tr> <td>011b</td> <td>Select DCT3 DCQ bypass</td> </tr> <tr> <td>100b</td> <td>Select DCT4 DCQ bypass</td> </tr> <tr> <td>101b</td> <td>Select DCT5 DCQ bypass</td> </tr> <tr> <td>110b</td> <td>Select DCT6 DCQ bypass</td> </tr> <tr> <td>111b</td> <td>Select DCT7 DCQ bypass</td> </tr> </tbody> </table>	Bits	Description	000b	Select DCT0 DCQ bypass	001b	Select DCT1 DCQ bypass	010b	Select DCT2 DCQ bypass	011b	Select DCT3 DCQ bypass	100b	Select DCT4 DCQ bypass	101b	Select DCT5 DCQ bypass	110b	Select DCT6 DCQ bypass	111b	Select DCT7 DCQ bypass
Bits	Description																		
000b	Select DCT0 DCQ bypass																		
001b	Select DCT1 DCQ bypass																		
010b	Select DCT2 DCQ bypass																		
011b	Select DCT3 DCQ bypass																		
100b	Select DCT4 DCQ bypass																		
101b	Select DCT5 DCQ bypass																		
110b	Select DCT6 DCQ bypass																		
111b	Select DCT7 DCQ bypass																		
1	Memory controller medium priority bypass (Tracks how often a low priority transaction bypasses a medium priority transaction.)																		
0	Memory controller high priority bypass (Tracks how often a medium or low priority transaction bypasses a high priority transaction.)																		

3.25.2 PMCx0E[F:8] Events (Crossbar)**NBPMCx0E8 Thermal Status**

UnitMask	Description
7	Reserved
6	Number of clocks HTC P-state is active
5	Number of clocks HTC P-state is inactive

4	Reserved. Deprecated STC trip point is crossed.
3	Reserved. Deprecated STC trip point active.
2	Number of times the HTC trip point is crossed

NBPMCx0E9 CPU/IO Requests to Memory/IO

These events reflect request flow between units and nodes, as selected by the UnitMask. The UnitMask is divided into two fields: request type (CPU or IO access to IO or Memory) and source/target location (local vs. remote). One or more requests types must be enabled via bits 3:0, and at least one source and one target location must be selected via bits 7:4. Each event reflects a request of the selected type(s) going from the selected source(s) to the selected target(s).

Not all possible paths are supported. The following table shows the UnitMask values that are valid for each request type:

Source/Target	CPU to Mem	CPU to IO	IO to Mem	IO to IO
Local -> Local	A8h	A4h	A2h	A1h
Local -> Remote	98h	94h	92h	91h
Remote -> Local	-	64h	-	61h
Remote -> Remote	-	-	-	-

Any of the mask values shown may be logically ORed to combine the events. For instance, local CPU requests to both local and remote nodes would be A8h | 98h = B8h. Any CPU to any IO would be A4h | 94h | 64h = F4h (but remote CPU to remote IO requests would not be included).

Note: It is not possible to tell from these events how much data is going in which direction, as there is no distinction between reads and writes. Also, particularly for IO, the requests may be for varying amounts of data, anywhere from one to sixty-four bytes. [NBPMCx0E5](#) provides an indication of 32- and 64-byte read and write transfers for such requests (although from the target point of view). For a direct measure of the amount and direction of data flowing between nodes, use events F6h, F7h and F8h.

UnitMask	Description
7	From local node
6	From remote node
5	To local node
4	To remote node
3	CPU to Mem
2	CPU to IO
1	IO to Mem
0	IO to IO

NBPMCx0EA Cache Block Commands

The number of requests made to the system for cache line transfers or coherency state changes, by request type. Each increment represents one cache line transfer, except for Change-to-Dirty. If a Change-to-Dirty request hits on a line in another processor's cache that's in the Owned state, it causes a cache line transfer, otherwise

there is no data transfer associated with Change-to-Dirty requests.

UnitMask	Description
7:6	Reserved.
5	Change-to-Dirty (first store to clean block already in cache)
4	Read Block Modified (Dcache store miss refill)
3	Read Block Shared (Icache refill)
2	Read Block (Dcache load miss refill)
1	Reserved.
0	Victim Block (Writeback)

NBPMCx0EB Sized Commands

The number of Sized Read/Write commands handled by the System Request Interface (local processor and hostbridge interface to the system). These commands may originate from the processor or hostbridge. Typical uses of the various Sized Read/Write commands are given in the UnitMask table. See [NBPMCx0E5](#), which covers commonly-used block sizes for these requests, and [NBPMCx0EC](#), which provides a separate measure of Hostbridge accesses.

UnitMask	Description
7:6	Reserved.
5	SzRd DW (1-16 DWORDs). Typical Usage: Block-oriented DMA reads, typically cache-line size.
4	SzRd Byte (4 bytes). Typical Usage: Legacy or mapped IO.
3	Posted SzWr DW (1-16 DWORDs). Typical Usage: Block-oriented DMA writes, often cache-line sized; also processor Write Combining buffer flushes.
2	Posted SzWr Byte (1-32 bytes). Typical Usage: Sub-cache-line DMA writes, size varies; also flushes of partially-filled Write Combining buffer.
1	Non-Posted SzWr DW (1-16 DWORDs). Typical Usage: Legacy or mapped IO, typically 1 DWORD.
0	Non-Posted SzWr Byte (1-32 bytes). Typical Usage: Legacy or mapped IO, typically 1-4 bytes.

NBPMCx0EC Probe Responses and Upstream Requests

This covers two unrelated sets of events: cache probe results, and requests received by the hostbridge from devices on non-coherent links.

Probe results: These events reflect the results of probes sent from a memory controller to local caches. They provide an indication of the degree data and code is shared between processors (or moved between processors due to process migration). The dirty-hit events indicate the transfer of a 64-byte cache line to the requestor (for a read or cache refill) or the target memory (for a write). The system bandwidth used by these, in terms of bytes per unit of time, may be calculated as 64 times the event count, divided by the elapsed time. Sized writes to memory that cover a full cache line do not incur this cache line transfer -- they simply invalidate the line and are reported as clean hits. Cache line transfers occur for Change2Dirty requests that hit cache lines in the Owned state. (Such cache lines are counted as Modified-state refills for [PMCx06C](#), System Read Responses.)

Upstream requests: The upstream read and write events reflect requests originating from a device on a local IO link. The two read events allow display refresh traffic in a UMA system to be measured separately from

other DMA activity. Display refresh traffic is typically dominated by 64-byte transfers. Non-display-related DMA accesses may be anywhere from 1 to 64 bytes in size, but may be dominated by a particular size such as 32 or 64 bytes, depending on the nature of the devices. [NBPMCx0E5](#) can provide a measure of 32- and 64-byte accesses by the hostbridge (possibly combined with write combining buffer flush activity from the processor, although that can be factored out via [NBPMCx0E5](#)).

UnitMask	Description
7	Upstream non-ISOC writes
6	Upstream ISOC writes
5	Upstream non-display refresh reads
4	Upstream display refresh/ISOC reads
3	Probe hit dirty with memory cancel (probed by DMA read or cache refill request)
2	Probe hit dirty without memory cancel (probed by Sized Write or Change2Dirty)
1	Probe hit clean
0	Probe miss

3.25.3 PMCx0F[F:0] Events (ONION, Crossbar)

3.25.4 NBPMCx1E[F:0] Events (Crossbar)

NBPMCx1E0 CPU to DRAM Requests to Target Node

This event counts all DRAM reads and writes generated by cores on the local node to the targeted node in the coherent fabric. This counter can be used to observe processor data affinity in NUMA aware operating systems.

UnitMask	Description
7	From Local node to Node 7
6	From Local node to Node 6
5	From Local node to Node 5
4	From Local node to Node 4
3	From Local node to Node 3
2	From Local node to Node 2
1	From Local node to Node 1
0	From Local node to Node 0

NBPMCx1E1 IO to DRAM Requests to Target Node

This event counts all DRAM reads and writes generated by IO devices attached to the IO links of the local node the targeted node in the coherent fabric. This counter can be used to observe IO device data affinity in NUMA aware operating systems.

UnitMask	Description
7	From Local node to Node 7
6	From Local node to Node 6

5	From Local node to Node 5
4	From Local node to Node 4
3	From Local node to Node 3
2	From Local node to Node 2
1	From Local node to Node 1
0	From Local node to Node 0

NBPMCx1E2 CPU Read Command Latency to Target Node 0-3

This event counts the number of NB clocks from when the targeted command is received in the NB to when the targeted command completes. This event only tracks one outstanding command at a time. To determine latency between the local node and a remote node set UnitMask[7:4] to select the node and UnitMask[3:0] to select the read command type. The count returned by the counter should be divided by the count returned by [NBPMCx1E3](#) do determine the average latency for the command type.

UnitMask	Description
7	From Local node to Node 3
6	From Local node to Node 2
5	From Local node to Node 1
4	From Local node to Node 0
3	Change-to-Dirty
2	Read block modified
1	Read block shared
0	Read block

NBPMCx1E3 CPU Read Command Requests to Target Node 0-3

This event counts the number of requests that a latency measurement is made for using [NBPMCx1E2](#). To determine the number of commands that a latency measurement are made for between the local node and a remote node set UnitMask[7:4] to select the node and UnitMask[3:0] to select the read command type.

UnitMask	Description
7	From Local node to Node 3
6	From Local node to Node 2
5	From Local node to Node 1
4	From Local node to Node 0
3	Change-to-Dirty
2	Read block modified
1	Read block shared
0	Read block

NBPMCx1E4 CPU Read Command Latency to Target Node 4-7

This event counts the number of NB clocks from when the targeted command is received in the NB to when the

targeted command completes. This event only tracks one outstanding command at a time. To determine latency between the local node and a remote node set UnitMask[7:4] to select the node and UnitMask[3:0] to select the read command type. The count returned by the counter should be divided by the count returned by [NBPMCx1E5](#) do determine the average latency for the command type.

UnitMask	Description
7	From Local node to Node 7
6	From Local node to Node 6
5	From Local node to Node 5
4	From Local node to Node 4
3	Change-to-Dirty
2	Read block modified
1	Read block shared
0	Read block

NBPMCx1E5 CPU Read Command Requests to Target Node 4-7

This event counts the number of requests that a latency measurement is made for using [NBPMCx1E4](#). To determine the number of commands that a latency measurement are made for between the local node and a remote node set UnitMask[7:4] to select the node and UnitMask[3:0] to select the read command type.

UnitMask	Description
7	From Local node to Node 7
6	From Local node to Node 6
5	From Local node to Node 5
4	From Local node to Node 4
3	Change-to-Dirty
2	Read block modified
1	Read block shared
0	Read block

NBPMCx1E6 CPU Command Latency to Target Node 0-3/4-7

This event counts the number of NB clocks from when the targeted command is received in the NB to when the targeted command completes. This event only tracks one outstanding command at a time. To determine latency between the local node and a remote node set UnitMask[7:4] to select the node, UnitMask[3] to select the node group and UnitMask[3:0] to select the command type. The count returned by the counter should be divided by the count returned by [NBPMCx1E7](#) do determine the average latency for the command type.

UnitMask	Description
7	From Local node to Node 3/7
6	From Local node to Node 2/6
5	From Local node to Node 1/5
4	From Local node to Node 0/4

3	Node Group Select. 0=Nodes 0-3. 1= Nodes 4-7.
2	Victim Block
1	Write Sized
0	Read Sized

NBPMCx1E7 CPU Requests to Target Node 0-3/4-7

This event counts the number of requests that a latency measurement is made for using [NBPMCx1E6](#). To determine the number of commands that a latency measurement are made for between the local node and a remote node set UnitMask[7:4] to select the node, UnitMask[3] to select the node group and UnitMask[3:0] to select the command type.

UnitMask	Description
7	From Local node to Node 3/7
6	From Local node to Node 2/6
5	From Local node to Node 1/5
4	From Local node to Node 0/4
3	Node Group Select. 0=Nodes 0-3. 1= Nodes 4-7.
2	Victim Block
1	Write Sized
0	Read Sized

NBPMCx1EB Request Cache Status 1

The probe response type for RdBlkM or ChgToDirty request type.

UnitMask	Description
7	Track Cache Stat for RdBlkM
6	Track Cache Stat for ChgToDirty
5	Directed Probe
4	Probe Miss
3	Probe Hit M
2	Probe Hit MuW or O
1	Probe Hit E
0	Probe Hit S

3.25.5 NBPMCx1F[F:0] Events (Memory Controller, Crossbar)

NBPMCx1F0 Memory Controller Requests

Read/Write requests: The read/write request events reflect the total number of commands sent to the DRAM controller.

Sized Read/Write activity: The Sized Read/Write events reflect 32- or 64-byte transfers (as opposed to other sizes which could be anywhere between 1 and 64 bytes), from either the processor or the Hostbridge (on any node in an MP system). Such accesses from the processor would be due only to write combining buffer flushes,

where 32-byte accesses would reflect flushes of partially-filled buffers. [PMCx065](#) provides a count of sized write requests associated with WC buffer flushes; comparing that with counts for these events (providing there is very little Hostbridge activity at the same time) gives an indication of how efficiently the write combining buffers are being used. [PMCx065](#) may also be useful in factoring out WC flushes when comparing these events with the Upstream Requests component of [PMCx06C](#).

UnitMask	Description
7	Read requests sent to the DCT while writes requests are pending in the DCT
6	64 Byte Sized Reads
5	32 Bytes Sized Reads
4	64 Bytes Sized Writes
3	32 Bytes Sized Writes
2	Prefetch requests sent to the DCT
1	Read requests (including prefetch requests) sent to the DCT
0	Write requests sent to the DCT

NBPMCx3EC DRAM Accesses

The number of memory accesses performed by the local DRAM controller. UnitMask[7:0] may be used to isolate the different DRAM page access cases. Page miss cases incur an extra latency to open a page; page conflict cases incur both a page-close as well as page-open penalties. These penalties may be overlapped by DRAM accesses for other requests and don't necessarily represent lost DRAM bandwidth. The associated penalties are as follows:

Page miss: Trcd (DRAM RAS-to-CAS delay)

Page conflict: Trp + Trcd (DRAM row-precharge time plus RAS-to-CAS delay)

Each DRAM access represents one 64-byte block of data transferred if the DRAM is configured for 64-byte granularity, or one 32-byte block if the DRAM is configured for 32-byte granularity. (The latter is only applicable to single-channel DRAM systems, which may be configured either way.)

UnitMask	Description
7:6	Reserved.
5	DCT1 Page Conflict
4	DCT1 Page Miss
3	DCT1 Page hit
2	DCT0 Page Conflict
1	DCT0 Page Miss
0	DCT0 Page hit

NBPMCx3ED DRAM Controller Page Table Overflows

The number of page table overflows in the local DRAM controller. This table maintains information about which DRAM pages are open. An overflow occurs when a request for a new page arrives when the maximum number of pages are already open. Each occurrence reflects an access latency penalty equivalent to a page con-

flict.

UnitMask	Description
1	DCT1 Page Table Overflow
0	DCT0 Page Table Overflow

NBPMCx3EE Memory Controller DRAM Command Slots Missed

UnitMask	Description
1	DCT1 Command Slots Missed (in MEMCLKs)
0	DCT0 Command Slots Missed (in MEMCLKs)

NBPMCx3EF Memory Controller Turnarounds

The number of turnarounds on the local DRAM data bus. UnitMask[7:0] may be used to isolate the different cases. These represent lost DRAM bandwidth, which may be calculated as follows (in bytes per occurrence):

DIMM turnaround: DRAM_width_in_bytes * 2 edges_per_memclk * 2

R/W turnaround: DRAM_width_in_bytes * 2 edges_per_memclk * 1

R/W turnaround: DRAM_width_in_bytes * 2 edges_per_memclk * (Tcl-1)

where DRAM_width_in_bytes is 8 or 16 (for single- or dual-channel systems), and Tcl is the CAS latency of the DRAM in memory system clock cycles (where the memory clock for DDR-400, or PC3200 DIMMS, for example, would be 200 MHz).

UnitMask	Description
5	DCT1 Write to read turnaround
4	DCT1 Read to write turnaround
3	DCT1 DIMM (chip select) turnaround
2	DCT0 Write to read turnaround
1	DCT0 Read to write turnaround
0	DCT0 DIMM (chip select) turnaround

3.26 Fusion Controller Hub Registers

3.26.1 Legacy Block Configuration Registers (IO)

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention.

IO000 Dma_Ch 0

Bits	Description
15:0	DmaCh0. Read-write. Reset: 0. DMA1 channel 0 base and current address.

IO002 Dma_Ch 1

Bits	Description
15:0	DmaCh1. Read-write. Reset: 0. DMA1 channel 1 base and current address.

IO004 Dma_Ch 2

Bits	Description
15:0	DmaCh2. Read-write. Reset: 0. DMA1 channel 2 base and current address.

IO006 Dma_Ch 3

Bits	Description
15:0	DmaCh3. Read-write. Reset: 0. DMA1 channel 3 base and current address.

IO008 Dma_Status

Bits	Description
7:0	DmaStatus. Read-write. Reset: 0. Specifies the DMA status register for channels 0-3 for reads; specifies the DMA control register for channels 0-3 for writes.

IO009 Dma_WriteRequest

Bits	Description
7:0	DmaWriteRequest. Read-write. Reset: 0. Request register.

IO00A Dma_WriteMask

Bits	Description
7:0	DmaWriteMask. Read-write. Reset: 0. DMA channel mask register.

IO00B Dma_WriteMode

Bits	Description
7:0	DmaWriteMode . Read-write. Reset: 0. DMA mode register.

IO00C Dma_Clear

Bits	Description
7:0	DmaClear . Read-write. Reset: 0. Channel 0-3 DMA clear byte pointer.

IO00D Dma_MasterClr

Dma_MasterClr register

Bits	Description
7:0	DmaMasterClr . Read-write. Reset: 0. Write: Channel 0-3 master clear register. Read: Intermediate register.

IO00E Dma_ClrMask

Bits	Description
7:0	DmaClrmask . Read-write. Reset: 0. Channel 0-3 DMA clear mask.

IO00F Dma_AllMask

Bits	Description
7:0	DmaAllMask . Read-write. Reset: 0. General mask register.

IO020 IntrCntrl1Reg1

Bits	Description
7:0	IntrCntrl1Reg1 . Read-write. Reset: 0. IRQ0-7 status and control. Read: IRR, ISR. Write: ICW1, OCW2, OCW3.

IO021 IntrCntrl1Reg2

Bits	Description
7:0	IntrCntrl1Reg2 . Read-write. Reset: 0. IRQ0-7 status and control. Read: IMR. Write: ICW2, ICW3, ICW4, OCW1.

IO022 IMCR_Index

Bits	Description
7:0	ImcrIndex. Read-write. Reset: 0. Index port for IMCR register. See IO023 [IMCR_Data] .

IO023 IMCR_Data

Bits	Description
7:0	ImcrData. Read-write. Reset: 0. Data port for IMCR register. The actual IMCR register is located at index 70h and it is at bit 0.

IO040 TimerCh0

Bits	Description
7:0	TimerCh0. Read-write. Reset: 0. 8254 Timer 1 Counter 0 Data Port.

IO041 TimerCh1

Bits	Description
7:0	TimerCh1. Read-write. Reset: 0. 8254 Timer 1 Counter 1 Data Port.

IO042 TimerCh2

Bits	Description
7:0	TimerCh2. Read-write. Reset: 0. 8254 Timer 1 Counter 2 Data Port.

IO043 Tmr1CntrlWord

Bits	Description
7:6	CounterSelect. Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b Select counter 0 01b Select counter 1 10b Select counter 2 11b Read back command
5:4	CommandSelect. Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b Counter latch command 01b Read/write least significant byte 10b Read/write most significant byte 11b Read/write least, and then most significant byte

3:1	ModeSelect . Read-write. Reset: 0.																
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IO060 Keyboard Data

Bits	Description
7:0	Data . Read-write. Reset: 0. Specifies the keyboard controller data port. It should only be read from when IO064[0] reads back 1. It should only be written to when IO064[1] reads back 0.

IO061 Nmi Status

Bits	Description
7	ParityErrNmi . Read-only. Reset: X. NMI is caused by parity error (either PERR# or SERR#).
6	IoChkNmi . Read-only. Reset: X. NMI is triggered by serial IOCHK.
5	SpkrClk . Read-only. Reset: X. The output of 8254 timer counter 2.
4	RefClk . Read-only. Reset: X. The output of 8254 timer counter 1.
3	IoChkNmiEn . Read-write. Reset: 1. 0=Enable IoChk to NMI generation. 1=Disable IoChk to NMI generation.
2	ParityErrNmiEn . Read-write. Reset: 1. 0=Enable Parity Error to NMI generation (from SERR# or PERR#). 1=Disable Parity Error to NMI generation and clear bit 7.
1	SpkrTmrEnable . Read-write. Reset: 0. 0=Speaker timer off. 1=Speaker timer on.
0	SpkrEnable . Read-write. Reset: 0. 0=Disable counter 2. 1=Enable counter 2.

IO064 Keyboard Status/Control

IF (READ)

Bits	Description
7	KeyPar . Read-only. Reset: 0. 1=Keyboard data transmission parity error.
6	KeyRTO . Read-only. Reset: 0. 1= Receive time out.
5	KeyTTO . Read-only. Reset: 0. 1=Keyboard transmit time out or mouse data available.
4	KeyEnB . Read-only. Reset: 0. 0=Password protected.
3	CmdData . Read-only. Reset: 0. 1=Between the keyboard command and data ports, the command port at 64h was last written to. 0=Between the keyboard command and data ports, the data port at 60h was last written to.
2	KeySys . Read-only. Reset: 0. Specifies system flag status. 1=Power up or reset. 1=Soft reset.

1	KeyIBF . Read-only. Reset: 0. 1=Input buffer full. 0=Ready to receive next command/data.
0	KeyOBF . Read-only. Reset: 0. 1=Data is available to read back. 0=No data available.

ELSE

Bits	Description
7:0	KeyCmd . Write-only. Reset: 0. Specified the keyboard command.

ENDIF.

IO070 RtcAddrPort and NmiMask

Bits	Description
7	NmiMask . Write-only. Reset: 0. 0=NMI enabled. 1=NMI masked.
6:0	RtcAddrPort: RTC Address Port . Read-write. Reset: 0. This is used with either internal RTC or external RTC. This port specifies the index to access RTC time registers and the CMOS RAM space. IO073_x0A [DV0] should be programmed first to select bank when accessing the CMOS RAM space. See IO073_x00 .

IO071 RtcDataPort

Bits	Description
7:0	RtcDataPort: RTC Data Port . Read-write. Reset: 0. This is used with either internal RTC or external RTC in conjunction with IO070 .

IO072 Alternate RTC AddrPort

Bits	Description
7:0	AlternatRTCAddrPort . Read-write. Reset: 0. This is used with internal RTC. This port allows user to specify the full 8 bit address (instead of bank0/bank1 indexing) to access the 256 bytes of RTC RAM.

IO073 Alternate RTC DataPort

Bits	Description
7:0	AlternatRTCDataPort . Read-write. Reset: 0. This is used with internal RTC in conjunction with IO072 .

IO073_x00 RTC Seconds

Bits	Description
7:0	Seconds . Read-write. Reset: 0. BCD format. The value range for this register is 00 through 59. If (IO073_x0B [SET]=1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B [SET]=0), this register is updated by the RTC logic once per second.

IO073_x01 RTC Seconds Alarm

Bits	Description
7:0	SecondsAlarm: Seconds Alarm. Read-write. Reset: 0. BCD format. If (IO073_x0B[SET]=1), the Seconds Alarm register will never match with IO073_x00 [RTC Seconds]. Else, if (bits [7:6] =11b) the RTC Seconds Alarm register always matches with RTC Seconds register and causes an RTC alarm event to be generated once per second. See IO073_x0C[AF].

IO073_x02 RTC Minutes

Bits	Description
7:0	Minutes. Read-write. Reset: 0. BCD format. The value range for this register is 00 through 59. If (IO073_x0B[SET]=1), this register programmed by software and hardware updating is disabled. If (IO073_x0B[SET]=0), this register is updated by the RTC logic once per second.

IO073_x03 RTC Minutes Alarm

Bits	Description
7:0	MinutesAlarm: Minutes Alarm. Read-write. Reset: 0. BCD format. If (IO073_x0B[SET]=1), the RTC Minutes Alarm register will never match with IO073_x02 [RTC Minutes]. Else, if (bits [7:6]=11b), the RTC Minutes Alarm register always matches with RTC Minutes register and causes an RTC alarm event to be generated once per minute. See IO073_x0C[AF].

IO073_x04 RTC Hours

Bits	Description
7:0	Hours. Read-write. Reset: 0. BCD format. The value range for this register is 00 through 23. If (IO073_x0B[SET]=1), this register can be set by software and hardware updating is disabled. If (IO073_x0B[SET]=0), this register is updated by the RTC logic once per second.

IO073_x05 RTC Hours Alarm

Bits	Description
7:0	HoursAlarm: Hours Alarm. Read-write. Reset: 0. BCD format. If (IO073_x0B[SET]=1), the RTC Hours Alarm register will never match with IO073_x04 [RTC Hours]. Else, if (bits [7:6] = 11b) the RTC Hours Alarm register always matches with the RTC Hours register and causes an RTC alarm event to be generated once per hour. See IO073_x0C[AF].

IO073_x06 RTC Day of Week

Bits	Description
7:0	DayOfWeek: Day of Week. Read-write. Reset: 0. BCD format. The value range for this register is 01 through 07 (Sunday = 1). Leap year correction is performed by software. If (IO073_x0B[SET] =1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET] =0), this register is updated by hardware.

IO073_x07 RTC Date of Month

Bits	Description
7:0	DateOfMonth: Date of Month. Read-write. Reset: 0. BCD format. The range is 01 through 31. Leap year correction is performed by software. If (IO073_x0B[SET] =1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET] =0), this register is updated by hardware.

IO073_x08 RTC Month

Bits	Description
7:0	Month. Read-write. Reset: 0. BCD format. The range is 01 through 12. Leap year correction is performed by software. If (IO073_x0B[SET] =1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET] =0), this register is updated by hardware.

IO073_x09 RTC Year

Bits	Description
7:0	Year. Read-write. Reset: 0. BCD format. Range is 00 through 99. No leap year correction capability. Leap year correction has to be done by software. If (IO073_x0B[SET] =1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET] =0), this register is updated by hardware.

IO073_x0A RTC Register A

Bits	Description
7	UIP: Update In Progress. Read-only. Reset: 0. If (IO073_x0B[SET] =1), UIP is cleared. 1=The update transfer will soon occur. 0=The update transfer will not occur for at least 244 us.
6:5	Reserved.

4	DV0: Bank Selection. Read-write. Reset: 0. 0=Select bank 0 when accessing the RTC CMOS RAM space through IO070 and IO071 . 1=Select bank 1 when accessing the RTC CMOS RAM space through IO070 and IO071 . The FCH has an alternate way to access the RAM without the use of bank select bit. IO072 [Alternate RTC AddrPort] and IO073 [Alternate RTC DataPort] provides indexed access to the full 256 bytes of RAM.																																		
3:0	<p>RS[3:0]: Rate Selection. Read-write. Reset: 0. These four rate selection bits select one of the 13 taps on the 15-stage frequency divider or disable the divider output (flat output signal). The tap selected can be used to generate a periodic interrupt. See the following table for the frequency selection.</p> <table> <thead> <tr> <th>Bits</th> <th>Tap Frequency (Interrupt Rate)</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Flat Signal (None)</td> </tr> <tr> <td>0001b</td> <td>256 Hz (3.90625 ms)</td> </tr> <tr> <td>0010b</td> <td>128 Hz (7.8125 ms)</td> </tr> <tr> <td>0011b</td> <td>8.192 kHz (122.070 us)</td> </tr> <tr> <td>0100b</td> <td>4.096 kHz (244.141 us)</td> </tr> <tr> <td>0101b</td> <td>2.048 kHz (488.281 us)</td> </tr> <tr> <td>0110b</td> <td>1.024 kHz (976.5625 us)</td> </tr> <tr> <td>0111b</td> <td>512 Hz (1.953125 ms)</td> </tr> <tr> <td>1000b</td> <td>256 Hz (3.90625 ms)</td> </tr> <tr> <td>1001b</td> <td>128 Hz (7.8125 ms)</td> </tr> <tr> <td>1010b</td> <td>64 Hz (15.625 ms)</td> </tr> <tr> <td>1011b</td> <td>32 Hz (31.25 ms)</td> </tr> <tr> <td>1100b</td> <td>16 Hz (62.5 ms)</td> </tr> <tr> <td>1101b</td> <td>8 Hz (125 ms)</td> </tr> <tr> <td>1110b</td> <td>4 Hz (250 ms)</td> </tr> <tr> <td>1111b</td> <td>2 Hz (500 ms)</td> </tr> </tbody> </table>	Bits	Tap Frequency (Interrupt Rate)	0000b	Flat Signal (None)	0001b	256 Hz (3.90625 ms)	0010b	128 Hz (7.8125 ms)	0011b	8.192 kHz (122.070 us)	0100b	4.096 kHz (244.141 us)	0101b	2.048 kHz (488.281 us)	0110b	1.024 kHz (976.5625 us)	0111b	512 Hz (1.953125 ms)	1000b	256 Hz (3.90625 ms)	1001b	128 Hz (7.8125 ms)	1010b	64 Hz (15.625 ms)	1011b	32 Hz (31.25 ms)	1100b	16 Hz (62.5 ms)	1101b	8 Hz (125 ms)	1110b	4 Hz (250 ms)	1111b	2 Hz (500 ms)
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IO073_x0B RTC Register B

Bits	Description
7	SET: Set new time. Read-write. Reset: 0. 1=No internal updating for RTC time registers occurs. 0=The RTC time registers are updated every second.
6	PIE: Periodic Interrupt Enable. Read-write. Reset: 0. 1=Enable the IO073_x0C[PF] bit to assert IRQ.
5	AIE: Alarm Interrupt Enable. Read-write. Reset: 0. 1=Enable the IO073_x0C[AF] bit to assert IRQ. When the alarm time is written in the appropriate hours, minutes, and seconds alarm registers, the alarm interrupt is initiated at the specified time each day if AIE=1.
4	UIE: Update Ended Interrupt Enable. Read-write. Reset: 0. 1=Enable the IO073_x0C[UF] bit to assert IRQ. If [SET]=1, UIE is cleared.
3:2	Reserved.
1	HourMode. Read-write. Reset: 0. 0=12 hour mode. 1=24 hour mode.
0	DaylightSavingEnable. Read-write. Reset: 0. 1=If (PMx5F_x00[DltSavEnable] =1) RTC daylight saving is enabled.

IO073_x0C RTC Register C

Bits	Description
7	IRQF: Interrupt Request Flag. Read-only. Reset: 0. IRQF=(PF*PIE)+(AF*AIE)+(UF*UIE). 1=The IRQ# pin is driven low. Reading RTC Register C clears IRQF bit.
6	PF: Periodic Interrupt Flag. Read-only. Reset: 0. 1=An edge is detected on the selected tap (through RS3 to RS0) of the frequency divider. Reading RTC Register C clears PF bit.
5	AF: Alarm Interrupt Flag. Read-only. Reset: 0. 1= IO073_x00 [RTC Seconds] , IO073_x02 [RTC Minutes] , IO073_x04 [RTC Hours] and IO073_x07 [RTC Date of Month] match IO073_x01 [RTC Seconds Alarm] , IO073_x03 [RTC Minutes Alarm] , IO073_x05 [RTC Hours Alarm] , and IO073_x0D [RTC Date Alarm] respectively. Reading RTC Register C clears AF bit.
4	UF: Update Ended Interrupt Flag. Read-only. Reset: 0. 1=Update cycle complete. Reading RTC Register C clears UF.
3:0	Reserved.

IO073_x0D RTC Date Alarm

Bits	Description
7	VRT: Valid RAM and Time. Read-only. Reset: 1. 1=RTC date, time, and CMOS RAM are valid. 0=RTC date, time, and CMOS RAM are invalid due to low RTC battery being monitored. See PMx58 [VRT_T1] and PMx59 [VRT_T2] .
6	ScratchBit. Read-write. Reset: 0.
5:0	DateAlarm. Read-write. Reset: 0. If (DateAlarm!=0), then DateAlarm is considered for alarm generation. 0=DateAlarm is not compared for alarm generation. DateAlarm is in BCD format.

IO073_x32 RTC AltCentury

Bits	Description
7:0	AltCentury. Read-write. Reset: 0. BCD format. Leap year correction is performed by hardware. This register is accessed only when (IO073_x0A[DV0]=0) and (PMx56[CenturyEn]=1). If (IO073_x0B[SET]=1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET]=1), this register is automatically updated by hardware every century.

IO073_x48 RTC Century

Bits	Description
7:0	Century. Read-write. Reset: 0. BCD format. Leap year correction is done through hardware. This register is accessed only when (IO073_x0A[DV0]=1). If (IO073_x0B[SET]=1), this register is programmed by software and hardware updating is disabled. If (IO073_x0B[SET]=0), this register is automatically updated by hardware every century.

IO073_x50 RTC Extended RAM Address Port

Bits	Description
7	Reserved.
6:0	ExtendedRamAddrPort . Read-write. Reset: 0. Because only 7 address bits are used in IO070 [RtcAddrPort], only the lower 128 bytes at offset 7Fh:00h are accessible through IO071 [Rtc-DataPort]. The Extended RAM are physically located at address 80h to FFh. In order to access these addresses, an address offset should be programmed into this register and access to them is done through IO073_x53 [RTC Extended RAM Data Port]. An offset of 80h is automatically be added to this 7-bit address.

IO073_x53 RTC Extended RAM Data Port

Bits	Description
7:0	ExtendedRamDataPort . Read-write. Reset: X. There is no physical register corresponding to this data port but the data port address is used for decoding to generate appropriate internal control signals.

IO073_x7E RTC Time Clear

Bits	Description
7:1	Reserved.
0	RtcTimeClear . Read-write. Reset: 0. 1=Clear the RTC second and stop RTC time.

IO073_x7F RTC RAM Enable

Bits	Description
7:1	Reserved.
0	RtcRamEnable . Read-write. Reset: 1. 1=Enable access to the RTC RAM.

IO080 PostCode

Bits	Description
7:0	PostCode: BIOS post code . Read-write. Reset: 0. BIOS post code register, can be 32-bits for writes, 8 bits for reads. See MISCx78 [PostCode].

IO081 Dma_PageCh2

Bits	Description
7:0	DmaPagech2 . Read-write. Reset: 0. DMA2 channel 2 page register.

IO082 Dma_PageCh3

Bits	Description
7:0	DmaPageCh3 . Read-write. Reset: 0. DMA2 channel 3 page register.

IO083 Dma_PageCh1

Bits	Description
7:0	DmaPageCh1 . Read-write. Reset: 0. DMA2 channel 1 page register.

IO084 Dma_Page_Reserved1

Bits	Description
7:0	DmaPageReserved1 . Read-write. Reset: 0. DMA Page Reserved1 register.

IO085 Dma_Page_Reserved2

Bits	Description
7:0	DmaPageReserved2 . Read-write. Reset: 0. DMA Page Reserved2 register.

IO086 Dma_Page_Reserved3

Bits	Description
7:0	DmaPageReserved3 . Read-write. Reset: 0. DMA Page Reserved3 register.

IO087 Dma_PageCh0

Bits	Description
7:0	DmaPageCh0 . Read-write. Reset: 0. DMA2 channel 0 page register.

IO088 Dma_Page_Reserved4

Bits	Description
7:0	DmaPageReserved4 . Read-write. Reset: 0. DMA Page Reserved4 register.

IO089 Dma_PageCh6

Bits	Description
7:0	DmaPageCh6 . Read-write. Reset: 0. DMA2 channel 6 page register.

IO08A Dma_PageCh7

Bits	Description
7:0	DmaPageCh7 . Read-write. Reset: 0. DMA2 channel 7 page register.

IO08B Dma_PageCh5

Bits	Description
7:0	DmaPageCh5 . Read-write. Reset: 0. DMA2 channel 5 page register.

IO08C Dma_Page_Reserved5

Bits	Description
7:0	DmaPageReserved5 . Read-write. Reset: 0. DMA Page Reserved5 register.

IO08D Dma_Page_Reserved6

Bits	Description
7:0	DmaPageReserved6 . Read-write. Reset: 0. DMA Page Reserved6 register.

IO08E Dma_Page_Reserved7

Bits	Description
7:0	DmaPageReserved7 . Read-write. Reset: 0. DMA Page Reserved7 register.

IO08F Dma_Refresh

Bits	Description
7:0	DmaRefresh . Read-write. Reset: 0. DMA2 channel 4 page register.

IO092 FastInit

Bits	Description
7:2	Reserved.
1	A20EnB: A20 Enable Bar bit . Read-write. Reset: 0. 1=A20M# function is disabled.
0	FastInit . Read-write. Reset: 0. This bit provides a fast software executed processor reset function. 1=Generate INIT assertion for approximately 4 ms. 0=Before another INIT pulse can be generated via this register, this bit must be written back to a 0.

IO0A0 IntrCntrl2Reg1

Bits	Description
7:0	IntrCntrl2Reg1. Read-write. Reset: 0. IRQ8-15 status and control. Read: IRR, ISR. Write: ICW1, OCW2, OCW3.

IO0A1 IntrCntrl2Reg2

Bits	Description
7:0	IntrCntrl2Reg2. Read-write. Reset: 0. IRQ8-15 status and control. Read: IMR. Write: ICW2, ICW3, ICW4, OCW1.

IO0C0 Dma2_Ch4Addr

Bits	Description
7:0	Dma2Ch4Addr. Read-write. Reset: 0. DMA2 channel 4 base and current address.

IO0C2 Dma2_Ch4Cnt

Bits	Description
7:0	Dma2Ch4Cnt. Read-write. Reset: 0. DMA2 channel 4 base and current count.

IO0C4 Dma2_Ch5Addr

Bits	Description
7:0	Dma2Ch5Addr. Read-write. Reset: 0. DMA2 channel 5 base and current address.

IO0C6 Dma2_Ch5Cnt

Bits	Description
7:0	Dma2Ch5Cnt. Read-write. Reset: 0. DMA2 channel 5 base and current count.

IO0C8 Dma2_Ch6Addr

Bits	Description
7:0	Dma2Ch6Addr. Read-write. Reset: 0. DMA2 channel 6 base and current address.

IO0CA Dma2_Ch6Cnt

Bits	Description
7:0	Dma2Ch6Cnt. Read-write. Reset: 0. DMA2 channel 6 base and current count.

IO0CC Dma2_Ch7Addr

Bits	Description
7:0	Dma2Ch7Addr. Read-write. Reset: 0. DMA2 channel 7 base and current address.

IO0CE Dma_Ch7Cnt

Bits	Description
7:0	Dma2Ch7Cnt. Read-write. Reset: 0. DMA2 channel 7 base and current count.

IO0D0 Dma_Status

Bits	Description
7:0	DmaStatus. Read-write. Reset: 0. DMA2 status register.

IO0D2 Dma_WriteRequest

Bits	Description
7:0	DmaWriteRequest. Read-write. Reset: 0. DMA2 request register.

IO0D4 Dma_WriteMask

Bits	Description
7:0	DmaWriteMask. Read-write. Reset: 0. DMA2 channel mask register.

IO0D6 Dma_WriteMode

Bits	Description
7:0	DmaWriteMode. Read-write. Reset: 0. DMA2 mode register.

IO0D8 Dma_Clear

Bits	Description
7:0	DmaClear. Read-write. Reset: 0. Channel 4-7 clear byte pointer.

IO0DA Dma_MasterClr

Bits	Description
7:0	DmaMasterClear. Read-write. Reset: 0. Write: Channel 4-7 DMA master clear. Read: Intermediate register.

IO0DC Dma_ClrMask

Bits	Description
7:0	DmaClrMask. Read-write. Reset: 0. Channel 4-7 DMA clear mask.

IO0DE Dma_AllMask

Bits	Description
7:0	DmaAllMask. Read-write. Reset: 0. DMA2 mask register.

IO0F0 NCP Error

Writes to this port assert IGNNE# if FERR# is true. If FERR# is false, writes to this port do not assert IGNNE#. The first write will set WarmBoot.

Bits	Description
7	WarmBoot. Read; write-once. Cold reset: 0. Warm or cold boot indicator. 0=Cold. 1=Warm. This bit is set when any value is written to this register. The BIOS reads (tests) this register early in to POST process, then writes the register, thus setting WarmBoot. On subsequent warm boots, this flag will remain set.
6:0	Reserved.

IO4D0 IntrEdgeControl

Bits	Description
15	IRQ15Control. Read-write. Reset: 0. 1=Level. 0=Edge.
14	IRQ14Control. Read-write. Reset: 0. 1=Level. 0=Edge.
13	Reserved.
12	IRQ12Control. Read-write. Reset: 0. 1=Level. 0=Edge.
11	IRQ11Control. Read-write. Reset: 0. 1=Level. 0=Edge.
10	IRQ10Control. Read-write. Reset: 0. 1=Level. 0=Edge.
9	IRQ9Control. Read-write. Reset: 0. 1=Level. 0=Edge.
8	IRQ8Control. Read-only. Reset: 0. Always edge.
7	IRQ7Control. Read-write. Reset: 0. 1=Level. 0=Edge.
6	IRQ6Control. Read-write. Reset: 0. 1=Level. 0=Edge.
5	IRQ5Control. Read-write. Reset: 0. 1=Level. 0=Edge.

4	IRQ4Control. Read-write. Reset: 0. 1=Level. 0=Edge.
3	IRQ3Control. Read-write. Reset: 0. 1=Level. 0=Edge.
2	Reserved.
1	IRQ1Control. Read-write. Reset: 0. 1=Level. 0=Edge.
0	IRQ0Control. Read-write. Reset: 0. 1=Level. 0=Edge.

IOC00 Pci_Intr_Index

Bits	Description
7	PciIntrApic. Read-write. Reset: 0. 0=IRQ routing to PIC. 1=IRQ routing to IOAPIC.
6:0	PciIntrIndex. Read-write. Reset: 0. PCI interrupt index. Selects which PCI interrupt to map.
	Bits Definition
00h	INTA#
01h	INTB#
02h	INTC#
03h	INTD#
04h	INTE#
05h	INTF#
06h	INTG#
07h	INTH#
08h	Misc
09h	Misc0
0Ah	Misc1
0Bh	Misc2
0Ch	INTA from serial IRQ
0Dh	INTB from serial IRQ
0Eh	INTC from serial IRQ
0Fh	INTD from serial IRQ
10h	SCI
11h	SMBUS0
12h	ASF
13h	HD audio
14h	FC
15h	Reserved
16h	PerMon
17h	SD
	Bits Definition
18h	Reserved
19h	DSM trigger Intr
1Fh-1Ah	Reserved
20h	IMC INT0
21h	IMC INT1
22h	IMC INT2
23h	IMC INT3
24h	IMC INT4
25h	IMC INT5
2Fh-26h	Reserved
30h	Dev12h (USB) INTA#
31h	Dev12h (USB) INTB#
32h	Dev13h (USB) INTA#
33h	Dev13h (USB) INTB#
34h	Dev16h (USB) INTA#
35h	Dev16h (USB) INTB#
40h-36h	Reserved
41h	SATA PCI interrupt
7Fh-42h	Reserved

IOC01 Pci_Intr_Data

Bits	Description
7:0	PciIntrData. Read-write. Reset: 0.

IOC01_x0[7:0] PCI INT[H#,G#,F#,E#,D#,C#,B#,A#] Map

Bits	Description
7:5	Reserved. Read-write. Reset: 3.
4:0	Pci2IntrMap . Read-write. Reset: 1Fh. If (IOC00[PciIntrApic]==1) then Pci2IntrMap specifies mapping of INT[H#:A#] to APIC interrupt number. If (IOC00[PciIntrApic]==0) then Pci2IntrMap specifies mapping of INT[H#:A#] to PIC interrupt number.

IOC01_x08 Intr Misc Map

Bits	Description										
7:6	Pci2Intr15Map . Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>IRQ15 mapped to legacy IDE</td> </tr> <tr> <td>01b</td> <td>IRQ15 mapped to SATA IDE</td> </tr> <tr> <td>10b</td> <td>IRQ15 mapped to SATA2</td> </tr> <tr> <td>11b</td> <td>IRQ15 come from Serial IRQ or PCI interrupt</td> </tr> </tbody> </table>	Bits	Definition	00b	IRQ15 mapped to legacy IDE	01b	IRQ15 mapped to SATA IDE	10b	IRQ15 mapped to SATA2	11b	IRQ15 come from Serial IRQ or PCI interrupt
Bits	Definition										
00b	IRQ15 mapped to legacy IDE										
01b	IRQ15 mapped to SATA IDE										
10b	IRQ15 mapped to SATA2										
11b	IRQ15 come from Serial IRQ or PCI interrupt										
5:4	Pci2Intr14Map . Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>IRQ14 mapped to legacy IDE</td> </tr> <tr> <td>01b</td> <td>IRQ14 mapped to SATA IDE</td> </tr> <tr> <td>10b</td> <td>IRQ14 mapped to SATA2</td> </tr> <tr> <td>11b</td> <td>IRQ14 mapped to Serial IRQ or PCI interrupt</td> </tr> </tbody> </table>	Bits	Definition	00b	IRQ14 mapped to legacy IDE	01b	IRQ14 mapped to SATA IDE	10b	IRQ14 mapped to SATA2	11b	IRQ14 mapped to Serial IRQ or PCI interrupt
Bits	Definition										
00b	IRQ14 mapped to legacy IDE										
01b	IRQ14 mapped to SATA IDE										
10b	IRQ14 mapped to SATA2										
11b	IRQ14 mapped to Serial IRQ or PCI interrupt										
3	PciIntrIrq12 . Read-write. Reset: 0. 0=IMC as IRQ12 input source. 1=Serial IRQ or PCI devices as IRQ12 input source.										
2	PciIntrIrq8 . Read-write. Reset: 0. 0=RTC is IRQ8 input source. 1=Serial IRQ or PCI devices as IRQ8 input source.										
1	PciIntrIrq1 . Read-write. Reset: 0. 0=IMC as IRQ1 input source. 1=Serial IRQ or PCI devices as IRQ1 input source.										
0	PciIntrIrq0 . Read-write. Reset: 0. 0=8254 timer as IRQ0 input source. 1=Serial IRQ or PCI devices as IRQ0 input source.										

IOC01_x09 Intr Misc 0 Map

Bits	Description
7	IntrDelay . Read-write. Reset: 1. INTR 600 ns delay.
6	IRQ12FilterEnable . Read-write. Reset: 1. IRQ12 filter enable.
5	IRQ1FilterEnable . Read-write. Reset: 1. IRQ1 filter enable.
4	IrqInputEn . Read-write. Reset: 0. 0=Mask off IRQ input. 1=Enable IRQ input.
3	MaskIrq1Irq12 . Read-write. Reset: 0. 0=Enable IRQ1 and IRQ12. 1=Mask off IRQ1 and IRQ12.
2	Merge_Ec_irq12 . Read-write. Reset: 1. 0=Route serial IRQ12 to USB IRQ12 input. 1=Route IMC IRQ12 to USB IRQ12 input.

1	Merge_Ec_irq1 . Read-write. Reset: 1. 0=Route serial IRQ1 to USB IRQ1 input. 1=Route IMC IRQ1 to USB IRQ1 input.
0	IntMap . Read-write. Reset: 1. 0=INT0 in IOAPIC comes from IRQ0 in PIC, INT2 in IOAPIC comes from INTR in PIC. 1=INT2 in IOAPIC comes from IRQ0 in PIC, INT0 in IOAPIC comes from INTR in PIC.

IOC01_x0A IntrMisc1Map

Bits	Description
7:0	HPET . Read-write. Reset: 0. Writes to this register update the bits in HPETx1[4:0:Step2]0[47:32] ; All 3 registers, HPETx100[47:32], HPETx120[47:32], and HPETx140[47:32], are updated at the same time. IOC01_x0A updates the lower 8 bits. IOC01_x0B updates the upper 8 bits.

IOC01_x0B IntrMisc2Map

Bits	Description
7:0	HPET . See: IOC01_x0A[HPET] .

IOC01_x0[7F:C] PCI Interrupt Map

Bits	Description
7:5	Reserved. Read-write. Reset: 3.
4:0	Pci2IntrMap . Read-write. Reset: 1Fh. If (IOC00[PciIntrApic]==1), then Pci2IntrMap specifies the APIC interrupt number that the corresponding PCI interrupt maps to. If (IOC00[PciIntrApic]==0), then Pci2IntrMap specifies the PIC interrupt number that the corresponding PCI interrupt maps to. See IOC00 [Pci_Intr_Index] for the PCI interrupt list.

IOC14 Pci_Error

Bits	Description
7:4	Reserved.
3	PerrNmi . Read-write. Reset: 1. Enable NMI generation from PERR#. 0=Enable. 1=Disable.
2	SerrNmi . Read-write. Reset: 1. Enable NMI generation from SERR#. 0=Enable. 1=Disable.
1	PerrNmiStatus . Read-only. Reset: X. 1=NMI generation is enabled and PERR# is asserted due to a PCI data parity error. This bit is cleared by writing 1 to IO061[2] .
0	SerrNmiStatus . Read-only. Reset: X. 1=NMI generation is enabled and SERR# is asserted due to a PCI error. This bit is cleared by writing 1 to IO061[2] .

IOCD0 PM2_Index

Bits	Description
7:0	Pm2Index: Power management 2 index register. Read-write. Reset: 0. This register specifies the index of the power management 2 register. See Power Management Block 2 (PM2) Registers .

IOCD1 PM2_Data

Bits	Description
7:0	Pm2Data: Power management 2 data register. Read-write. Reset: 0. This register specifies the data read from/written to the power management 2 register pointed by IOCD0 . See Power Management Block 2 (PM2) Registers .

IOCD4 BIO SRAMIndex

Bits	Description
7:0	BiosRamIndex: BIOS RAM index register. Read-write. Reset: 0. This register specifies the index in the 256-byte BIOS RAM. Data in this RAM is preserved until RSMRST# is asserted or S5 power is lost.

IOCD5 BIO SRAM Data

Bits	Description
7:0	BiosRamData: BIOS RAM data register. Read-write. Reset: 0. This register specifies the data read from/written to the BIOS RAM pointed by IOCD4 .

IOCD6 PM_Index

Bits	Description
7:0	PmIndex: Power management index register. Read-write. Reset: 0. This register specifies the index of the power management register. See 3.26.13 [Power Management (PM) Registers] .

IOCD7 PM_Data

Bits	Description
7:0	PmData: Power management data register. Read-write. Reset: 0. This register specifies the data read from/written to the power management register pointed by IOCD6 . See 3.26.13 [Power Management (PM) Registers] .

IOCF9 System Reset Register

This register can be accessed through [PMxC5 \[CF9 Shadow\]](#).

Bits	Description
7:4	Reserved.
3	FullRst . Read-write. Reset: 0. 0=Assert reset signals only. 1=Place system in S5 state for 3 to 5 seconds.
2	RstCmd . Read-write; Cleared-by-hardware. Reset: 0. 1=Generate reset as specified by FullRst and SysRst.
1	SysRst . Read-write. Reset: 0. 0=Send an INIT HT message. 1=Reset as specified by FullRst.
0	Reserved.

3.26.2 AB Configuration Registers (Scallion)

AB Configuration registers are accessed indirectly through **ABx00 [AB Index Register]** and **ABx04 [AB Data Register]**. The **ABx00/ABx04** register pair is located in IO address space as defined by **PMxE0**.

ABx00 AB Index Register

Bits	Description
31:29	RegSpace. Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 101b-000b Reserved 110b ABCFG. A-Link Bridge Configuration 111b Reserved Once a valid register block address is written to this field, only valid register block addresses can be written to this field.
28:17	Reserved.
16:0	RegAddr: Register Address. Read-write. Reset: 0.

ABx04 AB Data Register

Bits	Description
31:0	Data: Register Address. Read-write. Reset: 0.

ABx04_x54 Misc Control 1

Bits	Description
24	BIClkGateEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . 1=Enable gating of B-Link clocks when idle is detected.
23:16	BIClkGateDelay. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . Specifies the number of B-Link clocks to delay before gating B-Link clocks after idle condition is detected.
4	DbgClkGateEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . 1=Enable gating of B-Link debug clocks; hence no debug clock running.
3	Reserved.
2	UpSWrByteCntSbgMode. Read-write. Reset: 0. BIOS: See 2.15.11.4 . 1=Upstream 32/64 byte MST_BIF write requests will be issued only when all byte enables in the request are 1. This field is mutually exclusive with UpWr16BMode.
0	UpWr16BMode. Read-write. Reset: 1. BIOS: See 2.15.11.4 . Enables upstream writes to be limited to a maximum of 16-bytes per transaction. 0=Disable 16 Byte mode; AB can send DMA write request with length 16, 32, or 64 bytes. 1=Enable 16 Byte mode; AB will only send DMA write request with length 16 bytes. This bit should be mutually exclusive with UpSWrByteCntSbgMode. See ABx04_x204[Dma16ByteMode] .

ABx04_x58 B-Link RAB Control

Bits	Description
31	AlMemSDEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.2 . 1=Enable AB A-Link Memory Shut Down Feature. See ABx04_x10054 [27:26] for idle counter settings.
29	BIMemSDEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.2 . 1=Enable AB B-Link Memory Shut Down Feature. See ABx04_x10054 [27:26] for idle counter settings.

ABx04_x80 B-Link DMA Prefetch Control

Bits	Description										
31:22	Reserved. Reset: 0Ch.										
21:16	BIPrefMode. Read-write. Reset: 0. BIOS: 6. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[5:3]</td> <td>Reserved.</td> </tr> <tr> <td>[2]</td> <td>Reserved, must be programmed to 1 to set B-Link prefetch mode</td> </tr> <tr> <td>[1]</td> <td>Reserved, must be programmed to 1 to set B-Link prefetch mode</td> </tr> <tr> <td>[0]</td> <td>Reserved.</td> </tr> </tbody> </table>	Bit	Definition	[5:3]	Reserved.	[2]	Reserved, must be programmed to 1 to set B-Link prefetch mode	[1]	Reserved, must be programmed to 1 to set B-Link prefetch mode	[0]	Reserved.
Bit	Definition										
[5:3]	Reserved.										
[2]	Reserved, must be programmed to 1 to set B-Link prefetch mode										
[1]	Reserved, must be programmed to 1 to set B-Link prefetch mode										
[0]	Reserved.										
15:8	Reserved.										
7:0	BIPrefEn. Read-write. Reset: 0. BIOS: 1. Enable B-Link prefetch on a per-device basis. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[7:1]</td> <td>Reserved.</td> </tr> <tr> <td>[0]</td> <td>USB OHCI.</td> </tr> </tbody> </table>	Bit	Definition	[7:1]	Reserved.	[0]	USB OHCI.				
Bit	Definition										
[7:1]	Reserved.										
[0]	USB OHCI.										

ABx04_x90 BIF Control 0

Bits	Description
21	PpNpRfwCplCtrl. Read-write. Reset: 0. BIOS: 1. RFW completion control for posted pass non-posted. Required by “Posted pass Non-posted” feature. Set to 1 for SMI ordering enhancement enable.
20:0	Reserved. Read-write.

ABx04_x94 MSI Control

Bits	Description
31:21	Reserved.
20	MsiAddrEn. Read-write. Reset: 0. BIOS: 1. 1=Enable AB to detect MSI sent upstream from FCH and inform power-management controller.
19:0	MsiAddr[39:20]. Read-write. Reset: 0. BIOS: See 2.15.11.1 . Specifies MSI Address[39:20].

ABx04_x204 SBG Upstream Control

Bits	Description
0	Dma16ByteMode. Read-write. Reset: 0. To always split DMA write request to be 16 bytes request. 0=All the DMA write requests has the size that AB passes up. 1=Split the DMA write requests to be 16 bytes requests. Overrides ABx04_x54[UpWr16BMode] .

ABx04_x10054 A-Link Arbitration Control and Clock Control (AL_Arb_Ctl, AL_Clk_Ctl)

Bits	Description
25	DbgClkGateEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . 1=Enable gating of A-Link debug clocks; hence debug clock will be disabled.
24	AlClkGateEn. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . 1=Enable gating of A-Link clocks when idle is detected.
23:16	AlClkGateDelay. Read-write. Reset: 0. Char.Temp.BIOS: See 2.15.11.3 . Specifies the number of cycles to delay before gating A-Link clocks after idle condition is detected.
11:0	ArbCtl. Read-write. Reset: 0. BIOS: 7FFh. A-Link Arbiter Control. Enable the A-Link int_arbiter enhancement to allow the A-Link bandwidth to be used more efficiently

ABx04_x10090 Misc Control 3

Bits	Description
16	IOTrapDelayEnable: IO Trap Delay Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable the IO trap delay logic for the SMI message to ensure that the SMI messages are sent to the CPU in the right order.

3.26.3 SATA Controller

3.26.3.1 Device 11h Function 0 (SATA) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D11F0x00 Device/Vendor ID

Bits	Description														
31:16	<p>DeviceID. IF (D11F0x40[SubclassCodeWriteEnable]==1) THEN Read-write. ELSE Read-only. ENDIF.</p> <p>IF (Fuse[APU_FCH_FUSES[SATARAIDFUNC]]==x0b) THEN Reset: 7800h. ELSE Reset: 7803h. ENDIF.</p> <p>SATA controller has different device IDs for different drivers.</p> <table> <thead> <tr> <th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>7800h</td><td>SATA in IDE mode</td></tr> <tr> <td>7801h</td><td>SATA in AHCI mode with MS driver</td></tr> <tr> <td>7804h</td><td>SATA in AHCI mode with AMD driver</td></tr> <tr> <td>7802h</td><td>SATA in RAID mode with Promise non-Raid 5 driver</td></tr> <tr> <td>7803h</td><td>SATA in RAID mode with Promise Raid 5 driver</td></tr> <tr> <td>7805h</td><td>DotHill RAIDCore driver</td></tr> </tbody> </table> <p>IF(RevA1) THEN 780Ah 3rd party RAID driver ENDIF.</p> <p>If ((Fuse[APU_FCH_FUSES[SATARAIDFUNC]]==x0b) && (D11F0x40[SubclassCodeWriteEnable]==1)), attempts to program to 7803h will result in 7802h.</p> <p>IF (RevA1) THEN If ((D11F0x40[SubclassCodeWriteEnable]==1)&&(Fuse[APU_FCH_FUSES[SATARAIDFUNC]]==1xb)), bit 3 is programmable and 780Ah can be programmed. If (Fuse[APU_FCH_FUSES[SATARAIDFUNC]]==0xb), bit 3 is tied to 0. ENDIF.</p>	Bits	Definition	7800h	SATA in IDE mode	7801h	SATA in AHCI mode with MS driver	7804h	SATA in AHCI mode with AMD driver	7802h	SATA in RAID mode with Promise non-Raid 5 driver	7803h	SATA in RAID mode with Promise Raid 5 driver	7805h	DotHill RAIDCore driver
Bits	Definition														
7800h	SATA in IDE mode														
7801h	SATA in AHCI mode with MS driver														
7804h	SATA in AHCI mode with AMD driver														
7802h	SATA in RAID mode with Promise non-Raid 5 driver														
7803h	SATA in RAID mode with Promise Raid 5 driver														
7805h	DotHill RAIDCore driver														
15:0	VendorID: Vendor ID. Read-only. Reset: 1022h.														

D11F0x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; write-1-to-clear. Reset: 0. 1=The SATA controller detects a parity error.
30	SerrStatus: SERR# Status. Read; write-1-to-clear. Reset: 0. 1=The SATA controller detects a PCI address parity error.
29	ReceivedMasterAbort: Received Master Abort. Read; write-1-to-clear. Reset: 0. 1=The SATA controller aborts a PCI bus memory cycle while acting as a PCI master.
28	ReceivedTargetAbort: Received Target Abort. Read; write-1-to-clear. Reset: 0. 1=The SATA controller generated PCI cycle (SATA controller is the PCI master) is aborted by a PCI target.
27	SignaledTargetAbort: Signaled Target Abort. Read; write-1-to-clear. Reset: 0. 1=The SATA controller signals Target Abort.

26:25	DevSelTiming: DEVSEL# Timing. Value: 1. These bits indicate DEVSEL# timing when performing a positive decode. 1=DEVSEL# is asserted to meet the medium timing.
24	DataParityError: Data Parity Error. Read; write-1-to-clear. Reset: 0. 1=SATA controller detects PERR# being asserted while acting as PCI master, regardless whether PERR# was driven by SATA controller or not.
23	FastBack2BackCapable: Fast Back-to-Back Capable. Value: 0.
22	Reserved.
21	Support66MHz: 66 MHz Support. Read-only. Reset: 1. 1=66 MHz capable.
20	CapabilitiesList: Capabilities List. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. 1=Capability list supported.
19	InterruptStatus: Interrupt Status. Read-only. Reset: 0. This bit reflects the state of the interrupt in the device/function. If (InterruptDisable==0) && (InterruptStatus==1), the device/function's INTx# signal is asserted. Setting InterruptDisable to 1 has no effect on the state of this bit.
18:11	Reserved.
10	InterruptDisable: Interrupt Disable. Read-write. Reset: 0. This bit disables the device/function from asserting INTx#. 0=Enable the assertion of the device/function's INTx# signal. 1=Disable the assertion of the device/function's INTx# signal.
9	FastBack2BackEnable: Fast Back-to-Back Enable. Value: 0.
8	SERREnable: SERR# Enable. Read-write. Reset: 0. 1=The SATA controller asserts SERR# when it detects an address parity error && (PerrDetectionEnable==1). 0=SERR# is not asserted.
7	WaitCycleEnable: Wait Cycle Enable. Value: 0.
6	PerrDetectionEnable: PERR# Detection Enable. Read-write. Reset: 0. 1=The host controller asserts PERR# when it is the agent receiving data && when it detects a parity error. 0=PERR# is not asserted.
5	VGAPaletteSnoopEnable: VGA Palette Snoop Enable. Value: 0.
4	MemoryWriteandInvalidateEnable: Memory Write and Invalidate Enable. Value: 0.
3	SpecialCycleRecognitionEnable: Special Cycle Recognition Enable. Value: 0.
2	BusMasterEnable: Bus Master Enable. Read-write. Reset: 0. 1=Enable the device behaving as a bus master.
1	MemoryAccessEnable: Memory Access Enable. Read-write. Reset: 0. 1=Enable the SATA controller to respond to PCI memory space access.
0	IOAccessEnable: IO Access Enable. Read-write. Reset: 0. 1=Enable the SATA controller to respond to PCI IO space access.

D11F0x08 Revision ID/Class Code

SATA controller has different values for Subclass Code and ProgramIF[7:0] depending on its operating mode.

Table 230: SATA Controller Subclass Code and ProgramIF Settings

Subclass Code	ProgramIF[7:0]	Controller Type
01	8Fh/8Ah	IDE
06	01	AHCI

Bits	Description
31:24	ClassCode: Class Code. Value: 1. This is a Mass-Storage Controller.
23:16	SubclassCode. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 01h. BIOS: See 2.15.3.1 . See Table 230 .
15	ProgramIF[7]: Master IDE Device. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. BIOS: See 2.15.3.1 . 1=Master IDE device in IDE mode. See Table 230 .
14:12	Reserved. ProgramIF[6:4] BIOS: See 2.15.3.1 .
11	ProgramIF[3]: Secondary Operating Mode Programmable. IF ((D11F0x40[SubclassCodeWriteEnable]) (D11F0x08[SubclassCode] == 01h)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. BIOS: See 2.15.3.1 . 1=Both secondary operating modes are supported in IDE. See Table 230
10	ProgramIF[2]: Secondary Operating Mode. IF ((D11F0x40[SubclassCodeWriteEnable] == 1) (D11F0x08[SubclassCode] == 01h)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. BIOS: See 2.15.3.1 . See Table 230
	<u>Bits</u> <u>Definition</u> 0b Compatibility Mode in IDE 1b Native PCI Mode in IDE
9	ProgramIF[1]: Primary Operating Mode Programmable. IF ((D11F0x40[SubclassCodeWriteEnable] == 1) (D11F0x08[SubclassCode] == 01h)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. BIOS: See 2.15.3.1 . 1=Both Primary operating modes are supported in IDE mode. See Table 230
8	ProgramIF[0]: Primary Operating Mode. IF ((D11F0x40[SubclassCodeWriteEnable] == 1) (D11F0x08[SubclassCode] == 01h)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. BIOS: See 2.15.3.1 . See Table 230 .
	<u>Bits</u> <u>Definition</u> 0b Compatibility Mode in IDE 1b Native PCI Mode in IDE
7:0	RevisionID: Revision ID. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 39h.

D11F0x0C Header Type Register

Bits	Description
31	BISTCapable: BIST Capable. Value: 0. 0=No HBA related BIST function.
30	StartBIST: Start BIST. Read-write. Reset: 0. Programming this bit has no effect.
29:28	Reserved.
27:24	CompletionCode: Completion Code. Read-only. Reset: 0. Indicates the completion code status of BIST. A non-zero value indicates a failure.
23	MultiFunctionDevice: Multi-function device. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. 0=Single-function device.
22:16	HeaderType: Header Type. Read-only. Reset: 0. Since the SATA host controller is a single-function device, this field contains a value of 00h.

15:11	MasterLatencyTimer: Master Latency Timer. Read-write. Reset: 0. Specifies, in units of PCI bus clocks, the time slice allowed to SATA host controller for burst transactions.
10:8	Reserved.
7:4	CacheLineSize: Cache Line Size. Read-write. Reset: 0.
3:0	Reserved.

D11F0x10 Primary IDE CS0 Base Address (BAR0)

Bits	Description
31:3	PrimaryIDECS0BaseAddress: Primary IDE CS0 Base Address. Read-write. Reset: 0. Base address[31:3] for Primary IDE Bus CS0 in IDE mode. This register is used for native mode only. See 3.26.3.2.1 [IDE Compatibility Mode and Native Mode (BAR0, BAR1, BAR2, BAR3) Registers]
2:1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 1. 1=Base address field in this register maps to the IO space.

D11F0x14 Primary IDE CS1 Base Address (BAR1)

Bits	Description
31:2	PrimaryIDECS1BaseAddress: Primary IDE CS1 Base Address. Read-write. Reset: 0. Base address[31:2] for Primary IDE Bus CS1 in IDE mode. This register is used for native mode only. See 3.26.3.2.1 [IDE Compatibility Mode and Native Mode (BAR0, BAR1, BAR2, BAR3) Registers]
1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 1. 1=Base address field in this register maps to the IO space.

D11F0x18 Secondary IDE CS0 Base Address (BAR2)

Bits	Description
31:3	SecondaryIDECS0BaseAddress: Secondary IDE CS0 Base Address. Read-write. Reset: 0. Base address[31:3] for Secondary IDE Bus CS0 in IDE mode. This register is used for native mode only. See 3.26.3.2.1 [IDE Compatibility Mode and Native Mode (BAR0, BAR1, BAR2, BAR3) Registers]
2:1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 1. 1=Base address field in this register maps to the IO space.

D11F0x1C Secondary IDE CS1 Base Address (BAR3)

Bits	Description
31:2	SecondaryIDECS1BaseAddress: Secondary IDE CS1 Base Address. Read-write. Reset: 0. Base address[31:2] for Secondary IDE Bus CS1 in IDE mode. This register is used for native mode only. See 3.26.3.2.1 [IDE Compatibility Mode and Native Mode (BAR0, BAR1, BAR2, BAR3) Registers]

1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 1. 1=Base address field in this register maps to the IO space.

D11F0x20 Bus Master Interface Register Base Address (BAR4)

Bits	Description
31:4	BusMasterInterfaceRegisterBaseAddress: Bus Master Interface Register Base Address. Read-write. Reset: 0. Base address[31:4] for Bus Master interface registers. See 3.26.3.2.2 [IDE Bus Master (BAR4) Registers] .
3:1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 1. 1=Base address field in this register maps to the IO space.

D11F0x24 AHCI Base Address (BAR5)

Bits	Description
31:10	AHCIBaseAddress: AHCI Base Address[31:10]. Read-write. Reset: 0. Specifies base address[31:10] of the AHCI control register space. See 3.26.3.3 [SATA Memory Mapped AHCI Registers] .
9:1	Reserved.
0	ResourceTypeIndicator: Resource Type Indicator. Value: 0. 0=Base address field in this register maps to the memory space.

D11F0x2C Subsystem ID and Subsystem Vendor ID

Bits	Description
31:16	SubsystemID: Subsystem ID. Write-once; read. Reset: 0.
15:0	SubsystemVendorID: Subsystem Vendor ID. Write-once; read. Reset: 0.

D11F0x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapabilitiesPointer: Capabilities Pointer. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 60h. The first pointer of the Capability block.

D11F0x3C Interrupt Line

Bits	Description
31:24	MaximumLatency: Maximum Latency. Value: 0. Specifies the Maximum Latency time required before the SATA controller can start an access as a bus-master.

23:16	MinimumGrant: Minimum Grant. Value: 0. Specifies the desired settings for how long of a burst the SATA controller needs. The value specifies a period of time in units of 1/4 microseconds.
15:8	InterruptPin: Interrupt Pin. Value: 1.
7:0	InterruptLine: Interrupt Line. Read-write. Reset: 0. Identifies which input on the interrupt controller this function's PCI interrupt request pin as specified in InterruptPin is routed to.

D11F0x40 Misc Control

Bits	Description								
23:16	<p>SataPortDisable[7:0]. IF (PortDisableLock==1) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. BIOS: See 2.15.3.6.1. This field is bit-significant where bit 0 controls port 0. For each bit, 1=The corresponding port is disabled, link/transport layer clocks are shut down.</p> <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>1=Port 0 disable</td> </tr> <tr> <td>[1]</td> <td>1=Port 1 disable</td> </tr> <tr> <td>[7:2]</td> <td>Reserved</td> </tr> </tbody> </table>	Bit	Definition	[0]	1=Port 0 disable	[1]	1=Port 1 disable	[7:2]	Reserved
Bit	Definition								
[0]	1=Port 0 disable								
[1]	1=Port 1 disable								
[7:2]	Reserved								
0	<p>SubclassCodeWriteEnable: Subclass Code Write Enable. Read-write. Reset: 0. BIOS: See 2.15.3.1, 2.15.3.8.2. 1=The following registers/fields are programmable:</p> <ul style="list-style-type: none"> • D11F0x08[ProgramIF[7:0]] • D11F0x08[SubclassCode] • D11F0x50[MMC] • D11F0x60[CapabilityNextPointer] • D11F0x70[CapabilityNextPointer] • SATAxF8 • SATAxFC • D11F0x00[DeviceID] • D11F0x04[CapabilitiesList] • D11F0x08[RevisionID] • D11F0x0C[MultiFunctionDevice] • D11F0x34[CapabilitiesPointer] • D11F0x50[CapabilityNextPointer] • D11F0xD0[FlrCap] • SATAx00[NP] • SATAx0C • SATAx10 • SATAx24 • SATAx1[C,4]0 								

D11F0x44 Watch Dog Control And Status

Bits	Description
31:24	Reserved. Read-write.
23:16	WatchdogCounter: Watchdog Counter. Read-write. Reset: 80h. BIOS: 20h. Specifies the timeout retry count for PCI downstream retries for SATA ports.
15:2	Reserved. Read-write.

1	WatchdogTimeoutStatus: Watchdog Timeout Status. Read; write-1-to-clear. Reset: 0. 1=The watchdog counter has expired for PCI downstream transaction, and as a result, the transaction was aborted.
0	WatchdogEnable: Watchdog Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable the watchdog counter for all the PCI downstream transactions for SATA ports. This is used to prevent system hang.

D11F0x50 MSI Control

Bits	Description
31:24	Reserved.
23	C64: MSI 64-bit Address. Read-only. Reset: 1. 1=64-bit address is supported.
22:20	MME: Multiple Message Enable. Read-write. Reset: 0. Indicates the number of messages the HBA should assert. If the value programmed into this field exceeds the MMC field in this register, the results are undetermined.
19:17	MMC: Multiple Message Capable. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 2h. BIOS: See 2.15.3.8.2. Indicates the number of messages the HBA wishes to assert.
16	MSIE: Message Signaled Interrupt Enable. Read-write. Reset: 0. 1=MSI is enabled and the traditional pins are not used to generate interrupts. 0=MSI operation is disabled and the traditional interrupt pins are used.
15:8	CapabilityNextPointer: Capability Next Pointer. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: D0h. BIOS: 0. Points to Advanced Feature (AF) capability.
7:0	CapabilityID: Capability ID. Read-only. Reset: 5h. Indicates this is MSI capability ID.

D11F0x54 MSI Address

Bits	Description
31:2	MsiAddress. Read-write. Reset: 0. Specifies the lower 32 bits of the system specified message address [31:2]. Always doubleword aligned.
1:0	Reserved.

D11F0x58 MSI Upper Address

Bits	Description
31:0	MsiUpperAddress. Read-write. Reset: 0. Specifies the upper 32 bits of the system specified message address [63:32].

D11F0x5C MSI Data

Bits	Description
31:16	Reserved.
15:0	MsiData. Read-write. Reset: 0. MSI Data.

D11F0x60 Power Management Capability

Bits	Description
31:27	PSUP: PME Support. Read-only. Reset: 8. Indicates the states the can generate PME#. Bit Definition [0] 1=PME# can be generated from D0. Not supported; only interrupts are used. [1] 1=PME# can be generated from D1. D1 is not supported. [2] 1=PME# can be generated from D2. D2 is not supported. [3] 1=PME# can be generated from D3hot state. [4] 1=PME# can be generated from D3cold state. D3cold is not supported.
26	D2S: D2 Support. Read-only. Reset: 0. 0=D2 state is not supported.
25	D1S: D1 Support. Read-only. Reset: 0. 0=D1 state is not supported.
24:22	AUXC: Aux Current. Value: 0. Reports the maximum Suspend well current required in D3COLD state.
21	DSI: Device Specific Initialization. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. 1=Device-specific initialization is required.
20	Reserved.
19	PMEC: PME Clock. Read-only. Reset: 0. 0=PCI clock is not required to generate PME#.
18:16	Version: Version. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 3h. Indicates support for Revision 1.2 of the PCI Power Management Specification. .
15:8	CapabilityNextPointer: Capability Next Pointer. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 70h. Points to SATA Capability.
7:0	CapabilityID: Capability ID. Read-only. Reset: 1. Indicates that this pointer is for PCI power management.

D11F0x64 PCI Power Management Control And Status

Bits	Description
31:16	Reserved.
15	PMES: PME Status. Read; Set-by-hardware; Write-1-to-clear. Cold reset: 0. This bit is set independent of PMEE according to PCI IPM. Writing '0' will have no effect. 1=PME# is generated by HBA.
14:9	Reserved.
8	PMEE: PME Enable. Read-write. Reset: 0. 1=The SATA controller asserts the PME# signal when PMES==1. 0=PME# assertion is disabled.
7:4	Reserved.

3	NSR: No soft reset. IF (D11F0x40[D3HotToD0PciResetDis]==1) THEN Value: 1. ELSE Value: 0. ENDIF. If the device transitions from D3hot to D0 due to system or bus segment reset and PME is supported and enabled, it returns to the device D0 state uninitialized with only PME context preserved regardless of this bit. 1=Devices do not perform an internal reset upon transitioning from D3hot to D0 because of Power-State commands; Configuration contexts is still preserved; Upon transitioning from D3hot to D0 Initialized state, no additional operating system intervention is required to preserve configuration context beyond writing the PowerState bits. 0=Devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits; Configuration context is lost when performing the soft reset; Upon transition from the D3hot to D0 state, full re-initialization sequence is needed to return the device to D0 initialized.												
2	Reserved.												
1:0	PS: Power State. Read-write. Reset: 0. This field is used both to determine the current power state of the HBA and to set a new power state. The D1 and D2 states are not supported. When the HBA is in D3hot state, the configuration space is available, but the register memory spaces are not; Additionally, interrupts are blocked. <table style="margin-left: 20px;"> <tr> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Definition</u></th> <th style="text-align: left;"><u>Bits</u></th> <th style="text-align: left;"><u>Definition</u></th> </tr> <tr> <td>00b</td> <td>D0 state.</td> <td>10b</td> <td>Reserved.</td> </tr> <tr> <td>01b</td> <td>Reserved.</td> <td>11b</td> <td>D3hot state.</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	D0 state.	10b	Reserved.	01b	Reserved.	11b	D3hot state.
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>										
00b	D0 state.	10b	Reserved.										
01b	Reserved.	11b	D3hot state.										

D11F0x70 Serial ATA Capability Register 0

Bits	Description
31:24	Reserved.
23:20	MajorRevision: Major Revision. Read-only. Reset: 1. Major revision number of the SATA Capability Pointer implemented.
19:16	MinorRevision: Minor Revision. Read-only. Reset: 0. Minor revision number of the SATA Capability Pointer implemented.
15:8	CapabilityNextPointer: Capability Next Pointer. IF (D11F0x40[SubclassCodeWriteEnable]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 50h. BIOS: See 2.15.3.8.2. Points to MSI capability.
7:0	CapabilityID: Capability ID. Read-only. Reset: 12h. Indicate that this pointer is for Serial ATA Capability.

D11F0x74 Serial ATA Capability Register 1

Bits	Description
31:24	Reserved.
23:4	BAROffset: BAR Offset. Read-only. Reset: 0. Indicates the offset into the BAR where the index/data pair are located in doubleword granularity.
3:0	BARLocation: BAR Location. Read-only. Reset: Fh. Indicates that index/data pair is implemented in doublewords directly following SATA Capability Register 1 in the PCI configuration space.

D11F0x78 IDP Index Register

Bits	Description
31:10	Reserved.
9:2	IDPIndex: IDP Index. Read-write. Reset: 0. This register selects the doubleword offset of the memory mapped AHCI register to be accessed.
1:0	Reserved.

D11F0x7C IDP Data Register

Bits	Description
31:0	IDPData: IDP Data. Read-write. Reset: 0h. This register is a window through which data is read or written to the memory mapped AHCI register pointed to by the D11F0x78 [IDP Index Register] . See 3.26.3.3 [SATA Memory Mapped AHCI Registers] . This is not a physical register, the default value for this field is 0000_0000h, once software programs a valid address in D11F0x78 [IDP Index Register] , it switches to the register value which IDPIndex pointing to. The AHCI registers can be accessed both through D11F0x24 [AHCI Base Address (BAR5)] and through this index/data pair.

D11F0x7C_x00 HBA Capabilities (CAP)

Bits	Description
31:0	Alias of SATAx00 .

D11F0x7C_x04 Global HBA Control (GHC)

Bits	Description
31:0	Alias of SATAx04 .

D11F0x7C_x08 Interrupt Status (IS)

Bits	Description
31:0	Alias of SATAx08 .

D11F0x7C_x0C Ports Implemented (PI)

Bits	Description
31:0	Alias of SATAx0C .

D11F0x7C_x10 AHCI Version (VS)

Bits	Description
31:0	Alias of SATAx10 .

D11F0x7C_x14 Command Completion Coalescing Control (CCC_CTL)

Bits	Description
31:0	Alias of SATAx14 .

D11F0x7C_x18 Command Completion Coalescing Ports (CCC_PORTS)

Bits	Description
31:0	Alias of SATAx18 .

D11F0x7C_x1C Enclosure Management Location (EM_LOC)

Bits	Description
31:0	Alias of SATAx1C .

D11F0x7C_x20 Enclosure Management Control (EM_CTL)

Bits	Description
31:0	Alias of SATAx20 .

D11F0x7C_x24 HBA Capabilities Extended (CAP2)

Bits	Description
31:0	Alias of SATAx24 .

D11F0x7C_x28 BIOS/OS Handoff Control and Status (BOHC)

Bits	Description
31:0	Alias of SATAx28 .

D11F0x7C_x1[8,0]0 Port 1,0 Command List Base Address (PxCLB)

Bits	Description
31:0	Alias of SATAx1[8,0]0 .

D11F0x7C_x1[8,0]4 Port 1,0 Command List Base Upper Address (PxCLBU)

Bits	Description
31:0	Alias of SATAx1[8,0]4 .

D11F0x7C_x1[8,0]8 Port 1,0 FIS Base Address (PxFB)

Bits	Description
31:0	Alias of SATAx1[8,0]8 .

D11F0x7C_x1[8,0]C Port 1,0 FIS Base Address Upper (PxFBU)

Bits	Description
31:0	Alias of SATAx1[8,0]C .

D11F0x7C_x1[9,1]0 Port 1,0 Interrupt Status (PxIS)

Bits	Description
31:0	Alias of SATAx1[9,1]0 .

D11F0x7C_x1[9,1]4 Port 1,0 Interrupt Enable (PxIE)

Bits	Description
31:0	Alias of SATAx1[9,1]4 .

D11F0x7C_x1[9,1]8 Port 1,0 Command and Status (PxCMD)

Bits	Description
31:0	Alias of SATAx1[9,1]8 .

D11F0x7C_x1[A,2]0 Port 1,0 Task File Data (PxTFD)

Bits	Description
31:0	Alias of SATAx1[A,2]0 .

D11F0x7C_x1[A,2]4 Port 1,0 Signature (PxSIG)

Bits	Description
31:0	Alias of SATAx1[A,2]4 .

D11F0x7C_x1[A,2]8 Port 1,0 Serial ATA Status (PxSSTS)

Bits	Description
31:0	Alias of SATAx1[A,2]8 .

D11F0x7C_x1[A,2]C Port 1,0 Serial ATA Control (PxSCTL)

Bits	Description
31:0	Alias of SATAx1[A,2]C .

D11F0x7C_x1[B,3]0 Port 1,0 Serial ATA Error (PxSERR)

Bits	Description
31:0	Alias of SATAx1[B,3]0 .

D11F0x7C_x1[B,3]4 Port 1,0 Serial ATA Active (PxSACT)

Bits	Description
31:0	Alias of SATAx1[B,3]4 .

D11F0x7C_x1[B,3]8 Port 1,0 Command Issue (PxCI)

Bits	Description
31:0	Alias of SATAx1[B,3]8 .

D11F0x7C_x1[B,3]C Port 1,0 SNotification (PxSNTF)

Bits	Description
31:0	Alias of SATAx1[B,3]C .

D11F0x7C_x1[C,4]0 Port 1,0 FIS-based Switching Control (PxFBS)

Bits	Description
31:0	Alias of SATAx1[C,4]0 .

D11F0x80 PHY Core Control 1BIOS: See [2.15.3.4](#).

Bits	Description
31:9	Reserved. Read-write.

8	WRALL: Write Settings To All Ports. Write-only. Reset: 0. Allow software to simultaneously update all ports when writing to the port dependent PHY fine-tune setting registers: D11F0x95 , D11F0x96 , D11F0x98 , D11F0x9C , D11F0xA0 , D11F0xA4 , D11F0xF0 . 1=Writes to the PHY fine tune setting registers update all ports with the same value at the same time. 0=Writes to the PHY fine tune setting registers only update individual port selected by PN.												
7:6	Reserved. Read-write.												
5:4	GEN: Generation Speed. Read-write. Reset: 1. Selects the Generation Speed when software reads/writes to the generation speed dependent PHY fine-tune setting registers: D11F0x94 , D11F0x98 , D11F0x9C , D11F0xA8[15:8] , D11F0xD8 .												
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Reserved</td> <td>10b</td> <td>Gen 2</td> </tr> <tr> <td>01b</td> <td>Gen 1</td> <td>11b</td> <td>Gen 3</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	Reserved	10b	Gen 2	01b	Gen 1	11b	Gen 3
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>										
00b	Reserved	10b	Gen 2										
01b	Gen 1	11b	Gen 3										
3	Reserved. Read-write.												
2:0	PN: PHY Fine Tune Target Port. Read-write. Reset: 0. Selects the port when software reads/writes to the port dependent PHY fine-tune setting registers: D11F0x95 , D11F0x96 , D11F0x98 , D11F0x9C , D11F0xA0 , D11F0xA4 , D11F0xF0 .												
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Port 0 is selected</td> </tr> <tr> <td>01b</td> <td>Port 1 is selected</td> </tr> <tr> <td>7h-2h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	Port 0 is selected	01b	Port 1 is selected	7h-2h	Reserved				
<u>Bits</u>	<u>Definition</u>												
00b	Port 0 is selected												
01b	Port 1 is selected												
7h-2h	Reserved												

D11F0x84 PHY Core Control 2

Bits	Description						
31	Reserved.						
30	DShutDwn: PHY PLL Dynamic Shutdown. Read-write. Reset: 1. BIOS: See 2.22.3.7.4 . Turn on/off the advanced power saving feature.						
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>No PLL dynamic shutdown; SATA PHY PLL consumes power even though all the ports are inactive.</td> </tr> <tr> <td>1b</td> <td>SATA PHY PLL will dynamically shutdown when all the ports are inactive. This inactivity includes Slumber Mode and port disable, but excludes Partial Mode.</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0b	No PLL dynamic shutdown; SATA PHY PLL consumes power even though all the ports are inactive.	1b	SATA PHY PLL will dynamically shutdown when all the ports are inactive. This inactivity includes Slumber Mode and port disable, but excludes Partial Mode.
<u>Bits</u>	<u>Definition</u>						
0b	No PLL dynamic shutdown; SATA PHY PLL consumes power even though all the ports are inactive.						
1b	SATA PHY PLL will dynamically shutdown when all the ports are inactive. This inactivity includes Slumber Mode and port disable, but excludes Partial Mode.						
26	S5ShadowLdDis: S5 Shadow Register Reload Disable. Read-write. Reset: 1. BIOS: See 2.15.3.7 . 1=Not to load S5 shadow registers back to PHY related control registers when S0 domain loses power other than cold boot. 0=Turn on shadow register reloading.						
2	RSTB: PHY Global Reset. Read-write. Reset: 1. BIOS: See 2.15.3.5 . 0=Reset all port logic in PHY.						

D11F0x88 PHY Global Control 1

Bits	Description
31:28	PllVcoTune: PLL VCO Range Select Bits. Read-write. Reset: 0. BIOS: See 2.15.3.3 . PLL VCO range select bits.

D11F0x8C PHY Global Control 2

Bits	Description
7:0	PLL_CLKF: PLL Clock Divider Setting. Read-write. Reset: 7Dh. BIOS: See 2.15.3.5 . Feedback clock divider setting. (Default: 6 GHz/48 MHz = 7Dh).

D11F0x98 PHY Fine Tune PortX GenX Setting

This register is both port and generation speed sensitive. Software must program D11F0x80[PN] to select port and D11F0x80[GEN] to select generation speed before accessing this register.

Bits	Description																
16:12	<p>TX_SLEW_CNTRL: Transmitter Output Slew Control. Read-write. Reset: IF (D11F0x80[GEN]==1) THEN 3h. ELSEIF (D11F0x80[GEN]==2) THEN Fh. ELSEIF (D11F0x80[GEN]==3) THEN Fh. ENDIF. BIOS: See 2.15.3.4.</p> <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[4]</td> <td>0. Reserved</td> </tr> <tr> <td>[3:2]</td> <td>00b=CML driver on with 1K res. 01b=CML driver on with 2K res. 1xb=Tri-state pre-driver on.</td> </tr> <tr> <td>[1:0]</td> <td>Always set to 11b.</td> </tr> </tbody> </table> <p>Modification to this field should be limited to the following only. Values other than specified cause intermittent results.</p> <table> <thead> <tr> <th><u>Generation Speed</u></th> <th><u>Allowable Setting</u></th> </tr> </thead> <tbody> <tr> <td>Gen 1</td> <td>3h</td> </tr> <tr> <td>Gen 2</td> <td>Fh</td> </tr> <tr> <td>Gen 3</td> <td>Fh</td> </tr> </tbody> </table> <p>Rise/Fall time is controlled by the combined force of TX_DRV_STR, TX_SLEW_CNTRL, and TX_DEEMPH_STR. Depending on the channel loss, the value of TX_SLEW_CNTRL and TX_DEEMPH_STR may have to be adjusted based on package and board design.</p>	<u>Bit</u>	<u>Definition</u>	[4]	0. Reserved	[3:2]	00b=CML driver on with 1K res. 01b=CML driver on with 2K res. 1xb=Tri-state pre-driver on.	[1:0]	Always set to 11b.	<u>Generation Speed</u>	<u>Allowable Setting</u>	Gen 1	3h	Gen 2	Fh	Gen 3	Fh
<u>Bit</u>	<u>Definition</u>																
[4]	0. Reserved																
[3:2]	00b=CML driver on with 1K res. 01b=CML driver on with 2K res. 1xb=Tri-state pre-driver on.																
[1:0]	Always set to 11b.																
<u>Generation Speed</u>	<u>Allowable Setting</u>																
Gen 1	3h																
Gen 2	Fh																
Gen 3	Fh																

D11F0x9C PortX Setting 2

Bits	Description																				
11:9	<p>RX_SQDET_TH: Squelch Detector Threshold Control. Read-write. Reset: IF (D11F0x80[GEN]==1) THEN 4h. ELSEIF (D11F0x80[GEN]==2) THEN 4h. ELSEIF (D11F0x80[GEN]==3) THEN 4h. ENDIF. BIOS: See 2.15.3.4. Specifies the squelch detector threshold adjustment.</p> <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0</td> <td>100b</td> <td>+25 mV</td> </tr> <tr> <td>001b</td> <td>+6 mV</td> <td>101b</td> <td>+30 mV</td> </tr> <tr> <td>010b</td> <td>-16 mV</td> <td>110b</td> <td>+14 mV</td> </tr> <tr> <td>011b</td> <td>-7 mV</td> <td>111b</td> <td>+20 mV</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	000b	0	100b	+25 mV	001b	+6 mV	101b	+30 mV	010b	-16 mV	110b	+14 mV	011b	-7 mV	111b	+20 mV
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>																		
000b	0	100b	+25 mV																		
001b	+6 mV	101b	+30 mV																		
010b	-16 mV	110b	+14 mV																		
011b	-7 mV	111b	+20 mV																		

D11F0xB4 PortX BIST Control/Status

Software must program D11F0xB7 [PortX BIST Port Select] to select the port before reading from/writing to

this register.

Bits	Description																										
13:12	<p>PortXLinkBistSpeed: PortX Link BIST Speed. Read-write. Reset: 0. PHY PortX speed control for Link BIST mode.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Gen 1</td> <td>10b</td> <td>Gen 2</td> </tr> <tr> <td>01b</td> <td>Gen 1</td> <td>11b</td> <td>Gen 3</td> </tr> </tbody> </table> <p>When D11F0xC8[IoBistOperationMode]==1 and D11F0xC8[IoBistAtePorts]==1, this field is controlled by D11F0xC8[IoBistAteGenSpeed]. When D11F0xC8[IoBistOperationMode]==0 or D11F0xC8[IoBistAtePorts]==0, this field returns to its original value.</p>	Bits	Definition	Bits	Definition	00b	Gen 1	10b	Gen 2	01b	Gen 1	11b	Gen 3														
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00b	Gen 1	10b	Gen 2																								
01b	Gen 1	11b	Gen 3																								
5:2	<p>PortXLinkBistPattern: PortX Link BIST Pattern. Read-write. Reset: 0. When D11F0xC8[IoBistOperationMode] is set and D11F0xC8[IoBistAtePorts] is set, this field is controlled by D11F0xC8[IoBistPrbs10HftpTransmission] and only 1000b or 1001b are selected. Deasserting D11F0xC8[IoBistOperationMode] or D11F0xC8[IoBistAtePorts] returns this field to its original value.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern).</td> </tr> <tr> <td>0001b</td> <td>D10.2 Highest frequency (for Rx eye diagram measurement).</td> </tr> <tr> <td>0010b</td> <td>SYNC primitive (for Rx eye diagram measurement).</td> </tr> <tr> <td>0011b</td> <td>Lone Bit Pattern (LBP).</td> </tr> <tr> <td>0100b</td> <td>Mid Frequency Test Pattern (MFTP).</td> </tr> <tr> <td>0101b</td> <td>20-bit data pattern, programmed at D11F0xCC.</td> </tr> <tr> <td>0110b</td> <td>Force Far End Re-timed Loop Back Mode in HBA.</td> </tr> <tr> <td>0111b</td> <td>Forced T-mode enable. T-mode is defined as Far end transmit only mode without Device initiating. In T-mode, the BIST pattern generated is based on the values programed in D11F0xBC and D11F0xC0.</td> </tr> <tr> <td>1000b</td> <td>HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding.</td> </tr> <tr> <td>1001b</td> <td>PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding.</td> </tr> <tr> <td>1010b</td> <td>Forced Far End Analog Loop Back Mode. HBA does not need BIST Activate FIS from device to be able to run in this mode.</td> </tr> <tr> <td>1111b-1011b</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0000b	Pseudo-random with ALIGN insertion (when Error Count is used, must choose this pattern).	0001b	D10.2 Highest frequency (for Rx eye diagram measurement).	0010b	SYNC primitive (for Rx eye diagram measurement).	0011b	Lone Bit Pattern (LBP).	0100b	Mid Frequency Test Pattern (MFTP).	0101b	20-bit data pattern, programmed at D11F0xCC .	0110b	Force Far End Re-timed Loop Back Mode in HBA.	0111b	Forced T-mode enable. T-mode is defined as Far end transmit only mode without Device initiating. In T-mode, the BIST pattern generated is based on the values programed in D11F0xBC and D11F0xC0 .	1000b	HFTP pattern directly at the PHY-CORE interface without going through 8b/10b encoding.	1001b	PRBS10 pattern directly at the PHY-CORE interface without going through 8b/10b encoding.	1010b	Forced Far End Analog Loop Back Mode. HBA does not need BIST Activate FIS from device to be able to run in this mode.	1111b-1011b	Reserved.
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0	<p>PortXLinkBistEnable: PortX Link BIST Enable. Read-write. Reset: 0. 1=PortX is in link BIST mode overriding normal operation and device OOB is ignored by host. To resume normal operation, this bit needs to be cleared to 0 and a port reset is required. When D11F0xC8[IoBistOperationMode] is set and D11F0xC8[IoBistAtePorts] is set, this bit is set to 1 automatically. Deasserting D11F0xC8[IoBistOperationMode] or D11F0xC8[IoBistAtePorts] returns this field to its original value. See D11F0xB7 for details on selection port.</p>																										

D11F0xB7 PortX BIST Port Select

Bits	Description
------	-------------

7:2	Reserved.
1:0	PortXBistPortSelect: PortX BIST Port Select. Read-write. Reset: 0. This register is bit significant. When the bit is 1, it indicates the port that software will read from/write to during link BIST. For reads, the port is determined by the last significant bit with value 1 in this field. For writes, the port(s) is determined by the any bit with value 1 in this field. This register must be programmed before reading back from D11F0xB0 , or writing to/reading from D11F0xB4 to avoid reading from/written to an un-expected port.

D11F0xBC T-Mode BIST Transit Pattern DW1

Bits	Description
31:0	TmodeBistTransitPatternDW1: T-mode BIST Transit Pattern DW1. Read-write. Reset: 0. Transit Pattern DW1. See D11F0xB4[PortXLinkBistPattern] for T-mode enable.

D11F0xC0 T-Mode BIST Transit Pattern DW2

Bits	Description
31:0	TmodeBistTransitPatternDW2: T-mode BIST Transit Pattern DW2. Read-write. Reset: 0. Transit Pattern DW2. See D11F0xB4[PortXLinkBistPattern] for T-mode enable.

D11F0xC4 T-Mode BIST Transit Control

Bits	Description
31:3	Reserved. Read-write.
2	TmodePbit: T-mode P bit. Read-write. Reset: 0. The transmit primitives bit.
1	TmodeSbit: T-mode S bit. Read-write. Reset: 0. Scrambling Bypass.
0	TmodeAbit: T-mode A bit. Read-write. Reset: 0. ALIGN primitives bypass mode.

D11F0xD0 Advanced Features Capability Register 0

Bits	Description
31:26	Reserved.
25	FlrCap. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. 1=Indicates support for Function Level Reset (FLR).
24	TpCap. Read-only. Reset: 1. 1=Indicates support for the Transactions Pending (TP) bit (D11F0xD4[TP]). TP must be supported if FLR is supported.
23:16	Length. Read-only. Reset: 6h. Advanced Feature (AF) Structure Length (Bytes).
15:8	NextPtr: Next pointer. Read-only. Reset: 0. 0=End of list.
7:0	CapID: Capability ID. Read-only. Reset: 13h. Identifies the function being Advanced Feature (AF) capable.

D11F0xD4 Advanced Features Capability Register 1

Bits	Description
15:9	Reserved.
8	TP: Transactions Pending. Read-only; updated-by-hardware. Reset: 0. 1=The function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with retry. 0=All non-posted transactions have been completed.
7:1	Reserved.
0	InitiateFlr. Read-write; RAZ. Reset: 0. 1=Initiate Function Level Reset (FLR). FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there.

D11F0xE0 PCI Target Control TimeOut Counter

Bits	Description
15:8	Reserved.
7:0	Count: PCI Target Control Timeout Count. Read-write. Reset: 80h. This field specifies the PCI target control timeout count used to clear any stale target commands to the host controller. Granularity is 15.5 us (Timeout Counter = Count * 15.5 us). The counter is disabled if the count is programmed to 0.

3.26.3.2 SATA IO Registers

3.26.3.2.1 IDE Compatibility Mode and Native Mode (BAR0, BAR1, BAR2, BAR3) Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention.

Compatibility Mode is selected by D11F0x08[ProgramIF[0], ProgramIF[2]]==0 respectively. In Compatibility Mode the IO address is forced to the legacy compatible address. The same group of registers can be specified as Native Mode by D11F0x08[ProgramIF[0], ProgramIF[2]]==1 respectively. In Native Mode, the IO address is specified by D11F0x10, D11F0x14, D11F0x18 and D11F0x1C (BAR0, BAR1, BAR2, BAR3).

Table 231: IDE Compatibility Mode and Native Mode Address Mapping

Compatibility Mode: Interface, IO Address	Native Mode: Interface, BAR+Offset	Read Function	Write Function	Register
Primary, 1F0h	Primary, D11F0x10+0	Data (16 bit)	Data (16 bit)	IDE[0]_x00
Primary, 1F1h	Primary, D11F0x10+1	Error	Feature	IDE[0]_x01
Primary, 1F2h	Primary, D11F0x10+2	Sector Count	Sector Count	IDE[0]_x02
Primary, 1F3h	Primary, D11F0x10+3	Sector Number	Sector Number	IDE[0]_x03
Primary, 1F4h	Primary, D11F0x10+4	Cylinder Low	Cylinder Low	IDE[0]_x04
Primary, 1F5h	Primary, D11F0x10+5	Cylinder High	Cylinder High	IDE[0]_x05
Primary, 1F6h	Primary, D11F0x10+6	Drive/Head	Drive/Head	IDE[0]_x06
Primary, 1F7h	Primary, D11F0x10+7	Status	Command	IDE[0]_x07
Primary, 3F6h	Primary, D11F0x14+2	Alternate Status	Device Control	IDEA[0]_x02

Table 231: IDE Compatibility Mode and Native Mode Address Mapping

Compatibility Mode: Interface, IO Address	Native Mode: Interface, BAR+Offset	Read Function	Write Function	Register
Secondary, 170h	Secondary, D11F0x18+0	Data (16 bit)	Data (16 bit)	IDE[1]_x00
Secondary, 171h	Secondary, D11F0x18+1	Error	Feature	IDE[1]_x01
Secondary, 172h	Secondary, D11F0x18+2	Sector Count	Sector Count	IDE[1]_x02
Secondary, 173h	Secondary, D11F0x18+3	Sector Number	Sector Number	IDE[1]_x03
Secondary, 174h	Secondary, D11F0x18+4	Cylinder Low	Cylinder Low	IDE[1]_x04
Secondary, 175h	Secondary, D11F0x18+5	Cylinder High	Cylinder High	IDE[1]_x05
Secondary, 176h	Secondary, D11F0x18+6	Drive/Head	Drive/Head	IDE[1]_x06
Secondary, 177h	Secondary, D11F0x18+7	Status	Command	IDE[1]_x07
Secondary, 376h	Secondary, D11F0x1C+2	Alternate Status	Device Control	IDEA[1]_x02

IDE[1:0]x00 IDE DATA

Bits	Description
15:0	Data. Read-write. Reset: 0. Accesses to this register must be 16 bit. Addressing as an 8 bit register will result in IDE[1:0]x00[15:8] aliasing to IDE[1:0]x01 .

IDE[1:0]x01 Feature and Error

Bits	Description
7:0	FeatureError. Read-write. Reset: 0.

IDE[1:0]x02 Sector Count

Bits	Description
7:0	SectorCount. Read-write. Reset: 0.

IDE[1:0]x03 Sector Number

Bits	Description
7:0	SectorNumber. Read-write. Reset: 0.

IDE[1:0]x04 Cylinder Low

Bits	Description
7:0	CylinderLow. Read-write. Reset: 0.

IDE[1:0]x05 Cylinder High

Bits	Description
7:0	CylinderHigh. Read-write. Reset: 0.

IDE[1:0]x06 Drive and Head

Bits	Description
7:0	DriveHead. Read-write. Reset: 0.

IDE[1:0]x07 Command and Status

Bits	Description
7:0	CommandStatus. Read-write. Reset: 0.

IDEA[1:0]x02 Device Control and Alternate Status

Bits	Description
7:0	DevCtrlAltStatus. Read-write. Reset: 0.

3.26.3.2.2 IDE Bus Master (BAR4) Registers

See section 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention.

IDE_BMX0[8,0] Bus Master IDE Command

Primary and Secondary Bus Master IDE Command registers.

Bits	Description
7:4	Reserved.
3	BusMasterReadWrite: Bus Master Read/Write. Read-write. Reset: 0. This bit should not change during Bus Master transfer cycle, even if terminated by Bus Master IDE Stop. <u>Bits</u> <u>Definition</u> 0b Memory to IDE. 1b IDE to memory.
2:1	Reserved.
0	BusMasterIDEStartStop: Bus Master IDE Start/Stop. Read-write. Reset: 0. This bit will not be reset by interrupt from IDE device. This must be reset by software (device driver). <u>Bits</u> <u>Definition</u> 0b Stop. 1b Start.

IDE_BMx0[A,2] Bus-master IDE Status

Primary and Secondary Bus Master IDE Status registers.

Bits	Description						
7	SimplexOnly: Simplex Only. Value: 0.						
6	SlaveDeviceDMACapable: Slave Device DMA Capable. Read-write. Reset: 0. Device 1 (Slave) DMA capable.						
5	MasterDeviceDMACapable: Master Device DMA Capable. Read-write. Reset: 0. Device 0 (Master) DMA capable.						
4:3	Reserved.						
2	IDEInterrupt: IDE Interrupt. Read-write. Reset: 0. 1=An IDE device has asserted its interrupt line. IRQ14 is used for the primary channel, and IRQ15 is used for the secondary channel. If the Interrupt Status bit is set to 0, by writing a 1 to this bit while the interrupt line is still at the active level, this bit will remain 0 until another assertion edge is detected on the interrupt line.						
1	BusMasterDMAError: Bus Master DMA Error. Read; write-1-to-clear. Reset: 0. 1=The IDE host controller encounters a target abort, master abort, or parity error while transferring data on the PCI bus.						
0	BusMasterActive: Bus Master Active. Read-only; updated-by-hardware. Reset: 0. Bus Master IDE active. This bit is set to 1 when IDE_BMx0[8,0][0]==1 . This bit is set to 0 when IDE_BMx0[8,0][0]==0 or the last transfer for a region is performed. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0b</td> <td>Not active.</td> </tr> <tr> <td>1b</td> <td>Active.</td> </tr> </tbody> </table>	Bits	Definition	0b	Not active.	1b	Active.
Bits	Definition						
0b	Not active.						
1b	Active.						

IDE_BMx0[C,4] Descriptor Table Pointer

Primary and Secondary Bus Master IDE Descriptor Table Pointer register.

Bits	Description
31:2	DescriptorTableBaseAddress: Descriptor Table Base Address. Read-write. Reset: 0. These bits correspond to Address [31:2].
1:0	Reserved.

3.26.3.3 SATA Memory Mapped AHCI Registers

These are the AHCI memory mapped registers. The base address is defined by [D11F0x24 \[AHCI Base Address \(BAR5\)\]](#). See section [3.1 \[Register Descriptions and Mnemonics\]](#) for a description of the register naming convention.

3.26.3.3.1 Generic Host Control Registers

SATAx00 HBA Capabilities (CAP)

Bits	Description												
31	S64A: Supports 64-bit Addressing. Read-only. Reset: 1. Indicates whether HBA can access 64-bit data structures. 1=HBA will make the 32-bit upper bits of the port DMA Descriptor, the PRD Base, and each PRD entry read/write. 0=These bits are read-only and treated as 0s by the HBA.												
30	SNCQ: Supports Native Command Queuing. Read-only. Reset: 1. Indicates whether HBA supports Serial ATA native command queuing. 1=HBA can handle DMA Setup FISes natively, and can handle the auto-activate optimization through that FIS. 0=Native command queuing is not supported and software should not issue any native command queuing commands. Writing SATAxFC[CFG_CAP_SNCQ] updates this bit.												
29	SSNTF: Supports SNotification Register. Read-only. Reset: 1. 1=HBA supports the SATAx1[B,3]C [Port 1,0 SNotification (PxSNTF)] register and its associated functionality. 0=HBA does not support the SATAx1[B,3]C [Port 1,0 SNotification (PxSNTF)] register and its associated functionality. Writing SATAxFC[CFG_CAP_SSNTF] updates this bit.												
28	SMPS: Supports Mechanical Presence Switch. Read-only. Reset: 1. 1=HBA supports mechanical presence switches on its ports for use in hot plug operations. 0=This function is not supported. This value is loaded by the BIOS prior to OS initialization. Writing SATAxFC[CFG_CAP_SMPS] updates this bit.												
27	SSS: Supports Staggered Spin-up. Read-only. Reset: 0. 1=HBA supports staggered spin-up on its ports, for use in balancing power spikes. 0=This function is not supported. This value is loaded by the BIOS prior to OS initialization. Writing SATAxFC[CFG_CAP_SSS] updates this bit.												
26	SALP: Supports Aggressive Link Power Management. Read-only. Reset: 1. 1=HBA can support auto-generating link requests to the Partial or Slumber states when there are no commands to process. 0=This function is not supported and software will treat the SATAx1[9,1]8[ALPE] and SATAx1[9,1]8[ASP] bits as reserved. Writing SATAxFC[CFG_CAP_SALP] updates this bit.												
25	SAL: Supports Activity LED. Read-only. Reset: 1. 1=HBA supports a single activity indication output pin; This pin can be connected to an LED on the platform to indicate device activity on any drive. 0=This function is not supported.												
24	SCLO: Supports Command List Override. Read-only. Reset: 1. 1=HBA supports the SATAx1[9,1]8[CLO] bit and its associated function. 0=HBA is not capable of clearing the BSY and DRQ bits in the Status register in order to issue a software reset if these bits are still set from a previous operation.												
23:20	ISS: Interface Speed Support. Read-only. Reset: 3h. Indicates the maximum speed HBA can support on its ports. Writing SATAxFC[CFG_CAP_MAXGEN] updates this bit. These encodings match the system software programmable SATAx1[A,2]C[SPD] field. Values are: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Reserved</td> </tr> <tr> <td>0001b</td> <td>Gen1 (1.5 Gbps)</td> </tr> <tr> <td>0010b</td> <td>Gen1 and Gen2 (3 Gbps)</td> </tr> <tr> <td>0011b</td> <td>Gen1 and Gen2 and Gen3 (6 Gbps)</td> </tr> <tr> <td>1111b-0100b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	0000b	Reserved	0001b	Gen1 (1.5 Gbps)	0010b	Gen1 and Gen2 (3 Gbps)	0011b	Gen1 and Gen2 and Gen3 (6 Gbps)	1111b-0100b	Reserved
Bits	Definition												
0000b	Reserved												
0001b	Gen1 (1.5 Gbps)												
0010b	Gen1 and Gen2 (3 Gbps)												
0011b	Gen1 and Gen2 and Gen3 (6 Gbps)												
1111b-0100b	Reserved												
19	SNZO: Supports Non-Zero DMA Offsets. Read-only. Reset: 0. 0=Indicates HBA can not support non-zero DMA offsets for DMA Setup FISes. Writing SATAxFC[CFG_CAP_SNZO] updates this bit.												

18	SAM: Supports AHCI mode only. Read-only. Reset: 0. The SATA controller may optionally support AHCI access mechanisms only. 0=Indicates that in addition to the native AHCI mechanism (via AHCI BAR5), the SATA controller implements a legacy, task-file based register interface such as SFF-8038i. 1=Indicates the SATA controller does not implement a legacy, task-file based register interface.
17	SPM: Supports Port Multiplier. Read-only. Reset: 1. Indicates whether HBA can support a port multiplier. 1=A port multiplier using command-based switching is supported. 0=A port multiplier is not supported, and a port multiplier may not be attached to this HBA. Writing SATAxFC[CFG_CAP_SPM] updates this bit.
16	FBSS: FIS-based Switching Supported. Read-only. Reset: 1. 1=Indicates HBA supports Port Multiplier FIS-based switching. 0=Indicates HBA does not support FIS-based switching. Writing SATAxFC[CFG_CAP_FBSS] updates this bit.
15	PMD: PIO Multiple DRQ Block. Read-only. Reset: 1. 0=HBA only supports single DRQ block data transfers for the PIO command protocol. 1=HBA supports multiple DRQ block data transfers for the PIO command protocol.
14	SSC: Slumber State Capable. Read-only. Reset: 1. Indicates whether HBA can support transitions to the Slumber state. 0=Software must not allow the HBA to initiate transitions to the Slumber state via aggressive link power management nor the SATAx1[9,1]8[ICC] field in each port, and the SATAx1[A,2]C[IPM] field in each port must be programmed to disallow device initiated Slumber requests. 1=HBA and device initiated Slumber requests can be supported. Writing SATAxFC[CFG_CAP_SSC] updates this bit.
13	PSC: Partial State Capable. Read-only. Reset: 1. Indicates whether HBA can support transitions to the Partial state. 0=Software must not allow HBA to initiate transitions to the Partial state via aggressive link power management nor the SATAx1[9,1]8[ICC] field in each port, and the SATAx1[A,2]C[IPM] field in each port must be programmed to disallow device initiated Partial requests. 1=HBA and device initiated Partial requests can be supported. Writing SATAxFC[CFG_CAP_PSC] updates this bit.
12:8	NCS: Number of Command Slots. Read-only. Reset: 1Fh. 0's based value indicate the number of command slots per port supported by this HBA. A minimum of 1 and a maximum of 32 slots per port can be supported. The same number of command slots is available on each implemented port. Writing SATAxFC[CFG_CAP_NCS] updates this bit.
7	CCCS: Command Completion Coalescing Supported. Read-only. Reset: 1. 0=Indicates that HBA does not support command completion coalescing and SATAx14 [Command Completion Coalescing Control (CCC_CTL)] and SATAx18 [Command Completion Coalescing Ports (CCC_PORTS)] are not implemented. 1=Indicates that HBA supports command completion coalescing and HBA has implemented the SATAx14 [Command Completion Coalescing Control (CCC_CTL)] and the SATAx18 [Command Completion Coalescing Ports (CCC_PORTS)] global HBA registers. Writing SATAxFC[CFG_CAP_CCCS] updates this bit.
6	EMS: Enclosure Management Supported. Read-only. Reset: 0b. 1=Indicates that HBA supports enclosure management and has implemented the SATAx1C [Enclosure Management Location (EM_LOC)] and SATAx20 [Enclosure Management Control (EM_CTL)] global HBA registers. 0=Indicates that the HBA does not support enclosure management and the SATAx1C [Enclosure Management Location (EM_LOC)] and SATAx20 [Enclosure Management Control (EM_CTL)] global HBA registers are not implemented. Writing SATAxFC[CFG_CAP_EMS] updates this bit.

5	SXS: Supports External SATA. Read-only. Reset: 0. 1=Indicates that HBA has one or more Serial ATA ports that have a signal-only connector (i.e. power is not part of that connector) that is externally accessible. 0=Indicates that the HBA has no Serial ATA ports that have a signal-only connector externally accessible. If this bit is set to 1, software may refer to the SATAx1[9,1]8[ESP] bit to determine whether a specific port has its signal connector externally accessible as a signal-only connector. Writing SATAxFC[CFG_CAP_SXS] updates this bit.
4:0	NP: Number of Ports. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 3h. 0's based value indicating the maximum number of ports supported by the HBA silicon. A maximum of 32 ports can be supported. A value of 0, indicating one port, is the minimum requirement. Note that the number of ports indicated in this field may be more than the number of ports indicated in the SATAx0C[PI] .

SATAx04 Global HBA Control (GHC)

Bits	Description
31	AE: AHCI Enable. Read-write. Reset: 0. 1=Indicates that communication to HBA shall be via AHCI mechanisms. 0=Software shall only communicate with HBA using legacy mechanisms; FISes are not posted to memory, and no commands are sent via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms and AHCI to know when the HBA is running under an AHCI driver. Software shall set this bit to 1 before accessing other AHCI registers.
30:3	Reserved.
2	MRSM: MSI Revert to Single Message. Read-only. Reset: 0. 1=HBA requested more than one MSI vector but has reverted to using the first vector only. 0=HBA has not reverted to single MSI mode (i.e., hardware is already in single MSI mode, software has allocated the number of messages requested, or hardware is sharing interrupt vectors if D11F0x50[MME]<D11F0x50[MMC]). HBA may revert to single MSI mode when the number of vectors allocated by the host is less than the number requested. This bit shall only be set to 1 when the following conditions hold: <ul style="list-style-type: none"> • D11F0x50[MSIE]=1 (MSI is enabled) • D11F0x50MMC>0 (multiple messages requested) • D11F0x50MME>0 (more than one message allocated) • D11F0x50MME]!=D11F0x50[MMC] (messages allocated not equal to number requested) When this bit is set to 1, single MSI mode operation is in use and software is responsible for clearing bits in the IS register to clear interrupts. This bit shall be cleared to 0 by hardware when any of the four conditions stated is false. This bit is also cleared to 0 when D11F0x50[MSIE] = 1 and D11F0x50[MME] = 0h . In this case, hardware has been programmed to use single MSI mode, and is not “reverting” to that mode.
1	IE: Interrupt Enable. Read-write. Reset: 0. This global bit enables interrupts from HBA. 0>All interrupt sources from all ports are disabled. 1=Interrupts are enabled.
0	HR: HBA Reset. Read; write-1-only; cleared-by-hardware. Reset: 0. When set by software, this bit causes an internal reset of HBA. All state machines that relate to data transfers and queuing shall return to an idle condition, and all ports shall be re-initialized via COMRESET (if staggered spin-up is not supported). If staggered spin-up is supported, then it is the responsibility of software to spin-up each port after the reset has completed. When HBA has performed the reset action, it shall reset this bit to 0. For a description on which bits are reset when this bit is set, see AHCI spec, section 10.4.3.

SATAx08 Interrupt Status (IS)

Bits	Description
31:0	IPS: Interrupt Pending Status. Read; write-1-to-clear. Reset: 0. This register is bit significant where bit 0 corresponds to port 0. For each bit, 1=The corresponding port has an interrupt pending. Software can use this information to determine which ports require service after an interrupt. The IPS[X] bit is only defined for ports that are implemented or for the command completion coalescing interrupt defined by SATAx14[INT] . All other bits are reserved. <u>Bit</u> <u>Definition</u> [0] Port 0 has pending interrupt [1] Port 1 has pending interrupt ... [31] Port 31 has pending interrupt

SATAx0C Ports Implemented (PI)

Bits	Description
31:0	PI[31:0]: Port Implemented. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 3h. This register is bit significant. For each bit, 1=The corresponding port is available for software to use. 0=The port is not available for software to use. The maximum number of bits set to 1 shall not exceed SATAx00[NP] + 1, although the number of bits set in this register may be fewer than SATAx00[NP] + 1. At least one bit should be set to 1. This field is loaded by BIOS. <u>Bit</u> <u>Definition</u> [0] Port 0 Implemented [1] Port 1 Implemented [31:2] Reserved

SATAx10 AHCI Version (VS)

Bits	Description
31:16	MJR: Major Version Number. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. Indicates the major version is 1.
15:0	MNR: Minor Version Number. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 300h. Indicates the minor version is 10.

SATAx14 Command Completion Coalescing Control (CCC_CTL)

Bits	Description
31:16	TV: Timeout Value. Read-write. Reset: 1. The timeout value is specified in 1 millisecond intervals. The timer accuracy shall be within 5%. hCccTimer is loaded with this timeout value. hCccTimer is only decremented when commands are outstanding on selected ports. The HBA will signal a CCC interrupt when hCccTimer has decremented to 0. hCccTimer is reset to the timeout value on the assertion of each CCC interrupt. A timeout value of 0 is reserved.

15:8	CC: Command Completions. Read-write. Reset: 1. Specifies the number of command completions that are necessary to cause a CCC interrupt. The HBA has an internal command completion counter, hCccComplete that is incremented by one each time a selected port has a command completion. When hCccComplete is equal to the command completions value, a CCC interrupt is signaled. The internal command completion counter is reset to 0 on the assertion of each CCC interrupt. 0=Disable CCC interrupts being generated based on the number of commands completed, i.e. CCC interrupts are only generated based on the timer in this case.
7:3	INT: CCC Interrupt. Read-only. Reset: 2h. Specifies the interrupt used by the Command Completion Coalescing (CCC) feature. This interrupt must be marked as unused in SATAx0C [Ports Implemented (PI)] by having the corresponding bit being set to 0. Thus, the CCC interrupt corresponds to the interrupt for an un-implemented port on the controller. When a CCC interrupt occurs, the corresponding bit in SATAx08 [Interrupt Status (IS)] shall be asserted to 1. This field also specifies the interrupt vector used for MSI.
2:1	Reserved.
0	EN: CCC CTL Enable. Read-write. Reset: 0. 0=The Command Completion Coalescing (CCC) feature is disabled and no CCC interrupts are generated. 1=The CCC feature is enabled and CCC interrupts may be generated based on timeout or command completion conditions. Software shall only change the contents of the TV and CC fields in this register when this bit is cleared to 0. On transition of this bit from 0 to 1, any updated values for the TV and CC fields shall take effect.

SATAx18 Command Completion Coalescing Ports (CCC_PORTS)

Bits	Description
31:0	PRT: Ports. Read-write. Reset: 0. This register is bit significant. Each bit corresponds to a particular port, where bit 0 corresponds to port 0. If a bit is set to 1, the corresponding port is part of the command completion coalescing feature. If a bit is cleared to 0, the port is not part of the command completion coalescing feature. Bits set to 1 in this register must also have the corresponding bit set to 1 in the SATAx0C [Ports Implemented (PI)] . An updated value for this field shall take effect within one timer increment (1 millisecond).

SATAx1C Enclosure Management Location (EM_LOC)

Bits	Description
31:16	OFST: Offset. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Value: 0000h. ELSE Value: 0140h. ENDIF. Specifies the offset of the message buffer in doublewords from the beginning of BAR5 defined by D11F0x24 .
15:0	SZ: Buffer Size. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Value: 0000h. ELSE Value: 0040h. ENDIF. Specifies the size of the transmit message buffer area in doublewords. If both transmit and receive buffers are supported, then the transmit buffer begins at SATAx1C[OFST]*4 and the receive buffer directly follows it. If both transmit and receive buffers are supported, both buffers are of the size indicated in the Buffer Size field.

SATAx20 Enclosure Management Control (EM_CTL)

Bits	Description
31:28	Reserved.
27	ATTR_PM: Port Multiplier Support. Read-only. Reset: 0. 1=The HBA supports enclosure management messages for devices attached via a Port Multiplier. 0=The HBA does not. When cleared to 0, software should use the Serial ATA enclosure management bridge that is built into many Port Multipliers for enclosure services with these devices. For more information on Serial ATA enclosure management bridges, refer to the Serial ATA Revision 2.6 specification.
26	ATTR_ALHD: Activity LED Hardware Driven. Read-only. Reset: 0. 1=The HBA drives the activity LED for the LED message type in hardware and does not utilize software settings for this LED. The HBA does not begin transmitting the hardware based activity signal until after software has written CTL_TM to 1 after a reset condition.
25	ATTR_XMT: Transmit Only. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Value: 0b. ELSE Value: 1b. ENDIF. 1=The HBA only supports transmit messages and does not support receive messages. 0=The HBA supports transmit and receive messages.
24	ATTR_SMB: Single Message Buffer. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Value: 0b. ELSE Value: 1b. ENDIF. 1=The HBA has one message buffer that is shared for messages to transmit and messages received; Unsolicited receive messages are not supported and it is software's responsibility to manage access to this buffer. 0=There are separate receive and transmit buffers such that unsolicited messages could be supported.
23:20	Reserved.
19	SUPP_SGPIO: SGPIO Enclosure Management Messages. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Value: 0b. ELSE Value: 1b. ENDIF. 1=The HBA supports the SGPIO register interface message type.
18	SUPP_SES2: SES-2 Enclosure Management Messages. Read-only. Reset: 0. 1=The HBA supports the SES-2 message type.
17	SUPP_SAFTE: SAF-TE Enclosure Management Messages. Read-only. Reset: 0. 1=The HBA supports the SAF-TE message type.
16	SUPP_LED: LED Message Types. Read-only. Reset: 0. 1=The HBA supports the LED message type as defined in section 12.2.1 of AHCI 1.3 spec.
15:10	Reserved.
9	CTL_RST: Reset. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Read-only. ELSE Read; write-1-only; cleared-by-hardware. ENDIF. Reset: 0. When set to 1 by software, the HBA shall reset all enclosure management message logic and the attached enclosure processor (if applicable) and take all appropriate reset actions to ensure messages can be transmitted/received after the reset. After the HBA completes the reset operation, the HBA shall set the value to 0.
8	CTL_TM: Transmit Message. IF (SATAxFC[CFG_CAP_EMS]==0) THEN Read-only. ELSE Read; write-1-only; cleared-by-hardware. ENDIF. Reset: 0. When set to 1 by software, the HBA shall transmit the message contained in the message buffer. When the message is completely sent, the HBA shall clear this bit to 0. Software shall not change the contents of the message buffer while this bit is set to 1.
7:1	Reserved.
0	STS_MR: Message Received. Read; write-1-to-clear. Reset: 0. The HBA sets this bit to a 1 when a message is completely received into the message buffer.

SATAx24 HBA Capabilities Extended (CAP2)

Bits	Description
31:6	Reserved.
5	DESO: DevSleep Entrance from Slumber Only. Read-only. Reset: 0. 1=The HBA shall ignore software directed entrance to DevSleep via SATAx1[9,1]8[ICC] unless [SATAx1[A,2]8IPM] = 6h. 0=The HBA may enter DevSleep from any link state (active, Partial, or Slumber). If (SATAxF4[CFG_CAP2_SDS]==0) DESO reads back 0. If (SATAxF4[CFG_CAP2_SDS]==1) DESO is automatically set to 1.
4	SADM: Supports Aggressive Device Sleep Management. Read-only. Reset: 0. 1=The HBA supports hardware assertion of the DEVSLP signal after the idle timeout expires. 0=This function is not supported and software shall treat the PxDEVSLP.ADSE field as reserved. This bit can be backdoor programmed through SATAxF4[CFG_CAP2_SADM] . If (SATAxF4[CFG_CAP2_SDS]==0) SADM reads back 0. If (SATAxF4[CFG_CAP2_SDS]==1) SADM reads back SATAxF4[CFG_CAP2_SADM] .
3	SDS: Supports Device Sleep. Read-only. Reset: 0. 1=The HBA supports the Device Sleep feature. 0=DEVSLP is not supported and software shall not set SATAx1[9,1]8[ICC] to 8. This bit can be backdoor programmed through SATAxF4[CFG_CAP2_SDS] .
2:1	Reserved
0	BOH: BIOS/OS Handoff. IF (D11F0x40[SubclassCodeWriteEnable]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. 1=The HBA supports the BIOS/OS handoff mechanism as defined in AHCI 1.2 section 10.6 and the HBA has implemented SATAx28 [BIOS/OS Handoff Control and Status (BOHC)] . 0=The HBA does not support the BIOS/OS handoff mechanism and SATAx28 [BIOS/OS Handoff Control and Status (BOHC)] is not implemented.

SATAx28 BIOS/OS Handoff Control and Status (BOHC)

Bits	Description
31:5	Reserved.
4	BB: BIOS Busy. Read-write. Reset: 0. This bit is used by the BIOS to indicate that it is busy cleaning up for ownership change.
3	OOC: OS Ownership Change. Read; write-1-to-clear. Reset: 0. This bit is set to 1 when the OOS bit transitions from 0 to 1.
2	SOOE: SMI on OS Ownership Change Enable. Read-write. Reset: 0. 1=Enables an SMI when the OOC bit has been set to 1.
1	OOS: OS Owned Semaphore. Read-write. Reset: 0. The system software sets this bit to request ownership of the HBA controller. Ownership is obtained when this bit reads 1 and the BOS bit reads 0.
0	BOS: BIOS Owned Semaphore. Read-write. Reset: 0. The BIOS sets this bit to establish ownership of the HBA controller. BIOS will clear this bit in response to a request for ownership of the HBA by system software via OOS.

3.26.3.3.2 Port Control Registers

The following registers configure the SATA ports and are implemented per port. Each port shall have the same

register mapping. Port 0 starts at 100h. Port 1 starts at 180h. An algorithm to determine the offset is as follows:
 Port offset = 100h + (Asserted Bit Position in **SATAx0C [Ports Implemented (PI)]** * 80h).

SATAx1[8,0]0 Port 1,0 Command List Base Address (PxCLB)

Bits	Description
31:10	CLB[31:10]: Command List Base Address [31:10] . Read-write. Reset: 0. Specifies the lower 32 bits of the physical base address for the command list for this port. This base address is used by HBA to fetch commands to execute. The structure pointed to by this address range is 1K-bytes in length. This address must be 1K-byte aligned.
9:0	Reserved.

SATAx1[8,0]4 Port 1,0 Command List Base Upper Address (PxCLBU)

Bits	Description
31:0	CLBU: Command List Base Address Upper . Read-write. Reset: 0. Specifies the upper 32 bits of the physical base address for the command list for this port. If 64-bit addressing is not supported, this register reads 0.

SATAx1[8,0]8 Port 1,0 FIS Base Address (PxFB)

Bits	Description
31:8	FB[31:8]: FIS Base Address [31:8] . Read-write. Reset: 0. Specifies the lower 32 bits of the physical base address for the received FISes for this port. The structure pointed to by this address range is 256 bytes in length. This address must be 256-byte aligned.
7:0	Reserved.

SATAx1[8,0]C Port 1,0 FIS Base Address Upper (PxFBU)

Bits	Description
31:0	FBU: FIS Base Address Upper . Read-write. Reset: 0. Specifies the upper 32 bits of the physical base address for the received FISes for this port. If 64-bit addressing is not supported, this register reads 0.

SATAx1[9,1]0 Port 1,0 Interrupt Status (PxIS)

Bits	Description
31	CPDS: Cold Port Detect Status . Read; write-1-to-clear. Reset: 0. 1=The device status has changed as detected by the cold presence detection logic. This bit can be set due to either a non-connected port receiving a device, or a connected port having its device removed. This bit is only valid if SATAx1[9,1]8[CPD]==1 .
30	TFES: Task File Error Status . Read; write-1-to-clear. Reset: 0. 1=The error bit at bit [0] of the status field in the received FIS is set to 1 when the status register is updated by the device.

29	HBFS: Host Bus Fatal Error Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has encountered a host bus error that it cannot recover from, such as a bad software pointer. In PCI, it indicates a target or master abort.
28	HBDS: Host Bus Data Error Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has encountered a data error (uncorrectable ECC / parity) when reading from or writing to system memory.
27	IFS: Interface Fatal Error Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has encountered an error on the Serial ATA interface, which caused the transfer to stop.
26	INFS: Interface Non-fatal Error Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has encountered an error on the Serial ATA interface and was able to continue operation.
25	Reserved.
24	OFS: Overflow Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has received more bytes from a device than what was specified in the PRD table for the command.
23	IPMS: Incorrect Port Multiplier Status. Read; write-1-to-clear. Reset: 0. 1=The HBA has received a FIS from a device whose Port Multiplier field did not match what was expected. The IPMS bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.
22	PRCS: PhyRdy Change Status. Read-only. Reset: 0. 1=The internal PhyRdy signal has changed state. This bit reflects the state of SATAx1[B,3]0[DIAG] . To clear this bit, software must program SATAx1[B,3]0[DIAG] to 0.
21:8	Reserved.
7	DMPS: Device Mechanical Presence Status. Read; write-1-to-clear. Reset: 0. 1=A mechanical presence switch attached to this port has been opened or closed, which may lead to a change in the connection state of the device. This bit is only valid if ((SATAx00[SMPS]==1) && (SATAx1[9,1]8[MPSP]==1)).
6	PCS: Port Connect Change Status. Read-only. Reset: 0. 0=No change in Current Connect Status. 1=Change in Current Connect Status. This bit reflects the state of SATAx1[B,3]0[DIAG[10]] . This bit is only cleared when SATAx1[B,3]0[DIAG] is cleared.
5	DPS: Descriptor Processed. Read; write-1-to-clear. Reset: 0. 1=A Physical Region Descriptor (PRD) with the I bit set has transferred all of its data.
4	UFS: Unknown FIS Interrupt. Read-only. Reset: 0. 1=An unknown FIS was received with the I bit set and has been copied into system memory. This bit is cleared to 0 by software clearing the SATAx1[B,3]0[DIAG] bit to 0. This bit does not directly reflect the SATAx1[B,3]0[DIAG] bit. SATAx1[B,3]0[DIAG] is set immediately when an unknown FIS is detected, whereas this bit is set when that FIS is posted to memory. Software should wait to act on an unknown FIS until this bit is set to 1, or the two bits may become out-of- sync.
3	SDBS: Set Device Bits Interrupt. Read; write-1-to-clear. Reset: 0. 1=A Set Device Bits FIS has been received with the I bit set and has been copied into system memory.
2	DSS: DMA Setup FIS Interrupt. Read-write. Reset: 0. 1=A DMA Setup FIS has been received with the I bit set and has been copied into system memory.
1	PSS: PIO Setup FIS Interrupt. Read; write-1-to-clear. Reset: 0. 1=A PIO Setup FIS has been received with the I bit set, and it has been copied into system memory, and the data related to that FIS has been transferred. This bit shall be set even if the data transfer resulted in an error.
0	DHRS: Device to Host Register FIS Interrupt. Read; write-1-to-clear. Reset: 0. 1=A D2H Register FIS has been received with the I bit set, and has been copied into system memory.

SATAx1[9,1]4 Port 1,0 Interrupt Enable (PxIE)

Bits	Description
31	CPDE: Cold Presence Detect Enable. IF (SATAx1[9,1]8[CPD]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[CPDS]==1)).
30	TFEE: Task File Error Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[TFES]==1)).
29	HBFE: Host Bus Fatal Error Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[HBFS]==1)).
28	HBDE: Host Bus Data Error Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && SATAx1[9,1]0[HBDS]==1)).
27	IFE: Interface Fatal Error Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[IFS]==1)).
26	INFE: Interface Non-fatal Error Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[INFS]==1)).
25	Reserved.
24	OFE: Overflow Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[OFS]==1)).
23	IPME: Incorrect Port Multiplier Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[IPMS]==1)).
22	PRCE: PhyRdy Change Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[PRCS]==1)).
21:8	Reserved.
7	DMPE: Device Mechanical Presence Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[DMPS]==1)). For systems that do not support a mechanical presence switch, this bit will be read-only and will return a 0.
6	PCE: Port Change Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[PCS]==1)).
5	DPE: Descriptor Processed Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[DPS]==1)).
4	UFE: Unknown FIS Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[UFS]==1)).
3	SDBE: Set Device Bits FIS Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[SDBS]==1)).
2	DSE: DMA Setup FIS Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[DSS]==1)).
1	PSE: PIO Setup FIS Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[PSS]==1)).
0	DHRE: Device to Host Register FIS Interrupt Enable. Read-write. Reset: 0. 1=The HBA generates an interrupt if ((SATAx04[IE]==1) && (SATAx1[9,1]0[DHRS]==1)).

SATAx1[9,1]8 Port 1,0 Command and Status (PxCMD)

Bits	Description																		
31:28	<p>ICC: Interface Communication Control. Read-write. Reset: 0. This field is used to control power management states of the interface. If the Link layer is currently in the L_IDLE state, writing to this field shall cause the HBA to initiate a transition to the interface power management state requested. If the Link layer is not currently in the L_IDLE state, writing to this field shall have no effect.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>Fh-9h</td> <td>Reserved</td> </tr> <tr> <td>8h</td> <td>DevSleep. This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the Device Sleep Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DevSleep when the interface is in an idle state (i.e. PxCI is cleared to 0h and PxSACT are cleared to 0h); if CAP2.SDS is cleared to '0' or if the interface is not idle at the time the register is written, then the HBA shall not assert the DEVSLP signal and the interface remains in its current state. If CAPS.SDS is set to '1', CAP2.DESO is set to '1', and PxSSTS.IPM is not set to '6h', then the HBA shall not assert the DEVSLP signal and the interface shall remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion).</td> </tr> <tr> <td>7h</td> <td>Reserved</td> </tr> <tr> <td>6h</td> <td>Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state.</td> </tr> <tr> <td>5h-3h</td> <td>Reserved</td> </tr> <tr> <td>2h</td> <td>Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state.</td> </tr> <tr> <td>1h</td> <td>Active: This shall cause the HBA to request a transition of the interface into the active state.</td> </tr> <tr> <td>0h</td> <td>No-Op, Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not have occurred yet.</td> </tr> </tbody> </table> <p>When system software writes a non-reserved value other than No-Op (0h), the HBA shall perform the action and update this field back to Idle (0h). If software writes to this field to change the state to a state the link is already in (i.e. interface is in the active state and a request is made to go to the active state), the HBA shall take no action and return this field to Idle. If the interface is in a low power state and software wants to transition to a different low power state, software must first bring the link to active and then initiate the transition to the desired low power state with the exception of DEVSLP. The transition to DevSleep may occur from any other state if SATAx24[DESO]==0. If SATAx24[DESO]==1, then DevSleep may only be transitioned to if the link is in Slumber.</p>	Bits	Definition	Fh-9h	Reserved	8h	DevSleep. This shall cause the HBA to assert the DEVSLP signal associated with the port; the HBA shall ignore the Device Sleep Idle Timeout value specified by PxDEVSLP.DITO. Software shall only request DevSleep when the interface is in an idle state (i.e. PxCI is cleared to 0h and PxSACT are cleared to 0h); if CAP2.SDS is cleared to '0' or if the interface is not idle at the time the register is written, then the HBA shall not assert the DEVSLP signal and the interface remains in its current state. If CAPS.SDS is set to '1', CAP2.DESO is set to '1', and PxSSTS.IPM is not set to '6h', then the HBA shall not assert the DEVSLP signal and the interface shall remain in its current state. Additionally, the HBA shall not assert the DEVSLP signal until PHYRDY has been achieved (after a previous de-assertion).	7h	Reserved	6h	Slumber: This shall cause the HBA to request a transition of the interface to the Slumber state. The SATA device may reject the request and the interface shall remain in its current state.	5h-3h	Reserved	2h	Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state.	1h	Active: This shall cause the HBA to request a transition of the interface into the active state.	0h	No-Op, Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not have occurred yet.
Bits	Definition																		
Fh-9h	Reserved																		
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7h	Reserved																		
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5h-3h	Reserved																		
2h	Partial: This shall cause the HBA to request a transition of the interface to the Partial state. The SATA device may reject the request and the interface shall remain in its current state.																		
1h	Active: This shall cause the HBA to request a transition of the interface into the active state.																		
0h	No-Op, Idle: When software reads this value, it indicates the HBA is ready to accept a new interface control command, although the transition to the previously selected state may not have occurred yet.																		
27	<p>ASP: Aggressive Slumber/Partial. Read-write. Reset: 0. When set to 1, and ALPE==1, the HBA shall aggressively enter the Slumber state when it clears SATAx1[B,3]8 and SATAx1[B,3]4 is cleared or when it clears the SATAx1[B,3]4 register and SATAx1[B,3]8 is cleared. When cleared, and ALPE==1, the HBA shall aggressively enter the Partial state when it clears the SATAx1[B,3]8 register and the SATAx1[B,3]4 register is cleared or when it clears the SATAx1[B,3]4 register and SATAx1[B,3]8 is cleared. See SATAx00[SALP]. If (SATAx00[SALP]==0) software shall treat this bit as reserved.</p>																		

26	ALPE: Aggressive Link Power Management Enable. Read-write. Reset: 0. 1=The HBA shall aggressively enter a lower link power state (Partial or Slumber) based upon the setting of the ASP bit. See SATAx00[SALP] . If (SATAx00[SALP]==0) software shall treat this bit as reserved.
25	DLAE: Drive LED on ATAPI Enable. Read-write. Reset: 0. 1=The HBA shall drive the LED pin active for commands regardless of the state of bit ATAPI. 0=The HBA shall only drive the LED pin active for commands if bit ATAPI==0.
24	ATAPI: Device is ATAPI. Read-write. Reset: 0. 1=The connected device is an ATAPI device. This bit is used by the HBA to control whether or not to generate the desktop LED when commands are active.
23	Reserved.
22	FBSCP: FIS-based Switching Capable Port. Read-only. Reset: 1. 1=Indicates that this port supports Port Multiplier FIS-based switching. 0=Indicates that this port does not support FIS-based switching.
21	ESP: External SATA Port. Read-only. Reset: 0. 1=Indicates that this port's signal connector is externally accessible on a signal only connector. 0=Indicates that this port's signal connector is not externally accessible on a signal only connector. ESP is mutually exclusive with the HPCP bit in this register. When set to 1, SATAx00[SXS] shall be set to 1.
20	CPD: Cold Presence Detection. Read-only. Reset: 0. 1=The platform supports cold presence detection on this port. 0=The platform does not support cold presence detection on this port. When this bit is set to 1, SATAx1[9,1]8[HPCP] should also be set to 1.
19	MPSP: Mechanical Presence Switch Attached to Port. Read-only. Reset: 0. 1=The platform supports an mechanical presence switch attached to this port. 0=The platform does not support a mechanical presence switch attached to this port. When this bit is set to 1, SATAx1[9,1]8[HPCP] should also be set to 1.
18	HPCP: Hot Plug Capable Port. Read-only. Reset: 0. 1=Indicates that this port's signal and power connectors are externally accessible via a joint signal and power connector for blindmate device hot plug. 0=Indicates that this port's signal and power connectors are not externally accessible via a joint signal and power connector.
17	PMA: Port Multiplier Attached. IF (SATAx00[SPM]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=A Port Multiplier is attached to the HBA for this port. 0=A Port Multiplier is not attached to the HBA for this port. Software is responsible for detecting whether a Port Multiplier is present; hardware does not auto-detect the presence of a Port Multiplier.
16	CPS: Cold Presence State. Read-only. Reset: 0. The CPS bit reports whether a device is currently detected on this port via cold presence detection. 1=The HBA detects via cold presence that a device is attached to this port. 0=The HBA detects via cold presence that there is no device attached to this port.
15	CR: Command List Running. Read-only; S3-check-exclude. Reset: 0. 1=The command list DMA engine for the port is running.
14	FR: FIS Receive Running. Read-only. Reset: 0. 1=The FIS Receive DMA engine for the port is running.
13	MPSS: Mechanical Presence Switch State. Read-only. Reset: 1. This bit reports the state of a mechanical presence switch attached to this port. If SATAx00[SMPS]==1 and the mechanical presence switch is closed then this bit is cleared to 0. If SATAx00[SMPS]==1 and the mechanical presence switch is open then this bit is set to 1. If SATAx00[SMPS]==0 then this bit is cleared to 0. Software should only use this bit if ((SATAx00[SMPS]==1) && (SATAx1[9,1]8[MPSP]==1)).

12:8	CCS: Current Command Slot. Read-only; updated-by-hardware. Reset: 0. This field is valid if SATAx1[9,1]8[ST]==1 and shall be set to the command slot value of the command that is currently being issued by the HBA. When SATAx1[9,1]8[ST] transitions from 1 to 0, this field shall be reset to 0. After SATAx1[9,1]8[ST] transitions from 0 to 1, the highest priority slot to issue from next is command slot 0. After the first command has been issued, the highest priority slot to issue from next is CCS+1. For example, after the HBA has issued its first command, if CCS==0 and SATAx1[B,3]8==3 , the next command that will be issued is from command slot 1.
7:5	Reserved.
4	FRE: FIS Receive Enable. Read-write. Reset: 0. 1=The HBA may post the received FISes into the FIS receive area pointed to by SATAx1[8,0]8 [Port 1,0 FIS Base Address (PxFB)] (and SATAx1[8,0]C [Port 1,0 FIS Base Address Upper (PxFBU)] for 64-bit HBAs). 0=Received FISes are not accepted by the HBA, except for the first D2H register FIS after the initialization sequence, and no FISes are posted to the FIS receive area. System software must not set this bit until SATAx1[8,0]8 (and SATAx1[8,0]C for 64-bit) have been programmed with a valid pointer to the FIS receive area. If software wishes to move the base, this bit must first be cleared, and software must wait for the FR bit in this register to be cleared.
3	CLO: Command List Override. Read; write-1-only; cleared-by-hardware. Reset: 0. Setting this bit to 1 causes SATAx1[A,2]0[STS[7], STS[3]] to be cleared to 0. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the SATAx1[A,2]0[STS] register. The HBA sets this bit to 0 when SATAx1[A,2]0[STS[7], STS[3]] have been cleared to 0. This bit shall only be set to 1 immediately prior to setting SATAx1[9,1]8[ST] to 1 from a previous value of 0. Setting this bit to 1 at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to 0 before setting SATAx1[9,1]8[ST] to 1.
2	POD: Power On Device. IF (SATAx1[9,1]8[CPD]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. This bit is read/write for HBAs that support cold presence detection on this port as indicated by SATAx1[9,1]8[CPD]==1 . 1=HBAs does not support cold presence detect and the HBA sets the state of a pin on the HBA to 1 so that it may be used to provide power to a cold-presence detectable port.
1	SUD: Spin-Up Device. IF (SATAx00[SSS]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. This bit is read/write for HBAs that support staggered spin-up via SATAx00[SSS]==1 . 1=HBAs does not support staggered spin-up. On an edge detect from 0 to 1, the HBA shall start a COMRESET initialization sequence to the device. Clearing this bit does not cause any OOB signal to be sent on the interface. When this bit is cleared to 0 and SATAx1[A,2]C[DET]==0 the HBA will enter listen mode.
0	ST: Start. Read-write. Reset: 0. 1=The HBA may process the command list. 0=The HBA may not process the command list. Whenever this bit is changed from 0 to 1, the HBA starts processing the command list at entry 0. Whenever this bit is changed from a 1 to a 0, SATAx1[B,3]8 is cleared by the HBA upon the HBA putting the controller into an idle state. This bit will only be set to 1 by software after SATAx1[9,1]8[FRE] has been set to 1.

SATAx1[A,2]0 Port 1,0 Task File Data (PxTFD)

Bits	Description
31:16	Reserved.

15:8	ERR: Error. Read-only. Reset: 0. Contains the latest copy of the task file error register.												
7:0	<p>STS: Status. Read-only; updated-by-hardware. Reset: 7Fh. Contains the latest copy of the task file status register. Fields of note in this register that affect AHCI hardware operation are:</p> <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[7]</td> <td>BSY. 1=Indicates the interface is busy</td> </tr> <tr> <td>[6:4]</td> <td>CS. Command specific</td> </tr> <tr> <td>[3]</td> <td>DRQ. 1=Indicates a data transfer is requested</td> </tr> <tr> <td>[2:1]</td> <td>CS. Command specific</td> </tr> <tr> <td>[0]</td> <td>ERR. 1=Indicates an error during the transfer</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[7]	BSY. 1=Indicates the interface is busy	[6:4]	CS. Command specific	[3]	DRQ. 1=Indicates a data transfer is requested	[2:1]	CS. Command specific	[0]	ERR. 1=Indicates an error during the transfer
<u>Bit</u>	<u>Definition</u>												
[7]	BSY. 1=Indicates the interface is busy												
[6:4]	CS. Command specific												
[3]	DRQ. 1=Indicates a data transfer is requested												
[2:1]	CS. Command specific												
[0]	ERR. 1=Indicates an error during the transfer												

SATAx1[A,2]4 Port 1,0 Signature (PxSIG)

Bits	Description										
31:0	<p>SIG: Signature. Read-write. Reset: FFFF_FFFFh. Contains the signature received from a device on the first D2H Register FIS. The bit order is as following:</p> <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[31:24]</td> <td>LBA High Register</td> </tr> <tr> <td>[23:16]</td> <td>LBA Mid Register</td> </tr> <tr> <td>[15:08]</td> <td>LBA Low Register</td> </tr> <tr> <td>[07:00]</td> <td>Sector Count Register</td> </tr> </tbody> </table> <p>The register is updated once after each reset sequence.</p>	<u>Bit</u>	<u>Definition</u>	[31:24]	LBA High Register	[23:16]	LBA Mid Register	[15:08]	LBA Low Register	[07:00]	Sector Count Register
<u>Bit</u>	<u>Definition</u>										
[31:24]	LBA High Register										
[23:16]	LBA Mid Register										
[15:08]	LBA Low Register										
[07:00]	Sector Count Register										

SATAx1[A,2]8 Port 1,0 Serial ATA Status (PxSSTS)

Bits	Description																		
31:12	Reserved.																		
11:8	<p>IPM: Interface Power Management. Read-only; updated-by-hardware. Reset: 0. Indicates the current interface state.</p> <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Device not present or communication not established</td> </tr> <tr> <td>1h</td> <td>Interface in Active state</td> </tr> <tr> <td>2h</td> <td>Interface in Partial power management state</td> </tr> <tr> <td>5h-3h</td> <td>Reserved</td> </tr> <tr> <td>6h</td> <td>Interface in Slumber power management state</td> </tr> <tr> <td>7h</td> <td>Reserved</td> </tr> <tr> <td>8h</td> <td>Interface in DevSleep power management state</td> </tr> <tr> <td>Fh-9h</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0h	Device not present or communication not established	1h	Interface in Active state	2h	Interface in Partial power management state	5h-3h	Reserved	6h	Interface in Slumber power management state	7h	Reserved	8h	Interface in DevSleep power management state	Fh-9h	Reserved
<u>Bits</u>	<u>Definition</u>																		
0h	Device not present or communication not established																		
1h	Interface in Active state																		
2h	Interface in Partial power management state																		
5h-3h	Reserved																		
6h	Interface in Slumber power management state																		
7h	Reserved																		
8h	Interface in DevSleep power management state																		
Fh-9h	Reserved																		

7:4	SPD: Current Interface Speed. Read-only; updated-by-hardware. Reset: 0. Indicates the negotiated interface communication speed.
	<u>Bits</u> <u>Definition</u>
	0h Device not present or communication not established
	1h Generation 1 communication rate negotiated
	2h Generation 2 communication rate negotiated
	3h Generation 3 communication rate negotiated
	Fh-4h Reserved
3:0	DET: Device Detection. Read-only; updated-by-hardware. Reset: 0. Indicates the interface device detection and PHY state.
	<u>Bits</u> <u>Definition</u>
	0h No device detected and PHY communication not established
	1h Device presence detected but PHY communication not established
	2h Reserved.
	3h Device presence detected and PHY communication established
	4h PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode
	Fh-5h Reserved

SATAx1[A,2]C Port 1,0 Serial ATA Control (PxSCTL)

Bits	Description
31:20	Reserved.
19:16	PMP: Port Multiplier Port. Read-only. Reset: 0. This field is not used by AHCI.
15:12	SPM: Select Power Management. Read-only. Reset: 0. This field is not used by AHCI.
11:8	IPM: Interface Power Management Transitions Allowed. Read-write. Reset: 0. Indicates which power states the HBA is allowed to transition to. If an interface power management state is disabled, the HBA is not allowed to initiate that state and the HBA must respond with power management denial to any request from the device to enter that state.
	<u>Bits</u> <u>Definition</u>
	0h No interface restrictions
	1h Disable transitions to the Partial state.
	2h Disable transitions to the Slumber state.
	3h Disable transitions to both Partial and Slumber states.
	4h Disable transitions to the DevSleep power management state.
	5h Disable transitions to the Partial and DevSleep power management states.
	6h Disable transitions to the Slumber and DevSleep power management states.
	7h Disable transitions to the Partial, Slumber and DevSleep power management states.
	Fh-8h Reserved

	SPD: Speed Allowed. Read-write. Reset: 0. Indicates the highest allowable speed of the interface.												
7:4	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0h</td><td>No speed negotiation restrictions</td></tr> <tr> <td>1h</td><td>Limit speed negotiation to Generation 1 communication rate</td></tr> <tr> <td>2h</td><td>Limit speed negotiation to a rate not greater than Generation 2 communication rate</td></tr> <tr> <td>3h</td><td>Limit speed negotiation to a rate not greater than Generation 3 communication rate</td></tr> <tr> <td>Fh-4h</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0h	No speed negotiation restrictions	1h	Limit speed negotiation to Generation 1 communication rate	2h	Limit speed negotiation to a rate not greater than Generation 2 communication rate	3h	Limit speed negotiation to a rate not greater than Generation 3 communication rate	Fh-4h	Reserved
<u>Bits</u>	<u>Definition</u>												
0h	No speed negotiation restrictions												
1h	Limit speed negotiation to Generation 1 communication rate												
2h	Limit speed negotiation to a rate not greater than Generation 2 communication rate												
3h	Limit speed negotiation to a rate not greater than Generation 3 communication rate												
Fh-4h	Reserved												
3:0	<p>DET: Device Detection Initialization. Read-write. Reset: 0. Controls the HBA's device detection and interface initialization.</p> <table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0h</td><td>No device detection or initialization action requested</td></tr> <tr> <td>1h</td><td>Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface.</td></tr> <tr> <td>3h-2h</td><td>Reserved</td></tr> <tr> <td>4h</td><td>Disable the Serial ATA interface and put PHY in off-line mode</td></tr> <tr> <td>Fh-5h</td><td>Reserved</td></tr> </tbody> </table> <p>This field may only be modified when SATAx1[9,1]8[ST]==0. Changing this field while SATAx1[9,1]8[ST]==1 results in undefined behavior. When SATAx1[9,1]8[ST]==1, this field should have a value of 0.</p> <p>Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.</p>	<u>Bits</u>	<u>Definition</u>	0h	No device detection or initialization action requested	1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface.	3h-2h	Reserved	4h	Disable the Serial ATA interface and put PHY in off-line mode	Fh-5h	Reserved
<u>Bits</u>	<u>Definition</u>												
0h	No device detection or initialization action requested												
1h	Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized. While this field is 1h, COMRESET is transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface.												
3h-2h	Reserved												
4h	Disable the Serial ATA interface and put PHY in off-line mode												
Fh-5h	Reserved												

SATAx1[B,3]0 Port 1,0 Serial ATA Error(PxSERR)

Bits	Description
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31:16	DIAG: Diagnostics. Read; write-1-to-clear. Reset: 0. Contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes:	
	<u>Bit</u>	<u>Definition</u>
	[15:11]	Reserved
	[10]	Exchanged (X). Indicates a COMINIT signal was received. This bit is reflected in SATAx1[9,1]0[PCS] .
	[9]	Unknown FIS Type (F). Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized/known.
	[8]	Transport state transition error (T). Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared. This bit is always 0 in the current implementation.
	[7]	Link Sequence Error (S). Indicates that one or more Link state machine error conditions was encountered. The Link Layer state machine defines the conditions under which the link layer detects an erroneous transition. This bit is always 0 in the current implementation.
	[6]	Handshake Error (H). Indicates that one or more R_ERR handshake responses were received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
	[5]	CRC Error (C). Indicates that one or more CRC errors occurred with the Link Layer.
	[4]	Disparity Error (D). This field is not used by AHCI. This bit is always 0 in the current implementation.
	[3]	10B to 8B Decode Error (B). Indicates that one or more 10B to 8B decoding errors has occurred.
	[2]	Comm Wake (W). Indicates that a Comm Wake signal was detected by the PHY.
	[1]	Phy Internal Error (I). Indicates that the PHY detected some internal error. This bit is always 0 in the current implementation.
	[0]	PhyRdy Change (N). Indicates that the PhyRdy signal changed state. This bit is reflected in the SATAx1[9,1]0[PRCS] bit.

15:0	Err: Error. Read; write-1-to-clear. Reset: 0. Contains error information for use by host software in determining the appropriate response to the error condition.																		
	<table> <thead> <tr> <th style="text-align: center;"><u>Bit</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">[15:12]</td><td>Reserved.</td></tr> <tr> <td style="text-align: center;">[11]</td><td>Internal Error (E). The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically, when an internal error occurs, a non-fatal or fatal status bit in SATAx1[9,1]0 register will also be set to give software guidance on the recovery mechanism required.</td></tr> <tr> <td style="text-align: center;">[10]</td><td>Protocol Error (P). A violation of the Serial ATA protocol was detected.</td></tr> <tr> <td style="text-align: center;">[9]</td><td>Persistent Communication or Data Integrity Error (C). A communication error that was not recovered occurred and is expected to be persistent. Persistent communication errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.</td></tr> <tr> <td style="text-align: center;">[8]</td><td>Transient Data Integrity Error (T). A data integrity error occurred that was not recovered by the interface. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.</td></tr> <tr> <td style="text-align: center;">[7:2]</td><td>Reserved.</td></tr> <tr> <td style="text-align: center;">[1]</td><td>Recovered Communications Error (M). Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of PHY synchronization, or from other causes and may be derived from the PhyNRdy signal between the PHY and Link layers.</td></tr> <tr> <td style="text-align: center;">[0]</td><td>Recovered Data Integrity Error (I). A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.</td></tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[15:12]	Reserved.	[11]	Internal Error (E). The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically, when an internal error occurs, a non-fatal or fatal status bit in SATAx1[9,1]0 register will also be set to give software guidance on the recovery mechanism required.	[10]	Protocol Error (P). A violation of the Serial ATA protocol was detected.	[9]	Persistent Communication or Data Integrity Error (C). A communication error that was not recovered occurred and is expected to be persistent. Persistent communication errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.	[8]	Transient Data Integrity Error (T). A data integrity error occurred that was not recovered by the interface. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.	[7:2]	Reserved.	[1]	Recovered Communications Error (M). Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of PHY synchronization, or from other causes and may be derived from the PhyNRdy signal between the PHY and Link layers.	[0]	Recovered Data Integrity Error (I). A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.
<u>Bit</u>	<u>Definition</u>																		
[15:12]	Reserved.																		
[11]	Internal Error (E). The host bus adapter experienced an internal error that caused the operation to fail and may have put the host bus adapter into an error state. The internal error may include a master or target abort when attempting to access system memory, an elasticity buffer overflow, a primitive mis-alignment, a synchronization FIFO overflow, and other internal error conditions. Typically, when an internal error occurs, a non-fatal or fatal status bit in SATAx1[9,1]0 register will also be set to give software guidance on the recovery mechanism required.																		
[10]	Protocol Error (P). A violation of the Serial ATA protocol was detected.																		
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[8]	Transient Data Integrity Error (T). A data integrity error occurred that was not recovered by the interface. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.																		
[7:2]	Reserved.																		
[1]	Recovered Communications Error (M). Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of PHY synchronization, or from other causes and may be derived from the PhyNRdy signal between the PHY and Link layers.																		
[0]	Recovered Data Integrity Error (I). A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action. This bit is set upon any error when a Data FIS is received, including reception FIFO overflow, CRC error, or 10b/8b decoding error.																		

SATAx1[B,3]4 Port 1,0 Serial ATA Active (PxSACT)

Bits	Description
31:0	<p>DS: Device Status. Read; write-1-only; cleared-by-hardware. Reset: 0. This field is bit significant. Each bit corresponds to the TAG and command slot of a native queued command, where bit 0 corresponds to TAG 0 and command slot 0. This field is set by software prior to issuing a native queued command for a particular command slot. Prior to writing SATAx1[B,3]8 TAG to 1, software will set DS TAG to 1 to indicate that a command with that TAG is outstanding. The device clears bits in this field by sending a Set Device Bits FIS to the host. The HBA clears bits in this field that are set to 1 in the SActive field of the Set Device Bits FIS. The HBA only clears bits that correspond to native queued commands that have completed successfully.</p> <p>Software should only write to this field when SATAx1[9,1]8[ST]==1. This field is cleared when SATAx1[9,1]8[ST] is written from 1 to 0 by software. This field is not cleared by a COMRESET or a software reset.</p>

SATAx1[B,3]8 Port 1,0 Command Issue (PxCI)

Bits	Description
31:0	CI: Commands Issued. Read; write-1-only; cleared-by-hardware. Reset: 0. This field is bit significant. Each bit corresponds to a command slot, where bit 0 corresponds to command slot 0. This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to 1 by software when SATAx1[9,1]8[ST] is set to 1. This field is also cleared when SATAx1[9,1]8[ST] is written from 1 to 0 by software.

SATAx1[B,3]C Port 1,0 SNotification (PxSNTF)

Bits	Description
31:16	Reserved.
15:0	PMN: PM Notify. Read; write-1-to-clear. Reset: 0. This field is bit significant. Each bit corresponds to a Port Multiplier (PM) port number, where bit 0 corresponds to PM port 0 and bit 15 corresponds to PM port 15. This field indicates whether a particular device with the corresponding PM Port number issued a Set Device Bits FIS to the host with the Notification bit set. Individual bits are cleared by software writing 1 to the corresponding bit positions. This field is reset to default on a HBA Reset, but it is not reset by COMRESET or software reset.

SATAx1[C,4]0 Port 1,0 FIS-based Switching Control (PxFBS)

Bits	Description
31:20	Reserved.
19:16	DWE: Device With Error. Read-only; updated-by-hardware. Reset: 0. Set by hardware to the value of the Port Multiplier port number of the device that experienced a fatal error condition. This field is only valid when SATAx1[C,4]0[SDE]==1 .
15:12	ADO: Active Device Optimization. IF (D11F0x40[SubclassCodeWriteEnable] == 1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 2h. This register exposes the number of active devices that the FIS-based switching implementation has been optimized for. When there are more devices active than indicated in this field, throughput of concurrent traffic may degrade. For optimal performance, software should limit the number of active devices based on this value. The minimum value for this field shall be 2h, indicating that at least two devices may be active with high performance maintained.
11:8	DEV: Device To Issue. Read-write. Reset: 0. Set by software to the Port Multiplier port value of the next command to issue. This field enables hardware to know the port the command is to be issued to without fetching the command header. Software shall not issue commands to multiple Port Multiplier ports on the same write of SATAx1[B,3]8 register.
7:3	Reserved.

2	SDE: Single Device Error. Read-only. Reset: 0. 1=When a fatal error condition has occurred, hardware believes the error is localized to one device such that software's first error recovery step should be to utilize the SATAx1[C,4]0[DEC] functionality. 0=When a fatal error condition has occurred, the error applies to the entire port and to clear the error SATAx1[9,1]8[ST] shall be cleared to 0 by software. This bit is cleared on SATAx1[C,4]0[DEC] being set to 1 or on SATAx1[9,1]8[ST] being cleared to 0.
1	DEC: Device Error Clear. Read; write-1-only; cleared-by-hardware. Reset: 0. When set to 1 by software, the HBA shall clear the device-specific error condition and the HBA shall flush any commands outstanding for the device that experienced the error, including clearing SATAx1[B,3]8 and SATAx1[B,3]4 bits for that device to 0. When hardware has completed error recovery actions, hardware shall clear the bit to 0. Software shall only set this bit to 1 if ((SATAx1[C,4]0[EN]==1) && (SATAx1[C,4]0[SDE]==1)).
0	EN: Enable. Read-write. Reset: 0. 1=A Port Multiplier is attached and the HBA shall use FIS-based switching to communicate with it. 0=FIS-based switching is not being used. Software shall only change the value of this bit when SATAx1[9,1]8[ST]==0 .

SATAx1[C,4]4 Port 1,0 Device Sleep (PxDEVSLP)

Bits	Description												
31:29	Reserved.												
28:25	DM: DITO Multiplier. Read-only. Reset: 0. 0's based value that specifies the DITO multiplier that the HBA applies to the specified DITO value, effectively extending the range of DITO from 1 ms to 16383 ms. The HBA computes the total idle timeout as a product of DM and DITO (i.e. DITOactual = DITO * DM). <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>0h</td> <td>multiply 1</td> <td>Eh-2h</td> <td>multiply <DM+1></td> </tr> <tr> <td>1h</td> <td>multiply 2</td> <td>Fh</td> <td>multiply 16</td> </tr> </table> This field can be programmed though back door register SATAxF4[CFG_PxDEVSLP_DM] with the value of 0, 1 or 3. When SATAxF4[CFG_PxDEVSLP_DM] is programmed to 2, DM will read back 1.	Bits	Definition	Bits	Definition	0h	multiply 1	Eh-2h	multiply <DM+1>	1h	multiply 2	Fh	multiply 16
Bits	Definition	Bits	Definition										
0h	multiply 1	Eh-2h	multiply <DM+1>										
1h	multiply 2	Fh	multiply 16										
24:15	DITO: Device Sleep Idle Timeout. IF ((SATAx24[SDS]==0) (SATAx24[SADM]==0)) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. This field specifies the amount of the time (in approximate 1 ms granularity) that the HBA shall wait before driving the DEVSLP signal. Hardware reloads its port specific Device Sleep timer with this value each time the port transitions out of the DEVSLP state. For example: from DevSleep to Active or SATAx1[C,4]4[ADSE] transitions from 0 to 1. Software shall only set this value when SATAx1[9,1]8[ST]==0 and SATAx1[C,4]4[ADSE]==0 .												
14:10	MDAT: Minimum Device Sleep Assertion Time. IF (SATAx24[SDS]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. This field specifies the minimum amount of time (in 1 ms granularity) that the HBA must assert the DEVSLP signal before it may be de-asserted. The nominal value is 10 ms and the minimum is 1 ms depending on device identification information. Software shall only set this value when SATAx1[9,1]8[ST]==0 , SATAx1[C,4]4[ADSE]==0 and prior to setting SATAx1[9,1]8[ICC] to 8h.												

9:2	DETO: Device Sleep Exit Timeout. IF (SATAx24[SDS]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. This field specifies the maximum duration (in approximate 1 ms granularity) from DEVSLP de-assertion until the device is ready to accept OOB. The nominal value is 20 ms while the max value is 255 ms depending on device identification information. Software shall only set this value when SATAx1[9,1]8[ST]==0 , SATAx1[C,4]4[ADSE]==0 and prior to setting SATAx1[9,1]8[ICC] to 8h.
1	DSP: Device Sleep Present. Read-write. Reset: 0. 1=The platform supports Device Sleep on this port. 0=The platform does not support Device Sleep on this port. This bit may only be set to 1 if SATAx24[SDS]==1 . DSP is mutually exclusive with the SATAx1[9,1]8[HPCP] bit and SATAx1[9,1]8[ESP] bit.
0	ADSE: Aggressive Device Sleep Enable. IF ((SATAx24[SADM]==1) && (SATAx24[SDS]==1)) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. 0=The HBA does not enter DevSleep unless software directed via SATAx1[9,1]8[ICC] . 1=The HBA shall assert the DEVSLP signal after the port has been idle (SATAx1[B,3]8==0 and SATAx1[B,3]4==0) for the amount of time specified by the SATAx1[C,4]4[DITO] ; If (SATAx24[DESO]== 1), the HBA shall assert the DEVSLP signal after the port has been idle for the amount of time specified by SATAx1[C,4]4[DITO] and the interface is in Slumber state (SATAx1[A,2]8[IPM]==6h). This bit shall only be set to 1 if SATAx1[C,4]4[DSP]==1 .

3.26.3.3.3 Enclosure Buffer Management Registers

The Enclosure Buffer Management registers range from ([D11F0x24 \[AHCI Base Address \(BAR5\)\] + SATAx1C\[OFST\]*4 + 00h](#)) to ([D11F0x24 \[AHCI Base Address \(BAR5\)\] + SATAx1C\[OFST\]*4 + FFh](#)) within the memory mapped space.

SATA_EMx00 Message Header

Bits	Description												
31:28	Reserved.												
27:24	MTYPE: Message Type. Read-write. Reset: 0. Specifies the type of the message. The message types are: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>LED</td> </tr> <tr> <td>1h</td> <td>SAF-TE</td> </tr> <tr> <td>2h</td> <td>SES-2</td> </tr> <tr> <td>3h</td> <td>GPIO (register based interface)</td> </tr> <tr> <td>Fh-4h</td> <td>Reserved.</td> </tr> </tbody> </table> To reduce the complexity, current hardware implementation treats this field as don't-care. It is defined for future use.	Bits	Definition	0h	LED	1h	SAF-TE	2h	SES-2	3h	GPIO (register based interface)	Fh-4h	Reserved.
Bits	Definition												
0h	LED												
1h	SAF-TE												
2h	SES-2												
3h	GPIO (register based interface)												
Fh-4h	Reserved.												
23:16	DSIZE: Data Size. Read-write. Reset: 0. Specifies the data size in bytes. If the message (enclosure services command) has a data buffer associated with it that is transferred, the size of that data buffer is specified in this field. If there is no separate data buffer, this field shall have a value of 0. The data directly follows the message in the message buffer. To reduce the complexity, current hardware implementation treats this field as don't-care. It is defined for future use.												

15:8	MSIZE: Message Size. Read-write. Reset: 0. Specifies the size of the message in bytes. The message size does not include the one doubleword header. A value of 0 is invalid. To reduce the complexity, current hardware implementation treats this field as don't-care. It is defined for future use.
7:0	Reserved.

SATA_EMx04 Write SGPIO Register Request (I)

Bits	Description																
31:24	REG_INDX: Register Index. Read-write. Reset: 0. Specifies the index of the first register in the bank to write. Currently supported index range is: <table style="margin-left: 20px;"> <tr> <th><u>REG_TYPE</u></th> <th><u>REG_INDEX</u></th> </tr> <tr> <td>00h</td> <td>0-1</td> </tr> <tr> <td>03h</td> <td>0</td> </tr> <tr> <td>04h</td> <td>0-7</td> </tr> <tr> <td>0Ch</td> <td>0</td> </tr> </table> It is software's responsibility to make sure the index of which the first register it attempts to access is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. An out-of-range index for a specific type of register will be treated as don't care and none of the data for such index will be written.	<u>REG_TYPE</u>	<u>REG_INDEX</u>	00h	0-1	03h	0	04h	0-7	0Ch	0						
<u>REG_TYPE</u>	<u>REG_INDEX</u>																
00h	0-1																
03h	0																
04h	0-7																
0Ch	0																
23:16	REG_TYPE: Register Type. Read-write. Reset: 0. Specifies the bank of registers to write. Currently supported Register Types are: <table style="margin-left: 20px;"> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> <tr> <td>0h</td> <td>SGPIO Configuration</td> </tr> <tr> <td>2h-1h</td> <td>Reserved</td> </tr> <tr> <td>3h</td> <td>Transmit</td> </tr> <tr> <td>4h</td> <td>General Purpose Transmit</td> </tr> <tr> <td>Bh-5h</td> <td>Reserved</td> </tr> <tr> <td>Ch</td> <td>AMD Configuration</td> </tr> <tr> <td>FFh-Dh</td> <td>Reserved</td> </tr> </table> It is software's responsibility to make sure the type of registers that it attempts to access is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. This field has a second functionality when combined with SATAxF4[1:0] . It serves as the MUX select to read out the designated internal SGPIO registers to locations starting from (D11F0x24 [AHCI Base Address (BAR5)] + SATAx1C[OFST]*4 + 0Ch).	<u>Bits</u>	<u>Definition</u>	0h	SGPIO Configuration	2h-1h	Reserved	3h	Transmit	4h	General Purpose Transmit	Bh-5h	Reserved	Ch	AMD Configuration	FFh-Dh	Reserved
<u>Bits</u>	<u>Definition</u>																
0h	SGPIO Configuration																
2h-1h	Reserved																
3h	Transmit																
4h	General Purpose Transmit																
Bh-5h	Reserved																
Ch	AMD Configuration																
FFh-Dh	Reserved																
15:8	FUNC: Function. Read-write. Reset: 0. To be compatible with existing SGPIO-aware software, this field shall be set to 82h when performing any command issued to SGPIO targets. However, to reduce complexity, the current hardware implementation treats this field as don't-care.																
7:0	FRAME_TYPE: Frame Type. Read-write. Reset: 0. To be compatible with existing SGPIO-aware software, this field shall be set to 40h when performing any command issued to SGPIO targets. However, to reduce complexity, the current hardware implementation treats this field as don't-care.																

SATA_EMx08 Write SGPIO Register Request (II)

Bits	Description										
31:8	Reserved.										
7:0	<p>REG_CNT: Register Count. Read-write. Reset: 0. Specifies the number of registers starting with the specified index to write. Currently supported register count range is:</p> <table> <thead> <tr> <th><u>REG_TYPE</u></th> <th><u>REG_CNT</u></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>1-2</td> </tr> <tr> <td>03h</td> <td>1</td> </tr> <tr> <td>04h</td> <td>1-8</td> </tr> <tr> <td>0Ch</td> <td>1</td> </tr> </tbody> </table> <p>It is software's responsibility to make sure the register count is valid and supported, as hardware does not provide a mechanism to return a status to software indicating that the current operation fails. An out-of-range register count for a specific type of register will be treated as don't care and none of the data for such register count will be written.</p>	<u>REG_TYPE</u>	<u>REG_CNT</u>	00h	1-2	03h	1	04h	1-8	0Ch	1
<u>REG_TYPE</u>	<u>REG_CNT</u>										
00h	1-2										
03h	1										
04h	1-8										
0Ch	1										

SATA_EMx0C Write SGPIO Register Request (III)

Bits	Description
255:0	<p>DataRegister[7:0]: Data Register [7:0]. Read-write. Reset: 0. This field contains 256 bits of data registers ranging from (D11F0x24 [AHCI Base Address (BAR5)] + SATAx1C[OFST] * 4 + 0Ch) to (D11F0x24 [AHCI Base Address (BAR5)] + SATAx1C[OFST] * 4 + 2Bh). Once SATA_EMx04[REG_TYPE], SATA_EMx04[REG_IDX], and SATA_EMx08[REG_CNT] are specified, the values in this field will be written to the internal copy of SGPIO registers.</p>

3.26.4 USB Controllers

3.26.4.1 USB 1.1 (OHCI)

The OHCI controllers can be disabled by programming PMxEF.

3.26.4.1.1 Devices 16h, 13h, 12h Function 0 (OHCI) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D[16,13,12]F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Value: 7807h. This 16-bit field is assigned by the device manufacturer and identifies the type of device.
15:0	VendorID: vendor ID. Value: 1022h.

D[16,13,12]F0x04 Status/Command

Bits	Description
31	ParityErrorDetected: parity error detected. Read; set-by-hardware; write-1-to-clear. Reset: 0. Set by the device when it detects a parity error. This is not affected by ParityErrorEn.
30	SignaledSystemError: signaled system error. Read; set-by-hardware; write-1-to-clear. Reset: 0. Set when the device asserts SERR#.
29	ReceivedMasterAbort: received master abort. Read; set-by-hardware; write-1-to-clear. Reset: 0. Set by a master device when its transaction (except for Special Cycle) is terminated with master-abort.
28	ReceivedTargetAbort: received target abort. Read; set-by-hardware; write-1-to-clear. Reset: 0. Set by a master device when its transaction is terminated with target-abort.
27	SignaledTargetAbort: signaled target abort. Read; set-by-hardware; write-1-to-clear. Reset: 0. Set by a target device when it terminates a transaction with target-abort.
26:25	DevSelTiming: DEVSEL# timing. Value: 01b. 01b=Medium timing.
24	MasterDataParityError: master data parity error. Read; set-by-hardware; write-1-to-clear. Reset: 0.
23	FastB2BCap: fast back-to-back capable. Value: 1. 1=Fast back-to-back capable.
22	Reserved.
21	PCI66En: 66 MHz capable. Value: 1. 1=66 MHz capable.
20	CapList: capabilities list. Value: 1. 1=D[16,13,12]F0x34 [Capabilities Pointer] points to a linked list of capabilities.
19	InterruptStatus: interrupt status. Read-only. Reset: 0. 1=An INTx interrupt Message is pending in the device.
18:11	Reserved.
10	InterruptDis: interrupt disable. Read-write. Reset: 0. 0=Enable the assertion of the device/function's INTx# signal. 1=Disable the assertion of the device/function's INTx# signal.

9	FastB2BEn: fast back-to-back enable. Read-write. Reset: 0. 0=Only fast back-to-back transactions to the same agent are allowed. 1=The master is allowed to generate fast back-to-back transactions to different agents.
8	SerrEn: system error enable. Read-write. Reset: 0. 0=Disable the SERR# driver. 1=Enable the SERR# driver. Address parity errors are reported only if both SerrEn and ParityErrorEn are 1.
7	Reserved.
6	ParityErrorEn: parity error response enable. Read-write. Reset: 0. 0=The device sets D[16,13,12]F0x04[ParityErrorDetected] when an error is detected, but continues normal operations without asserting PERR#. 1=The device takes its normal action when a parity error is detected.
5	VgaPaletteRegisterAccesses: VGA palette register accesses. Value: 0. 0=Indicates the device should treat palette write accesses like all other accesses.
4	MemWriteInvalidateEn: memory write and invalidate command enable. Read-write. Reset: 0. 0=Memory write must be used. 1=Masters may use the memory write and invalidate command.
3	SpecialCycle: special cycle. Value: 0. 0=No Special Cycle support.
2	BusMasterEn: bus master enable. Read-write. Reset: 0. 0=Disable the device from generating PCI accesses. 1=Allow the device to behave as a bus master.
1	MemAccessEn: memory access enable. Read-write. Reset: 0. Specifies whether memory accesses to this device are enabled. 1=Enabled. 0=Disabled.
0	IOAccessEn: IO access enable. Read-write. Reset: 0. Specifies whether IO accesses to this device are enabled. 1=Enabled. 0=Disabled.

D[16,13,12]F0x08 Class Code/Revision ID

Bits	Description
31:24	BC: base class. Value: 0Ch. 0Ch=Device is a Serial Bus Controller.
23:16	SC: sub class. Value: 03h. 03h=Device is a Universal Serial Bus.
15:8	PI: programming interface. Value: 10h. 10h=Device is an OpenHCI Host Controller.
7:0	RevisionID: revision ID. Value: 39h.

D[16,13,12]F0x0C Miscellaneous

Bits	Description
31:24	Bist. Value: 00h. 00h=BIST is not supported.
23:16	HeaderType: header type. Value: 80h. 80h=This device contains multiple functions.
15:10	LatencyTimer[7:2]: latency timer. Read-write. Reset: 0. This field specifies, in units of PCI bus clocks, the value of the latency timer for this PCI bus master.
9:8	LatencyTimer[1:0]. Value: 0. See LatencyTimer[7:2]. LatencyTimer[1:0] are hard-wired to 00b, resulting in a timer granularity of at least four clocks.
7:0	CacheLineSize: cache line size. Read-write. Reset: 0. Specifies the system cache line size in units of doublewords.

D[16,13,12]F0x10 OHCI Base Address

Bits	Description
31:12	Bar: base address. Read-write. Reset: 0. Specifies the upper 20 bits of the 32-bit base address for the OHCI memory mapped IO registers. See 3.26.4.1.2 [OHCI Memory Mapped IO Registers] .
11:4	Reserved.
3	Pref: prefetchable. Value: 0. 0=Non-prefetchable memory region.
2:1	Type: base address register type. Value: 00b. 00b=32-bit base address register.
0	MemSpace: memory space type. Value: 0. 0=Memory mapped base address.

D[16,13,12]F0x2C Subsystem and Subvendor ID

Bits	Description
31:16	SubsystemID: subsystem ID. Write-once. Reset: 7807h.
15:0	SubsystemVendorID: subsystem vendor ID. Write-once. Reset: 1022h.

D[16,13,12]F0x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Value: D0h. Address of the first element in the capabilities linked list.

D[16,13,12]F0x3C Interrupt Line

Bits	Description
31:24	MaxLat. Value: 00h.
23:16	MinGnt. Value: 00h.
15:8	InterruptPin: interrupt pin. IF (D[16,13,12]F0x50[InterruptPinWriteEnable]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 01h. 01h=INTA#.
7:0	InterruptLine: interrupt line routing. Read-write. Reset: 0. POST software will write the interrupt routing information into this register as it initializes and configures the system.

D[16,13,12]F0x40 Miscellaneous 2

Bits	Description												
19:16	PortDisable. IF (D[16,13,12]F0x50[PortDisableWriteEn]==1) THEN Read-write. ELSE Read; write-once; write-1-only. ENDIF. Reset: 0h. 1=The corresponding port is disabled. <table style="margin-left: 20px;"> <tr> <th>Bit</th> <th>Definition</th> <th>Bit</th> <th>Definition</th> </tr> <tr> <td>[0]</td> <td>Port 0</td> <td>[2]</td> <td>Port 2</td> </tr> <tr> <td>[1]</td> <td>Port 1</td> <td>[3]</td> <td>Port 3</td> </tr> </table>	Bit	Definition	Bit	Definition	[0]	Port 0	[2]	Port 2	[1]	Port 1	[3]	Port 3
Bit	Definition	Bit	Definition										
[0]	Port 0	[2]	Port 2										
[1]	Port 1	[3]	Port 3										
15:9	Reserved.												

8	MsiDisable: MSI disable. Read-write. Reset: 1. 1=MSI capability is disabled.
7:0	TrdyTimer: TRDY timer. Read-write. Reset: 80h. Target Ready timeout for non-responding target.

D[16,13,12]F0x44 USB Battery Charger

Bits	Description
31:0	Reserved.

D[16,13,12]F0x48 Port Force Reset

Bits	Description								
7:6	Port3ForceResetEn: port 3 force reset enable. Read-write. Reset: 0. See: Port0ForceResetEn.								
5:4	Port2ForceResetEn: port 2 force reset enable. Read-write. Reset: 0. See: Port0ForceResetEn.								
3:2	Port1ForceResetEn: port 1 force reset enable. Read-write. Reset: 0. See: Port0ForceResetEn.								
1:0	Port0ForceResetEn: port 0 force reset enable. Read-write. Reset: 0. Specifies whether the port is held in reset when the system is in S3, S4, or S5. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>x0b</td> <td>Port is not held in reset when the system is in S3, S4, or S5.</td> </tr> <tr> <td>01b</td> <td>The host controller will hold the port in reset when the system is in S3, S4, or S5 and the port is not connected.</td> </tr> <tr> <td>11b</td> <td>The host controller will hold the port in reset when the system is in S3, S4, or S5 regardless of the port connection status.</td> </tr> </tbody> </table>	Bits	Definition	x0b	Port is not held in reset when the system is in S3, S4, or S5.	01b	The host controller will hold the port in reset when the system is in S3, S4, or S5 and the port is not connected.	11b	The host controller will hold the port in reset when the system is in S3, S4, or S5 regardless of the port connection status.
Bits	Definition								
x0b	Port is not held in reset when the system is in S3, S4, or S5.								
01b	The host controller will hold the port in reset when the system is in S3, S4, or S5 and the port is not connected.								
11b	The host controller will hold the port in reset when the system is in S3, S4, or S5 regardless of the port connection status.								

D[16,13,12]F0x50 OHCI Misc Control

This register is shared among all the OHCI controllers if ([D\[16,13,12\]F0x50\[ShareRegisterEnable\]==1](#)).

Bits	Description
31	PmeMergeDisable: PME merge disable. Read-write. Reset: 1. 1=Disable merging PMEs from all USB controllers.
28	ShareRegisterEnable: share register enable. Read-write. Reset: 1. 1=Enable register sharing among all OHCI and EHCI controllers. 0=Disable register sharing. When register sharing is enabled, values written to the following registers for any enabled OHCI or EHCI controller will be copied to the equivalent register in the other enabled OHCI or EHCI controller(s): <ul style="list-style-type: none"> • D[16,13,12]F0x78 • D[16,13,12]F0x7C • D[16,13,12]F0x50 • D[16,13,12]F0x80 • D[16,13,12]F2x50 • D[16,13,12]F2x54
26	FlrEnable: FLR enable. Read-write. Reset: 0. 1=Enable FLR support.
25	OhciL1BlockDisable: OHCI L1 block disable. Read-write. Reset: 0. 1=OHCI L1 block disabled. 0=Enabled.

24	OhciLoopbackControlRegisterEnable: OHCI loopback control register enable. Read-write. Reset: 0. 1=Enable the OHCI[3:1]xF0 [HC Loopback Control] register. The HcLoopBackControl register is hidden by default and can only be accessed by software when this bit is set.												
23:22	OhciPacketBufferThreshold: OHCI packet buffer threshold. Read-write. Reset: 0. BIOS: 11b. Specifies the threshold of OHCI packet buffer. <table> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>48 bytes</td> <td>10b</td> <td>200 bytes</td> </tr> <tr> <td>01b</td> <td>128 bytes</td> <td>11b</td> <td>256 bytes</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	48 bytes	10b	200 bytes	01b	128 bytes	11b	256 bytes
Bits	Definition	Bits	Definition										
00b	48 bytes	10b	200 bytes										
01b	128 bytes	11b	256 bytes										
20	OhciAdvancePlistEnable: OHCI advance Plist enable. Read-write. Reset: 0. BIOS: 1. 1=Enable advancing Plist.												
19	SofSyncEn: start of frame sync enable. Read-write. Reset: 0. BIOS: 1. 1=Enable start of frame synchronization for all OHCI controllers.												
15	OhciDisconnectDetectionTime: OHCI disconnect detection time. Read-write. Reset: 0. 1=Increase the OHCI disconnect (SE0 state) detection time to 6.16 us. 0=2.33 us.												
12	SmiHandshakeDisable: SMI handshake disable. Read-write. Reset: 1. BIOS: 0. 1=The handshake between USB and ACPI is disabled when SMI is requested by USB.												
11:10	OhciPrefetchTimeoutTimer: OHCI prefetch timeout timer. Read-write. Reset: 0. Timeout timer to purge the prefetch data in the AB data FIFO if the data is not used. <table> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>255 ms</td> <td>10b</td> <td>767 ms</td> </tr> <tr> <td>01b</td> <td>511 ms</td> <td>11b</td> <td>1023 ms</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	255 ms	10b	767 ms	01b	511 ms	11b	1023 ms
Bits	Definition	Bits	Definition										
00b	255 ms	10b	767 ms										
01b	511 ms	11b	1023 ms										
9:8	OhciPrefetchCacheLineCount: OHCI prefetch cache line count. Read-write. Reset: 3h. Number of data cache lines prefetch requests for ISO out transaction. The related logic may be removed as packet buffer size will be increased. <table> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>Prefetch is disabled.</td> <td>10b</td> <td>2 cache lines</td> </tr> <tr> <td>01b</td> <td>1 cache line</td> <td>11b</td> <td>3 cache lines</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	Prefetch is disabled.	10b	2 cache lines	01b	1 cache line	11b	3 cache lines
Bits	Definition	Bits	Definition										
00b	Prefetch is disabled.	10b	2 cache lines										
01b	1 cache line	11b	3 cache lines										
6	OHCI Cache Enable: OHCI cache enable. Read-write. Reset: 1. 1=Enable 64 byte OHCI DMA cache. The function may be removed as packet buffer size will be increased.												
5	HTMSISupportEnable: HT MSI support enable. Read-write. Reset: 0. 1=Enable HyperTransport™ MSI support.												
3	A20StateFunctionEnable: A20 state function enable. Read-write. Reset: 0. 0=Disable A20 Mask. 1=Enable A20 Mask.												
2	Reserved												
0	OHCIDynamicPowerSavingEnable: OHCI dynamic power saving enable. Read-write. Reset: 0. 1=Dynamic Power Saving for OHCI is enabled.												

D[16,13,12]F0x58 Over-Current Control 1

Bits	Description
31:20	Reserved.
19:16	Reserved. Read-only. Reset: Fh.
15:12	HSPort3OverCurrentControl: HS Port 3 OverCurrent Control. Read-only. Reset: Fh. See: HSPort0OverCurrentControl.

11:8	HSPort2OverCurrentControl: HS Port 2 OverCurrent Control. Read-only. Reset: Fh. See: HSPort0OverCurrentControl.																								
7:4	HSPort1OverCurrentControl: HS Port 1 OverCurrent Control. Read-only. Reset: Fh. See: HSPort0OverCurrentControl.																								
3:0	HSPort0OverCurrentControl: HS Port 0 OverCurrent Control. Read-only. Reset: Fh. Specifies the OverCurrent pin mapping for port 0. There are 8 OverCurrent pins (USB_OC[7:0]), any value greater than 7 will disable the OverCurrent function for port 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>USB_OC0#</td> <td>0100b</td> <td>USB_OC4#</td> </tr> <tr> <td>0001b</td> <td>USB_OC1#</td> <td>0101b</td> <td>USB_OC5#</td> </tr> <tr> <td>0010b</td> <td>USB_OC2#</td> <td>0110b</td> <td>USB_OC6#</td> </tr> <tr> <td>0011b</td> <td>USB_OC3#</td> <td>0111b</td> <td>USB_OC7#</td> </tr> <tr> <td>1111b-1000b</td> <td>Disable OverCurrent</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000b	USB_OC0#	0100b	USB_OC4#	0001b	USB_OC1#	0101b	USB_OC5#	0010b	USB_OC2#	0110b	USB_OC6#	0011b	USB_OC3#	0111b	USB_OC7#	1111b-1000b	Disable OverCurrent		
Bits	Definition	Bits	Definition																						
0000b	USB_OC0#	0100b	USB_OC4#																						
0001b	USB_OC1#	0101b	USB_OC5#																						
0010b	USB_OC2#	0110b	USB_OC6#																						
0011b	USB_OC3#	0111b	USB_OC7#																						
1111b-1000b	Disable OverCurrent																								

D[16,13,12]F0x68 OHCI Over-Current PME Enable

Bits	Description
31:5	Reserved.
4:0	OHCIOverCurrentPMEEnable[4:0]: OHCI over-current PME enable. Read-write. Reset: 0. 1=Enables the respective port to be sensitive to over-current conditions as wake-up events when it is owned by OHCI.

D[16,13,12]F0x74 Target Timeout Control

Bits	Description
31:24	TimeoutTimer: Timeout Timer. Read-write. Reset: 80h. Timer to control the purge of the delay queue when the master that has initiated the access does not return to complete the transaction. After the timer expires, the queue is invalidated and the next transaction is serviced.
23:8	Reserved.
7:0	RetryCounter: Retry Counter. Read-write. Reset: FFh. Counter to control the purge of the delay queue when the downstream access cycle is not completed within certain time. The transaction is target aborted when the counter expired. 0=The retry counter is disabled.

D[16,13,12]F0x80 OHCI Spare 1

Bits	Description
31:16	Reserved.
9	OhciFsOEFunctional. Read-write. Reset: 0. BIOS: 1. 1=Enable USB 1.1 devices to be functional when EHCI controller is disabled.
8	OHCIArbVldCtl. Read-write. Reset: 0. BIOS: See 2.15.2.5 [OHCI Arbiter Mode] . Specifies that the slot valid signal in OHCI arbiter can be cleared per slot instead of per host. 0=OHCI arbiter can only be cleared per host. 1=OHCI arbiter can be cleared per slot. This bit should be programmed to 1 when (D[16,13,12]F0x80[OHCIArbiterMode]==1xb).

7	OHCIGlobalDeepBLinkPowerSavingEnable: OHCI Global Deep B-Link Power Saving Enable. Read-write. Reset: 0. BIOS: 1. 1=OHCI will request to stop the global B-Link clock when the list processor is idle and the cache master is idle. 0=Disable.																				
6	OHCILocalDeepBLinkPowerSavingEnable: OHCI Local Deep B-Link Power Saving Enable. Read-write. Reset: 0. 1=OHCI B-Link clock will be gated when the list processor is idle and the cache master is idle. 0=Disable.																				
5:4	OHCIArbiterMode. Read-write. Reset: 0. BIOS: See 2.15.2.5 [OHCI Arbiter Mode] . OHCI Arbiter Fix Enable. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> <td>10b</td> <td>Grant Fix Enable</td> </tr> <tr> <td>01b</td> <td>Request Fix Enable</td> <td>11b</td> <td>Request + Grant Fix Enable</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Disable	10b	Grant Fix Enable	01b	Request Fix Enable	11b	Request + Grant Fix Enable								
Bits	Definition	Bits	Definition																		
00b	Disable	10b	Grant Fix Enable																		
01b	Request Fix Enable	11b	Request + Grant Fix Enable																		
3:1	OHCIL1EarlyExitTimerSelect: OHCI L1 Early Exit Timer Select. Read-write. Reset: 5h. Timer to control the OHCI L1 early exit. When OHCIL1EarlyExitEnable=1, this field selects the amount of time before SOF that the OHCI controller will request UMI to exit from L1. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>20 us</td> <td>100b</td> <td>60 us</td> </tr> <tr> <td>001b</td> <td>30 us</td> <td>101b</td> <td>70 us</td> </tr> <tr> <td>010b</td> <td>40 us</td> <td>110b</td> <td>80 us</td> </tr> <tr> <td>011b</td> <td>50 us</td> <td>111b</td> <td>90 us</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	20 us	100b	60 us	001b	30 us	101b	70 us	010b	40 us	110b	80 us	011b	50 us	111b	90 us
Bits	Definition	Bits	Definition																		
000b	20 us	100b	60 us																		
001b	30 us	101b	70 us																		
010b	40 us	110b	80 us																		
011b	50 us	111b	90 us																		
0	OHCIL1EarlyExitEnable: OHCI L1 Early Exit Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable OHCI L1 Early Exit. 0=Disable.																				

D[16,13,12]F0xD0 MSI Control

Bits	Description
31:23	Reserved.
22:20	MSIControl: MSI Control. Read-write. Reset: 0.
19:17	Reserved.
16	MSIControlOut: MSI Control Out. Read-write. Reset: 0. 1=Disable IRQ and use MSI instead.
15:8	NextItemPointer: Next Item Pointer. IF (D[16,13,12]F0x50[FlrEnable]==0 && D[16,13,12]F0x50[HTMSISupportEnable]==1) THEN Value: E4h. ELSIF (D[16,13,12]F0x50[FlrEnable]==1) THEN Value: F0h. ELSE Value: 00h. ENDIF. Pointer to next capability structure.
7:0	MSIUSB: MSI USB. Read-only. Reset: 5h. MSI USB ID.

D[16,13,12]F0xD4 MSI Address

Bits	Description
31:2	MsiAddress: MSI Address. Read-write. Reset: 0. System-specified message address.
1:0	Reserved.

D[16,13,12]F0xD8 MSI Data

Bits	Description

31:16	Reserved.
15:0	MsiData: MSI Data. Read-write. Reset: 0. System-specified message.

D[16,13,12]F0xE4 HT MSI Support

Bits	Description
31:0	HTMSISupport: HT MSI Support. IF (D[16,13,12]F0x50[HTMSISupportEnable]==0) THEN Value: 0h. ELSE Value: A803_0008h. ENDIF. For HyperTransport™ MSI support.

D[16,13,12]F0xF0 Function Level Reset Capability

Bits	Description
31:26	Reserved.
25	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE FunctionLevelResetCapability: Function Level Reset Capability. Read-only. Reset: 1. Function level reset support. ENDIF.
24	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE TransactionPendingCapability. Value: 1. 1=Transaction pending feature is supported. ENDIF.
23:16	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE Length. Read-only. Reset: 6h. AF structure length (byte). ENDIF.
15:8	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE NextItemPointer: Next Item Pointer. ENDIF. IF (D[16,13,12]F0x50[HTMSISupportEnable]==0) THEN Value: 00h. ELSE Value: E4h. ENDIF. Pointer to next capability structure. 00h=This is the final item on the list. ENDIF.
7:0	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE CapId. Value: 13h. 13h=Identifies that the function as being AF capable. ENDIF.

D[16,13,12]F0xF4 Function Level Reset Control

Bits	Description
31:9	Reserved.
8	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE TransactionPending. Read-only. Reset: 0. 1=Indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0=Indicates that all non-posted transactions have been completed. ENDIF.
7:1	Reserved.
0	IF (D[16,13,12]F0x50[FlrEnable]==0) THEN Reserved. ELSE InitiateFLR: Initiate FLR. RAZ; Write-1-only. Reset: 0. 1=Initiates Function Level Reset (FLR). ENDIF.

3.26.4.1.2 OHCI Memory Mapped IO Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. The OHCI MMIO base address is specified by D[16,13,12]F0x10[Bar]. For details of OHCI USB controller implementa-

tion requirements and behavior consult the *OpenHCI Speciation*.

OHCI[3:1]x00 HC Revision

Bits	Description
31:9	Reserved.
8	L: Legacy. Value: 1. 1=Indicates that the legacy support registers are present in this HC.
7:0	REV: Revision. Value:10h. Version of HCI specification.

OHCI[3:1]x04 HC Control

Bits	Description												
31:11	Reserved.												
10	RWE: remote wakeup enable. Read-write. Reset: 0. This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. 1=If (OHCI[3:1]x0C[RD]==1), a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.												
9	RWC: remote wakeup connected. Read-write. Reset: 0. This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.												
8	IR: interrupt routing. Read-write. Reset: 0. Specifies the routing of interrupts generated by events registered in OHCI[3:1]x0C . 0=All interrupts are routed to the normal host bus interrupt mechanism. 1=Interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.												
7:6	HCFS: host controller functional state. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>USBRESET</td> <td>10b</td> <td>USBOPERATIONAL</td> </tr> <tr> <td>01b</td> <td>USBRESUME</td> <td>11b</td> <td>USBSUSPEND</td> </tr> </tbody> </table> A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading OHCI[3:1]x0C[SF] . This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.	Bits	Definition	Bits	Definition	00b	USBRESET	10b	USBOPERATIONAL	01b	USBRESUME	11b	USBSUSPEND
Bits	Definition	Bits	Definition										
00b	USBRESET	10b	USBOPERATIONAL										
01b	USBRESUME	11b	USBSUSPEND										
5	BLE: bulk list enable. Read-write. Reset: 0. 1=Enable the processing of the Bulk list in the next frame. If cleared by HCD , processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If OHCI[3:1]x2C [HC BulkCurrent ED] is pointing to an ED to be removed, HCD must advance the pointer by updating OHCI[3:1]x2C [HC BulkCurrent ED] before re-enabling processing of the list.												

4	CLE: control list enable. Read-write. Reset: 0. 1=Enable the processing of the Control list in the next Frame. If cleared by HCD , processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If OHCI[3:1]x24 [HC Control Current ED] is pointing to an ED to be removed, HCD must advance the pointer by updating OHCI[3:1]x24 [HC Control Current ED] before re-enabling processing of the list.												
3	IE: isochronous enable. Read-write. Reset: 0. This bit is used by HCD to enable/disable processing of isochronous EDs. 1=The HC continues processing the EDs when it finds an Isochronous ED (F=1). 0=HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). Setting this bit takes effect in the next Frame (not the current Frame).												
2	PLE: periodic list enable. Read-write. Reset: 0. 1=Enable the processing of the periodic list in the next Frame. If cleared by HCD , processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.												
1:0	CBSR: control bulk service ratio. Read-write. Reset: 0. This specifies the service ratio between Control and Bulk EDs. When processing any of the non-periodic lists, HC compares the ratio specified with its internal count on how many non-empty Control EDs have been processed, in order to determine whether to continue serving another Control ED or switching to Bulk EDs. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Service Ratio</th> <th>Bits</th> <th>Service Ratio</th> </tr> <tr> <td>00b</td> <td>1:1</td> <td>10b</td> <td>3:1</td> </tr> <tr> <td>01b</td> <td>2:1</td> <td>11b</td> <td>4:1</td> </tr> </table>	Bits	Service Ratio	Bits	Service Ratio	00b	1:1	10b	3:1	01b	2:1	11b	4:1
Bits	Service Ratio	Bits	Service Ratio										
00b	1:1	10b	3:1										
01b	2:1	11b	4:1										

OHCI[3:1]x08 HC Command Status

Bits	Description
31:18	Reserved.
17:16	SOC: SchedulingOverrunCount. Read-write. Reset: 0. These bits increment on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. Increments when a scheduling overrun is detected even if OHCI[3:1]x0C[SO] has already been set. This is used by HCD to monitor any persistent scheduling problems.
15:4	Reserved.
3	OCR: OwnershipChange. Read-write. Reset: 0. When set, HC will set the OHCI[3:1]x0C[OC] . This bit is set by an OS HCD to request a change of control of the HC. After the changeover, this bit is cleared and remains so until the next request from OS HCD .
2	BLF: BulkListFilled. Read-write. Reset: 0. This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BLF. As long as (OHCI[3:1]x08[BLF]==0), HC will not start processing the Bulk list. If (OHCI[3:1]x08[BLF]==1), HC will start processing the Bulk list and will set BLF to 0. If HC finds a TD on the list, then HC will set OHCI[3:1]x08[BLF]=1 , causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.

1	CLF: ControlListFilled. Read-write. Reset: 0. This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as (OHCI[3:1]x08[CLF]==0), HC will not start processing the Control list. If (OHCI[3:1]x08[CLF]==1) the HC starts processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set OHCI[3:1]x08[CLF]=1 , causing control list processing to continue. If no TD is found on the Control list, and if the HCD does not set OHCI[3:1]x08[CLF]=1 , then OHCI[3:1]x08[CLF] will still be 0 when HC completes processing the Control list and Control list processing will stop.
0	HCR: HostControllerReset. Read; write-1-only; cleared-when-done. Reset: 0. This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USB-SUSPEND state in which most of the operational registers are reset except those stated otherwise; e.g., OHCI[3:1]x04[IR] , and no Host bus accesses are allowed. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub, and no subsequent reset signaling should be asserted to its downstream ports.

OHCI[3:1]x0C HC Interrupt Status

Bits	Description
31	Reserved.
30	OC: OwnershipChange. Read-write. Reset: 0. 1= The HC detected that the HCD set OHCI[3:1]x08[OCR] . This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.
29:7	Reserved.
6	RHSC: RootHubStatusChange. Read-write. Reset: 0. This bit is set when the content of OHCI[3:1]x50 or the content of any of OHCI[3:1]x[60:54:step4] has changed.
5	FNO: FrameNumberOverflow. Read-write. Reset: 0. This bit is set when the FrameNumber MSB OHCI[3:1]x3C[FN[15]] changes value from 0 to 1 or from 1 to 0 and after FrameNumber has been updated.
4	UE: UnrecoverableError. Read-write. Reset: 0. 1=The HC detected a system error not related to USB. HC should not proceed with any processing or signaling before the system error has been corrected. HCD clears this bit after HC has been reset.
3	RD: ResumeDetected. Read-write. Reset: 0. 1=The HC detected that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.
2	SF: StartOfFrame. Read-write. Reset: 0. This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.
1	WDH: WritebackDoneHead. Read-write. Reset: 0. This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.
0	SO: SchedulingOverrun. Read-write. Reset: 0. This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

OHCI[3:1]x10 HC Interrupt Enable

Bits	Description
31	MIE: MasterInterruptEnable. Read; write-1-only. Reset: 0. 1=Enables interrupt generation due to events specified in the other bits of this register. See corresponding field in OHCI[3:1]x14 for disable. This is used by HCD as a Master Interrupt Enable.
30	OC: OwnershipChange. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Ownership Change. See corresponding field in OHCI[3:1]x14 for disable.
29:7	Reserved.
6	RHSC: RootHubStatusChange. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Root Hub Status Change. See corresponding field in OHCI[3:1]x14 for disable.
5	FNO: FrameNumberOverflow. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Frame Number Overflow. See corresponding field in OHCI[3:1]x14 for disable.
4	UE: UnrecoverableError. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Unrecoverable Error. See corresponding field in OHCI[3:1]x14 for disable.
3	RD: ResumeDetect. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Resume Detect. See corresponding field in OHCI[3:1]x14 for disable.
2	SF: StartofFrame. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Start of Frame. See corresponding field in OHCI[3:1]x14 for disable.
1	WDH: HcDoneHeadWriteback. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to HcDoneHead Writeback. See corresponding field in OHCI[3:1]x14 for disable.
0	SO: SchedulingOverrun. Read; write-1-only. Reset: 0. 1=Enable interrupt generation due to Scheduling Overrun. See corresponding field in OHCI[3:1]x14 for disable.

OHCI[3:1]x14 HC Interrupt Disable

Reset: 8000_0000h.

Bits	Description
31	MIE: MasterInterruptEnable. Read; write-1-only. 1=Disables interrupt generation due to events specified in the other bits of this register. See corresponding field in OHCI[3:1]x10 for enable.
30	OC: OwnershipChange. Read; write-1-only. 1=Disable interrupt generation due to Ownership Change. See corresponding field in OHCI[3:1]x10 for enable.
29:7	Reserved.
6	RHSC: RootHubStatusChange. Read; write-1-only. 1=Disable interrupt generation due to Root Hub Status Change. See corresponding field in OHCI[3:1]x10 for enable.
5	FNO: FrameNumberOverflow. Read; write-1-only. 1=Disable interrupt generation due to Frame Number Overflow. See corresponding field in OHCI[3:1]x10 for enable.
4	UE: UnrecoverableError. Read; write-1-only. 1=Disable interrupt generation due to Unrecoverable Error. See corresponding field in OHCI[3:1]x10 for enable.
3	RD: ResumeDetect. Read; write-1-only. 1=Disable interrupt generation due to Resume Detect. See corresponding field in OHCI[3:1]x10 for enable.
2	SF: StartofFrame. Read; write-1-only. 1=Disable interrupt generation due to Start of Frame. See corresponding field in OHCI[3:1]x10 for enable.

1	WDH: HcDoneHeadWriteback. Read; write-1-only. 1=Disable interrupt generation due to HcDone-Head Writeback. See corresponding field in OHCI[3:1]x10 for enable.
0	SO: SchedulingOverrun. Read; write-1-only. 1=Disable interrupt generation due to Scheduling Overrun. See corresponding field in OHCI[3:1]x10 for enable.

OHCI[3:1]x18 HC HCCA

Bits	Description
31:8	HCCA: HostControllerCommunicationArea. Read-write. Reset: 0. This is the base address of the Host Controller Communication Area
7:0	Reserved.

OHCI[3:1]x1C HC Period Current ED

Bits	Description
31:4	PCED: PeriodCurrentED. Read-write. Reset: 0. This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.
3:0	Reserved.

OHCI[3:1]x20 HC Control Head ED

Bits	Description
31:4	CHED: ControlHeadED. Read-write. Reset: 0. HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	Reserved.

OHCI[3:1]x24 HC Control Current ED

Bits	Description
31:4	CCED: ControlCurrentED. Read-write. Reset: 0. This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to 0 to indicate the end of the Control list.
3:0	Reserved.

OHCI[3:1]x28 HC Bulk Head ED

Bits	Description

31:4	BHED: BulkHeadED. Read-write. Reset: 0. HC traverses the Bulk list starting with the HcBulk-HeadED pointer. The content is loaded from HCCA during the initialization of HC.
3:0	Reserved.

OHCI[3:1]x2C HC BulkCurrent ED

Bits	Description
31:4	BCED: BulkCurrentED. Read-write. Reset: 0. This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to 0 to indicate the end of the Bulk list.
3:0	Reserved.

OHCI[3:1]x30 HC Done Head

Bits	Description
31:4	DH: DoneHead. Read-write. Reset: 0. When a TD is completed, HC writes the content of HcDone-Head to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to 0 whenever HC writes the content of this register to HCCA. It also sets OHCI[3:1]x0C[WDH] .
3:0	Reserved.

OHCI[3:1]x34 HC Frame Interval

Bits	Description
31	FIT: frame interval toggle. Read-write. Reset: 0. HCD toggles this bit whenever it loads a new value to OHCI[3:1]x34[FI] .
30:16	FSMPS: FS largest data packet. Read-write. Reset: 0. This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD .
15:14	Reserved.
13:0	FI: frame interval. Read-write; updated-by-hardware. Reset: 2EDFh. This specifies the interval between two consecutive SOFs in bit times. HCD should store the current value of this field before resetting HC. Programming OHCI[3:1]x08[HCR]=1 causes the HC to overwrite this field with the reset value. HCD may choose to restore the stored value upon the completion of the reset sequence.

OHCI[3:1]x38 HC Frame Remaining

Bits	Description

31	FRT: FrameRemainingToggle. Read-only. Reset: 0. This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.
30:14	Reserved.
13:0	FR: FrameRemaining. Read-only. Reset: 0. This counter is decremented at each bit time. When it reaches 0, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval field of HcFmInterval and uses the updated value from the next SOF.

OHCI[3:1]x3C HC Frame Number

Bits	Description
31:16	Reserved.
15:0	FN[15:0]: FrameNumber. Read-only. Reset: 0. This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after FFFFh. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set OHCI[3:1]x0C[SF] .

OHCI[3:1]x40 HC Periodic Start

Bits	Description
31:14	Reserved.
13:0	PS: PeriodicStart. Read-write. Reset: 0. This bit is set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the interrupt list after completing the current Control or Bulk transaction that is in progress.

OHCI[3:1]x44 HC LS Threshold

Bits	Description
31:12	Reserved.
11:0	LST: LSThreshold. Read-write. Reset: 628h. This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining is equal or greater than this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

OHCI[3:1]x48 HC RH Descriptor A

Table 232: [OHCI\[3:1\]x48](#) reset values

Register	Reset
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Table 232: OHCI[3:1]x48 reset values

OHCI1x48	0200_0B04h
OHCI2x48	0200_0B04h
OHCI3x48	0200_0B02h

Bits	Description
31:24	POTPGT: PowerOnToPowerGoodTime. Read-write. This field specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23:13	Reserved.
12	NOCP: NoOverCurrentProtection. Read-write. Specifies how the over-current status for the Root Hub ports is reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting. 0=Over-current status is reported collectively for all downstream ports. 1=No over-current protection supported.
11	OCPM: OverCurrentProtectionMode. Read-write. Specifies how the over-current status for the Root Hub ports are reported. At reset, this field should reflect the same mode as PSM. This field is valid only if (OHCI[3:1]x48[NOCP]==0). 0=Over-current status is reported collectively for all downstream ports. 1=Over-current status is reported on a per-port basis.
10	DT: DeviceType. Value: 0. 0=Specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device.
9	NPS: NoPowerSwitching. Read-write. Reset: 1. Specifies whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PSM specifies global or per-port switching. 0=Ports are power switched. 1=Ports are always powered on when the HC is powered on.
8	PSM: PowerSwitchingMode. Read-write. Reset: 1. Specifies how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0>All ports are powered at the same time. 1=Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the OHCI[3:1]x4C[PPCM] bit is set, the port responds only to port power commands (SetPortPower/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (SetGlobalPower/ClearGlobalPower).
7:0	NDP: NumberDownstreamPorts. Read-only. Specifies the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15. Note: For OHCI 1/OHCI 2 (device-13h:12h, func-0), each OHCI controller owns 4 downstream ports. OHCI 3 (device-16h, func-0) owns 2 downstream ports.

OHCI[3:1]x4C HC RH Descriptor B

Bits	Description

31:16	PPCM: PortPowerControlMask. Read-write. Reset: 0. Each bit indicates if a port is affected by a global power control command when PSM is set. 1=The port's power state is only affected by per-port power control (SetPortPower/ClearPortPower). 0=The port is controlled by the global power switch (SetGlobalPower/ClearGlobalPower). If (OHCI[3:1]x48[PSM]==0), this field is not valid. <table border="0" style="width: 100%;"><tr><td style="width: 10px;"><u>Bit</u></td><td style="width: 10px;"><u>Definition</u></td></tr><tr><td>[0]</td><td>Reserved</td></tr><tr><td>[1]</td><td>Ganged-power mask on Port #1</td></tr><tr><td>[2]</td><td>Ganged-power mask on Port #2</td></tr><tr><td>[14:3]</td><td>...</td></tr><tr><td>[15]</td><td>Ganged-power mask on Port #15</td></tr></table>	<u>Bit</u>	<u>Definition</u>	[0]	Reserved	[1]	Ganged-power mask on Port #1	[2]	Ganged-power mask on Port #2	[14:3]	...	[15]	Ganged-power mask on Port #15
<u>Bit</u>	<u>Definition</u>												
[0]	Reserved												
[1]	Ganged-power mask on Port #1												
[2]	Ganged-power mask on Port #2												
[14:3]	...												
[15]	Ganged-power mask on Port #15												
15:0	DR: DeviceRemovable. Read-write. Reset: 0. Each bit is dedicated to a port of the Root Hub. 0=The attached device is removable. 1=The attached device is not removable. <table border="0" style="width: 100%;"><tr><td style="width: 10px;"><u>Bit</u></td><td style="width: 10px;"><u>Definition</u></td></tr><tr><td>[0]</td><td>Reserved</td></tr><tr><td>[1]</td><td>Device attached to Port #1</td></tr><tr><td>[2]</td><td>Device attached to Port #2</td></tr><tr><td>[14:3]</td><td>...</td></tr><tr><td>[15]</td><td>Device attached to Port #15</td></tr></table>	<u>Bit</u>	<u>Definition</u>	[0]	Reserved	[1]	Device attached to Port #1	[2]	Device attached to Port #2	[14:3]	...	[15]	Device attached to Port #15
<u>Bit</u>	<u>Definition</u>												
[0]	Reserved												
[1]	Device attached to Port #1												
[2]	Device attached to Port #2												
[14:3]	...												
[15]	Device attached to Port #15												

OHCI[3:1]x50 HC RH Status

Bits	Description
31	CRWE: ClearRemoteWakeupsEnable. RAZ; write-1-only. Reset: 0. Writing a 1 clears DeviceRemoveWakeupsEnable.
30:18	Reserved.
17	OCIC: OverCurrentIndicatorChange. Read; write-1-to-clear. Reset: 0. 1=A change of state occurred in OHCI[3:1]x50[OCI] .
16	LPSC: LocalPowerStatusChange. RAZ; write. Reset: 0. IF (READ) THEN LocalPowerStatusChange. The Root Hub does not support the local power status feature; this bit is always read as 0. ELSE SetGlobalPower. In global power mode (OHCI[3:1]x48[PSM]==0), this bit is written to 1 to turn on power to all ports (clear PortPowerStatus). In per-port power mode (OHCI[3:1]x48[PSM]==1), it sets PortPowerStatus only on ports whose (OHCI[3:1]x4C[PPCM]==0). ENDIF.
15	DRWE: DeviceRemoteWakeupsEnable. Read-write. Reset: 0. IF (READ) THEN DeviceRemoteWakeupsEnable. This bit enables the ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. 0=ConnectStatusChange is not a remote wakeup event. 1=ConnectStatusChange is a remote wakeup event. ELSE SetRemoteWakeupsEnable. 1=Set DeviceRemoveWakeupsEnable. 0=No effect. ENDIF.
14:2	Reserved.
1	OCI: OverCurrentIndicator. Read-only. Reset: 0. This bit reports over-current conditions when the global reporting is implemented. 1=An over-current condition exists. 0=All power operations are normal. If per-port over-current protection is implemented, this bit is always 0

0	<p>LPS: LocalPowerStatus. RAZ; write. Reset: 0.</p> <p>IF (READ) THEN LocalPowerStatus. The Root Hub does not support the local power status feature and this bit is always read as 0.</p> <p>ELSE ClearGlobalPower. In global power mode (OHCI[3:1]x48[PSM]==0), writing 1 to this bit turns off power to all ports (clear PortPowerStatus). In per-port power mode (OHCI[3:1]x48[PSM]==1), it clears PortPowerStatus only on ports whose (OHCI[3:1]x4C[PPCM]==0). ENDIF.</p>
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OHCI[3:1]x[60:54:step4] HC RH Port Status [4:1]

Bits	Description
31:21	Reserved. Read-write.
20	PRSC: PortResetStatusChange. Read; write-1-to-clear. Reset: 0. This bit is set at the end of the 10 ms port reset signal. 0=Port reset is not complete. 1=Port reset is complete.
19	OCIC: PortOverCurrentIndicatorChange. Read; write-1-to-clear. Reset: 0. This bit is valid only if over-current conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. 0>No change in PortOverCurrentIndicator. 1=PortOverCurrentIndicator has changed.
18	PSSC: PortSuspendStatusChange. Read; write-1-to-clear. Reset: 0. This bit is set when the full resume sequence has been completed. This sequence includes the 20 s resume pulse, LS EOP, and 3 ms resynchronization delay. This bit is also cleared when ResetStatusChange is set. 0=Resume is not completed. 1=Resume completed.
17	PESC: PortEnableStatusChange. Read; write-1-to-clear. Reset: 0. This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. 0>No change in PortEnableStatus. 1=Change in PortEnableStatus.
16	CSC: ConnectStatusChange. Read; write-1-to-clear. Reset: 0. This bit is set whenever a connect or disconnect event occurs. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0>No change in CurrentConnectStatus. 1=Change in CurrentConnectStatus. Note: If the OHCI[3:1]x4C[DR] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.
15:10	Reserved. Read-write.
9	LSDA. Read; write-1-only. Reset: X. IF (READ) THEN LowSpeedDeviceAttached. This field is valid only when the CurrentConnectStatus is set. This bit indicates the speed of the device attached to this port. 1=A Low Speed device is attached to this port. 0=A Full Speed device is attached to this port. ELSE ClearPortPower. Writing 1 to this bit clears the PortPowerStatus bit. Writing 0 has no effect. ENDIF.

8	<p>PPS. Read; write-1-only. Reset: 0.</p> <p>IF (READ) THEN PortPowerStatus. This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an over-current condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PSM and OHCI[3:1]x4C[PPCM]. In global switching mode, (PSM=0), only SetGlobalPower/ClearGlobalPower controls this bit. In per-port power switching (PSM=1), if the OHCI[3:1]x4C[PPCM] bit for the port is set, only SetPortPower/ClearPortPower commands are enabled. If the mask is not set, only SetGlobalPower/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0=Port power is off. 1=Port power is on.</p> <p>ELSE SetPortPower. Writing 1 to this bit sets the PortPowerStatus bit. Writing 0 has no effect.</p> <p>ENDIF.</p> <p>Note: This bit always reads 1b if power switching is not supported.</p>
7:5	Reserved. Read-write.
4	<p>PRS. Read; write-1-only. Reset: 0.</p> <p>IF (READ) THEN PortResetStatus. When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0=Port reset signal is not active. 1=Port reset signal is active.</p> <p>ELSE SetPortReset. The HCD sets the port reset signaling by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</p> <p>ENDIF.</p>
3	<p>POCI. Read-write. Reset: 0.</p> <p>IF (READ) THEN PortOverCurrentIndicator. This bit is only valid when the Root Hub is configured in such a way that over-current conditions are reported on a per-port basis. If per-port over-current reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an over-current condition exists on this port. This bit always reflects the over-current input signal. 0=No over-current condition. 1=Over-current condition detected.</p> <p>ELSE ClearSuspendStatus. The HCD writes a 1 to initiate a resume. Writing a 0 has no effect. A resume is initiated only if PortSuspendStatus is set.</p> <p>ENDIF.</p>
2	<p>PSS. Read-write. Reset: 0.</p> <p>IF (READ) THEN PortSuspendStatus. This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC. 0=Port is not suspended. 1=Port is suspended.</p> <p>ELSE SetPortSuspend. The HCD sets the PortSuspendStatus bit by writing a 1 to this bit. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.</p> <p>ENDIF.</p>

1	<p>PES. Read-write. Reset: 0.</p> <p>IF (READ) THEN PortEnableStatus. This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an over-current condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0=Port is disabled. 1=Port is enabled.</p> <p>ELSE SetPortEnable. The HCD sets PortEnableStatus by writing a 1. Writing a 0 has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.</p> <p>ENDIF.</p>
0	<p>CCS. Read-write. Reset: 0.</p> <p>IF (READ) THEN CurrentConnectStatus. This bit reflects the current state of the downstream port. 0=No device connected. 1=Device connected.</p> <p>ELSE ClearPortEnable. The HCD writes a 1 to this bit to clear the PortEnableStatus bit. Writing a 0 has no effect. CurrentConnectStatus is not affected by any write.</p> <p>ENDIF.</p> <p>Note: This bit is always read 1b when the attached device is nonremovable (OHCI[3:1]x4C[DR]).</p>

OHCI[3:1]xF0 HC Loopback Control

Reset: 0000_0000h.

IF ([D\[16,13,12\]F0x50](#)[OhciLoopbackControlRegisterEnable]==1) THEN then this register is defined; otherwise it is reserved. ENDIF.

Bits	Description										
31	<p>LoopBackTestDone. Read-only. 1=Loop back is done. Cleared when software clears LoopBackTestStart.</p>										
30:16	<p>LoopBackTestStatus. Read-only. Specifies the loop back test status for the port under test. For each bit, 0=Fail. 1=Pass. Software can only check these status bits when LoopBackTestDone is set by the host controller. These bits can only be cleared when software clears LoopBackTestStart.</p> <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Port 0</td> </tr> <tr> <td>[1]</td> <td>Port 1</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>[14]</td> <td>Port 14</td> </tr> </tbody> </table>	Bit	Definition	[0]	Port 0	[1]	Port 1	[14]	Port 14
Bit	Definition										
[0]	Port 0										
[1]	Port 1										
...	...										
[14]	Port 14										
15:8	<p>LoopBackTestData. Read-write. 1-byte test data pattern for transmit and receive logic check the received data to match with this data pattern.</p>										
7:4	<p>PortUnderTest: Port Under Test. Read-write. Software selects the port under test through these bits. Software should only program the port number to the range of ports that OHCI supports.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Port 0</td> </tr> <tr> <td>1h</td> <td>Port 1</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>Fh</td> <td>Port 15</td> </tr> </tbody> </table>	Bits	Definition	0h	Port 0	1h	Port 1	Fh	Port 15
Bits	Definition										
0h	Port 0										
1h	Port 1										
...	...										
Fh	Port 15										
3:1	Reserved.										

0	LoopBackTestStart . Read-write. 1=Start the loop back test. 0=Clear out all the test status before starting the next loop.
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OHCI[3:1]x100 HCE Control

Reset: 0000_0000h.

Bits	Description
31:9	Reserved.
8	A20State . Read-write. Indicates current state of Gate A20 on keyboard controller. Used to compare against value written to 60h when GateA20Sequence is active.
7	IRQ12Active . Read; write-1-to-clear. 1=A positive transition on IRQ12 from the keyboard controller has occurred.
6	IRQ1Active . Read; write-1-to-clear. 1=A positive transition on IRQ1 from the keyboard controller has occurred.
5	GateA20Sequence . Read-write. Set by HC when (IO port64h==D1h). Cleared by HC on write to (IO port 64h!=D1h).
4	ExternalIRQEn . Read-write. 1=Enable IRQ1 and IRQ12 from the keyboard controller to cause an emulation interrupt. The function controlled by this bit is independent of the setting of the Emulation-Enable bit in this register.
3	IRQEn . Read-write. 1=Enable the HC generation of IRQ1 or IRQ12 as long as the (OHCI[3:1]x10C[OutputFull] ==1). IF (OHCI[3:1]x10C[AuxOutputFull] ==0) THEN IRQ1 is generated. ELSE IRQ12 is generated.
2	CharacterPending . Read-write. 1=An emulation interrupt is generated when the OutputFull bit of the HceStatus register is set to 0.
1	EmulationInterrupt . Read-only. This bit is a static decode of the emulation interrupt condition.
0	EmulationEnable . Read-write. 1=Enable HC legacy keyboard and mouse emulation. The HC decodes accesses to IO registers 60h and 64h and generates IRQ1 and/or IRQ12 when appropriate. Additionally, the HC generates an emulation interrupt at appropriate times to invoke the emulation software.

OHCI[3:1]x104 HCE Input

Bits	Description
31:8	Reserved.
7:0	InputData . Read-write. Reset: 0. This register holds data that is written to IO ports 60h and 64h.

OHCI[3:1]x108 HCE Output

Bits	Description
31:8	Reserved.
7:0	OutputData . Read-write. Reset: 0. This register hosts data that is returned when an IO read of port 60h is performed by application software.

OHCI[3:1]x10C HCE Status

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7	Parity. Read-write. 1=Indicates parity error on keyboard/mouse data.
6	TimeOut. Read-write. 1=Indicates a timeout.
5	AuxOutputFull. Read-write. IRQ12 is asserted whenever this bit is set to 1 and OutputFull is set to 1 and the IRQEn bit is set.
4	InhibitSwitch. Read-write. This bit reflects the state of the keyboard inhibit switch and is set if the keyboard is NOT inhibited.
3	CmdData. Read-write. The HC sets this bit to 0 on an IO write to port 60h and to 1 on an IO write to port 64h.
2	Flag. Read-write. Nominally used as a system flag by software to indicate a warm or cold boot.
1	InputFull. Read-write. Except for the case of a Gate A20 sequence, this bit is set to 1 on an IO write to address 60h or 64h. While this bit is set to 1 and emulation is enabled, an emulation interrupt condition exists.
0	OutputFull. Read-write. The HC sets this bit to 0 on a read of IO port 60h. If IRQEn is set and AuxOutputFull is set to 0, then an IRQ1 is generated as long as this bit is set to 1. If IRQEn is set and AuxOutputFull is set to 1, then an IRQ12 is generated as long as this bit is set to 1. While this bit is 0 and CharacterPending in HceControl is set to 1, an emulation interrupt condition exists.

3.26.4.2 USB 2.0 (EHCI)The EHCI controllers can be disabled by programming **PMxEF**.**3.26.4.2.1 Devices 16h, 13h, 12h Function 2 (EHCI) Configuration Registers**

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D[16,13,12]F2x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: Device ID. Read-only. Reset: 7808h. This 16-bit field is assigned by the device manufacturer and identifies the type of device.
15:0	VendorID: Vendor ID. Read-only. Reset: 1022h.

D[16,13,12]F2x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; write-1-to-clear. Reset: 0. 1=The EHCI controller detects a parity error.

30	SignaledSystemError: Signaled System Error. Read; write-1-to-clear. Reset: 0. 1=The EHCI controller asserted SERR#.
29	ReceivedMasterAbort: Received Master Abort. Read; write-1-to-clear. Reset: 0. 1=The EHCI controller received a PCI master abort while acting as a PCI master.
28	ReceivedTargetAbort: Received Target Abort. Read; write-1-to-clear. Reset: 0. 1=The EHCI controller generated PCI cycle (EHCI controller is the PCI master) is aborted by a PCI target.
27	SignaledTargetAbort: Signaled Target Abort. Read; write-1-to-clear. Read. Reset: 0. 1=The EHCI controller signals Target Abort.
26:25	DEVSELtiming: DEVSEL timing. Value: 01b. 01b=Medium timing.
24	MasterDataParityError: Master Data Parity Error. Read; write-1-to-clear. Reset: 0. 1=EHCI controller detects PERR# being asserted while acting as PCI master, regardless whether PERR# was driven by EHCI controller or not.
23	FastBack2BackCapable: Fast Back-to-Back Capable. Value: 1. 1=Indicates Fast Back-to-Back capable.
22	Reserved.
21	Capable66MHz: 66 MHz Capable. Value: 1. 1=Indicates 66 MHz capable.
20	CapabilitiesList: Capabilities List. Read-only. Reset: 1. 0=Indicates that no New Capabilities linked list is available. 1=Indicates that the value read at D[16,13,12]F2x34 [Capability Pointer] is a pointer in Configuration Space to a linked list of new capabilities.
19	InterruptStatus: Interrupt Status. Read-only. Reset: 0. This bit reflects the state of the interrupt in the device/function. Only when (D[16,13,12]F2x04[InterruptDisable]==0) and this bit is 1, will the device/function's INTx# signal be asserted. Setting (D[16,13,12]F2x04[InterruptDisable]==1) has no effect on the state of this bit.
18:11	Reserved.
10	InterruptDisable: Interrupt Disable. Read-write. Reset: 0. 0=Enable the assertion of the device/function's INTx# signal. 1=Disable the assertion of the device/function's INTx# signal.
9	FastBack2BackEnable: Fast Back-to-Back Enable. Read-write. Reset: 0. 0=Only fast back-to-back transactions to the same agent are allowed. 1=The master is allowed to generate fast back-to-back transactions to different agents.
8	SERREnable: SERR# Enable. Read-write. Reset: 0. 0=Disable the SERR# driver. 1=Enable the SERR# driver. Address parity errors are reported only if this bit and ParityEnable are 1.
7	RAZ. Hard-wired to 0 per PCI2.3 spec.
6	ParityEnable: Parity Enable. Read-write. Reset: 0. 0=The device sets its DetectedParityError bit when an error is detected, but continues normal operations without asserting PERR#. 1=The device must take its normal action when a parity error is detected.
5	VgaPaletteRegisterAccesses: VGA palette register accesses. Value: 0. 0=The device treats palette write accesses the same as other accesses.
4	MemoryWriteAndInvalidateCommand: Memory Write and Invalidate Command. Read-write. Reset: 0. 0=Memory Write must be used. 1=Masters may generate the command.
3	SpecialCycle: Special Cycle. Value: 0. 0=Indicates no Special Cycle support.
2	BusMaster: Bus Master. Read-write. Reset: 0. 0=Disable the device from generating PCI accesses. 1=Allow the device to behave as a bus master.
1	MemorySpaceAccesses: Memory Space Accesses. Read-write. Reset: 0. 0=Disable the device response. 1=Allow the device to respond to memory space accesses.

0	IOSpaceAccesses: IO Space Accesses. Read-write. Reset: 0. 0=Disable the device response. 1=Allow the device to respond to IO space accesses.
---	---

D[16,13,12]F2x08 Revision ID / Class Code

Bits	Description
31:24	BC: Base Class. Value: 0Ch. 0Ch=Identifies the device being a Serial Bus Controller.
23:16	SC: Sub Class. Value: 3h. Sub Class. 03h=Identifies the device being of Universal Serial Bus.
15:8	PI: Programming Interface. Value: 20h. 20h=Identifies the device being an EHCI Host Controller.
7:0	RevisionID: Revision ID. Value: 39h.

D[16,13,12]F2x0C Miscellaneous

Bits	Description
31:24	Bist. Value: 0. 00h=BIST is not supported.
23:16	HeaderType: Header Type. Value: 00h. This field identifies the layout of the second part of the pre-defined header (beginning at byte 10h in Configuration Space) and also whether or not the device contains multiple functions. 00h=Indicates EHCI is single function.
15:8	LatencyTimer[7:0]: Latency Timer. Read-only. Reset: 0. LatencyTimer[1:0] are hard-wired to 00b, resulting in a timer granularity of at least four clocks. This field specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master.
7:0	CacheLineSize: Cache Line Size. Read-write. Reset: 0. Specifies the system cache line size in units of doublewords .

D[16,13,12]F2x10 BAR_EHCI

Bits	Description
31:8	BA: Base Address[31:8]. Read-write. Reset: 0. Specifies the MMIO Base address of the EHCI USB controller. See 3.26.4.2.2 [EHCI Memory Mapped IO Registers] .
7:4	Reserved.
3	PM: Prefetch Memory. Value: 0. 0=Non-prefetchable memory region.
2:1	Type: base address register type. Read-only. Reset: 00b. 00b=32-bit base address register.
0	MemSpace: memory space type. Read-only. Reset: 0. 0=Memory mapped base address.

D[16,13,12]F2x2C Subsystem ID / Subsystem Vendor ID

Bits	Description
31:16	SubsystemID. Read; Write-once. Reset: 7808h.
15:0	SubsystemVendorID. Read; Write-once. Reset: 1022h.

D[16,13,12]F2x34 Capability Pointer

Bits	Description
31:8	Reserved.
7:0	CapabilityPointer: Capability Pointer. Read-only. IF (D[16,13,12]F2x50[PMEDisable]==0) THEN Reset: C0h. ELSEIF (D[16,13,12]F2x50[MSIDisable]==0) THEN Reset: D0h. ELSEIF ((EHC[3:1]xA0[EnableDebugPortNumberReMapping]==0 EHC[3:1]xA0[DebugPortNumberReMapping]!=0) THEN Reset: E4h. ELSEIF (D[16,13,12]F2x50[FlrEn]==1) THEN Reset: F0h. ELSE Reset: 00h. ENDIF. Specifies the address of the first element of capability link.

D[16,13,12]F2x3C Interrupt Line

Bits	Description
31:24	MaxLat. Value: 00h.
23:16	MinGnt. Value: 00h.
15:8	InterruptPin: Interrupt Pin. IF (D[16,13,12]F0x50[InterruptPinWriteEnable]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 2h. 02h=INTB#.
7:0	InterruptLine: Interrupt Line. Read-write. Reset: 0. Identifies which input on the interrupt controller the function's PCI interrupt request pin is routed to.

D[16,13,12]F2x50 EHCI Misc Control

This register is shared among all the EHCI controllers if (D[16,13,12]F0x50[ShareRegisterEnable]==1).

Bits	Description
31	PHYAdvancePowerSavingEnable: PHY Advance Power Saving Enable. Read-write. Reset: 1. 1=Enable the advance PHY power saving feature to save active power from the USB PHY.
28	DisableAsyncQHCacheEnhancement: Disable Async QH Cache Enhancement. Read-write. Reset: 0. 1=Disable async QH/QTD cache enhancement.
27	DisablePeriodicListCache: Disable Periodic List Cache. Read-write. Reset: 0. 1=Disable periodic list cache.
26	DisableAsyncDataCache: Disable Async Data Cache. Read-write. Reset: 0. 1=Disable async data cache request.
25	DisableAsyncQHCache: Disable Async QH Cache. Read-write. Reset: 0. 1=Disable async QH/QTD cache.
24	AsyncQHCacheThresholdControl: Async QH Cache Threshold Control. Read-write. Reset: 0. For OUT, 0=Cache only if packet size is greater than 128 Bytes. 1=Cache only if packet size is greater than 64 Bytes. For IN, 0=Cache only if expected packet size is greater than 192 Bytes. 1=Cache only if expected packet size is greater than 96 Bytes.
23	AsyncParkDisable: async-park disable. Read-write. Reset: 0. 1=Disable async-park mode.
22	Reserved.
21	EnableIPGapExt: Enable InterPacket Gap Extension. Read-write. Reset: 1. 1=Enable interpacket gap extension in PIE idle state on starting a new transaction.

20	Reserved.								
19	QualifyCacheHit: Qualify Cache Hit. Read-write. Reset: 0. BIOS: 1. 1=Qualify cache hit with EHCI_RDWRN command.								
18	Reserved.								
17	AsyncParkCacheControl: Async Park Cache Control. Read-write. Reset: 1. 1=Enable async park cache control.								
15:12	AsyncParkOUTControl: Async Park OUT Control. Read-write. Reset: 1. Async Park Mode Count for OUT Packet. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Standard count as specified by EHCI[3:1]x20[AsyncScheduleParkModeCount].</td> </tr> <tr> <td>1h</td> <td>8 packets.</td> </tr> <tr> <td>Fh-2h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0h	Standard count as specified by EHCI[3:1]x20[AsyncScheduleParkModeCount] .	1h	8 packets.	Fh-2h	Reserved.
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1h	8 packets.								
Fh-2h	Reserved.								
11:8	AsyncParkINControl: Async Park IN Control. Read-write. Reset: 1. Async Park Mode Count for IN Packet.. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Standard count as specified by EHCI[3:1]x20[AsyncScheduleParkModeCount].</td> </tr> <tr> <td>1h</td> <td>8 packets.</td> </tr> <tr> <td>Fh-2h</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	0h	Standard count as specified by EHCI[3:1]x20[AsyncScheduleParkModeCount] .	1h	8 packets.	Fh-2h	Reserved.
Bits	Definition								
0h	Standard count as specified by EHCI[3:1]x20[AsyncScheduleParkModeCount] .								
1h	8 packets.								
Fh-2h	Reserved.								
7	EnablePerPortChangeEventsCapability: Enable Per-Port Change Events Capability. Read-write. Reset: 0. Enable the support of Per-Port Change Event Capability. 1=Set EHCI[3:1]x08[PerPortChangeEventCapability] to 1. 0=Clear EHCI[3:1]x08[PerPortChangeEventCapability] to 0.								
6	MSIDisable: MSI Disable. Read-write. Reset: 0. BIOS: 1. 1=Disable MSI support.								
5	PMEDisable: PME Disable. Read-write. Reset: 0. 1=Disable PME support.								
4	EhciPmeLevelSignalByResumeWakeupEnable: EHCI PME level signal by resume-wakeup enable. Read-write. Reset: 0. 1=PME is a level signal instead of pulse when resume wake-up event is detected.								
2	FlrEn: FLR Enable. Read-write. Reset: 0. 1=Enable FLR support.								
1	DisableSMI: disable SMI. Read-write. Reset: 0. 1=Disable EHCI_SMI sent to USB SMI output (to ACPI). 0=Enable.								
0	D3ColdPMEsupport: D3Cold PME support. Read-write. Reset: 0. BIOS: 1. 1=Enable EHCI host controller PME support at D3Cold. 0=Disable.								

D[16,13,12]F2x54 EHCI Spare 1

This register is shared among all the EHCI controllers if ([D\[16,13,12\]F0x50\[ShareRegisterEnable\]](#)==1).

Bits	Description
31	Reserved.
26	EnMaskIntrOfD0: Enable masking interrupt out of D0 state. Read-write. Reset: 0. 0=Disable masking interrupt for all state, including D3hot. 1=Enable masking interrupt out of D0 state.
14	Reserved
10	ResumePmeD123En: Resume PME in D123 Enable. Read-write. Reset: 0. 1=PME Status will be set only in non-D0 state when resume occurs.

9:7	EhciL1EarlyExitTimer: EHCI L1 early exit timer. Read-write. Reset: 5h. BIOS: 100b. Timer to control EHCI L1 exit. When EhciL1EarlyExitEnable is set to 1, this field selects the amount of time before SOF that the EHCI controller will request UMI to exit from L1.																				
	<table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>20 us</td><td>100b</td><td>60 us</td></tr> <tr> <td>001b</td><td>30 us</td><td>101b</td><td>70 us</td></tr> <tr> <td>010b</td><td>40 us</td><td>110b</td><td>80 us</td></tr> <tr> <td>011b</td><td>50 us</td><td>111b</td><td>90 us</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	20 us	100b	60 us	001b	30 us	101b	70 us	010b	40 us	110b	80 us	011b	50 us	111b	90 us
Bits	Definition	Bits	Definition																		
000b	20 us	100b	60 us																		
001b	30 us	101b	70 us																		
010b	40 us	110b	80 us																		
011b	50 us	111b	90 us																		
6	EhciL1EarlyExitMode: Ehci L1 early exit mode. Read-write. Reset: 0. BIOS: 1. Mode selection bit for EHCI L1 early exit function. 0=Exit signal active in every uFrame if PDC schedule is enabled. 1=Exit signal active in current uFrame when detecting next uFrame has active PDC work.																				
5	EhciL1EarlyExitEnable: EHCI L1 early exit enable. Read-write. Reset: 0. BIOS: 1. 0=Disable. 1=Enable.																				
4	LSConnectionWakeUpEnable: LS connection wake up enable. Read-write. Reset: 1. 1=Enable wake up from S states for Low Speed (LS) connection. 0=Disable.																				
3	EhciEmptyListMode: EHCI empty list mode. Read-write. Reset: 1. 1=Enable empty list mode. 0=Disable.																				
2	EhciBlockCStateEnable: EHCI block-C-state enable. Read-write. Reset: 0. 1=Enable EHCI sending block-C-state signal to ACPI.																				
0	EhciDelayBifL1Enable: EHCI delay BIF L1 enable. Read-write. Reset: 0. 1=Enable EHCI delaying BIF on entering L1 when there are USB transactions on the controller and when USB delaying BIF L1 is enabled in A-link bridge.																				

D[16,13,12]F2x60 Serial Bus Release Number / FLADJ

Bits	Description
31:14	Reserved.
13:8	FLADJ: Frame Length Timing Value. Read-write. Reset: 20h. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF micro-frame length)= $59488 + 16 * \text{FLAdj}$.
7:0	SBRN: Serial Bus Release Number. Value: 20h.

D[16,13,12]F2xA0 USB Legacy Support Extended Capability

Bits	Description
31:25	Reserved.
24	HcOsOwnedSemaphore. Read-write. Reset: 0. System software sets this bit to request ownership of the EHCI controller. Ownership is obtained when this bit reads as 1 and the HcBiosOwnedSemaphore reads as 0.
23:17	Reserved.
16	HcBiosOwnedSemaphore. Read-write. Reset: 0. The BIOS sets this bit to establish ownership of the EHCI controller. System BIOS will set this bit to a 0 in response to a request for ownership of the EHCI controller by system software.

15:8	NextEhciExtendedCapabilityPointer . Read-only. Reset: 00h. 00h=The end of the extended capability list.
7:0	CapabilityID . Read-only. Reset: 01h. 01h=Legacy Support.

D[16,13,12]F2xA4 USB Legacy Support Control / Status

Bits	Description
31	SmiOnBar . Read; Set-by-hardware; write-1-to-clear. Reset: 0. 1=The Base Address Register (BAR) is written.
30	SmiOnPciCommand . Read; Set-by-hardware; write-1-to-clear. Reset: 0. 1=The PCI Command Register is written.
29	SmiOnOsOwnershipChange . Read; set-by-hardware; write-1-to-clear. Reset: 0. 1= D[16,13,12]F2xA0[HcOsOwnedSemaphore] transitions from 1 to 0 or 0 to 1.
28:22	Reserved.
21	SmiOnAsyncAdvance . Read-only. Reset: 0. This is the shadow bit of EHCI[3:1]x24[InterruptOnAsyncAdvance] . Writing 1 to EHCI[3:1]x24[InterruptOnAsyncAdvance] clears this bit to 0.
20	SmiOnHostSystemError . Read-only. Reset: 0. This is the shadow bit of EHCI[3:1]x24[HostSystemError] . Writing 1 to EHCI[3:1]x24[HostSystemError] clears this bit to 0.
19	SmiOnFrameListRollover . Read-only. Reset: 0. This is the shadow bit of EHCI[3:1]x24[FrameListRollover] . Writing 1 to EHCI[3:1]x24[FrameListRollover] clears this bit to 0.
18	SmiOnPortChangeDetect . Read-only. Reset: 0. This is the shadow bit of EHCI[3:1]x24[PortChangeDetect] . Writing 1 to EHCI[3:1]x24[PortChangeDetect] clears this bit to 0.
17	SmiOnUsbError . Read-only. Reset: 0. This is the shadowbit of EHCI[3:1]x24[UsbErrInt] . Writing 1 to EHCI[3:1]x24[UsbErrInt] clears this bit to 0.
16	SmiOnUsbComplete . Read-only. Reset: 0. This is the shadow bit of EHCI[3:1]x24[UsbInt] . Writing 1 to EHCI[3:1]x24[UsbInt] clears this bit to 0.
15	SmiOnBarEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnBar==1.
14	SmiOnPciCommandEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnPciCommand==1.
13	SmiOnOsOwnershipEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnOsOwnershipChange==1.
12:6	Reserved.
5	SmiOnAsyncAdvanceEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnAsyncAdvance==1.
4	SmiOnHostSystemErrorEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnHostSystemError==1.
3	SmiOnFrameListRolloverEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnFrameListRollover==1.
2	SmiOnPortChangeEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnPortChangeDetect==1.
1	SmiOnUsbErrorEnable . Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnUsbError==1.

0	UsbSmiEnable. Read-write. Reset: 0. 1=The host controller will issue an SMI if SmiOnUsbComplete==1.
---	--

D[16,13,12]F2xC0 PME Capability

Bits	Description												
31:27	PmeSupport[4:0]. Read-only. Reset: 0Fh. Indicates the power states in which the function may assert PME#. For each bit, 0=the function is not capable of asserting the PME# signal while in that power state. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>1=PME# can be asserted from D0</td> </tr> <tr> <td>[1]</td> <td>1=PME# can be asserted from D1</td> </tr> <tr> <td>[2]</td> <td>1=PME# can be asserted from D2</td> </tr> <tr> <td>[3]</td> <td>1=PME# can be asserted from D3hot</td> </tr> <tr> <td>[4]</td> <td>1=PME# can be asserted from D3cold</td> </tr> </tbody> </table>	Bit	Definition	[0]	1=PME# can be asserted from D0	[1]	1=PME# can be asserted from D1	[2]	1=PME# can be asserted from D2	[3]	1=PME# can be asserted from D3hot	[4]	1=PME# can be asserted from D3cold
Bit	Definition												
[0]	1=PME# can be asserted from D0												
[1]	1=PME# can be asserted from D1												
[2]	1=PME# can be asserted from D2												
[3]	1=PME# can be asserted from D3hot												
[4]	1=PME# can be asserted from D3cold												
26	D2Support. Read-only. Reset: 1. 1=This function supports the D2 Power Management State.												
25	D1Support. Read-only. Reset: 1. 1=This function supports the D1 Power Management State.												
24:22	AuxCurrent. Value: 0. Reports the 3.3V auxiliary current requirements for the PCI function. 0=Self-powered.												
21	DSI: device specific initialization. Value: 0. Indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.												
20	Reserved.												
19	PmeClock: PME clock. Value: 0. 0=Indicates that no PCI clock is required for the function to generate PME#.												
18:16	Version. Read-only. Reset: 2h. 2h=Indicates that this function complies with Revision 1.1 of the PCI Power Management Interface Specification.												
15:8	NextItemPointer: next item pointer. Read-only. Reset: D0h. Specifies the address of the next capability structure.												
7:0	CapId: capability ID. Value: 01h. Identifies the linked list items as being the PCI Power Management registers.												

D[16,13,12]F2xC4 PME Control / Status

Bits	Description
31:16	Reserved.
15	PmeStatus. Read; set-by-hardware; write-1-to-clear. Cold reset: 0. 1=PME# signal is asserted, independent of the state of the PmeEn bit.
14:9	Reserved.
8	PmeEn. Read-write; S3-check-exclude. Cold reset: 0. 1=Enables the function to assert PME#. 0=PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from D3cold.
7:2	Reserved.

1:0	PowerState. Read-write. Reset: 0. This 2-bit field is used both to determine the current power state of a function and to set the function into a new power state. If software attempts to write an unsupported, optional state to this field, the write operation must be completed normally on the bus; however, the data is discarded and no state change occurs.
<u>Bits</u>	<u>Definition</u>
00b	D0
01b	D1
<u>Bits</u>	<u>Definition</u>
10b	D2
11b	D3hot

D[16,13,12]F2xD0 MSI Control

Bits	Description
31:24	Reserved.
23	C64: 64-bit Address Capable. Read-only. IF (EHCI[3:1]x08[AddressingCapability64Bit]==1) THEN Reset: 1. ELSE Reset: 0. ENDIF. 1=Indicates that the EHCI is capable of generating a 64-bit message address. 0=Indicates the EHCI is not capable of generating a 64-bit address.
22:20	MSIControl: MSI Control. Read-write. Reset: 0.
19:17	Reserved.
16	MSIE: MSI Enable. Read-write. Reset: 0. 1=MSI is enabled and the traditional pins are not used to generate interrupts. 0=MSI operation is disabled and the traditional interrupt pins are used.
15:8	NextItemPointer: Next Item Pointer. Read-only. Reset: E4h. Pointer to next capability structure.
7:0	CapabilityID. Read-only. Reset: 5h. Indicates this is USB MSI capability ID.

D[16,13,12]F2xD4 MSI Address

Bits	Description
31:2	MsiAddress: MSI Address. Read-write. Reset: 0. Specifies system specified message address [31:2].
1:0	Reserved.

D[16,13,12]F2xD8 MSI Upper Address

Bits	Description
31:0	MsiUpperAddress: MSI Upper Address. Read-write. Reset: 0. IF (D[16,13,12]F2xD0[C64]==1) THEN This field specifies the upper 32 bit of system specific message address [63:32]. ELSE This field specifies the MSI data. ENDIF.

D[16,13,12]F2xDC MSI Data

Bits	Description
31:0	MsiData: MSI Data. Read-write. Reset: 0. IF (D[16,13,12]F2xD0[C64]==1) THEN This field specifies the MSI data. ELSE This field is reserved. ENDIF.

D[16,13,12]F2xF0 Function Level Reset Capability

IF (D[16,13,12]F2x50[FlrEn]==0) THEN

Bits	Description
31:0	Reserved.

ELSE

Bits	Description
31:26	Reserved.
25	FunctionLevelResetCapability: Function Level Reset Capability. Value: 1. 1=Function level reset support.
24	TransactionPendingCapability. Value: 1. 1=Transaction pending feature is supported.
23:16	Length. Read-only. Reset: 6h. Advanced Feature (AF) structure length (byte).
15:8	NextItemPointer: Next Item Pointer. Value: 0. Pointer to next capability structure. 0=This is the final item on the list.
7:0	CapId. Read-only. Reset: 13h. 13h=Identifies that the function is Advanced Feature (AF) capable.

ENDIF.

D[16,13,12]F2xF4 Function Level Reset Control

IF (D[16,13,12]F2x50[FlrEn]==0) THEN

Bits	Description
31:0	Reserved.

ELSE

Bits	Description
31:9	Reserved.
8	TransactionPending. Read-only; updated-by-hardware. Reset: 0. 1=Indicates that the Function has issued one or more non-posted transactions which have not been completed, including non-posted transactions that a target has terminated with Retry. 0=Indicates that all non-posted transactions have been completed.
7:1	Reserved.
0	InitiateFLR: Initiate FLR. RAZ; write-1-only. Reset: 0. 1=Initiates Function Level Reset (FLR).

ENDIF.

3.26.4.2.2 EHCI Memory Mapped IO Registers

The EHCI MMIO base address is specified by D[16,13,12]F2x10[BA]. For details of EHCI USB controller implementation requirements and behavior consult the *Universal Serial Bus Specification 2.0* and *Enhanced Host Controller Interface Specification for Universal Serial Bus*.

EHCI[3:1]x00 Capability Length

Bits	Description
7:0	CapLength. Value: 20h. This register is used as an offset to add to the register base to find the beginning of the Operational Register Space starting at EHCI[3:1]x20 .

EHCI[3:1]x02 HC Interface Version

Bits	Description
15:0	HciVersion. Value: 110h. Specifies a BCD encoding of the version number of interface to which this host controller interface conforms.

EHCI[3:1]x04 HC Structural Parameters**Table 233: Reset mapping for EHCI[3:1]x04**

Register	Reset
EHCI1x04	0010_1404h
EHCI2x04	0010_1404h
EHCI3x04	0010_1202h

Bits	Description
31:24	Reserved.
23:20	DebugPortNumber. Read-only. Reset: 1. This register identifies which of the host controller ports is the debug port. The value is the port number (one-based) of the debug port. A non-zero value in this field indicates the presence of a debug port. The value in this register must not be greater than EHCI[3:1]x04[NPorts] . Writing EHCI[3:1]xA0[DebugPortNumberReMapping] updates this field.
19:17	Reserved.
16	PortIndicators. Read-only. Indicates whether the ports support port indicator control. 1=The port status and control registers include a read/writable field for controlling the state of the port indicator.
15:12	N_CC: number of companion controllers. Read-only. Indicates the number of companion controllers associated with this USB 2.0 host controller. 0=Indicates there are no companion host controllers. Port-ownership hand-off is not supported. Only high-speed devices are supported on the host controller root ports. A value larger than 0 in this field indicates there are companion USB 1.1 host controller(s). Port-ownership handoffs are supported. High-speed, Full-speed and Low-speed devices are supported on the host controller root ports.
11:8	N_PCC: NumberOfPortsPerCompanionController. Read-only. Indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to system software. For example, if NPorts has a value of 6 and N_CC has a value of 2, then N_PCC could have a value of 3. The convention is that the first N_PCC ports are assumed to be routed to companion controller 1, the next N_PCC ports to companion controller 2, etc. In the previous example, the N_PCC could have been 4, where the first 4 are routed to companion controller 1 and the last two are routed to companion controller 2. The number in this field must be consistent with NPorts and N_CC.

7	PortRoutingRules . Read-only. Specifies how all ports are mapped to companion controllers. 0=The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. 1=The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.						
6:5	Reserved.						
4	PPC: PortPowerControl . Read-only. Specifies whether the host controller implementation includes port power control. 1=The ports have port power switches. 0=The port does not have port power switches. The value of this field affects the functionality of EHCI[3:1]x[70,6C,68,64] [PortPower].						
3:0	NPorts . Read-only. Specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. <table style="margin-left: 20px;"> <tr> <th style="text-align: left;">Bits</th> <th style="text-align: left;">Definition</th> </tr> <tr> <td>0h</td> <td>undefined</td> </tr> <tr> <td>Fh-1h</td> <td><NPorts> Ports</td> </tr> </table>	Bits	Definition	0h	undefined	Fh-1h	<NPorts> Ports
Bits	Definition						
0h	undefined						
Fh-1h	<NPorts> Ports						

EHCI[3:1]x08 HC Capability Parameters

Bits	Description
31:20	Reserved.
19	Frame32PeriodicListCapability: 32-Frame Periodic List Capability . Read-only. Reset: 0. 1=The host controller supports a 32 frame periodic schedule as specified by using the value 11b in EHCI[3:1]x20 [FrameListSize]. 0=Software must treat a Frame List Size value of 11b as reserved.
18	PerPortChangeEventCapability: Per-Port Change Event Capability . Value: D[16,13,12]F2x50[EnablePerPortChangeEventCapability]. 1=Host controller supports per-port change events and the associated fields Ehci[3:1]x20 [PerPortChangeEventEnable], Ehci[3:1]x24 [PortNChangeDetect] and Ehci[3:1]x28 [PortChangeIntEn]. 0=Per-port change events are not supported; software should treat those fields as reserved.
17	LinkPowerManagementCapability: Link Power Management Capability . Read-only. Reset: 0. 1=Host controller supports the Link Power Management L1 state and associated Suspend using L1, Suspend Status, and Device Address fields in Ehci[3:1]x[70,6C,68,64] . 0=Link Power Management L1 State is not supported; Software should treat those fields as reserved.
16	HardwarePrefetchCapability: Hardware Prefetch Capability . Read-only. Reset: 0. 1=Indicates the host controller supports the Hardware Prefetching capability and associated Ehci[3:1]x20 [Fully-SynchronizedPrefetch, PeriodicSchedulePrefetchEnable, AsynchronousSchedulePrefetchEnable] fields. 0=Hardware prefetch capability is not supported; Software should treat those fields as reserved.
15:8	EhciExtendedCapabilitiesPointer . Read-only. Reset: A0h. Specifies the offset in PCI configuration space of the first EHCI extended capability. See D[16,13,12]F2xA0 .
7	IsochronousSchedulingThreshold3 . IF (Ehci[3:1]xB0 [EnableWriteToEorCap08]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. The value of this field determines the function of IsochronousSchedulingThreshold[2:0].

6:4	IsochronousSchedulingThreshold[2:0] . IF (EHCI[3:1]xB0[EnableWriteToEorCap08]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 111b. This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. IF (IsochronousSchedulingThreshold3==0) THEN Field value indicates the number of micro-frames of isochronous data structures (one or more) a host controller can hold before flushing the state. ELSE Host software assumes the host controller may cache an isochronous data structure for an entire frame. ENDIF.
3	Reserved.
2	AsyncScheduleParkCapability . Read-only. Reset: 1. 1=The host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule.
1	ProgrammableFrameListFlag . Read-only. Reset: 1. 0= EHCI[3:1]x20[FrameListSize] is read-only; System software must use a frame list length of 1024 elements with this host controller. 1= EHCI[3:1]x20[FrameListSize] is read-writeable; System software can specify and use a smaller frame list via EHCI[3:1]x20[FrameListSize] .
0	AddressingCapability64Bit . IF (EHCI[3:1]xB0[EnableWriteToEorCap08]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. Specifies the addressing range capability of this implementation. 0=Data structures using 32-bit address memory pointers. 1=Data structures using 64-bit address memory pointers.

EHCI[3:1]x20 USB Command

Bits	Description
31:28	Reserved.
27:24	HostInitiatedResumeDuration: host-initiated resume duration . IF (EHCI[3:1]x08[LinkPowerManagementCapability]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. This field is used by system software to specify the minimum amount of time the host controller will drive the K-state during a host-initiated resume from a LPM state (e.g. L1), and is conveyed to each LPM-enabled device (via the HIRD bits within an LPM Token's bmAttributes field) upon entry into a low-power state. <u>Bits</u> <u>Definition</u> Fh-0h (<HostInitiatedResumeDuration> *75 us) + 50 us
23:16	InterruptThresholdControl: Interrupt Threshold Control . Read-write. Reset: 8h. This field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below. Any other value in this register yields undefined results. <u>Bits</u> <u>Definition</u> <u>Bits</u> <u>Definition</u> 00h Reserved 08h 8 micro-frames (default, 1 ms) 01h 1 micro-frame 10h 16 micro-frames (2 ms) 02h 2 micro-frames 20h 32 micro-frames (4 ms) 04h 4 micro-frames 40h 64 micro-frames (8 ms) Software modifications to this bit while (EHCI[3:1]x24[HCHalted]==0) results in undefined behavior.

15	PerPortChangeEventsEnable: Per-Port Change Events Enable. IF (EHCI[3:1]x08 [PerPortChangeEventCapability]==1) THEN Read-write. ELSE Read-only. ENDIF. Reset: 0. 1=Enable the per-port change event capability as defined by EHCI[3:1]x24 [PortNChangeDetect] and EHCI[3:1]x28 [PortNChangeEventEnable]. Note that enabling per-port change events has no affect on the existing Port Change Detect capability. In other words, one or both of these may be enabled and used by software independently of the other, where per-port change events can be used to streamline the process for resolving which port(s) caused a given event (interrupt).
14	FullySynchronizedPrefetch: Fully Synchronized Prefetch. IF (EHCI[3:1]x08 [HardwarePrefetchCapability]==1) THEN Read-write. ELSE Read-only. Reset: 0. ENDIF. This field is used to inform hardware whether software fully supports the use of the AsynchronousSchedulePrefetchEnable and PeriodicSchedulePrefetchEnable fields, where software ensures that any and all updates to the periodic and/or asynchronous schedules by software will only occur when hardware prefetching of the associated schedule has been fully disabled. Software should not use the AsynchronousSchedulePrefetchEnable and PeriodicSchedulePrefetchEnable fields unless this bit==1.
13	AsynchronousSchedulePrefetchEnable: Asynchronous Schedule Prefetch Enable. IF (EHCI[3:1]x08 [HardwarePrefetchCapability]==1) THEN Read-write. ELSE Read-only. Reset: 0. ENDIF. 1=Enable hardware prefetching of the asynchronous schedule. 0=Disable hardware prefetching of the asynchronous schedule; software must wait until a read of this field returns 0. This bit shall only be set when the FullySynchronizedPrefetch==1. Hardware prefetching must be disabled before software applies any changes to the asynchronous schedule or structures linked to this schedule. Note that hardware prefetching of the periodic schedule may remain active when software is solely modifying the asynchronous schedule.
12	PeriodicSchedulePrefetchEnable: Periodic Schedule Prefetch Enable. IF (EHCI[3:1]x08 [HardwarePrefetchCapability]==1) THEN Read-write. ELSE Read-only. Reset: 0. ENDIF. 1=Enable hardware prefetching of the periodic schedule. 0=Disable hardware prefetching of the periodic schedule; software should wait to read this bit back 0 after writing 0 to make sure hardware prefetching is disabled. This bit shall only be set when the FullySynchronizedPrefetch==1. Hardware prefetching must be disabled before software applies any changes to the periodic schedule or structures linked to this schedule. Note that hardware prefetching of the asynchronous schedule may remain active when software is solely modifying the periodic schedule.
11	AsyncScheduleParkModeEnable: asynchronous schedule park mode enable. Read-write. Reset: 1. 1=Park mode is enabled. 0=Park mode is disabled.
10	Reserved.
9:8	AsyncScheduleParkModeCount: Asynchronous Schedule Park Mode Count. Read-write. Reset: 11b. This field contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. Valid values are 1h to 3h. Software must not write a 0 to this field when AsyncScheduleParkModeEnable==1, as this will result in undefined behavior.
7	LightHostControllerReset: Light Host Controller Reset. Read-only. Reset: 0. Not implemented.

6	InterruptOnAsyncAdvanceDoorbell: Interrupt on Async Advance Doorbell. Read; cleared-by-hardware; write-1-only. Reset: 0. This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write a 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets EHCI[3:1]x24 [InterruptOnAsyncAdvance] to 1 and clears this bit to 0. Software should not write a 1 to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.												
5	AsynchronousScheduleEnable: Asynchronous Schedule Enable. Read-write. Reset: 0. This bit controls whether the host controller skips processing the Asynchronous Schedule. 0=Do not process the Asynchronous Schedule. 1=Use EHCI[3:1]x38 to access Asynchronous Schedule.												
4	PeriodicScheduleEnable: Periodic Schedule Enable. Read-write. Reset: 0. This bit controls whether the host controller skips processing the Periodic Schedule. 0=Do not process the Periodic Schedule. 1=Use EHCI[3:1]x34 to access the Periodic Schedule.												
3:2	<p>FrameListSize: frame list size. IF ((EHCI[3:1]x08[ProgrammableFrameListFlag]==1) (EHCI[3:1]x08[Frame32PeriodicListCapability]==1)) THEN Read-write. ELSE RAZ. ENDIF. Reset: 0. This field specifies the size of the frame list. The size the frame list controls which bits in the Frame Index Register should be used for the Frame List Current index.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1024 frames (4096 bytes)</td> <td>01b</td> <td>512 frames (2098 bytes)</td> </tr> <tr> <td>10b</td> <td>256 frames (1024 bytes)</td> <td>11b</td> <td>Reserved or 32 frames (see below)</td> </tr> </tbody> </table> <p>Software may only program a 32 frame list when EHCI[3:1]x08[Frame32PeriodicListCapability]=1, and a 512 or 256 frame list when EHCI[3:1]x08[ProgrammableFrameListFlag]=1. Note that hardware employs a slightly different model for Frame List Rollover events when a 32 frame list is in use. See EHCI[3:1]x24[FrameListRollover].</p>	Bits	Definition	Bits	Definition	00b	1024 frames (4096 bytes)	01b	512 frames (2098 bytes)	10b	256 frames (1024 bytes)	11b	Reserved or 32 frames (see below)
Bits	Definition	Bits	Definition										
00b	1024 frames (4096 bytes)	01b	512 frames (2098 bytes)										
10b	256 frames (1024 bytes)	11b	Reserved or 32 frames (see below)										
1	<p>HCRESET: Host Controller Reset. Read; cleared-by-hardware; write-1-only. Reset: 0. This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. Software must reinitialize the host controller in order to return the host controller to an operational state.</p> <p>1=The Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value; Any transaction currently in progress on USB is immediately terminated; A USB reset is not driven on downstream ports; PCI Configuration registers are not affected by this reset; All operational registers, including port registers and port state machines are set to their initial values; Port ownership reverts to the companion host controller(s).</p> <p>Software should not set this bit to a 1 when EHCI[3:1]x24[HCHalted]==0. Attempting to reset an actively running host controller will result in undefined behavior.</p>												
0	<p>RunStop: Run/Stop. Read-write. Reset: 0. 1=Run; the Host Controller proceeds with execution of the schedule as long as this bit is set to 1. 0=Stop; the Host Controller completes the current and any actively pipelined transactions on the USB and then halts within 16 micro-frames after software clears this bit.</p> <p>Software must not write a 1 to this field unless EHCI[3:1]x24[HCHalted]==1. Doing so will yield undefined results.</p>												

EHCI[3:1]x24 USB Status

Bits	Description

31:16	<p>PortNChangeDetect: Port-n Change Detect. IF (EHCI[3:1]x08[PerPortChangeEventCapability]==1) THEN Read; set-by-hardware; write-1-to-clear. ELSE Read-only. ENDIF. Reset: 0. This field should only be used by software when (EHCI[3:1]x20[PerPortChangeEventsEnable]==1). Each bit in this field correspond to a port. For each bit, 1=A port change event was detected for that port; see EHCI[3:1]x24[PortChangeDetect] for port change event details.</p> <p>EHCI[3:1]x04[NPorts] specifies how many ports are exposed by the host controller and thus how many bits in this field are valid.</p> <table border="1" data-bbox="274 439 567 614"> <thead> <tr> <th>Bit</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Port 1</td></tr> <tr> <td>[1]</td><td>Port 2</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>[15]</td><td>Port 16</td></tr> </tbody> </table>	Bit	Definition	[0]	Port 1	[1]	Port 2	[15]	Port 16
Bit	Definition										
[0]	Port 1										
[1]	Port 2										
...	...										
[15]	Port 16										
15	<p>AsynchronousScheduleStatus: Asynchronous Schedule Status. Read-only. Reset: 0. The bit reports the current real status of the Asynchronous Schedule. 0=Status of the Asynchronous Schedule is disabled. 1=Status of the Asynchronous Schedule is enabled.</p> <p>The host controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions EHCI[3:1]x20[AsynchronousScheduleEnable]. When this bit and the EHCI[3:1]x20[AsynchronousScheduleEnable] are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).</p>										
14	<p>PeriodicScheduleStatus: Periodic Schedule Status. Read-only. Reset: 0. The bit reports the current real status of the Periodic Schedule. 0=Periodic Schedule is disabled. 1=Periodic Schedule is enabled.</p> <p>The host controller is not required to immediately disable or enable the Periodic Schedule when software transitions EHCI[3:1]x20[PeriodicScheduleEnable]. When this bit and the Periodic Schedule Enable bit are the same value, Periodic Schedule is either enabled (1) or disabled (0).</p>										
13	Reclamation. Read-only. Reset: 0. Indicates an empty asynchronous schedule.										
12	HCHalted. Read-only. Reset: 1. 0= EHCI[3:1]x20[RunStop] is 1 or the host controller has not yet stopped. 1=The host controller has stopped executing as a result of EHCI[3:1]x20[RunStop] being set to 0, either by software or by the host controller hardware due to an internal error.										
11:6	Reserved.										
5	InterruptOnAsyncAdvance: Interrupt on Async Advance. Read-write. Reset: 0. 1=Indicate the assertion of interrupt source caused by EHCI[3:1]x20[InterruptOnAsyncAdvanceDoorbell] .										
4	HostSystemError: Host System Error. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=A serious error occurs during a host system access involving the host controller module. In a PCI system, conditions that set this bit to 1 include PCI Parity error, PCI Master Abort, and PCI Target Abort. When this error occurs, the host controller clears EHCI[3:1]x20[RunStop] to prevent further execution of the scheduled TDs.										
3	FrameListRollover: Frame List Rollover. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1= EHCI[3:1]x2C[FrameIndex] rolls over from its maximum value to zero. The exact Frame List Index value at which the rollover occurs depends on the frame list size. For example, if the frame list size as programmed by EHCI[3:1]x20[FrameListSize] is 1024, then a frame list rollover would occur every time EHCI[3:1]x2C[FrameIndex[13]] toggles. Similarly, a frame list rollover would occur every time EHCI[3:1]x2C[FrameIndex[12]] toggles for a 512 frame list. Note this behavior is different for a 32 frame list where a rollover event occurs every time EHCI[3:1]x2C[FrameIndex[13]] toggles (same as 1024).										

2	PortChangeDetect: Port Change Detect. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=One of the following port change event has occurred: <ul style="list-style-type: none"> • EHCI[3:1]x[70,6C,68,64][PortOwner] changed from 0 to 1; • EHCI[3:1]x[70,6C,68,64][ForcePortResume] changed from 0 to 1; • EHCI[3:1]x[70,6C,68,64][ConnectStatusChange] is set to 1.
1	UsbErrInt: USB Error Interrupt. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=The completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and the UsbInt bit are set.
0	UsbInt: USB Interrupt. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=A USB transaction has completed, which results in the retirement of a Transfer Descriptor that had its IOC bit set; A short packet is detected (actual number of bytes received was less than the expected number of bytes).

EHCI[3:1]x28 USB Interrupt Enable

Bits	Description										
31:16	PortNChangeEventEnable: Port-n Change Event Enable. Read-write. Reset: 0. This field is bit significant. Each bit corresponds to a port. For each bit, 1=The host controller will issue an interrupt if the corresponding bit in EHCI[3:1]x24[PortNChangeDetect] is set to 1. The interrupt is acknowledged by software clearing EHCI[3:1]x24[PortNChangeDetect] . EHCI[3:1]x04[NPorts] specifies how many ports are exposed by the host controller and thus how many bits in this field are valid. <table> <thead> <tr> <th>Bit</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Port 1</td></tr> <tr> <td>[1]</td><td>Port 2</td></tr> <tr> <td>...</td><td>...</td></tr> <tr> <td>[15]</td><td>Port 16</td></tr> </tbody> </table>	Bit	Definition	[0]	Port 1	[1]	Port 2	[15]	Port 16
Bit	Definition										
[0]	Port 1										
[1]	Port 2										
...	...										
[15]	Port 16										
15:6	Reserved.										
5	InterruptOnAsyncAdvanceEn: Interrupt on Async Advance Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt at the next interrupt threshold if EHCI[3:1]x24[InterruptOnAsyncAdvance]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[InterruptOnAsyncAdvance] .										
4	HostSystemErrorEn: Host System Error Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt if EHCI[3:1]x24[HostSystemError]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[HostSystemError] .										
3	FrameListRolloverEn: Frame List Rollover Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt if EHCI[3:1]x24[FrameListRollover]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[FrameListRollover] .										
2	PortChangeIntEn: Port Change Interrupt Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt if EHCI[3:1]x24[PortChangeDetect]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[PortChangeDetect] .										
1	UsbErrIntEn: USB Error Interrupt Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt at the next interrupt threshold if EHCI[3:1]x24[UsbErrInt]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[UsbErrInt] .										
0	UsbIntEn: USB Interrupt Enable. Read-write. Reset: 0. 1=The host controller will issue an interrupt at the next interrupt threshold if EHCI[3:1]x24[UsbInt]==1 . The interrupt is acknowledged by software clearing EHCI[3:1]x24[UsbInt] .										

EHCI[3:1]x2C Frame Index

Bits	Description
31:14	Reserved. These bits are reserved and should be 0.
13:0	<p>FrameIndex: Frame Index. Read-write; updated-by-hardware. Reset: 0. This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on EHCI[3:1]x20[FrameListSize].</p> <p>This register must be written as a DWord. Byte writes produce undefined results. This register cannot be written unless EHCI[3:1]x24[HCHalted]==1. Writes to this register also affect the SOF value. The host controller behaves slightly different when using a 32-frame Frame List Size, specifically it continues to count FrameIndex up to a full 1024 frames, transmit SOF values from 0 to 2047, and generate Frame List Rollover events (when enabled) every 1024 frames - exactly as if a 1024 frame list size was employed. The host controller will only reference 32 elements on the periodic schedule, however. This is accomplished by formulating the Periodic Frame List Element Address using {FrameIndex[N:3] modulo 32} rather than FrameIndex[N:3]. The same mapping should be done by system software whenever it needs to correlate the current FrameIndex value to a specific periodic schedule element. Note this new behavior only applies to a 32-frame list.</p>

EHCI[3:1]x30 Control Data Structure Segment

Bits	Description
31:0	<p>CtrlDSSegment. IF (EHCI[3:1]x08[AddressingCapability64Bit]==0) THEN RAZ. ELSE Read-write. ENDIF. Reset: 0. Specifies the most significant address bits [63:32] for all EHCI data structures if EHCI[3:1]x08[AddressingCapability64Bit]==1. This register is concatenated with the link pointer from either EHCI[3:1]x34, or EHCI[3:1]x38, or any control data structure link field to construct a 64-bit address.</p>

EHCI[3:1]x34 Periodic Frame List Base Address

Bits	Description
31:12	<p>BaseAddress: Base Address. Read-write. Reset: 0. Specifies the beginning address [31:12] of the Periodic Frame List in the system memory. If (EHCI[3:1]x08[AddressingCapability64Bit]==1), the most significant 32 bits of every control data structure address comes from EHCI[3:1]x30.</p>
11:0	Reserved. Must be written as 0s. During runtime, the values of these bits are undefined.

EHCI[3:1]x38 Current Async List Address

Bits	Description
31:5	<p>LPL: Link Pointer Low. Read-write. Reset: 0. Specifies the address [31:5] of the next asynchronous queue head to be executed. If (EHCI[3:1]x08[AddressingCapability64Bit]==1), the most significant 32 bits of every control data structure address comes from EHCI[3:1]x30. This field may only reference a Queue Head (QH).</p>
4:0	Reserved.

EHCI[3:1]x60 Configure Flag

Bits	Description
31:1	Reserved.
0	CF: Configure Flag. Read-write. Reset: 0. This bit controls the default port-routing control logic. Software sets this bit as the last action in its process of configuring the host controller. 0=Port routing control logic default-routes each port to an implementation dependent classic host controller. 1=Port routing control logic default-routes all ports to this host controller.

EHCI[3:1]x[70,6C,68,64] Port Status Control [4:1]

Bits	Description																				
31:25	DeviceAddress: Device Address. Read-write. Reset: 0. Specifies the 7-bit USB device address for the device attached to and immediately downstream of the associated root port. 0=Indicates no device is present or support for this feature is not present.																				
24:23	SuspendStatus: Suspend Status. Read-only; updated-by-hardware. Reset: 0. These two bits are used by software to determine whether the most recent L1 suspend request was successful, specifically: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Success: State transition was successful (ACK)</td> </tr> <tr> <td>01b</td> <td>Not Yet: Device was unable to enter the L1 state at this time (NYET)</td> </tr> <tr> <td>10b</td> <td>Not Supported: Device does not support the L1 state (STALL)</td> </tr> <tr> <td>11b</td> <td>Timeout/Error: Device failed to respond or an error occurred.</td> </tr> </tbody> </table> This field is updated by hardware immediately following the completion of an L1 transition request (via an LPM Token). To avoid any race conditions with hardware, software should only consume the contents of this field when Suspend==0 (port no longer in L1).	Bits	Definition	00b	Success: State transition was successful (ACK)	01b	Not Yet: Device was unable to enter the L1 state at this time (NYET)	10b	Not Supported: Device does not support the L1 state (STALL)	11b	Timeout/Error: Device failed to respond or an error occurred.										
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11b	Timeout/Error: Device failed to respond or an error occurred.																				
22	WakeOnOverCurrentEnable: wake on over-current enable. Read-write. Reset: 0. 1=Enables the port to be sensitive to over-current conditions as wake-up events. This field is 0 if (PortPower==0).																				
21	WakeOnDisconnectEnable: wake on disconnect enable. Read-write. Reset: 0. 1=Enables the port to be sensitive to device disconnects as wake-up events. This field is 0 if (PortPower==0).																				
20	WakeOnConnectEnable: wake on connect enable. Read-write. Reset: 0. 1=Enables the port to be sensitive to device connects as wake-up events. This field is 0 if (PortPower==0).																				
19:16	PortTestControl: Port Test Control. Read-write. Reset: 0. When this field is 0, the port is not operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. <table> <thead> <tr> <th>Bits</th> <th>TestMode</th> <th>Bits</th> <th>TestMode</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Test mode not enabled</td> <td>0100b</td> <td>Test Packet</td> </tr> <tr> <td>0001b</td> <td>Test J_STATE</td> <td>0101b</td> <td>Test FORCE_ENABLE</td> </tr> <tr> <td>0010b</td> <td>Test K_STATE</td> <td>1111-0110b</td> <td>Reserved</td> </tr> <tr> <td>0011b</td> <td>Test SE0_NAK</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	TestMode	Bits	TestMode	0000b	Test mode not enabled	0100b	Test Packet	0001b	Test J_STATE	0101b	Test FORCE_ENABLE	0010b	Test K_STATE	1111-0110b	Reserved	0011b	Test SE0_NAK		
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0010b	Test K_STATE	1111-0110b	Reserved																		
0011b	Test SE0_NAK																				
15:14	PortIndicatorControl: Port Indicator Control. IF (EHCI[3:1]x04[PortIndicators]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. This field is 0 if PortPower==0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Port indicators are off.</td> <td>10b</td> <td>Green</td> </tr> <tr> <td>01b</td> <td>Amber</td> <td>11b</td> <td>Undefined</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Port indicators are off.	10b	Green	01b	Amber	11b	Undefined								
Bits	Definition	Bits	Definition																		
00b	Port indicators are off.	10b	Green																		
01b	Amber	11b	Undefined																		

13	PortOwner: Port Owner. Read-write. Reset: 1. 1=A companion host controller owns and controls the port. Software writes a 1 to this bit when the attached device is not a high-speed device. This bit unconditionally goes to a 0 when EHCI[3:1]x60[CF] transitions from 0 to 1. This bit unconditionally goes to 1b whenever EHCI[3:1]x60[CF]==0 . System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device).										
12	PortPower: Port Power. IF (EHCI[3:1]x04[PPC]==0) THEN Read-only. ELSE Read-write. ENDIF. IF (EHCI[3:1]x04[PPC]==0) THEN Reset: 1. ELSE Reset: X. ENDIF. 0=Power is off; the port is non-functional and will not report attaches, detaches, etc. 1=Power is on. When an over-current condition is detected on a powered port and EHCI[3:1]x04[PPC]==1 , the PortPower bit in each affected port may be transitioned by the host controller from 1 to 0 (removing power from the port).										
11:10	LineStatus[1:0]: Line Status. Read-only. Reset: X. These bits reflect the current logical levels of the D+ (LineStatus[1]) and D- (LineStatus[0]) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when PortEnable==0 and CurrentConnectStatus==1. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>SE0. Not Low-speed device, perform EHCI reset</td> </tr> <tr> <td>01b</td> <td>K-state. Low-speed device, release ownership of port</td> </tr> <tr> <td>10b</td> <td>J-state. Not Low-speed device, perform EHCI reset</td> </tr> <tr> <td>11b</td> <td>Undefined. Not Low-speed device, perform EHCI reset.</td> </tr> </tbody> </table> <p>This value of this field is undefined if (PortPower==0).</p>	Bits	Definition	00b	SE0. Not Low-speed device, perform EHCI reset	01b	K-state. Low-speed device, release ownership of port	10b	J-state. Not Low-speed device, perform EHCI reset	11b	Undefined. Not Low-speed device, perform EHCI reset.
Bits	Definition										
00b	SE0. Not Low-speed device, perform EHCI reset										
01b	K-state. Low-speed device, release ownership of port										
10b	J-state. Not Low-speed device, perform EHCI reset										
11b	Undefined. Not Low-speed device, perform EHCI reset.										
9	SuspendUsingL1: Suspend using L1. Read-write. Reset: 0. 0=The host controller will employ the legacy (L2) suspend mechanism. 1=If a non-zero value is specified in DeviceAddress, the host controller will generate an LPM Token to enter the L1 state whenever software writes a 1 to the Suspend bit, as well as L1 exit timing during any device- or host-initiated resume. <p>Software should only set this bit when the device attached immediately downstream of this root port supports L1 transitions.</p>										
8	PortReset: Port Reset. Read-write. Reset: 0. 1=Port is in Reset. 0=Port is not in Reset. Software writes 1 to start the bus reset sequence; It must keep this bit at a 1 long enough to ensure the reset sequence completes. Software writes 0 to terminate the bus reset sequence; This bit will not read as a 0 until after the reset has completed. <p>When software writes this bit to a 1, it must also write a 0 to the PortEnable bit. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a 1). EHCI[3:1]x24[HCHalted] should be a 0 before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a 1. This field is 0 if PortPower==0.</p>										
7	Suspend. Read; cleared-by-hardware; write-1-only. Reset: 0. 0=IF (EHCI[3:1]x[70,6C,68,64][PortEnable]==1) THEN Port is enabled. ELSE Port is disabled. ENDIF. 1=IF (EHCI[3:1]x[70,6C,68,64][PortEnable]==1) THEN Port is in suspend state; The port can be in either L1 or L2 suspend state depending on SuspendUsingL1. ELSE Port is disabled. ENDIF. <p>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. If this bit is written with a 1 when a transaction is in progress then the blocking will not occur until the end of the current transaction. In the suspend state, the port is sensitive to resume detection. Additional status for L1-based transitions is provided to software via the SuspendStatus field. This field is 0 if PortPower==0. If system software sets this bit to a 1 when the port is not enabled (i.e. PortEnable == 0) the results are undefined. A write of 0 to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a 0 when:</p> <ul style="list-style-type: none"> • Software sets the ForcePortResume bit to a 0 from a 1. • Software sets the PortReset bit to a 1 from a 0. • Whenever PortPower is zero. 										

6	<p>ForcePortResume: Force Port Resume. Read-write; set-by-hardware. Reset: 0. 1=Resume detected/driven on port. 0=No resume (K-state) detected/driven on port. This field is 0 if PortPower==0.</p> <p>This functionality defined for manipulating this bit depends on the value of the Suspend and SuspendUsingL1 bits. For example, if the port is not suspended (Suspend and Enabled bits are a 1) and software transitions this bit to a 1, then the effects on the bus are undefined.</p> <p>The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. In this case, EHCI[3:1]x24[PortChangeDetect] and/or EHCI[3:1]x24[PortNChangeDetect] will also be set to 1.</p> <p>Software sets this bit to a 1 to drive resume signaling. If software sets this bit to a 1, the host controller must not set EHCI[3:1]x24[PortChangeDetect] and/or EHCI[3:1]x24[PortNChangeDetect]. Writing a 0 (from 1) causes the port to return to high-speed mode. This bit will remain a 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a 0.</p> <p>For legacy (L2) transitions, software must appropriately time the Resume and set this bit to a 0 when the appropriate amount of time has elapsed. Software does not need to time resume signaling for L1 transactions as host controller hardware will automatically enforce the necessary timing and clear this bit when the port has fully resumed. Software can influence the amount of time hardware will drive resume signaling during L1 exit via EHCI[3:1]x20[HostInitiatedResumeDuration].</p>
5	OverCurrentChange: over-current change. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=There is a change to OverCurrentActive.
4	OverCurrentActive: over-current active. Read-only; updated-by-hardware. Reset: 0. 1=This port currently has an over-current condition. 0=This port does not have an over-current condition.
3	<p>PortEnableDisableChange: Port Enable/Disable Change. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Port enabled/disabled status has changed. 0=No change. For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2. This field is 0 if PortPower==0.</p>
2	<p>PortEnable: port enable. Read-write; set-by-hardware. Reset: 0. 1=Enable. 0=Disable.</p> <p>Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a 1 to this field. The host controller will only set this bit to a 1 when the reset sequence determines that the attached device is a high-speed device.</p> <p>Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. The bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled, downstream propagation of data is blocked on this port, except for reset. This field is 0 if PortPower==0.</p>
1	<p>ConnectStatusChange: Connect Status Change. Read; set-by-hardware; write-1-to-clear. Reset: 0. Indicates a change has occurred in the port's CurrentConnectStatus. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. This field is 0 if PortPower==0. 1=Change in Current Connect Status. 0=No change.</p>
0	CurrentConnectStatus: Current Connect Status. Read-only. Reset: 0. This value reflects the current state of the port, and may not correspond directly to the event that caused the ConnectStatusChange to be set to 1. This field is 0 if PortPower==0. 1=Device is present on port. 0=No device is present.

EHCI[3:1]xA4 Packet Buffer Threshold Values

BIOS: 0040_0040h.

Bits	Description
31:24	Reserved.
23:16	OUTThreshold: OUT Threshold. Read-write. Reset: 40h. The transmit packet starts at UTMI interface when threshold of internal FIFO for transmit packet is reached. The value represents multiple of 8 bytes. For example, 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).
15:8	Reserved.
7:0	INTThreshold: IN Threshold. Read-write. Reset: 40h. The PCI transaction starts when threshold of internal FIFO for receive packet is reached. The value represents multiple of 8 bytes. For example, 10h means 128 bytes. The smallest acceptable value is 08h (64 bytes).

EHCI[3:1]xB4 UTMI Control

BIOS: See [2.15.2.6](#)&[2.15.2.7](#).

Bits	Description																												
31:18	Reserved.																												
17	VBusy. Read-only. Reset: 0. 1=Block software writes to bits[16:8] when port router is updating the field.																												
16:13	PortNumber: Port Number. Read-write. Reset: 0. Select the corresponding port PHY or common block to load the VControl bits. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Port 0</td> <td>0011b</td> <td>Port 3</td> </tr> <tr> <td>0001b</td> <td>Port 1</td> <td>1110b-0100b</td> <td>Reserved</td> </tr> <tr> <td>0010b</td> <td>Port 2</td> <td>1111b</td> <td>Common block</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000b	Port 0	0011b	Port 3	0001b	Port 1	1110b-0100b	Reserved	0010b	Port 2	1111b	Common block												
Bits	Definition	Bits	Definition																										
0000b	Port 0	0011b	Port 3																										
0001b	Port 1	1110b-0100b	Reserved																										
0010b	Port 2	1111b	Common block																										
12	VLoadB. Read-write. Reset: 1. VControl value load, active low. 0=Load the new VControl value to the PHY or common block specified by PortNumber. VLoadB must be 1 while VControlModeSel is changed.																												
11	Reserved.																												
10:7	VControlModeSel. Read-write. Reset: 0. Selects the PHY control mode group. There are 8 groups defined for PHY control mode. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Group 0</td> <td>0110b</td> <td>Group 6. Analog Control</td> </tr> <tr> <td>0001b</td> <td>Group 1</td> <td>0111b</td> <td>Group 7</td> </tr> <tr> <td>0010b</td> <td>Group 2</td> <td>1000b</td> <td>Group 8</td> </tr> <tr> <td>0011b</td> <td>Group 3</td> <td>1001b</td> <td>Group 9</td> </tr> <tr> <td>0100b</td> <td>Group 4. CDR DFT control</td> <td>1111b-1010b</td> <td>Reserved</td> </tr> <tr> <td>0101b</td> <td>Group 5. CDR DFT control</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000b	Group 0	0110b	Group 6. Analog Control	0001b	Group 1	0111b	Group 7	0010b	Group 2	1000b	Group 8	0011b	Group 3	1001b	Group 9	0100b	Group 4. CDR DFT control	1111b-1010b	Reserved	0101b	Group 5. CDR DFT control		
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0100b	Group 4. CDR DFT control	1111b-1010b	Reserved																										
0101b	Group 5. CDR DFT control																												

EHCI[3:1]xB8 Loopback Test

Bits	Description
31:27	Reserved.

26:21	StatusOfPortsforPowerUpStateCheck[5:0]: Status of ports for PowerUp State Check. Read-only. Reset: 0. Status bit to indicate the Power Up state auto-checking result from the individual port. Each bit maps to a corresponding port, from port 0 to port 5. <table border="1"> <thead> <tr> <th>Bit</th><th>Definition</th><th>Bit</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Port 0</td><td>[3]</td><td>Port 3</td></tr> <tr> <td>[1]</td><td>Port 1</td><td>[4]</td><td>Port 4</td></tr> <tr> <td>[2]</td><td>Port 2</td><td>[5]</td><td>Port 5</td></tr> </tbody> </table> For each bit, 0=PHY Power Up State checking is fail. 1=PHY Power Up State checking is good.	Bit	Definition	Bit	Definition	[0]	Port 0	[3]	Port 3	[1]	Port 1	[4]	Port 4	[2]	Port 2	[5]	Port 5
Bit	Definition	Bit	Definition														
[0]	Port 0	[3]	Port 3														
[1]	Port 1	[4]	Port 4														
[2]	Port 2	[5]	Port 5														
20	EnablePHYPowerUpStateChecking: Enable PHY PowerUp State Checking. Read-write. Reset: 0. 1=Enable auto-checking on PHY Power Up State. There is built-in logic to check the PHY default Power Up state to detect manufacturing defects in the PHY macro.																
19:12	GoodReceivedPacketCount: Good Received Packet Count. Read-only; updated-by-hardware. Reset: 0. Specified the number of good packets that the host controller received during the loopback test mode. These bits will be cleared by clearing EnableLoopBackTest.																
11	Reserved.																
10	LoopbackTestDone: Loopback Test Done. Read-only. Reset: 0. 1=Loopback test is done.																
9	LoopbackTestStatus: Loopback Test Status. Read-only. Reset: 0. 0=CRC error on loopback receiving data. 1=Good CRC on loopback receiving data.																
8	EnableLoopBackTest: Enable Loop Back Test. Read-write. Reset: 0. 1=Enable external USB port loopback test. The loopback test is to set one port to TX mode (Test Packet mode) and one port to RX mode (Test SE0_NAK). See EHCI[3:1]x[70,6C,68,64][PortTestControl] for information on the tests.																
7:4	Reserved.																
3:0	ReceivedPacketCount: Received Packet Count. Read-write. Reset: 0. RX data packet count. This counter defines the number (in power of 16) of RX data packet that should be checked for the loopback test.																

EHCI[3:1]xBC EOR MISC Control

Bits	Description
31:24	ForceTxData[7:0]: Force TX Data [7:0]. Read-write. Reset: 0. Used to force TxData[7:0] when the port is in TEST_K mode. This can be used to force PHY to generate a desired output pattern for PHY debugging and characterization purposes.
23:15	Reserved.
14	EHCIDeepBlinkPowerSavingEnable: EHCI Deep Blink Power Saving Enable. Read-write. Reset: 1. 1=Enable Deep Blink power saving clock gating; EHCI will request to stop the Global Blink clock when the list processor is idle.
13	Reserved.
12	EHCIPowerSavingEnable: EHCI Power Saving Enable. Read-write. Reset: 1. 1=Enable power saving clock gating. When enabled, dynamic clock gating is enabled when EHCI is not in operational mode. The clock going to all memory modules will be gated off. Blink clock also gets gated off unless the connection interrupt is detected.
11	DisablesHSuFrameBabbledetection: Disables HS uFrame Babble detection. Read-write. Reset: 0. 1=Disable HS uFrame babble detection.
10:8	Reserved.

7:4	InterPacketGapAdjustCounter: Inter-packet Gap Adjust Counter. Read-write. Reset: 4h. Specifies the counter used to adjust the inter-packet gap for test packet.
3:2	Reserved.
1	InterruptrouteControlonForcePortResume: Interrupt route Control on ForcePortResume. Read-write. Reset: 0. This bit only takes effect when the EnableInterruptOnForcePortResume=1. 0=Report interrupt to EHCI[3:1]x24 [UsbInt] bit on software clear EHCI[3:1]x[70,6C,68,64] [ForcePortResume]. 1=Report interrupt to EHCI[3:1]x24 [PortChangeDetect] bit on software clear EHCI[3:1]x[70,6C,68,64] [ForcePortResume].
0	EnableInterruptonForcePortResume: Enable Interrupt on ForcePortResume. Read-write. Reset: 0. 1=Enable host controller to generate interrupt on software clear EHCI[3:1]x[70,6C,68,64] [ForcePortResume].

EHCI[3:1]xC0 USB Common PHY CAL and Control

Bits	Description
31	Reserved.
30:24	CommonPhyCalBus. Read-only; updated-by-hardware. Reset: X. PHY Common Calibration Bus.
23	Reserved.
22:20	ComCalAmp. Read-only; updated-by-hardware. Reset: X. Specifies the amplitude calibration data from PHY.
19:18	Reserved.
17	AddToCommonCalibration. Read-write. Reset: 1. BIOS: 0. 1=The signed NewCalBus is added to the ComCalBus and returned to the PHY ports; Any overflow is clamped to all 1s; Any underflow is clamped to all 0s. 0=The signed NewCalBus replaces the ComCalBus and returns to the PHY ports if UseCommonCalibration=0.
16	UseCommonCalibration. Read-write. Reset: 0. BIOS: 1. 1=The PHY's calibration value in ComCalBus is returned to the PHY ports. 0=The value after adjustment is returned to the PHY ports.
15:8	NewCalBus. Read-write. Reset: 0. BIOS: 0. New calibration bus signed value.
7	Reserved.
6:0	ComCalBus. Read-only; updated-by-hardware. Reset: X. Calibration bus value from PHY before adjustment.

EHCI[3:1]xC4 USB Common PHY Control 1BIOS: See [2.15.2.6](#).

Bits	Description										
31:24	DLLControl: DLL Control. Read-write. Reset: A0h. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[1:0]</td> <td>Reserved.</td> </tr> <tr> <td>[2]</td> <td>DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.</td> </tr> <tr> <td>[5:3]</td> <td>DLL_cpump. DLL charge pump current control.</td> </tr> <tr> <td>[7:6]</td> <td>DLL_VtoI. DLL gain control.</td> </tr> </tbody> </table>	Bit	Definition	[1:0]	Reserved.	[2]	DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.	[5:3]	DLL_cpump. DLL charge pump current control.	[7:6]	DLL_VtoI. DLL gain control.
Bit	Definition										
[1:0]	Reserved.										
[2]	DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.										
[5:3]	DLL_cpump. DLL charge pump current control.										
[7:6]	DLL_VtoI. DLL gain control.										
23:21	Reserved.										
20	PLLBypass: PLL Bypass. Read-write. Reset: 0. 1=Enable USB Common PLL bypass.										

19:16	DutyAdj. Read-write. Reset: 4h. Specifies CLK480 duty cycle control from 40-60% to 60-40%.
15:12	PVI. Read-write. Reset: 2h. Specifies PLL V-I Converter Control for common block PLL.
11:8	IRefAdj. Read-write. Reset: 1. Specifies internal reference bias adjustment for common block.
7:4	XRefAdj. Read-write. Reset: 1. Specifies external reference bias adjustment for common block.
3:0	CPAdj. Read-write. Reset: 4h. Charge pump setting for common block PLL.

EHCI[3:1]xD0 USB Common PHY Control 2

Bits	Description
31:16	Reserved.
15	BgBypass. Read-write. Reset: 0. Bandgap bypass.
14	Reserved.
13:12	PllLockAdj[1:0]. Read-write. Reset: 0. PLL lock detection tuning.
11	UnlockSticky. Read-only. Reset: X. Sticky unlock detection observability.
10	UnlockReset. Read-write. Reset: 0. Reset sticky un-lock detector.
9	LockDetect. Read-only. Reset: X. Lock detection observability.
8	EnLockDetect. Read-write. Reset: 0. Enable PLL lock detection.
7:4	CBackUp. Read-write. Reset: 0h. Common block backup.
3:0	BgAdj. Read-write. Reset: 6. BIOS: See 2.15.2.6 . Bandgap voltage adjust.

EHCI[3:1]xD4 USB Common PHY Control 3BIOS: See [2.15.2.6](#).

Bits	Description
31:8	Reserved.
7:6	PllFilter. Read-write. Reset: 0. PLL Filter tuning setting.
5:4	PllDiv. Read-write. Reset: 0. PLL divider setting.
3:2	PllReg. Read-write. Reset: 0. PLL Regulator tuning setting.
1	CalEnable. Read-write. Reset: 0. Calibration Enable.
0	BgStart. Read-write. Reset: 0. Bandgap startup tuning setting.

EHCI[3:1]xDC USB Battery Charger Enable

Bits	Description
31:4	Reserved.
3:0	UsbBatteryChargerEnable. Read-write. Reset: 0. One bit controls one respective port. For each bit, 1=Enable USB PHY battery charger function for the port.

3.26.4.3 USB 3.0 (xHCI)

The xHCI controller has a PCI configuration register space and two memory mapped IO register spaces. The PCI configuration register space uses device 10h function 0 and is defined below as D10F0xXX. The two memory mapped IO register spaces are defined in [3.27.4.3.2 \[xHCI Memory Mapped IO Configuration Registers\]](#) and [3.26.4.3.2 \[xHCI Power Management Registers\]](#).

3.26.4.3.1 Device 10h Function 0 (xHCI) Configuration Registers

See [3.1 \[Register Descriptions and Mnemonics\]](#) for a description of the register naming convention. See [2.7 \[Configuration Space\]](#) for details about how to access this space.

D10F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: Device ID. Read-only. Reset: 7814h. Device Identifier. Programmable through PCI/JTAG path and locked by (D10F0x4C_x04 [CfgWriteOnceLock]==1).
15:0	VendorID: Vendor ID. Read-only. Reset: 1022h. Vendor Identifier. Programmable through PCI/JTAG path and locked by (D10F0x4C_x04 [CfgWriteOnceLock]==1).

D10F0x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; set-by-hardware; write-1-to-clear. Reset: 0.
30	SignaledSystemError: Signaled System Error. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=System error signaled via SERR#.
29	ReceivedMasterAbort: Received Master Abort. Read; set-by-hardware; write-1-to-clear. Reset: 0.
28	ReceivedTargetAbort: Received Target Abort. Read; set-by-hardware; write-1-to-clear. Reset: 0.
27	SignaledTargetAbort: Signaled Target Abort. Read; set-by-hardware; write-1-to-clear. Reset: 0.
26:25	DEVSELTiming: DEVSEL Timing. Value: 0.
24	MasterDataParityError: Master Data Parity Error. Read; set-by-hardware; write-1-to-clear. Reset: 0.
23	FastBack2BackCapable: Fast Back-to-Back Capable. Value: 0.
22	Reserved.
21	Capable66MHz: 66 MHz Capable. Value: 0.
20	CapabilitiesList: Capabilities List. Value: 1. 1=Indicates that the value read at offset 34h is a pointer in Configuration Space to a linked list of new capabilities.
19	InterruptStatus: Interrupt Status. Read-only. Reset: 0. 1=An INTx interrupt Message is pending in the device.
18:11	Reserved.
10	InterruptDisable: Interrupt Disable. Read-only. Reset: 0. 0=Enable the assertion of the device/function's INTx# signal. 1=Disable the assertion of the device/function's INTx# signal.

9	FastBack2BackEnable: Fast Back-to-Back Enable. Value: 0. 0=Only fast back-to-back transactions to the same agent are allowed.
8	SERREnable: SERR# Enable. Read-write. Reset: 0. 1=System error reporting enabled.
7	RAZ.
6	ParityEnable: Parity Enable. Read-write. Reset: 0. 0=The device sets its DetectedParityError when an error is detected, but continues normal operations without asserting PERR#. 1=The device must take its normal action when a parity error is detected.
5	VgaPaletteRegisterAccesses: VGA palette register accesses. Value: 0. 0=The device should treat palette write accesses like all other accesses.
4	MemoryWriteandInvalidateCommand: Memory Write and Invalidate Command. Value: 0. 0=Memory Write must be used.
3	SpecialCycle: Special Cycle. Value: 0. 0=No Special Cycle support.
2	BusMaster: Bus Master. Read-write. Reset: 0. 0=Disable the device from generating PCI accesses. 1=Allow the device to behave as a bus master.
1	MemorySpaceAccesses: Memory Space Accesses. Read-write. Reset: 0. 0=Disable the device response. 1=Allow the device to respond to Memory Space accesses.
0	IOSpaceAccesses: IO Space Accesses. Value: 0. 0=IO accesses targeting this device are not accepted.

D10F0x08 Revision ID / Class Code

Bits	Description
31:24	BaseClass: Base Class. Read-only. Reset: Ch. Base Class. Serial Bus Controller.
23:16	SubClass: Sub Class. Read-only. Reset: 3h. Sub Class. Universal Serial Bus Host Controller.
15:8	ProgrammingInterface: Programming Interface. Read-only. Reset: 30h. Programming Interface. USB 3.0 Host Controller that conforms to xHC specification.
7:0	RevisionID. Read-only. IF (RevA0) THEN Reset: 00h. ELSEIF (RevA1) THEN Reset: 01h. ENDIF.

D10F0x0C Miscellaneous

Bits	Description
31:24	Bist. Value: 0. 00h=BIST is not supported.
23:16	HeaderType: Header Type. Value: 00h. 00h=The device does not have multiple functions. Bit 7 of this field can be modified through XHCI_PMx28[PciHeaderTypeBit7] .
15:8	LatencyTimer: Latency Timer. Value: 0.
7:0	CacheLineSize: Cache Line Size. Read-write. Reset: 0. This read/write field specifies the system cache line size in units of doublewords and must be initialized to 00h.

D10F0x10 Bar 0

Bits	Description
31:4	Bar0. Read-write. Reset: 0. Specifies Base Address [31:4]. See 3.27.4.3.2 [xHCI Memory Mapped IO Configuration Registers] .
3	PM: Prefetch memory. Value: 0. 0=Indicates that there is no support for prefetchable memory.
2:1	Tp: Type. Value: 10b. 10b=64 bit address.
0	Ind: Indicator. Value: 0. 0=Indicates that the operational registers of the device are mapped into memory space of the main memory of the PC host system.

D10F0x14 Bar 1

Bits	Description
31:0	Bar1: Base Address High. Read-write. Reset: 0. Specifies Base Address [63:32]. See 3.27.4.3.2 [xHCI Memory Mapped IO Configuration Registers] .

D10F0x2C Subsystem Vendor ID / Subsystem ID

Bits	Description
31:16	SubsystemID: Subsystem ID. Read-only. Reset: 7814h. Subsystem ID. Programmable through PCI/JTAG path and locked by (D10F0x4C_x04 [CfgWriteOnceLock]==1).
15:0	SubsystemVendorID: Subsystem Vendor ID. Read-only. Reset: 1022h. Subsystem Vendor ID. Programmable through PCI/JTAG path and locked by (D10F0x4C_x04 [CfgWriteOnceLock]==1).

D10F0x34 Capability Pointer

Bits	Description
7:0	CapabilityPointer: Capability Pointer. Read-only. Reset: 50h. Address of the 1st element of capability link.

D10F0x3C Interrupt Line

Bits	Description
31:16	Reserved.
15:8	InterruptPin: Interrupt Pin. Read-only. Reset: 1. Specifies which interrupt pin the device (or device function) uses. A value of 1 corresponds to INTA#.
7:0	InterruptLine: Interrupt Line. Read-write. Reset: 0. Specifies which input of the system interrupt controller(s) the device's interrupt pin is connected to. The device itself does not use this value; rather it is used by device drivers and operating systems to determine priority and vector information.

D10F0x40 IDP Index Register

Bits	Description
31:13	Reserved.
12:2	IDPIndex: IDP Index. Read-only. Reset: 0. This register selects the doubleword offset of the memory mapped register to be accessed. All register accesses are at doubleword granularity.
1:0	Reserved.

D10F0x44 IDP Data Register

Bits	Description
31:0	IDPData: IDP Data. Read-only. Reset: 0. Specifies the data read from or written to the memory mapped register pointed to by D10F0x40 . A physical register is not actually implemented as the data is actually stored in the memory mapped registers. The default value is the same as the default value of the register pointed to by D10F0x40 . D10F0x4C_x04 [CfgWriteOnceLock]==1 is used to prevent use of indirect data register.

D10F0x48 Indirect PCI Index Register

Bits	Description												
31:30	IndirectPCIIndex[31:30]: Indirect PCI Index. Read-write. Reset: 0. Selects the PCI indirect space. This field is combined with IndirectPCIIndex[15:2] to select the PCI indirect register to be accessed. <ul style="list-style-type: none"> IndirectPCIIndex[31:0] range for 3.26.4.3.1.1 [USB 3.0 125 MHz PCI Indirect Space]: 0000_FFFFh-0000_0000h. IndirectPCIIndex[31:0] range for 3.26.4.3.1.2 [USB 3.0 60 MHz PCI Indirect Space]: 4000_FFFFh-4000_0000h. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Selects 125 MHz PCI indirect space</td> <td>10b</td> <td>Reserved</td> </tr> <tr> <td>01b</td> <td>Selects 60 MHz PCI indirect space</td> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Selects 125 MHz PCI indirect space	10b	Reserved	01b	Selects 60 MHz PCI indirect space	11b	Reserved
Bits	Definition	Bits	Definition										
00b	Selects 125 MHz PCI indirect space	10b	Reserved										
01b	Selects 60 MHz PCI indirect space	11b	Reserved										
29:16	Reserved.												
15:2	IndirectPCIIndex[15:2]: Indirect PCI Index. Read-write. Reset: 0. Selects the doubleword offset of the PCI indirect space register to be accessed. All register accesses are at doubleword granularity.												
1:0	Reserved.												

D10F0x4C Indirect PCI Data Register

Bits	Description
31:0	IndirectPCIData: Indirect PCI Data. Read-write. Reset: 0. Specifies the data written to/read from the PCI indirect space register pointed to by D10F0x48 . A physical register is not actually implemented as the data is actually stored in the PCI indirect space registers. The default value is the same as the default value of the register pointed to by D10F0x48 .

3.26.4.3.1.1 USB 3.0 125 MHz PCI Indirect Space

These registers are indirectly accessed through [D10F0x48](#) and [D10F0x4C](#).

D10F0x4C_x08 Port Disable Write Once

Bits	Description						
31:2	Reserved.						
1:0	XhcPortDisableWriteOnce: xHC Port Disable Write Once. Read; write-once; write-1-only. Reset: 0. This field is bit significant. Once written, the register can only be cleared by PciRst#. For each bit, 1=Disable the corresponding port. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>port 0</td> </tr> <tr> <td>[1]</td> <td>port 1</td> </tr> </tbody> </table> If (D10F0x4C_x08 [XhcPortDisableWriteOnce] D10F0x4C_x0C [XhcPortDisableRW]), then the corresponding xHC port is disabled.	Bit	Definition	[0]	port 0	[1]	port 1
Bit	Definition						
[0]	port 0						
[1]	port 1						

D10F0x4C_x0C Port Disable RW

Bits	Description						
31:2	Reserved.						
1:0	XhcPortDisableRW: xHC Port Disable RW. Read-write. Reset: 0. This field is bit significant. For each bit, 1=The corresponding port is disabled. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>port 0</td> </tr> <tr> <td>[1]</td> <td>port 1</td> </tr> </tbody> </table> If (D10F0x4C_x08 [XhcPortDisableWriteOnce] D10F0x4C_x0C [XhcPortDisableRW]), then the corresponding xHC port is disabled.	Bit	Definition	[0]	port 0	[1]	port 1
Bit	Definition						
[0]	port 0						
[1]	port 1						

D10F0x4C_x10 USB DCLK Event Counter 0

Bits	Description
31:0	UsbDclkEventCnt0Lo. Read-only. Reset: 0. USB DClk Event Counter 0[31:0].

D10F0x4C_x14 USB DCLK Event Counter 1

Bits	Description
31:0	UsbDclkEventCnt1Lo. Read-only. Reset: 0. USB DClk Event Counter 1[31:0].

D10F0x4C_x18 USB DCLK Event Counter Select

Bits	Description
31:24	UsbDclkEventCnt1Hi. Read-only. Reset: 0. USB DClk Event Counter 1[39:32].
23:16	UsbDclkEventCnt0Hi. Read-only. Reset: 0. USB DClk Event Counter 0[39:32].

15:8	UsbDclkEventSel1 . Read-write. Reset: 0. Select the event to be counted by Usb DClk Event Counter 1.
7:0	UsbDclkEventSel0 . Read-write. Reset: 0. Select the event to be counted by Usb DClk Event Counter 0.

D10F0x4C_x1C USB DCLK Event Counter Control

Bits	Description
31:3	Reserved.
2	UsbDclkEventCntShadow . Read-write. Reset: 0. Transfer USB DClk event counter to shadow register.
1	UsbDclkEventCntResetb . Read-write. Reset: 1. Active low reset for USB DClk event counters.
0	UsbDclkEventCntEn . Read-write. Reset: 0. 1=Enable USB DClk event counters.

3.26.4.3.1.2 USB 3.0 60 MHz PCI Indirect Space

These registers are accessed through [D10F0x48](#) and [D10F0x4C](#).

D10F0x4C_x4000_0000 UTMI Control

BIOS: See [2.15.2.8](#), [2.15.2.10](#) & [2.15.2.11](#).

Bits	Description												
31:18	Reserved.												
17	VBusy . Read-only. Reset: 0. This bit is used to block software from writing to bit [16:8] when port router is updating the field.												
16:13	PortNumber: Port Number . Read-write. Reset: 0. Selects the corresponding port PHY or common block to load the VControl bits. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Port 0</td> <td>1110b-0010b</td> <td>Reserved</td> </tr> <tr> <td>0001b</td> <td>Port 1</td> <td>1111b</td> <td>Common block</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000b	Port 0	1110b-0010b	Reserved	0001b	Port 1	1111b	Common block
Bits	Definition	Bits	Definition										
0000b	Port 0	1110b-0010b	Reserved										
0001b	Port 1	1111b	Common block										
12	VLoadB . Read-write. Reset: 1. Update PHY control mode (active low). 0=Load the new VControl value to PHY/common block. 1=Only load VControlModeSel value to PHY to select different PHY status group (see D10F0x4C_x4000_0004); VControl[6:0] value inside PHY won't get affected.												
11	Reserved.												
10:7	VControlModeSel . Read-write. Reset: 0. Selects the PHY control mode group. See: EHCI[3:1]xB4[VControlModeSel] .												
6:0	VControl . Read-write. Reset: 24h. Controls PHY setting. See: EHCI[3:1]xB4[VControl] .												

D10F0x4C_x4000_0004 USB PHY Status

Bits	Description
31:16	Reserved.

15:8	Port1PhyStatus . Read-only; updated-by-hardware. Reset: 21h. Specifies the PHY Status of Port 1. Use the D10F0x4C_x4000_0000[VControlModeSel] to select which group's status should be read back.
7:0	Port0PhyStatus . Read-only; updated-by-hardware. Reset: 21h. PHY Status of Port 0. Use the D10F0x4C_x4000_0000[VControlModeSel] to select which group's status should be read back.

D10F0x4C_x4000_0008 USB Common PHY Calibration and Control

Bits	Description
31	Reserved.
30:24	CommonPhyCalBus . Read-only; updated-by-hardware. Reset: X. Specifies PHY common calibration bus.
23	Reserved.
22:20	ComCalAmp . Read-only; updated-by-hardware. Reset: X. Specifies the amplitude calibration data from PHY.
19:18	Reserved.
17	AddToCommonCalibration . Read-write. Reset: 1. BIOS: 0. 1=The signed NewCalBus is added to the ComCalBus and returned to the PHY ports; Any overflow is clamped to all 1s; Any underflow is clamped to all 0s. 0=The signed NewCalBus replaces ComCalBus and returns to the PHY ports.
16	UseCommonCalibration . Read-write. Reset: 0. BIOS: 1. 1=The PHY's calibration value in ComCalBus is returned to the PHY ports. 0=The value after adjustment is returned to the PHY ports.
15:8	NewCalBus . Read-write. Reset: 0. BIOS: 0. Specifies the new calibration bus signed value.
7	Reserved.
6:0	ComCalBus . Read-only; updated-by-hardware. Reset: X. Specifies the common calibration bus value from PHY before adjustment.

D10F0x4C_x4000_000C USB Common PHY ControlBIOS: See [2.15.2.8 \[xHC USB2.0 Common PHY Calibration\]](#).

Bits	Description										
31:24	DllControl: DLL Control . Read-write. Reset: A0h. Specifies USB PHY DLL control. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[1:0]</td> <td>Reserved.</td> </tr> <tr> <td>[2]</td> <td>DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.</td> </tr> <tr> <td>[5:3]</td> <td>DLL_cpump. DLL charge pump current control.</td> </tr> <tr> <td>[7:6]</td> <td>DLL_VtoI. DLL gain control.</td> </tr> </tbody> </table>	Bit	Definition	[1:0]	Reserved.	[2]	DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.	[5:3]	DLL_cpump. DLL charge pump current control.	[7:6]	DLL_VtoI. DLL gain control.
Bit	Definition										
[1:0]	Reserved.										
[2]	DLL_EN_PFDphases. 1=Enable DLL phase-sampling based lock detection.										
[5:3]	DLL_cpump. DLL charge pump current control.										
[7:6]	DLL_VtoI. DLL gain control.										
23:21	Reserved.										
20	PllBypass: PLL Bypass . Read-write. Reset: 0. 1=Enable USB Common PLL bypass.										
19:16	DutyAdj . Read-write. Reset: 4h. Specifies CLK480 duty cycle control from 40-60% to 60-40%. Only bits [2:0] are used; bit [3] doesn't have any effect on common block control.										
15:12	PVI . Read-write. Reset: 2h. Specifies PLL V-I converter control for common block PLL. Only bits [2:0] are used; bit [3] doesn't have any effect on common block control.										

11:8	IRefAdj. Read-write. Reset: 1. Specifies internal reference bias adjustment for common block. Only bits [2:0] are used, bit [3] doesn't have any effect on common block control.
7:4	XRefAdj. Read-write. Reset: 1. Specifies external reference bias adjustment for common block. Only bits [2:0] are used, bit [3] doesn't have any effect on common block control.
3:0	CPAdj. Read-write. Reset: 4h. Specifies charge pump setting for common block PLL. Only bits [2:0] are used, bit [3] doesn't have any effect on common block control.

D10F0x4C_x4000_0010 HS Loopback Test

Bits	Description						
31:23	Reserved.						
22:21	StatusOfPowerUpStateCheck: Status of ports for PowerUp State Check. Read-only; updated-by-hardware. Reset: 0. This field is bit-significant. It indicates the Power Up state auto-checking result from the individual port. For each bit, 0=PHY Power Up State checking failed. 1=PHY Power Up State checking is good. <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Port 0</td> </tr> <tr> <td>[1]</td> <td>Port 1</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	Port 0	[1]	Port 1
<u>Bit</u>	<u>Definition</u>						
[0]	Port 0						
[1]	Port 1						
20	EnablePHYPowerUpStateChecking. Read-write. Reset: 0. 1=Enable auto-checking on PHY Power Up State. There is built-in logic to check the PHY default Power Up state to detect manufacturing defects in the PHY macro.						
19:12	GoodReceivedPacketCount. Read-only; updated-by-hardware. Reset: 0. Specifies the number of good packets that the host controller received during the loopback test mode. These bits will be cleared by programming EnableLoopBackTest=0.						
11	Reserved.						
10	LoopbackTestDone. Read-only. Reset: 0. 1=Loopback test is done.						
9	LoopbackTestStatus. Read-only. Reset: 0. 0=CRC error on loopback receiving data. 1=Good CRC on loopback receiving data.						
8	EnableLoopBackTest. Read-write. Reset: 0. 1=Enable external USB port loopback test. The loopback test is to set one port to TX mode (Test Packet mode) and one port to RX mode (Test SE0_NAK). See EHCI[3:1]x[70,6C,68,64][PortTestControl] for information on the tests.						
7:4	Reserved.						
3:0	RxPktCnt: Received Packet Count. Read-write. Reset: 0. This counter defines the number (in power of 16) of RX data packets that should be checked for the loop back test.						

D10F0x4C_x4000_0014 CL Loopback Control

Bits	Description
31	LoopBackTestDone. Read-only; updated-by-hardware. Reset: 0. Host controller sets the bit when loop back is done. The bit is cleared when software clears the LoopBackTestStart bit. 1=Loopback test is done.

30:16	LoopBackTestStatus . Read-only; updated-by-hardware. Reset: 0. This field is bit-significant. It specifies the loopback test status for the port under test. Software can only check these status bits when the LoopBackTestDone bit is set by the host controller. These bits can only be cleared when software clears the LoopBackTestStart bit. For each bit, 0=Fail. 1=Pass.								
	<table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Port 0</td> </tr> <tr> <td>[1]</td> <td>Port 1</td> </tr> <tr> <td>[4:2]</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	Port 0	[1]	Port 1	[4:2]	Reserved
<u>Bit</u>	<u>Definition</u>								
[0]	Port 0								
[1]	Port 1								
[4:2]	Reserved								
15:8	LoopBackTestData . Read-write. Reset: 0. Specifies the 1-byte test data pattern for transmit; receive logic checks the received data to match with this data pattern.								
7:4	PortUnderTest . Read-write. Reset: 0. Software selects the port under test through these bits.								
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0001b-0000b</td> <td>Port number <PortUnderTest></td> </tr> <tr> <td>1111b-0010b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0001b-0000b	Port number <PortUnderTest>	1111b-0010b	Reserved		
<u>Bits</u>	<u>Definition</u>								
0001b-0000b	Port number <PortUnderTest>								
1111b-0010b	Reserved								
3:1	Reserved.								
0	LoopBackTestStart . Read-write. Reset: 0. Software sets this bit to start the loopback test and clears this bit to clear out all the test status before starting the next loop. 1=Start the loopback test. 0=Clear LoopBackTestStatus and LoopBackTestDone.								

D10F0x4C_x4000_0018 Misc Control

Bits	Description
31:12	Reserved.
11:8	InterPacketGapAdjustCounter . Read-write. Reset: 4h. Specifies the counter used to adjust the inter-packet gap for test packet.
7:3	Reserved.
2	TestPacketInterPacketGapEnable . Read-write. Reset: 1. 1=Enable inter-packet gap function for general test packet mode.
1	Reserved.
0	U2IFPowerSavingEnable . Read-write. Reset: 1. 1=Enable power saving clock gating; dynamic clock gating is enabled when U2IF trans_state is in idle state. (The clock going to all memory modules can be gated off. Blink clock also can get gated off unless the connection interrupt is detected).

D10F0x4C_x4000_0020 USB SCLK Event Counter 0

Bits	Description
31:0	UsbSclkEventCnt0Lo . Read-only. Reset: 0. USB SClk Event Counter 0[31:0].

D10F0x4C_x4000_0024 USB SCLK Event Counter 1

Bits	Description
31:0	UsbSclkEventCnt1Lo . Read-only. Reset: 0. USB SClk Event Counter 1[31:0].

D10F0x4C_x4000_0028 USB SCLK Event Counter Select

Bits	Description
31:24	UsbSclkEventCnt1Hi. Read-only. Reset: 0. USB SClk Event Counter 1[39:32].
23:16	UsbSclkEventCnt0Hi. Read-only. Reset: 0. USB SClk Event Counter 0[39:32].
15:8	UsbSclkEventSel1. Read-write. Reset: 0. Selects event to be counted by USB SClk Event Counter 1.
7:0	UsbSclkEventSel0. Read-write. Reset: 0. Selects event to be counted by USB SClk Event Counter 0.

D10F0x4C_x4000_002C USB SCLK Event Counter Control

Bits	Description
31:3	Reserved.
2	UsbSclkEventCntShadow. Read-write. Reset: 0. 1=Transfer USB SClk event counter to shadow register.
1	UsbSclkEventCntResetB. Read-write. Reset: 1. 0=Resets USB SClk event counters.
0	UsbSclkEventCntEn. Read-write. Reset: 0. 1=Enable USB SClk event counters.

D10F0x4C_x4000_0048 LPM Control

Bits	Description																				
31:18	Reserved.																				
17	CfguP1VirLpmRespEn: Port1 Virtual LPM Response Enable. Read-write. Reset: 0. 0=Disable virtual LPM Response. 1=Force a virtual response of port 1 LPM transaction. The type of response is determined by CfguP1VirLpmResp.																				
16:14	CfguP1VirLpmResp: Port1 Virtual LPM Response. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>ACK</td> <td>100b</td> <td>Reserved</td> </tr> <tr> <td>001b</td> <td>Reserved</td> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>010b</td> <td>STALL</td> <td>110b</td> <td>TIMEOUT</td> </tr> <tr> <td>011b</td> <td>NYET</td> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	ACK	100b	Reserved	001b	Reserved	101b	Reserved	010b	STALL	110b	TIMEOUT	011b	NYET	111b	Reserved
Bits	Definition	Bits	Definition																		
000b	ACK	100b	Reserved																		
001b	Reserved	101b	Reserved																		
010b	STALL	110b	TIMEOUT																		
011b	NYET	111b	Reserved																		
13	CfguP0VirLpmRespEn: Port0 Virtual LPM Response Enable. Read-write. Reset: 0. 0=Disable virtual LPM Response. 1=Force a virtual response of port 0 LPM transaction. The type of response is determined by CfguP0VirLpmResp.																				
12:10	CfguP0VirLpmResp: Port0 Virtual LPM Response. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>ACK</td> <td>100b</td> <td>Reserved</td> </tr> <tr> <td>001b</td> <td>Reserved</td> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>010b</td> <td>STALL</td> <td>110b</td> <td>TIMEOUT</td> </tr> <tr> <td>011b</td> <td>NYET</td> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	ACK	100b	Reserved	001b	Reserved	101b	Reserved	010b	STALL	110b	TIMEOUT	011b	NYET	111b	Reserved
Bits	Definition	Bits	Definition																		
000b	ACK	100b	Reserved																		
001b	Reserved	101b	Reserved																		
010b	STALL	110b	TIMEOUT																		
011b	NYET	111b	Reserved																		
9	CfguDevRecoveryDis: Device Recovery Timer Disable. Read-write. Reset: 0. 1=xHC does not wait for the device recovery time.																				

8:5	CfguRWakeRsmDuration[3:0]: Remote Wake Resume Duration. Read-write. Reset: 0. Software sets this field to indicate how long the xHC should stay in L1Resuming after remote wake is detected. The L1 Resume Timer will load this duration after remote wake is detected and HLE is 0. When the timer expires, the Root Hub state will jump to SENDEOR.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	0000b	60 us	1011b-0011b	60 us + value * 75 us
	0001b	135 us	1100b	960 us
	0010b	210 us	1111b-1101b	Reserved
4:0	CfguL1ResidencyDuration: L1 Residency Duration. Read-write. Reset: 0. BIOS: 1. Software sets this field to indicate the minimum duration that the xHC should stay in L1Suspend. The L1 Residency Timer will load this duration when LPM transaction ACK is received and HLE is 0. When the timer expires and there is either Hardware Initiated L1 Resume Request or Remote Wake detected, the Root Hub state will jump to L1Resuming.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	00000b	50 us	11110b-00010b	(value + 1)* 50 us
	00001b	100 us	11111b	1.6 ms

D10F0x4C_x4000_0050 USB Common PHY Control 2

BIOS: See [2.15.2.8 \[xHC USB2.0 Common PHY Calibration\]](#).

Bits	Description
3:0	BgAdj. Read-write; S3-check-exclude. Reset: 6. Bandgap voltage adjust.

D10F0x4C_x4000_0054 USB Common PHY Control 3

BIOS: See [2.15.2.8 \[xHC USB2.0 Common PHY Calibration\]](#).

Bits	Description
1	CalEnable. Read-write. Reset: 0. 1=Enable calibration.

D10F0x50 PME Capability

Bits	Description	
31:27	PmeSupport. Read-only. Reset: 19h. Indicates the power states in which the function may assert PME#. For each bit, 0=The function is not capable of asserting the PME# signal while in that power state.	
	<u>Bit</u>	<u>Definition</u>
	[0]	1=PME# can be asserted from D0
	[1]	1=PME# can be asserted from D1
	[2]	1=PME# can be asserted from D2
	[3]	1=PME# can be asserted from D3hot
	[4]	1=PME# can be asserted from D3cold
26	D2Support. Read-only. Reset: 0. 0=This function doesn't support the D2 Power Management State.	
25	D1Support. Read-only. Reset: 0. 0=This function doesn't support the D1 Power Management State.	

24:22	AuxCurrent. Read-only. Reset: 0. Specifies the 3.3 V auxiliary current requirements for the PCI function. Since D10F0x54[Data] is implemented by this function, reads of this field must return a value of 000b; D10F0x54[Data] takes precedence over this field for 3.3 V auxiliary current requirement reporting.
21	DSI: Device Specific Initialization. Read-only. Reset: 0. This bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.
20	Reserved.
19	PmeClock: PME clock. Read-only. Reset: 0. 0=Indicates that no PCI clock is required for the function to generate PME#.
18:16	Version. Read-only. Reset: 011b. 011b=Indicates that this function complies with Revision 1.2 of the PCI Power Management Interface Specification.
15:8	NextItemPointer: Next Item Pointer. Read-only. Reset: 70h. Points to the location of next item in the function's capability list.
7:0	CapId. Read-only. Reset: 1. The linked list item is for PCI Power Management.

D10F0x54 PME Control / Status

Bits	Description
31:24	Data. Read-only. Reset: 0. Reports the state dependent data requested by D10F0x54[DataSelect]. The value of this field is scaled by D10F0x54[DataScale].
23:16	Reserved.
15	PmeStatus. Read; set-by-hardware; write-1-to-clear. Cold reset: 0. BIOS: See 2.15.2.13. 1=The PME# signal is asserted, which is independent of PmeEn. 0=PME# is de-asserted. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
14:13	DataScale. Read-only. Reset: 0. Indicates the scaling factor to be used when interpreting the value of D10F0x54[Data]. The value and meaning of this field will vary depending on which data value has been selected by D10F0x54[DataSelect].
12:9	DataSelect. Read-only. Reset: 0. Selects which data is to be reported through D10F0x54[Data] and D10F0x54[DataScale].
8	PmeEn. Read-write. Cold reset: 0. 1=Enable the function to assert PME# if PmeStatus=1. 0=PME# assertion is disabled. This bit defaults to 0 if the function does not support PME# generation from D3cold. If the function supports PME# from D3cold, then this bit is sticky and must be explicitly cleared by the operating system each time the operating system is initially loaded.
7:4	Reserved.

3	NoSoftReset. Read-only. Reset: 1. 1=Upon transitioning from D3hot to D0 because of PowerState, devices do not perform an internal reset ; Configuration context is preserved; No additional operating system intervention is required to preserve configuration context beyond writing the PowerState bits. 0=Upon transitioning from D3hot to D0 via software control of the PowerState bits, devices do perform an internal reset; Configuration context is lost; Full reinitialization sequence is needed to return the device to D0 Initialized. Regardless of this bit, devices that transition from D3hot to D0 by a system or bus segment reset will return to the device state D0 uninitialized with only PME context preserved if PME is supported and enabled. This bit is read-writeable by PCI/JTAG path and AHB path rather than read-only defined in PCI PM 1.2 spec.												
2	Reserved.												
1:0	PowerState. Read-only. Reset: 0. This field determines the current power state of a function and sets the function into a new power state. When doing FLR, power state will be reset to D0 state immediately when D10F0xA8[InitiateFLR] is set. If software attempts to write an unsupported, optional state to this field, the write operation must be completed normally on the bus; however, the data is discarded and no state change occurs. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>D0</td> <td>10b</td> <td>D2</td> </tr> <tr> <td>01b</td> <td>D1</td> <td>11b</td> <td>D3hot</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	D0	10b	D2	01b	D1	11b	D3hot
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>										
00b	D0	10b	D2										
01b	D1	11b	D3hot										

D10F0x60 SBRN

Bits	Description																				
31:24	Reserved.																				
23:20	DBESLD: Default Best Effort Service Latency Deep. Read-only. Reset: 0h. Vendor Defined. If the value of this field is non-zero, it defines the recommended value for programming XHCI_OPx4[3,2]C[BESLD] . This field can be modified through the backdoor register at XHCI_PMx24[DBESLDCtl] .																				
19:16	DBESL: Default Best Effort Service Latency. Read-only. Reset: 0h. Vendor Defined. If the value of this field is non-zero, it defines the recommended value for programming XHCI_OPx4[3,2]4[BESL] field. This field can be modified through the backdoor register at XHCI_PMx24[DBESLCtl] .																				
15:14	Reserved.																				
13:8	FLAdj: Frame Length Timing Value. Read-only. Reset: 20h. Each decimal value change to this register corresponds to 16 high-speed bit times. The SOF cycle time (number of SOF counter clock periods to generate a SOF microframe length)=59488 + 16*FLAdj. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th><u>Bits</u></th> <th><u>Frame Length (# HS bit times)</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>59488</td> </tr> <tr> <td>1</td> <td>59504</td> </tr> <tr> <td>2</td> <td>59520</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>31</td> <td>59984</td> </tr> <tr> <td>32</td> <td>60000</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>62</td> <td>60480</td> </tr> <tr> <td>63</td> <td>60496</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Frame Length (# HS bit times)</u>	0	59488	1	59504	2	59520	31	59984	32	60000	62	60480	63	60496
<u>Bits</u>	<u>Frame Length (# HS bit times)</u>																				
0	59488																				
1	59504																				
2	59520																				
...	...																				
31	59984																				
32	60000																				
...	...																				
62	60480																				
63	60496																				

7:0	SBRN: Serial Bus Specification Release Number. Value: 30h. Specifies the release of the Universal Serial Bus Specification with which this Universal Serial Bus Host Controller module is compliant with.
-----	--

D10F0x70 MSI Control

Bits	Description																				
31:25	Reserved.																				
24	PVMC: Per-vector masking capable. Read-only. Reset: 0. 1=The function supports MSI per-vector masking. 0=The function does not support MSI per-vector masking.																				
23	C64: 64-bit Address Capable. Read-only. Reset: 1. 1=The function is capable of sending a 64-bit message address. 0=The function is not capable of sending a 64-bit message address.																				
22:20	MME: Multiple Message Enable. Read-write. Reset: 0. System software writes to this field to indicate the number of allocated messages. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th># of messages allocated</th> <th>Bits</th> <th># of messages allocated</th> </tr> <tr> <td>000b</td> <td>1</td> <td>100b</td> <td>16</td> </tr> <tr> <td>001b</td> <td>2</td> <td>101b</td> <td>32</td> </tr> <tr> <td>010b</td> <td>4</td> <td>111b-110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>8</td> <td></td> <td></td> </tr> </table>	Bits	# of messages allocated	Bits	# of messages allocated	000b	1	100b	16	001b	2	101b	32	010b	4	111b-110b	Reserved	011b	8		
Bits	# of messages allocated	Bits	# of messages allocated																		
000b	1	100b	16																		
001b	2	101b	32																		
010b	4	111b-110b	Reserved																		
011b	8																				
19:17	MMC: Multiple Message Capable. Read-only. Reset: 011b. System software reads this field to determine the number of requested messages. 011b=8 messages requested.																				
16	MSIE: MSI Enable. Read-write. Reset: 0. 1=MSI is enabled and INTx# pins are not used to generate interrupts. 0=MSI is disabled and the traditional pins are used to request service.																				
15:8	NextItemPointer: Next Item Pointer. Read-only. Reset: 90h. Points to next the capability structure.																				
7:0	Capability. Read-only. Reset: 5h. MSI USB ID.																				

D10F0x74 MSI Address

Bits	Description
31:2	MsiAddress: MSI Address. Read-write. Reset: 0. Specifies the lower bits of system-specified message address [31:2]. Always doubleword aligned.
1:0	Reserved. Reset: X.

D10F0x78 MSI Upper Address

Bits	Description
31:0	MsiUpperAddress: MSI Upper Address. Read-write. Reset: 0. Specifies the system-specified message upper address [61:32].

D10F0x7C MSI Data

Bits	Description
15:0	MsiData: MSI Data. Read-write. Reset: 0. System-specified message.

D10F0x80 MSI Mask Bits

Bits	Description
31:0	MaskBits: Mask Bits. Read-write. Reset: 0. For each mask bit that is set, the function is prohibited from sending the associated message.

D10F0x90 MSI-X Control

Bits	Description
31	MsiXEnable: MSI-X Enable. Read-write. Reset: 0.
30	FunctionMask: Function Mask. Read-write. Reset: 0.
29:27	Reserved.
26:16	TableSize: Table Size. Read-only. Reset: 7h.
15:8	NextItemPointer: Next Item Pointer. Read-only. Reset: A0h.
7:0	CapabilityID: Capability ID. Read-only. Reset: 11h.

D10F0x94 MSI-X Table Offset/Table BIR

Bits	Description																				
31:3	TableOffset: Table Offset. Read-only. Reset: 200h. Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X Table. The lower 3 TableBIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.																				
2:0	TableBIR: Table BIR. Read-only. Reset: 0. Indicates which Base Address register, starting at 10h in the configuration space, is used to map the function's MSI-X table into memory space. For a 64-bit Base Address register, the TableBIR indicates the lower DWORD. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Base Address Register</th> <th>Bits</th> <th>Base Address Register</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>10h</td> <td>4h</td> <td>20h</td> </tr> <tr> <td>1h</td> <td>14h</td> <td>5h</td> <td>24h</td> </tr> <tr> <td>2h</td> <td>18h</td> <td>7h-6h</td> <td>Reserved</td> </tr> <tr> <td>3h</td> <td>1Ch</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Base Address Register	Bits	Base Address Register	0h	10h	4h	20h	1h	14h	5h	24h	2h	18h	7h-6h	Reserved	3h	1Ch		
Bits	Base Address Register	Bits	Base Address Register																		
0h	10h	4h	20h																		
1h	14h	5h	24h																		
2h	18h	7h-6h	Reserved																		
3h	1Ch																				

D10F0x98 MSI-X PBA Offset/PBA BIR

Bits	Description
31:3	PBAOffset: PBA Offset. Read-only. Reset: 210h. Used as an offset from the address contained by one of the function's Base Address registers to point to the base of the MSI-X PBA. The lower 3 PBA BIR bits are masked off (set to zero) by software to form a 32-bit QWORD-aligned offset.
2:0	PBABIR: PBA BIR. Read-only. Reset: 0. Indicates which Base Address register, strating at 10h in the configuration space, is used to map the functions MSI-X PBA into memory space. See: D10F0x94[TableBIR] .

D10F0xA0 PCIe Capability List

Bits	Description
31:30	Reserved.
29:25	IntMsgNum: Interrupt Message Number. Read-only. Reset: 0. This field indicates which MSI/MSI-X vector is used for the interrupt message generated in association with any of the status bits of this Capability structure.
24	SlotImplemented: Slot Implemented. Value: 0.
23:20	DevicePortType: Device/Port Type. Value: 9h. 9h=Indicates Root Complex Integrated Endpoint.
19:16	CapabilityVersion: Capability Version. Value: 2h. Indicates PCI-SIG defined PCI Express Capability structure version number. 2h=PCI Express Base Rev 2.0.
15:8	NextItemPointer: Next Item Pointer. Value: 0. 00h=End of linked list capabilities.
7:0	CapabilityID: Capability ID. Read-only. Reset: 10h. PCI Express Capability.

D10F0xA4 Device Capability

Bits	Description										
31:29	Reserved.										
28	FLRCapability: Function Level Reset Capability. Read-only. Reset: 0. Writing to D10F0x4C_x04[FlrEn] updates this field. This field applies to Endpoints only. 1=Function level reset is supported. 0=Function Level Reset is not supported.										
27:26	SlotPowerLimitScale: Captured Slot Power Limit Scale (Upstream Ports only). Value: 0. Specifies the scale used for the SlotPowerLimitValue. <table style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1.0 x</td> </tr> <tr> <td>01b</td> <td>0.1 x</td> </tr> <tr> <td>10b</td> <td>0.01 x</td> </tr> <tr> <td>11b</td> <td>0.001 x</td> </tr> </tbody> </table> This value is set by the Set_Slot_Power_Limit Message or hardwired to 00b.	Bits	Definition	00b	1.0 x	01b	0.1 x	10b	0.01 x	11b	0.001 x
Bits	Definition										
00b	1.0 x										
01b	0.1 x										
10b	0.01 x										
11b	0.001 x										
25:18	SlotPowerLimitValue: Captured Slot Power Limit Value (Upstream Ports only). Read-only. Reset: 0. In combination with SlotPowerLimitScale, specifies the upper limit on power supplied by slot. Power limit (in Watts)=SlotPowerLimitValue * SlotPowerLimitScale. This value is set by the Set_Slot_Power_Limit Message or hardwired to 00h. This field could be programmed through PCI/JTAG path.										
17:16	Reserved.										
15	RoleBasedErrorReport: Role-Based Error Reporting. Value: 1. 1=Indicates that the function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1.										
14:12	Reserved.										

11:9	EndpointL1AcceptableLatency: Endpoint L1 Acceptable Latency. Value: 111b. This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. It is essentially an indirect measure of the Endpoint's internal buffering. Power management software uses the reported L1 Acceptable Latency number to compare against the L1 Exit Latencies reported (see below) by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L1 entry can be used with no loss of performance. 111b=No limit.																				
8:6	EndpointL0sAcceptableLatency: Endpoint L0s Acceptable Latency. Value: 111b. This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. It is essentially an indirect measure of the Endpoints internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether ASPM L0s entry can be used with no loss of performance. 111b=No limit.																				
5	ExtTagFieldSup: Extended Tag Field Supported. Value: 0. This bit indicates the maximum supported size of the Tag field as a Requester. 0=Tag field size of 5-bits supported.																				
4:3	PhantomFunctSup: Phantom Functions Supported. Value: 0. 0=No Function Number bits are used for Phantom Functions.																				
2:0	MaxPayloadSizeSup: Max Payload Size Supported. Value: 0. This field indicates the maximum payload size that the function can support for TLPs. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Payload Size</th> <th>Bits</th> <th>Payload Size</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>128 bytes max payload size</td> <td>4h</td> <td>2048 bytes max payload size</td> </tr> <tr> <td>1h</td> <td>256 bytes max payload size</td> <td>5h</td> <td>4096 bytes max payload size</td> </tr> <tr> <td>2h</td> <td>512 bytes max payload size</td> <td>7h-6h</td> <td>Reserved</td> </tr> <tr> <td>3h</td> <td>1024 bytes max payload size</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Payload Size	Bits	Payload Size	0h	128 bytes max payload size	4h	2048 bytes max payload size	1h	256 bytes max payload size	5h	4096 bytes max payload size	2h	512 bytes max payload size	7h-6h	Reserved	3h	1024 bytes max payload size		
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1h	256 bytes max payload size	5h	4096 bytes max payload size																		
2h	512 bytes max payload size	7h-6h	Reserved																		
3h	1024 bytes max payload size																				

D10F0xA8 Device Control/Status

Bits	Description
31:22	Reserved.
21	TransPending: Transactions Pending. Read-only. Reset: 0. 1=The function has issued Non-Posted Requests which have not been completed. 0>All outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.
20	AUXPowerDetected: AUX Power Detected. Read-only. Reset: 0. 1=AUX power is detected by the function.
19	UnsupReqDetected: Unsupported Request Detected. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=The function received an Unsupported Request. Errors are logged in this register regardless of UnsupReqRptEn.
18	FatalErrDetected: Fatal Error Detected. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Fatal errors are detected. Errors are logged in this register regardless of FatalErRptEn.
17	NonFatalErrDetected: Non-Fatal Error Detected. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Nonfatal errors are detected. Errors are logged in this register regardless of NonFatalErrRptEn.
16	CorrErrDetected: Correctable Error Detected. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Correctable errors are detected. Errors are logged in this register regardless of CorrErrRptEn.

15	InitiateFLR: Initiate Function Level Reset. RAZ; write-1-only. Reset: 0. IF(D10F0x4C_x04[FlrEn]==1) THEN Writing 1 initiates Function Level Reset to the function. ELSE FLR is not supported; writing 1 doesn't initiate Function Level Reset to the function.																				
14:12	MaxReadRequestSize. Read-write. Reset: 010b. This field sets the maximum Read Request size for the function as a Requester. The function must not generate Read Requests with size exceeding the set value. 010b=512 bytes maximum Read Request size.																				
11	EnNoSnoop: Enable No Snoop. Read-write. Reset: 1. 1=Function is permitted to set the No Snoop bit in the Requester Attributes of transactions that it initiates and do not require hardware enforced cache coherency. Setting this bit to 1b should not cause a function to blindly set the No Snoop attribute on all transactions that it initiates. Even when this bit is set, a function is only permitted to set the No Snoop attribute on a transaction when it can ensure that the address of the transaction is not stored in any cache in the system.																				
10	AuxPowerPMEEn: Auxiliary Power PM Enable. Read-write. Cold reset: 0. 1=Enable a function to draw auxiliary (AUX) power independent of PME AUX power. Functions that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in D10F0x50[AuxCurrent] independent of D10F0x54[PmeEn]. Functions that consume AUX power must preserve the value of this sticky register when AUX power is available and preserve the value through Conventional Reset.																				
9	PhantomFunctionsEn: Phantom Functions Enable. Value: 0. 0=The Function is not allowed to use Phantom Functions.																				
8	ExtTagFieldEn: Extended Tag Field Enable. Value: 0. 0=Function is restricted to a 5-bit Tag field.																				
7:5	MaxPayloadSize. Read-write. Reset: 0. This field sets maximum TLP payload size for the function. as a receiver, the function must handle TLPs as large as the set value. As a Transmitter, the Function must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by D10F0xA4[MaxPayloadSizeSup]. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Payload Size</th> <th>Bits</th> <th>Payload Size</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>128 bytes max payload size</td> <td>4h</td> <td>2048 bytes max payload size</td> </tr> <tr> <td>1h</td> <td>256 bytes max payload size</td> <td>5h</td> <td>4096 bytes max payload size</td> </tr> <tr> <td>2h</td> <td>512 bytes max payload size</td> <td>7h-6h</td> <td>Reserved</td> </tr> <tr> <td>3h</td> <td>1024 bytes max payload size</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Payload Size	Bits	Payload Size	0h	128 bytes max payload size	4h	2048 bytes max payload size	1h	256 bytes max payload size	5h	4096 bytes max payload size	2h	512 bytes max payload size	7h-6h	Reserved	3h	1024 bytes max payload size		
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3h	1024 bytes max payload size																				
4	EnRelaxOrder: Enable Relaxed Ordering. Read-write. Reset: 1. 1= Function is permitted to set the Relaxed Ordering bit in the Attributes field of transactions that it initiates and do not require strong write ordering.																				
3	UnsupReqRptEn: Unsupported Request Reporting Enable. Read-write. Reset: 0. This bit, in conjunction with other bits, controls the signaling of Unsupported Requests by sending Error Messages.																				
2	FatalErrRptEn: Fatal Error Reporting Enable. Read-write. Reset: 0. This bit, in conjunction with other bits, controls sending ERR_FATAL Messages																				
1	NonFatalErrRptEn: Non-Fatal Error Reporting Enable. Read-write. Reset: 0. This bit, in conjunction with other bits, controls sending ERR_NONFATAL Messages																				
0	CorrErrRptEn: Correctable Error Reporting Enable. Read-write. Reset: 0. This bit, in conjunction with other bits, controls sending ERR_COR Messages																				

D10F0xC4 Device Capabilities 2

Bits	Description
31:12	Reserved.

11	LTRMechanismSupported: LTR Mechanism Supported. Read-only. Reset: 1. 1=Latency Tolerance Reporting (LTR) mechanism capability is supported.
10:5	Reserved.
4	CompletionTimeoutDisableSupported: Completion Timeout Disable Supported. Read-only. Reset: 1. 1=The Completion Timeout Disable mechanism is supported.
3:0	CompletionTimeoutRangesSupported: Completion Timeout Ranges Supported. Read-only. Reset: 0. Specifies the Completion Timeout value range that can be programmed into D10F0xC8[CompletionTimeoutValue] . 0=Completion Timeout programmability mechanism is not supported.

D10F0xC8 Device Control/Status 2

Bits	Description
31:11	Reserved.
10	LTRMechanismEnable: LTR Mechanism Enable. Read-write. Reset: 0. 1=Enable the Latency Tolerance Reporting (LTR) mechanism.
9:5	Reserved.
4	CompletionTimeoutDisable: Completion Timeout Disable. Read-write. Reset: 0. 1=Disable the Completion Timeout mechanism.
3:0	CompletionTimeoutValue: Completion Timeout Value. Read-only. Reset: 0. In device functions that support Completion Timeout programmability, this field allows system software to modify the Completion Timeout value. See D10F0xC4[CompletionTimeoutRangesSupported] .

D10F0x100 LTR Extended Capability Header

Bits	Description
31:20	NextCapabilityOffset: Next Capability Offset. Read-only. Reset: 00h. 00h=End of capability list.
19:16	CapabilityVersion: Capability Version. Read-only. Reset: 1.
15:0	PCIExpressExtendedCapabilityID: PCI Express Extended Capability ID. Read-only. Reset: 18h. Extended Capability ID for Latency Tolerance.

D10F0x104 Max Latency

Bits	Description
31:29	Reserved.
28:26	MaxNoSnoopLatencyScale: Max No-Snoop Latency Scale. Read-only. Reset: 0. This register provides a scale for the value contained within MaxNoSnoopLatencyValue. Encoding is the same as the Latency Scale fields in the LTR Message.
25:16	MaxNoSnoopLatencyValue: Max No-Snoop Latency Value. Read-only. Reset: 0. Along with MaxNoSnoopLatencyScale, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less.
15:13	Reserved.

12:10	MaxSnoopLatencyScale: Max Snoop Latency Scale. Read-only. Reset: 0. This register provides a scale for the value contained within MaxSnoop LatencyValue. Encoding is the same as the Latency Scale fields in the LTR Message.
9:0	MaxSnoopLatencyValue: Max Snoop Latency Value. Read-only. Reset: 0. Along with MaxSnoopLatencyScale, this register specifies the maximum no-snoop latency that a device is permitted to request. Software should set this to the platform's maximum supported latency or less.

3.26.4.3.1.3 USB xHCI Capability Registers (XHCI_CAP)

The base address of the xHCI Capability register space is specified by {D10F0x14[Bar1], D10F0x10[Bar0], 0h}.

XHCI_CAPx02 HC Interface Version

Bits	Description
15:0	HCIVersion: Host Controller Interface Version Number. Read-only. Reset: 96h. Contains a BCD encoding of the xHCI specification revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision. e.g. 0100h corresponds to xHCI version 1.0. Writing to XHCI_PMx30[HCIVersion10En] updates this field.

3.26.4.3.2 xHCI Power Management Registers

xHCI power management registers are accessed through the AcpiMmio region, which can be memory mapped or IO mapped. They range from [PMx24\[AcpiMmioAddr\]+1C00h](#) to [PMx24\[AcpiMmioAddr\]+1CFFh](#). See [PMx24 \[AcpiMmioEn\]](#). These registers reside in USB 3.0 and can hold their values during S3 or S5 state if the xHC host is programmed into D3 state before entering into S3/S5 state.

XHCI_PMx00 xHCI Config 0

Bits	Description
30	FwPreloadComplete: Firmware Preload Complete. Read-only; updated-by-hardware. Reset: 0. 1=Firmware preload is complete. 0=FwPreloadStart is cleared by software.
29	FwPreloadStart: Firmware Preload Start. Read-write. Reset: 0. BIOS: See 2.15.2.12 . When set from 0 to 1, firmware preload will be initiated. Upon completion of firmware preload (FwPreloadComplete==1), this field should be programmed to 0.
28	FwLoadMode: Firmware Load Mode. Read-write. Reset: 1. Controls whether the firmware will execute a bootstrap routine to load firmware into instruction ram, or whether instruction ram is to be preloaded. 0=xHCI will execute bootstrap routine. 1=xHCI will not execute bootstrap routine.
27	Reserved.
26	Xhc0BlmCgDis: xHC0 BLM Clock Gating Disable. Read-write. Reset: 0. BIOS: 0. IF (U3CoreReset==0) THEN clock gating takes effect. ENDIF. 1=Disable xHC0 BLM Clock Gating.
25	AIGcgDis: A-Link Global Clock Gating Disable. Read-write. Reset: 0. BIOS: 0. 1=Disable USB3.0 A-Link Global Clock Gating.
24	BIGcgDis: B-Link Global Clock Gating Disable. Read-write. Reset: 0. BIOS: 0. 1=Disable USB3.0 B-Link Global Clock Gating.

21	XhcSmibEn: xHC SMIB Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable XHC_SMIB to ACPI controller.
16:13	Reserved.
12	Reserved.
11	Xhc0Reset: xHC0 Reset. Read-write. Reset: 0. 1=Reset xHC0 core logic.
10	U3CoreReset: USB3 Core Reset. Read-write. Reset: 1. BIOS: See 2.15.2.12 . 1=Reset the USB3.0/xHCI (xHC0) core logic. 0=xHC clock gating enable.
9	U3pPhyReset: USB3 PHY Reset. Read-write. Reset: 1. 1=Reset SSPHYIF power control logic in 125 MHz clock domain.
8	U3pPllReset: USB3 PHY PLL Reset. Read-write. Reset: 1. 1=Reset USB3.0 PHY PLL and SSPHYIF power control logic in LFPS clock domain.
7	U3pLock: USB3 PHY PLL Lock. Read-only. Reset: 0. 1=USB3.0 PHY PLL is locked.
1	Reserved.
0	Xhci0Enable. Read-write. Reset: 0. BIOS: See 2.15.2.4 . 1=Enable xHCI0.

XHCI_PMx04 xHCI Firmware Addr 0

Bits	Description
31	XhciFwPreloadType. Read-write. Reset: 0. BIOS: See 2.15.2.12 . Controls the destination of the preload operation. 0=Instruction RAM. 1=Boot RAM.
30:17	Reserved.
16:0	XhciFwRomAddr. Read-write. Reset: 0. BIOS: See 2.15.2.12 . Specifies the address of the first byte of application firmware in external ROM.

XHCI_PMx08 xHCI Firmware Addr 1

Bits	Description
31:16	XhciFwSize: xHCI Firmware Size. Read-write. Reset: 0. BIOS: See 2.15.2.12 . Specifies the size of the application firmware in the external ROM.
15:0	XhciFwRamAddr: xHCI Firmware Start Address. Read-write. Reset: 0. BIOS: See 2.15.2.12 . Specifies the address where the first byte of application firmware is to be stored in boot RAM or instruction RAM.

XHCI_PMx10 xHCI Memory Config

Bits	Description
31:23	Reserved. Read-write.

15:8	<p>CcuMode: Clock Control Mode. Read-write. Reset: 07h. BIOS: 32h. This field contains a set of bits which, when set, enable individual features of the clock control unit.</p> <table border="0"> <thead> <tr> <th style="text-align: center;"><u>Bit</u></th><th style="text-align: center;"><u>Definition</u></th></tr> </thead> <tbody> <tr> <td style="text-align: center;">[0]</td><td>1=Enable power control mode.</td></tr> <tr> <td style="text-align: center;">[1]</td><td>1=Enable SuperSpeed remote wake mode.</td></tr> <tr> <td style="text-align: center;">[2]</td><td>1=Enable PCLK control mode.</td></tr> <tr> <td style="text-align: center;">[3]</td><td>1=Enable Memory Sleep Sequencing. When enabled, modify clock sequencing to delay clock gating until memory is in sleep state.</td></tr> <tr> <td style="text-align: center;">[4]</td><td>1=Enable Stop CPU mode. When enabled, assert stop to CPU rather than gating its clock</td></tr> <tr> <td style="text-align: center;">[5]</td><td>1=Enable firmware clock control to start firmware after PCI reset is released</td></tr> <tr> <td style="text-align: center;">[7:6]</td><td>Reserved.</td></tr> </tbody> </table> <p>When programming bit[4] to 1, bit[3] should be programmed to 0 at the same time.</p>	<u>Bit</u>	<u>Definition</u>	[0]	1=Enable power control mode.	[1]	1=Enable SuperSpeed remote wake mode.	[2]	1=Enable PCLK control mode.	[3]	1=Enable Memory Sleep Sequencing. When enabled, modify clock sequencing to delay clock gating until memory is in sleep state.	[4]	1=Enable Stop CPU mode. When enabled, assert stop to CPU rather than gating its clock	[5]	1=Enable firmware clock control to start firmware after PCI reset is released	[7:6]	Reserved.
<u>Bit</u>	<u>Definition</u>																
[0]	1=Enable power control mode.																
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[5]	1=Enable firmware clock control to start firmware after PCI reset is released																
[7:6]	Reserved.																
7:3	Reserved.																
1	<p>XhcCpuMemSlpDis: Non-CPU Memory Sleep Disable. Read-write. Reset: 0. Controls whether the sleep feature is disabled on xHCI Non-CPU internal SRAMs. 0=Do not disable sleep. 1=Disable sleep. When programming this bit and bit XhcCpuMemSlpDis, it is invalid to program XhcCpuMemSlpDis=1 and XhcNCpuMemSlpDis=0.</p>																
0	<p>XhcCpuMemSlpDis: CPU Memory Sleep Disable. Read-write. Reset: 0. Controls whether the sleep feature is disabled on xHCI Embedded CPU internal SRAMs. 0=Do not disable sleep. 1=Disable sleep.</p>																

XHCI_PMx14 PLL Control

Bits	Description
1	U2ShutdnPllEn: U2 Shutdown SSPHY PLL Enable. Read-write. Reset: 0. Controls shutdown SSPHY PLL Enable when LTSSM is in U2 state. 1=Enable. 0=Disable.
0	P3ShutdnPllEn: P3 Shutdown SSPHY PLL Enable. Read-write. Reset: 0. Controls shutdown SSPHY PLL Enable when SSPHY is in P3 state. 1=Enable. 0=Disable.

XHCI_PMx20 USB2.0 Wake Control

Bits	Description
25:24	SysBW: System Bandwidth. Read-write. Reset: 0. BIOS: 1. This field is used to provide information to the controller about the available system bandwidth.
23:22	U2SE1DisconMode: xHC USB2 Interface SE1 Disconnect Mode. Read-write. Reset: 1. 0=Take SE1 > 2.5us as a disconnect. 1=Do not take SE1 as a disconnect.

XHCI_PMx30 xHCI 1.0 Enable

Bits	Description
15	HCIVersion10En. Read-write. Reset: 0. BIOS: 1. Controls the host controller interface version number reported in XHCI_CAPx02 . 0=HCI Version is 0096h. 1=HCI Version is 0100h.

14	MSEFrameIdEn: Missed Server Error Frame ID Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable a clarification in xHCI 1.0 specifying the conditions under which a Missed Service Error should be detected based on Frame ID. 0=Disable.
11	SoftRetryEn: Soft Retry Enable. Read-write. Reset: 0. BIOS: 1. 0=Do not support soft retry. 1=Support soft retry.
10	SkipMsLocEvtEn: Skip Missed Service IOC Event Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable the parsing of TRBs during re-sync of an ISO pipe following detection of a Missed Service Error. 0=Disable. Always enable this bit when SkipTrbLocEvtEn==1.
9	EpStateUpdateChangeEn: EPState Update Change Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable a clarification in xHCI 1.0 specifying that when an endpoint transitions from Stopped to Running due to a doorbell ring, the EP State shall be updated to Running before any Transfer Events are generated. 0=Disable.
8	CASEn: Cold Attach Status Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable the xHCI 1.0 feature Cold Attach Status flag. 0=Disable.
7	SbdCapObsolete: SBD Reporting Capability Obsolete. Read-write. Reset: 0. BIOS: 1. 1=Enable xHCI 1.0 feature which makes Secondary Bandwidth Domain Reporting mandatory. 0=Disable.
6	SkipTrbLocEvtEn: Skip TRB IOC Event Enable. Read-write. Reset: 0. BIOS: 1. 1=Enable xHCI 1.0 features related to the parsing of TRBs and generation of events while skipping over TRBs due to errors and short packets. 0=Disable.
5	Reserved.
3	SwLpmEn: Software LPM Enable. Read-write. Reset: 0. IF (RevA0) THEN BIOS: 0. ELSE BIOS: 1. ENDIF. 0=Disable software controlled LPM feature. 1=Enable software controlled LPM feature.
2	FseEn: FSE Enable. Read-write. Reset: 0. BIOS: 1. 0=Disable FSE feature. 1=Enable FSE feature.
1	IntBlockEn: Interrupt Blocking Enable. Read-write. Reset: 0. BIOS: 1. 0=Disable interrupt blocking. 1=Enable interrupt blocking.
0	Xhci10En: xHCI 10 Enable. Read-write. Reset: 0. Global enable bit for xHCI 1.0 features. All xHCI 1.0 features may be enabled by setting this bit, or can be individually enabled by setting the individual feature enables. 1=Enable all xHCI 1.0 features.

XHCI_PMx48 SSPHY ACPI Indirect Index

Bits	Description
31:8	Reserved.
7:2	IndirectIndex: Indirect Index. Read-write. Reset: 00h. Specifies the SSPHY ACPI indirect register offset[7:2]. Accesses to all the indirect registers are doubleword-aligned. See 3.27.4.3.3.1 [xHCI SSPHY 60MHz ACPI Indirect Space] .
1:0	Reserved.

XHCI_PMx4C SSPHY ACPI IndirectData

Bits	Description
31:0	IndirectData: Indirect Data. Read-write. Reset: 0000_0000h. Specifies the data read from or written to the SSPHY ACPI indirect register pointed by XHCI_PMx48 . See 3.27.4.3.3.1 [xHCI SSPHY 60MHz ACPI Indirect Space] .

XHCI_PMx8C SSPHY Common Control 0

Bits	Description
24	CrPllCalibEn. Read-write. Reset: 0h. BIOS: See 2.15.2.9 . 1=Auto calibration is enabled; use calibrated value as the VCO setting. 0=Auto calibration is disabled; Use CP_PLL_VCO_TUNE[3:0] as the VCO setting if auto calibration has never been enabled; Use previously calibrated value as the VCO setting if auto calibration has been enabled once.
19:16	PllVcoTune[3:0]. Read-write. Reset: 0h. BIOS: See 2.15.2.9 . Specifies PLL VCO range initial setting (in Thermometer code). Valid settings are 0000b, 0001b, 0011b, 0111b, and 1111b. Programming invalid values may result in unpredictable behavior.

XHCI_PMxA0 SPI BAR0

Bits	Description
31:16	XhcSpiDataType0Size. Read-write. Reset: 0. Type 0 data size.
15:0	XhcSpiDataType0Addr. Read-write. Reset: 0. Type0 data ROM address.

XHCI_PMxA4 SPI BAR1

Bits	Description
31:16	XhcSpiDataType1Size. Read-write. Reset: 0. Type 1 data size.
15:0	XhcSpiDataType1Addr. Read-write. Reset: 0. Type 1 data ROM address.

XHCI_PMxA8 SPI BAR2

Bits	Description
31:16	XhcSpiDataType2Size. Read-write. Reset: 0. Type 2 data size.
15:0	XhcSpiDataType2Addr. Read-write. Reset: 0. Type 2 data ROM address.

XHCI_PMxAC SPI BAR3

Bits	Description
31:16	XhcSpiDataType3Size. Read-write. Reset: 0. Type 3 data size.
15:0	XhcSpiDataType3Addr. Read-write. Reset: 0. Type 3 data ROM address.

XHCI_PMxB0 SPI Valid Base

Bits	Description
31:26	SpiBase3. Read-write. Reset: 0. Specifies the offset in SPI data block of type 3 data.
25	Reserved.
24	SpiBar3Vld: SPI BAR3 Valid. Read-write. Reset: 0. 1=SPI_BAR4 register is valid.

23:18	SpiBase2 . Read-write. Reset: 0. Specifies the offset in SPI data block of type 2 data.
17	Reserved.
16	SpiBar2Vld: SPI BAR2 Valid . Read-write. Reset: 0. 1=SPI_BAR2 register is valid.
15:10	SpiBase1 . Read-write. Reset: 0. Specifies the offset in SPI data block of type 1 data.
9	Reserved.
8	SpiBar1Vld: SPI BAR1 Valid . Read-write. Reset: 0. 1=SPI_BAR1 register is valid.
7:2	SpiBase0 . Read-write. Reset: 0. Specifies the offset in SPI data block of type 0 data.
1	Reserved.
0	SpiBar0Vld: SPI BAR0 Valid . Read-write. Reset: 0. 1=SPI_BAR0 register is valid.

XHCI_PMxB4 SPI Misc

Bits	Description
15:0	XhcSpiFwId: SPI Firmware ID . Read-write. Reset: 0. Firmware Version ID. This value will be loaded into CCUMODE2[15:0] after synchronous reset if XHCI_PMx00[FwLoadMode]=1 .

XHCI_PMx[FC:C0] SPI Data Block N

Bits	Description
31:0	XhcSpiDataBlock . Read-write. Reset: 0. SPI Data Block.

3.26.5 HD Audio Controller

3.26.5.1 Device 14h Function 2 (Audio Controller) Configuration Registers

D14F2x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: device ID. Read-only. Reset: 780Dh.
15:0	VendorID: vendor ID. Read-only. Reset: 1022h.

D14F2x04 Status/Command

Reset: 0010_0000h.

Bits	Description
31:30	Reserved.
29	ReceivedMasterAbort: received master abort. Read; write-1-to-clear. 1=A completion with an unsupported request completion status was received.
28:21	Reserved.
20	CapList: capability list. Read-only. 1=capability list supported.
19	IntStatus: interrupt status. Read-only; updated-by-hardware. 1=INTx interrupt message pending. This bit is not set by MSI
18:11	Reserved.
10	IntDis: interrupt disable. Read-write. 1=INTx interrupt messages generation disabled. This bit does not affect the generation of MSI.
9:3	Reserved.
2	BusMasterEn: bus master enable. Read-write. 1=Memory read and write request generation enabled.
1	MemAccessEn: IO access enable. Read-write. This bit controls if memory accesses targeting this device are accepted. 1=Enabled. 0=Disabled.
0	Reserved.

D14F2x08 Class Code/Revision ID

Bits	Description
31:24	BaseClassCode. Read-only. Reset: 04h.
23:16	SubClassCode. Read-only. Reset: 03h.
15:8	ProgramInterface. Read-only. Reset: 00h.
7:0	RevID: revision ID. Read-only. Reset: 03h.

D14F2x0C Header Type

Bits	Description
31:24	BIST. Value: 0.
23:16	HeaderTypeReg. Value: 0.
15:8	LatencyTimer. Value: 0.
7:0	CacheLineSize. Read-write. Reset: 0. This field specifies the system cache line size in units of double words. This field is implemented as a read-write field for legacy compatibility purposes only and has no functional impact.

D14F2x10 Lower Base Address Register

Reset: 0000_0004h.

Bits	Description
31:14	HDABaseAddr[31:14]: low base address. Read-write. Lower Base Address for the HD Audio controller's memory mapped configuration registers. 16K bytes are requested by hardwiring bits [13:4] to 0.
13:4	Reserved.
3	Pref: prefetchable. Read-only. 0=Non-prefetchable memory region.
2:1	Type: base address register type. Read-only. 10b=64 bit base address register. BAR can be located anywhere in 64-bit address space.
0	MemSpace: memory space type. Read-only. 0=Memory mapped base address.

D14F2x14 Upper Base Address Register

Reset: 0000_0000h.

Bits	Description
31:0	HDABaseAddr[63:32]: Upper Base Address. Read-write. Upper Base Address for the HD Audio controller's memory mapped configuration registers.

D14F2x2C Subsystem and Subvendor ID

Reset: 0000_0000h.

Bits	Description
31:16	SubsystemID. Write-once.
15:0	SubsystemVendorID. Write-once.

D14F2x34 Capabilities Pointer

Reset: 0000_0050h.

Bits	Description
31:8	Reserved.
7:0	CapPtr: capabilities pointer. Read-only. Pointer to PM capability.

D14F2x3C Interrupt Line

Reset: 0000_0100h.

Bits	Description
31:24	MaximumLatency. Read-only.
23:16	MinimumGrant. Read-only.
15:12	Reserved.
11:8	InterruptPin: interrupt pin. Read-only. This register reflects the value programs into Interrupt Control Pin register D14F2x44[InterruptPinControl] .
7:0	InterruptLine: interrupt line. Read-write. This field contains the interrupt line routing information. This is not used by the HD Audio controller.

D14F2x40 Misc Control

Read-write. Reset: 0000_0000h.

Bits	Description
31:23	Reserved.
22	EnableStopALinkClock. 1=Enable stop A-Link clock indication. 0=Disable.
21	EnableClockGating. 1=Enable clock gating. 0=Disable.
20	DisableMinimumRetry. 1=Disable minimum retry on ALINK Bus. 0=Enable. When enabled, after the first request of a transaction, it will not generate another request for the same transaction unless notified by AB the data is available.
19	Reserved.
18	EnableNoSnoopRequest. 1=Enable No Snoop request to ACPI. 0=Disable. No snoop request to ACPI When enabled and the DMA cycle is No Snoop, ACPI will not generate a wake to CPU in C2 state.
17	DisableNoSnoopOverride. 1=DisableNoSnoop controlling the No Snoop attribute. 0=Override DisableNoSnoop setting and always generate No Snoop attribute on Buffer Descriptor and Data Buffer DMA.

16	DisableNoSnoop. 1=No Snoop attribute is disabled on Buffer Descriptor and Data Buffer DMA. 0=Set the No Snoop attribute on Buffer Descriptor and Data Buffer DMA when the Traffic Priority bit is set in the Stream Descriptor.										
15:9	Reserved.										
8	StaticOutputFIFOSizeEnable. 1=Enable Static Output FIFO Size. 0=Output FIFO Size is set dynamically set based on Stream Format.										
7:2	Reserved.										
1:0	StaticOutputFIFOSizeSelect. Static Output FIFO Size is functional only when (D14F2x40[StaticOutputFIFOSizeEnable]==1). <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1/8 of the maximum Output FIFO Size.</td> </tr> <tr> <td>01b</td> <td>1/4 of the maximum Output FIFO size.</td> </tr> <tr> <td>10b</td> <td>1/2 of the maximum Output FIFO Size.</td> </tr> <tr> <td>11b</td> <td>Use the maximum Output FIFO Size</td> </tr> </tbody> </table>	Bits	Definition	00b	1/8 of the maximum Output FIFO Size.	01b	1/4 of the maximum Output FIFO size.	10b	1/2 of the maximum Output FIFO Size.	11b	Use the maximum Output FIFO Size
Bits	Definition										
00b	1/8 of the maximum Output FIFO Size.										
01b	1/4 of the maximum Output FIFO size.										
10b	1/2 of the maximum Output FIFO Size.										
11b	Use the maximum Output FIFO Size										

D14F2x44 Interrupt Pin/Capability/Debug Control

Reset: 0000_0001h.

Bits	Description
15:11	Reserved.
10	IF (RevA0) THEN Reserved. ELSE BClkOnInD3. Read-write. Reset: 0. 1=Do not turn off AZ_BCLK in D3. ENDIF.
9	EnAFCap. Read-write. BIOS: 0. 1=Enable Advanced Features Capability. See Table 81 .
8	EnMsiCap. Read-write. BIOS: 1. 1=Enable MSI Capability. See Table 81 .
7:4	Reserved.
3:0	InterruptPinControl. Read-write. Controls the value reports in D14F2x3C[InterruptPin] .

D14F2x50 Power Management Capability

Bits	Description
31:27	PmeSupport. Value: 11001b. Indicates PME# can be generated from D0 and D3 states.
26	D2Support: D2 support. Value: 0. Indicates that D2 is not supported in hardware.
25	D1Support: D1 support. Value: 0. Indicates that D1 is not supported in hardware.
24:22	AuxCurrent: auxiliary current. Value: 001b. Indicates 55mA maximum suspend well current is required in the D3cold state.

21	DevSpecificInit: device specific initialization. Value: 0. Indicates that there is no device specific initialization necessary.
20	Reserved.
19	PmeClock. Value: 0. Indicates that no PCI clock is required for the function to generate PME#.
18:16	Version: version. Value: 010b. Indicates this function complies with Revision 1.1 of the PCI Power Management Interface Specification
15:8	NextPtr: next pointer. IF (D14F2x44[EnAFCap] && D14F2x44[EnMsiCap]) THEN Value: 60h. ELSEIF (D14F2x44[EnAFCap]) THEN Value: 70h. ELSEIF (D14F2x44[EnMsiCap]) THEN Value: 60h. ELSE Value: 00h. ENDIF. Specifies the address of the next capability structure, or zero if this is the end of the linked list of capability structures. See Table 81 .
7:0	CapID: capability ID. Value: 01h. Indicates that the capability structure is a PCI power management data structure.

D14F2x54 Power Management Control and Status

Bits	Description												
31:16	Reserved.												
15	PmeStatus: PME status. Read; set-by-hardware; write-1-to-clear. Cold reset: 0. This bit set when the HD Audio controller asserts the PME# signal, and is independent of the PME Enable bit.												
14:9	Reserved.												
8	PmeEn: PME# enable. Read-write. Cold reset: 0. Enables the function to assert PME#.												
7:2	Reserved.												
1:0	PowerState: power state. Read-write. Reset: 0. Specifies the current power state of the root port and sets the root port into a new power state. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>D0</td> <td>10b</td> <td>Reserved.</td> </tr> <tr> <td>01b</td> <td>Reserved</td> <td>11b</td> <td>D3hot</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	D0	10b	Reserved.	01b	Reserved	11b	D3hot
Bits	Definition	Bits	Definition										
00b	D0	10b	Reserved.										
01b	Reserved	11b	D3hot										

D14F2x60 MSI Capability

Bits	Description
31:24	Reserved.
23	Msi64bit: MSI 64 bit capability. Read-only. Reset: 1. 1=The device is capable of sending 64-bit MSI messages.
22:20	MsiMultiEn: MSI multiple message enable. Read-write. Reset: 000b. Software writes to this field to indicate the number of allocated vectors (equal to or less than the number of requested vectors). When MSI is enabled, a function is allocated at least 1 vector.
19:17	MsiMultiCap: MSI multiple message capability. Read-only. Reset: 000b. 000b=The device is requesting one vector.
16	MsiEn: MSI enable. Read-write. Reset: 0. 1=MSI generation is enabled and INTx generation is disabled. 0=MSI generation disabled and INTx generation is enabled.

15:8	NextPtr: next pointer. IF (D14F2x44[EnAFCap]) THEN Value: 70h. ELSE Value: 00h. ENDIF. Specifies the address of the next capability structure, or zero if this is the end of the linked list of capability structures. See Table 81 .
7:0	CapID: capability ID. IF (D14F2x44[EnMsiCap]==1) THEN Value: 05h. ELSE Value: 00h. ENDIF. 05h=MSI capability structure. See Table 81 .

D14F2x64 MSI Message Address Low

Reset: 0000_0000h.

Bits	Description
31:2	MsiMsgAddrLo: MSI message address. Read-write. This register specifies the doubleword aligned address for the MSI memory write transaction.
1:0	Reserved.

D14F2x68 MSI Message Address High

Reset: 0000_0000h.

Bits	Description
31:8	Reserved.
7:0	MsiMsgAddrHi: MSI message address. Read-write. This register specifies the upper 8 bits of the MSI address in 64-bit MSI mode.

D14F2x6C MSI Message Data

Reset: 0000_0000h.

Bits	Description
31:16	Reserved.
15:0	MsiData: MSI message data. Read-write. This register specifies lower 16 bits of data for the MSI memory write transaction. The upper 16 bits are always 0.

D14F2x70 Advanced Features Capability

Bits	Description
31:26	Reserved.
25	TPCapabilities. Read-only. IF (D14F2x44[EnAFCap]==1) THEN Reset: 1. ELSE Reset: 0. ENDIF. 1=Support for Transactions Pending. See Table 81 .
24	FLRCapabilities. Read-only. IF (D14F2x44[EnAFCap]==1) THEN Reset: 1. ELSE Reset: 0. ENDIF. 1=Support for Function Level Reset (FLR). See Table 81 .
23:16	AFLength. Read-only. IF (D14F2x44[EnAFCap]==1) THEN Reset: 06h. ELSE Reset: 00h. ENDIF. Indicates AF Structure Length (bytes). See Table 81 .

15:8	NextPtr: next pointer. Read-only. Reset: 00h. 00h=This the end of the linked list of capability structures. See Table 81 .
7:0	AFCapID: capability ID. Read-only. IF (D14F2x44[EnAFCap]==1) THEN Reset: 13h. ELSE Reset: 00h. ENDIF. 13h=Indicates Advanced Features Capability. See Table 81 .

D14F2x74 Advanced Features Control and Status

Bits	Description
31:9	Reserved.
8	TransactionPending. Read-only; updated-by-hardware. Reset: 0. 1=Indicates that the function has issued one or more non-posted transactions which have not been completed including non-posted transactions that a target has terminated with retry. 0=Indicates that all non-posted transactions have been completed.
7:1	Reserved.
0	InitiateFLR. RAZ; write-1-only; cleared-when-done. Reset: 0. A write of 1 initiates Function Level Reset. FLR requirements are defined in the PCI Express Base Specification. Registers and state information that do not apply to conventional PCI are exempt from the FLR requirements given there.

3.26.6 Secure Digital (SD) Controller

3.26.6.1 Device 14h Function 7 Configuration Registers (SD)

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D14F7x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: Device ID. Value: 7813h.
15:0	VendorID: Vendor ID. Value: 1022h. Specifies a unique 16-bit value assigned to a vendor.

D14F7x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; updated-by-hardware; write-1-to-clear. Reset: 0. 1=The FCH detects a parity error.
30	SignaledSystemError: Signaled System Error. Read; updated-by-hardware; write-1-to-clear. Reset: 0. SERR# status. 1=The FCH detects a PCI address parity error.
29	ReceivedMasterAbort: Received Master Abort. Read; updated-by-hardware; write-1-to-clear. Reset: 0. 1=The FCH acts as a PCI master and aborts a PCI bus memory cycle.
28	ReceivedTargetAbort: Received Target Abort. Read; updated-by-hardware; write-1-to-clear. Reset: 0. 1=FCH received Target Abort from a PCI target.
27	SignaledTargetAbort: Signaled Target Abort. Read; updated-by-hardware; write-1-to-clear. Reset: 0. 1=The FCH signaled Target Abort while acting as Bus Master.
26:25	DeviceSelectTiming: Device Select Timing. Value: 01b. 01b=DEVSEL# Medium timing when performing a positive decode.
24	MasterDataParityError: Master Data Parity Error. Read; updated-by-hardware; write-1-to-clear. Reset: 0. Data Parity reported. 1=The FCH detects PERR# asserted while acting as PCI master.
23:21	Reserved.
20	CapabilitiesList: Capabilities List. IF ((D14F7xB0[CapMsiEn]==1) (D14F7xB0[CapPmcEn]==1)) THEN Value: 1. ELSE Value: 0. ENDIF.
19:10	Reserved.
9	FastBack2BackEnable: Fast Back-to-Back Enable. Value: 0.
8	SERREnable: SERR# Enable. Read-write. Reset: 0. 1=FCH asserts SERR# when it detects an address parity error.
7	SteppingControl: Stepping Control. Value: 0. 1=Wait Cycle enable.
6	ParityErrorResponse: Parity Error Response. Read-write. Reset: 0. PERR# (Response) detection enable bit. 1=The FCH asserts PERR# when it is the agent receiving data and it detects a parity error. 0=PERR# is not asserted.
5	VGAPaletteSnoop: VGA Palette Snoop. Value: 0. 1=VGA Palette Snoop Enable.
4	MemoryWriteandInvalidateEnable: Memory Write and Invalidate Enable. Value: 0. 1=Memory write and invalidate enable.

3	SpecialCycles: Special Cycles. Value: 0. 1=Special cycle recognition enable.
2	BusMaster: Bus Master. Read-write. Reset: 0. 1=Bus master function enable.
1	MemorySpace: Memory Space. Read-write. Reset: 0. 1=Enable memory access. 0=Disable.
0	IOSpace: IO Space. Value: 0. 1=IO access enable.

D14F7x08 Revision ID/Class Code

Bits	Description										
31:24	ClassCode: Class Code. IF (D14F7xB0[BackdoorClassCode]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 8h. Basic Class.										
23:16	SubClass: Sub Class. Read-only. Reset: 5h. For SD host controller										
15:8	InterfaceCode: Interface Code. Value: 1. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Standard host not supporting DMA</td> </tr> <tr> <td>01h</td> <td>Standard host supporting DMA</td> </tr> <tr> <td>02h</td> <td>Vendor unique SD host controller</td> </tr> <tr> <td>FFh-03h</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	00h	Standard host not supporting DMA	01h	Standard host supporting DMA	02h	Vendor unique SD host controller	FFh-03h	Reserved
Bits	Definition										
00h	Standard host not supporting DMA										
01h	Standard host supporting DMA										
02h	Vendor unique SD host controller										
FFh-03h	Reserved										
7:0	RevisionID: Revision ID. Value: 01h.										

D14F7x0C Cache Line Size

Bits	Description
31:24	Bist. Read-only. Reset: 0. No BIST modes.
23:16	HeaderType: Header Type. Read-only. Reset: 80h. Specifies the type of the predefined header in the configuration space.
15:8	LatencyTimer: Latency Timer. Read-only. Reset: 0. Specifies the value of the Latency Timer in units of PCICLKs.
7:0	CacheLineSize: Cache Line Size. Read-only. Reset: 0.

D14F7x10 Base Address Reg 0

Bits	Description
31:8	BaseAddress0: Base Address 0. Read-write. Reset: 0h. Specifies base address 0[31:8].
7:4	Reserved.
3	Prefetchable. Value: 0. 0=Non-prefetchable.
2:1	Type. IF (D14F7xB0[BAddr64En]==0) THEN Value: 00b. ELSE Value: 10b. ENDIF. 00b=32-bit base address. 10b=64-bit base address.
0	SpaceIndicator: Space Indicator. Value: 0. 0=Memory-mapped base address.

D14F7x14 Upper Base Address Reg 0

Bits	Description
31:0	BaseAddress0Upper: Base Address 0 Upper. IF (D14F7xB0[BAddr64En]==0) THEN RAZ. ELSE Read-write. ENDIF. Reset: 0. Specifies base address 0[63:32].

D14F7x2C Subsystem ID and Subsystem Vendor ID

Write-once. This 4-byte register is a write-once & read-only afterward register. The BIOS writes this register once (all 4 bytes at once) and software reads its value (when needed).

Bits	Description
31:16	SubsystemID: Subsystem ID. Reset: 7813h. Subsystem ID.
15:0	SubsystemVendorID: Subsystem Vendor ID. Reset: 1022h. Subsystem Vendor ID.

D14F7x34 Capabilities Pointer

Bits	Description
31:8	Reserved.
7:0	CapabilitiesPointer: Capabilities Pointer.

D14F7x3C Interrupt Line

Bits	Description
31:16	Reserved.
15:8	InterruptPin: Interrupt Pin. IF (D14F7xB0[BackdoorIntPin]) THEN Read-write. ELSE Read-only. ENDIF. Reset: 1. Interrupt pin.
7:0	InterruptLine: Interrupt Line. Read-write. Reset: 0. Interrupt line.

D14F7x40 Slot Information

Bits	Description
31:7	Reserved.
6:4	NumberOfSlots: Number of Slots. Read-write. Reset: 0. Number of slots supported. These bits indicate the number of slots the Host Controller supports. In the case of a single function, a maximum of 6 slots can be assigned.

Bits	Definition	Bits	Definition
000b	1 slot	100b	5 slots
001b	2 slots	101b	6 slots
010b	3 slots	110b	Reserved
011b	4 slots	111b	Reserved

3	Reserved.																				
2:0	<p>FirstBaseAddressRegisterNumber: First Base Address Register Number. Read-write. Reset: 0. Up to 6 base addresses can be specified in single configuration. These bits indicate the first base address register number assigned to SD Host Controller register set. In the case of single function and multiple register sets, contiguous base addresses are used. D14F7x40[NumberOfSlots] specifies the number of base addresses.</p> <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Base Address 10h (BAR0)</td> <td>100b</td> <td>Base Address 20h (BAR4)</td> </tr> <tr> <td>001b</td> <td>Base Address 14h (BAR1)</td> <td>101b</td> <td>Base Address 24h (BAR5)</td> </tr> <tr> <td>010b</td> <td>Base Address 18h (BAR2)</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>Base Address 1Ch (BAR3)</td> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	000b	Base Address 10h (BAR0)	100b	Base Address 20h (BAR4)	001b	Base Address 14h (BAR1)	101b	Base Address 24h (BAR5)	010b	Base Address 18h (BAR2)	110b	Reserved	011b	Base Address 1Ch (BAR3)	111b	Reserved
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>																		
000b	Base Address 10h (BAR0)	100b	Base Address 20h (BAR4)																		
001b	Base Address 14h (BAR1)	101b	Base Address 24h (BAR5)																		
010b	Base Address 18h (BAR2)	110b	Reserved																		
011b	Base Address 1Ch (BAR3)	111b	Reserved																		

D14F7x80 SD PCI MSI Capability Header

Bits	Description
31:24	Reserved. MsiCtrlReserved.
23	ExtendAddrEn. IF (D14F7xB0[Msi64En]) THEN Value: 1. ELSE Value: 0. ENDIF. 64-bit Address Capable.
22:20	MulMsgEn. Read-write. Reset: 0. Multiple Message Enable.
19:17	MulMsgCap. Read-only. Reset: 0. Multiple Message Capable.
16	MsiEnable. Read-write. Reset: 0. MSI Enable.
15:8	CapNxtPtr. IF (D14F7xB0[CapMsiEn]==1 && D14F7xB0[CapPmcEn] ==1) THEN Value: 90h. ELSE Value: 0. ENDIF. Reset: 0.
7:0	CapId. Read-only. Reset: 5h. A value of 05h indicates MSI.

D14F7x84 SD PCI MSI Address

Bits	Description
31:2	MsgAddr. Read-write. Reset: 0. Specifies Message Address[31:2].
1:0	Reserved. MsiAddrReserved.

D14F7x88 SD PCI MSI Upper Address

Bits	Description
31:0	MsgUpperAddr. Read-write. Reset: 0. Specifies Message Upper Address[63:32]. Bits [15:0] of this register will be MSI_DATA if 32 bit MSI is selected.

D14F7x8C SD PCI MSI Data

Bits	Description
31:16	Reserved.
15:0	MsgData. Read-write. Reset: 0. Message Data.

D14F7x90 Power Management Capability Header

Bits	Description												
31:27	PMESupport: PME Support. Read-only. Reset: 0. This 5-bit field indicates the power states in which the function may assert PME#. A value of 0b for any bit indicates that the function is not capable of asserting the PME# signal while in that power state. <table> <thead> <tr> <th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>xxxx1b</td><td>PME# can be asserted from D0</td></tr> <tr> <td>xxx1xb</td><td>PME# can be asserted from D1</td></tr> <tr> <td>xx1xxb</td><td>PME# can be asserted from D2</td></tr> <tr> <td>x1xxxb</td><td>PME# can be asserted from D3hot</td></tr> <tr> <td>1xxxxb</td><td>PME# can be asserted from D3cold</td></tr> </tbody> </table>	Bits	Definition	xxxx1b	PME# can be asserted from D0	xxx1xb	PME# can be asserted from D1	xx1xxb	PME# can be asserted from D2	x1xxxb	PME# can be asserted from D3hot	1xxxxb	PME# can be asserted from D3cold
Bits	Definition												
xxxx1b	PME# can be asserted from D0												
xxx1xb	PME# can be asserted from D1												
xx1xxb	PME# can be asserted from D2												
x1xxxb	PME# can be asserted from D3hot												
1xxxxb	PME# can be asserted from D3cold												
26	D2Support: D2 Support. Read-only. Reset: 0. 1=This function supports the D2 Power Management State.												
25	D1Support: D1 Support. Read-only. Reset: 0. 1=This function supports the D1 Power Management State.												
24:22	AuxCurrent: Aux Current. Read-only. Reset: 0. This 3 bit field reports the 3.3V auxiliary current requirements for the PCI function.												
21	Dsi. Read-only. Reset: 0. The Device Specific Initialization required. 1=Indicates special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it.												
20	Reserved.												
19	PmeClock: PME Clock. Value: 0. PME Clock. 0=Indicates that no PCI clock is required for the function to generate PME#. 1=Indicates that the function relies on the presence of the PCI clock for PME# operation.												
18:16	Version. Value: 011b. 011b=Indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.												
15:8	CAPNextPointer: CAP Next Pointer. Read-only. Reset: 0. No other capability.												
7:0	CAPID: CAP ID. Read-only. Reset: 1. Power management.												

D14F7x94 Power Management Control and Status Register

Bits	Description
31:24	Data. Read-only. Reset: 0. Reports the state dependent data requested by the DataSelect field. The value of this register is scaled by the value reported by the DataScale field.
23	BPCCEn: Bus Power/Clock Control Enable. Read-only. Reset: 0. Bus Power/Clock Control Enable.
22	B2B3: B2 B3#. Read-only. Reset: 0. B2/B3 support for D3hot.
21:16	Reserved.
15	PMEStatus: PME Status. Read-only; updated-by-hardware. Reset: 0. Set when the function normally asserts the PME# signal independent of the state of PMEEn.
14:13	DataScale: Data Scale. Read-only. Reset: 0. Indicates the scaling factor to be used when interpreting the value of the Data register. The value and meaning of this field will vary depending on which data value has been selected by the DataSelect field.

12:9	DataSelect: Data Select. Read-only. Reset: 0. Selects which data is to be reported through the Data register and DataScale field.												
8	PMEEn: PME En. Read-only. Reset: 0. 1=Enable the function to assert PME#. 0=PME# assertion is disabled.												
7:4	Reserved.												
3	NoSoftReset: No Soft Reset. Read-only. Reset: 0. 1=Indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset.												
2	Reserved.												
1:0	Power. Read-only. Reset: 0. Determines the current power state of a function and to set the function into a new power state. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>D0</td> <td>10b</td> <td>D2</td> </tr> <tr> <td>01b</td> <td>D1</td> <td>11b</td> <td>D3hot</td> </tr> </table> If software attempts to write an unsupported, optional state to this field, the write operation must complete normally on the bus; however, the data is discarded and no state change occurs.	Bits	Definition	Bits	Definition	00b	D0	10b	D2	01b	D1	11b	D3hot
Bits	Definition	Bits	Definition										
00b	D0	10b	D2										
01b	D1	11b	D3hot										

3.26.6.2 SD Host Controller Configuration Registers (SDHC)

The registers are accessed directly mapped by [D14F7x10 \[Base Address Reg 0\]](#) and [D14F7x14 \[Upper Base Address Reg 0\]](#). For full details refer to the *SD Specification Part A2 SD Host Controller Standard Specification Version 3.00*.

SDHCx00 SDHC System Address / Argument 2

Bits	Description
31:16	SysAddr1. Read-write. Reset: 0. System Address upper bits. Updating this register clears DMA_WAIT. It indicates system memory address for DMA. When DMA transfer detects the DMA Buffer Boundary specified by the Host DMA Buffer Boundary in the Block Size register, SD controller asserts DMA_WAIT. Also SD controller generates DMA interrupt at this time when corresponding bits in the Normal Interrupt Status Enable register and Normal Interrupt Signal Enable register are set. While ADMA is enabled, this register will not be used.
15:0	SysAddr0. Read-write. Reset: 0. System Address lower bits. Updating this register clears DMA_WAIT.

SDHCx04 SDHC Block CS

Block Size and Block Count.

Bits	Description
31:16	BlkCnt. Read-write. Reset: 0. Block Count. It indicates block count of multiple data transfer. It is enabled when the Block Count Enable bit (D01) in the Transfer Mode register is set to 1. It is decremented after each block data transmission. During infinite data transmission, setting of this bit is meaningless.
15	Reserved.

14:12	DmaBufBndry. Read-write. Reset: 0. Host DMA Buffer Boundary. Indicates the contiguous buffer size in the system memory. When the boundary is reached, DMA interrupt will be generated.																				
	<table> <thead> <tr> <th>Bits</th><th><u>Definition</u></th><th>Bits</th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>4K bytes</td><td>100b</td><td>64K bytes</td></tr> <tr> <td>001b</td><td>8K bytes</td><td>101b</td><td>128K bytes</td></tr> <tr> <td>010b</td><td>16K bytes</td><td>110b</td><td>256K bytes</td></tr> <tr> <td>011b</td><td>32K bytes</td><td>111b</td><td>512K bytes</td></tr> </tbody> </table>	Bits	<u>Definition</u>	Bits	<u>Definition</u>	000b	4K bytes	100b	64K bytes	001b	8K bytes	101b	128K bytes	010b	16K bytes	110b	256K bytes	011b	32K bytes	111b	512K bytes
Bits	<u>Definition</u>	Bits	<u>Definition</u>																		
000b	4K bytes	100b	64K bytes																		
001b	8K bytes	101b	128K bytes																		
010b	16K bytes	110b	256K bytes																		
011b	32K bytes	111b	512K bytes																		
11:0	BlkSize. Read-write. Reset: 0. Transfer Data Length (max. block size is 2K bytes). When the CE-ATA Enable bit of the CE-ATA Control register is set, a value of 0x000 indicates block size of 4K bytes.																				

SDHCx08 SDHC Command Argument

Bits	Description
31:16	ARGUMENT1. Read-write. Reset: 0. Upper bits. Command Argument. Command arguments specified as bits [39:8] of the command format.
15:0	ARGUMENT0. Read-write. Reset: 0. Lower bits.

SDHCx0C SDHC Command/Transfer Mode

Bits	Description										
31:30	Reserved.										
29:24	CmdIdx. Read-write. Reset: 0. Command Index.										
23:22	CmdType. Read-write. Reset: 0. Command Type. <table> <thead> <tr> <th>Bits</th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>Normal.</td></tr> <tr> <td>01b</td><td>Suspend CMD52 for writing BR in CCCR.</td></tr> <tr> <td>10b</td><td>Resume CMD52 for writing Function Sel in CCCR.</td></tr> <tr> <td>11b</td><td>Abort CMD12 (SD Memory) or Abort CMD52 (SDIO).</td></tr> </tbody> </table>	Bits	<u>Definition</u>	00b	Normal.	01b	Suspend CMD52 for writing BR in CCCR.	10b	Resume CMD52 for writing Function Sel in CCCR.	11b	Abort CMD12 (SD Memory) or Abort CMD52 (SDIO).
Bits	<u>Definition</u>										
00b	Normal.										
01b	Suspend CMD52 for writing BR in CCCR.										
10b	Resume CMD52 for writing Function Sel in CCCR.										
11b	Abort CMD12 (SD Memory) or Abort CMD52 (SDIO).										
21	DataPrsnt. Read-write. Reset: 0. Data Present Select. Indicates data is present and will be transferred on the DAT line. When command is issued with this bit enabled, internal buffer will be cleared. 0=No data. 1=Data.										
20	CmdIdxChkEn. Read-write. Reset: 0. 1=Command Index Check Enable. 0=Disable.										
19	CrcChkEn. Read-write. Reset: 0. 1=Command CRC Check Enable. 0=Disable.										
18	Reserved.										
17:16	RespType. Read-write. Reset: 0. Response Type Select. <table> <thead> <tr> <th>Bits</th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>No Response.</td></tr> <tr> <td>01b</td><td>Response length is 136 bits.</td></tr> <tr> <td>10b</td><td>Response length is 48 bits without busy.</td></tr> <tr> <td>11b</td><td>Response length is 48 bits with busy.</td></tr> </tbody> </table>	Bits	<u>Definition</u>	00b	No Response.	01b	Response length is 136 bits.	10b	Response length is 48 bits without busy.	11b	Response length is 48 bits with busy.
Bits	<u>Definition</u>										
00b	No Response.										
01b	Response length is 136 bits.										
10b	Response length is 48 bits without busy.										
11b	Response length is 48 bits with busy.										
15:6	Reserved.										
5	MultiBlk. Read-write. Reset: 0. 1=Multiple/Single Block Select. 0=Single Block.										
4	DataDir. Read-write. Reset: 0. Data Transfer Direction. 0=Write. 1=Read.										

3:2	AutoCmdEn. Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b Auto Command Disabled 01b Auto CMD12 Enable 10b Auto CMD23 Enable 11b Reserved
1	BlkCntEn. Read-write. Reset: 0. 1=Block Count Enable.
0	DmaEn. Read-write. Reset: 0. 1=DMA Enable. 0=Disable.

SDHCx10 SDHC_RESP1_0

Bits	Description
31:16	RESPONSE1. Read-only. Reset: 0. R39-24 of response is saved in this register.
15:0	RESPONSE0. Read-only. Reset: 0. R23-8 of response is saved in this register.

SDHCx14 SDHC_RESP3_2

Bits	Description
31:16	RESPONSE3. Read-only. Reset: 0. R71-56 of response is saved in this register.
15:0	RESPONSE2. Read-only. Reset: 0. R55-40 of response is saved in this register.

SDHCx18 SDHC_RESP5_4

Bits	Description
31:16	RESPONSE5. Read-only. Reset: 0. R103-88 of response is saved in this register.
15:0	RESPONSE4. Read-only. Reset: 0. R87-72 of response is saved in this register.

SDHCx1C SDHC_RESP7_6

Bits	Description
31:16	RESPONSE7. Read-only. Reset: 0. R127-120 of response or R39-24 of Auto CMD12 response is saved in this register.
15:0	RESPONSE6. Read-only. Reset: 0. R119-104 of response or R23-8 of Auto CMD12 response is saved in this register.

SDHCx20 SDHC_BUFFER

Bits	Description
31:16	BuffData1. Read-write. Reset: 0. Upper bits. Data Buffer. Data will be accessed through this register. Data which exceeds the size designated by the Block Size register will not be written in the data buffer.
15:0	BuffData0. Read-write. Reset: 0. Lower bits.

SDHCx24 SDHC_PRSNT_STATE

Bits	Description
31:25	Reserved.
24	CmdLevel . Read-only. Reset: 0. CMD Line Signal Level. Reflects signal level of CMD line.
23:20	DatLevel . Read-only. Reset: 0. DAT Line Signal Level. Reflects signal level of DAT line.
19	WpLevel . Read-only. Reset: 0. Write Protect Switch Level. 0=Write protected. 1=Write enable.
18	CdLevel . Read-only. Reset: 0. Card Detect Pin Level. 0=No card present. 1=Card present.
17	CardStable . Read-only. Reset: 0. Card State Stable. Indicates Card Detect signal level is stable. 0=Not stable (debouncing or resetting). 1=Card stable.
16	CardIns . Read-only. Reset: 0. Card Inserted. 0=No card inserted or debouncing state or resetting. 1=Card inserted.
15:12	Reserved.
11	BufRdEn . Read-only. Reset: 0. Buffer Read Enable. Indicates buffer is ready for reading. 0=Read disable. 1=Read enable.
10	BufWrEn . Read-only. Reset: 0. Buffer Write Enable. Indicates buffer is ready for writing. 0=Write disable. 1=Write enable.
9	RdTxA . Read-only. Reset: 0. Read Transfer Active. Indicates occurrence of read data transfer. 0=No data transferring. 1=Read data transferring.
8	WrTxA . Read-only. Reset: 0. Write Transfer Active. Indicates occurrence of write data transfer. 0=No data transferring. 1=Write data transferring.
7:3	Reserved.
2	DatLineActive . Read-only. Reset: 0. DAT Line Active. Indicates DAT line on SD Bus is active. 0=DAT line inactive. 1=DAT line active.
1	CmdInhibDat . Read-only. Reset: 0. Command Inhibit (DAT). Indicates that commands which use also the DAT line can be issued. 0=Can issue commands which use DAT line. 1=Cannot issue any commands which use DAT line.
0	CmdInhibCmd . Read-only. Reset: 0. Command Inhibit (CMD). Indicates that commands which use only the CMD line can be issued. 0=Can issue commands which use CMD line. 1=Cannot issue any commands.

SDHCx28 SDHC_CTRL1

Bits	Description
31:27	Reserved.
26	SdRemWakeEn . Read-write. Reset: 0. 1=SD Card Removal Wake up. 0=Disable.
25	SdInsWakeEn . Read-write. Reset: 0. 1=SD Card Insertion Wake up. 0=Disable.
24	SdIntWakeEn . Read-write. Reset: 0. 1=SD Card Interrupt Wake up. 0=Disable.
23:20	Reserved.
19	BgIntEn . Read-write. Reset: 0. Interrupt at Block Gap. 1=Enable interrupt detection during 4-bit block transmission. 0=Disable.

18	ReadWaitEn. Read-write. Reset: 0. Read Wait Control. 1=Indicates Read Wait will be inserted when needed. 0=Disable.												
17	ContReq. Read-write. Reset: 0. Continue Request. Writing 1 to this bit triggers restart of halted data transaction with current register setting. Once this bit is 1, the internal buffer will be cleared and data transfer sequence will be restarted. 1=Restart.												
16	BgStopReq. Read-write. Reset: 0. Stop at Block Gap Request. Writing 1 to this bit triggers halting of current data transfer after next block gap. To use this request, the Read Wait function is necessary in read transaction. Even if the Auto CMD12 Enable bit is set to 1, Auto CMD12 is not issued in case this bit is set to 1. This bit is cleared by not only writing 0 to this bit, but also issuing abort commands. 0=Transfer. 1=Stop.												
15:12	Reserved.												
11:9	SdBusVoltage. Read-write. Reset: 0. SD Bus Voltage. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>100b-000b</td> <td>Reserved</td> <td>110b</td> <td>3.0 Volts</td> </tr> <tr> <td>101b</td> <td>1.8 Volts</td> <td>111b</td> <td>3.3 Volts</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	100b-000b	Reserved	110b	3.0 Volts	101b	1.8 Volts	111b	3.3 Volts
Bits	Definition	Bits	Definition										
100b-000b	Reserved	110b	3.0 Volts										
101b	1.8 Volts	111b	3.3 Volts										
8	SdBusEn. Read-write. Reset: 0. SD Bus Power. Automatically cleared when card is removed. 0=Off. 1=On.												
7	CdTestEn. Read-write. Reset: 0. Card Detect Signal Selection. 0=I/O pin. 1=SD_TEST_LEVEL.												
6	CdTestLevel. Read-write. Reset: 0. Card Detect Test Level. 0=Card removed. 1=Card inserted.												
5	MmcWidth. Read-write. Reset: 0. Extended Data Transfer Width (MMC). 0=Use width set by DAT_TX_WIDTH. 1=Force 8-bit.												
4:3	DmaSelect. Read-write. Reset: 0. DMA Select. Valid only when DMA is enabled. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>No DMA or SDMA selected</td> <td>10b</td> <td>32-bit ADMA2</td> </tr> <tr> <td>01b</td> <td>32-bit ADMA</td> <td>11b</td> <td>64-bit ADMA2</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	No DMA or SDMA selected	10b	32-bit ADMA2	01b	32-bit ADMA	11b	64-bit ADMA2
Bits	Definition	Bits	Definition										
00b	No DMA or SDMA selected	10b	32-bit ADMA2										
01b	32-bit ADMA	11b	64-bit ADMA2										
2	HighSpeedEn. Read-write. Reset: 0. High Speed Enable. When disabled, SD controller outputs commands and data on the falling edge of the SD clock. (Up to 25 MHz SD clock can be supported.) When enabled, SD controller outputs commands and data on the rising edge of the SD clock. (Up to 50 MHz SD clock can be supported.) 0=Normal speed. 1=High speed.												
1	DatTxWidth. Read-write. Reset: 0. Data Transfer Width. 0=1-bit. 1=4-bit.												
0	LedCtrl. Read-write. Reset: 0. LED control. 1=Drives the LED_ON output. 0=Off.												

SDHCx2C SDHC_CTRL2

Bits	Description
31:27	Reserved.
26	SoftRstDat. Read-write. Reset: 0. Software Reset for DAT Line. The following registers will be cleared: SDHCx20 [BuffData1,BuffData0], SDHCx24 [BufRdEn, BufWrEn, RdTxActive, WrTxActive, DatLineActive, CmdInhibDat], SDHCx28 [ContReq, BgStopReq], SDHCx30 [BufRdRdy, BufWrRdy, BlockGapEvt, DatDone].
25	SoftRstCmd. Read-write. Reset: 0. Software Reset for CMD Line. The following registers will be cleared: SDHCx24 [CmdInhibCmd], SDHCx30 [CmdDone].

24	SoftRstAll. Read-write. Reset: 0. Software Reset for All. The following registers will not be cleared:- CMD Line Signal Level- DAT[3:0] Line Signal Level- Write Protect Switch Pin Level- Card Detect Pin Level- Card State Stable- Card Inserted- all bits in the Capabilities Register- all bits in the Maximum Current Capabilities Register.																														
23:20	Reserved.																														
19:16	DataToCnt. Read-write. Reset: 0. Data Timeout Counter Value. By using this counter value, DAT line timeouts are detected. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>Eh-0h</td> <td>$2^{(DataToCnt+13)}$</td> <td>Fh</td> <td>Reserved.</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	Eh-0h	$2^{(DataToCnt+13)}$	Fh	Reserved.																						
Bits	Definition	Bits	Definition																												
Eh-0h	$2^{(DataToCnt+13)}$	Fh	Reserved.																												
15:8	SdclkDiv[7:0]. Read-write. Reset: 0. SDCLK Frequency Select. If multiple bits are set, the most significant bit will be selected. Host Controller Version 1.00 and 2.00: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000_0000b</td> <td>Divide by 1.</td> <td>0001_xxxxb</td> <td>Divide by 32</td> </tr> <tr> <td>0000_0001b</td> <td>Divide by 2.</td> <td>001x_xxxxb</td> <td>Divide by 64.</td> </tr> <tr> <td>0000_001xb</td> <td>Divide by 4.</td> <td>01xx_xxxxb</td> <td>Divide by 128.</td> </tr> <tr> <td>0000_01xxb</td> <td>Divide by 8.</td> <td>1xxx_xxxxb</td> <td>Divide by 256.</td> </tr> <tr> <td>0000_1xxxxb</td> <td>Divide by 16.</td> <td></td> <td></td> </tr> </tbody> </table> Host Controller Version 3.00: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>3FFh-001h</td> <td>Divide by $1/(2*SdclkDiv[9:0])$</td> </tr> <tr> <td>000h</td> <td>Divide by 1</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0000_0000b	Divide by 1.	0001_xxxxb	Divide by 32	0000_0001b	Divide by 2.	001x_xxxxb	Divide by 64.	0000_001xb	Divide by 4.	01xx_xxxxb	Divide by 128.	0000_01xxb	Divide by 8.	1xxx_xxxxb	Divide by 256.	0000_1xxxxb	Divide by 16.			Bits	Definition	3FFh-001h	Divide by $1/(2*SdclkDiv[9:0])$	000h	Divide by 1
Bits	Definition	Bits	Definition																												
0000_0000b	Divide by 1.	0001_xxxxb	Divide by 32																												
0000_0001b	Divide by 2.	001x_xxxxb	Divide by 64.																												
0000_001xb	Divide by 4.	01xx_xxxxb	Divide by 128.																												
0000_01xxb	Divide by 8.	1xxx_xxxxb	Divide by 256.																												
0000_1xxxxb	Divide by 16.																														
Bits	Definition																														
3FFh-001h	Divide by $1/(2*SdclkDiv[9:0])$																														
000h	Divide by 1																														
7:6	SdclkDiv[9:8]. Read-write. Reset: 0. See version 3.00 above.																														
5	ClkGenSel: Clock Generator Select. Read-write. Reset: 0. 1=Programmable Clock Mode. 0=Divided Clock Mode. Version 3.00.																														
4:3	Reserved.																														
2	SdclkEn. Read-write. Reset: 0. SD Clock Enable. SDCLK Frequency Select can be changed when this bit is 0. When card is removed, this bit is cleared to 0 automatically. 0=Disable. 1=Enable.																														
1	SysclkStable. Read-only. Reset: 0. Internal Clock Stable. 0=Unstable. 1=Stable.																														
0	SysclkEn. Read-write. Reset: 0. 1= Internal Clock Enable. 0=Disable.																														

SDHCx30 SDHC_INT_STATUS

Bits	Description
31:30	Reserved.
29	CeAtaErr. Read; Write-1-to-clear. Reset: 0. CE-ATA Error.
28	SdmaErr. Read; Write-1-to-clear. Reset: 0. SDMA Error.
27	Reserved.
26	TuningError. Read; Write-1-to-clear. Reset: 0. 1=An unrecoverable tuning error is detected in a during the tuning procedure.
25	AdmaErr. Read; Write-1-to-clear. Reset: 0. ADMA Error.
24	Acmd12Err. Read; Write-1-to-clear. Reset: 0. Auto CMD12 Error. Logical OR of Auto CMD12 Error Status Register.

23	Reserved.
22	DatEndErr. Read; Write-1-to-clear. Reset: 0. Data CRC Error.
21	DatCrcErr. Read; Write-1-to-clear. Reset: 0. Data CRC Error.
20	DatToErr. Read; Write-1-to-clear. Reset: 0. Data Timeout Error.
19	CmdIdxErr. Read; Write-1-to-clear. Reset: 0. Command Index Error. Mismatch of Command Index and index of response.
18	CmdEndErr. Read; Write-1-to-clear. Reset: 0. Command End Bit Error.
17	CmdCrcErr. Read; Write-1-to-clear. Reset: 0. Command CRC Error. If both CMD_TO_ERR and CMD_CRC_ERR are set, this indicates Command Conflict Error.
16	CmdToErr. Read; Write-1-to-clear. Reset: 0. Command Timeout Error. Response not returned within 128 SDCLK cycles.
15	Error. Read; Write-1-to-clear. Reset: 0. Error Interrupt.
14:13	Reserved.
12	ReTuningEvent. Read-only. Reset: 0. 1=Re-tuning should be performed.
11:9	Reserved.
8	Sdio. Read; Write-1-to-clear. Reset: 0. SDIO Card Interrupt. Writing 1 to this register does not clear this bit. To clear this bit, interrupt factor of SDIO cards should be cleared. The value of this bit is latched internally as long as the Card Interrupt bit (D08) in the Normal Interrupt Status Enable register is 1.
7	CardRem. Read; Write-1-to-clear. Reset: 0. Card Removal.
6	CardIns. Read; Write-1-to-clear. Reset: 0. Card Insertion.
5	BufRdRdy. Read; Write-1-to-clear. Reset: 0. Buffer Read Ready. In the case where Auto CMD12 is enabled and last block has been transferred, Auto CMD12 will be issued prior to this bit being set to 1. Clearing this bit should be done before buffer reading, because SD controller has dual buffer and the next Buffer Read Ready interrupt may occur immediately.
4	BufWrRdy. Read; Write-1-to-clear. Reset: 0. Buffer Write Ready. Clearing this bit should be done before buffer writing, because the SD controller has dual buffer and the next Buffer Write Ready interrupt may occur immediately.
3	DmaEvt. Read; Write-1-to-clear. Reset: 0. DMA Interrupt. It is set when internal counter reaches the value designated by Host DMA Buffer Boundary. It should be cleared by Host Driver after System Address Register is updated.
2	BlockGapEvt. Read; Write-1-to-clear. Reset: 0. Block Gap Event. It indicates the timing of next block gap, which was requested by the Stop At Block Gap Request. In case of write transaction, this interrupt will be generated before busy completion.
1	DatDone. Read; Write-1-to-clear. Reset: 0. Data Transfer Complete. Indicates the timing for completion of data transaction, which includes the completion at the block gap by the Stop At Block Gap Request. When some errors are detected during data transaction, this bit will not be set. In the case where Auto CMD12 is enabled, Auto CMD12 will be issued prior to this bit being set to 1.
0	CmdDone: cmdDone (r). Read-write. Reset: 0. Command Complete. The end bit of the command response is received. In the case of commands with no response, the end of the command.

SDHCx34 SDHC_INT_MASK

Bits	Description
31:30	Reserved.
29	CeAtaErrMask. Read-write. Reset: 0. CE-ATA Error. 0=Masked. 1=Enable.
28	SdmaErrMask. Read-write. Reset: 0. SDMA Error. 0=Masked. 1=Enable.
27	Reserved.
26	TuningErrorStatusEnable. Read-write. Reset: 0. 1=Tuning Event Status Enable. 0=Masked.
25	AdmaErrMask. Read-write. Reset: 0. ADMA Error. 0=Masked. 1=Enable.
24	Acmd12ErrMask. Read-write. Reset: 0. Auto CMD12 Error. 0=Masked. 1=Enable.
23	CurLimErrMask. Read-write. Reset: 0. Current Limit Error. 0=Masked. 1=Enable.
22	DatEndErrMask. Read-write. Reset: 0. Data End Bit Error. 0=Masked. 1=Enable.
21	DatCrcErrMask. Read-write. Reset: 0. Data CRC Error. 0=Masked. 1=Enable.
20	DatToErrMask. Read-write. Reset: 0. Data Timeout Error. 0=Masked. 1=Enable.
19	CmdIdxErrMask. Read-write. Reset: 0. Command Index Error. 0=Masked. 1=Enable.
18	CmdEndErrMask. Read-write. Reset: 0. Command End Bit Error. 0=Masked. 1=Enable.
17	CmdCrcErrMask. Read-write. Reset: 0. Command CRC Error. 0=Masked. 1=Enable.
16	CmdToErrMask. Read-write. Reset: 0. Command Timeout Error. 0=Masked. 1=Enable.
15:13	Reserved.
12	ReTuningEventStatusEn. Read-write. Reset: 0. 1=Re-Tuning Event Status Enable. 0=Masked.
11:9	Reserved.
8	SdioMask. Read-write. Reset: 0. Card Interrupt. 0=Masked. 1=Enable.
7	CardRemMask. Read-write. Reset: 0. Card Removal. 0=Masked. 1=Enable.
6	CardInsMask. Read-write. Reset: 0. Card Insertion. 0=Masked. 1=Enable.
5	BufRdRdyMask. Read-write. Reset: 0. Buffer Read Ready. 0=Masked. 1=Enable.
4	BufWrRdyMask. Read-write. Reset: 0. Buffer Write Ready. 0=Masked. 1=Enable.
3	DmaEvtMask. Read-write. Reset: 0. DMA Interrupt. 0=Masked. 1=Enable.
2	BlockGapEvtMask. Read-write. Reset: 0. Block Gap Event. 0=Masked. 1=Enable.
1	DatDoneMask. Read-write. Reset: 0. Transfer Complete. 0=Masked. 1=Enable.
0	CmdDoneMask. Read-write. Reset: 0. Command Complete. 0=Masked. 1=Enable.

SDHCx38 SDHC_SIG_MASK

Bits	Description
31:30	Reserved.
29	CeAtaErrEn. Read-write. Reset: 0. CE-ATA Error. 0=Masked. 1=Enable.
28	SdmaErrEn. Read-write. Reset: 0. SDMA Error. 0=Masked. 1=Enable.
27	Reserved.
26	TuningErrorStatusEnable. Read-write. Reset: 0. 1=Tuning Event Status Enable. 0=Masked.

25	AdmaErrEn. Read-write. Reset: 0. ADMA Error. 0=Masked. 1=Enable.
24	Acmd12ErrEn. Read-write. Reset: 0. Auto CMD12 Error. 0=Masked. 1=Enable.
23	CurLimErrEn. Read-write. Reset: 0. Current Limit Error. 0=Masked. 1=Enable.
22	DatEndErrEn. Read-write. Reset: 0. Data End Bit Error. 0=Masked. 1=Enable.
21	DatCrcErrEn. Read-write. Reset: 0. Data CRC Error. 0=Masked. 1=Enable.
20	DatToErrEn. Read-write. Reset: 0. Data Timeout Error. 0=Masked. 1=Enable.
19	CmdIdxErrEn. Read-write. Reset: 0. Command Index Error. 0=Masked. 1=Enable.
18	CmdEndErrEn. Read-write. Reset: 0. Command End Bit Error. 0=Masked. 1=Enable.
17	CmdCrcErrEn. Read-write. Reset: 0. Command CRC Error. 0=Masked. 1=Enable.
16	CmdToErrEn. Read-write. Reset: 0. Command Timeout Error. 0=Masked. 1=Enable.
15:13	Reserved.
12	ReTuningEventStatusEn. Read-write. Reset: 0. 1=Re-Tuning Event Status Enable. 0=Masked.
11:9	Reserved.
8	SdioEn. Read-write. Reset: 0. Card Interrupt. 0=Masked. 1=Enable.
7	CardRemEn. Read-write. Reset: 0. Card Removal. 0=Masked. 1=Enable.
6	CardInsEn. Read-write. Reset: 0. Card Insertion. 0=Masked. 1=Enable.
5	BufRdRdyEn. Read-write. Reset: 0. Buffer Read Ready. 0=Masked. 1=Enable.
4	BufWrRdyEn. Read-write. Reset: 0. Buffer Write Ready. 0=Masked. 1=Enable.
3	DmaEvtEn. Read-write. Reset: 0. DMA Interrupt. 0=Masked. 1=Enable.
2	BlockGapEvtEn. Read-write. Reset: 0. Block Gap Event. 0=Masked. 1=Enable.
1	DatDoneEn. Read-write. Reset: 0. Transfer Complete. 0=Masked. 1=Enable.
0	CmdDoneEn. Read-write. Reset: 0. Command Complete. 0=Masked. 1=Enable.

SDHCx3C SDHC ACMD12 Error/Host Control 2

Bits	Description												
31	PresetValEn. Read-write. Reset: 0. 1=Enable automatic selection of Preset Value. 0=SDCLK and driver strength are controlled by Host Driver.												
30	AsyncIntEn. Read-write. Reset: 0. Enable Asynchronous Interrupts.												
29:24	Reserved.												
23	SamplingClkSel. Read-write. Reset: 0. 1=Tuned clock is used to sample data. 0=Fixed clock is used to sample data.												
22	ExecTuning. Read-write; cleared-when-done. Reset: 0. 1=Execute Tuning. 0=Not Tuned or Tuning Completed.												
21:20	DvrStrengthSel. Read-write. Reset: 0. <table border="1" style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>Driver Type B is Selected (Default)</td> <td>10b</td> <td>Driver Type C is Selected</td> </tr> <tr> <td>01b</td> <td>Driver Type A is Selected</td> <td>11b</td> <td>Driver Type D is Selected</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	Driver Type B is Selected (Default)	10b	Driver Type C is Selected	01b	Driver Type A is Selected	11b	Driver Type D is Selected
Bits	Definition	Bits	Definition										
00b	Driver Type B is Selected (Default)	10b	Driver Type C is Selected										
01b	Driver Type A is Selected	11b	Driver Type D is Selected										
19	En_1_8VSignaling. Read-write. Reset: 0. 1=1.8 Volt Signaling. 0=3.3 Volt Signaling.												

18:16	UHS_ModeSel. Read-write. Reset: 0. Select UHS-I mode when (En_1_8VSignaling==1).																
	<table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>SDR12</td><td>011b</td><td>SDR104</td></tr> <tr> <td>001b</td><td>SDR25</td><td>100b</td><td>DDR50</td></tr> <tr> <td>010b</td><td>SDR50</td><td>111b-101b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	SDR12	011b	SDR104	001b	SDR25	100b	DDR50	010b	SDR50	111b-101b	Reserved
Bits	Definition	Bits	Definition														
000b	SDR12	011b	SDR104														
001b	SDR25	100b	DDR50														
010b	SDR50	111b-101b	Reserved														
15:8	Reserved.																
7	CmdErr. Read-only. Reset: 0. Command Not Issued By Auto CMD12 Error.																
6:5	Reserved.																
4	IndexErr. Read-only. Reset: 0. Auto CMD12 Index Error.																
3	EndErr. Read-only. Reset: 0. Auto CMD12 End Bit Error.																
2	CrcErr. Read-only. Reset: 0. Auto CMD12 CRC Error.																
1	ToErr. Read-only. Reset: 0. Auto CMD12 Timeout Error.																
0	ExeErr. Read-only. Reset: 0. Auto CMD12 Not Executed Error.																

SDHCx40 SDHC_CAPABILITY

Bits	Description												
31:30	SlotType. Read-only. Reset: 0. <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>Removable Card Slot</td><td>10b</td><td>Shared Bus Slot</td></tr> <tr> <td>01b</td><td>Embedded Slot for One Device</td><td>11b</td><td>Reserved.</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	Removable Card Slot	10b	Shared Bus Slot	01b	Embedded Slot for One Device	11b	Reserved.
Bits	Definition	Bits	Definition										
00b	Removable Card Slot	10b	Shared Bus Slot										
01b	Embedded Slot for One Device	11b	Reserved.										
29	AsynIntSup: Asynchronous Interrupt Support. Read-only. Reset: 1. 1=Asynchronous interrupt supported. 0=Asynchronous interrupt not supported.												
28	Support64BitSystemBus. Read-only. Reset: 0. 1=Host Controller supports 64-bit address descriptor mode and 64-bit address system bus.												
27	Reserved.												
26	Support18v. Read-only. Reset: 1. 1=Voltage Support for 1.8V.												
25	Support30v. Read-only. Reset: 0. 1=Voltage Support for 3.0V.												
24	Support33v. Read-only. Reset: 1. 1=Voltage Support for 3.3V.												
23	SusResSupport. Read-only. Reset: 1. 1=Suspend and Resume is supported.												
22	DmaSupport. Read-only. Reset: 1. 1=DMA is supported.												
21	HiSpeedSupport. Read-only. Reset: 1. 1=High Speed is supported.												
20	AdmaSupport. Read-only. Reset: 1. 1=Advanced DMA is supported.												
19	Adma2Support. Read-only. Reset: 1. 1=Advanced DMA2 is supported.												
18	Mmc8Support. Read-only. Reset: 0. Extended Media Bus Support (MMC).												
17:16	MaxBlkLen. Read-only. Reset: 2h. Specifies the maximum block size that the Host Driver can read and write to the buffer in the Host Controller. The buffer shall transfer this block size without wait cycles. <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>512 bytes</td><td>10b</td><td>2048 bytes</td></tr> <tr> <td>01b</td><td>1024 bytes</td><td>11b</td><td>Reserved</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	512 bytes	10b	2048 bytes	01b	1024 bytes	11b	Reserved
Bits	Definition	Bits	Definition										
00b	512 bytes	10b	2048 bytes										
01b	1024 bytes	11b	Reserved										

15:8	BaseClkFreq. Read-only. Reset: 32h. Specifies the base clock frequency for SD Clock. <u>Bits</u> <u>Definition</u> 00h Reserved FFh-01h <BaseClkFreq> MHz
7	TmoClkUnit: Timeout Clock Unit. Read-only. Reset: 1. Specifies the unit of TmoClkFreq. 0=Unit is KHz. 1=Unit is MHz.
6	Reserved.
5:0	TmoClkFreq: Timeout Clock Frequency. Read-only. Reset: 32h. Specifies the base clock frequency used to detect Data Timeout Error. TmoClkUnit defines the unit of this field's value.

SDHCx44 SDHC_CAPABILITY 2

Bits	Description
31:24	Reserved.
23:16	ClockMultiplier. Read-only. Reset: 3. <u>Bits</u> <u>Definition</u> 00h ClockMultiplier not supported. FFh-01h <ClockMultiplier+1> MHz
15:14	ReTuningModes. Read-only. Reset: 0. Specifies re-tuning method and limits the maximum data length. <u>Bits</u> <u>Definition</u> 00b Mode 1, Timer, 4 MBMax Data length. 01b Mode 2, Timer and Re-Tuning Request, 4 MBMax Data length. 10b Mode 3, Auto Re-Tuning (for transfer)Timer and Re-Tuning Request, any Data Length. 11b Reserved.
13	UseTuningForSDR50. Read-only. Reset: 0. 1=SDR50 requires tuning.
12	Reserved.
11:8	TimerCountForReTuning. Read-only. Reset: 5. Specifies value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. <u>Bits</u> <u>Definition</u> 0h Re-tuning timer disabled. 1h 1 Second Bh-2h <2^(TimerCountForReTuning-1)> Seconds Eh-Ch Reserved Fh Get information from other source.
7	Reserved.
6	DriverTypeDSupport. Read-only. Reset: 0. 1=Support of Driver Type D for 1.8 Signaling.
5	DriverTypeCSupport. Read-only. Reset: 0. 1=Support of Driver Type C for 1.8 Signaling.
4	DriverTypeASupport. Read-only. Reset: 0. 1=Support of Driver Type A for 1.8 Signaling.
3	Reserved.

2	DDR50Support. Read-only. Reset: 0. 1=DDR50 is supported.
1:0	SDRSupport. Read-only. Reset: 3. <u>Bit</u> <u>Definition</u> [0] 1=SDR50 is supported. [1] 1=SDR104 is supported.

SDHCx48 SDHC_CURR_CAPABILITY

Bits	Description
31:24	Reserved.
23:16	MaxCurr18v. Read-only. Reset: C8h. Max Current for 1.8V.
15:8	MaxCurr30v. Read-only. Reset: 0. Max Current for 3.0V.
7:0	MaxCurr33v. Read-only. Reset: 64h. Max Current for 3.3V.

SDHCx50 SDHC_FORCE_EVT

Bits	Description
31:30	Reserved.
29	CeAtaErrFrc. Read-write. Reset: 0. Force CE-ATA Error.
28	SdmaErrFrc. Read-write. Reset: 0. Force SDMA Error.
27:26	Reserved.
25	AdmaErrFrc. Read-write. Reset: 0. Force ADMA Error.
24	Acmd12ErrFrc. Read-write. Reset: 0. Force Auto CMD12 Error.
23	CurLimErrFrc. Read-write. Reset: 0. Force Current Limit Error.
22	DatEndErrFrc. Read-write. Reset: 0. Force Data End Bit Error.
21	DatCrcErrFrc. Read-write. Reset: 0. Force Data CRC Error.
20	DatToErrFrc. Read-write. Reset: 0. Force Data Timeout Error.
19	CmdIdxErrFrc. Read-write. Reset: 0. Force Command Index Error.
18	CmdEndErrFrc. Read-write. Reset: 0. Force Command End Bit Error.
17	CmdCrcErrFrc. Read-write. Reset: 0. Force Command CRC Error.
16	CmdToErrFrc. Read-write. Reset: 0. Force Command Timeout Error.
15:8	Reserved.
7	Acmd12CmdErrFrc. Read-write. Reset: 0. Force Command Not Issued By Auto CMD12 Error.
6:5	Reserved.
4	Acmd12IdxErrFrc. Read-write. Reset: 0. Force Auto CMD12 Index Error.
3	Acmd12EndErrFrc. Read-write. Reset: 0. Force Auto CMD12 End Bit Error.
2	Acmd12CrcErrFrc. Read-write. Reset: 0. Force Auto CMD12 CRC Error.
1	Acmd12ToErrFrc. Read-write. Reset: 0. Force Auto CMD12 Timeout Error.
0	Acmd12ExeErrFrc. Read-write. Reset: 0. Force Auto CMD12 Not Executed Error.

SDHCx54 SDHC_ADMA_ERR

Bits	Description										
31:3	Reserved.										
2	AddrLenMismatch. Read-only. Reset: 0. ADMA Address Length Mismatch Error. This error occurs in the following 2 cases:1. While Block Count Enable being set, the total data length specified by the descriptor table is different from that specified by the Block Count and Block Length.2. Total data length cannot be divided by the block length.										
1:0	AdmaState. Read-only. Reset: 0. ADMA State when error has occurred. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Stop DMA</td> </tr> <tr> <td>01b</td> <td>Fetch Descriptor.</td> </tr> <tr> <td>10b</td> <td>Change Address.</td> </tr> <tr> <td>11b</td> <td>Transfer Data.</td> </tr> </tbody> </table>	Bits	Definition	00b	Stop DMA	01b	Fetch Descriptor.	10b	Change Address.	11b	Transfer Data.
Bits	Definition										
00b	Stop DMA										
01b	Fetch Descriptor.										
10b	Change Address.										
11b	Transfer Data.										

SDHCx58 SDHC_ADMA_SAD

Bits	Description
31:16	AdmaSysAddr1. Read-write. Reset: 0. Upper bits. ADMA System Address. Before ADMA data transfer, the descriptor address should be set by the Host Driver. This address needs to be set with 4-byte alignment, since the descriptor table has 32-bit (4 byte) information formatted.
15:0	AdmaSysAddr0. Read-write. Reset: 0. Lower bits.

SDHCx6[C:0:step4] Preset Value

Table 234: Register Mapping for SDHCx6[C:0:step4]

Register	Function					
SDHCx60	Initialization 3.3V or 1.8V/Default Speed 3.3V					
SDHCx64	High Speed 3.3V/SDR12 1.8V Preset Values					
SDHCx68	SDR25 1.8V/SDR50 1.8V Preset Values					
SDHCx6C	SDR104 1.8V/DDR50 1.8V Preset Values					

Table 235: Field Mapping for SDHCx6[C:0:step4]

Register	Bits						
	31:30	26	25:16	15:14	10	9:0	
SDHCx60	DefaultSpeed	DefaultSpeed	DefaultSpeed	Initialization	Initialization	Initialization	
SDHCx64	SDR12	SDR12	SDR12	HighSpeed	HighSpeed	HighSpeed	
SDHCx68	SDR50	SDR50	SDR50	SDR25	SDR25	SDR25	
SDHCx6C	DDR50	DDR50	DDR50	SDR104	SDR104	SDR104	

Bits	Description
31:30	DvrStrengthSelPreset1. See: DvrStrengthSelPreset0.

29:27	Reserved.												
26	ClkGenSelPreset1 . See: ClkGenSelPreset0.												
25:16	SdClkFreqSel1 . See: SdClkFreqSel0.												
15:14	DvrStrengthSelPreset0 . Read-only. Driver Strength is supported by 1.8V signaling bus speed modes. Does not apply for 3.3V signaling. See SDHCx3C[DvrStrengthSel] .												
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Driver Type B is Selected</td> <td>10b</td> <td>Driver Type C is Selected</td> </tr> <tr> <td>01b</td> <td>Driver Type A is Selected</td> <td>11b</td> <td>Driver Type D is Selected</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	Driver Type B is Selected	10b	Driver Type C is Selected	01b	Driver Type A is Selected	11b	Driver Type D is Selected
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00b	Driver Type B is Selected	10b	Driver Type C is Selected										
01b	Driver Type A is Selected	11b	Driver Type D is Selected										
13:11	Reserved.												
10	ClkGenSelPreset0 . Read-only. Clock Generator Select Value. See SDHCx2C[ClkGenSel] . 1=Programmable Clock Generator. 0=Host Controller Ver2.00 Compatible Clock Generator.												
9:0	SdClkFreqSel0 . Read-only. A10-bit preset value. See SDHCx2C[SdclkDiv[9:0]] .												

SDHCxE0 Shared Bus Control Register

Bits	Description																				
31	Reserved.																				
30:24	BackEndPwrCtrl: Back-End Power Control . Read-write. Reset: 0. 0=Back-end Power is Off. 1=Back-end Power is Supplied. <table> <thead> <tr> <th>Bit</th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>Back-end Power Control for Device 1</td> </tr> <tr> <td>[1]</td> <td>Back-end Power Control for Device 2</td> </tr> <tr> <td>[2]</td> <td>Back-end Power Control for Device 3</td> </tr> <tr> <td>[3]</td> <td>Back-end Power Control for Device 4</td> </tr> <tr> <td>[4]</td> <td>Back-end Power Control for Device 5</td> </tr> <tr> <td>[5]</td> <td>Back-end Power Control for Device 6</td> </tr> <tr> <td>[6]</td> <td>Back-end Power Control for Device 7</td> </tr> </tbody> </table>	Bit	<u>Definition</u>	[0]	Back-end Power Control for Device 1	[1]	Back-end Power Control for Device 2	[2]	Back-end Power Control for Device 3	[3]	Back-end Power Control for Device 4	[4]	Back-end Power Control for Device 5	[5]	Back-end Power Control for Device 6	[6]	Back-end Power Control for Device 7				
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[5]	Back-end Power Control for Device 6																				
[6]	Back-end Power Control for Device 7																				
23	Reserved.																				
22:20	IntPinSel . Read-write. Reset: 0. Selects interrupt pin inputs. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Interrupt is detected by Interrupt Cycle</td> <td>x1xb</td> <td>INT_B is Enabled</td> </tr> <tr> <td>xx1b</td> <td>INT_A is Enabled</td> <td>1xxb</td> <td>INT_C is Enabled</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	000b	Interrupt is detected by Interrupt Cycle	x1xb	INT_B is Enabled	xx1b	INT_A is Enabled	1xxb	INT_C is Enabled								
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xx1b	INT_A is Enabled	1xxb	INT_C is Enabled																		
19	Reserved.																				
18:16	ClkPinSel . Read-write. Reset: 0. Selects one of clock pin outputs. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Clock Pins are Disabled</td> <td>100b</td> <td>CLK[4] is Selected</td> </tr> <tr> <td>001b</td> <td>CLK[1] is Selected</td> <td>101b</td> <td>CLK[5] is Selected</td> </tr> <tr> <td>010b</td> <td>CLK[2] is Selected</td> <td>110b</td> <td>CLK[6] is Selected</td> </tr> <tr> <td>011b</td> <td>CLK[3] is Selected</td> <td>111b</td> <td>CLK[7] is Selected</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	000b	Clock Pins are Disabled	100b	CLK[4] is Selected	001b	CLK[1] is Selected	101b	CLK[5] is Selected	010b	CLK[2] is Selected	110b	CLK[6] is Selected	011b	CLK[3] is Selected	111b	CLK[7] is Selected
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011b	CLK[3] is Selected	111b	CLK[7] is Selected																		
15	Reserved.																				

14:8	BusWidthPreset. Read-only. 0=4-bit bus width mode (Data Transfer Width = 1). 1=8-bit bus width mode. <table border="0"> <thead> <tr> <th><u>Bit</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Bus Width Preset for Device 1</td></tr> <tr> <td>[1]</td><td>Bus Width Preset for Device 2</td></tr> <tr> <td>[2]</td><td>Bus Width Preset for Device 3</td></tr> <tr> <td>[3]</td><td>Bus Width Preset for Device 4</td></tr> <tr> <td>[4]</td><td>Bus Width Preset for Device 5</td></tr> <tr> <td>[5]</td><td>Bus Width Preset for Device 6</td></tr> <tr> <td>[6]</td><td>Bus Width Preset for Device 7</td></tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	Bus Width Preset for Device 1	[1]	Bus Width Preset for Device 2	[2]	Bus Width Preset for Device 3	[3]	Bus Width Preset for Device 4	[4]	Bus Width Preset for Device 5	[5]	Bus Width Preset for Device 6	[6]	Bus Width Preset for Device 7				
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[5]	Bus Width Preset for Device 6																				
[6]	Bus Width Preset for Device 7																				
7:6	Reserved.																				
5:4	NumIntInputPins. Read-only. Indicates support of interrupt input pins INT_A#, INT_B# and INT_C# for shared bus system. <table border="0"> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th><th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>Interrupt Input Pin is Not Supported</td><td>10b</td><td>INTA and INTB are Supported</td></tr> <tr> <td>01b</td><td>INTA is Supported</td><td>11b</td><td>INTA, INTB and INTC are Supported</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	Interrupt Input Pin is Not Supported	10b	INTA and INTB are Supported	01b	INTA is Supported	11b	INTA, INTB and INTC are Supported								
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3	Reserved.																				
2:0	NumofClkPins. Read-only. This field indicates support of clock pins to select one of devices for shared bus system. <table border="0"> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th><th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>Shared bus is not supported</td><td>100b</td><td>4 SDCLK pin is supported</td></tr> <tr> <td>001b</td><td>1 SDCLK pin is supported</td><td>101b</td><td>5 SDCLK pin is supported</td></tr> <tr> <td>010b</td><td>2 SDCLK pin is supported</td><td>110b</td><td>6 SDCLK pin is supported</td></tr> <tr> <td>011b</td><td>3 SDCLK pin is supported</td><td>111b</td><td>7 SDCLK pin is supported</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	000b	Shared bus is not supported	100b	4 SDCLK pin is supported	001b	1 SDCLK pin is supported	101b	5 SDCLK pin is supported	010b	2 SDCLK pin is supported	110b	6 SDCLK pin is supported	011b	3 SDCLK pin is supported	111b	7 SDCLK pin is supported
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>																		
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011b	3 SDCLK pin is supported	111b	7 SDCLK pin is supported																		

SDHCxFc SDHC_VER_SLOT

Bits	Description
31:24	VendorVersion. Read-only. Reset: 0. Vendor version.
23:16	SpecVersion. Read-only. Reset: 0. Specification version.
15:8	Reserved.
7:0	SlotIntrpt. Read-only. Reset: 0. Interrupt Signal for Each Slot. The value of XSLT_INT7-0 inputs, which indicates the logical OR of Interrupt signal and Wakeup signal, are inverted and referred to by this register. In case of multiple slots, Interrupt signal and Wakeup signal should be logical OR'ed externally and should be inputted to each of XSLT_INT7-0.

3.26.7 SMBus Host Controller

3.26.7.1 Device 14h Function 0 (SMBus) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D14F0x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: Device Identifier. Value: 780Bh. This 16-bit field is assigned by the device manufacturer and identifies the type of device. The device ID is selected by internal e-fuses.
15:0	VendorID. Read-only. Reset: 1022h. Vendor Identifier.

D14F0x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; write-1-to-clear. Reset: 0. This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled.
30	SignaledSystemError: Signaled System Error. Read; write-1-to-clear. Reset: 0. This bit is set by the device whenever the device asserts SERR#.
29	ReceivedMasterAbort: Received Master Abort. Read; write-1-to-clear. Reset: 0. This bit is set by a slave device whenever it terminates its transaction with master abort.
28	ReceivedTargetAbort: Received Target Abort. Read; write-1-to-clear. Reset: 0. This bit is set by a master device whenever its transaction is terminated with target abort.
27	SignaledTargetAbort: Signaled Target Abort. Read; write-1-to-clear. Reset: 0. This bit is set by a slave device whenever it terminates a cycle with target abort.
26:25	DEVSELTiming: DEVSEL Timing. Value: 1. These bits encode the timing of DEVSEL#. This module always responds in medium timing.
24	DataParityErrorDetected: Data Parity Error Detected. Read; write-1-to-clear. Reset: 0. 1=The Parity Error Response bit is set and the module has detected PERR# asserted while acting as a PCI master regardless of whether PERR# was driven by this module.
23	FastBack2BackCapable: Fast Back to Back Capable. Value: 0. 0=Fast back to back cycles are not supported.
22	UDFSupported: UDF Supported. Value: 0. 0=User definable feature is not supported.
21	Capable66MHz: 66 MHz Capable. Value: 1. 1=This device is 66 MHz capable.
20	MsiMappingCapability: MSI Mapping Capability. Value: 1. 1=This device supports MSI mapping.
19:10	Reserved.
9	FastBack2BackEnable: Fast Back-to-Back Enable. Value: 0. ACPI/SMBus does not support fast back-to-back.
8	SERREnable: System Error Enable. Read-write. Reset: 0. 1=Enable system error reporting.
7	WaitCycleControl: Wait Cycle Control. Value: 0. 0=This module does not use address stepping.

6	ParityErrorResponse: Parity Error Response. Read-write. Reset: 0. This bit controls the device's response to parity errors. 1=The device must take its normal action when a parity error is detected. 0=The device must ignore any parity errors that it detects and continue normal operation.
5	VGAPaletteSnoop: VGA Palette Snoop. Value: 0. This bit does not apply to this module.
4	MemoryWriteInvalidateEnable: Memory Write and Invalidate Enable. Value: 0. This module does not generate Memory Write and Invalidate command.
3	SpecialCycle: Special Cycle. Value: 0. This module does not respond to special cycle.
2	BusMaster: Bus Master. Value: 0. ACPI/SMBus does not have PCI master.
1	MemorySpace: Memory Space. Read-write. Reset: 1. 1=Enable the device to respond to memory space accesses.
0	IOSpace: IO Space. Read-write. Reset: 1. 1=Enable the device to respond to IO space accesses.

D14F0x08 Revision ID/Class Code

Bits	Description
31:8	ClassCode: Class Code. Value: C0500h. Specifies a SMBUS controller.
7:0	RevisionID: Revision ID. Value: IF (RevA0) THEN 39h. ELSEIF (RevA1) THEN 3Ah. ENDIF.

D14F0x0C Cache Line Size

Bits	Description
31:24	Bist. Value: 0. The module has no built-in self-test and so this is always 0.
23:16	HeaderType: Header Type. Value: 80h. This device is a multifunction device.
15:8	LatencyTimer: Latency Timer. Value: 0. This register specifies the value of the Latency Timer. This is not used in this module and so it is always 0.
7:0	CacheLineSize: Cache Line Size. Value: 0. This register specifies the system cache line size. This module does not use Memory Write and Invalidate command and so this register is not applicable. It is hard coded to 0.

D14F0x10 Base Address 0

Bits	Description
31:0	BaseAddress0: Base Address 0. Value: 0. Not used and is hard coded to 0.

D14F0x14 Base Address 1

Bits	Description
31:0	BaseAddress1: Base Address 1. Value: 0. Not used and is hard coded to 0.

D14F0x18 Base Address 2

Bits	Description
31:0	BaseAddress2: Base Address 2. Value: 0. Not used and is hard coded to 0.

D14F0x1C Base Address 3

Bits	Description
31:0	BaseAddress3: Base Address 3. Value: 0. Not used and is hard coded to 0.

D14F0x20 Base Address 4

Bits	Description
31:0	BaseAddress4: Base Address 4. Value: 0. Not used and is hard coded to 0.

D14F0x24 Base Address 5

Bits	Description
31:0	BaseAddress5: Base Address 5. Value: 0. Not used and is hard coded to 0.

D14F0x28 Cardbus CIS Pointer

Bits	Description
31:0	CardbusCISPointer: Cardbus CIS Pointer. Value: 0. Not used and is hard coded to 0.

D14F0x2C Subsystem Vendor ID

Bits	Description
31:16	SubsystemID: Subsystem ID. Write-once. Reset: 780Bh.
15:0	SubsystemVendorID: Subsystem Vendor ID. Write-once. Reset: 1022h.

D14F0x30 Expansion ROM Base Address

Bits	Description
31:8	Reserved.
7:0	ExpansionROMBaseAddress: Expansion ROM Base Address. Value: 0. Not used.

D14F0x34 Capability Pointer

Bits	Description
31:8	Reserved.
7:0	CapabilityPointer: Capability Pointer. Read-only. Reset: 0.

D14F0x3C Interrupt Line

Bits	Description
31:24	MaxLat. Value: 0. Device has no requirements for the setting.
23:16	MinGnt. Value: 0. Device has no requirements for the setting.
15:8	InterruptPin: Interrupt Pin. Value: 0. 0=This module does not generate interrupts.
7:0	InterruptLine: Interrupt Line. Value: 0. This module does not generate interrupts.

3.26.7.2 ASF (Alert Standard Format) Registers

ASF register space is accessed through two methods:

- IO access through ASF IO base address defined by [PMx28 \[AsfEn\]](#):
 - A. Program the base address of ASF IO space through [PMx28\[AsfIoBase\]](#).
 - B. Enable ASF function and IO decoding through [PMx28\[AsfEn\]](#).
- Direct memory mapped or IO mapped access through the AcpiMmio region. The ASF registers range from [PMx24\[AcpiMmioAddr\]+900h](#) to [PMx24\[AcpiMmioAddr\]+9FFh](#). See [PMx24 \[AcpiMmioEn\]](#).

ASFx00 HostStatus

Bits	Description
7	LastByte. Read; set-by-hardware; write-1-to-clear. Reset: 0. 0=Last byte has not received. 1=Last byte has received.
6:5	Reserved.
4	PECError. Read; set-by-hardware; write-1-to-clear. Reset: 0. 0=No CRC error. 1=CRC error happened.
3	BusCollision. Read; set-by-hardware; write-1-to-clear. Reset: 0. 0=No bus collision. 1=Bus collision.
2	DevError. Read; set-by-hardware; write-1-to-clear. Reset: 0. 0=Slave device behaves correctly. 1=No ACK or slave device responses incorrectly.
1	Intr. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Termination of a command. Whenever [HostBusy] is cleared, this bit is set.
0	HostBusy. Read-only; updated-by-hardware. Reset: 0. This bit reports the status of the ASF host. 0=SM bus host is idle. 1=SM bus host is busy.

ASFx02 HostControl

Bits	Description																		
7	PECEnable. Read-write. Reset: 0. 0=PEC disable. 1=PEC enable. Enable CRC checking when ASF HC presents as SM master and SM slave.																		
6	Start. Write-1-only; Read. Reset: 0. 1=Writing 1 to initiate the command. Always read back as 0.																		
5	PECApend. Read-write. Reset: 0. 0=No PEC append. 1=Automatic PEC append. ASF HC calculates CRC code and append to the tail of the data packets.																		
4:2	Protocol. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Quick</td> </tr> <tr> <td>001b</td> <td>Byte</td> </tr> <tr> <td>010b</td> <td>Byte data</td> </tr> <tr> <td>011b</td> <td>Word data</td> </tr> <tr> <td>100b</td> <td>Process call</td> </tr> <tr> <td>101b</td> <td>Block</td> </tr> <tr> <td>110b</td> <td>Block write-block read-process call</td> </tr> <tr> <td>111b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	000b	Quick	001b	Byte	010b	Byte data	011b	Word data	100b	Process call	101b	Block	110b	Block write-block read-process call	111b	Reserved
Bits	Definition																		
000b	Quick																		
001b	Byte																		
010b	Byte data																		
011b	Word data																		
100b	Process call																		
101b	Block																		
110b	Block write-block read-process call																		
111b	Reserved																		
1	KillHost. Read-write. Reset: 0. 0=Enable SM master. 1=Reset SM master.																		
0	Reserved.																		

ASFx03 HostCommand

Bits	Description
7:0	HostCommand. Read-write. Reset: 0. Command to be transmitted by master.

ASFx04 SlaveAddress

Bits	Description
7:1	Address. Read-write. Reset: 0. Provide the SM address of slave.
0	RW. Read-write. Reset: 0. 0=Write. 1=Read.

ASFx05 Data0

Bits	Description
7:0	Data0. Read-write. Reset: 0. Contains count or DATA0 field of transaction. This field has different meanings depending on the transactions: <ul style="list-style-type: none"> • Contains count to indicate how many bytes to be sent (not including PEC byte) in block write and block write-block read-process call. • Contains count to indicate how many bytes have been received in block read and block write-block read-process call. • First byte of Data bytes in byte/word write and process Call or first byte received in byte/word read.

ASFx06 Data1

Bits	Description
7:0	Data1 . Read-write. Reset: 0. Contains DATA1 field of transaction.

ASFx07 DataIndex

Bits	Description
7:0	DataIndex . Read-write. Reset: 0. It is mapped to 72 data registers in data buffer for block write/read and block write-block read-process call.

ASFx08 PEC

Bits	Description
7:0	Pec . Read-write. Reset: 0. PEC byte to be sent to slave.

ASFx09 ListenAdr

Bits	Description
7:1	ListenAdr . Read-write. Reset: 0. The slave address which ASF slave responds in listen mode.
0	ListenAdrEn . Read-write. Reset: 0. 1=Enable Listen Mode when the slave address equals to ListenAdr[7:1]. 0=Disable Listen Mode when the slave address equals to ListenAdr[7:1].

ASFx0A ASFStatus

Bits	Description
7:6	SlaveBusy . Read-Only. Reset: 0. Indicates if ASF slave is receiving data.
5	SlaveIntr . Read; write-1-to-clear. Reset: 0. ASF Slave interrupt Status.
4	Reserved.
3	RemotePowerCycle . Read; write-1-to-clear. Reset: 0. 1=Power cycle has been triggered by ASF. 0=No power cycle ASF event.
2	RemotePowerUp . Read; write-1-to-clear. Reset: 0. 1=Power up has been triggered by ASF. 0=No Power up ASF event.
1	RemotePowerDown . Read; write-1-to-clear. Reset: 0. 1=Power down has been triggered by ASF. 0=No Power down ASF event.
0	RemoteReset . Read; write-1-to-clear. Reset: 0. 1=Reset has been triggered by ASF. 0=No Reset cycle ASF event.

ASFx0B StatusMask0

Bits	Description
7:6	Reserved.
5	FanSpeed0StatusEnable . Read-write. Reset: 0. 1=Report Fan0 Speed Status to ASF. 0=No report.
4:1	Reserved.
0	Temp0StatusEnable . Read-write. Reset: 0. 1=Report TempTsi status to ASF. 0=No report.

ASFx0C StatusMask1

Bits	Description
7:0	Reserved.

ASFx0D SlaveStatus

Bits	Description
7:4	Reserved.
3	WrongSP . Read; write-1-to-clear. Reset: 0. 1=No SP symbol is detected when bus turns to read.
2	SlaveDevError . Read; write-1-to-clear. Reset: 0. 1=Unexpected response.
1	SlaveBusCollision . Read; write-1-to-clear. Reset: 0. 1=BusCollision happens.
0	SlavePECError . Read; write-1-to-clear. Reset: 0. 1=PEC error.

ASFx0E RemoteCtrlAdr

Bits	Description
7:1	RemoteCtrlAdr . Read-write. Reset: 54h. SM address of Remote Control device.
0	Reserved.

ASFx0F SensorAdr

Bits	Description
7:1	SensorAdr . Read-write. Reset: 55h. SM address of Sensor.
0	Reserved.

ASFx10 DataReadPointer

Bits	Description
7:0	DataReadPointer . Read-only. Reset: 0. Current read pointer to the value specified in this register.

ASFx11 DataWritePointer

Bits	Description
7:0	DataWritePointer . Read-only. Reset: 0. Show current write pointer to the value specified in this register.

ASFx12 SetDataReadPointer

Bits	Description
7:0	SetDataReadPointer . Read-write. Reset: 0. Force the current write pointer to the value specified in this register.

ASFx13 DataBankSel

Bits	Description										
7	SetReadHostDataBank . Read-write. Reset: 0. 1=Select to read data from Host Data Bank. 0=Select to read data from Data Bank 0 or Data Bank 1 decided by SetReadRevDataBank.										
6	Reserved.										
5:4	SetReadRevDataBank . Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Select to read data from Data Bank 0.</td></tr> <tr> <td>01b</td> <td>Select to read data from Data Bank 1.</td></tr> <tr> <td>10b</td> <td>Select to read data from Data Bank 1.</td></tr> <tr> <td>11b</td> <td>Select to read data from Data Bank 1.</td></tr> </tbody> </table>	Bits	Definition	00b	Select to read data from Data Bank 0.	01b	Select to read data from Data Bank 1.	10b	Select to read data from Data Bank 1.	11b	Select to read data from Data Bank 1.
Bits	Definition										
00b	Select to read data from Data Bank 0.										
01b	Select to read data from Data Bank 1.										
10b	Select to read data from Data Bank 1.										
11b	Select to read data from Data Bank 1.										
3	Databank1Full . Read; write-1-to-clear. Reset: 0. 0=Data Bank 1 is free. 1=Data Bank 1 is full.										
2	Databank0Full . Read; write-1-to-clear. Reset: 0. 0=Data Bank 0 is free. 1=Data Bank 0 is full.										
1	DataBank[1] . Read; write-1-to-clear. Reset: 0. 0=Data Bank still has space. 1=Data Bank is now full.										
0	DataBank[0] . Read; write-1-to-clear. Reset: 0. 0=Data Bank 0 is the latest touched data bank. 1=Data Bank 1 is the latest touched data bank.										

ASFx14 Semaphore

Bits	Description
7:4	Reserved.
3	ClrEcSemaphore . Write-1-only; cleared-by-hardware. Reset: 0. Write 1 to clear [EcSemaphore] bit.
2	EcSemaphore . Read; write-1-only. Reset: 0. This bit can only be set when [HostSemaphore] is clear.

1	ClrHostSemaphore . Write-1-only; cleared-by-hardware. Reset: 0. Write 1 to clear [HostSemaphore] bit.
0	HostSemaphore . Read; write-1-only. Reset: 0. Bits [0] and [2] are meant to be used as software semaphore between the host and IMC. When both host and IMC want to use the same resource, they can write to these semaphore bits first, followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Read returns the value of this bit.

ASFx15 SlaveEn

Bits	Description
7	FairArbEn . Read-write. Reset: 0. 0=Disable Fair arbiter logic. 1=Enable Fair Arbiter logic, which forces ASF master to give up SMBus for a certain time, specified in register at offset 16h.
6	TmrOutEn . Read-write. Reset: 0. 1=Enable timer out function.
5	LegacySensorEn . Read-write. Reset: 0. 1=Enable Legacy Sensor.
4	KillSlave . Read-write. Reset: 0. Write 1 to reset Slave ASF Slave state machine.
3	SuspendSlave . Read-write. Reset: 0. Write 1 to Suspend (stop) ASF Slave state machine.
2	Reserved.
1	SlaveIntrListenEn . Read-write. Reset: 0. 1=Allow ASF slave to generate slave interrupt when the address of received packet is the same as the one specified in ListenAdr register ASFx09 [ListenAdr] .
0	Reserved.

ASFx16 DelayMasterTimer

Bits	Description
7:0	FairArbTimer . Read-write. Reset: 10h. Specify how long ASF master has to wait before submitting next packet. Wait time = FairArbTimer* 2 us.

3.26.7.3 SMBus Registers

SMBus register space is accessed through two methods:

- IO access through SMBus IO base address defined by [PMx2C \[Smbus0En\]](#):
 - A. Program the base address of SMBus IO space through [PMx2C\[Smbus0IoBase\]](#).
 - B. Enable SMBus function and IO decoding through [PMx2C\[SmBus0En\]](#).
- Direct memory mapped or IO mapped access through the AcpiMmio region. The SMBus registers range from [PMx24\[AcpiMmioAddr\]+A00h](#) to [PMx24\[AcpiMmioAddr\]+AFFh](#). See [PMx24 \[AcpiMmioEn\]](#).

SMBUSx00 SMBusStatus

Bits	Description
7:5	Reserved.
4	Failed . Write-1-to-clear; set-by-hardware; read. Reset: 0. 1=A Failed bus transaction. IF (SMBUSx02[Kill]==1) THEN SMBUSx00[Failed]=1 . ENDIF.
3	BusCollision . Write-1-to-clear; set-by-hardware; read. Reset: 0. 1=An SMBus transaction collision.

2	DeviceErr. Write-1-to-clear; set-by-hardware; read. Reset: 0. 1=An error of one of the following: <ul style="list-style-type: none">• Illegal command field.• Unclaimed cycle• Host device time-out.
1	SMBusInterrupt. Write-1-to-clear; set-by-hardware; read. Reset: 0. 1=The completion of the last host command.
0	HostBusy. Read-only. Reset: 0. 1=The SMBus controller is in the process of completing a command. When this bit is set, software should not access any other SMBus registers.

SMBUSx01 SMBusSlaveStatus

Bits	Description
7:6	Reserved.
5	AlertStatus. Read-only. Reset: 0. This bit is set by hardware to indicate an SMBALERT_ signal. This function is not supported.
4	Shadow2Status. Write-1-to-clear; set-by-hardware; read. Reset: 0. This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow2 port.
3	Shadow1Status. Write-1-to-clear; set-by-hardware; read. Reset: 0. This bit is set by hardware to indicate a slave cycle address match of the SMB_Shadow1 port.
2	SlaveStatus. Write-1-to-clear; set-by-hardware; read. Reset: 0. This bit is set by hardware to indicate a slave cycle event match of the SMBus slave command and SMBus Slave Event match.
1	SlaveInit. RAZ; write-1-only. Reset: 0. Writing a 1 to this bit initializes the slave.
0	SlaveBusy. Read-only. Reset: 0. This bit indicates the SMBus controller slave interface is in the process of receiving data. Software should not try to access any other SMBus register when this bit is set.

SMBUSx02 SMBusControl

Bits	Description																
7	Reset. Write-only. Reset: 0. Set the bit to 1 to stop SMBus transaction and reset SMBus controller state machine.																
6	Start. Read-write. Reset: 0. Writing a 1 in this field initiates SMBus controller host interface to execute the command programmed in the [SMBusProtocol] field.																
5	Reserved.																
4:2	SMBusProtocol. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Quick Read or Write</td> </tr> <tr> <td>001b</td> <td>Byte Read or Write</td> </tr> <tr> <td>010b</td> <td>Byte Data Read or Write</td> </tr> <tr> <td>011b</td> <td>Word Data Read or Write</td> </tr> <tr> <td>100b</td> <td>Reserved</td> </tr> <tr> <td>101b</td> <td>Block Read or Write</td> </tr> <tr> <td>111b-110b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	000b	Quick Read or Write	001b	Byte Read or Write	010b	Byte Data Read or Write	011b	Word Data Read or Write	100b	Reserved	101b	Block Read or Write	111b-110b	Reserved
Bits	Definition																
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010b	Byte Data Read or Write																
011b	Word Data Read or Write																
100b	Reserved																
101b	Block Read or Write																
111b-110b	Reserved																

1	Kill . Read-write. Reset: 0. Stop the current host transaction in process.
0	InterruptEnable . Read-write. Reset: 0. 1=Enable the generation of interrupts on the completion of current host transaction.

SMBUSx03 SMBusHostCmd

Bits	Description
7:0	SMBusHostCmd . Read-write. Reset: 0. This field contains the data transmitted in the command field of SMBus host transaction.

SMBUSx04 SMBusAddress

Bits	Description
7:1	SMBusAddr . Read-write. Reset: 0. This field contains the 7-bit address of the target slave device.
0	SMBusRdWr . Read-write. Reset: 0. 0=Execute a Write command. 1=Execute a Read command.

SMBUSx05 SMBusData0

Bits	Description
7:0	SMBusData0 . Read-write. Reset: 0. This register should be programmed with a value to be transmitted in the data 0 field of an SMBus host interface transaction. For Block Write commands, the count of the memory should be stored in this field. The value of this register is loaded into the block transfer count field. A valid value for block command count is between 1 and 32. For block reads, count received from SMBus device is stored here.

SMBUSx06 SMBusData1

Bits	Description
7:0	SMBusData1 . Read-write. Reset: 0. This register should be programmed with a value to be transmitted in the data 1 field of an SMBus host interface transaction. When (SMBUSx14[SMBusPoll2Byte]==1) & ((SMBUSx02[SMBusProtocol]==Byte Read/Write) (SMBUSx02[SMBusProtocol]==Byte Data Read/Write)), this register is used as the data field in the second transaction.

SMBUSx07 SMBusBlockData

Bits	Description
7:0	SMBusBlockData . Read-write. Reset: 0. This register is used to transfer data into or out of the block data storage array.

SMBUSx08 SMBusSlaveControl

Bits	Description
7	ClrEcSemaphore . Read-write; Cleared-by-hardware. Reset: 0. Write 1 to clear EcSemaphore bit. Writing 0 has no effect.
6	EcSemaphore . Read-write. Reset: 0. Write 1 to set this bit. This bit can only be set when HostSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit
5	ClrHostSemaphore . Read-write; Cleared-by-hardware. Reset: 0. Write 1 to clear HostSemaphore bit. Writing 0 has no effect.
4	HostSemaphore . Read-write. Reset: 0. Bits 4 and 6 are meant to be used as software semaphore between the host and embedded controller. When both host and IMC want to use the same resource, they can write to these semaphore bits first, followed by a read. If the read returns a 1 in the semaphore bit, it means it has established the semaphore first. Write 1 to set this bit. This bit can only be set when EcSemaphore is clear. Writing 0 has no effect. Reading returns the value of this bit.
3	SMBusAlertEnable . Read-only. Reset: 0. Enable the generation of an interrupt or resume event on the assertion of AMBALERT_ signal. (This function is not supported).
2	SMBusShadow2En . Read-write. Reset: 0. Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 2 register.
1	SMBusShadow1En . Read-write. Reset: 0. Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the SMBus Shadow 1 register.
0	SlaveEnable . Read-write. Reset: 0. Enable the generation of an interrupt or resume event upon an external SMBus master generating a transaction with an address that matches the host controller slave port of 10h, a command field that matches the SMBus slave control register, and a match of corresponding enabled events.

SMBUSx09 SMBusShadowCmd

Bits	Description
7:0	SMBusShadowCmd . Read-write. Reset: 0. This field contains the command value that was received during an external SMBus master access whose address field matched the host slave address (10h) or one of the slave shadow ports.

SMBUSx0A SMBusSlaveEvent

Bits	Description
15:0	SMBusSlaveEvent . Read-write. Reset: 0. This field contains data bits used to compare against incoming data to the SMBus Slave Data register. When a bit in this register is 1 and a corresponding bit in SMBus Slave register is set, then an interrupt or resume event is generated if the command value matches the value in the SMBus slave control register and the access was to SMBus host address 10h.

SMBUSx0C SlaveData

Bits	Description
15:0	SlaveData . Read-write. Reset: 0. This field contains the data value which was transmitted during an external SMBus master access whose address field matched one of the slave shadow port addresses or the SMBus host controller slave port address of 10h.

SMBUSx0E SMBusTiming

Bits	Description
7:0	SMBusTiming . Read-write. Reset: B0h. This register controls the frequency on the SMBUS. The formula to calculate the frequency is: Frequency = 66 MHz/(SMBusTiming * 4).

SMBUSx10 I2CbusConfig

Bits	Description
7:4	I2CRevision . Read-write. Reset: 0. Sm bus controller revision.
3:1	Reserved.
0	I2CbusInterrupt . Read-write. Reset: 0. 0=SMI#. 1=IRQ.

SMBUSx11 I2CCommand

Bits	Description
7:0	I2Ccommand . Read-write. Reset: 0. I2C Host Slave Command. This value specifies the command value to be matched for I2C master accesses to the I2Ccontroller host slave interface.

SMBUSx12 I2CShadow1

Bits	Description
7:1	I2CslaveAddr1 . Read-write. Reset: 0. SMBus Slave Address for shadow port 1. This value specifies the address used to match against incoming I2C addresses for Shadow port 1.
0	ReadWriteShadowPort1 . Read-write. Reset: 0. This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction. 0=Write command. 1=Read command.

SMBUSx13 I2Cshadow2

Bits	Description
7:1	I2CslaveAddr2 . Read-write. Reset: 0. SMBus Slave Address for shadow port 2. This value specifies the address used to match against incoming I2C addresses for Shadow port 2.
0	ReadWriteShadowPort2 . Read-write. Reset: 0. This bit must be programmed to 0 because I2C slave controller only responds to Word Write Transaction. 0=Write command. 1=Read command.

SMBUSx14 SMBusAutoPoll

Bits	Description												
7	SMBusPoll2Byte . Read-write. Reset: 1. When set, if ((SMBUSx02[SMBusProtocol]==Byte Read/Write) (SMBUSx02[SMBusProtocol]==Byte Data Read/Write)), the last command will be performed twice at each polling interval. SMBUSx06 [SMBusData1] contains data transmitted and retrieved from the second transaction. SMBUSx17 [SMBusHostCmd2] contains data transmitted in the command field in the second transaction.												
6:4	Reserved.												
3:1	SMBusPollPeriod . Read-write. Reset: 2h. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>poll every 1/16 second</td> </tr> <tr> <td>001b</td> <td>poll every 1/8 second</td> </tr> <tr> <td>010b</td> <td>poll every 1/ 4 second</td> </tr> <tr> <td>011b</td> <td>poll every 1/ 2 second</td> </tr> <tr> <td>111b-100b</td> <td>poll every 1 second</td> </tr> </tbody> </table>	Bits	Definition	000b	poll every 1/16 second	001b	poll every 1/8 second	010b	poll every 1/ 4 second	011b	poll every 1/ 2 second	111b-100b	poll every 1 second
Bits	Definition												
000b	poll every 1/16 second												
001b	poll every 1/8 second												
010b	poll every 1/ 4 second												
011b	poll every 1/ 2 second												
111b-100b	poll every 1 second												
0	SMBusAutoPollEn . Read-write. Reset: 0. 1=SMBUS will periodically execute the last command whenever SMBUSx15 [SMBusCounter] expires. The polling interval is defined by [SMBusPollPeriod]. The purpose of this function is to use the SMBUS to read CPU temperature via TSI. Values in SMBUSx05 [SMBusData0] and SMBUSx06 [SMBusData1] are to be used for controlling the fan speed.												

SMBUSx15 SMBusCounter

Bits	Description
7:0	SMBusCounter . Read-only. This counter specifies the remaining time until the next read. The interval is based on SMBUSx14[SMBusPollPeriod] . For example, if SMBUSx14[SMBusPollPeriod] is 000b, then each tick in this counter represents 1/16 / 256 = 244us.

SMBUSx16 SMBusStop

Bits	Description
15:1	Reserved.
0	SMBusPausePoll . Read-write. Reset: 0. This is to be used as a semaphore mechanism by software to stop the next polling. If software wants to use the SMBUS for other purpose but the hardware has already been enabled (SMBUSx14[SMBusAutoPollEn] =1) to perform auto polling, software can halt the next polling by setting this bit to 1. If the halt is successful, this bit will return 1. If the HW has already started the polling operation at the same time software tries to set this bit, this bit will return 0. When the pending polling operation is finally complete, this bit will then get set. When this bit is set, polling counter will temporarily stop (not reset). It is now safe for software to access the SMBUS. Upon completion, software must restore the previous command in the appropriate register prior to setting this bit. software should also clear this bit so the counter can resume counting.

SMBUSx17 SMBusHostCmd2

Bits	Description
7:0	SMBusHostCmd2. Read-write. Reset: 0. This field contains the data transmitted in the command field in the second command when (SMBUSx14 [SMBusPoll2Byte]==1) and (SMBUSx02 [SMBus-Protocol]==Byte Data Read/Write).

3.26.8 IOAPIC Registers

IOAPIC configuration registers are accessed through IOAPIC base address defined by [PMx34\[IoApicEn\]](#):

- 1.Select the IOAPIC register space to be memory mapped or IO mapped through [PMx34\[IoApicMmIo\]](#).
- 2.Program the IOAPIC base address through [PMx34\[IoApicBaseAddr\]](#).
- 3.Enable IOAPIC decoding through [PMx34\[IoApicEnable\]](#).

IOAPICx00 IO Register Select Register

Bits	Description
31:8	Reserved.
7:0	IndirectAddressOffset . Read-write. Reset: 0. Indirect Address Offset to IO Window Register. It is used to determine which register is manipulated during an IO Window Register read/write operation.

IOAPICx10 IO Window Register

Bits	Description
31:0	IOWindow . Read-write. Reset: 0. Mapped by IOAPICx00 to the designated indirect access register.

IOAPICx10_x00 IOAPIC ID Register

This register is not used in IOxAPIC PCI bus delivery mode.

Bits	Description
31:24	ID . Read-write. Reset: 0. IOAPIC device ID. IF (PMx34[IoApicIdExtEn]==1) THEN This field is 8-bit wide. ELSE This field is 8-bit wide and [31:28] are reserved. ENDIF.
23:0	Reserved.

IOAPICx10_x01 IOAPIC Version Register

Bits	Description
31:24	Reserved.
23:16	MaxRedirectionEntries . Value: 17h. Indicates 24 entries [23:0]
15	PRQ . Value: 1. IRQ pin assertion supported
14:8	Reserved.
7:0	Version . Value: 21h. PCI 2.2 compliant

IOAPICx10_x02 IOAPIC Arbitration Register

This register is not used in IOxAPIC PCI bus delivery mode.

Bits	Description
31:28	Reserved.
27:24	ArbitrationID: Arbitration ID . Read-only. Reset: 0.
23:0	Reserved.

IOAPICx10_x[3E:10:step2] Redirection Table Entry [23:0]

Bits	Description																				
63:56	DestinationID . Read-write. Reset: 0. Bits [19:12] of the address field of the interrupt message																				
55:32	Reserved.																				
31:17	Reserved.																				
16	Mask . Read-write. Reset: 1. 1=Mask the interrupt injection at the input of this device. 0=Unmask.																				
15	TriggerMode . Read-write. Reset: 0. 0=Edge. 1=Level																				
14	RemoteIRR . Read-only. Reset: 0. Used for level triggered interrupts only. It is cleared by EOI special cycle transaction or write to EOI register. 1=Interrupt message is delivered.																				
13	InterruptPinPolarity . Read-write. Reset: 0. 0=High. 1=Low.																				
12	DeliveryStatus . Read-only. Reset: 0. 0=Idle. 1=Send Pending.																				
11	DestinationMode . Read-write. Reset: 0. 0=Physical. 1=Logical																				
10:8	DeliveryMode . Read-write. Reset: 0. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Fixed</td> <td>100b</td> <td>NMI</td> </tr> <tr> <td>001b</td> <td>Lowest Priority</td> <td>101b</td> <td>INIT</td> </tr> <tr> <td>010b</td> <td>SMI/PMI</td> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>011b</td> <td>Reserved</td> <td>111b</td> <td>ExtINT</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	Fixed	100b	NMI	001b	Lowest Priority	101b	INIT	010b	SMI/PMI	110b	Reserved	011b	Reserved	111b	ExtINT
Bits	Definition	Bits	Definition																		
000b	Fixed	100b	NMI																		
001b	Lowest Priority	101b	INIT																		
010b	SMI/PMI	110b	Reserved																		
011b	Reserved	111b	ExtINT																		
7:0	Vector . Read-write. Reset: 0. Interrupt vector associated with this interrupt input																				

IOAPICx20 IRQ Pin Assertion Register

Bits	Description
31:8	Reserved.
7:0	InputIrq . Read-write. Reset: 0. IRQ number for the requested interrupt. A write to this register will trigger an interrupt associated with the redirection table entry referenced by the IRQ number. Currently the redirection table has 24 entries. Writes with IRQ number greater than 17h have no effect.

IOAPICx40 EOI Register

Bits	Description
31:8	Reserved.
7:0	Vector . Write-only. Reset: 0. Interrupt vector. A write to this register will clear the remote IRR bit in the redirection table entry found matching the interrupt vector. This provides an alternate mechanism other than PCI special cycle for EOI to reach IOxAPIC.

3.26.9 LPC-ISA Bridge

3.26.9.1 Device 14h Function 3 (LPC Bridge) Configuration Registers

See 3.1 [Register Descriptions and Mnemonics] for a description of the register naming convention. See 2.7 [Configuration Space] for details about how to access this space.

D14F3x00 Device/Vendor ID

Bits	Description
31:16	DeviceID: Device Identifier. Value: 780Eh. This 16-bit field is assigned by the device manufacturer and identifies the type of device.
15:0	VendorID: Vendor Identifier. Read-only. Reset: 1022h.

D14F3x04 Status/Command

Bits	Description
31	DetectedParityError: Detected Parity Error. Read; write-1-to-clear. Reset: 0. 1=The FCH detects a parity error.
30	SignaledSystemError: Signaled System Error. Read; write-1-to-clear. Reset: 0. 1=The FCH detects a PCI address parity error.
29	ReceivedMasterAbort: Received Master Abort. Read; write-1-to-clear. Reset: 0. 1=The FCH acts as a PCI master and aborts a PCI bus memory cycle.
28	ReceivedTargetAbort: Received Target Abort. Read; write-1-to-clear. Reset: 0. 1=An FCH generated PCI cycle (the FCH is the PCI master) is aborted by a PCI target.
27	SignaledTargetAbort: Signaled Target Abort. Read; write-1-to-clear. Reset: 0. 1=The FCH signals target abort.
26:25	DeviceSelectTiming: Device Select Timing. Value: 1. Indicates DEVSEL# timing when performing a positive decode. DEVSEL# is asserted to meet the medium timing.
24	MasterDataParityError: Master Data Parity Error. Read; write-1-to-clear. Reset: 0. 1=The FCH detects PERR# asserted while acting as PCI master regardless whether PERR# was driven by the FCH or not.
23:21	Reserved.
20	CapabilitiesList: Capabilities List. Read-only. Reset: IF (D14F3x78[MsiOn]==1) THEN 1. ELSE 0. ENDIF.
19:10	Reserved.
9	FastBack2BackEnable: Fast Back-to-Back Enable. Value: 0.
8	SERREnable: SERR# Enable. Read-only. Reset: 0. 1=The FCH asserts SERR# when it detects an address parity error. 0=SERR# is not asserted.
7	SteppingControl: Stepping Control. Value: 0.
6	ParityErrorResponse: Parity Error Response. Read-write. Reset: 0. PERR# (Response) Detection Enable bit. 1=The FCH asserts PERR# when it is the agent receiving data and it detects a parity error. 0=PERR# is not asserted.
5	VGAPaletteSnoop: VGA Palette Snoop. Value: 0.

4	MemoryWriteAndInvalidateEnable: Memory Write and Invalidate Enable. Value: 0.
3	SpecialCycles: Special Cycles. Value: 1.
2	BusMaster: Bus Master. Read-only. Reset: 1. 1=Bus master enabled.
1	MemorySpace: Memory Space. Value: 1.
0	IOSpace: IO Space. Read-only. Reset: 1. This bit controls access to the IO space registers. 1=Enable access to the legacy IDE ports, and PCI bus master IDE IO registers are enabled.

D14F3x08 Revision ID/Class Code

Bits	Description
31:8	ClassCode: Class Code. Read-only. Reset: 60100h. Indicates an ISA bridge.
7:0	RevisionID: Revision ID. Value: 11h. Indicates the revision level of the chip design.

D14F3x0C Cache Line Size

Bits	Description
31:24	Bist: Read-only. Reset: 0. No BIST modes.
23:16	HeaderType: Header Type. Read-only. Reset: 80h. Identifies the type of the predefined header in the configuration space. The most significant bit is set to 1 to indicate a multifunction device.
15:8	LatencyTimer: Latency Timer. Read-only. Reset: 0. Specifies the value of the latency timer in units of PCICLKs.
7:0	CacheLineSize: Cache Line Size. Value: 0.

D14F3x10 Base Address Reg 0

Bits	Description
31:5	BaseAddress0[31:5]: Base Address 0. RAZ; write-only. Reset: 7F60000h. This register has an internal value used as base address for APIC memory space. Writing to the register changes its internal value. The default internal base address is FEC0_0000h.
4:0	BaseAddress0[4:0]. Value: 0.

D14F3x2C Subsystem ID and Subsystem Vendor ID

Bits	Description
31:16	SubsystemID: Subsystem ID. Write-once; Read. Reset: 780Eh.
15:0	SubsystemVendorID: Subsystem Vendor ID. Write-once; Read. Reset: 1022h.

D14F3x34 Capabilities Pointer

Bits	Description

31:8	Reserved.
7:0	CapabilitiesPointer: Capabilities Pointer. Read-only. Reset: IF (D14F3x78[MsiOn]==1) THEN 80h. ELSE 0. ENDIF. Specifies the starting address of the MSI capability register.

D14F3x40 PCI Control

Bits	Description
31:8	Reserved.
7	IntegratedEcPresent. Read-write. Reset: 0. This bit can only be programmed by IMC. 1=IMC is present.
6	EcSemaphore. Read-write. Reset: 0. This bit is writable by IMC and read by BIOS. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. IMC should read bit [BiosSemaphore] first to see if BIOS has taken ownership of the resource. If [BiosSemaphore] == 0, then IMC should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means IMC has successfully taken ownership of the resource. If this bit returns a 0 and [BiosSemaphore] returns a 1, then BIOS has taken ownership first. IMC should always clear this bit after it has completed its access to the resource.
5	BiosSemaphore. Read-write. Reset: 0. This bit is writable by BIOS and read by the IMC. This is used as the software semaphore mechanism between BIOS and IMC to see who can access the common resource. BIOS should read bit [EcSemaphore] first to see if IMC has taken ownership of the resource. If [EcSemaphore] == 0, then BIOS should write a 1 to this bit and then follow by a read to see if this bit is set. If this bit is set, it means BIOS has successfully taken ownership of the resource. If this bit returns 0 and [EcSemaphore] returns a 1, then IMC has taken ownership first. Software should always clear this bit after it has completed its access to the resource.
4:3	Reserved.
2	LegacyDmaEnable: Legacy DMA Enable. Read-write. Reset: 1. BIOS: See 2.15.4.1. 1=Enable LPC DMA cycle. Transfer size for channel 3-0 is 8 bits; Transfer size for channel 7-5 is 16 bits. 32-bit DMA is not supported.
1:0	Reserved.

D14F3x44 IO Port Decode Enable

Bits	Description
31	AdLibPortEnable: Ad-Lib Port Enable. Read-write. Reset: 0. Port enable for Ad-Lib port, 388h-389h. 1=Enable the IO range.
30	AcpiMicroControllerPortEnable: ACPI Micro-Controller Port Enable. Read-write. Reset: 0. Port enable for ACPI micro-controller port, 62h & 66h. 1=Enable the IO range.
29	KBCPortEnable: KBC Port Enable. Read-write. Reset: 0. Port enable for KBC port, 60h & 64h. 1=Enable the IO range.
28	GamePortEnable: Game Port Enable. Read-write. Reset: 0. Port enable for game port, 200h-20Fh. 1=Enable the IO range.
27	FDCPortEnable1: FDC Port Enable 1. Read-write. Reset: 0. Port enable for FDC port, 370h-377h. 1=Enable the IO range.

26	FDCPortEnable0: FDC Port Enable 0. Read-write. Reset: 0. Port enable for FDC port, 3F0h-3F7h. 1=Enable the IO range.
25	MSSPortEnable3: MSS Port Enable 3. Read-write. Reset: 0. Port enable for MSS port, F40h-F47h. 1=Enable the IO range.
24	MSSPortEnable2: MSS Port Enable 2. Read-write. Reset: 0. Port enable for MSS port, E80h-E87h. 1=Enable the IO range.
23	MSSPortEnable1: MSS Port Enable 1. Read-write. Reset: 0. Port enable for MSS port, 604h-60bh. 1=Enable the IO range.
22	MSSPortEnable0: MSS Port Enable 0. Read-write. Reset: 0. Port enable for MSS port, 530h-537h. 1=Enable the IO range.
21	MIDIPortEnable3: MIDI Port Enable 3. Read-write. Reset: 0. Port enable for MIDI port, 330h-331h. 1=Enable the IO range.
20	MIDIPortEnable2: MIDI Port Enable 2. Read-write. Reset: 0. Port enable for MIDI port, 320h-321h. 1=Enable the IO range.
19	MIDIPortEnable1: MIDI Port Enable 1. Read-write. Reset: 0. Port enable for MIDI port, 310h-311h. 1=Enable the IO range.
18	MIDIPortEnable0: MIDI Port Enable 0. Read-write. Reset: 0. Port enable for MIDI port, 300h-301h. 1=Enable the IO range.
17	AudioPortEnable3: Audio Port Enable 3. Read-write. Reset: 0. Port enable for audio port, 280h-293h. 1=Enable the IO range.
16	AudioPortEnable2: Audio Port Enable 2. Read-write. Reset: 0. Port enable for audio port, 260h-273h. 1=Enable the IO range.
15	AudioPortEnable1: Audio Port Enable 1. Read-write. Reset: 0. Port enable for audio port, 240h-253h. 1=Enable the IO range.
14	AudioPortEnable0: Audio Port Enable 0. Read-write. Reset: 0. Port enable for audio port, 230h-233h. 1=Enable the IO range.
13	SerialPortEnable7: Serial Port Enable 7. Read-write. Reset: 0. Port enable for serial port, 3E8h-3EFh. 1=Enable the IO range.
12	SerialPortEnable6: Serial Port Enable 6. Read-write. Reset: 0. Port enable for serial port, 338h-33Fh. 1=Enable the IO range.
11	SerialPortEnable5: Serial Port Enable 5. Read-write. Reset: 0. Port enable for serial port, 2E8h-2EFh. 1=Enable the IO range.
10	SerialPortEnable4: Serial Port Enable 4. Read-write. Reset: 0. Port enable for serial port, 238h-23Fh. 1=Enable the IO range.
9	SerialPortEnable3: Serial Port Enable 3. Read-write. Reset: 0. Port enable for serial port, 228h-22Fh. 1=Enable the IO range.
8	SerialPortEnable2: Serial Port Enable 2. Read-write. Reset: 0. Port enable for serial port, 220h-227h. 1=Enable the IO range.
7	SerialPortEnable1: Serial Port Enable 1. Read-write. Reset: 0. Port enable for serial port, 2F8h-2FFh. 1=Enable the IO range.
6	SerialPortEnable0: Serial Port Enable 0. Read-write. Reset: 0. Port enable for serial port, 3F8h-3FFh. 1=Enable the IO range.
5	ParallelPortEnable5: Parallel Port Enable 5. Read-write. Reset: 0. Port enable for parallel port, 7BCh-7BFh. 1=Enable the IO range.

4	ParallelPortEnable4: Parallel Port Enable 4. Read-write. Reset: 0. Port enable for parallel port, 3BCh-3BFh. 1=Enable the IO range.
3	ParallelPortEnable3: Parallel Port Enable 3. Read-write. Reset: 0. Port enable for parallel port, 678h-67Fh. 1=Enable the IO range.
2	ParallelPortEnable2: Parallel Port Enable 2. Read-write. Reset: 0. Port enable for parallel port, 278h-27Fh. 1=Enable the IO range.
1	ParallelPortEnable1: Parallel Port Enable 1. Read-write. Reset: 0. Port enable for parallel port, 778h-77Fh. 1=Enable the IO range.
0	ParallelPortEnable0: Parallel Port Enable 0. Read-write. Reset: 0. Port enable for parallel port, 378h-37Fh. 1=Enable the IO range.

D14F3x48 IO/Mem Port Decode Enable

Bits	Description
31:26	Reserved.
25	WideIO2Enable. Read-write. Reset: 0. Port enable for wide generic IO port 2 defined by D14F3x90 [IOBaseAddress2]. 1=Enable the IO range.
24	WideIO1Enable. Read-write. Reset: 0. Port enable for wide generic IO port 1 defined by D14F3x64 [IOBaseAddress1]. 1=Enable the IO range.
23	IOPortEnable6: IO port enable 6. Read-write. Reset: 0. Port enable for IO port FD60h-FD6Fh. 1=Enable the IO range.
22	IOPortEnable5: IO port enable 5. Read-write. Reset: 0. Port enable for IO port 4700h-470Bh. 1=Enable the IO range.
21	IOPortEnable4: IO port enable 4. Read-write. Reset: 0. Port enable for IO port 80h. 1=Enable the IO range.
20	MemPortEnable: Mem port enable. Read-write. Reset: 0. Port enable for 4K byte memory range defined in D14F3x4C [Memory Range] . 1=Enable the memory range.
19	IOPortEnable3: IO port enable 3. Read-write. Reset: 0. Port enable for IO port 580h-5BFh. 1=Enable the IO range.
18	IOPortEnable2: IO port enable 2. Read-write. Reset: 0. Port enable for IO port 500h-53Fh. 1=Enable the IO range.
17	IOPortEnable1: IO port enable 1. Read-write. Reset: 0. Port enable for IO port 480h-4BFh. 1=Enable the IO range.
16	IOPortEnable0: IO port enable 0. Read-write. Reset: 0. Port enable for IO port 400h-43Fh. 1=Enable the IO range.
15:8	SyncTimeoutCount: Sync Timeout Count. Read-write. Reset: FFh. When [SyncTimeoutCounterEnable] == 1, this is the number of LPC clocks that the state machine will wait during LPC data sync before aborting the cycle.
7	SyncTimeoutCounterEnable: Sync Timeout Counter Enable. Read-write. Reset: 0. 1=LPC sync timeout counter is enabled. 0=The counter is disabled. This counter is used to avoid a deadlock condition if an LPC device drives sync forever. Timeout count is programmed in [SyncTimeoutCount]. Write 0 to this bit if an LPC device is extremely slow and takes more than 255 LPC clocks to complete a cycle.

6	RtcIORangePortEnable: RTC IO Range Port Enable. Read-write. Reset: 0. Port enable for RTC IO range 70h-73h. 1=Enable the IO range.
5	MemoryRangePortEnable: Memory Range Port Enable. Read-write. Reset: 0. Port enable for LPC memory target range defined by D14F3x60 [PCI Memory Address for LPC Target Cycles] . 1=Enable the memory range.
4	RomRange2PortEnable: ROM Range 2 Port Enable. Read-write. Reset: 0. Port enable for LPC ROM address range 2 defined by D14F3x6C [ROM Address Range 2] . 1=Enable the ROM range.
3	RomRange1PortEnable: ROM Range 1 Port Enable. Read-write. Reset: 0. Port enable for LPC ROM address range 1 defined by D14F3x68 [ROM Address Range 1] . 1=Enable the ROM range.
2	WideIO0Enable. Read-write. Reset: 0. Port enable for wide generic IO port defined by D14F3x64[IOBaseAddress0] . 1=Enable the IO range.
1	AlternateSuperIOConfigurationPortEnable: Alternate Super IO Configuration Port Enable. Read-write. Reset: 0. Port enable for alternate Super IO configuration port, 4Eh-4Fh. 1=Enable the IO range.
0	SuperIOConfigurationPortEnable: Super IO Configuration Port Enable. Read-write. Reset: 0. Port enable for Super IO configuration port, 2Eh-2Fh. 1=Enable the IO range.

D14F3x4C Memory Range

Bits	Description
31:12	BaseAddress: Base Address. Read-write. Reset: 0. Specifies a 4K byte memory range from {Base Address, 000h} to {Base Address, FFFh}. The range is enabled by D14F3x48[MemPortEnable] .
11:0	Reserved.

D14F3x[5C,58,54,50] ROM Protect 3, 2, 1, 0

These registers specify different ROM ranges to be protected. [SPIx1D\[SpiProtectEn0\]](#) enables the protection ranges. The addresses are within the defined ROM range if:

{RomBase, 000_0000_0000b} <= address[31:0] <= ({RomBase, 000_0000_0000b} + {0_0000_0000_0000b, RomOffset, 11_1111_1111b}).

For host, these registers can only be written once after hardware reset; Subsequent writes to it have no effect. For IMC, these registers are always read-writable.

Bits	Description
31:11	RomBase: ROM Base. Read; write-once. Reset: 0.
10:2	RomOffset: ROM Offset. Read; write-once. Reset: 0.
1	ReadProtect: Read Protect. Read; write-once. Reset: 0. 1=The memory range defined by this register is read-protected and reading any location in the range returns FFFF_FFFFh.
0	WriteProtect: Write Protect. Read; write-once. Reset: 0. 1=The memory range defined by this register is write-protected and writing to the range has no effect.

D14F3x60 PCI Memory Address for LPC Target Cycles

This register contains the upper 16 bits of the start and end address of the LPC memory target range. The lower 16 bits of the start address are considered 0s. The lower 16 bits of the end address are considered 1s. This range can be enabled or disabled using [D14F3x48\[MemoryRangePortEnable\]](#).

Bits	Description
31:16	MemoryEndAddress: Memory End Address. Read-write. Reset: 0. Specifies the upper 16 bits of the end address of the LPC target memory range.
15:0	MemoryStartAddress: Memory Start Address. Read-write. Reset: 0. Specifies the upper 16 bits of the start address of the LPC target memory range.

D14F3x64 PCI IO base Address for Wide Generic Port

Bits	Description
31:16	IOBaseAddress1: IO Base Address 1. Read-write. Reset: 0. 16-bit PCI IO base address for wide generic IO port range. This function is enabled by D14F3x48[WideIO1Enable] . If D14F3x74[AlternativeWideIO1RangeEnable] == 1, the range is 16 bytes; else the range is 512 bytes.
15:0	IOBaseAddress0: IO Base Address 0. Read-write. Reset: 0. 16-bit PCI IO base address for wide generic IO port range. This function is enabled by D14F3x48[WideIO0Enable] . If D14F3x74[AlternativeWideIO0RangeEnable] == 1, the range is 16 bytes; else the range is 512 bytes.

D14F3x68 ROM Address Range 1

This register contains the upper 16 bits of the start and end address of the ROM address range 1. The lower 16 bits of the start address are considered 0s. The lower 16 bits of the end address are considered 1s. This range can be enabled or disabled using [D14F3x48\[RomRange1PortEnable\]](#). This register is used for both LPC and SPI flash.

Bits	Description
31:16	RomEndAddress1: ROM End Address 1. Read-write. Reset: 0Fh. Specifies the upper 16 bits of the end address of the ROM memory address range 1. If the strap is disabled, the reset value is 0h.
15:0	RomStartAddress1: ROM Start Address 1. Read-write. Reset: 08h. Specifies the upper 16 bits of the start address of the ROM memory address range 1. If the strap is disabled, the reset value is 00h.

D14F3x6C ROM Address Range 2

This register contains the upper 16 bits of the start and end address of the ROM address range 2. The lower 16 bits of the start address are considered 0s. The lower 16 bits of the end address are considered 1s. This range can be enabled or disabled using [D14F3x48\[RomRange2PortEnable\]](#). This register is used for both LPC and SPI flash.

Bits	Description
31:16	RomEndAddress2: ROM End Address 2. Read-write. Reset: FFFFh. Specifies the upper 16 bits of the end address of the ROM memory address range 2. If the strap is disabled, the reset value is 00h.
15:0	RomStartAddress2: ROM Start Address 2. Read-write. Reset: FFF8h. Specifies the upper 16 bits of the start address of the ROM memory address range 2. If the strap is disabled, the reset value is 00h.

D14F3x74 Alternative Wide IO Range Enable

Bits	Description
31:4	Reserved.
3	AlternativeWideIO2RangeEnable: Alternative Wide IO 2 Range Enable. Read-write. Reset: 0. This bit is similar to bit [AlternativeWideIO0RangeEnable], but it applies to the IO range defined by D14F3x90[IOBaseAddress2] . See bit [AlternativeWideIO0RangeEnable] for detailed description.
2	AlternativeWideIO1RangeEnable: Alternative Wide IO 1 Range Enable. Read-write. Reset: 0. This bit is similar to bit [AlternativeWideIO0RangeEnable], but it applies to the IO range defined by D14F3x64[IOBaseAddress1] . See bit [AlternativeWideIO0RangeEnable] for detailed description.
1	Reserved.
0	AlternativeWideIO0RangeEnable: Alternative Wide IO 0 Range Enable. Read-write. Reset: 0. 0=Wide IO range defined by D14F3x64[IOBaseAddress0] is 512 bytes. 1=The range is 16 bytes. To use this feature, address in D14F3x64[IOBaseAddress0] must be aligned to 16 bytes, i.e., bits[3:0] must be 0. If the address is not aligned to 16 bytes, the IO range is from address[15:0] to {address[15:4], 0xF}.

D14F3x78 Miscellaneous Control Bits

Bits	Description
31:9	Reserved.
7	AllowHostInDma. Read-write. Reset: 1. 1=Allow Host to access LPC if ACPI has not given GNT to LPC during DMA transfer. 0=DMA hold LPC even ACPI has not given GNT to LPC during DMA transfer.
6	GateWrongRx. Read-write. Reset: 0. 1=Allow AltRxByteCount to be 0.
5	GateSpiAccessDis. Read-write. Reset: 0. 1=Pass ROM access to SPI even if it is strapped as LPC.
4	SMMWriteRomEn. Read-write. Reset: 1. 1=Enable ROM access in SMM mode.
3	LDRQ1. Read-write. Reset: 0. BIOS: See 2.15.4.1 . 1=Enable LDRQ1# on LPC bus.
2	LDRQ0. Read-write. Reset: 0. BIOS: See 2.15.4.1 . 1=Enable LDRQ0# on LPC bus.
0	NoHog: No Hog. Read-write. Reset: 1. BIOS: See 2.15.4.1 . 1=The internal bus is not locked by LPC bridge during a slave access (eg. LPC DMA fetch). 0=LPC may hold the internal bus during a DMA transfer.

D14F3x7C TPM

Bits	Description
31:14	Reserved.
13	TpmBufferEn. Read-write. Reset: 0. 1=Enable TPM buffer. 0=Disable TPM buffer.
12	TpmPfetchEn. Read-write. Reset: 0. 1=Enable TPM burst read. 0=Disable TPM burst read.
11	LpcClk1IsGpio. Read-write. Reset: 1. 1=Treat LpcClk1 as GPIO. 0=Treat LpcClk1 as LpcClk1.
10	GpioLpcClk1Out. Read-write. Reset: 0. Control GpioLpcClk1 output value.

9	GpioLpcClk1OeB . Read-write. Reset: 1. 1=disable GpioLpcClk1 output. 0=Enable GpioLpcClk1 output.										
8	GpioLpcClk1 . Read-only; S3-check-exclude. Reset: X. Status of LpcClk1 port.										
7	WiderTpmEn . Read-write. Reset: 0. 1=Force logic to decode FED4_xxxh as TPM cycles instead of FED4_0xxxh, FED4_1xxxh, FED4_2xxxh, FED4_3xxxh, and FED4_4xxxh.										
6:5	TmkbcSel . Read-write. Reset: 0. Select which one of the four sets of TMKBC registers specified in D14F3x84 , D14F3x88 , D14F3x8C are accessed. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>set 0</td> </tr> <tr> <td>01b</td> <td>set 1</td> </tr> <tr> <td>10b</td> <td>set 2</td> </tr> <tr> <td>11b</td> <td>set 3</td> </tr> </tbody> </table>	Bits	Definition	00b	set 0	01b	set 1	10b	set 2	11b	set 3
Bits	Definition										
00b	set 0										
01b	set 1										
10b	set 2										
11b	set 3										
4	TmkbcSet . Write-once. Reset: 0. 1=All TMKBC address/remap registers cannot be changed until the next reset.										
3	TmkbcEnable . Read-write. Reset: 0. 1=Enable the TMKBC function.										
2	TpmLegacy . Read-write. Reset: 0. 1=Enable decoding of legacy TPM addresses: IO addresses 7Eh/7Fh and EEh/EFh.										
0	Tpm12En . Read-write. Reset: 0. 1=Enable decoding of TPM cycles defined in TPM1.2 spec. See the addresses defined in [TpmAmd]. Note that this bit and [TpmLegacy] are independent bits; they respectively turn on decoding of different TPM addresses.										

D14F3x84 TMKBC_BaseAddrLow

Bits	Description
31:7	TmkbcBaseAddrLow . Read-write. Reset: 0. This register defines the lower 32 bit memory address used for the TMKBC function. There are actually four sets of such mapping. The selection is controlled by D14F3x7C [TmkbcSel].
6	MaskBits13thru8 . Read-write. Reset: 0. Defines whether TMKBC address bits [13:8] are masked as do-not-care bits. 1=Masked. 0=No mask.
5	MaskBits12thru8 . Read-write. Reset: 0. Defines whether TMKBC address bits [12:8] are masked as do-not-care bits. 1=Masked. 0=No mask.
4	MaskBits11thru8 . Read-write. Reset: 0. Defines whether TMKBC address bits [11:8] are masked as do-not-care bits. 1=Masked. 0=No mask.
3	MaskBits10thru8 . Read-write. Reset: 0. Defines whether TMKBC address bits[10:8] are masked as do-not-care bits. 1=Masked. 0=No mask.
2	Addr64 . Read-write. Reset: 0. Defines whether the TMKBC address is 32 or 64 bits. 1=The address is 64-bit. 0=The address is 32-bit.
1:0	Reserved.

D14F3x88 TMKBC_BaseAddrHigh

Bits	Description
31:0	TmkbcBaseAddrHigh. Read-write. Reset: 0. If D14F3x84[Addr64] == 1, this register defines the upper 32 bit memory address used for the TMKBC function. If D14F3x84[Addr64] == 0, this register has no meaning. There are actually four sets of such mapping. The selection is controlled by D14F3x7C[TmkbcSel] .

D14F3x8C TMKBC_Remap

Bits	Description
31:16	Reserved.
15:8	TmkbcRemap. Read-write. Reset: 0. This register defines the remap address [15:8] on the LPC bus. There are actually four sets of such mapping. The selection is controlled by D14F3x7C[TmkbcSel] .
7:0	Reserved.

D14F3x90 Wide IO 2

Bits	Description
31:16	Reserved.
15:0	IOBaseAddress2: IO Base Address 2. Read-write. Reset: 0. 16-bit PCI IO base address for wide generic IO port range. This function is enabled by D14F3x48[WideIO2Enable] . If D14F3x74[AlternativeWideIO2RangeEnable] == 1, the range is 16 bytes; else, the ranges is 512 bytes.

D14F3x98 EC_LPC_Cntrl

Bits	Description
31:9	Reserved.
8	EcHoldLpc. Read-write. Reset: 0. 1=IMC holds the LPC bridge and host cannot access LPC.
7:1	Reserved.
0	HostHoldLpc. Read-write. Reset: 0. 1=Host holds the LPC bridge and prevents IMC from accessing LPC.

D14F3xA0 SPI Base_Addr

Bits	Description
31:6	SpiBaseAddr[31:6]. Read-write. Reset: 0. BIOS: See 2.15.4 . This register specifies the MMIO base address for the SPI ROM controller registers. See 3.26.9.2 [SPI Registers] .
5:4	Reserved.
3	RouteTpm2Spi. Read-write. Reset: 0. 1=TPM cycles are routed to SPI bus with TPM_SPI_CS# asserted.

2	Reserved.
1	SpiRomEnable . Read-write. Reset: 1. 1=SPI ROM is enabled if chip is strapped to SPI ROM. 0=SPI ROM is disabled.
0	Reserved.

D14F3xA4 EC_PortAddress

Bits	Description
31:16	Reserved.
15:1	EcPortAddr15_1 . IF (D14F3xB8[EcPortHostAccessEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 17h. If this field is non-zero, [EcPortActive] is set to 1, and an IO cycle from host has address[15:1] == EcPortAddr15_1, the cycle is routed to IMC.
0	EcPortActive . Read-write. Reset: 1. 1=LPC can decode the address specified in [EcPortAddr15_1]. 0= LPC ignores it.

D14F3xB0 RomDmaSrcAddr

Bits	Description
31:6	DmaStartAddr . Read-write. Reset: 0. Specifies the starting DMA address to read from the ROM. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT code quicker.
5:0	Reserved.

D14F3xB4 RomDmaDstAddr

Bits	Description
31:6	DmaDstAddr . Read-write. Reset: 0. Specifies the target DMA address to be written in the system memory. Note this is not the same as the legacy DMA function. This is meant to be used by BIOS to fetch BOOT code quicker.
5:0	Reserved.

D14F3xB8 RomDmaControl/EcControl/HostControl

Bits	Description
31:30	Reserved.
29	PrefetchMissEnHost . Read-write. Reset: 1. 1=Force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for host.
28	PrefetchArbNoSwitch . Read-write. Reset: 1. 1=Only allow prefetch.
27	T_start_fix . Read-write. Reset: 0. BIOS: 1. 1=Enable hand-instance of the pulse generator; allow LPCCLK0/LPCCLK1 to stop under ClkRun# protocol.

26	DisableSpiInSleep. Read-write. Reset: 0. BIOS: 1. 1=SPI signals (SpiCs#, SpiDin, SpiDout, SpiWp#, SPiHold#) are driven to low when IMC is not enabled in S3 or S5 and PwrGood goes to low. 0=SPI signals (SpiCs#, SpiDin, SpiDout, SpiWp#, SPiHold#) are left high when IMC is not enabled in S3 or S5 and PwrGood goes to low.
25	LpcBusPullUpEn. Read-write. Reset: 0. BIOS: 1. 1=Leave pull-up for LFrame#, LDrq# to be enabled in S0 and disabled in S3/S5 if IMC is not enabled. 0=Force the pull-up for LFrame#, LDrq# to be disabled.
24	PrefetchEnSpiFromHost. Read-write. Reset: 0. BIOS: 1. This is for performance enhancement purpose. 1=SPI controller prefetches from the flash on behalf of the host.
23	PrefetchEnSpiFromUSB. Read-write. Reset: 0. BIOS: 1. This is for performance enhancement purpose. 1=SPI controller prefetches from the flash on behalf of USB3 controller.
22	PrefetchEnSel. Read-write. Reset: 1. 0=Prefetch only the address of the read request that is on the 4 byte boundary. 1=Prefetch only the address of the read request that is on the 8 byte boundary.
21	PrefetchMissEn. Read-write. Reset: 1. 1=Force the on-going prefetch to stop if the address of the pending read is not within the prefetch range for IMC.
20	EcReadOfSwitch. Read-write. Reset: 0. 1=Upper 16 bits of IMC read request address are specified in D14F3xC4 [EcRomRdOffset] . 0=Upper 16 bits of IMC read request address are specified by auto-rom detection logic, see D14F3xCC [AutoRomCfg] for auto-rom detection.
19	EcPortHostAccessEn. Read-write. Reset: 0. 1=Allow host to program D14F3xA4 [EC_PortAddress] .
18	PrefetchEnSpiFromEC. Read-write. Reset: 0. 1=Enable prefetching a cache line (64 bytes) when IMC reads code from the SPI ROM. This bit can be programmed by IMC only. This bit should be set to 1 by IMC firmware.
17	SpiHoldOnGevent9Dis. Read-write. Reset: 0. 0=GEVENT9 and ROM_RST# are configured to SPI_HOLD# and SPI_WP# function. 1=GEVENT9 and ROM_RST# are not configured to SPI_HOLD# and SPI_WP# function.
16	ECPageProtect. Read-write. Reset: 0. Enable protection of the IMC page registers. 1=D14F3x[C7:BC] are only read/writable by IMC; host writes have no effect and host reads return 0. 0=D14F3x[C7:BC] are read/writable by both IMC and host.
15:6	DWCount. Read-write. Reset: 0. This register specifies the number of cache lines (64 bytes) to be fetched from the ROM when DMA is used.
5:3	Reserved.
2	RomcpSupportAbRetry. Read-write. Reset: 1. 0=ROM copy doesn't support AB retry. 1=ROM copy supports AB retry.
1	DmaErrorStatus. Read; write-1-to-clear. Reset: 0. 1=Previous transfer has error. 0=Previous transfer has completed successfully.
0	DmaStart. Read; write-1-only; cleared-by-hardware. Reset: 0. Writing 1 to this bit causes LPC bridge to start the DMA function, with starting addresses defined by D14F3xB0 and D14F3xB4 . This bit returns the status of the DMA transfer. A return value of 0 means the DMA transfer is complete. A return value of 1 means the DMA transfer is running.

D14F3xC0 EcRomWrOffset

Bits	Description
31:0	EcRomWrOffset. Read-write. Reset: FFF20000h. Specifies the address of IMC write requests. If D14F3xB8[ECPageProtect] == 1, this register returns its current value. If D14F3xB8[ECPageProtect] == 0, this register returns all 0s.

D14F3xC4 EcRomRdOffset

Bits	Description
31:0	EcRomRdOffset. Read-write. Reset: FFF20000h. Specifies the address of IMC read requests. If D14F3xB8[ECPageProtect] == 1, this register returns its current value. If D14F3xB8[ECPageProtect] == 0, this register returns all 0s.

D14F3xC8 ClientRomProtect

Bits	Description
31	AutoSizeStart. Read; write-1-only. Reset: 0. IF (READ) THEN This bit returns the status of Auto-Rom detection. 1=The AutoRom detection is done. 0=AutoRom detection is not done yet. ELSE 1=Trigger AutoRom detection. 0=No effect. ENDIF.
30:8	Reserved.
7:3	Reserved. Read-write.
2	UsbRomProtectEn. Read-write. Reset: 0. 1=Software cannot access USB portion of the flash.
1	Reserved.
0	EcRomPortectEn. Read-write. Reset: 0. 1=Software cannot access IMC portion of the flash.

D14F3xCC AutoRomCfg

Bits	Description										
31:2	AutoRomAddr. Read-only. Reset: X. Based on the setting of AutoAddressSelect, this register returns the address value detected by the auto-rom detection logic (EcCodeOffset, XhciRomOffset).										
1:0	AutoAddressSelect. Read-write. Reset: 0. The FCH auto detects the IMC and USB3 firmware locations. After detection, it writes the address pointers of each firmware onto bits[31:2]. This field configures which address to be returned on bits[31:2]. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Reserved</td> </tr> <tr> <td>01b</td> <td>IMC</td> </tr> <tr> <td>10b</td> <td>Reserved</td> </tr> <tr> <td>11b</td> <td>USB XHCI</td> </tr> </tbody> </table>	Bits	Definition	00b	Reserved	01b	IMC	10b	Reserved	11b	USB XHCI
Bits	Definition										
00b	Reserved										
01b	IMC										
10b	Reserved										
11b	USB XHCI										

D14F3xD0 ClkCntrl

Bits	Description										
31	ClkRunEn. Read-write. Reset: 0. BIOS: 1. 1=ClkRun function is enabled and LPCCLK0/LPCCLK1 can be stopped. 0=ClkRun function is disabled and LPCCLK0/LPCCLK1 can be running all the time.										
30:24	ClkRunDlyCounter. Read-write. Reset: 8h. Specifies the amount of clocks to be extended before stopping the LPCCLK0/LPCCLK1.										
23	Reserved. Reset: 1.										
22	Lclk1ClkrunOvrid. Read-write. Reset: 1. 0=LPCCLK1 will be functioning with CLKRUN protocol. 1=LPCCLK1 will be forced running.										
21	Lclk0ClkrunOvrid. Read-write. Reset: 1. 0=LPCCLK0 will be functioning with CLKRUN protocol. 1=LPCCLK0 will be forced running.										
20:15	Reserved. Reset: 3Fh.										
14	Lclk1En. Read-write. Reset: 1. 0=LPCCLK1 will be forced to stop. 1=LPCCLK1 will be functioning with CLKRUN protocol.										
13	Lclk0En. Read-write. Reset: 1. 0=LPCCLK0 will be forced to stop. 1=LPCCLK0 will be functioning with CLKRUN protocol.										
12:3	Reserved. Reset: 3E0h.										
2	ClkRunDisable. Read-write. Reset: 0. 1=CLKRUN# assertion is not allowed; In other words, the internal CLKRUN# coming from LPC is always 0, which means ClkRun logic can never stop the clock.										
1:0	ClkGateCntrl. Read-write. Reset: 2h. These two bits control whether the LPC module allows clock gating to the internal 66MHz core clock. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable the clock gating function</td> </tr> <tr> <td>01b</td> <td>Wait 16 clocks before allowing clock gating to the LPC module</td> </tr> <tr> <td>10b</td> <td>Wait 64 clocks before allowing clock gating to the LPC module</td> </tr> <tr> <td>11b</td> <td>Wait 256 clocks before allowing clock gating to the LPC module</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable the clock gating function	01b	Wait 16 clocks before allowing clock gating to the LPC module	10b	Wait 64 clocks before allowing clock gating to the LPC module	11b	Wait 256 clocks before allowing clock gating to the LPC module
Bits	Definition										
00b	Disable the clock gating function										
01b	Wait 16 clocks before allowing clock gating to the LPC module										
10b	Wait 64 clocks before allowing clock gating to the LPC module										
11b	Wait 256 clocks before allowing clock gating to the LPC module										

D14F3xD4 ClkRunOption

Bits	Description
31:8	Reserved.
7:4	MinAssertion. Read-write. Reset: 4h. Specifies the minimum time of ClkRun# assertion. The unit is 30 ns.
3:1	Reserved.
0	ClkRunInputDly. Read-write. Reset: 0. 0=Delay 30 ns before capturing ClkRun# input. 1=Delay 60 ns before capturing ClkRun# input.

3.26.9.2 SPI Registers

SPI configuration registers are accessed through SPI base address specified by [D14F3xA0 \[SPI Base Addr\]](#). Software can communicate with the SPI ROM through the default memory or alternate program method:

- Memory access to the BIOS ROM address space is automatically handled by the hardware. The SPI ROM

controller translates the memory address onto the SPI bus and accesses the SPI ROM data. Any other commands besides memory read or memory write to the SPI ROM need to go through the alternate program method.

- In alternate program method, software needs to program the SpiOpCode, SpiAddress, TxByteCount, RxByteCount, put the data into the transmit FIFO, and then execute the command. The hardware communicates with the SPI ROM using these parameters. This alternate method basically allows software to issue any flash vendor specific commands such as ERASE and STATUS.

SPIx00 SPI_Cntrl0

Bits	Description																		
31	SpiBusy . Read-only; updated-by-hardware. Reset: 0. 0=SPI bus is idle. 1=SPI bus is busy.																		
30:29	SpiReadMode[2:1] . Read-write. Reset: 0. This field, along with SpiReadMode[0] below, combine to specify the SPI read mode: <table> <thead> <tr> <th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>Normal read (up to 33M)</td></tr> <tr> <td>001b</td><td>Reserved</td></tr> <tr> <td>010b</td><td>Dual IO (1-1-2)</td></tr> <tr> <td>011b</td><td>Quad IO (1-1-4)</td></tr> <tr> <td>100b</td><td>Dual IO (1-2-2)</td></tr> <tr> <td>101b</td><td>Quad IO (1-4-4)</td></tr> <tr> <td>110b</td><td>Normal read (up to 66M)</td></tr> <tr> <td>111b</td><td>Fast Read</td></tr> </tbody> </table>	Bits	Definition	000b	Normal read (up to 33M)	001b	Reserved	010b	Dual IO (1-1-2)	011b	Quad IO (1-1-4)	100b	Dual IO (1-2-2)	101b	Quad IO (1-4-4)	110b	Normal read (up to 66M)	111b	Fast Read
Bits	Definition																		
000b	Normal read (up to 33M)																		
001b	Reserved																		
010b	Dual IO (1-1-2)																		
011b	Quad IO (1-1-4)																		
100b	Dual IO (1-2-2)																		
101b	Quad IO (1-4-4)																		
110b	Normal read (up to 66M)																		
111b	Fast Read																		
28	SpiClkGate . Read-write. Reset: 0. 1=Skip the 8th SPI clock at the end data when doing read.																		
27	Reserved. Read-write. Reset: 1.																		
26:24	ArbWaitCount . Read-write. Reset: 7h. Specifies the amount of wait time the SPI controller asserts HOLD# before it should access the SPI ROM, under ROM sharing mode with the MAC.																		
23	SpiHostAccessRomEn . Read-write. Reset: 1. This is a clear-once protection bit; once it is cleared to 0 it cannot be set back to 1. 0=MAC cannot access BIOS ROM space (upper 512KB). 1=MAC can access BIOS ROM space.																		
22	SpiAccessMacRomEn . Read-write. Reset: 1. This is a clear-once protection bit. 0=Software cannot access MAC's portion of the ROM space (lower 512KB). 1=Software can access MAC's portion of the ROM space.																		
21	IllegalAccess . Read-only; updated-by-hardware. Reset: 0. 0=Legal index mode access. 1=Illegal index mode access.																		
20	FifoPtrClr . RAZ; write-1-only. Reset: 0. Writing 1 to this bit clears the internal FIFO pointer at SPIx0C[FifoPtr] .																		
19	SpiArbEnable . Read-write. Reset: 0. If a MAC is sharing the ROM with the FCH, both chips need to go through an arbitration process before either one can access the ROM. If MAC is not sharing the SPI ROM, BIOS should set this bit to 0 to speed up the SPI ROM access. 1=Enable the arbitration.																		
18	SpiReadMode[0] . Read-write. Reset: 0. Bit 0 of SpiReadMode. See the definition of SpiReadMode[2:1] in this register.																		
17	Reserved.																		
16	ExecuteOpCode . Write-1-only; cleared-by-hardware. Reset: 0. Write 1 to execute the transaction in the alternate program registers. This bit returns to 0 when the transaction is complete. If the command is an illegal command, the bit cannot be set and thereby cannot execute.																		

15:8	Reserved.
7:0	SpiOpCode . Read-write. Reset: 0. Specifies the SPI opcode in alternate program method.

SPIx04 SPI_RestrictedCmd

Bits	Description
31:24	RestrictedCmd3 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as RestrictedCmd0.
23:16	RestrictedCmd2 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as RestrictedCmd0.
15:8	RestrictedCmd1 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as RestrictedCmd0.
7:0	RestrictedCmd0 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. This specifies a restricted command issued by the MAC which is checked by the FCH. If the opcode issued by the MAC matches with this field and the address space is in the BIOS space, the SPI controller jams the entire interface as an attempt to stop that transaction.

SPIx08 SPI_RestrictedCmd2

Bits	Description
31:24	RestrictedCmdWoAddr2 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as [RestrictedCmdWoAddr0].
23:16	RestrictedCmdWoAddr1 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as [RestrictedCmdWoAddr0].
15:8	RestrictedCmdWoAddr0 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as SPIx04 [RestrictedCmd0] except that this field defines a restricted command that does not have address.
7:0	RestrictedCmd4 . IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. Same as SPIx04 [RestrictedCmd0].

SPIx0C SPI_Cntrl1

Bits	Description
31:24	ByteCommand . Read-write. Reset: 0. Specifies the command byte for the opcode transaction.
23:22	Reserved.
21:16	WaitCount . Read-write. Reset: 0. Specifies the time unit =15 ns * (WaitCount+1).
15:12	Reserved.

11	TrackMacLockEn . Read-write. Reset: 0. 1=The SPI controller locks the SPI from the MAC when it has detected a command from the MAC matching the value defined in SPIx10[MacLockCmd0] or SPIx10[MacLockCmd1] . 0=The SPI controller unlocks the bus when it has detected a command from the MAC matching the value defined in SPIx10[MacUnlockCmd0] or SPIx10[MacUnlockCmd1] .
10:8	FifoPtr . Read-only. Reset: 0. This specifies the internal pointer location, which can be cleared through SPIx00[FifoPtrClr] .
7:0	SpiParameters . Read-write. Reset: 0. This is the TX/RX FIFO port which can take up to 8 bytes. To send data to SPI ROM, software writes data into this port. To retrieve data that are received from the SPI ROM, software reads from this port.

SPIx10 SPI_CmdValue0

Bits	Description
31:24	MacUnlockCmd1 . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 4h. Same as MacUnlockCmd0
23:16	MacUnlockCmd0 . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 4h. This field is used to compare against the opcode sent out by the MAC. If SPIx0C[TrackMacLockEn]==1 , the controller unlocks the SPI bus for the MAC. In other words, access by the CPU is allowed again.
15:8	MacLockCmd1 . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 20h. Same as MacLockCmd0.
7:0	MacLockCmd0 . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 6h. This is used to compare against the opcode sent out by the MAC. If SPIx0C[TrackMacLockEn]==1 , the controller locks the SPI bus for the MAC. In other words, the MAC has the exclusive access to the ROM and access by the CPU is delayed until this is unlocked. This allows the MAC to do a certain sequence of operations without interruption.

SPIx14 SPI_CmdValue1

Bits	Description
31:24	RDSR . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 5h. This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDSR (read status register) command from the MAC.
23:16	RDID . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 9Fh. This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the RDID (read ID) command from the MAC.
15:8	WRDI . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 4h. This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WRDI (write disable) command from the MAC.
7:0	WREN . IF (SPIx00[SpiAccessMacRomEn]==0 SPIx00[SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 6h. This is used to compare against the opcode sent out by the MAC. This is a predefined value to decode for the WREN (write enable) command from the MAC.

SPIx18 SPI_CmdValue2

Bits	Description
31:24	BYTEWR. IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 2h. This is a predefined value to decode for the BYTEWR (byte write) command from the MAC.
23:16	Reserved.
15:8	FRead. IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: Bh. This is a predefined value to decode for the FRead (fast read) command from the MAC.
7:0	Read. IF (SPIx00 [SpiAccessMacRomEn]==0 SPIx00 [SpiHostAccessRomEn]==0) THEN Read-only. ELSE Read-write. ENDIF. Reset: 3h. This is a predefined value to decode for the Read (read byte) command from the MAC.

SPIx1C Reserved

Bits	Description
7:0	Reserved. Reset: FFh. Read-write.

SPIx1D Alt_SPI_CS

Bits	Description										
7	SpiCsDlySel. Read-write. Reset: 0. 1=125 ns minimum SPI_CS# de-assertion time. 0=75 ns minimum SPI_CS# de-assertion time.										
6	Reserved.										
5	SpiProtectLock. Read-write. Reset: 0. 1=bit 3, 4, and 5 are no longer writable.										
4	SpiProtectEn1. IF (SPIx1D [SpiProtectLock]==1) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=Enable SPI protection to prevent host from accessing IMC and USB3 space.										
3	SpiProtectEn0. IF (SPIx1D [SpiProtectLock]==1) THEN Read-only. ELSE Read-write. ENDIF. Reset: 0. 1=Enable SPI read/write protection ranges specified by D14F3x[5C,58,54,50] .										
2	WriteBufferEn. Read-write. Reset: 0. SPI write performance enhancement. 1=SPI bridge can take burst write from the host and transfer it to the SPI flash.										
1:0	AltSpiCsEn. Read-write. Reset: 0. These two bits enable the alternate SPI_CS#. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>select xSPI_CS#</td> </tr> <tr> <td>01b</td> <td>select xSPI_CS1#</td> </tr> <tr> <td>10b</td> <td>select xSPI_CS2#</td> </tr> <tr> <td>11b</td> <td>select xSPI_CS3#</td> </tr> </table>	Bits	Definition	00b	select xSPI_CS#	01b	select xSPI_CS1#	10b	select xSPI_CS2#	11b	select xSPI_CS3#
Bits	Definition										
00b	select xSPI_CS#										
01b	select xSPI_CS1#										
10b	select xSPI_CS2#										
11b	select xSPI_CS3#										

SPIx1E SpiExtRegIdx

Bits	Description
7:0	SPI_ExtReg_Idx . Read-write. Reset: 0. Specifies the offset of the extended SPI register to be read written from SPIx1F [SpiExtRegData] .

SPIx1F SpiExtRegData

Bits	Description
7:0	SPI_ExtReg_Data . Read-write. Reset: 00h. Specifies the read data or write data of the extended SPI register.

SPIx1F_x00 DDR_CMD

Bits	Description
7:0	DDR_CMD . Read-write. Reset: 3Bh. Specifies the command value to be used when host is doing a Dual Output Read. This is programmable to accommodate different opcodes.

SPIx1F_x01 QDR_CMD

Bits	Description
7:0	QDR_CMD . Read-write. Reset: 6Bh. Specifies the command value to be used when host is doing a Quad Output Read. This is programmable to accommodate different opcodes.

SPIx1F_x02 DPR_CMD

Bits	Description
7:0	DPR_CMD . Read-write. Reset: BBh. Specifies the command value to be used when host is doing a Dual IO High Performance Read. This is programmable to accommodate different opcodes.

SPIx1F_x03 QPR_CMD

Bits	Description
7:0	QPR_CMD . Read-write. Reset: EBh. Specifies the command value to be used when host is doing a Quad IO High Performance Read. This is programmable to accommodate different opcodes.

SPIx1F_x04 ModeByte

Bits	Description
7:0	ModeByte . Read-write. Reset:0. Bits [7:4] of this field control the length of the next Dual/Quad IO High Performance instruction through the inclusion or exclusion of the first byte instruction code. Bits [3:0] of this field are don't care bits ("x"). If ModeByte == Axh, then the device remains in Dual IO High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the instruction opcode. Whenever DPR_CMD or QPR_CMD is used, ModeByte is also sent out onto the SPI stream.

SPIx1F_x05 TxByteCount

Bits	Description
7:0	TxByteCount . Read-write. Reset: 0. Specifies the number of bytes to be sent to SPI ROM.

SPIx1F_x06 RxByteCount

Bits	Description
7:0	RxByteCount . Read-write. Reset: 0. Specifies the number of bytes to be received from the SPI ROM.

SPIx1F_x07 SPIDataFifoPtr

Bits	Description
7:0	SPIDataFiFoPtr . Read-only. Reset: 0. Specifies the current pointer of read/write Data FIFO.

SPIx20 SPI100 Enable

Bits	Description
0	UseSpi100 . Read-write. Reset: 0. BIOS: see 2.15.4.2 . 0=Use the old SPI engine; Do not support 100 MHz speed. 1=Use the new SPI100 engine; Support 100 MHz speed. The actual read speed also depends on SPIx22 .

SPIx22 SPI100 Speed Config

Bits	Description			
15:12	NormSpeedNew[3:0] . Read-write. Reset: 0011b . Configures the SPI bus normal speed in new SPI100 engine. If the command is not using TpmSpeed and FastSpeed, it will use NormSpeed.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	000b	66.66 MHz	100b	100 MHz
	001b	33.33 MHz	101b	Reserved
	010b	22.22 MHz	110b	Reserved
	011b	16.66 MHz	111b	800 KHz

11:8	FastSpeedNew[3:0] . Read-write. Reset: 0001b. Configures the SPI bus speed for the following command in new SPI100 engine: <ul style="list-style-type: none"> • FAST READ • DDR READ (1-1-2) • QDR READ (1-1-4) • DPR READ (1-2-2) • QPR READ (1-4-4) <table border="1"> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>66.66 MHz</td><td>100b</td><td>100 MHz</td></tr> <tr> <td>001b</td><td>33.33 MHz</td><td>101b</td><td>Reserved</td></tr> <tr> <td>010b</td><td>22.22 MHz</td><td>110b</td><td>Reserved</td></tr> <tr> <td>011b</td><td>16.66 MHz</td><td>111b</td><td>800 KHz</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	66.66 MHz	100b	100 MHz	001b	33.33 MHz	101b	Reserved	010b	22.22 MHz	110b	Reserved	011b	16.66 MHz	111b	800 KHz
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010b	22.22 MHz	110b	Reserved																		
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7:4	AltSpeedNew[3:0] . Read-write. Reset: 0001b. Configures the SPI bus speed for the AltOpCode mode in new SPI100 engine. <table border="1"> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>66.66 MHz</td><td>100b</td><td>100 MHz</td></tr> <tr> <td>001b</td><td>33.33 MHz</td><td>101b</td><td>Reserved</td></tr> <tr> <td>010b</td><td>22.22 MHz</td><td>110b</td><td>Reserved</td></tr> <tr> <td>011b</td><td>16.66 MHz</td><td>111b</td><td>800 KHz</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	66.66 MHz	100b	100 MHz	001b	33.33 MHz	101b	Reserved	010b	22.22 MHz	110b	Reserved	011b	16.66 MHz	111b	800 KHz
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001b	33.33 MHz	101b	Reserved																		
010b	22.22 MHz	110b	Reserved																		
011b	16.66 MHz	111b	800 KHz																		
3:0	TpmSpeedNew[3:0] . Read-write. Reset: 0011b. Configures the SPI bus speed for TPM read and write in new SPI100 engine. <table border="1"> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>000b</td><td>66.66 MHz</td><td>100b</td><td>100 MHz</td></tr> <tr> <td>001b</td><td>33.33 MHz</td><td>101b</td><td>Reserved</td></tr> <tr> <td>010b</td><td>22.22 MHz</td><td>110b</td><td>Reserved</td></tr> <tr> <td>011b</td><td>16.66 MHz</td><td>111b</td><td>800 KHz</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	66.66 MHz	100b	100 MHz	001b	33.33 MHz	101b	Reserved	010b	22.22 MHz	110b	Reserved	011b	16.66 MHz	111b	800 KHz
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010b	22.22 MHz	110b	Reserved																		
011b	16.66 MHz	111b	800 KHz																		

SPIx40 DDRCmdCode

Bits	Description
7:0	DDR_CMD . Read-write. Reset: 3Bh. This is the shadow register of SPIx1F_x00 .

SPIx41 QDRCmdCode

Bits	Description
7:0	QDR_CMD . Read-write. Reset: 6Bh. This is the shadow register of SPIx1F_x01 .

SPIx42 DPRCmdCode

Bits	Description
7:0	DPR_CMD . Read-write. Reset: BBh. This is the shadow register of SPIx1F_x02 .

SPIx43 QPRCmdCode

Bits	Description
7:0	QPR_CMD . Read-write. Reset: EBh. This is the shadow register of SPIx1F_x03 .

SPIx44 ModeByte

Bits	Description
7:0	ModeByte . Read-write. Reset: 0. This is the shadow register of SPIx1F_x04 .

SPIx45 CmdCode

Bits	Description
7:0	SpiOpCode . Read-write. Reset: 0. This is the shadow register of SPIx00[SpiOpCode] .

SPIx47 CmdTrigger

Bits	Description
7	Execute . Write-1-only; cleared-by-hardware. Reset: 0. This bit is the shadow register of SPIx00[ExecuteOpCode] .
6:0	Reserved.

SPIx48 TxByteCount

Bits	Description
7:0	TxByteCount . Read-write. Reset: 0. This is the shadow register of SPIx1F_x05 .

SPIx4B RxByteCount

Bits	Description
7:0	RxByteCount . Read-write. Reset: 0. This is the shadow register of SPIx1F_x06 .

SPIx4C SpiStatus

Bits	Description
31	SpiBusy . Read-only; updated-by-hardware. Reset: 0. 1=SPI bus is busy. 0=SPI bus is idle.
30:23	Reserved.
22:16	FiFoRdPtr . Read-only; updated-by-hardware. Reset: 0. The current Data FIFO read pointer.
15	Reserved.

14:8	FiFoWrPtr. Read-only; updated-by-hardware. Reset: 0. The current Data FIFO write pointer.
7:0	DoneByteCount. Read-only; updated-by-hardware. Reset: 0. Indicates how many bytes has been received or sent in the previous SPI transaction.

SPIx[C6:80] FIFO[70:0]

Bits	Description
7:0	FiFo. Read-write. Reset: 0. Contains the Data FiFo byte which is used in command mode to send or receive data.

3.26.10 High Precision Event Timer (HPET) Registers

HPET registers are accessed through two methods:

- Memory access through HPET base address defined by [PMx50 \[HPETEn\]](#):
 - Program the HPET base address through [PMx50\[HpetBaseAddress\]](#).
 - Enable HPET address decoding through [PMx50\[HpetDecodeEn\]](#).
- Memory mapped or IO mapped access through the AcpiMmio region. The HPET registers range from [PMx24\[AcpiMmioAddr\]+C00h](#) to [PMx24\[AcpiMmioAddr\]+CFFh](#). See [PMx24 \[AcpiMmioEn\]](#).

HPETx000 ID

Bits	Description
31:16	VendorID . Read-only. Reset: 1022h.
15	LegacyCap . Read-only. Reset: 1. Legacy replacement interrupt is supported.
14	Reserved.
13	CounterSizeCap . Read-only. Reset: 0. Main counter is 32-bits wide and cannot operate in 64-bit mode.
12:8	NumTmrCap . Read-only. Reset: 2h. Three timers are supported.
7:0	RevID . Read-only. Reset: 10h. Revision ID.

HPETx004 ClkPeriod

Bits	Description
31:0	CounterClkPeriod . Read-only; updated-by-hardware. Reset: 429B17Eh. Specifies the clock period of each HPET timer tick. HPET main counter runs at 14.31818 MHz. The unit is femtosecond (10^{-15} seconds). The value of this register can be modified through MISCx74 .

HPETx010 Config

Bits	Description
31:2	Reserved.
1	LegacyEn . Read-write. Reset: 0. 1=Timer0 interrupt goes to IRQ0 of PIC controller, INT2 of IOAPIC; Timer1 interrupt goes to IRQ8 of PIC controller, INT8 of IOAPIC.
0	TmrEn . Read-write. Reset: 0. 0=Pause main counter and disable all timer interrupts. 1=Allow main counter to run and allow timer interrupts if enabled.

HPETx020 Interrupt Status

Bits	Description
31:3	Reserved.
2	Tmr2IntrSts . IF (HPETx140[TmrIntTyp]==1) THEN Read; set-by-hardware; write-1-to-clear. ELSE Read-write. ENDIF. Reset: 0. 0=Timer2 interrupt is not active. 1=Timer2 interrupt is active. If Timer2 is set to edge-triggered mode, software should ignore this bit and always write 0 to this bit.

1	Tmr1IntrSts. IF (HPETx120[TmrIntTyp]==1) THEN Read; set-by-hardware; write-1-to-clear. ELSE Read-write. ENDIF. Reset: 0. 0=Timer1 interrupt is not active. 1=Timer1 interrupt is active. If Timer1 is set to edge-triggered mode, software should ignore this bit and always write 0 to this bit.
0	Tmr0IntrSts. IF (HPETx100[TmrIntTyp]==1) THEN Read; set-by-hardware; write-1-to-clear. ELSE Read-write. ENDIF. Reset: 0. 0=Timer0 interrupt is not active. 1=Timer0 interrupt is active. If Timer0 is set to edge-triggered mode, software should ignore this bit and always write 0 to this bit.

HPETx0F0 Main Counter

Bits	Description
63:32	Reserved.
31:0	MainCounter. Read-write. Reset: 0. Specified the HPET main counter, incremented by 1 on every clock. Counter should be written to only when it is halted.

HPETx1[4:0:Step2]0 Timer[2:0] Config Capability

Bits	Description
63:32	TmrIntRouteCap. Read-only. Reset: C00000h. Indicates which INT entry of IOAPIC can be assigned to the timer interrupt.
31:16	Reserved.
15	TmrFsbCap. Read-only. Reset: 1. 1=Front side bus delivery is supported. This bit can be modified by PMx50[4:2] .
14	TmrFsbEn. Read-write. Reset: 0. 1=Enable front side bus delivery of interrupt.
13:9	TmrIntRoute. Read-write. Reset: 0. This specifies which INT entry of IOAPIC the timer is routed to if HPETx010[LegacyEn] == 0.
8	Tmr32ModeEn. Read-only. Reset: 0. 0=64-bit timer is not supported.
7	Reserved.
6	TmrSetPer. Read-write. Reset: 0. 1=Allow software to set the timer's accumulator if the timer is set to periodic mode. The bit is automatically cleared when HPETx1[4:0:Step2]8 [Timer[2:0] Comparator] is written by software.
5	TmrSizeCap. Read-only. Reset: 0. The timer is 32-bits wide.
4	TmrTypCap. Read-only. Reset: 1. The timer supports periodic interrupt delivery mode.
3	TmrTyp. Read-write. Reset: 0. Selects the timer interrupt type. 0=Non-periodic. 1=Periodic
2	TmrIntEn. Read-write. Reset: 0. 1=Enable the timer interrupt.
1	TmrIntTyp. Read-write. Reset: 0. Specifies the timer interrupt polarity. 0=Edge triggered. 1=Level triggered
0	Reserved.

HPETx1[4:0:Step2]8 Timer[2:0] Comparator

Bits	Description

63:32	Reserved.
31:0	Comparator. IF (HPETx1[4:0:Step2]0[TmrTyp] == 0) THEN Read-write. ELSEIF ((HPETx1[4:0:Step2]0[TmrTyp] == 1) && (HPETx1[4:0:Step2]0[TmrSetPer] == 1)) THEN Read-write. ELSE Read-only. ENDIF. Reset: FFFF_FFFFh. Comparator is periodically incremented by the value last written to this register. This register is updated by hardware when (HPETx1[4:0:Step2]0[TmrTyp] == 1) && the current value in this register matches with the value in HPETx0F0 [Main Counter].

3.26.11 Miscellaneous (MISC) Registers

MISC register space is accessed through the AcpiMmio region, which can be memory mapped or IO mapped. The MISC registers range from [PMx24\[AcpiMmioAddr\]+E00h](#) to [PMx24\[AcpiMmioAddr\]+EFFh](#). See [PMx24 \[AcpiMmioEn\]](#).

MISCx00 GPPClkCntrl

BIOS: See [2.15.9.1](#).

Bits	Description																				
31	Reserved.																				
30:27	CG1PLL_VREG_BIAS . Read-write. Reset: 0. Voltage regulator current bias control (Spare).																				
26:25	CG1PLL_VREG_CNTL . Read-write. Reset: 0. Voltage regulator voltage control (Spare).																				
24	CG1PLL_VREG_VREF_SEL . Read-write. Reset: 0. Select Voltage regulator reference (Spare). 0=Bandgap. 1=Resistor Divider.																				
23	CG1PLL_PLLCORE_PWDN_EN . Read-write. Reset: 0. Control for powering down PLL's analog core (including PFD/CP, OTA, VCO, REFGENS, LF and all differential output drivers). It is only used for external clock-chip mode to bypass XTALIN 25 MHz to SATA differentially, when CG1_PLL is required to be off. 0=Disable. 1=Enable.																				
22:19	CGPLL_BG_ADJ . Read-write. Reset: 8. Fine adjust for band-gap. Level shifted inside PLL to 1.8V.																				
18:16	CG_OSC_GAIN_EN . Read-write. Reset: 6. CG_XTAL Pad Gain setting control of oscillator buffer.																				
15:12	GPP_CLK3_ClockRequestMapping . Read-write. Reset: Fh. GPP3 PCIE clock pins (GPP_CLK3P/GPP_CLK3N) output control by CLK_REQ# pin. GPP_CLK3P/GPP_CLK3N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP3 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP3 PCIE clock output pins if it is asserted. GPP3_CLKREQ_Mapping:																				
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Off</td> </tr> <tr> <td>0001b</td> <td>CLK_REQ0#</td> </tr> <tr> <td>0010b</td> <td>CLK_REQ1#</td> </tr> <tr> <td>0011b</td> <td>CLK_REQ2#</td> </tr> <tr> <td>0100b</td> <td>CLK_REQ3#</td> </tr> <tr> <td>1001b-0101b</td> <td>Reserved; Off</td> </tr> <tr> <td>1010b</td> <td>CLK_REQGfx#</td> </tr> <tr> <td>1110b-1011b</td> <td>Reserved; Off</td> </tr> <tr> <td>1111b</td> <td>On</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0000b	Off	0001b	CLK_REQ0#	0010b	CLK_REQ1#	0011b	CLK_REQ2#	0100b	CLK_REQ3#	1001b-0101b	Reserved; Off	1010b	CLK_REQGfx#	1110b-1011b	Reserved; Off	1111b	On
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0100b	CLK_REQ3#																				
1001b-0101b	Reserved; Off																				
1010b	CLK_REQGfx#																				
1110b-1011b	Reserved; Off																				
1111b	On																				

11:8	GPP_CLK2_ClockRequestMapping . Read-write. Reset: Fh. GPP2 PCIE clock pins (GPP_CLK2P/GPP_CLK2N) output control by CLK_REQ# pin. GPP_CLK2P/GPP_CLK2N pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP2 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP2 PCIE clock output pins if it is asserted. GPP2_CLKREQ_Mapping:
<u>Bits</u>	<u>Definition</u>
0000b	Off
0001b	CLK_REQ0#
0010b	CLK_REQ1#
0011b	CLK_REQ2#
0100b	CLK_REQ3#
1001b-0101b	Reserved; Off
1010b	CLK_REQGfx#
1110b-1011b	Reserved; Off
1111b	On

7:4	<p>GPP_CLK1_ClockRequestMapping. Read-write. Reset: Fh. GPP1 PCIE clock pins (GPP_CLK1P/GPP_CLK1N) output control by CLK_REQ# pin. GPP_CLK1P/GPP_CLK1N pins are powered off when FCH is strapped to use an external clock and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP1 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off GPP1 PCIE clock output pins if it is asserted.</p> <p>GPP1_CLKREQ_Mapping:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th><th style="text-align: left;"><u>Definition</u></th></tr> </thead> <tbody> <tr><td>0000b</td><td>Off</td></tr> <tr><td>0001b</td><td>CLK_REQ0#</td></tr> <tr><td>0010b</td><td>CLK_REQ1#</td></tr> <tr><td>0011b</td><td>CLK_REQ2#</td></tr> <tr><td>0100b</td><td>CLK_REQ3#</td></tr> <tr><td>1001b-0101b</td><td>Reserved; Off</td></tr> <tr><td>1010b</td><td>CLK_REQGfx#</td></tr> <tr><td>1110b-1011b</td><td>Reserved; Off</td></tr> <tr><td>1111b</td><td>On</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0000b	Off	0001b	CLK_REQ0#	0010b	CLK_REQ1#	0011b	CLK_REQ2#	0100b	CLK_REQ3#	1001b-0101b	Reserved; Off	1010b	CLK_REQGfx#	1110b-1011b	Reserved; Off	1111b	On
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1010b	CLK_REQGfx#																				
1110b-1011b	Reserved; Off																				
1111b	On																				
3:0	<p>GPP_CLK0_ClockRequestMapping. Read-write. Reset: Fh. GPP0 PCIE clock pins (GPP_CLK0P/GPP_CLK0N) output control by CLK_REQ# pin. GPP_CLK0P/GPP_CLK0N pins are powered off when FCH is strapped to use an external clock and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, GPP0 PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off the GPP0 PCIE clock output pins if it is asserted.</p> <p>GPP0_CLKREQ_Mapping:</p> <table border="1" style="margin-left: 20px;"> <thead> <tr> <th style="text-align: left;"><u>Bits</u></th><th style="text-align: left;"><u>Definition</u></th></tr> </thead> <tbody> <tr><td>0000b</td><td>Off</td></tr> <tr><td>0001b</td><td>CLK_REQ0#</td></tr> <tr><td>0010b</td><td>CLK_REQ1#</td></tr> <tr><td>0011b</td><td>CLK_REQ2#</td></tr> <tr><td>0100b</td><td>CLK_REQ3#</td></tr> <tr><td>1001b-0101b</td><td>Reserved; Off</td></tr> <tr><td>1010b</td><td>CLK_REQGfx#</td></tr> <tr><td>1110b-1011b</td><td>Reserved; Off</td></tr> <tr><td>1111b</td><td>On</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0000b	Off	0001b	CLK_REQ0#	0010b	CLK_REQ1#	0011b	CLK_REQ2#	0100b	CLK_REQ3#	1001b-0101b	Reserved; Off	1010b	CLK_REQGfx#	1110b-1011b	Reserved; Off	1111b	On
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0011b	CLK_REQ2#																				
0100b	CLK_REQ3#																				
1001b-0101b	Reserved; Off																				
1010b	CLK_REQGfx#																				
1110b-1011b	Reserved; Off																				
1111b	On																				

MISCx04_ClkOutputCntrl

Bits	Description
31	CG2_RegulatorOff. Read-write. Reset: 0. 1=Turn off CG2_PLL Regulator.
30	CG1_RegulatorOff. Read-write. Reset: 0. 1=Turn off CG1_PLL Regulator.
29	Reserved.
28	PciePhyRefClkPwdn. Read-write. Reset: 0. 1=Power-off Clkggen_outpad 100Mhz CML reference clock for PCIE_PHY.
27	CLKGEN_TestClkPwDn. Read-write. Reset: 0. 1=Power off Clkggen_outpad TestClk Output buffer.

26	EXT_CLK_ClockSourceOverride. Read-write. Reset: 0. EXT_CLK clock source override control. EXT_CLK clock source is controlled by strap (LPCCLK1). If Strap (LPCCLK1) == 1, clock source is from CG_PLL. If Strap (LPCCLK1) == 0, clock source is from external clock chip through GPP_CLK3_P/N pins. This override bit allows to invert the strap that controls EXT_CLK clock source. 0=Use the strap value (LPCCLK1) to determine whether EXT_CLK clock source from either CG_PLL or external clock chip. 1=Invert the strap that controls EXT_CLK clock source.										
25	CG2PLL_CoreClkOutputEn. Read-write. Reset: 1. CG2_PLL Core Clock (400 MHz) Output Enable. 0=Clock Output Buffer disable. 1=Clock Output Buffer Enable.										
24:23	CG1PLL_DS_Order. Read-write. Reset: 1. DS order setting. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>disable</td> </tr> <tr> <td>01b</td> <td>1st order</td> </tr> <tr> <td>10b</td> <td>2nd order</td> </tr> <tr> <td>11b</td> <td>3rd order</td> </tr> </tbody> </table>	Bits	Definition	00b	disable	01b	1st order	10b	2nd order	11b	3rd order
Bits	Definition										
00b	disable										
01b	1st order										
10b	2nd order										
11b	3rd order										
22	CG1PLL_DS_PrbsEn. Read-write. Reset: 1. 1=Enable CG1_PLL PRBS17 generator in DS modulator.										
21:20	CG1PLL_FBDIV_FractionCtl. Read-write. Reset: 1. CG1_PLL Slip Req/Ack handshaking control: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)</td> </tr> <tr> <td>01b</td> <td>Slip once every clock cycle (ignore slip_ack)</td> </tr> <tr> <td>10b</td> <td>Slip once every 2 clock cycles (ignore slip_ack)</td> </tr> <tr> <td>11b</td> <td>Slip once every 4 clock cycles (ignore slip_ack)</td> </tr> </tbody> </table>	Bits	Definition	00b	Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)	01b	Slip once every clock cycle (ignore slip_ack)	10b	Slip once every 2 clock cycles (ignore slip_ack)	11b	Slip once every 4 clock cycles (ignore slip_ack)
Bits	Definition										
00b	Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)										
01b	Slip once every clock cycle (ignore slip_ack)										
10b	Slip once every 2 clock cycles (ignore slip_ack)										
11b	Slip once every 4 clock cycles (ignore slip_ack)										
16	ClockBufferBiasPowerDownEnable. Read-write. Reset: 1. 1=Power down the clock buffers bias current circuit for power saving.										
13	PCIE_RCLK_PowerDownEnable. Read-write. Reset: 0. BIOS: See 2.15.9.1 . 1=Power down PCIE_RCLK input buffer for power saving.										
12	GFX_GPP_CLK_ClockOutputOverride: GFX_GPP_CLK [2:0] ClockOutputOverride. Read-write. Reset: 0. GFX_GPP_CLK[2:0] clock output override control. GFX_CLK and GPP_CLK[2:0] clock outputs are controlled by [SLT_GFX_CLKClockRequestMapping] and MISCx00[GPP_CLK0_ClockRequestMapping, GPP_CLK1_ClockRequestMapping, GPP_CLK2_ClockRequestMapping] . Basically it depends on whether chip is in internal (Strap (LPCCLK1)=1) or external (Strap (LPCCLK1)=0) clock mode. This override bit allows to invert the strap value that controls clock output buffer. 0=Use SLT_GFX Clock Request mapping and GPP_CLK[2:0] Clock Request mapping to determine whether clock output buffer is on or off. 1=Invert the strap that controls those clock output buffer.										
11	GPP_CLK3_ClockOutputOverride. Read-write. Reset: 0. GPP_CLK3 clock output override control. GPP_CLK3 is a bi-directional pin depending on LPCCLK1 strap value. If Strap (LPCCLK1)=1, GPP_CLK3 provides clock for external device and output buffer will be on. If Strap (LPCCLK1)=0, GPP_CLK3 receives clock from external clock chip and output buffer will be off. This override bit allows to invert the strap that controls GPP_CLK3 clock output buffer. 0=Use the strap value (LPCCLK1) to determine whether GPP_CLK3 clock output buffer is on or off. 1=Invert the strap that controls GPP_CLK3 clock output buffer.										

10	CPU_CLK_ClockSourceOverride. Read-write. Reset: 0. CPU_CLK clock source override control. CPU_CLK clock source is controlled by strap (LPCCLK1). If Strap (LPCCLK1)=1, CPU_CLK clock source is from CG_PLL. If Strap (LPCCLK1)=0, CPU_CLK clock source is from external clock chip through GPP_CLK3_P/N pins. This override bit allows to invert the strap that controls CPU_CLK clock source. 0=Use the strap value (LPCCLK1) to determine whether CPU_CLK clock source from either CG_PLL or external clock chip. 1=Invert the strap that controls CPU_CLK clock source.																				
7:4	SLT_GFX_CLK_ClockRequestMapping. Read-write. Reset: Fh. Gfx PCIE clock pins (SLT_GFX_CLKP/SLT_GFX_CLKN) output control. SLT_GFX_CLKP/SLT_GFX_CLKN pins are powered off when FCH is strapped to use an external clock, and powered on when FCH is strapped to operate in integrated clock mode. When FCH is in integrated clock mode, Gfx PCIE clock can be powered off according to the CLK_REQ mapping table below, and the selected CLK_REQ# input can power off Gfx PCIE clock output pins if it is asserted. Gfx_CLKREQ_Mapping: <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>Off</td> </tr> <tr> <td>0001b</td> <td>CLK_REQ0#</td> </tr> <tr> <td>0010b</td> <td>CLK_REQ1#</td> </tr> <tr> <td>0011b</td> <td>CLK_REQ2#</td> </tr> <tr> <td>0100b</td> <td>CLK_REQ3#</td> </tr> <tr> <td>1001b-0101b</td> <td>Reserved; Off</td> </tr> <tr> <td>1010b</td> <td>CLK_REQGfx#</td> </tr> <tr> <td>1110b-1011b</td> <td>Reserved; Off</td> </tr> <tr> <td>1111b</td> <td>On</td> </tr> </tbody> </table>	Bits	Definition	0000b	Off	0001b	CLK_REQ0#	0010b	CLK_REQ1#	0011b	CLK_REQ2#	0100b	CLK_REQ3#	1001b-0101b	Reserved; Off	1010b	CLK_REQGfx#	1110b-1011b	Reserved; Off	1111b	On
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0100b	CLK_REQ3#																				
1001b-0101b	Reserved; Off																				
1010b	CLK_REQGfx#																				
1110b-1011b	Reserved; Off																				
1111b	On																				
3:2	CG1PLL_LOCK_FREQ_SEL. Read-write. Reset: 0. CG1_PLL VCO centre frequency selection for calibration. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>set VCO centre at 1200 MHz</td> </tr> <tr> <td>01b</td> <td>set VCO centre at 1000 MHz</td> </tr> <tr> <td>10b</td> <td>set VCO centre at 800 MHz</td> </tr> <tr> <td>11b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Definition	00b	set VCO centre at 1200 MHz	01b	set VCO centre at 1000 MHz	10b	set VCO centre at 800 MHz	11b	Reserved										
Bits	Definition																				
00b	set VCO centre at 1200 MHz																				
01b	set VCO centre at 1000 MHz																				
10b	set VCO centre at 800 MHz																				
11b	Reserved																				
1	CG1PLL_BYPASS_CAL. Read-write. Reset: 0. CG1_PLL Calibration bypass enable. 0=Always do VCO calibration after a reset. 1=Bypass VCO calibration after a reset.																				
0	CG1PLL_CAL_BYPASS_REFDIV_EN. Read-write. Reset: 0. CG1_PLL Calibration reference divider bypass enable. 0=Reference divider set by MISCx10[CG1PLL_CAL_REFDIV] during calibration. 1=Bypass reference divider during calibration.																				

MISCx08 CGPLLConfig1

Bits	Description
31:16	CG1PLL_DS_Frac. Read-write. Reset: 0. CG1_PLL DS fractional setting.
15:11	Reserved. DS fractional setting.
10	CG2PLL_Reset. Read-write; Cleared-by-hardware. Reset: 0. 1=Reset the CG2_PLL. The bit will be cleared to 0 by hardware after reset sequence is done.
9	Reserved.

5	Cg1PllSataClkBypass . Read-write. Reset: 0. SATA clock source frequency select from CG1_PLL. SATA reference clock output from CG1_PLL has an option for either output 100Mhz or bypass CG1_PLL RefClk input. 0=PLL 100Mhz. 1=Bypass CG1_PLL RefClk input (48Mhz or 100Mhz)
4	Reserved.
2:1	Reserved.
0	CG1PLL_SpreadSpectrumEnable . Read-write. Reset: 0. 1=Enable CG1_PLL Spread Spectrum. 0=Disable Spread Spectrum.

MISCx0C CGPLLConfig2

Bits	Description												
31:25	CG1PLL_PDIV_PCIECLK . Read-write. Reset: 12h. CG1_PLL 100 MHz clock post divider (PCIE and SATA clock). <table> <thead> <tr> <th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Bypass</td></tr> <tr> <td>1h</td><td>Bypass</td></tr> <tr> <td>7Fh-02h</td><td>Divide by <CG1PLL_PDIV_PCIECLK></td></tr> </tbody> </table>	Bits	Definition	0h	Bypass	1h	Bypass	7Fh-02h	Divide by <CG1PLL_PDIV_PCIECLK>				
Bits	Definition												
0h	Bypass												
1h	Bypass												
7Fh-02h	Divide by <CG1PLL_PDIV_PCIECLK>												
24:18	CG1PLL_PDIV_CoreCLK . Read-write. Reset: 03h. CG1_PLL 400 MHz clock post divider (core clock). <table> <thead> <tr> <th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>0h</td><td>Bypass</td></tr> <tr> <td>1h</td><td>Bypass</td></tr> <tr> <td>7Fh-02h</td><td>Divide by <CG1PLL_PDIV_CoreCLK></td></tr> </tbody> </table>	Bits	Definition	0h	Bypass	1h	Bypass	7Fh-02h	Divide by <CG1PLL_PDIV_CoreCLK>				
Bits	Definition												
0h	Bypass												
1h	Bypass												
7Fh-02h	Divide by <CG1PLL_PDIV_CoreCLK>												
17:16	SATA_REFIN_ClkBufDrvStr . Read-write. Reset: 01b. Specifies the drive strength control for internal SATA RefClk input differential clock buffers (from CLKGEN to SATA_PHY). <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>6X driving</td><td>10b</td><td>10X driving</td></tr> <tr> <td>01b</td><td>8X driving</td><td>11b</td><td>12X driving</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	6X driving	10b	10X driving	01b	8X driving	11b	12X driving
Bits	Definition	Bits	Definition										
00b	6X driving	10b	10X driving										
01b	8X driving	11b	12X driving										
15:14	USB2_REFIN_ClkBufDrvStr . Read-write. Reset: 01b. Specifies the drive strength control for internal USB2 RefClk input differential clock buffers (from CLKGEN to USB2_PHY). <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1.5X driving</td><td>10b</td><td>3X driving</td></tr> <tr> <td>01b</td><td>2X driving</td><td>11b</td><td>3.5X driving</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	1.5X driving	10b	3X driving	01b	2X driving	11b	3.5X driving
Bits	Definition	Bits	Definition										
00b	1.5X driving	10b	3X driving										
01b	2X driving	11b	3.5X driving										
13:12	USB3_REFIN_ClkBufDrvStr . Read-write. Reset: 01b. Specifies the drive strength control for internal USB3 RefClk input differential clock buffers (from CLKGEN to USB3_PHY). <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>2X driving</td><td>10b</td><td>4X driving</td></tr> <tr> <td>01b</td><td>3X driving</td><td>11b</td><td>5X driving</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	2X driving	10b	4X driving	01b	3X driving	11b	5X driving
Bits	Definition	Bits	Definition										
00b	2X driving	10b	4X driving										
01b	3X driving	11b	5X driving										
11:10	PCIe_REFIN_ClkBufDrvStr . Read-write. Reset: 01b. Specifies the drive strength control for internal PCIe RefClk input differential clock buffers (from CLKGEN to PCIe). <table> <thead> <tr> <th>Bits</th><th>Definition</th><th>Bits</th><th>Definition</th></tr> </thead> <tbody> <tr> <td>00b</td><td>2X driving</td><td>10b</td><td>4X driving</td></tr> <tr> <td>01b</td><td>3X driving</td><td>11b</td><td>5X driving</td></tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	2X driving	10b	4X driving	01b	3X driving	11b	5X driving
Bits	Definition	Bits	Definition										
00b	2X driving	10b	4X driving										
01b	3X driving	11b	5X driving										

9:8	CGPLL_REFIN_ClkBufDrvStr. Read-write. Reset: 01b. Specifies the drive strength control for CGPLL external refclk input differential clock buffers (from CLKGEN to CGPLL).												
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th><th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>1.5X driving</td><td>10b</td><td>3X driving</td></tr> <tr> <td>01b</td><td>2X driving</td><td>11b</td><td>3.5X driving</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	1.5X driving	10b	3X driving	01b	2X driving	11b	3.5X driving
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>										
00b	1.5X driving	10b	3X driving										
01b	2X driving	11b	3.5X driving										
7:2	Reserved.												
1:0	Cg1BgVrefBias. Read-write. Reset: 0. Specifies the CGPLL voltage regulator current bias control from Bandgap VREG_BIAS[1:0].												
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th><th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>100 uA</td><td>10b</td><td>75 uA</td></tr> <tr> <td>01b</td><td>120 uA</td><td>11b</td><td>85 uA</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	00b	100 uA	10b	75 uA	01b	120 uA	11b	85 uA
<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>										
00b	100 uA	10b	75 uA										
01b	120 uA	11b	85 uA										

MISCx10 CGPLLConfig3

Bits	Description								
31:30	Reserved.								
29:26	CG1PLL_CAL_REFDIV. Read-write. Reset: 0100b. Calibration reference divider control. It is only used when MISCx04 [CG1PLL_CAL_BYPASS_REFDIV_EN] == 0.								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0h</td><td>invalid</td></tr> <tr> <td>1h</td><td>invalid</td></tr> <tr> <td>Fh-2h</td><td>Divide by <CG1PLL_CAL_REFDIV></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0h	invalid	1h	invalid	Fh-2h	Divide by <CG1PLL_CAL_REFDIV>
<u>Bits</u>	<u>Definition</u>								
0h	invalid								
1h	invalid								
Fh-2h	Divide by <CG1PLL_CAL_REFDIV>								
25:22	CG1PLL_FBDIV_Fraction. Read-write. Reset: 0. Fractional part setting of the CG1_PLL feedback divider value.								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td></tr> <tr> <td>9-1</td><td><CG1PLL_FBDIV_Fraction*0.1></td></tr> <tr> <td>15-10</td><td>0</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	0	9-1	<CG1PLL_FBDIV_Fraction*0.1>	15-10	0
<u>Bits</u>	<u>Definition</u>								
0	0								
9-1	<CG1PLL_FBDIV_Fraction*0.1>								
15-10	0								
21:10	CG1PLL_FBDIV. Read-write. Reset: 50. Integer part setting of the CG1_PLL Feedback divider value.								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Divide by 2</td></tr> <tr> <td>1</td><td>Divide by 2</td></tr> <tr> <td>FFFh-2h</td><td>Divide by <CG1PLL_FBDIV></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Divide by 2	1	Divide by 2	FFFh-2h	Divide by <CG1PLL_FBDIV>
<u>Bits</u>	<u>Definition</u>								
0	Divide by 2								
1	Divide by 2								
FFFh-2h	Divide by <CG1PLL_FBDIV>								
9:0	CG1PLL_REFDIV. Read-write. Reset: 2. Reference divider control. It is only used after calibration is done.								
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Bypass</td></tr> <tr> <td>1</td><td>Bypass</td></tr> <tr> <td>3FFh-2h</td><td>Divide by <CG1PLL_REFDIV></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Bypass	1	Bypass	3FFh-2h	Divide by <CG1PLL_REFDIV>
<u>Bits</u>	<u>Definition</u>								
0	Bypass								
1	Bypass								
3FFh-2h	Divide by <CG1PLL_REFDIV>								

MISCx14 CGPLLConfig4

Bits	Description

31:16	CG1PLL_SS_AMOUNT_DSFRAC . Read-write. Reset: 1FFFh. CG1_PLL Spread spectrum amount DS setting.
15:0	CG1PLL_SS_STEP_SIZE_DSFRAC . Read-write. Reset: 16Dh. CG1_PLL Spread spectrum step size DS control.

MISCx18 CGPLLConfig5

Bits	Description										
31:30	Reserved.										
29	CG2PLL_VCO800M_EN . Read-write. Reset: 0. 1=Enable CG2_PLL VCO running at 800 MHz. 0=Disable. A warm reset is required after programming this bit to enable/disable VCO running at 800 MHz.										
28:27	Reserved.										
26	CG1PLL_VCO800M_EN . Read-write. Reset: 0. 1=Enable CG1_PLL VCO running at 800 MHz. 0=Disable. A warm reset is required after setting this bit to enable/disable VCO running at 800 MHz.										
25:24	CG1PLL_PCALREF . Read-write. Reset: 0. CG1_PLL VCO input2 control. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>close loop configuration</td> </tr> <tr> <td>1</td> <td>1/3 supply voltage</td> </tr> <tr> <td>2</td> <td>1/2 supply voltage</td> </tr> <tr> <td>3</td> <td>2/3 supply voltage</td> </tr> </tbody> </table>	Bits	Definition	0	close loop configuration	1	1/3 supply voltage	2	1/2 supply voltage	3	2/3 supply voltage
Bits	Definition										
0	close loop configuration										
1	1/3 supply voltage										
2	1/2 supply voltage										
3	2/3 supply voltage										
23:22	CG1PLL_PVCOREF . Read-write. Reset: 0. CG1_PLL VCO input1control. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>close loop configuration</td> </tr> <tr> <td>1</td> <td>1/3 supply voltage</td> </tr> <tr> <td>2</td> <td>1/2 supply voltage</td> </tr> <tr> <td>3</td> <td>2/3 supply voltage</td> </tr> </tbody> </table>	Bits	Definition	0	close loop configuration	1	1/3 supply voltage	2	1/2 supply voltage	3	2/3 supply voltage
Bits	Definition										
0	close loop configuration										
1	1/3 supply voltage										
2	1/2 supply voltage										
3	2/3 supply voltage										
21:13	Reserved.										
12	CG1PLL_SS_MODE . Read-write. Reset: 1. CG1_PLL Spread spectrum mode select. 0=Center spread. 1=Down spread.										
11:8	CG1PLL_SS_AMOUNT_NFRAC_SLIP . Read-write. Reset: 2. CG1_PLL Spread spectrum amount fractional setting.										
7:0	CG1PLL_SS_AMOUNT_FBDIV . Read-write. Reset: 0. CG1_PLL Spread spectrum amount setting.										

MISCx1C CGPLLConfig6BIOS: See [2.15.9.3 \[CG_PLL CMOS Clock Driver Setting for Power Saving\]](#).

Bits	Description
31:30	Reserved.
29	CgpllClkDriverUpdate . Read-write. Cold Reset: X. CGPLL clock output drive type update. CGPLL has CML and CMOS type of clock output drivers. The selections are in MISCx1C[28:21] . 0=CG_PLL clock driver type selection only gets updated from MISCx1C[28:21] when CG_PLL got reset. 1=CG_PLL clock driver type selection gets updated on the fly from MISCx1C[28:21] .

28:25	Cg1RefClk48MHzDriverType . Read-write. Cold Reset: 0. Selects CG1_PLL RefClk 48Mhz clock driver type. For each bit, 0=CML type clock driver. 1=CMOS type clock driver (consume less power).										
	<table> <thead> <tr> <th><u>Bit</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>Reserved</td></tr> <tr> <td>[1]</td><td>Buf48 MHz for USB2 and SATA</td></tr> <tr> <td>[2]</td><td>Reserved</td></tr> <tr> <td>[3]</td><td>Reserved</td></tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	Reserved	[1]	Buf48 MHz for USB2 and SATA	[2]	Reserved	[3]	Reserved
<u>Bit</u>	<u>Definition</u>										
[0]	Reserved										
[1]	Buf48 MHz for USB2 and SATA										
[2]	Reserved										
[3]	Reserved										
24:21	Cg1ClkDriverType . Read-write. Cold Reset: 0. Selects CG1_PLL clock driver type. For each bit, 0=CML type clock driver. 1=CMOS type clock driver (consume less power).										
	<table> <thead> <tr> <th><u>Bit</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>USB</td></tr> <tr> <td>[1]</td><td>SATA</td></tr> <tr> <td>[2]</td><td>Reserved</td></tr> <tr> <td>[3]</td><td>PCIE</td></tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	USB	[1]	SATA	[2]	Reserved	[3]	PCIE
<u>Bit</u>	<u>Definition</u>										
[0]	USB										
[1]	SATA										
[2]	Reserved										
[3]	PCIE										
20	SataRefClkSrc . Read-write. Reset: 0. Selects SATA reference clock source. 0=SATA reference clock is from CG XTAL 48 Mhz non-spread. 1=Reserved.										
19:18	Reserved.										
17:9	CG1PLL_LF_MODE . Read-write. Reset: 0FEh. CG1_PLL Loop filter control. It defines the setting of loop filter R and C values.										
8	CG2PLL_RefClk_Sel . Read-write. Reset: 1. CG2_PLL reference clock select. 0=100 MHz from external clock chip. 1=25 MHz from XTAL.										
7	Force25mXtalPadPwdn . Read-write. Reset: 0. Force 25M XTAL Pad Power Down. Set this bit and MISCx40[Pwdn25Mxtal] to 1 to power down 25 MHz XTAL Pad										
6	CG2PLL_PWDN_FORCE . Read-write. Reset: 0. Force CG2_PLL Power Down. Set this bit and MISCx08[CG2PLL_PowerDown] to 1 to power down CG2_PLL.										
5	Reserved.										
4:0	CG1PLL_CAL_MODE . Read-write. Reset: 5. CG1_PLL VCO calibration mode control.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0xxxxb</td><td>VCO mode set to calibrated values</td></tr> <tr> <td>1xxxxb</td><td>VCO mode forced to the value set in CG1PLL_CAL_MODE[3:0]</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0xxxxb	VCO mode set to calibrated values	1xxxxb	VCO mode forced to the value set in CG1PLL_CAL_MODE[3:0]				
<u>Bits</u>	<u>Definition</u>										
0xxxxb	VCO mode set to calibrated values										
1xxxxb	VCO mode forced to the value set in CG1PLL_CAL_MODE[3:0]										

MISCx20 IMPCalibration

Bits	Description
31:26	CG1PLL_SPARE . Read-write. Reset: 0. CG1_PLL general spare pins.
25:23	Reserved.
22:20	CG1PLL_DIG_SPARE . Read-write. Reset: 0. CG1_PLL digital block spare pins.
19	CG1PLL_SATA_CLK_CUSTOM_PDIV_EN . Read-write. Reset: 1. CG1_PLL CLKOUT3B (SATA 100 MHz) Post-dividers selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.
18	CG1PLL_PCIE_CLK_CUSTOM_PDIV_EN . Read-write. Reset: 1. CG1_PLL CLKOUT3A (PCIe 100 MHz) post divider selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.

17	CG1PLL_USB2CLK_CUSTOM_PDIV_EN. Read-write. Reset: 0. CG1_PLL CLKOUT2 (USB 48 MHz) post divider selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.																																														
16	CG1PLL_CLKOUT3A_PDIVSEL. Read-write. Reset:1. CG1_PLL PCIe clock select between Ref-Clk (input of reference divider) and post divider 3. 0=Input of reference divider. 1=PDIV3 Output.																																														
15	CG1PLL_CLKOUT2_PDIVSEL. Read-write. Reset: 1. CG1_PLL USB2 clock select between Ref-Clk (input of reference divider) and post divider 2. 0=Input of reference divider. 1=PDIV2 Output.																																														
14	CG1PLL_CLKOUT1_PDIVSEL. Read-write. Reset: 1. CG1_PLL Core Clock select between Ref-Clk (input of reference divider) and post divider 1. 0=Input of reference divider. 1=PDIV1 Output.																																														
13:12	CG1PLL_PFD_PULSE_SEL. Read-write. Reset: 2. CG1_PLL Change reset pulse inside PFD. <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>~110 ps</td> </tr> <tr> <td>01b</td> <td>~220 ps</td> </tr> <tr> <td>10b</td> <td>~350 ps</td> </tr> <tr> <td>11b</td> <td>~500 ps</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	~110 ps	01b	~220 ps	10b	~350 ps	11b	~500 ps																																				
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11:8	CG1PLL_CP. Read-write. Reset: 0001b. CG1_PLL charge pump control. IF(RevA0) THEN <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>0 uA</td> </tr> <tr> <td>0001b</td> <td>5 uA</td> </tr> <tr> <td>1110b-0010b</td> <td><CG1PLL_CP*5 uA></td> </tr> <tr> <td>1111b</td> <td>75 uA</td> </tr> </tbody> </table> ELSE <table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>15 uA</td> <td>1000b</td> <td>55 uA</td> </tr> <tr> <td>0001b</td> <td>10 uA</td> <td>1001b</td> <td>50 uA</td> </tr> <tr> <td>0010b</td> <td>5 uA</td> <td>1010b</td> <td>45 uA</td> </tr> <tr> <td>0011b</td> <td>0 uA</td> <td>1011b</td> <td>40 uA</td> </tr> <tr> <td>0100b</td> <td>35 uA</td> <td>1100b</td> <td>75 uA</td> </tr> <tr> <td>0101b</td> <td>30 uA</td> <td>1101b</td> <td>70 uA</td> </tr> <tr> <td>0110b</td> <td>25 uA</td> <td>1110b</td> <td>65 uA</td> </tr> <tr> <td>0111b</td> <td>20 uA</td> <td>1111b</td> <td>60 uA</td> </tr> </tbody> </table> ENDIF	<u>Bits</u>	<u>Definition</u>	0000b	0 uA	0001b	5 uA	1110b-0010b	<CG1PLL_CP*5 uA>	1111b	75 uA	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>	0000b	15 uA	1000b	55 uA	0001b	10 uA	1001b	50 uA	0010b	5 uA	1010b	45 uA	0011b	0 uA	1011b	40 uA	0100b	35 uA	1100b	75 uA	0101b	30 uA	1101b	70 uA	0110b	25 uA	1110b	65 uA	0111b	20 uA	1111b	60 uA
<u>Bits</u>	<u>Definition</u>																																														
0000b	0 uA																																														
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0111b	20 uA	1111b	60 uA																																												
7:0	CG1PLL_IBIAS. Read-write. Reset: 59h. CG1_PLL current bias control. <table> <thead> <tr> <th><u>Bit</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>BIAS0</td> </tr> <tr> <td>[1]</td> <td>BIAS1</td> </tr> <tr> <td>[2]</td> <td>CPTUNE0</td> </tr> <tr> <td>[3]</td> <td>CPTUNE1</td> </tr> <tr> <td>[4]</td> <td>AMPTUNE0 (SPARE)</td> </tr> <tr> <td>[5]</td> <td>AMPTUNE1 (SPARE)</td> </tr> <tr> <td>[6]</td> <td>HALFGM</td> </tr> <tr> <td>[7]</td> <td>SPARE</td> </tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	BIAS0	[1]	BIAS1	[2]	CPTUNE0	[3]	CPTUNE1	[4]	AMPTUNE0 (SPARE)	[5]	AMPTUNE1 (SPARE)	[6]	HALFGM	[7]	SPARE																												
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[6]	HALFGM																																														
[7]	SPARE																																														

MISCx24 ClkDrvStr1

Bits	Description
31:20	CG2PLL_FBDIV . Read-write. Reset: 48. Integer part setting of the CG2_PLL feedback divider value. <u>Bits</u> <u>Definition</u> 0 Divide by 2 1 Divide by 2 FFFh-2h Divide by <CG2PLL_FBDIV>
19:18	SLT_GFX_ClockBufferDrivingStrengthControl . Read-write. Reset: 10b. Drive strength control for SLT_GFX differential clock buffers. <u>Bits</u> <u>Definition</u> 00b 12 mA 01b 13 mA 10b 14 mA 11b 15 mA
17	CG2PLL_BYPASS_CAL . Read-write. Reset: 0. CG2_PLL Calibration bypass enable. 0=Always do VCO calibration after a reset. 1=Bypass VCO calibration after a reset.
16	CG2PLL_CAL_BYPASS_REFDIV_EN . Read-write. Reset: 0. CG2_PLL Calibration reference divider bypass enable. 0=Reference divider set by MISCx28[CG2PLL_CAL_REFDIV] during calibration. 1=Bypass reference divider during calibration.
15:12	CG2PLL_VREG_BIAS . Read-write. Reset: 0. CG2_PLL Voltage regulator current bias control (Spare).
11:10	CG2PLL_VREG_CNTL . Read-write. Reset: 0. CG2_PLL Voltage regulator voltage control (Spare).
9	CG2PLL_VREG_VREF_SEL . Read-write. Reset: 0. CG2_PLL Select Voltage regulator reference (Spare). 0=Bandgap. 1=Resistor Divider.
8	CG2PLL_PLLCORE_PWDN_EN . Read-write. Reset: 0. CG2_PLL Control for power-down PLL's analog core (including PFD/CP, OTA, VCO, REFGENS, LF and all Diff output drivers). It is only used for external clock-chip mode to bypass XTALIN 25 MHz to SATA differentially when CG2_PLL is required to be off. 0=Disable. 1=Enable.
7:6	GppClk3_ClockBufferDrivingStrengthControl . Read-write. Reset: 10b. Drive strength control for GPP_CLK3 differential clock buffers. <u>Bits</u> <u>Definition</u> 00b 12 mA 01b 13 mA 10b 14 mA 11b 15 mA
5:4	GppClk2_ClockBufferDrivingStrengthControl . Read-write. Reset: 10b. Drive strength control for GPP_CLK2 differential clock buffers. <u>Bits</u> <u>Definition</u> 00b 12 mA 01b 13 mA 10b 14 mA 11b 15 mA

3:2	GppClk1_ClockBufferDrivingStrengthControl. Read-write. Reset: 10b. Drive strength control for GPP_CLK1 differential clock buffers.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>12 mA</td></tr> <tr> <td>01b</td><td>13 mA</td></tr> <tr> <td>10b</td><td>14 mA</td></tr> <tr> <td>11b</td><td>15 mA</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	12 mA	01b	13 mA	10b	14 mA	11b	15 mA
<u>Bits</u>	<u>Definition</u>										
00b	12 mA										
01b	13 mA										
10b	14 mA										
11b	15 mA										
1:0	GppClk0_ClockBufferDrivingStrengthControl. Read-write. Reset: 10b. Drive strength control for GPP_CLK0 differential clock buffers.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>12 mA</td></tr> <tr> <td>01b</td><td>13 mA</td></tr> <tr> <td>10b</td><td>14 mA</td></tr> <tr> <td>11b</td><td>15 mA</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	12 mA	01b	13 mA	10b	14 mA	11b	15 mA
<u>Bits</u>	<u>Definition</u>										
00b	12 mA										
01b	13 mA										
10b	14 mA										
11b	15 mA										

MISCx28_ClkDrvStr2

Bits	Description										
31:28	CG2PLL_FBDIV_FRACTION. Read-write. Reset: 0. Fractional part setting of CG2_PLL Feed-back divider value.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td></tr> <tr> <td>9-1</td><td><CG2PLL_FBDIV_FRACTION*0.1></td></tr> <tr> <td>15-10</td><td>0</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	0	9-1	<CG2PLL_FBDIV_FRACTION*0.1>	15-10	0		
<u>Bits</u>	<u>Definition</u>										
0	0										
9-1	<CG2PLL_FBDIV_FRACTION*0.1>										
15-10	0										
27:24	Reserved.										
23:22	CG2PLL_FBDIV_FRACTION_CTL. Read-write. Reset: 1. CG2_PLL Slip Req/Ack handshaking control.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)</td></tr> <tr> <td>01b</td><td>Slip once every clock cycle (ignore slip_ack)</td></tr> <tr> <td>10b</td><td>Slip once every 2 clock cycles (ignore slip_ack)</td></tr> <tr> <td>11b</td><td>Slip once every 4 clock cycles (ignore slip_ack)</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)	01b	Slip once every clock cycle (ignore slip_ack)	10b	Slip once every 2 clock cycles (ignore slip_ack)	11b	Slip once every 4 clock cycles (ignore slip_ack)
<u>Bits</u>	<u>Definition</u>										
00b	Slip_req/Slip_ack handshake (8 VCO clock cycles per slip)										
01b	Slip once every clock cycle (ignore slip_ack)										
10b	Slip once every 2 clock cycles (ignore slip_ack)										
11b	Slip once every 4 clock cycles (ignore slip_ack)										
21:19	OSCOUT2_CLK_SEL. Read-write. Reset: 0. Defines auxiliary output clock frequency on USB-CLK/OSCOUT2 pin.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>48 MHz, non-spread</td></tr> <tr> <td>001b</td><td>25 MHz, spread</td></tr> <tr> <td>111b-010b</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	000b	48 MHz, non-spread	001b	25 MHz, spread	111b-010b	Reserved		
<u>Bits</u>	<u>Definition</u>										
000b	48 MHz, non-spread										
001b	25 MHz, spread										
111b-010b	Reserved										
18:16	OSCOUT1_CLK_SEL. Read-write. Reset: 0. Defines auxiliary output clock frequency on OSCOUT1 pin.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>000b</td><td>48 MHz, non-spread</td></tr> <tr> <td>001b</td><td>25 MHz, spread</td></tr> <tr> <td>111b-010b</td><td>Reserved</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	000b	48 MHz, non-spread	001b	25 MHz, spread	111b-010b	Reserved		
<u>Bits</u>	<u>Definition</u>										
000b	48 MHz, non-spread										
001b	25 MHz, spread										
111b-010b	Reserved										

15:14	CG2PLL_LOCK_FREQ_SEL. Read-write. Reset: 0. CG2_PLL VCO centre frequency selection for calibration.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>set VCO centre at 1200 MHz</td></tr> <tr> <td>01b</td><td>set VCO centre at 1000 MHz</td></tr> <tr> <td>10b</td><td>set VCO centre at 800 MHz</td></tr> <tr> <td>11b</td><td>Forbidden</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	set VCO centre at 1200 MHz	01b	set VCO centre at 1000 MHz	10b	set VCO centre at 800 MHz	11b	Forbidden
<u>Bits</u>	<u>Definition</u>										
00b	set VCO centre at 1200 MHz										
01b	set VCO centre at 1000 MHz										
10b	set VCO centre at 800 MHz										
11b	Forbidden										
13:4	CG2PLL_REF_DIV. Read-write. Reset: 1. CG2_PLL Reference divider control. It is only used after calibration is done.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Bypass</td></tr> <tr> <td>1</td><td>Bypass</td></tr> <tr> <td>3FFh-2h</td><td>Divide by <CG2PLL_REF_DIV></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Bypass	1	Bypass	3FFh-2h	Divide by <CG2PLL_REF_DIV>		
<u>Bits</u>	<u>Definition</u>										
0	Bypass										
1	Bypass										
3FFh-2h	Divide by <CG2PLL_REF_DIV>										
3:0	CG2PLL_CAL_REFDIV. Read-write. Reset: 2. CG2_PLL Calibration reference divider control. It is only used when MISCx24[CG2PLL_CAL_BYPASS_REFDIV] == 0.										
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>0</td><td>Invalid</td></tr> <tr> <td>1</td><td>Invalid</td></tr> <tr> <td>Fh-2h</td><td>Divide by <CG2PLL_CAL_REFDIV></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Invalid	1	Invalid	Fh-2h	Divide by <CG2PLL_CAL_REFDIV>		
<u>Bits</u>	<u>Definition</u>										
0	Invalid										
1	Invalid										
Fh-2h	Divide by <CG2PLL_CAL_REFDIV>										

MISCx2C ClkGatedCntl

Bits	Description																		
27:26	CG2PLL_PFD_PULSE_SEL. Read-write. Reset: 2. CG2_PLL Change reset pulse inside PFD.																		
	<table> <thead> <tr> <th><u>Bits</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>00b</td><td>~110 ps</td></tr> <tr> <td>01b</td><td>~220 ps</td></tr> <tr> <td>10b</td><td>~350 ps</td></tr> <tr> <td>11b</td><td>~500 ps</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00b	~110 ps	01b	~220 ps	10b	~350 ps	11b	~500 ps								
<u>Bits</u>	<u>Definition</u>																		
00b	~110 ps																		
01b	~220 ps																		
10b	~350 ps																		
11b	~500 ps																		
25:18	CG2PLL_IBIAS. Read-write. Reset: 59h. CG2_PLL Current bias control.																		
	<table> <thead> <tr> <th><u>Bit</u></th><th><u>Definition</u></th></tr> </thead> <tbody> <tr> <td>[0]</td><td>BIAS0</td></tr> <tr> <td>[1]</td><td>BIAS1</td></tr> <tr> <td>[2]</td><td>CPTUNE0</td></tr> <tr> <td>[3]</td><td>CPTUNE1</td></tr> <tr> <td>[4]</td><td>AMPTUNE0 --SPARE</td></tr> <tr> <td>[5]</td><td>AMPTUNE1 --SPARE</td></tr> <tr> <td>[6]</td><td>HALFGM</td></tr> <tr> <td>[7]</td><td>SPARE</td></tr> </tbody> </table>	<u>Bit</u>	<u>Definition</u>	[0]	BIAS0	[1]	BIAS1	[2]	CPTUNE0	[3]	CPTUNE1	[4]	AMPTUNE0 --SPARE	[5]	AMPTUNE1 --SPARE	[6]	HALFGM	[7]	SPARE
<u>Bit</u>	<u>Definition</u>																		
[0]	BIAS0																		
[1]	BIAS1																		
[2]	CPTUNE0																		
[3]	CPTUNE1																		
[4]	AMPTUNE0 --SPARE																		
[5]	AMPTUNE1 --SPARE																		
[6]	HALFGM																		
[7]	SPARE																		
17	BlinkClkGateOffEn: B-Link Clock Gate Off Enable. Read-write. Cold Reset: 0. BIOS: See 2.15.9.2. Internal B-Link clock has two clock trees: one is a free running clock and the other is a gated clock. When all controllers agree to stop the gated B-Link clock and this bit is set, clock gating logic will gate off the clock tree from clock root. 0=Disable BLink Clock Gate Off function. 1=Enable BLink Clock Gate Off function. This is a sticky bit.																		

16	AlinkClkGateOffEn: A-Link Clock Gate Off Enable. Read-write. Cold Reset: 0. BIOS: See 2.15.9.2 . Internal A-Link clock has two clock trees: one is a free-running clock and the other is a gated clock. When all controllers agree to stop the gated A-Link clock and this bit is set, clock gating logic will gate off the clock tree from clock root. 0=Disable A-Link Clock Gate-Off function. 1=Enable A-Link Clock Gate-Off function. This is a sticky bit.						
15:8	BlinkClkGateOffThreshold. Read-write. Reset: 0. B-Link Clock Gate Off Threshold. When all controllers agree to stop B-Link clock, clock gating logic will start a timer and deassert BLClk_Enable when the timer reaches a programmable threshold (BLClk_Enable is an internal handshake signal indicating whether gated B-Link clock is running or not).						
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>Gated clock will stop at 3 falling edge after BLClk_Enable is deasserted.</td> </tr> <tr> <td>FFh-01h</td> <td>Gated clock will stop at <3+AlinkClkGateOffThreshold> falling edge after BLClk_Enable is deasserted.</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	00h	Gated clock will stop at 3 falling edge after BLClk_Enable is deasserted.	FFh-01h	Gated clock will stop at <3+AlinkClkGateOffThreshold> falling edge after BLClk_Enable is deasserted.
<u>Bits</u>	<u>Definition</u>						
00h	Gated clock will stop at 3 falling edge after BLClk_Enable is deasserted.						
FFh-01h	Gated clock will stop at <3+AlinkClkGateOffThreshold> falling edge after BLClk_Enable is deasserted.						
7:0	AlinkClkGateOffThreshold. Read-write. Reset: 0. A-Link Clock Gate Off Threshold. When all controllers agree to stop A-Link clock, clock gating logic will start a timer and deassert ALClk_Enable when the timer reaches a programmable threshold (ALClk_Enable is an internal handshake signal indicating whether gated A-Link clock is running or not).						
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<u>Bits</u>	<u>Definition</u>						
00h	Gated clock will stop at 3 falling edge after ALClk_Enable is deasserted.						
FFh-01h	Gated clock will stop at <3+AlinkClkGateOffThreshold> falling edge after ALClk_Enable is deasserted.						

MISCx30 CGPLLConfig7

Bits	Description										
31:30	CG2PLL_DS_ORDER. Read-write. Reset: 0. CG2_PLL DS order setting.										
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>disable</td> </tr> <tr> <td>1</td> <td>1st order</td> </tr> <tr> <td>2</td> <td>2nd order</td> </tr> <tr> <td>3</td> <td>3rd order</td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	disable	1	1st order	2	2nd order	3	3rd order
<u>Bits</u>	<u>Definition</u>										
0	disable										
1	1st order										
2	2nd order										
3	3rd order										
29	CG2PLL_SS_MODE. Read-write. Reset: 1. CG2_PLL Spread spectrum mode select. 0=Centre spread. 1=Down spread.										
28	CG2PLL_DS_PRBS_EN. Read-write. Reset: 0. Enable CG2_PLL PRBS17 generator in DS modulator.										
27:21	Reserved.										
20:14	CG2_PDIV_PCIECLK. Read-write. Reset: 12. CG2_PLL 100 MHz clock post divider (PCIE and SATA clock).										
	<table> <thead> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Bypass</td> </tr> <tr> <td>1</td> <td>Bypass</td> </tr> <tr> <td>7Fh-2h</td> <td>Divide by <CG2_PDIV_PCIECLK></td> </tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Bypass	1	Bypass	7Fh-2h	Divide by <CG2_PDIV_PCIECLK>		
<u>Bits</u>	<u>Definition</u>										
0	Bypass										
1	Bypass										
7Fh-2h	Divide by <CG2_PDIV_PCIECLK>										

13:7	CG2_PDIV_USB2CLK . Read-write. Reset: 25. CG2_PLL USB2 clock post divider (USB 2 48 MHz clock).								
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Bypass</td></tr> <tr> <td style="text-align: center;">1</td><td>Bypass</td></tr> <tr> <td style="text-align: center;">7Fh-2h</td><td>Divide by <CG2_PDIV_USB2CLK></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Bypass	1	Bypass	7Fh-2h	Divide by <CG2_PDIV_USB2CLK>
<u>Bits</u>	<u>Definition</u>								
0	Bypass								
1	Bypass								
7Fh-2h	Divide by <CG2_PDIV_USB2CLK>								
6:0	CG2_PDIV_CoreCLK . Read-write. Reset: 3. CG2_PLL 400 MHz clock post divider (core clock).								
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>Bypass</td></tr> <tr> <td style="text-align: center;">1</td><td>Bypass</td></tr> <tr> <td style="text-align: center;">7Fh-2h</td><td>Divide by <CG2_PDIV_CoreCLK></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	Bypass	1	Bypass	7Fh-2h	Divide by <CG2_PDIV_CoreCLK>
<u>Bits</u>	<u>Definition</u>								
0	Bypass								
1	Bypass								
7Fh-2h	Divide by <CG2_PDIV_CoreCLK>								

MISCx34 CGPLLConfig8

Bits	Description
31:16	CG2PLL_SS_STEP_SIZE_DSFRAC . Read-write. Reset: 0. CG2_PLL Spread spectrum step size DS control.
15:0	CG2PLL_DS_FRAC . Read-write. Reset: 0. CG2_PLL DS fractional setting.

MISCx38 CGPLLConfig9

Bits	Description
31	Reserved.
30	CG2PLL_CLKOUT3A_PDIVSEL . Read-write. Reset: 1. CG2_PLL CLKOUT3A select between RefClk (input of reference divider) and post divider 3. 0=Input of reference divider. 1=PDIV3 Output.
29	CG2PLL_CLKOUT2_PDIVSEL . Read-write. Reset: 1. CG2_PLL CLKOUT2 select between Ref-Clk (input of reference divider) and post divider 2. 0=Input of reference divider. 1=PDIV2 Output.
28	CG2PLL_CLKOUT1_PDIVSEL . Read-write. Reset: 1. CG2_PLL CLKOUT1 select between Ref-Clk (input of reference divider) and post divider 1. 0=Input of reference divider. 1=PDIV1 Output.
27:24	CG2PLL_SS_AMOUNT_NFRAC_SLIP . Read-write. Reset: 0. CG2_PLL spread spectrum amount fractional setting.
23:16	CG2PLL_SS_AMOUNT_FBDIV . Read-write. Reset: 0. CG2_PLL spread spectrum amount setting.
15:0	CG2PLL_SS_AMOUNT_DSFRAC . Read-write. Reset: 0. CG2_PLL spread spectrum amount DS setting.

MISCx3C CGPLLConfig10

Bits	Description						
30:27	CG2PLL_CP . Read-write. Reset: 2. CG2_PLL Charge pump control.						
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0000b</td><td>0uA</td></tr> <tr> <td style="text-align: center;">1111b-0001b</td><td><CG2PLL_CP*5uA></td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0000b	0uA	1111b-0001b	<CG2PLL_CP*5uA>
<u>Bits</u>	<u>Definition</u>						
0000b	0uA						
1111b-0001b	<CG2PLL_CP*5uA>						
26:18	CG2PLL_LF_MODE . Read-write. Reset: DEh. CG2_PLL Loop filter control. It defines the setting of loop filter R and C values.						

17:13	CG2PLL_CAL_MODE . Read-write. Reset: 5. CG2_PLL VCO calibration mode control.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0xxxxb</td><td>VCO mode set to calibrated values</td></tr> <tr> <td style="text-align: center;">1xxxxb</td><td>VCO mode forced to the value set in CORE_CG2PLL_CAL_MODE[3:0]</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0xxxxb	VCO mode set to calibrated values	1xxxxb	VCO mode forced to the value set in CORE_CG2PLL_CAL_MODE[3:0]				
<u>Bits</u>	<u>Definition</u>										
0xxxxb	VCO mode set to calibrated values										
1xxxxb	VCO mode forced to the value set in CORE_CG2PLL_CAL_MODE[3:0]										
12:11	CG2PLL_PCALREF . Read-write. Reset: 0. CG2_PLL VCO input2 control.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>close loop configuration</td></tr> <tr> <td style="text-align: center;">1</td><td>1/3 supply voltage</td></tr> <tr> <td style="text-align: center;">2</td><td>1/2 supply voltage</td></tr> <tr> <td style="text-align: center;">3</td><td>2/3 supply voltage</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	close loop configuration	1	1/3 supply voltage	2	1/2 supply voltage	3	2/3 supply voltage
<u>Bits</u>	<u>Definition</u>										
0	close loop configuration										
1	1/3 supply voltage										
2	1/2 supply voltage										
3	2/3 supply voltage										
10:9	CG2PLL_PVCOREF . Read-write. Reset: 0. CG2_PLL VCO input1control.										
	<table> <thead> <tr> <th style="text-align: center;"><u>Bits</u></th> <th style="text-align: center;"><u>Definition</u></th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td><td>close loop configuration</td></tr> <tr> <td style="text-align: center;">1</td><td>1/3 supply voltage</td></tr> <tr> <td style="text-align: center;">2</td><td>1/2 supply voltage</td></tr> <tr> <td style="text-align: center;">3</td><td>2/3 supply voltage</td></tr> </tbody> </table>	<u>Bits</u>	<u>Definition</u>	0	close loop configuration	1	1/3 supply voltage	2	1/2 supply voltage	3	2/3 supply voltage
<u>Bits</u>	<u>Definition</u>										
0	close loop configuration										
1	1/3 supply voltage										
2	1/2 supply voltage										
3	2/3 supply voltage										
8:0	Reserved.										

MISCx40 MiscClkCntl1

Bits	Description
31	CG2_Atomic_Update . Read-write; cleared-by-hardware. Reset: 0. 1=Request CG2_PLL to load FBDIV, FBDIV_Fraction, DS_FRAS value into CG2_PLL. The bit is cleared to 0 by hardware after request send to CG2_PLL.
30	CG1_Atomic_Update . Read-write; cleared-by-hardware. Reset: 0. 1=Request CG1_PLL to load FBDIV, FBDIV_Fraction, DS_FRAS value into CG1_PLL. The bit is cleared to 0 by hardware after request send to CG1_PLL.
29	Atomic_Update_R_Skip . Read-write. Reset: 0. 1=Hardware initializes CG1 and CG2 atomic update regardless whether CG_PLL is ready from previous update.
28:27	SDCLK_PDIVSEL . Read-write. Reset: 0. SDCLK Post divider selection.
26	CG1PLL_FBDIV_Test . Read-write. Reset: 0. 1=Enable loading MISCx10[CG1PLL_FBDIV] value for testing. A warm reset is required for this bit to take effect.
25:21	Reserved.
20	EnableBlinkClkSlowMode . Read-write. Reset: 0. 1=Enable internal core clock (B-Link clock) running at slower speed (66 MHz) for power saving. This bit only takes effect when MISCx40[1]== 1.
19	DrvStrAuxiliaryClk2 . Read-write. Reset: 1. Drive Strength Control for Auxiliary Clock2 (USB-CLK/14M_25M_48M_50M_OSC). 0=4 mA. 1=8 mA.
18	DrvStrAuxiliaryClk1 . Read-write. Reset: 1. Drive Strength Control for Auxiliary Clock1 (14M_25M_48M_50M_OSC). 0=4 mA. 1=8 mA.
17	Pwdn25Mxtal . Read-write. Reset: 0. 1=Power off 25M Xtal. 0=Power on 25M Xtal. Setting this bit to 1 can power off 25 MHz Xtal pad when the following conditions are not true. <ul style="list-style-type: none"> • chip in integrated clock mode. • USB 48 MHz clock from CG2_PLL. • SATA use CG2_PLL clock as ref clock source. • 14.318 MHz clock generated from CG2_PLL. • 25 MHz Auxiliary clock selected.

16	Reserved.
15	BlinkClkSlowEnable . Read-write. Reset: 0. 1=Internal B-Link clock runs on 66 MHz. The normal internal B-Link clock runs on 133 MHz. See more detail on MISCx40[20] .
14	OscClkSwitchEn . Read-write. Reset: 0. BIOS: 1. 1=The FCH uses the internal PLL to generate the 14 MHz OscClk.
13	InvertTermResistor . Read-write. Reset: 0. 1=Invert normal RefClk (NB_PCIE_CLK) termination. 0=Normal RefClk termination.
12	Auxiliary_14mClk_Sel . Read-write. Reset: 0. 14 MHz clock selection for Auxiliary clock output. 0=14.285 MHz clock is from CG2_PLL. 1=14.318 MHz clock is from CLK_REQG#/14M_OSC/GPIO65 pin.
11:8	Reserved.
7	OSCOUT2_OutOff . Read-write. Reset: 1. If USB uses internal 48 MHz as clock source, setting this bit to 1 will turn off USBCLK/OSCOUT2 clock output. 0=OSCOUT2 pin output enable. 1=OSCOUT2 pin output disable.
6	UsbClkCfg . Read-write. Reset: 1. Defines whether USB uses the internal or external 48 MHz clock. 0=External 48 MHz. 1=Internal 48 MHz. If USB uses internal 48 MHz as clock source, USBCLK/OSCOUT2 pin can output 14/24/48/50 MHz clock depending on OSCOUT2_sel setting. If USB uses external 48 MHz clock as clock source, USBCLK/OSCOUT2 pin cannot be used as auxiliary clock output. Output enable of OSCOUT2 pin is controlled by [UsbClkCfg] and [OSCOUT2_OutOff]. When [UsbClkCfg]=1 & [OSCOUT2_OutOff]=0, pin output enable will be on.
4	Usb3RefclkSel . Read-write. Reset: 1. BIOS: 0. USB3.0 reference clock source selection in internal clock mode. 0=100 MHz spread clock from internal CG1_PLL. 1=100 MHz non-spread clock from internal CG2_PLL.
2	OSCOUT1_ClkOutputEnb . Read-write. Reset: 1. 0=Enable Auxiliary Clock1 and OSCOUT1 clock output. 1=Disable.
1	CoreSpeedMode . Read-write. Reset: 0. Slow down Internal Core Clock (B-Link clock) for power saving. 0=Full speed B-Link clock. 1=Slow speed B-Link clock.
0	Reserved.

MISCx44 MiscClkCntl2

Bits	Description
31:20	Reserved.
19	CG2PLL_CLKOUT3B_CUSTOM_PDIV_EN . Read-write. Reset: 0. CG2_PLL CLKOUT3B (SATA 100 MHz) Post-dividers selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.
18	CG2PLL_CLKOUT3A_CUSTOM_PDIV_EN . Read-write. Reset: 0. CG2_PLL CLKOUT3A (PCIe 100 MHz) Post-dividers selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.
17	CG2PLL_CLKOUT2_CUSTOM_PDIV_EN . Read-write. Reset: 0. CG2_PLL CLKOUT2 (USB2 48 MHz) Post-dividers selection. 0=Use Programmable CMOS PostDIV inside digital block. 1=Use Custom CMOS Post-dividers.
16:10	Reserved.

9	CG1PLL_USB2_CLKOUT_EN . Read-write. Reset: 0. CG1_PLL USB2 28 MHz Clock Output Enable.
8	CG2_PLL_REFCLK_RESET . Read-write. Reset: 0.
7	CG1_PLL_REFCLK_RESET . Read-write. Reset: 0.
6	CG2PLL_ANTIGLITCH_RESET . Read-write. Reset: 0. Anti-glitch reset: Forced to 1 during CG2 PLL reset and set to 0 after reset.
5	CG1PLL_ANTIGLITCH_RESET . Read-write. Reset: 0. Anti-glitch reset: Forced to 1 during CG1 PLL reset and set to 0 after reset.
4	CG2_CAL_REFDIV_Update . Read-write. Reset: 0. 1=Update CG2_CAL_REFDIV from Register MISCx28 [CG2PLL_CAL_REFDIV]. A warm reset is required for this bit to take effect.
3	CG1_CAL_REFDIV_Update . Read-write. Reset: 0. 1=Update CG1_CAL_REFDIV from Register MISCx10 [CG1PLL_CAL_REFDIV]. A warm reset is required for this bit to take effect.
2	CG2_FBDIV_Test . Read-write. Reset: 0. Enable loading MISCx24 [CG2PLL_FBDIV] value for testing. A warm reset is required for this bit to take effect. 0=Disable. 1=Enable.
1	CG2_FBDIV_LoadEn . Read-write. Reset: 0. 1=Enable loading CG2PLL_FBDIV value form register MISCx24 [CG2PLL_FBDIV].
0	CG1_FBDIV_LoadEn . Read-write. Reset: 0. 1=Enable loading CG1PLL_FBDIV value from register MISCx10 [CG1PLL_FBDIV].

MISCx48 MiscClkCtl3

Bits	Description
31:30	CG2PLL_CLKOUT3B_DIFF_GAIN . Read-write. Reset: 2. Diff CML Driver Strength Control for CG2PLL_CLKGEN_SATA_P/N.
29:28	Cg2PllXtalDpllDiffGain . Read-write. Reset: 10b. Diff CML driver strength control for XTAL_DPLL_REFCLK_P/N (48Mhz).
27:26	CG2PLL_CLKOUT3A_DIFF_PRE_GAIN . Read-write. Reset: 3. Diff CML Pre-Driver Strength Control for CG2PLL_DPLL_REFCLK_P/N and CG2PLL_CLKGEN_SATA_P/N.
25:24	CG2PLL_CLKOUT3A_DIFF_GAIN . Read-write. Reset: 2. Diff CML Driver Strength Control for CG2PLL_CLKGEN_PCIE_USB3_P/N.
23:22	CG2PLL_CLKOUT2_DIFF_GAIN . Read-write. Reset: 2. Diff CML Driver Strength Control for CG2PLL_CLKGEN_USB2_P/N.
21:20	Cg1PllSataUsb2DiffGain . Read-write. Reset: 10b. Diff CML driver strength control for CG1PLL_SATA_USB2_P/N (48Mhz).
19:16	Reserved.
15:14	CG1PLL_CLKOUT3A_DIFF_GAIN . Read-write. Reset: 2. Diff CML Driver Strength Control for CG1PLL_CLKGEN_PCIE_CPU_USB3_P/N
13:12	CG1PLL_CLKOUT2_DIFF_GAIN . Read-write. Reset: 2. Diff CML Driver Strength Control for CG1PLL_CLKGEN_USB2_P/N.
11:6	CG2PLL_SPARE . Read-write. Reset: 0. CG2_PLL general spare pins.
5	Reserved.

4:3	Cg1XtalCmlPreDiffGain. Read-write. Reset: 10b. CG1_PLL CML driver strength selection for both SATA2/USB and DPLL_REFCLK output drivers.
2:0	CG2PLL_DIG_SPARE. Read-write. Reset: 0. CG2_PLL spare pins to digital block.

MISCx4C MiscClkCtl4

Bits	Description
31	LowPowerDisplay400MClkEnB. Read-write. Reset: 0. Non Sticky bit. 0=Enable low power display 400Mhz clock output. 1=Disable.
30	LowPowerDisplay300MClkEnB. Read-write. Reset: 0. Non Sticky bit. 0=Enable low power display 300Mhz clock output. 1=Disable.
29:0	Reserved.

MISCx60 IdleCntrl

Bits	Description										
31:24	IdleCount. Read-write. Reset: X. This returns the idle count from the latest monitored period.										
23:16	Reserved.										
15:8	IdleThreshold. Read-write. Reset: 80h. This defines the idle-ness threshold when the dynamic clock logic down shifts the clock frequency. Each unit represents 1/256 of the interval.										
7:6	Reserved. Read-write.										
5	DFSlowSpeedSel. Read-write. Reset: 0. Dynamic frequency Slow Speed selection. It selects clock speed to run at either 50% of full speed or 25% of full speed. 0=50% of full speed. 1=25% of full speed.										
4	ForceSlowFreq. Read-write. Reset: 0. 1=Force core logic clock (Secondary PCI, internal A-link, and B-link clock frequency) to run at 50% or 25% of full speed as defined by [DFSlowSpeedSel] when [IdleMonEn] is 0.										
3:2	IdlePeriodSel. Read-write. Reset: 1. Select interval for monitoring. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>53.76 us</td> </tr> <tr> <td>01b</td> <td>302 us</td> </tr> <tr> <td>10b</td> <td>2.29 ms</td> </tr> <tr> <td>11b</td> <td>18.3 ms</td> </tr> </tbody> </table>	Bits	Definition	00b	53.76 us	01b	302 us	10b	2.29 ms	11b	18.3 ms
Bits	Definition										
00b	53.76 us										
01b	302 us										
10b	2.29 ms										
11b	18.3 ms										
1	IdleMonCEn. Read-write. Reset: 0. 1=The dynamic clock frequency logic only considers the chip to be in idle state when CPU is in the C state.										
0	IdleMonEn. Read-write. Reset: 0. Control the dynamic clock frequency logic. When the dynamic clock frequency logic is enabled, it will monitor the amount of idle-ness defined by [IdleThreshold] within a period defined by [IdlePeriodSel]. Whenever the condition is met, it will down shift the internal clock (Secondary PCI, A-link, and B-link clock frequency) as defined by [DFSlowSpeedSel]. 0=Disable. 1=Enable.										

MISCx68 Memory Power Saving Control (MemPwrSavCntrl)

Bits	Description
29:28	Reserved. Reset: 11b.
27:20	Reserved. Reset: 7Fh.
19	Reserved. Reset: 1.
15:5	Reserved. Reset: 7FFh.
3	Reserved. Reset: 1.
2	ABBypassMemDsd . Read-write. Reset: 1. BIOS: See 2.15.11.2 . AB memory BypassMemdsd control. 0=Enable memory deep sleep and shutdown features. 1=Disable memory deep sleep and shutdown.

MISCx70 OscFreqCounter

Bits	Description
31	CountEnable . Read-write. Reset: 0b. 1=Enable the internal counter to count the number of OSC clocks. When SW is not using this function, it should always set it back to 0 to conserve power.
30	CountIsValid . Read-only. Reset: 0b. 1=OscCountPerSec is valid. SW should always wait for this bit to be set before it reads OscCountPerSec.
29:28	Reserved.
27:0	OscCountPerSec . Read-write. Reset: 0000000h. Number of OSC clocks per 1 second. Whenever [CountEnable] is set, an internal counter will start counting the number of OSC clocks per second and record the count value here.

MISCx74 HpetClkPeriod

Bits	Description
31:0	HpetClkPeriod . Read-write. Reset: 0429B17Eh. The register controls the value of HPETx004[CounterClkPeriod] register in HPET MMIO register space.

MISCx78 PostCode

Bits	Description
31:0	PostCode[31:0] . Read-only; S3-check-exclude. Reset: 0. BIOS 32 bit writes to IO080 [PostCode] go to this internal 32-bit PostCode Register. Reads from IO080 [PostCode] return PostCode[7:0]. If MISCx6C[PostCodeWidthSel]==1 , Read from this register returns {24'b0, PostCode[7:0]}. If MISCx6C[PostCodeWidthSel]==0 , Read from this register returns PostCode[31:0].

MISCx80 StrapStatus

Bits	Description
31:19	Reserved.

18	BifGen2ComplianceStrap . Read-only. Reset: 0. BIF gen 2 compliance strap.
17	ClkGenStrap . Read-only. Reset: X. BIOS: See 2.15.9 . 1==Internal clocking mode; Use 48MHz crystal clock as the reference clock. 0=External clocking mode; Use 100MHz differential spread clock as the reference clock.
16	BootFailTmrEnStrap . Read-only. Reset: X. Enable Watchdog function.
15	PciRomBootStrap . Read-only. Reset: 1. PCI ROM Boot.
14:13	Reserved.
12	CPUClkSelStrap . Read-only. Reset: 0.
11	ShortResetStrap . Read-only. Reset: 0. Generate short reset
10	PciPllBypStrap . Read-only. Reset: 0. Bypass PCI PLL (used in functional test at tester).
9	SDPllBypStrap . Read-only. Reset: 0.
8	Reserved.
7	I2CRomStrap . Read-only. Reset: 0. Getting UMI core strap from I2C ROM or using default value.
6	Reserved.
4:3	Reserved.
2	EcEnableStrap . Read-only. Reset: 0. BIOS: See 2.15.8 . 1=IMC is enabled.
1	UseLpcRomStrap . Read-only. Reset: X.
0	Reserved.

MISCx90 AutoTransaction/Allow EC

Bits	Description										
9	DisableAuto . Read; write-1-only. Reset: 0. 1=The entire Auto Transaction logic is disabled. Once this bit is set, it cannot be cleared except by system reset.										
8	AllowECToAutoTransactEn . Read-write. Reset: 0. Only BIOS can change this bit. 0= IMC cannot write to any of registers MISCx90/MISCx94/MISCx98/MISCx9C in the Auto Transaction Generation logic. 1=IMC can change any of these registers.										
7:4	TransactionType . Read-write. Reset: 0. PCI Command type used for this auto transaction. See PCI specification for PCI command types.										
3:2	ByteCount . Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1 byte</td> </tr> <tr> <td>01b</td> <td>2 bytes</td> </tr> <tr> <td>10b</td> <td>4 bytes</td> </tr> <tr> <td>11b</td> <td>4 bytes</td> </tr> </tbody> </table>	Bits	Definition	00b	1 byte	01b	2 bytes	10b	4 bytes	11b	4 bytes
Bits	Definition										
00b	1 byte										
01b	2 bytes										
10b	4 bytes										
11b	4 bytes										
1	DualAddr . Read-write. Reset: 0. 0=Use single address cycle. 1=Use dual address cycle.										
0	AutoExecute . Read-write; cleared-by-hardware. Reset: 0. Writing 1 to this bit causes the HW to execute the transaction defined by bit[7:1]. Once it is written, this bit stays as 1 until the transaction is completed, in which case it will return to 0.										

MISCx94 AutoAddrLow

Bits	Description
31:0	AutoAddrLow . Read-write. Reset: 0. Low address to be used by the MISCx90[AutoExecute] operation.

MISCx98 AutoAddrHigh

Bits	Description
31:0	AutoAddrHigh . Read-write. Reset: 0. High address to be used by the MISCx90[AutoExecute] operation. This register is only applicable when MISCx90[DualAddr] == 1 .

MISCx9C AutoData

Bits	Description
31:0	AutoData . Read-write. Reset: 0. If MISCx90[TransactionType] is read, this register will return the read data. If the MISCx90[TransactionType] is a write command, this register will contain the write data. Note byte is aligned accordingly.

MISCxC0 CPU Pstate0

Bits	Description																		
31:15	Reserved.																		
14:12	Core3Pstate . Read-only. Reset: 0. See: Core0Pstate.																		
11	Reserved.																		
10:8	Core2Pstate . Read-only. Reset: 0. See: Core0Pstate.																		
7	Reserved.																		
6:4	Core1Pstate . Read-only. Reset: 0. See: Core0Pstate.																		
3	Reserved.																		
2:0	Core0Pstate . Read-only. Reset: 0. FCH will monitor the P state of each CPU core. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>P0</td> </tr> <tr> <td>001b</td> <td>P1</td> </tr> <tr> <td>010b</td> <td>P2</td> </tr> <tr> <td>011b</td> <td>P3</td> </tr> <tr> <td>100b</td> <td>P4</td> </tr> <tr> <td>101b</td> <td>P5</td> </tr> <tr> <td>110b</td> <td>P6</td> </tr> <tr> <td>111b</td> <td>P7</td> </tr> </tbody> </table>	Bits	Definition	000b	P0	001b	P1	010b	P2	011b	P3	100b	P4	101b	P5	110b	P6	111b	P7
Bits	Definition																		
000b	P0																		
001b	P1																		
010b	P2																		
011b	P3																		
100b	P4																		
101b	P5																		
110b	P6																		
111b	P7																		

MISCxC4 CPU Pstate1

Bits	Description
31:0	Reserved.

MISCxD0 CPU Cstate0

Bits	Description
31:15	Reserved.
14:12	Core3Cstate . Read-only. Reset: 0. See: Core0Cstate.
11	Reserved.
10:8	Core2Cstate . Read-only. Reset: 0. See: Core0Cstate.
7	Reserved.
6:4	Core1Cstate . Read-only. Reset: 0. See: Core0Cstate.
3	Reserved.
2:0	Core0Cstate . Read-only. Reset: 0. <u>Bits</u> <u>Definition</u> 000b C0 001b C1 010b C2 011b C3 100b C4 101b C5 110b C6 111b C7

MISCxD4 CPU Cstate1

Bits	Description
31:0	Reserved.

MISCxF0 SataPortSts

Bits	Description
31:26	Reserved.
25:24	SataPortSel . Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b Select “led” for Port 0 to 1 01b Select “det” for Port 0 to 1 10b Select “err” for Port 0 to 1 11b Select “led” for Port 0 to 1
23:2	Reserved.

1	Port1Sts. Read-write; S3-check-exclude. Reset: X. The selected status of Port 1. This status bit indicates the internal status of SATA port 1.
0	Port0Sts. Read-write; S3-check-exclude. Reset: X. The selected status of Port 0. This status bit indicates the internal status of SATA port 0.

MISCxF4_ClkCntrlSts

Bits	Description

3.26.12 GPIO Pin control registers

The GPIO pins are controlled by a combination of device enables and by their specific **GPIOx[E4:00]** and **IOMUXx[E4:00]** register pair.

3.26.12.1 GPIO Registers

GPIO register space is accessed through the AcpiMmio region, which can be memory mapped or IO mapped. The registers range from **PMx24[AcpiMmioAddr]+100h** to **PMx24[AcpiMmioAddr]+1FFh**. See **PMx24 [AcpiMmioEn]**.

GPIOx[E4:00] GPIO

BIOS: See [2.15.6](#).

Bits	Description
7	GpioIn. Read-only; updated-by-hardware. Reset: 0. Current pin state.
6	GpioOut. Read-write; S3-check-exclude. Reset: 0. Output state when GpioOutEnB is enabled.
5	GpioOutEnB. Read-write. Reset: 1. 0=Output enable. 1=Output disable.
4	PullDown. Read-write. Reset: 0. 0=Pull down disabled. 1=Pull down enabled.
3	PullUpB. Read-write. Reset: 0. 1=Pull up disabled. 0=Pull up enabled.
2	Sticky. Read-write. Reset: 0. 1=Bits[6:3] are sticky and can be reloaded to the default value on PCI reset. 0=Bits [6:3] can be reloaded to the default value on RsmRst and SYS_RST#. This will allow every GPIO to be sticky or non-sticky.
1	OwnedByHost. Read-write. Reset: 0. This bit can only be written by host (BIOS). If this bit is set, only host can write to bits[6:2] and bit 0 can no longer be written by IMC. This bit is always sticky.
0	OwnedByEc. Read-write. Reset: 0. This bit can only be written by IMC. If this bit is set, only IMC can write to bits[6:2] and bit 1 can no longer be written by host. This bit is always sticky.

3.26.12.2 IOMUX Registers

IOMUX register space is accessed through the AcpiMmio region, which can be memory mapped or IO mapped. The registers range from **PMx24[AcpiMmioAddr]+D00h** to **PMx24[AcpiMmioAddr]+DFFh**. See **PMx24 [AcpiMmioEn]**.

IOMUXx[E4:00] IoMux

Table 236: Reset Mapping for IOMUXx[E4:00]

Register	Reset	Register	Reset	Register	Reset	Register	Reset
IOMUXx[1F:00]	00h	IOMUXx3D	00h	IOMUXx60	00h	IOMUXx75	00h
IOMUXx20	00h	IOMUXx3E	00h	IOMUXx61	00h	IOMUXx76	00h
IOMUXx21	00h	IOMUXx3F	00h	IOMUXx62	02h	IOMUXx77	00h
IOMUXx[2A:22]	00h	IOMUXx40	02h	IOMUXx63	00h	IOMUXx[A0:78]	00h
IOMUXx2B	00h	IOMUXx41	00h	IOMUXx64	01h	IOMUXxA1	00h
IOMUXx2C	00h	IOMUXx42	00h	IOMUXx65	01h	IOMUXxA2	00h
IOMUXx2D	01h	IOMUXx43	00h	IOMUXx66	01h	IOMUXxA3	00h
IOMUXx2E	00h	IOMUXx44	00h	IOMUXx67	01h	IOMUXxA4	00h
IOMUXx2F	00h	IOMUXx45	00h	IOMUXx68	00h	IOMUXxA5	00h
IOMUXx30	00h	IOMUXx46	00h	IOMUXx69	00h	IOMUXxA6	00h
IOMUXx31	00h	IOMUXx47	00h	IOMUXx6A	01h	IOMUXxA7	00h
IOMUXx32	02h	IOMUXx48	00h	IOMUXx6B	01h	IOMUXxA8	00h
IOMUXx33	02h	IOMUXx49	00h	IOMUXx6C	00h	IOMUXxA9	00h
IOMUXx34	00h	IOMUXx4A	00h	IOMUXx6D	00h	IOMUXxAA	00h
IOMUXx[36:35]	00h	IOMUXx4B	00h	IOMUXx6E	00h	IOMUXx[AD:AB]	00h
IOMUXx37	02h	IOMUXx4C	00h	IOMUXx6F	00h	IOMUXxAE	00h
IOMUXx38	00h	IOMUXx4D	00h	IOMUXx70	01h	IOMUXx[B7:AF]	00h
IOMUXx39	01h	IOMUXx4E	00h	IOMUXx71	02h	IOMUXxB8	00h
IOMUXx3A	01h	IOMUXx4F	00h	IOMUXx72	00h	IOMUXx[E2:B9]	00h
IOMUXx3B	02h	IOMUXx50	00h	IOMUXx73	00h	IOMUXxE3	00h
IOMUXx3C	00h	IOMUXx[5F:51]	00h	IOMUXx74	00h	IOMUXxE4	00h

Bits	Description										
7:2	Reserved.										
1:0	IOMuxGPIO. Read-write. Multi-function IO pin function select for pin GPIO[X]. <table style="margin-left: 20px;"> <tr> <th><u>Bits</u></th> <th><u>Definition</u></th> </tr> <tr> <td>00b</td> <td>function 0</td> </tr> <tr> <td>01b</td> <td>function 1</td> </tr> <tr> <td>10b</td> <td>function 2</td> </tr> <tr> <td>11b</td> <td>function 3</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	00b	function 0	01b	function 1	10b	function 2	11b	function 3
<u>Bits</u>	<u>Definition</u>										
00b	function 0										
01b	function 1										
10b	function 2										
11b	function 3										

3.26.13 Power Management (PM) Registers

PM register space is accessed through two methods:

- Indirect IO access through **IOCD6 [PM_Index]** and **IOCD7 [PM_Data]**. Software first programs the offset into the index register **IOCD6** and then reads from/writes to the data register **IOCD7**.
- Direct memory mapped or IO mapped access through the AcpiMmio region. The PM registers range from **PMx24[AcpiMmioAddr]+300h** to **PMx24[AcpiMmioAddr]+3FFh**. See **PMx24** for details on how to set up the AcpiMmio region.

PMx00 DecodeEn

Bits	Description
31	Reserved.
30	Port92Enable . Read-write. Reset: 1. 1=Enable the decoding of IO Port 92h.
29:28	Reserved. Read-write. Reset: 0. Spare bits.
27:26	Reserved.
25	PMAddrEnable . Read-write. Reset: 1. 1=Enable the decoding of IO Port CD6h and CD7h.
24:20	Reserved.
19	RtcAddrEn . Read-write. Reset: 1. 1=Enable the decoding of IO Port 70h and 71h.
18	NmiAddrEn . Read-write. Reset: 1. 1=Enable the decoding of IO Port 61h.
17	PitAddrEn . Read-write. Reset: 1. 1=Enable the decoding of IO Port 40h, 41h, 42h, 43h.
16	DmaAddrEn . Read-write. Reset: 1. 1=Enable the decoding of IO Port 1Fh:00h, 8Fh:80h, CFh:C0h, DFh:D0h.
15:8	Reserved.
5:4	Reserved.
3	PmEnable . Read-write. Reset: 1. 1=Enable IO port CD6h and CD7h decoding on the internal ISA bus. This bit has to be set all the time.
2	TmrEnable . Read-write. Reset: 1. 1=Enable 8254 timer function.
1	IntrEnable . Read-write. Reset: 1. 1=Enable PIC interrupt function.
0	Reserved. Read-write. Reset: 0. This is an obsolete function; BIOS should leave it as 0.

PMx04 IsaControl

Bits	Description
16	ABLinkClkGateEn . Read-write. Reset: 0. BIOS: See 2.15.9.2 [Global A-Link / B-Link Clock Gating] . Specifies the master switch for A-link and B-link clock gating. This bit is non-sticky. 1=A-link/B-link clock gating global enable.
15:12	Reserved.
7	DmaLimitEn . Read-write. Reset: 0. 1=Enable DmaLimit on legacy DMA transfers on the LPC bus.
6:0	DmaLimit . Read-write. Reset: 0. Specifies the legacy DMA transfer size.

PMx08 PciControl

Bits	Description
31:26	Reserved.
25	ForceSlpStateRetry . Read-write. Reset: 0. 1=Send out SMI message before the completion response of IO writes to AcpiPm1CntBlkx00[SlpTyp] . This is to be used in conjunction with SMI trapping on writes to AcpiPm1CntBlkx00[SlpTyp] .
24	ForceStpClkRetry . Read-write. Reset: 1. 1=Send out STPCLK message before the completion response to the following 3 types of requests: <ul style="list-style-type: none">• IO writes to AcpiPm1CntBlkx00[SlpTyp].• IO write LDT_STP command.• C1e cycle. Normally it is required to send out STPCLK before completion of the cycles listed above, except for the case of SMI trapping. In the case of SMI trapping, this bit should be programmed as 0.
23	AbStallEn . Read-write. Reset: 0. 1=Allow the legacy DMA engine to hold the internal bus before completing legacy DMA on the LPC bus. This is only needed for certain old LPC devices.
22:20	Reserved.
19	MasterNoWait . Read-write. Reset: 0. 1=ACPI PCI Master doesn't wait for Slave idle when it wants to request bus. 0=PCI Master will wait for Slave idle.
18:15	Reserved.
14:12	ExtIntrTime . Read-write. Reset: 0. Specifies the extended interrupt time in 2 microsecond intervals. This is used for preventing APU from re-entering C state right away when it just breaks out from a C state.
11	Reserved.
9	Reserved.
8	PicApicArbiter . Read-write. Reset: 1. 1=Enable arbitration between PIC request and IOAPIC request.
7	ForceSmafMatch . Read-write. Reset: 0. 1=Enable STPGNT message matching to the expected SMAF.
6	MtsAuto . Read-write. Reset: 0. 1=Encode PIC interrupt request as legacy PIC ExtInt message type and PIC NMI request as legacy PIC NMI message type if IOAPIC is enabled && MtsSet==0.
5	MtsSet . Read-write. Reset: 1. 1=Encode PIC interrupt request as legacy PIC ExtInt message type and NMI request as legacy NMI message type. 0=Encode PIC interrupt request as ExtInt message type and NMI request as NMI message type.
4	MsgIntrEnable . Read-write. Reset: 0. 1=Deliver legacy PIC interrupt as message type.
3	MaskMsgBmStsEn . Read-write. Reset: 0. 1=Enable A20#, IGNNE#, INIT#, NMI, SMI# message delivery.
2	DmaVerifyEn . Read-write. Reset: 0. 1=Enable mimicking of legacy DMA VERIFY function. This is only needed for old LPC driver, such as floppy, that requires VERIFY function.
1	Reserved.
0	ArbDmaDis . Read-write. Reset: 0. BIOS: See 2.15.4.1 . 1=Enable arbitration between legacy DMA and other PCI masters. 0=Disable arbitration between legacy DMA and other PCI masters.

PMx0C StpClkSmaf

Bits	Description
31	Reserved.
30:28	TtSmaf . Read-write. Reset: 5h. Specifies the system management action field for thermal throttling STPCLK message.
27	Reserved.
26:24	NsSmaf . Read-write. Reset: 5h. Specifies the system management action field for normal throttling STPCLK message.
23	Reserved.
22:20	S3Smaf . Read-write. Reset: 4h. Specifies the system management action field for S3 STPCLK message.
19	Reserved.
18:16	S1Smaf . Read-write. Reset: 3h. Specifies the system management action field for S1 STPCLK message.
15	Reserved.
14:12	VfSmaf . Read-write. Reset: 2h. Specifies the system management action field for VFID STPCLK message.
11	Reserved.
10:8	C3Smaf . Read-write. Reset: 1. Specifies the system management action field for C3 STPCLK message.
7	Reserved.
6:4	C2Smaf . Read-write. Reset: 0. Specifies the system management action field for C2 STPCLK message.
3	Reserved.
2:0	S4S5Smaf . Read-write. Reset: 6h. Specifies the system management action field for S4/5 STPCLK message.

PMx20 BiosRamEn

Bits	Description
31:8	BiosRamMemAddr . Read-write. Reset: FED100h. Specifies the BIOS RAM base address[31:8].
7:2	Reserved.
1	BiosRamMemPmEnable . Read-write. Reset: 0. 1=Enable BIOS RAM auto-deep-sleep mode.
0	BiosRamMemEnable . Read-write. Reset: 0. 1=Enable BIOS RAM access.

PMx24 AcpiMmioEn

The AcpiMmio region mapping is disabled at initial power up. Software needs to program it using the indirect IO access through the index register [IOCD6 \[PM_Index\]](#) and the data register [IOCD7 \[PM_Data\]](#):

1. Select the AcpiMmio region to be memory mapped or IO mapped through [PMx24\[AcpiMmioSel\]](#)
2. Program the base address through [PMx24\[AcpiMmioAddr\]](#).
3. Enable the direct mapping through [PMx24\[AcpiMmioDecodeEn\]](#).

Bits	Description																																						
31:13	AcpIMmioAddr. Read-write. Reset: 7F6C0h. Specifies the base address[31:13] of the AcpIMmio region for FCH resources. The AcpIMmio base address is FED8_0000h at default. The following lists the offsets of various register blocks within this region: <table> <tr> <td>00FFh-0000h</td><td>SMBus PCI configuration registers, see D14F0x00.</td></tr> <tr> <td>01FFh-0100h</td><td>GPIO, see GPIOx[E4:00]</td></tr> <tr> <td>02FFh-0200h</td><td>SMI, see SMIx00.</td></tr> <tr> <td>03FFh-0300h</td><td>PMIO, see PMx00.</td></tr> <tr> <td>04FFh-0400h</td><td>PMIO2, see PM2x00.</td></tr> <tr> <td>05FFh-0500h</td><td>BIOS RAM</td></tr> <tr> <td>06FFh-0600h</td><td>CMOS RAM, see IO073_x00.</td></tr> <tr> <td>07FFh-0700h</td><td>CMOS</td></tr> <tr> <td>08FFh-0800h</td><td>ACPI, see 3.26.15 [Standard ACPI Registers].</td></tr> <tr> <td>09FFh-0900h</td><td>ASF registers, see ASFx00.</td></tr> <tr> <td>0AFFh-0A00h</td><td>SMBus registers, see SMBUSx00</td></tr> <tr> <td>0BFFh-0B00h</td><td>Watchdog registers, see WDTx00.</td></tr> <tr> <td>0CFFh-0C00h</td><td>HPET, see HPETx000.</td></tr> <tr> <td>0DFFh-0D00h</td><td>IOMUX, see IOMUXx[E4:00].</td></tr> <tr> <td>0EFFh-0E00h</td><td>Miscellaneous registers, see MISCx00.</td></tr> <tr> <td>10FFh-1000h</td><td>Serial Debug bus, see SBDx00.</td></tr> <tr> <td>1CFFh-1C00h</td><td>USB3 Phy, see XHCI_PMx00.</td></tr> <tr> <td>1DFFh-1D00h</td><td>Wake Device (AC DC timer), see AcDcTimerx00.</td></tr> <tr> <td>1EFFh-1E00h</td><td>AOAC Registers, see AOACx00.</td></tr> </table>	00FFh-0000h	SMBus PCI configuration registers, see D14F0x00 .	01FFh-0100h	GPIO, see GPIOx[E4:00]	02FFh-0200h	SMI, see SMIx00 .	03FFh-0300h	PMIO, see PMx00 .	04FFh-0400h	PMIO2, see PM2x00 .	05FFh-0500h	BIOS RAM	06FFh-0600h	CMOS RAM, see IO073_x00 .	07FFh-0700h	CMOS	08FFh-0800h	ACPI, see 3.26.15 [Standard ACPI Registers] .	09FFh-0900h	ASF registers, see ASFx00 .	0AFFh-0A00h	SMBus registers, see SMBUSx00	0BFFh-0B00h	Watchdog registers, see WDTx00 .	0CFFh-0C00h	HPET, see HPETx000 .	0DFFh-0D00h	IOMUX, see IOMUXx[E4:00] .	0EFFh-0E00h	Miscellaneous registers, see MISCx00 .	10FFh-1000h	Serial Debug bus, see SBDx00 .	1CFFh-1C00h	USB3 Phy, see XHCI_PMx00 .	1DFFh-1D00h	Wake Device (AC DC timer), see AcDcTimerx00 .	1EFFh-1E00h	AOAC Registers, see AOACx00 .
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1EFFh-1E00h	AOAC Registers, see AOACx00 .																																						
12:2	Reserved.																																						
1	AcpIMmioSel. Read-write. Reset: 0. Selects the AcpIMmio region to be in memory-mapped or IO-mapped space. 0=Memory mapped space. 1=IO mapped space.																																						
0	AcpIMmioDecodeEn. Read-write. Reset: 0. BIOS: 1. 1=Enable the AcpIMmio space.																																						

PMx28 AsfEn

Bits	Description																								
31:24	Reserved.																								
23	AsfClkSwitchEn. Read-write. Cold reset: 0. 1=Change ASF master clock from RTC (32 kHz) to the clock defined in AsfClkSel.																								
22:16	AsfClkSel. Read-write. Cold reset: 0. Specifies the frequency of ASF master clock. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>~100 kHz</td> <td>5h</td> <td>~800 kHz</td> </tr> <tr> <td>1h</td> <td>~200 kHz</td> <td>6h</td> <td>~900 kHz</td> </tr> <tr> <td>2h</td> <td>~300 kHz</td> <td>7h</td> <td>~1 MHz</td> </tr> <tr> <td>3h</td> <td>~400 kHz</td> <td>7Fh-8h</td> <td>66.67 MHz / ((AsfClkSel + 1) * 2)</td> </tr> <tr> <td>4h</td> <td>~600 kHz</td> <td></td> <td></td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	0h	~100 kHz	5h	~800 kHz	1h	~200 kHz	6h	~900 kHz	2h	~300 kHz	7h	~1 MHz	3h	~400 kHz	7Fh-8h	66.67 MHz / ((AsfClkSel + 1) * 2)	4h	~600 kHz		
Bits	Definition	Bits	Definition																						
0h	~100 kHz	5h	~800 kHz																						
1h	~200 kHz	6h	~900 kHz																						
2h	~300 kHz	7h	~1 MHz																						
3h	~400 kHz	7Fh-8h	66.67 MHz / ((AsfClkSel + 1) * 2)																						
4h	~600 kHz																								
15:5	AsfIoBase. Read-write. Cold reset: 590h. Specifies AsfIoBase[15:5]. AsfIoBase is B20h at default.																								
4:3	Reserved.																								
2	AsfSmMasterEn. Read-write. Cold reset: 0. 1=Enable ASF SMBUS master function.																								

1	AsfClkStretchEn . Read-write. Cold reset: 0. 1=Enable clock stretching support.
0	AsfEn . Read-write. Cold reset: 0. 1=Enable ASF function and IO decoding.

PMx2C Smbus0En

Bits	Description
15:5	SmBus0IoBase . Read-write. Cold reset: 580h. Specifies Smbus0IoBase[15:5]. Smbus0IoBase is B00h at default.
4:1	Reserved.
0	SmBus0En . Read-write. Cold reset: 0. 1=Enable SMBUS0 function and IO decoding.

PMx2E Smbus0Sel

Bits	Description								
7:3	Reserved.								
2:1	SmBus0Sel . Read-write. Reset: 0. SmBus port selection. There is only one SMBUS engine controlling up to four SMBUS ports (port 3&4 are not used). This register routes the SMBUS engine to the desired port. Port1 is always controlled by ASF, which has its dedicated SMBUS engine. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>Port 0</td> </tr> <tr> <td>01b</td> <td>Port 2</td> </tr> <tr> <td>11b-10b</td> <td>Reserved</td> </tr> </table>	Bits	Definition	00b	Port 0	01b	Port 2	11b-10b	Reserved
Bits	Definition								
00b	Port 0								
01b	Port 2								
11b-10b	Reserved								
0	Reserved.								

PMx2F SmbusSlpGate

Bits	Description
7:6	Reserved.
5	SmBusSlpGate[1] . Read-write. Reset:0. 1=Gate-off SmBus Port2 during S3/S5 if (PMx2E[SmBus0Sel]==01b). 0=No gate-off during S3/S5.
4	SmBusSlpGate[0] . Read-write. Reset:0. 1=Gate-off SmBus Port0 during S3/S5 if (PMx2E[SmBus0Sel]==00b). 0=No gate-off during S3/S5.
3:0	Reserved.

PMx34 IoApicEn

Bits	Description
31:5	IoApicBaseAddr . Read-write. Reset: 7F60000h. Specifies IOAPIC base address[31:5]. IOAPIC base address[31:0] is FEC0_0000h at default.
4	IoApicIdExtEn . Read-write. Reset: 1. 1=Extend APIC ID defined at IOAPICx10_x00 [ID] from 4 bits to 8 bits.
3	Reserved.

2	IoApicMmIo . Read-write. Reset: 1. 0=IO space. 1=Memory space.
1	IoApicMode . Read-write. Reset: 1. 1=Enable IOxAPIC. This bit is only valid if (IoApicEnable==1).
0	IoApicEnable . Read-write. Reset: 0. 1=Enable IOAPIC decoding.

PMx44 BootTimerEn

Bits	Description
31	BootTmrDisable . Read-write. Cold reset: 0. BIOS: 1. 0=Boot timer starts running. 1=Boot timer is stopped; it will not trigger a system reset or de-assertion on the NbPwrGood. Software should set the bit to 1 after every reset or S3/S4/S5 resume before the timer expires in 1.17 s.
30	FailBootRstSts . Write-1-to-clear; Read. Cold reset: 0. 0=Boot timer has not been fired. 1=Boot timer has been fired.
29	ExpireBootTmr . Read-write. Cold reset: 0. 1=Force boot timer to expire; then NbPwrGood can be asserted.
28	BootTmrStopOnGAlink . Read-write. Cold reset: 1. BIOS: 0. 0=Enable the boot timer to ensure a good boot. 1=Boot timer stops when FCH observes a good boot after PCI reset or S3/S4/S5 resume.
27	BootTmrFuncEn . Read-write. Cold reset: 1. BIOS: 1. 0=Disable boot timer function; avoid system restarts when performing BIOS debug. 1=Enable boot timer function; the boot timer starts to count down and will toggle NbPwrGood after 1.17 s if software has not set ExpireBootTmr to 1 after PCI reset or resuming from S3/S4/S5.
26:25	Reserved.
24:0	FailBootTimer . Read-write. Cold reset: 0. Specifies the counter of APU boot timer (14.318 MHz), which starts counting when both of the following conditions are met: <ul style="list-style-type: none"> • BootTmrDisable==1. • PCI reset is not asserted.

PMx48 WatchdogTimerEn

Bits	Description
31:3	WatchdogBase . Read-write. Cold reset: 1FD60000h. Specifies the watchdog timer memory mapped base address[31:3]. The base address is FEBO_0000h at default.
2	Reserved.
1	WatchdogFuncDisable . Read-write. Cold reset: 1. 0=Enable watchdog timer. 1=Disable watchdog timer.
0	WatchdogDecodeEn . Read-write. Cold reset: 0. 1=Enable decoding of watchdog timer address. This watchdog timer is a standard defined by Microsoft.

PMx4C WatchdogTimerConfig

Bits	Description

7:2	Reserved. WatchdogOptions. Read-write. Reset: 0.			
1:0	WatchdogFreq . Read-write. Cold reset: 3h. Specifies the clock frequency used by the watchdog timer.			
	<u>Bits</u>	<u>Definition</u>	<u>Bits</u>	<u>Definition</u>
	00b	32 us	10b	100 ms
	01b	10 ms	11b	1 s

PMx50 HPETEn

Bits	Description
31:10	HpetBaseAddress . Read-write. Reset: 3FB400h. Specifies the HPET MMIO base address[31:10]. The base address is FED0_0000h at default.
9:5	Reserved.
4	HpetTimer2MsiEn . Read-write. Reset: 0. 1=Enable HPET timer2 MSI capability. Writes to this bit modify the value in HPETx140[TmrFsbCap].
3	HpetTimer1MsiEn . Read-write. Reset: 0. 1=Enable HPET timer1 MSI capability. Writes to this bit modify the value in HPETx120[TmrFsbCap].
2	HpetTimer0MsiEn . Read-write. Reset: 0. 1=Enable HPET timer0 MSI capability. Writes to this bit modify the value in HPETx100[TmrFsbCap].
1	HpetIrqEn . Read-write. Reset: 0. 1=Enable HPET IRQ output.
0	HpetDecodeEn . Read-write. Reset: 0. 1=Enable HPET MMIO space decoding.

PMx54 SerialIrqConfig

Bits	Description
15:14	Reserved.
11:8	Reserved.
7	SerialIrqEnable . Read-write. Cold reset: 0. 1=Enable the serial IRQ function.
6	SerIrqMode . Read-write. Cold reset: 0. 0=Continuous mode. 1=Active (quiet) mode.
5:2	NumSerIrqBits . Read-write. Cold reset: 0. Specifies the total number of serial IRQs. <u>Bits</u> <u>Definition</u> 0 17 serial IRQs (15 IRQ#, SMI#, IOCHK#) 1 18 serial IRQs (15 IRQ#, SMI#, IOCHK#, INTA#) 15-2 <NumSerIrqBits+17> The serial IRQ can support 15 IRQ#, SMI#, IOCHK#, INTA#, INTB#, INTC#, and INTD#. When serial SMI# is used, BIOS needs to check super IO or device that generates serial SMI# for status.
1:0	NumStartBits . Read-write. Cold reset: 0. This field specifies the number of clocks in the start frame. Start Frame Width = 4 + 2 * NumStartBits.

PMx56 RTC Control

Bits	Description
15	Reserved.

14	ExtraRtcCmosEn . Read-write. Cold reset: 0. 1=Software can access the extra 16 bytes of RTC CMOS RAM through IO072 and IO073 ; The extra RAM space are located at index 0x00-0x03, 0x40-0x43, 0x80-0x83, 0xC0-0xC3. 0=Access to the extra RTC CMOS RAM space is disabled.
13	AltCmosMapEn . Read-write. Cold reset: 0. 1=When accessing the RTC CMOS RAM through IO070 and IO071 , Bank 1 of CMOS RAM is changed: Index 0Dh:00h still returns the time and alarm settings; Index 7Fh:0Eh returns the absolute offset FFh:8Eh, which map to the extended RAM space.
12	CenturyEn . Read-write. Cold reset: 1. 1=Enable RTC Century support.
11	MaskRtcClkOut . Read-write. Cold reset: 0. 0=Disable RtcClk output.
10	RtcClkDrive . Read-write. Cold reset: 1. 0=HIGHDRIVE is tied low for RtcClkOut pad. 1=HIGH-DRIVE is tied high for RtcClkOut pad.
4	RtcProtectC0_CF . Write-once. Cold reset: 0. 1=RTC RAM index CFh:C0h are locked from read/write.
3	RtcProtectD0_DF . Write-once. Cold reset: 0. 1=RTC RAM index DFh:D0h are locked from read/write.
2	RtcProtectE0_EF . Write-once. Cold reset: 0. 1=RTC RAM index EFh:E0h are locked from read/write.
1	RtcProtectF0_FF . Write-once. Cold reset: 0. 1=RTC RAM index FFh:F0h are locked from read/write.
0	RtcProtect38_3F . Write-once. Cold reset: 0. 1=RTC RAM index 3Fh:38h are locked from read/write.

PMx58 VRT_T1

Bits	Description
7:0	VRT_T1 . Read-write. Cold reset: 1. This field specifies the time of VRT_Enable being high for RTC battery monitor circuit in milliseconds. To conserve power, the RTC battery is sampled periodically for checking its state of health. VRT_T1 and PMx59 [VRT_T2] make up the interval of the checking. When VRT_Enable is high, the battery is being sampled. When VRT_Enable is low, the battery is not being sampled.

PMx59 VRT_T2

Bits	Description
7:0	VRT_T2 . Read-write. Cold reset: FFh. This field specifies the time of VRT_Enable being low for the RTC battery monitor circuit in 4 ms increments. See PMx58 [VRT_T1] for detailed description.

PMx5B RTC Shadow

Bits	Description
3:0	PwrFailShadow . Read-write. Cold reset: 0. BIOS: 0100b. Writing to these four bits sets the value of bits [7:4] above. Software should always program bit[2]=1.

PMx5C LLBCntrl

Bits	Description
7:3	Reserved.
2	AllowWakeS3En. Read-write. Cold reset: 0. 1=Allow LLB# as wake event in S3. Note: LLB (Low low battery) event should trigger a SCI if system is in S0. It should block wake-up if the system is in S-States. To meet that required behavior, SW should use the following setting: LLB_En (PMxC8[10]) = 1 BlockWakeEn = 0 UseAsWakeEn = 1 AllowWakeS3En = 0 or 1 (don't care).
1	UseAsWakeEn. Read-write. Cold reset: 0. 1=Treat LLB# as wake event.
0	BlockWakeEn. Read-write. Cold reset: 0. 1=Block wake event if LLB# is asserted; if (UseAsWakeEn==1) && (AllowWakeS3En==1), LLB# and other wake events can wake the system up from S3.

PMx5E RTC ExtIndex

Bits	Description
7:0	Index. Read-write. Cold reset: X. Specifies the offset of the RTC Extended Register to be read/written from PMx5F .

PMx5F RTC ExtData

Bits	Description
7:0	Data. Read-write. Cold reset: X. Specifies the read data or write data of the RTC Extended Register.

PMx5F_x00 RTCEXT DltSavEnable

Bits	Description
7:1	Reserved.
0	DltSavEnable. Read-write. Reset: 0. 1=Enable RTC daylight saving feature.

PMx5F_x01 RTCEXT SprFwdCtrl

Bits	Description
7	Reserved.
6	SprFwdWeek. Read-write. Reset: 0. This specifies which Sunday morning to do the “spring forward”. Spring forward is usually at the 1st Sunday of April in United States and last Sunday of March in Europe. 0=The 1st Sunday of the month. 1=The last Sunday of the month.
5:0	SprFwdHour. Read-write. Reset: 0. This Binary-Coded Decimal (BCD) value specifies which hour (24 hour mode) to do the “spring forward”. Spring forward is usually 2 am in United States and 1 am in Europe. 0=2 am. 02h=2 am.

PMx5F_x02 RTCEXT SprFwdMonth

Bits	Description
7:5	Reserved.
4:0	SprFwdMonth. Read-write. Reset: 0. This Binary-Coded Decimal (BCD) value determines which month to do the “spring forward”. Spring forward is usually at April in United States and March in Europe. 0=April. 04h=April.

PMx5F_x03 RTCEXT FallBackCtrl

Bits	Description
7	Reserved.
6	FallBackWeek. Read-write. Reset: 0. This value specifies which Sunday morning to do the “fall back”. Fall back is usually at the last Sunday of October in both United States and Europe. 0=The last week of the month. 1=The first week of the month.
5:0	FallBackHour. Read-write. Reset: 0. This Binary-Coded Decimal (BCD) value specifies which hour (24 hour mode) to do the “fall back”. Fall back is usually 2 am in United States and 1 am in Europe. 0=2 am. 02h=2 am.

PMx5F_x04 RTCEXT FallBackMonth

Bits	Description
7:5	Reserved.
4:0	FallBackMonth. Read-write. Reset: 0. This Binary-Coded Decimal (BCD) value specifies which month to “fall back”. Fall back is usually at October in both United States and Europe. 0=October. 10h=October.

PMx5F_x10 RTCEXT WeekTimerControl

The 16-bit Week Timer is a battery-powered down counter timer that supports 1ms, 1 second, and 1minute resolution and auto reloads when the timer reaches 0. The WEEK_ALRM interrupt is asserted when the timer reaches 0 and stays asserted until the timer is disabled.

Bits	Description												
7:3	Reserved.												
2:1	Resolution. Read-write. Reset: 0. This field specifies the resolution of the Week Timer counter. Before programing this bit, software should program Enable to 0 to disable the Week Timer. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>1 minute</td> <td>10b</td> <td>1 ms</td> </tr> <tr> <td>01b</td> <td>1 second</td> <td>11b</td> <td>Reserved</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	1 minute	10b	1 ms	01b	1 second	11b	Reserved
Bits	Definition	Bits	Definition										
00b	1 minute	10b	1 ms										
01b	1 second	11b	Reserved										
0	Enable. Read-write. Reset: 0. 0=Disable Week Timer. 1=Enable Week Timer.												

PMx5F_x11 RTCEXT WeekTimerReloadLow

Bits	Description
7:0	WeekTimerReloadLow . Read-write. Reset: 0. This field is used to program the lower 8 bits of the 16-bit WeekTimerReload register. Writing the WeekTimerReloadLow register causes the 16-bit WeekTimerReload to be written into the Week Timer. Software should program PMx5F_x10[Enable] = 0 before writing to this register.

PMx5F_x12 RTCEXT WeekTimerReloadHigh

Bits	Description
7:0	WeekTimerReloadHigh . Read-write. Reset: 0. This field is used to program the upper 8 bits of the 16-bit WeekTimerReload register. This field should be programmed before programming PMx5F_x11 [RTCEXT WeekTimerReloadLow] . Software should program PMx5F_x10[Enable] to 0 before writing to this register.

PMx5F_x13 RTCEXT WeekTimerDataLow

Bits	Description
7:0	WeekTimerDataLow . Read-only. Reset: 0. This field is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataLow register returns the lower 8 bits of the 16-bit Week Timer and causes the upper 8 bits to be latched into PMx5F_x14 [RTCEXT WeekTimerDataHigh] .

PMx5F_x14 RTCEXT WeekTimerDataHigh

Bits	Description
7:0	WeekTimerDataHigh . Read-only. Reset: 0. This field is used to read the current state of the 16-bit Week Timer. Reading from the WeekTimerDataHigh register returns the upper 8 bits of the 16-bit Week Timer latched by a previous read from PMx5F_x11 [RTCEXT WeekTimerReloadLow] .

PMx60 AcpiPm1EvtBlk

Bits	Description
15:2	AcpiPm1EvtBlk . Read-write. Cold reset: 0. Specifies the 16-bit IO range base address[15:2] of the ACPI power management event block defined in 3.26.15.1 [AcpiPmEvtBlk] .
1:0	Reserved.

PMx62 AcpiPm1CntBlk

Bits	Description

15:1	AcpiPm1CntBlk. Read-write. Cold reset: 0. Specifies the 16-bit IO base address[15:1] of the ACPI power management control block defined in 3.26.15.2 [AcpiPm1CntBlk] .
0	Reserved.

PMx64 AcpiPmTmrBlk

Bits	Description
15:1	AcpiPmTmrBlk. Read-write. Cold reset: 0. Specifies the 16-bit IO base address[15:1] of the ACPI power management timer block defined in 3.26.15.4 [AcpiPmTmrBlk] .
0	Reserved.

PMx66 CpuCntBlk

Bits	Description
15:3	CpuControl. Read-write. Cold reset: 0. Specifies the 16-bit IO base address[15:3] of the ACPI power management CPU control block defined in 3.26.15.5 [CpuCntBlk] .
2:0	Reserved.

PMx68 AcpiGpe0Blk

Bits	Description
15:2	AcpiGpe0Blk. Read-write. Cold reset: 0. Specifies the 16-bit IO base address[15:2] of the ACPI power management general purpose event block defined in 3.26.15.6 [AcpiGpe0Blk] .
1:0	Reserved.

PMx6A AcpiSmiCmd

Bits	Description
15:0	AcpiSmiCmd. Read-write. Cold reset: 0. These bits define the 16-bit IO base address[15:0] of the ACPI SMI command block defined in 3.26.15.7 [SmiCmdBlk] . The address is required to be WORD-aligned (Addr[0]=0).

PMx6E AcpiPm2CntBlk

Bits	Description
15:0	AcpiPm2CntBlk. Read-write. Cold reset: 0. These bits define the 16-bit IO base address[15:0] of the ACPI power management additional control block defined in 3.26.15.3 [AcpiPm2CntBlk] .

PMx74 AcpiConfig

Bits	Description
31:30	Reserved.
29	RtcWakeAlarm . Read-write. Cold reset: 1. BIOS: 0. 0=Use IO073_x0C[IRQF] as one of the system wake-up event if IRQF is enabled. 1=Use IO073_x0C[AF] as one of the system wake-up event if AF is enabled.
28	PcieGeventMap . Read-write. Cold reset: 0. 1=Route PME message from NB to GEvent 24, hot plug message from APU to GEvent 7.
27	WakePinAsGevent . Read-write. Cold reset: 0. 1=Treat Wake# pin as GEvent input.
25	PcieWakMask . Read-write. Cold reset: 0. 1=Disable the PCIE_WAK_STS and PCIE_WAK_DIS function defined in AcpiPmEvtBlkx00[PciExpWakeStatus] and AcpiPmEvtBlkx02[PciExpWakeDis] .
24	PcieNative . Read-write. Cold reset: 0. 1=Block PCIe GPP PME message and hot plug message from generating SCI.
23:8	Reserved.
7	BiosRls . RAZ; write-1-only. Cold reset: 0. Writing 1 to this bit generates SMI, NMI or IRQ13 depending on SMIxB0[Smicontrol73] .
6	MaskArbDis . Read-write. Cold reset: 1. 1= Disable the ArbDis function defined in AcpiPm2CntBlkx00[ArbDis] . ArbDis is not really used, but it still needs to be accessible by OS.
5	Reserved.
4	TmrEnEn . Read-write. Cold reset: 0. 1=Enable the TMR_EN function defined in AcpiPmEvtBlkx02[TmrEn] .
3	Reserved. Read-write.
2	RtcEnEn . Read-write. Cold reset: 0. 1=Enable the RTC_EN function defined in AcpiPmEvtBlkx02[RtcEn] .
1	GblEnEn . Read-write. Cold reset: 0. 1=Enable the GBL_EN function defined in AcpiPmEvtBlkx02[GblEn] .
0	DecEnAcpi . Read-write. Cold reset: 0. 1=Enable decoding of the standard ACPI registers.

PMx78 WakeIoAddr

Bits	Description
15:0	WakeIoBaseAddress . Read-write. Reset: FFFFh. Specifies the wake IO address. Any IO write to this IO address can cause APU to wake from C state. This is an obsolete function that is not used anymore.

PMx7A HaltCountEn

Bits	Description
15	CountHaltMsgEn . Read-write. Reset: 0. 1=FCH keeps track of the APU state by counting HALT entering and exit messages; When the number of net HALT enter messages matches with NumOfHalt, FCH initiates C1e.

14:4	Reserved.
3:0	NumOfHalt . Read-write. Reset: 0. Defines the number of HALT messages to track before FCH should initiate C1e sequence.

PMx7C C1eWrPortAdr

Bits	Description
15:0	C1eWrPortAdr . Read-write. Reset: FFFFh. IO write decoding Base address. Write to this IO address will cause FCH to initiate C1e sequence. This is an obsolete function that is not used anymore.

PMx7E CStateEn

Bits	Description
15	MaskIntrEn . Read-write. Reset: 1. 1=APIC interrupts are deferred until the first ACPI access after the system resumes from S state; In addition, A20M, IGNNE, INTR, NMI, INIT messages are deferred the same way, but SMI is not be deferred. This is mainly to guard against unexpected interrupt being sent to OS during S1 resume.
14	MaskCStateSys . Read-write. Reset: 0. 1=Skip C state if there is a pending interrupt such as SMI, NMI, and INIT request.
13:7	Reserved.
6	CPopUpEn . Read-write. Reset: 1. 1=Enable pop up capability, which means APU goes to C2 if there is a traffic and comes back to C3 after being idle for a while. This bit should be set to 0 when AltVid is not enabled.
5	C1eToC3En . Read-write. Reset: 1. 1=Put APU into C3 state in C1e state.
4	C1eToC2En . Read-write. Reset: 0. 1=Put APU into C2 state in C1e state.
3	C2EnhanceEn . Read-write. Reset: 0. 1=Enable C2 enhancement.
2	C2ToC3Enable . Read-write. Reset: 0. 1=Put APU into C3 even in the case of IO reads to CpuCntBlkx04 [PLvl2] .
1:0	Reserved.

PMx80 Break Event

Bits	Description
31	Reserved.
30:24	AutoStutterLimit . Read-write. Cold reset: 0. This specifies the limit for the AutoStutterTimer. Time unit is defined by [AutoStutterTimeSel]. See [AutoStutterTimerEn] for detailed description on AutoStutterTimer.
23:22	Reserved.
21	UsbPeriodicalSetBmSts . Read-write. Cold reset: 1. 1=Treat USB isochronous traffic as source of DMA traffic; this is to serve as a quicker way to bring the link between FCH and Fusion back to the active state.
20:19	Reserved.

18	Usb20SetBmSts. Read-write. Cold reset: 1. 1=Treat USB 2.0 traffic as source of DMA traffic; this is to serve as a quicker way to bring the link between FCH and Fusion back to the active state.
17	Usb11SetBmSts. Read-write. Cold reset: 1. 1=Treat USB 1.1 traffic as source of DMA traffic; this is to serve as a quicker way to bring the link between FCH and Fusion back to the active state.
16	Usb11BmStsEn. Read-write. Cold reset: 0. 1=Any USB 1.1 activity sets AcpiPmEvtBlkx00[BmStatus] to 1.
15:14	Reserved.
13	ServerCEn. Read-write. Cold reset: 0. 1=FCH monitors the HALT messages coming from APU(s). When all APUs are in HALT state, FCH automatically transitions to C3/C1e state. If any APU exits from HALT state, FCH will exit out from C3/C1e state as well. This is used in conjunction with PMx7A .
12	AutoStutterTimeSel. Read-write. Cold reset: 0. This bit selects the time increment used by the AutoStutterTimer. 0=2 us increment. 1=1 ms increment.
11	AutoStutterTimerEn. Read-write. Cold reset: 0. 1=Enable an AutoStutterTimer that automatically counts whenever LDTSTOP is asserted during C3/C1e state. When the timer reaches the threshold defined by AutoStutterLimit, it will stutter the C state machine. This feature is specifically designed to periodically reconnect the HT link in the case of a long idle time for multi-CPUs.
10	MergeBMReqEn. Read-write. Cold reset: 0. 1=The logic merges BMREQ# and AllowLdtStop together internally.
9	BusReqHoldEn. Read-write. Cold reset: 0. 1=Extend BMREQ# until LDTSTP# is asserted.
8	BmReqPopUpEn. Read-write. Cold reset: 0. 1=Allow PopUp if BMREQ# is toggled when PopUp function is enabled.
7	BmReqEn. Read-write. Cold reset: 0. 1=Treat BMREQ# as one source of Break Event.
6:5	Reserved.
4	EnableBreak. Read-write. Cold reset: 0. 1=Skip the C state transition if there is break event when entering C state.
3	Reserved.
2	AutoClrBmSts. Read-write. Cold reset: 0. It is used for PopUp and C1e function. 1=Automatically clear AcpiPmEvtBlkx00[BmStatus] before entering C1e state.
1	AutoBmRld. Read-write. Cold reset: 0. 1=Generate an internal AcpiPmEvtBlkx00[BmStatus] enable bit (that is similar to AcpiPm1CntBlkx00[BmRld]) upon entry to C1e. Depending on the configuration of other bits, bus master activity or IDLE_EXIT# pin could cause FCH to break out from C1e.
0	BmStsRdMask. Read-write. Cold reset: 0. 0= AcpiPmEvtBlkx00[BmStatus] is set to 1 if there is any DMA traffic in FCH. 1=Make AcpiPmEvtBlkx00[BmStatus] always return 0 except for USB 1.1 traffic.

PMx88 CStateControl

Bits	Description
31:14	Reserved.
13	LdtStpCmd. Read-write. Reset: 0. Programming it to 1 from 0 forces FCH to toggle LDTSTP#.
12	StutterMode. Read-write. Reset: 0. 1=Enable stutter mode.
11:6	Reserved.

5	SlpEn . Read-write. Reset: 0. 1=Enable LDTSTOP# as an output.
4	CcEn . Read-write. Reset: 0. 1=Enable C State. This bit must be set in order to exercise C state.
3	Reserved.
2	DlySlpEn . Read-write. Reset: 0. 1=Delay recognition of STPGNT# until there is no pending read in AB.
1	Reserved.
0	WaitStpGntEnB . Read-write. Reset: 0. 1=Wait for STPGNT# in ACPI S state.

PMx8E PopUpEndTime

Bits	Description
7:0	PopUpEndTime . Read-write. Cold reset: 10h. During C1e pop-up, FCH monitors internal DMA traffic. If there has been no traffic for PopUpEndTime, FCH will bring system back to C1e. The time is counted by 14.318 MHz clock. This can be considered as a minimum LDTSTOP deassertion time; however, this has been combined into LdtStartTime (PMx94[23:16]), and is not really required.

PMx94 CStateTiming0

Bits	Description												
31:26	Reserved.												
25:24	LdtEndTime . Read-write. Cold reset: 0. Specifies the delay from deassertion of LDTSTP# till the deassertion of STPCLK. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>0 us</td> <td>10b</td> <td>32 us</td> </tr> <tr> <td>01b</td> <td>1 us</td> <td>11b</td> <td>64 us</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	00b	0 us	10b	32 us	01b	1 us	11b	64 us
Bits	Definition	Bits	Definition										
00b	0 us	10b	32 us										
01b	1 us	11b	64 us										
23:16	LdtStartTime . Read-write. Cold reset: 10h. Specifies the LDTSTP# deassertion time in 1 us increments in C state.												
15:8	SLdtStartTime . Read-write. Cold reset: 0. Specifies the delay between LPC_PD# assertion and LDTSTP# assertion when the system enters ACPI S states. The time is in 1 us increments, with 1 us uncertainty.												
7:0	StutterTime . Read-write. Cold reset: 1. Specifies the LDTSTP# duration in 1 us increments. This is basically the minimum LDTSTP# assertion time.												

PMx98 CStateTiming1

Bits	Description																				
31	Reserved.																				
30:28	VidFidTime . Read-write. Cold reset: 1. Specifies the VID/FID LDTSTP# duration. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0 us</td> <td>100b</td> <td>16 us</td> </tr> <tr> <td>001b</td> <td>2 us</td> <td>101b</td> <td>32 us</td> </tr> <tr> <td>010b</td> <td>4 us</td> <td>110b</td> <td>64 us</td> </tr> <tr> <td>011b</td> <td>8 us</td> <td>111b</td> <td>128 us</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	0 us	100b	16 us	001b	2 us	101b	32 us	010b	4 us	110b	64 us	011b	8 us	111b	128 us
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001b	2 us	101b	32 us																		
010b	4 us	110b	64 us																		
011b	8 us	111b	128 us																		

27:16	Reserved.
15:8	FirstLdtStartTime . Read-write. Cold reset: 10h. Specifies the very first LDTSTP# assertion delay in 1 us increments from reception of STPGNT.
7:0	StpClkDlyTime . Read-write. Cold reset: 0. Specifies the additional STPCLK# deassertion delay in number of oscillator clocks for S1 resume.

PMx9C C2Count

Bits	Description
7:0	C2Count . Read-only; updated-by-hardware. Reset: 0. Specifies the amount of time the APU spends in STPGNT state (but LDTSTOP# is not asserted) during C1e. Each increment is approximately 0.39% (1/256). This field is updated every second.

PMx9D C3Count

Bits	Description
7:0	C3Count . Read-only; updated-by-hardware. Reset: 0. Specifies the amount of time LDTSTOP# is asserted during C1e. Each increment is approximately 0.39% (1/256). This field is updated every second.

PMxA0 MessageCState

Bits	Description												
31	CheckCoreIdDis . Read-write. Reset: 0. 1=Ignore core ID check if (MultiCoreEn == 1). 0=Enable core ID check if (MultiCoreEn == 1).												
30:24	ExtendValue . Read-write. Reset: 0. Specifies the timer value to be used with ExtendEnable. The value is the number of 66 MHz clocks.												
23	MultiCoreEn . Read-write. Reset: 0. 1=C state control logic inside FCH assumes multi-core configuration; PMx7A[NumOfHalt] should be programmed accordingly; FCH keeps track of APU C state by monitoring each core's C state message instead of package state.												
22	FusionExitCMsgDis . Read-write. Reset: 0. 1=ExitC Message will be blocked.												
21	FusionAllowCMsgDis . Read-write. Reset: 0. 1=AllowC Message will be blocked.												
20:16	TmrSelOverride . Read-write. Reset: 0. These bits are used with TimerTickChgMsgEn. In case that FCH auto-timer detection logic doesn't function properly, these bits can be used to override the logic and force the logic to monitor the specific timer. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[4]</td> <td>1=Force the logic to monitor HPET timer 2 if HPET is selected</td> </tr> <tr> <td>[3]</td> <td>1=Force the logic to monitor HPET timer 1 if HPET is selected</td> </tr> <tr> <td>[2]</td> <td>1=Force the logic to monitor HPET timer 0 if HPET is selected</td> </tr> <tr> <td>[1]</td> <td>1=Use RTC</td> </tr> <tr> <td>[0]</td> <td>1=Use HPET</td> </tr> </tbody> </table>	Bit	Definition	[4]	1=Force the logic to monitor HPET timer 2 if HPET is selected	[3]	1=Force the logic to monitor HPET timer 1 if HPET is selected	[2]	1=Force the logic to monitor HPET timer 0 if HPET is selected	[1]	1=Use RTC	[0]	1=Use HPET
Bit	Definition												
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[3]	1=Force the logic to monitor HPET timer 1 if HPET is selected												
[2]	1=Force the logic to monitor HPET timer 0 if HPET is selected												
[1]	1=Use RTC												
[0]	1=Use HPET												

15:14	UsbEhciModeFusion[1:0] . Read-write. Reset: 0. These bits are used with Fusion CPU C state.
	<u>Bit Definition</u>
[1]	1=FCH causes CPU to break out from C state when USB EHCI has pending traffic.
[0]	1=FCH stutters the CPU C state whenever USB EHCI has pending traffic.
13:12	UsbOhciModeFusion[1:0] . Read-write. Reset: 0. These bits are used with Fusion CPU C state.
	<u>Bit Definition</u>
[1]	1=FCH causes CPU to break out from C state when USB OHCI has pending traffic.
[0]	1=FCH stutters the CPU C state whenever USB OHCI has pending traffic.
11	ExtendEnable . Read-write. Reset: 0. 1=Enable FCH to start a timer whenever the C state is exited, in order to prevent CPU from going back to C state before the timer expires. See ExtendValue for the timer.
10	ClkIntrTagEn . Read-write. Reset: 0. 1=Enable FCH to mark the periodic timer interrupt.
9	PopUpByEc . Read-write. Reset: 0. A static bit that can be written by IMC to cause FCH to pop up C state message to CPU.
8	WakeByEc . Read-write. Reset: 0. A static bit that can be written by IMC to cause FCH to generate C state exit message to CPU.
7	SelfExitEnable . Read-write. Reset: 0. 1=FCH exits to C0 state from non-C0 state when there is a break event, and exits to C1 state from non-C0 state when there is traffic.
6	BatteryModeEn . Read-write. Reset: 0. 1=A change in power mode (battery vs AC) causes FCH to tell CPU to exit from C state.
5	Reserved.
4	FusionSerrEn . Read-write. Reset: 0. 1=FCH C state coordination logic causes CPU to exit from C state when there is a system error within the FCH.
3	FusionPerrEn . Read-write. Reset: 0. 1=FCH C state coordination logic causes CPU to exit from C state when there is a parity error within the FCH.
2	FusionCEnable . Read-write. Reset: 1=Enable the FCH Fusion C state coordination logic. Fusion CPU contains the actual C state logic and FCH contains the coordination logic which sends hand-shake message to CPU to help it to decide which C state to go into.
1	TimerTickChgMsgEn . Read-write. Reset: 0. 1=FCH sends a message to APU indicating the latest periodic timer interval. FCH automatically determines which timer (PIT, RTC, or HPET) is being used. See TmrSelOverride.
0	BattModeChgMsgEn . Read-write. Reset: 0. 1=FCH automatically sends a message to CPU indicating the power mode (AC vs battery); In addition, every time it is changed, FCH generates a message to indicate the update.

PMxA4 Traffic Monitor and Status

Address: [PMxA4\[PmioA4Sel\]](#).

Bits	Description
31	PmioA4Sel . Read-write. Reset: 0. 0=This register is the TrafficMonitorEn register. 1=This register is selected to be TrafficStatus register. In both cases, this bit has the same definition.
30:0	TrafficData .

PMxA4_x0 TrafficMonitorEn

Bits	Description										
31	PmioA4Sel. Read-write. Reset: 0. 0=This register is the TrafficMonitorEn register. 1=This register is selected to be TrafficStatus register. In both cases, this bit has the same definition.										
30	IntrSciSts. Read-only. Reset: 0. This bit can be cleared by programming InterruptSciEn to 0. 0=SCI event from interrupt monitoring doesn't happen. 1=SCI event from interrupt monitoring has been fired. See InterruptSciEn for details on interrupt monitoring.										
29	TrafficSciSts. Read-only. Reset: 0. This bit can be cleared by programming TrafficSciEn to 0. 0=SCI event from traffic monitoring doesn't happen. 1=SCI event from traffic monitoring has been fired. See TrafficSciEn for details on traffic monitoring.										
28	ModFusionCHandShakeEn. Read-write. Reset: 0. 0=Fusion C-state logic uses a 3-way handshake protocol: CPU -> C1 entry message FCH -> C-state allow message CPU -> C-state taken message 1=Fusion C-state logic uses a 2-way handshake protocol: CPU -> C1 entry message FCH -> C-state allow message From there, FCH assumes CPU will take the highest C state indicated by the C-state allow message.										
27	IntrLess. Read-write. Reset: 0. 0=Monitor whether the number of interrupts is more than PMxA4[IntrTimeLimit]. 1=Monitor whether the number of interrupts is less than PMxA4[IntrTimeLimit].										
26	TrafficLess. Read-write. Reset: 0. 0=Monitor whether the idle number is less than PMxA4[IdleTimeLimit]. 1=Monitor whether the idle number is more than PMxA4[IdleTimeLimit].										
25:24	PerfMonPeriodSel. Read-write. Reset: 0. Specifies the traffic/interrupt monitoring period. It is used when [PerfMonEn] == 1. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>15 ns between each count and the monitored interval is ~1 ms.</td> </tr> <tr> <td>01b</td> <td>240 ns between each count and the monitored interval is 15.67 ms.</td> </tr> <tr> <td>10b</td> <td>1.92 us between each count and the monitored interval is 125.3 ms.</td> </tr> <tr> <td>11b</td> <td>15.36 us between each count and the monitored interval is ~1 second.</td> </tr> </tbody> </table>	Bits	Definition	00b	15 ns between each count and the monitored interval is ~1 ms.	01b	240 ns between each count and the monitored interval is 15.67 ms.	10b	1.92 us between each count and the monitored interval is 125.3 ms.	11b	15.36 us between each count and the monitored interval is ~1 second.
Bits	Definition										
00b	15 ns between each count and the monitored interval is ~1 ms.										
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10b	1.92 us between each count and the monitored interval is 125.3 ms.										
11b	15.36 us between each count and the monitored interval is ~1 second.										
23:15	Reserved.										
14	MaskIntrToCState. Read-write. Reset: 0. 1=Interrupts are masked off internally and do not cause FCH to generate Exit message to Fusion CPU. This function is only applicable to Fusion CPU configuration.										
13	Reserved.										
12	CheckFc. Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to monitor FC (NAND flash) traffic.										
11	Reserved.										
10	CheckLpc. Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to monitor LPC traffic.										
9	CheckAz. Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to monitor HD audio traffic.										
8	Reserved.										

7	CheckUsb . Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to monitor USB traffic.
6	CheckSata . Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to monitor SATA traffic.
5	Reserved.
4	CheckC3 . Read-write. Reset: 0. This bit is used with TrafficSciEn. 1=Enable FCH to only consider the system as in idle state if CPU is in C state.
3	CheckInterrupt . Read-write. Reset: 0. This bit is used with InterruptSciEn. 1=Enable FCH to monitor interrupts.
2	InterruptSciEn . Read-write. Reset: 0. 1=FCH monitors the number of interrupts within the monitored interval; If the number of interrupts is less than the number defined in PMxA8[IntrTimeLimit] , FCH generates an SCI.
1	TrafficSciEn . Read-write. Reset: 0. 1=FCH generates an SCI when the amount of traffic is less than PMxA8[IdleTimeLimit] within the monitored interval.
0	PerfMonEn . Read-write. Reset: 0. 1=FCH monitors the amount of DMA traffic enabled by bits [12:6] and the number of interrupts within the monitored interval defined by PerfMonPeriodSel.

PMxA4_x1 TrafficStatus

Bits	Description												
31	PmioA4Sel . Read-write. Reset: 0. 0=This register is the TrafficMonitorEn register. 1=This register is selected to be TrafficStatus register. In both cases, this bit has the same definition.												
30:24	Reserved.												
23:22	FusionCState3 . Read-write. Reset: 0. Status of fusion C state monitor for core pair 3. See FusionC-State.												
21:20	FusionCState2 . Read-write. Reset: 0. Status of fusion C state monitor for core pair 2. See FusionC-State.												
19:18	FusionCState1 . Read-write. Reset: 0. Status of fusion C state monitor for core pair 1. See FusionC-State.												
17:16	FusionCState0 . Read-write. Reset: 0. Status of fusion C state monitor for core pair 0. See FusionC-State.												
15:14	FusionCState . Read-write. Reset: 0. Status of fusion C state monitor. <table border="1" style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>Fusion Idle</td> <td>10b</td> <td>Fusion C4</td> </tr> <tr> <td>01b</td> <td>Fusion C5/6</td> <td>11b</td> <td>Fusion C3</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	Fusion Idle	10b	Fusion C4	01b	Fusion C5/6	11b	Fusion C3
Bits	Definition	Bits	Definition										
00b	Fusion Idle	10b	Fusion C4										
01b	Fusion C5/6	11b	Fusion C3										
13	Reserved.												
12	FcTrafficStatus . Read-only; updated-by-hardware. Reset: X. Indicates whether Flash Controller (NAND flash) is active. 0=Inactive. 1=Active.												
11	Reserved.												
10	LpcTrafficStatus . Read-only; updated-by-hardware. Reset: X. Indicates whether LPC is active. 0=Inactive. 1=Active.												
9	AzTrafficStatus . Read-only; updated-by-hardware. Reset: X. Indicates whether HD audio is active. 0=Inactive. 1=Active.												

8	Reserved.
7	UsbTrafficStatus . Read-only; updated-by-hardware. Reset: X. Indicates whether USB is active. 0=Inactive. 1=Active.
6	SataTrafficStatus . Read-only; updated-by-hardware. Reset: X. Indicates whether SATA is active. 0=Inactive. 1=Active.
5:0	Reserved.

PMxA8 TrafficMonitorIdleTime

Bits	Description
15:0	IdleTimeLimit . Read-write. Reset: 0. This field is used with PMxA4_x0[PerfMonEn] . It specifies the amount of DMA traffic limit that causes FCH to generate an SCI. Time granularity is defined by PMxA4_x0[PerfMonPeriodSel] .

PMxAA TrafficMonitorIntTime

Bits	Description
15:0	IntrTimeLimit . Read-write. Reset: 0. This field is used with PMxA4_x0[PerfMonEn] . It specifies the amount of interrupt limit that causes FCH to generate an SCI. Time granularity is defined by PMxA4_x0[PerfMonPeriodSel] .

PMxAC TrafficMonitorTrafficCount

Bits	Description
15:0	TrafficCount . Read-only; updated-by-hardware. Reset: 0. Specifies the actual recorded value of the combined DMA traffic during the monitored period.

PMxAE TrafficMonitorIntrCount

Bits	Description
15:0	IntrCount . Read-only; updated-by-hardware. Reset: 0. Specifies the actual recorded value of the number of interrupts during the monitored period.

PMxB0 DeferTimeTick / OBFF Control

Bits	Description
11	Reserved.
10:8	DeferTimerTickValue . Read-write. Reset: 0.
	<u>Bits</u> <u>Definition</u>
	000b No skipping
	001b Skip 1 timer tick
	010b Skip 2 timer ticks
	011b Skip 3 timer ticks
	<u>Bits</u> <u>Definition</u>
	100b Skip 4 timer ticks
	101b Skip 5 timer ticks
	110b Skip 6 timer ticks
	111b Skip 7 timer ticks

7:2	Reserved.
1	ForceTmrTickEn . Read-write. Reset: 0. 1=If (DeferTimerTickEn == 1) && FCH has skipped a timer tick interrupt, FCH immediately generates the timer tick interrupt upon C state exit.
0	DeferTimerTickEn . Read-write. Reset: 0. 1=FCH skips a number of timer tick interrupts based on the value defined in DeterTimeTickValue when CPU is in C state. When CPU is not in C state, FCH does not skip any timer tick interrupt.

PMxB4 AcpiMiscDebug / Tpreset1b

Bits	Description																				
31:30	Reserved.																				
29:24	Tpreset1b . Read-write. Cold reset: 5h. This is the timing parameter used for S*->S0 state transition. It specifies the delay between CPU_STP# de-assertion and LPC_PD# de-assertion, in 8 us increment with 8 us uncertainty.																				
11:9	FidVidOption . Read-write. Cold reset: 0. Specifies the additional FID/VID exit delay. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>0 ns</td> <td>100b</td> <td>490 ns</td> </tr> <tr> <td>001b</td> <td>140 ns</td> <td>101b</td> <td>560 ns</td> </tr> <tr> <td>010b</td> <td>210 ns</td> <td>110b</td> <td>350 ns</td> </tr> <tr> <td>011b</td> <td>280 ns</td> <td>111b</td> <td>420 ns</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	0 ns	100b	490 ns	001b	140 ns	101b	560 ns	010b	210 ns	110b	350 ns	011b	280 ns	111b	420 ns
Bits	Definition	Bits	Definition																		
000b	0 ns	100b	490 ns																		
001b	140 ns	101b	560 ns																		
010b	210 ns	110b	350 ns																		
011b	280 ns	111b	420 ns																		
8	DelayLdtStp . Read-write. Cold reset: 0. 1=Enable LDTSTP# assertion time.																				
0	FidProtectEn . Read-write. Cold reset: 0. 1=Skip C-state transition when FID/VID messages are received concurrently.																				

PMxB8 Tpreset2

Bits	Description										
7:6	ClkGateCntrl . Read-write. Cold reset: 2h. These two bits control whether SMBUS module allows clock gating to the internal 66 MHz core clock. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable the clock gating function</td> </tr> <tr> <td>01b</td> <td>Wait 16 clocks before allowing clock gating to the SMBUS module</td> </tr> <tr> <td>10b</td> <td>Wait 64 clocks before allowing clock gating to the SMBUS module</td> </tr> <tr> <td>11b</td> <td>Wait 256 clocks before allowing clock gating to the SMBUS module</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable the clock gating function	01b	Wait 16 clocks before allowing clock gating to the SMBUS module	10b	Wait 64 clocks before allowing clock gating to the SMBUS module	11b	Wait 256 clocks before allowing clock gating to the SMBUS module
Bits	Definition										
00b	Disable the clock gating function										
01b	Wait 16 clocks before allowing clock gating to the SMBUS module										
10b	Wait 64 clocks before allowing clock gating to the SMBUS module										
11b	Wait 256 clocks before allowing clock gating to the SMBUS module										
5:0	Tpreset2 . Read-write. Cold reset: 8h. This is the timing parameter used for S*->S0 state transitions. It specifies the LDTSTP# deassertion delay in 8 us increment with 8 us uncertainty.										

PMxB9 LpcMisc

Bits	Description
7:4	Reserved.

3	ClkRunDisable . Read-write. Cold reset: 0. Legacy DMA and serial IRQ logic reside in this module and they are running on the 33 MHz LPCCLK. 1=Disable this module's ability to support CLKRUN# function from PCIBridge; In other words, this module prevents PCIBridge from stopping the 33 MHz clock.
2:0	Reserved.

PMxBA S_StateControl

Bits	Description
15	MaskPmeMsgEn . Read-write. Cold reset: 0. 1=If (PmeMsgEn == 1), PmeAck messages coming from PCIe device are ignored and ACPI S state logic solely uses the timeout mechanism to sequence through the S3 state. This bit is used as an option to guard against multiple PmeAck messages coming from CNB and internal FCH PCIe bridges so that FCH S state logic does not sequence into S3 state prematurely.
14	WakePinEnable . Read-write; S3-check-exclude. Cold reset: 0. 1=Enable wake up from WAKE# pin.
12:4	Reserved
3	PmeMsgEn . Read-write. Cold reset: 0. 1=Enable PmeTurnOff/PmeMsgAck handshake.
2	Reserved.
0	LongSLPS3 . Read-write. Cold reset: 0. 1=Extend SLP_S3# assertion to 1 s minimum.

PMxBC ThrottlingControl

Bits	Description																				
15	Therm2SecDelay . Read-write. Cold reset: 0. 1=Enable 2 second delay for thermal clock throttle. This bit affects both hardware and software throttle.																				
14	NoWaitStpGntEn . Read-write. Cold reset: 0. 0=Wait for STPGNT after asserting STPCLK. 1=Do not wait for STPGNT after asserting STPCLK. This bit affects both hardware and software throttle.																				
13	ThermThrotPeriod . Read-write. Cold reset: 0. Specifies the clock throttle period for hardware thermal throttle. 0=30 us. 1=244 us.																				
12:8	Reserved.																				
7	ThrottleControl[3] . Read-write. Cold reset: 0. 1=Enable hardware thermal clock throttle. This function is used in conjunction with TALERT#, PROCHOT#, or TEMPIN0.																				
6:4	ThrottleControl[2:0] . Read-write. Cold reset: 0. Specifies the throttle interval for STPCLK de-assertion in hardware thermal clock throttle:																				
	<table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>50%</td> <td>100b</td> <td>50%</td> </tr> <tr> <td>001b</td> <td>12.5%</td> <td>101b</td> <td>62.5%</td> </tr> <tr> <td>010b</td> <td>25%</td> <td>110b</td> <td>75%</td> </tr> <tr> <td>011b</td> <td>37.5%</td> <td>111b</td> <td>87.5%</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	50%	100b	50%	001b	12.5%	101b	62.5%	010b	25%	110b	75%	011b	37.5%	111b	87.5%
Bits	Definition	Bits	Definition																		
000b	50%	100b	50%																		
001b	12.5%	101b	62.5%																		
010b	25%	110b	75%																		
011b	37.5%	111b	87.5%																		

3:2	Reserved.												
1:0	AcpThrotPeriod . Read-write. Cold reset: 0. Specifies the clock throttle period for software thermal throttle. See CpuCntBlkx00 [ClkValue] for software thermal throttle. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>15 us</td> <td>10b</td> <td>244 us</td> </tr> <tr> <td>01b</td> <td>30 us</td> <td>11b</td> <td>Reserved</td> </tr> </table>	Bits	Definition	Bits	Definition	00b	15 us	10b	244 us	01b	30 us	11b	Reserved
Bits	Definition	Bits	Definition										
00b	15 us	10b	244 us										
01b	30 us	11b	Reserved										

PMxBE ResetControl1

Table 237: BIOS Recommendations for KbRstEn

Case	Condition	Setting	Comments
1	If the KBRST# / GEVENT1# I/O pin is not connected to system keyboard reset or is configured as GEvent1 function.	0	This bit must be cleared by the platform system BIOS in this case. CIM-x does not support call back function to clear this bit.
2	All other situations other than that specified in Case 1	Do not program.	Value should remain at power-up default setting.

Bits	Description										
7	RstToCpuPwrGdEn . Read-write. Cold reset: 0. 1=FCH toggles CpuPwrGd on every reset.										
6	HwmResetOption . Read-write. Cold reset: 1. 0=Hwm function defined at 3.26.14 [Power Management Block 2 (PM2) Registers] is reset by RsmRst. 1=Hwm function defined at 3.26.14 [Power Management Block 2 (PM2) Registers] is reset by PciRst.										
5	SlpTypeControl . Read-write. Cold reset: 1. 1=Enable the function of AcpPm1CntBlkx00[SlpTypeEn] . 0= AcpPm1CntBlkx00[SlpTypeEn] bit has no effect.										
4	KbRstEn . Read-write. Cold reset: 1. BIOS: See Table 237 . 1= Enable KBRST# pin to trigger keyboard reset.										
3:2	CpuRstControl . Read-write. Cold reset: 0. <table style="margin-left: 20px;"> <tr> <th>Bits</th> <th>Definition</th> </tr> <tr> <td>00b</td> <td>CpuReset is deasserted after PciReset</td> </tr> <tr> <td>01b</td> <td>CpuReset is deasserted as PciReset</td> </tr> <tr> <td>10b</td> <td>CpuReset is deasserted before PciReset</td> </tr> <tr> <td>11b</td> <td>CpuReset is deasserted after PciReset</td> </tr> </table>	Bits	Definition	00b	CpuReset is deasserted after PciReset	01b	CpuReset is deasserted as PciReset	10b	CpuReset is deasserted before PciReset	11b	CpuReset is deasserted after PciReset
Bits	Definition										
00b	CpuReset is deasserted after PciReset										
01b	CpuReset is deasserted as PciReset										
10b	CpuReset is deasserted before PciReset										
11b	CpuReset is deasserted after PciReset										
1	KbPciRstEn . Read-write. Cold reset: 1. This bit must not be programmed by the BIOS. It should be left with the power up default value of 1. 1=Make PCI reset during keyboard reset, which can be triggered by KBRST# pin or IMC.										
0	SoftResetEn . Read-write. Cold reset: 0. 1=Block any reset request until the system is not in C state.										

PMxC0 S5/Reset Status

This register shows the source of previous reset.

Bits	Description
31:30	Reserved.
29	EcWatchdogRst . Write-1-to-clear; Read. Cold reset: 0.

28	HangReset . Write-1-to-clear; Read. Cold reset: 0.										
27	SyncFlood . Write-1-to-clear; Read. Cold reset: 0.										
26	RemoteResetFromASF . Write-1-to-clear; Read. Cold reset: 0.										
25	WatchdogIssueReset . Write-1-to-clear; Read. Cold reset: 0.										
24	FailBootRst . Write-1-to-clear; Read. Cold reset: 0.										
23	LtReset . Write-1-to-clear; Read. Cold reset: 0.										
22	KbReset . Write-1-to-clear; Read. Cold reset: 0.										
21	SleepReset . Write-1-to-clear; Read. Cold reset: 0.										
20	DoFullReset . Write-1-to-clear; Read. Cold reset: 0.										
19	DoReset . Write-1-to-clear; Read. Cold reset: 0.										
18	DoInit . Write-1-to-clear; Read. Cold reset: 0.										
17	SoftPciRst . Write-1-to-clear; Read. Cold reset: 0.										
16	UserRst . Write-1-to-clear; Read. Cold reset: 0.										
15:14	PmeTurnOffTime . Read-write. Cold reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>1 ms</td> </tr> <tr> <td>01b</td> <td>2 ms</td> </tr> <tr> <td>10b</td> <td>4 ms</td> </tr> <tr> <td>11b</td> <td>8 ms</td> </tr> </tbody> </table>	Bits	Definition	00b	1 ms	01b	2 ms	10b	4 ms	11b	8 ms
Bits	Definition										
00b	1 ms										
01b	2 ms										
10b	4 ms										
11b	8 ms										
13	DisSbToNbPG . Read-write. Cold reset: 0. 1=Disable NBPwrGood.										
12	DisableLdtPwrGood . Read-write. Cold reset: 0. This is a LdtPwrGood control bit. 1=Disable the LdtPwrGood assertion along with NBPwrGood.										
11	SlpS3ToLdtPwrGdEn . Read-write. Cold reset: 1. 1=De-assert LDT_PWRGD as long as SLP_S3# goes low.										
10	PwrGdDwnBeforeSlpS3 . Read-write. Cold reset: 0. BIOS: 1. 1=Delay SLP_S3 by 64 us and also qualify the FCH PwrGood with SLP_S3; This allows internal logic to put signals into correct states before turning off the S0 power.										
9:6	Reserved.										
5	ShutDownFan0 . Write-1-to-clear; Read. Cold reset: 0.										
4	RemotePowerDownFromASF . Write-1-to-clear; Read. Cold reset: 0.										
3	ThermalTripFromTemp . Write-1-to-clear; Read. Cold reset: 0.										
2	Shutdown . Write-1-to-clear; Read. Cold reset: 0.										
1	FourSecondPwrBtn . Write-1-to-clear; Read. Cold reset: 0.										
0	ThermalTrip . Write-1-to-clear; Read. Cold reset: 0.										

PMxC4 ResetCommand

Bits	Description
7	ResetEn . Read-write. Cold reset: 0. 0=Writing to bit Reset is not allowed. 1=Writing to bit Reset is allowed.
6	ResetAllAcpi . Write-1-only; cleared-by-hardware. Cold reset: 0. Writing 1 to this bit emulates a reset button event.

5	ResetButtonEnForEC . Read-write. Cold reset: 1. 1=When IMC is enabled, reset from reset button can reset the entire ACPI block. 0=Only part of the ACPI block can be reset.
4	ResetPcie . Read-write. Cold reset: 0. 1=Reset the GPP ports. 0=Release the PCIe reset.
3	UsrRst2Pll . Read-write. Cold reset: 1. 1=Stop PLL when reset button is pressed.
2	SelectDebug . Read-write. Cold reset: 0. 0=Select PMxC0 [S5/Reset Status] to be S5/Reset Status register. 1=Select PMxC0 [S5/Reset Status] to be a debug status register.
1	MemRstDisable . Read-write. Cold reset: 0. 1=The memory reset function at DDR_RST# pin is disabled.
0	Reset . Write-1-only; cleared-by-hardware. Cold reset: 0. Writing 1 to this bit causes a PCI reset. This bit is enabled by RestEn bit.

PMxC5 CF9 Shadow

Bits	Description
7:0	Alias of IOCF9 .

PMxC8 Misc

Bits	Description										
31:24	ClkIntrVectorOrd . Read-write. Cold reset: 0. Specifies the value used to identify the clock interrupt.										
23	Reserved.										
22	ClkIntrVectorOrdEn . Read-write. Cold reset: 0. 1=The system timer interrupt in the IOAPIC is tagged with a value defined by ClkIntrVectorOrd.										
21	Reserved.										
20	ProcHotStsEn . Read-write. Cold reset: 0. 1=Enable PROCHOT# to generate TwarnStatus SMIx84[16] and thermal throttle.										
19	UseCpuRst . Read-write. Cold reset: 1. 0=System reset causes INIT# instead of CPURST#.										
18	UseBypassRom . Read-write. Cold reset: 0. 1=Override the ROM straps and use BypassRomSel to determine which type of ROM to use. This is for BIOS debugging purpose or for systems having multiple BIOSes on board.										
17:16	BypassRomSel . Read-write. Cold reset: 0. These two bits override the two ROM strap pins if [Use-BypassRom] == 1. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>LPC ROM</td> </tr> <tr> <td>01b</td> <td>Reserved</td> </tr> <tr> <td>10b</td> <td>Reserved</td> </tr> <tr> <td>11b</td> <td>SPI ROM</td> </tr> </tbody> </table>	Bits	Definition	00b	LPC ROM	01b	Reserved	10b	Reserved	11b	SPI ROM
Bits	Definition										
00b	LPC ROM										
01b	Reserved										
10b	Reserved										
11b	SPI ROM										
15	HideSmbus . Read-write. Cold reset: 0. 1=Hide the SMBus PCI configuration space and promote LPC bridge PCI configuration space to function 0.										
14	Reserved. Read-write. Cold reset: 1.										
13	IdChangeEn . Read-write. Cold reset: 0. 1=Allow the software to change D14F0x00[DeviceID] and D14F0x08[RevisionID] .										
12	S5ResetOverride . Read-write. Cold reset: 0. 1=Mask off internet PCI reset used in ACPI.										

11	WriteBackEnable. Read-write. Cold reset: 0. 1=The WakeOnRing status bit is written back to HD audio controller upon system power up. Note: Since HD audio controller is in S0 power domain, we have to temporarily store the status (such WakeOnRing) in S5 power domain (ACPI). After S0 power domain is powered up, the status bit should be written back to HD audio controller. Software should read the WakeOnRing bit in HD audio controller. ACPI is not responsible for reporting the WakeOnRing bit.
10	LlbEn. Read-write. Cold reset: 0. 1=LLB function is enabled and system won't wake up from ACPI S state until LLB# is de-asserted.
9:8	TempPolarity. Read-write. Cold reset: 0. Temperature polarity control for THRMTRIP and TALERT respectively. 0=Active low. 1=Active high.
7	DisablePciRom. Read-write. Cold reset: 0. 1=Disable PCI from strap.
6	TwarnEn. Read-write. Cold reset: 0. 1=Enable TALERT# pin.
3	TDeadEn. Read-write. Cold reset: 1. 1=GEVENT2 takes up the THRMTRIP function; When THRMTRIP pin is low and [TFatalEn] is set, hardware switches the system to S5 automatically.
2	TFatalEn. Read-write. Cold reset: 1. 1=Enable both the soft PciRst and the THRMTRIP function.
1	Reserved.
0	CpuIoPullDownDrvStrength. Read-write. Cold reset: 0. 1=The integrated pull-down drive strength of all CPU IOs are increased by 50%.

PMxD0 RstCntrl

Bits	Description
7:6	RstLengthSel. Read-write. Cold reset: 0. This field selects which register is defined at PMxD1 .
5:0	Reserved.

PMxD1 Reset Function

Address: [PMxD0](#)[RstLengthSel].

Bits	Description
7:0	RstFunctLength.

PMxD1_x0 RstLength

Bits	Description
7:0	RstLength. Read-write. Cold reset: F4h. Specifies the A_RST# length. The amount of reset time = RstLength * 4096 * 69.84 ns.

PMxD1_x1 APURstLength

Bits	Description
7:0	APURstLength. Read-write. Cold reset: FBh. Specifies the APU_RST# length. The amount of reset time = ApuRstLength * 4096 * 69.84 ns.

PMxD1_x3 APUPwrGdLength

Bits	Description
7:0	APUPwrGdLength. Read-write. Cold reset: EAh. Specifies the LdtPwrGd latency. The amount of delay = APUPwrGdLength * 4096 * 69.84 ns.

PMxD3 ManualReset

Bits	Description
7	Reserved.
6	AssertSDRstB. Read-write. Cold reset: 1. 0=Assert the reset to SDIO controller.
5	AssertAzRstB. Read-write. Cold reset: 1. 0=Assert the reset to AZ controller.
4	AssertUsbRstB. Read-write. Cold reset: 1. BIOS: See 2.15.2.5 . 0=Assert the reset to USB controllers.
3	AssertSataRstB. Read-write. Cold reset: 1. 0=Assert the reset to SATA controller.
2	AssertPciRstB. Read-write. Cold reset: 1. 0=Assert PCIRST# low.
1	AssertARstB. Read-write. Cold reset: 1. 0=Assert A_RST# low.
0	AssertLdtRstB. Read-write. Cold reset: 1. 0=Assert LDT_RST# low.

PMxD6 IMC Gating

Bits	Description
15	ImcEnable. Read-write. Reset: 0. BIOS: See 2.15.8 . 1=Enable IMC. This is one of the ways to enable IMC. Another way is to override strap through MISCx84 .

PMxD8 Eprom/Efuse Index

Bits	Description

PMxD9 Eprom/Efuse Data

Bits	Description

PMxDA SataConfig

Bits	Description
7:6	RefDivSel. Read-write. Cold reset: 00b. BIOS: See 2.15.3.5 . This specifies the reference clock divider setting. <u>Bits</u> <u>Definition</u> 00b Divide by 1 (25 MHz or 48 MHz reference clock) 01b Divide by 2 10b Divide by 4 (100 MHz reference clock) 11b Divide by 4 (100 MHz reference clock)
5:4	RefClkSel. Read-write. Cold reset: 01b. BIOS: See 2.15.3.5 . This specifies the reference clock source selection for SATA PLL. <u>Bits</u> <u>Definition</u> 00b Reference clock from crystal oscillator via PAD_XTALI and PAD_XTALO 01b Reference clock from internal clock through CP_PLL_REFCLK_P and CP_PLL_REFCLK_N via RDL 10b Reserved. 11b Reserved.
3	Reserved.
2	SetMaxGen2. Read-write. Cold reset: 0. 0=SATA controller operates in maximum Gen3 (6.0 Gb/s) speed. 1=SATA controller operates in maximum Gen2 (3.0 Gb/s) speed for reduced power consumption. If (PMxD9_x02[SataGen2] ==1), this bit becomes don't-care and SATA controller operates in maximum Gen2 (3.0 Gb/s) speed.
1	Reserved.
0	SataEnable. Read-write. Cold reset: 1. BIOS: 1. 0=SATA controller is disabled. 1=SATA controller is enabled. Whenever SATA controller is being enabled by programming this field from 0 to 1, a IOCF9 software reset is recommended to reset the controller to a proper operational state.

PMxDC SataConfig2

Bits	Description
16	PllCalibEn: SATA PHY PLL calibration enable. Read-write. Reset: 0. BIOS: See 2.15.3.3 .

PMxE0 ABRegBar

Bits	Description
31:16	Reserved.
15:3	ABRegBar. Read-write. Cold reset: 0. BIOS: See 2.15.10 . IO Base address of AB Configuration Registers. See AB configuration registers defined in 3.26.2 [AB Configuration Registers (Scallion)] .
2:0	Reserved.

PMxE8 SDFlashCntrl

Bits	Description
7:2	Reserved.
0	SDFlashEnable . Read-write. Cold reset: 0. 0=Disable SD flash controller. 1=Enable SD flash controller, and GPIO[73:80] become SD flash interface.

PMxEB AzEn

Bits	Description
7:2	Reserved.
1	AzNoSnoopEnable . Read-write. Cold reset: 0. 1=HD audio data transfer doesn't cause the AcpIPmEvtBlkx00[BmStatus] bit to be set nor to wake up the CPU from C3 state. Under current C1e implementation, there is no need to set this bit.
0	AzEnable . Read-write. Cold reset: 1. BIOS: 1. 0=Disable HD audio controller. 1=Enable HD audio controller.

PMxEC LpcGating

Bits	Description
2	AbNoBypassEn . Read-write. Cold reset: 0. BIOS: 1. 1=Enable the fix for TeamTrack #SB02634 (Solution 1); Tells the A-Link that the LPC cycle should not be bypassed when a retry has timed out.
1	LpcA20En . Read-write. Cold reset: 0. 1=Enable A20# input.
0	LpcEnable . Read-write. Cold reset: 1. 1=Enable LPC bridge.

PMxED USB Gating

Bits	Description
7:5	Reserved.
4	UsbSmiEn . Read-write; S3-check-exclude. Cold reset: 0. 1=Enable SMI for USB legacy support.
1	UsbIrqEn . Read-write. Cold reset: 0. 1=Route IRQ1/IRQ12 from USB OHCI to PIC/IOAPIC for USB legacy support.
0	UsbA20En . Read-write. Cold reset: 0. 1=Enable A20Gate from USB OHCI controller for USB legacy support.

PMxEF USB Enable

BIOS: See [2.15.2.4 \[Enabling the xHCI Controller\]](#) && [2.15.2.14 \[xHCI Enable OHCI3/EHCI3 on S4/S5 State Entry\]](#).

Bits	Description
7	PortRoutingSelect . Read-write. Cold reset: 0. Specifies controller(s) for USB ports 8 and 9. 0=EHCI 3 and OHCI 3 controllers. 1=xHCI controller.

6	Reserved. Cold reset: 1.
5	Usb3EhciEnable . Read-write. Cold reset: 1. 1=Enable EHCI 3 controller.
4	Usb3OhciEnable . Read-write. Cold reset: 1. 1=Enable OHCI 3 controller (device 16h, function 0).
3	Usb2EhciEnable . Read-write. Cold reset: 1. 1=Enable EHCI 2 controller.
2	Usb2OhciEnable . Read-write. Cold reset: 1. 1=Enable OHCI 2 controller (device 13h, function 0).
1	Usb1EhciEnable . Read-write. Cold reset: 1. 1=Enable EHCI 1 controller.
0	Usb1OhciEnable . Read-write. Cold reset: 1. 1=Enable OHCI 1 controller (device 12h, function 0).

PMxF0 USB Control

Table 238: BIOS Recommendations for UsbPhyS5PwrDwnEnable

Option	Description	Setting	Comment
1	USB Wake from S5 not supported on the platform	1	When the USB power rails USB PHY PLL, USB PHY core power and USB PHY DLL are connected to S0-S3 power, set the bit to 1 to disable the USB S4/S5 wake up function
2	USB Wake from S5 supported on the platform	0	When the USB power rails USB PHY PLL, USB PHY core power and USB PHY DLL are connected to S5 power, set the bit to 0 to enable the USB S4/S5 wakeup function

Bits	Description																		
15	PmioEhciMemSlpDis . Read-write. Cold Reset: 0. 0=Enable EHCI memory sleep. 1=Disable EHCI memory sleep.																		
12	Usb2B1GlobalClkGateEn . Read-write. Cold reset: 1. 1=Enable USB2.0 B-Link Global Clock Gating.																		
11	Reserved.																		
10:8	UsbSleepCtrl . Read-write. Cold reset: 3h. Control on USB advanced asynchronous sleep function. Setting of 000b:100b are for the advanced asynchronous sleep. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>Standard 10 us sleep</td> </tr> <tr> <td>001b</td> <td>Advanced sleep for up to 2 micro frames</td> </tr> <tr> <td>010b</td> <td>Advanced sleep for up to 4 micro frames</td> </tr> <tr> <td>011b</td> <td>Advanced sleep for up to 6 micro frames</td> </tr> <tr> <td>100b</td> <td>Advanced sleep for up to next micro frame</td> </tr> <tr> <td>101b</td> <td>Reserved</td> </tr> <tr> <td>110b</td> <td>Reserved</td> </tr> <tr> <td>111b</td> <td>If CPU is in C state and the controller has already exhausted the link list, it can simply stop the asynchronous packets until CPU resumes back to C0 state. In this case, the controller will resume back to its standard mode.</td> </tr> </tbody> </table>	Bits	Definition	000b	Standard 10 us sleep	001b	Advanced sleep for up to 2 micro frames	010b	Advanced sleep for up to 4 micro frames	011b	Advanced sleep for up to 6 micro frames	100b	Advanced sleep for up to next micro frame	101b	Reserved	110b	Reserved	111b	If CPU is in C state and the controller has already exhausted the link list, it can simply stop the asynchronous packets until CPU resumes back to C0 state. In this case, the controller will resume back to its standard mode.
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011b	Advanced sleep for up to 6 micro frames																		
100b	Advanced sleep for up to next micro frame																		
101b	Reserved																		
110b	Reserved																		
111b	If CPU is in C state and the controller has already exhausted the link list, it can simply stop the asynchronous packets until CPU resumes back to C0 state. In this case, the controller will resume back to its standard mode.																		
5	PmioOhciMemSlpDis . Read-write. Cold reset: 0. 0=Enable OHCI memory sleep mode. 1=Disable OHCI memory sleep mode.																		
4	Usb11PdResistorEnable . Read-write. Cold reset: 1. 0=Disconnect pull-down resistors on stand-alone USB1.1 pads.																		

3	UsbS5ResetEnable. Read-write. Cold reset: 1. 1=Enable USB reset on S4/S5 resume detection.
2	UsbKbResetEnable. Read-write. Cold reset: 1. BIOS: See 2.15.2.3 . 1=Enable resetting USB on keyboard reset.
1	Reserved.
0	UsbPhyS5PwrDwnEnable. Read-write. Cold reset: 0. BIOS: See Table 238 . 1=Enable S4/S5 USB PHY power down support and disable S4 USB wake up support. 0=Disable S4/S5 USB PHY power down support and enable S4 USB wakeup support. The bit has to be set to 0 to support S4 USB wake up.

3.26.14 Power Management Block 2 (PM2) Registers

PM2 register space is accessed through two methods:

- Indirect IO access through index/data address pair at [IOCD0 \[PM2_Index\]](#) and [IOCD1 \[PM2_Data\]](#). Software first programs the offset into the index register [IOCD0 \[PM2_Index\]](#) and then reads/writes to/from the data register [IOCD1 \[PM2_Data\]](#).
- Direct memory mapped or IO mapped access through the AcpiMmio region. The PM2 registers range from [PMx24\[AcpiMmioAddr\]+400h](#) to [PMx24\[AcpiMmioAddr\]+4FFh](#). See [PMx24 \[AcpiMmioEn\]](#).

PM2x00 Fan0InputControl

Bits	Description										
7:4	Reserved.										
3	TwoRampAlgorithmEn. Read-write. Reset: 0. 1=The two ramp fan control algorithm is enabled. 0=Disabled.										
2:0	FanInputControl. Read-write. Reset: 0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>100b-000b</td> <td>Reserved.</td> </tr> <tr> <td>101b</td> <td>FanOut0 is enabled and temperature input is from TempTsi.</td> </tr> <tr> <td>110b</td> <td>FanOut0 is enabled and temperature input is 0.</td> </tr> <tr> <td>111b</td> <td>FanOut0 is disabled.</td> </tr> </tbody> </table>	Bits	Definition	100b-000b	Reserved.	101b	FanOut0 is enabled and temperature input is from TempTsi.	110b	FanOut0 is enabled and temperature input is 0.	111b	FanOut0 is disabled.
Bits	Definition										
100b-000b	Reserved.										
101b	FanOut0 is enabled and temperature input is from TempTsi.										
110b	FanOut0 is enabled and temperature input is 0.										
111b	FanOut0 is disabled.										

PM2x01 Fan0Control

When [AutoMode] == 1, the active duty cycle is controlled by the hardware automatically.

- If ActualTemperature < LowTemp {[PM2x07](#), [PM2x06](#)}, DutyCycle = 0;
- If LowTemp {[PM2x07](#), [PM2x06](#)} <= ActualTemperature < MedTemp {[PM2x09](#), [PM2x08](#)}, DutyCycle = [PM2x03 \[LowDuty0\]](#).
- If MedTemp {[PM2x09](#), [PM2x08](#)} <= ActualTemperature < HighTemp {[PM2x0B](#), [PM2x0A](#)},
 - If [LinearMode] == 0, DutyCycle = [PM2x04 \[MedDuty0\]](#).
 - If [LinearMode] == 1, DutyCycle = ((ActualTemperature - LowTemp {[PM2x07](#), [PM2x06](#)}) * ([PM2x05\[Multiplier\]](#) + 1)) >> [PM2x05\[DutySel\]](#) + [PM2x03 \[LowDuty0\]](#).
- If ActualTemperature >= HighTemp {[PM2x0B](#), [PM2x0A](#)}, DutyCycle = 100%.

In Automode, hysteresis limit defined by [PM2x0C \[LinearRange0\]](#) is applied to keep the fan from oscillating erratically.

Bits	Description
7:3	LinearAdjust. Read-write. Reset: 0. Specifies the additional offset to effective duty cycle under Linear mode.

2	FanPolarity . Read-write. Reset: 0. 0=FanOut0 drives low. 1=FanOut0 drives high.
1	LinearMode . Read-write. Reset: 0. 0=Use step function. 1=Use Linear function. See above description for details.
0	AutoMode . Read-write. Reset: 0. 0=FanOut0 is controlled by PM2x03 [LowDuty0] . 1=FanOut0 is controlled by the temperature input. See the above description for details on AutoMode.

PM2x02 Fan0Freq

Bits	Description	
7:0	FanFreq . Read-write. Reset: 0. Normally, 4-wire fan runs at 25 kHz and 3-wire fan runs at 100 Hz. FanOut0 frequency is programmed as below:	
	<u>Bits</u>	<u>Definition</u>
	00h	28.64 kHz
	01h	25.78 kHz
	02h	23.44 kHz
	03h	21.48 kHz
	04h	19.83 kHz
	05h	18.41 kHz
	F7h	100 Hz
	F8h	87 Hz
	<u>Bits</u>	<u>Definition</u>
	F9h	58 Hz
	FAh	44 Hz
	FBh	35 Hz
	FCh	29 Hz
	FDh	22 Hz
	FEh	14 Hz
	FFh	11 Hz
	F6h-06h	
	1/(FanFreq*2048*15 ns)	

PM2x03 LowDuty0

Bits	Description	
7:0	LowDuty0 . Read-write. Reset: 0. Specifies Fan0 duty number if (LowTemp{ PM2x07 , PM2x06 } <= temperature < MedTemp{ PM2x09 , PM2x08 }). There are 256 time slots in one fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot 0~ slot N, and stops from slot (N+1) ~ slot 255.	
	<u>Bits</u>	<u>Definition</u>
	00h	Always stop
	FEh-01h	Fan spins for time slots <= LowDuty, stops for time slots > LowDuty.
	FFh	Full speed run

PM2x04 MedDuty0

Bits	Description	
7:0	MedDuty . Read-write. Reset: 0. Specifies Fan0 duty number using step function if (MedTemp{ PM2x09 , PM2x08 } <= temperature <= HighTemp{ PM2x0B , PM2x0A }). There are 256 time slots in one fan cycle. Duty number N represents the (N+1)th time slot. Fan actively spins in time slot0 ~ slotN, and stops from slot (N+1) ~ slot255.	
	<u>Bits</u>	<u>Definition</u>
	00h	Always stop
	FEh-01h	Fan spins for time slots <= MedDuty, stops for time slots > MedDuty.
	FFh	Full speed run

PM2x05 Multiplier0

When ([PM2x01\[AutoMode\] == 1](#)) && ([PM2x00\[TwoRampAlgorithm\] == 1](#)), Fan0 is in TwoRamp mode. The slope value of ramp1 and ramp0 is: Slope[7:0] = {[PM2x05\[DutySel\]](#), [PM2x05\[Multiplier\]](#)}. Slope[7:2] are the integer bits and Slope[1:0] are the fractional bits of the ramp slope.

BIOS has to calculate Slope[7:0] using the following equation:

$$\text{Slope} = (16'hFF00 - \{\text{LowDuty0}[7:0], 8'b0\}) / (\text{HighTemp0}[15:0] - \text{Hysteresis0}[15:0] - \text{MedTemp0}[15:0])$$

For example, if our setting is:

$$\text{LowDuty0}[7:0] = 25\% = 40h$$

$$\text{HighTemp0}[15:0] = 90^{\circ}\text{C} = 5A00h$$

$$\text{MedTemp0}[15:0] = 40^{\circ}\text{C} = 2800h$$

$$\text{Hysteresis0}[15:0] = 10^{\circ}\text{C} = 0A00h$$

Then:

$$\text{Slope} = (FF00h - 4000h) / (5A00h - 0A00h - 2800h) = 48896 / 10240 = 4.775$$

Convert the number 4.775 into our 8-bit format: 00010011b (13h). BIOS should program the Multiplier0 register as 13h in this example.

Bits	Description
7:6	DutySel . Read-write. Reset: 0. When Fan0 is programmed in AutoMode with linear function being selected, this field selects part of duty to be fed into fan as described in PM2x01 [Fan0Control] register description. When Fan0 is programmed in TwoRamp mode, this field specifies the upper 2 bits in Slope[7:0]. See the above register description for detail.
5:0	Multiplier . Read-write. Reset: 0. When Fan0 is programmed in AutoMode with linear function being selected, this field specifies the factor to calculate duty number as described in PM2x01 [Fan0Control] register description. When Fan0 is programmed in TwoRamp mode, this field specifies the lower 6 bits in Slope[7:0]. See the above register description for detail.

PM2x06 LowTemp0Lo

Bits	Description
7:0	LowTemp0[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of low temperature threshold.

PM2x07 LowTemp0Hi

Bits	Description
7:0	LowTemp0[15:8] . Read-write. Reset: 0. Specifies the higher 8 bits of low temperature threshold.

PM2x08 MedTemp0Lo

Bits	Description
7:0	MedTemp0[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of medium temperature threshold.

PM2x09 MedTemp0Hi

Bits	Description
7:0	MedTemp0[15:8] . Read-write. Reset: 0. Specifies the higher 8 bits of medium temperature threshold.

PM2x0A HighTemp0Lo

Bits	Description
7:0	HighTemp0[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of high temperature threshold.

PM2x0B HighTemp0Hi

Bits	Description
7:0	HighTemp0[15:8] . Read-write. Reset: 0. Specifies the higher 8 bits of high temperature threshold.

PM2x0C LinearRange0

Bits	Description
7:0	LinearRange . Read-write. Reset: 0. Specifies a variable range that Fan0 can tolerate. Fan0 is not affected if temperature varies within this range.

PM2x0D LinearHoldCount0

Bits	Description
7:0	LinearHoldCount . Read-write. Reset: 0. Specifies the fan cycles to be waited before duty cycle can be changed.

PM2x0E Fan0Hysteresis

Bits	Description
15:8	HysteresisHi . Read-write. Reset: 0. Specifies the hysteresis value (in temperature) of the Two Ramp Fan Control Algorithm. The unit is °C. See PM2x05 [Multiplier0] on how to program this register.
7:0	HysteresisLo . Read-write. Reset: 0. Reserved. This byte should always be programmed as 0.

PM2x50 Med2Temp0Lo

Bits	Description
7:0	Med2Temp0[7:0] . Read-write. Reset: 0. IF (PM2x00[TwoRampAlgorithmEn]==1) THEN It specifies the lower byte of the temperature value of the turning point on the ramp. ELSE Unused. ENDIF.

PM2x51 Med2Temp0Hi

Bits	Description
7:0	Med2Temp0[15:8] . Read-write. Reset: 0. IF (PM2x00 [TwoRampAlgorithmEn]==1) THEN It specifies the higher byte of the temperature value of the turning point on the ramp. ELSE Unused. ENDIF.

PM2x52 Med2Duty0

Bits	Description
7:0	Med2Duty0[7:0] . Read-write. Reset: 0. IF (PM2x00 [TwoRampAlgorithmEn]==1) THEN It specifies the fan duty value of the turning point on the ramp. ELSE Unused. ENDIF.

PM2x53 Multiplier2_0

BIOS has to calculate Multiplier2_0[7:0] using the following equation:

$$\text{Multiplier2_0} = (\{\text{Med2Duty0}[7:0], 8'b0\} - \{\text{LowDuty0}[7:0], 8'b0\}) / (\text{Med2Temp0}[15:0] - \text{MedTemp0}[15:0])$$

For example, if our setting is:

$$\text{PM2x52}[\text{Med2Duty0}[7:0]] = 50\% = 80h$$

$$\text{PM2x03}[\text{LowDuty0}[7:0]] = 25\% = 40h$$

$$\text{Med2Temp0}[15:0] = \{\text{PM2x51, PM2x50}\} = 70^{\circ}\text{C} = 4600h$$

$$\text{MedTemp0}[15:0] = \{\text{PM2x09, PM2x08}\} = 40^{\circ}\text{C} = 2800h$$

Then:

$$\text{Multiplier2_0}[7:0] = (8000h - 4000h) / (4600h - 2800h) = 16384 / 7680 = 2.133$$

Convert the number 4.775 into our 8bit format: 00001000b (08h). BIOS should program Multiplier2_0 register as 08h in this example.

Bits	Description						
7:0	Multiplier2_0[7:0] . Read-write. Reset: 0. BIOS: See above description. IF (PM2x00 [TwoRampAlgorithmEn]==1) THEN It specifies the slope value of ramp1lo and ramp0lo. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[1:0]</td> <td>Integer bits of the ramp slope</td> </tr> <tr> <td>[7:2]</td> <td>Fractional bits of the ramp slope</td> </tr> </tbody> </table>	Bit	Definition	[1:0]	Integer bits of the ramp slope	[7:2]	Fractional bits of the ramp slope
Bit	Definition						
[1:0]	Integer bits of the ramp slope						
[7:2]	Fractional bits of the ramp slope						

PM2x60 FanStatus

Bits	Description
7:1	Reserved.
0	Fan0SpeedTooSlow . Read; write-1-to-clear. Reset: 0. 1=Fan0 runs slower than the value in the Fan0SpeedLimit{ PM2x68 , PM2x67 }.

PM2x61 FanINTRouteLo

Bits	Description

7:2	Reserved.
1:0	Fan0INTRoute . Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b No SCI/SMI generated 01b SMI 10b SMI or SCI depending on GEVENT13 routing 11b No SCI/SMI generated

PM2x63 SampleFreqDiv

Bits	Description
7:4	LinearRangeOutLimit[4:1] . Read-write. Reset:0. LinearRangeOutLimit[7:0] = {000b, LinearRangeOutLimit[4:1], 1b}. LinearRangeOutLimit specifies how close the fan duty follows the target duty cycle and is only used when the fan duty is changing. It is different from the PM2x0C [LinearRange0] , which works like a hysteresis and used when fan duty is not changing.
3	Reserved.
2	FanLinearEnhanceEn2 . Read-write. Reset: 0. 1=The positive hysteresis of fan duty is removed; PM2x0C [LinearRange0] only applies to the negative direction; As a result, the fan duty increases once the temperature is increased instead of waiting for a hysteresis.
1:0	SampleFreqDiv . Read-write. Reset: 0. This field specifies the sampling rate of Fan Speed. <u>Bits</u> <u>Definition</u> 00b Base (22.5 kHz) 01b Base (22.5 kHz) / 2 10b Base (22.5 kHz) / 4 11b Base (22.5 kHz) / 8

PM2x64 FanDebounceCounterLo

Bits	Description
7:0	FanDebounceCounter[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of the debounced counter when measuring fan speed.

PM2x65 FanDebounceCounterHi

Bits	Description
7:0	FanDebounceCounter[15:8] . Read-write. Reset: 0. Specifies the high 8 bits of the debounced counter when measuring fan speed.

PM2x66 Fan0DetectorControl

Bits	Description
7:5	Reserved.
4	ShutDownEnable . Read-write. Reset: 0. 1=The system will be shut down if PM2x60[Fan0SpeedTooSlow] remains 1 for more than 4 seconds.

3:2	Reserved.
1	UseAverage . Read-write. Reset: 0. 0=Do not to use average fan0 speed. 1=Use average fan0 speed.
0	FanDetectorEnable . Read-write. Reset: 0. 0=Disable fan0 speed measurement. 1=Enable fan0 speed measurement.

PM2x67 Fan0SpeedLimitLo

Bits	Description
7:0	FanSpeedLimit[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of Fan0SpeedLimit

PM2x68 Fan0SpeedLimitHi

Bits	Description
7:0	FanSpeedLimit[15:8] . Read-write. Reset: 0. Specifies the higher 8 bits of Fan0SpeedLimit.

PM2x69 Fan0SpeedLo

Bits	Description
7:0	FanSpeed[7:0] . Read-only; updated-by-hardware. Reset: 0. Specifies the lower 8 bits of fan0 speed.

PM2x6A Fan0SpeedHi

Bits	Description
7:0	FanSpeed[15:8] . Read-only; updated-by-hardware. Reset: 0. Specifies the higher 8 bits of fan0 speed.

PM2x8A TempTsiLo

Bits	Description
7:0	TempTsi[7:0] . IF (PM2x8F [TempTsiWe]==1) THEN Read-Write. ELSE Read-only; updated-by-hardware. ENDIF. Reset: 0. Specifies the lower 8 bits of TempTsi.

PM2x8B TempTsiHi

Bits	Description
7:0	TempTsi[15:8] . IF (PM2x8F [TempTsiWe]==1) THEN Read-Write. ELSE Read-only; updated-by-hardware. ENDIF. Reset: 0. Specifies the higher 8 bits of TempTsi.

PM2x8C TempTsiLimitLo

Bits	Description
7:0	TempTsiLimit[7:0] . Read-write. Reset: 0. Specifies the lower 8 bits of TempTsiLimit.

PM2x8D TempTsiLimitHi

Bits	Description
7:0	TempTsiLimit[15:8] . Read-write. Reset: 0. Specifies the higher 8 bits of TempTsiLimit.

PM2x8E TempTsiChangeLimit

If (TempTsiChangeLimit != 0), filtering is applied to TempTsi {[PM2x8B \[TempTsiHi\]](#), [PM2x8A \[TempTsiLo\]](#)} as below:

- If TempTsi_New > (TempTsi_Old + (TempTsiChangeLimit<<6)), then
- If TempTsi_New < (TempTsi_Old - (TempTsiChangeLimit<<6)), then
- If (Temp_Old - (TempTsiChangeLimit<<6)) <= TempTsi_New <= (TempTsi_Old + (TempTsiChangeLimit<<6)), then

Bits	Description
7:0	TempTsiChangeLimit . Read-write. Reset: 0.

PM2x8F TempTsiWe

Bits	Description
7:6	Reserved.
5	TempTsiWe: TempTsi Write Enable . Read-write. Reset: 0. 0=TempTsi registers, PM2x8B [TempTsiHi] and PM2x8A [TempTsiLo] , are read-only and updated by hardware with the result from TempTsi sensor. 1=TempTsi registers are writable only by host and IMC; they are not updated by hardware with the result from the TempTsi sensor.
4:0	Reserved.

PM2x90 TempTsiStatus

Bits	Description
7:6	Reserved.
5	TempTsiStatus . Write-1-to-clear; Read. Reset: 0. 1=TempTsi { PM2x8B [TempTsiHi] , PM2x8A [TempTsiLo] } is out of the limit.
4:0	Reserved.

PM2x92 TempTsiControl

Bits	Description
7:4	Reserved.
3:2	TempTsiControl. Read-write. Reset: 0. TempTsi sensor is enabled if (TempTsiControl != 0). <u>Bits</u> <u>Definition</u> 00b Disable. 01b If (TempTsi > TempTsiLimit), then PM2x90 [TempTsiStatus] = 1. 10b If (TempTsi < TempTsiLimit), then PM2x90 [TempTsiStatus] = 1. 11b If ((TempTsiHi > TempTsiLimitLo) (TempTsiHi < TempTsiLimitHi)), then PM2x90 [TempTsiStatus] = 1.
1:0	Reserved.

PM2x94 TempTsiINTRoute

Bits	Description
7:4	Reserved.
3:2	TempTsiINTRoute. Read-write. Reset: 0. <u>Bits</u> <u>Definition</u> 00b No SCI/SMI generated. 01b SMI 10b SMI or SCI according to GEVENT 13 INT routing. 11b No SCI/SMI generated.
1:0	Reserved.

PM2xDF TempTsiRstSel

Bits	Description
7:6	Reserved.
5	TempTsiRstSel. Read-write. Reset: 0. 1=Thermal diode monitoring function is not stopped by reset.
4:0	Reserved.

PM2xE0 AlertThermaltripStatus

Bits	Description
7:2	Reserved.
1	ThermalTripStatus. Read-only; updated-by-hardware. Reset: 0. 0=Current temperature is not above ThermalTripLimit. 1=Current temperature is above ThermalTripLimit.
0	AlertStatus. Read-only; updated-by-hardware. Reset: 0. 0=Current temperature is not above AlertLimit. 1=Current temperature is above AlertLimit.

PM2xE1 AlertLimitLo

Bits	Description
7:0	AlertLimit[7:0] . Read-write. Reset: 0.

PM2xE2 AlertLimitHi

Bits	Description
7:0	AlertLimit[15:8] . Read-write. Reset: 0.

PM2xE3 ThermalTripLimitLo

Bits	Description
7:0	ThermalTripLimit[7:0] . Read-write. Reset: 0.

PM2xE4 ThermalTripLimitHi

Bits	Description
7:0	ThermalTripLimit[15:8] . Read-write. Reset: 0.

PM2xE5 AlertThermaltripControl

Bits	Description								
7:5	TempSelAlert . Read-write. Reset: 0. This field selects which temperature sensor is the event source. It converts the selected Temp input pin into either TAlert or ThermalTrip function. <table> <thead> <tr> <th>Bits</th> <th>Field Definition</th> </tr> </thead> <tbody> <tr> <td>100b-000b</td> <td>Reserved</td> </tr> <tr> <td>101b</td> <td>TempTsi</td> </tr> <tr> <td>111b-110b</td> <td>Reserved</td> </tr> </tbody> </table>	Bits	Field Definition	100b-000b	Reserved	101b	TempTsi	111b-110b	Reserved
Bits	Field Definition								
100b-000b	Reserved								
101b	TempTsi								
111b-110b	Reserved								
4:2	Reserved.								
1:0	AlertControl . Read-write. Reset: 0. <table> <thead> <tr> <th>Bit</th> <th>Field Definition</th> </tr> </thead> <tbody> <tr> <td>[1]</td> <td>Enable ThermalTrip on the selected Temp input</td> </tr> <tr> <td>[0]</td> <td>Enable TAlert on the selected Temp input</td> </tr> </tbody> </table>	Bit	Field Definition	[1]	Enable ThermalTrip on the selected Temp input	[0]	Enable TAlert on the selected Temp input		
Bit	Field Definition								
[1]	Enable ThermalTrip on the selected Temp input								
[0]	Enable TAlert on the selected Temp input								

3.26.15 Standard ACPI Registers

These are the standard registers defined by the ACPI specification. In order to access these ACPI registers, [PMx74\[DecEnAcpi\]](#) must be programmed to 1. ACPI registers are accessed through two methods:

- IO mapped access through base addresses defined by [PMx60](#) through [PMx6E](#).
- Memory mapped or IO mapped access through the AcpiMmio region. The ACPI registers range from [PMx24\[AcpiMmioAddr\]+800h](#) to [PMx24\[AcpiMmioAddr\]+8FFh](#). See [PMx24 \[AcpiMmioEn\]](#).

3.26.15.1 AcpiPmEvtBlk

The IO mapped base address of this register block is defined by [PMx60](#). Its offset in the AcpiMmio region is 800h.

AcpiPmEvtBlkx00 Pm1Status

Bits	Description
15	WakeStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=The system is in the sleep state and a wake-up event occurs.
14	PciExpWakeStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=The system wake is due to a PCI Express wakeup event.
13:11	Reserved.
10	RtcStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=RTC generates an alarm. If both AcpiPmEvtBlkx02[RtcEn] and this bit are set to 1, a power management event: SCI, SMI, or resume event, is generated.
9	Reserved. Read-write.
8	PwrBtnStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. Power button status bit. 1=The Power Button is pressed. In the system working state, if AcpiPmEvtBlkx02[PwrBtnEn] and this bit are both set to 1, an interrupt event is raised. In the sleeping or soft-off state, a wake event is generated when the power button is pressed regardless of the setting of AcpiPmEvtBlkx02[PwrBtnEn] .
7:6	Reserved.
5	GblStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=An SCI is generated due to the BIOS wanting the attention of the SCI handler; Writing 1 to PMx74[BiosRls] sets this bit.
4	BmStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. Bus master status bit. 1=A system bus master requests the system bus. Note: this bit is no longer used.
3:1	Reserved.
0	TmrStatus . Read; set-by-hardware; write-1-to-clear. Reset: 0. Timer carry status bit. 1=The 31st bit of the 32-bit counter changes from low to high or high to low. If both AcpiPmEvtBlkx02[TmrEn] and this bit are set to 1, an interrupt event is raised.

AcpiPmEvtBlkx02 Pm1Enable

Bits	Description
15	Reserved.
14	PciExpWakeDis . Read-write. Reset: 1. 1=Disable the inputs to AcpiPmEvtBlkx00[PciExpWakeStatus] from waking the system.
13:11	Reserved. Read-write.
10	RtcEn . Read-write. Reset: 0. 1=A wake event is generated whenever AcpiPmEvtBlkx00[RtcStatus] is also set to 1.
9	Reserved.
8	PwrBtnEn . Read-write. Reset: 0. 1=A power management event (SCI or wake) is generated whenever AcpiPmEvtBlkx00[PwrBtnStatus] is also set to 1.
7:6	Reserved.

5	GblEn. Read-write. Reset: 0. 1=An SCI is raised whenever AcpiPmEvtBlkx00 [GblStatus] is also set to 1.
4:1	Reserved.
0	TmrEn. Read-write. Reset: 0. This is the timer carry interrupt enable bit. 1=An SCI event is generated whenever the AcpiPmEvtBlkx00 [TmrStatus] is set to 1. 0=No interrupt is generated when the AcpiPmEvtBlkx00 [TmrStatus] bit is set to 1.

3.26.15.2 AcpiPm1CntBlk

The IO mapped base address of this register block is defined by [PMx62](#). Its offset in the AcpiMmio region is 804h.

AcpiPm1CntBlkx00 PmControl

Bits	Description
15:14	Reserved. Read-write.
13	SlpTypeEn. RAZ; write-1-only. Reset: 0. 1=The system sequences into the sleeping state defined by SlpTyp when PMxBE [SlpTypeControl] is set to 1.
12:10	SlpTyp. Read-write. Reset: 0. Specifies the sleep state the system enters if SlpTypeEn is set to 1. This design currently implements 5 states: S0, S1, S3, S4, and S5.
9:3	Reserved.
2	GblRls. RAZ; write-only. Reset: 0. If SMIxB0 [17:16] is set to 01b, writing 1 to this bit generates SMI and sets SMIx88 [8].
1	BmRld. Read-write. Reset: 0. 1=Any bus master activity causes the C state logic to break out from C3. This is no longer needed for current C state implementation.
0	SciEn. Read-write. Reset: 0. Selects the power management event to be either an SCI or SMI interrupt for the power management events. 1=Power management events generate SCI interrupts; 0=Power management events generate SMI interrupts.

3.26.15.3 AcpiPm2CntBlk

The IO mapped base address of this register block is defined by [PMx6E](#). Its offset in the AcpiMmio region is 824h.

AcpiPm2CntBlkx00 Pm2Control

Bits	Description
7:1	Reserved.
0	ArbDis. Read-write. Reset: 0. 1=System arbiter is disabled. Note: Under the current C state implementation, this is no longer used and should not be reported to OS.

3.26.15.4 AcpiPmTmrBlk

The IO mapped base address of this register block is defined by [PMx64](#). Its offset in the AcpiMmio region is 808h.

AcpiPmTmrBlkx00 TmrValue/ETmrValue

Bits	Description
31:0	TmrValue. Read-only. Reset: X. It returns the running count of the power management timer (ACPI timer).

3.26.15.5 CpuCntBlk

The IO mapped base address of this register block is defined by [PMx66](#). Its offset in the AcpiMmio region is 80Ch.

CpuCntBlkx00 ClkValue

Bits	Description																				
31:5	Reserved.																				
4	ThtEn. Read-write. Reset: 0. 1=Enable clock throttling as programmed in ClkValue.																				
3:1	ClkValue. Read-write. Reset: 0. Specifies the throttle interval for STPCLK in software clock throttling. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>50%</td> <td>100b</td> <td>50%</td> </tr> <tr> <td>001b</td> <td>12.5%</td> <td>101b</td> <td>62.5%</td> </tr> <tr> <td>010b</td> <td>25%</td> <td>110b</td> <td>75%</td> </tr> <tr> <td>011b</td> <td>37.5%</td> <td>111b</td> <td>87.5%</td> </tr> </tbody> </table>	Bits	Definition	Bits	Definition	000b	50%	100b	50%	001b	12.5%	101b	62.5%	010b	25%	110b	75%	011b	37.5%	111b	87.5%
Bits	Definition	Bits	Definition																		
000b	50%	100b	50%																		
001b	12.5%	101b	62.5%																		
010b	25%	110b	75%																		
011b	37.5%	111b	87.5%																		
0	Reserved.																				

CpuCntBlkx04 PLvl2

Bits	Description
7:0	PLvl2. RAZ; read-only. Reset: 0. Reads to this register return all zeros and generate an “enter C2” sequence to APU.

CpuCntBlkx05 PLvl3

Bits	Description
7:0	PLvl3. RAZ; read-only. Reset: 0. Reads to this register return all zeros and generate an “enter C3” sequence to APU.

3.26.15.6 AcpiGpe0Blk

The IO mapped base address of this register block is defined by [PMx68](#). Its offset in the AcpiMmio region is 814h.

AcpGpe0Blkx00 EventStatus

Bits	Description
31:0	EventStatus. Read; write-1-to-clear. Reset: X. Each bit represents an ACPI event status. For each bit, 1=The selected event input equals to the corresponding value in SMIx08 [SciTrig] . Configuration for the events are located at SMIx08 [SciTrig] through SMIx78 [SciMap14] . The status bits are also mirrored in SMIx00 [Event_Status] .

AcpGpe0Blkx04 EventEnable

Bits	Description
31:0	EventEnable. Read-write. Reset: 0. Each bit controls whether ACPI should generate wakeup and SCI interrupt. The enable bits are also mirrored in SMIx04 [Event_Enable] .

3.26.15.7 SmiCmdBlk

The IO mapped base address of this register block is defined by [PMx6A](#). Its offset in the AcpIMmio region is 81Ch.

SmiCmdBlkx00 SmiCmdPort

Bits	Description
7:0	SmiCmdPort. Read-write. Reset: 0. When SMI command port is enabled, a write to this port generates SMI, NMI or IRQ3 depending on the setting of SMIxB0[23:22] . A read from this port returns the previously written value but does not generate SMI. The SMI command port has to be located at an even address (ie, 0, 2, 4, 6,8, A, C, or E). SmiCmdStatus is always located one byte immediately after the SmiCmdPort. The implementation actually contains four (4) bytes of address space. If SMI command port is assigned to byte 0, then byte 1 is SmiCmdStatus. Byte 2 and 3 can be used as scratch. If SmiCmdPort is assigned to byte 2, then bytes 0 and 1 are not available.

SmiCmdBlkx01 SmiCmdStatus

Bits	Description
7:0	SmiCmdStatus. Read-write. Reset: 0. Used by BIOS and OS.

3.26.16 SMI Registers

SMI register space is accessed through the AcpiMmio region, which can be memory mapped or IO mapped. The SMI registers range from [PMx24\[AcpimMmioAddr\]+200h](#) to [PMx24\[AcpimMmioAddr\]+2FFh](#). See [PMx24 \[AcpimMmioEn\]](#).

SMIx00 Event_Status

Bits	Description
31:0	EventStatus . Read; write-1-to-clear. Reset: X. This is a mirror register of the standard ACPI register AcpGpe0Blkx00 [EventStatus] . Each event status bit is set when the selected event input equals to the corresponding value in SMIx08 [SciTrig] .

SMIx04 Event_Enable

Bits	Description
31:0	EventEnable . Read-write. Reset: 0. This is the mirror register of the standard ACPI register AcpGpe0Blkx04 [EventEnable] . Each bit controls whether ACPI should generate wake up and SCI interrupt.

SMIx08 SciTrig

Each bit in this register controls the way to set each corresponding bit in [SMIx00 \[Event_Status\]](#).

Bits	Description
31	SciTrig31 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 31. 0=Active low. 1=Active high.
30	SciTrig30 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 30. 0=Active low. 1=Active high.
29	SciTrig29 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 29. 0=Active low. 1=Active high.
28	SciTrig28 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 28. 0=Active low. 1=Active high.
27	SciTrig27 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 27. 0=Active low. 1=Active high.
26	SciTrig26 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 26. 0=Active low. 1=Active high.
25	SciTrig25 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 25. 0=Active low. 1=Active high.
24	SciTrig24 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 24. 0=Active low. 1=Active high.
23	SciTrig23 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 23. 0=Active low. 1=Active high.
22	SciTrig22 . Read-write. Reset: 1. The bit controls the way to set Event_Status bit 22. 0=Active low. 1=Active high.

21	SciTrig21. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 21. 0=Active low. 1=Active high.
20	SciTrig20. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 20. 0=Active low. 1=Active high.
19	SciTrig19. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 19. 0=Active low. 1=Active high.
18	SciTrig18. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 18. 0=Active low. 1=Active high.
17	SciTrig17. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 17. 0=Active low. 1=Active high.
16	SciTrig16. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 16. 0=Active low. 1=Active high.
15	SciTrig15. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 15. 0=Active low. 1=Active high.
14	SciTrig14. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 14. 0=Active low. 1=Active high.
13	SciTrig13. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 13. 0=Active low. 1=Active high.
12	SciTrig12. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 12. 0=Active low. 1=Active high.
11	SciTrig11. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 11. 0=Falling edge. 1=Active high.
10	SciTrig10. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 10. 0=Active low. 1=Active high.
9	SciTrig9. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 9. 0=Active low. 1=Active high.
8	SciTrig8. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 8. 0=Active low. 1=Active high.
7	SciTrig7. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 7. 0=Active low. 1=Active high.
6	SciTrig6. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 6. 0=Active low. 1=Active high.
5	SciTrig5. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 5. 0=Active low. 1=Active high.
4	SciTrig4. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 4. 0=Active low. 1=Active high.
3	SciTrig3. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 3. 0=Active low. 1=Active high.
2	SciTrig2. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 2. 0=Active low. 1=Active high.
1	SciTrig1. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 1. 0=Active low. 1=Active high.
0	SciTrig0. Read-write. Reset: 1. The bit controls the way to set Event_Status bit 0. 0=Active low. 1=Active high.

SMIx0C SciLevl

Reset: 0000_0000h. This register specifies the trigger mode for each of the corresponding bit in [SMIx00 \[Event_Status\]](#).

Bits	Description
31	SciLevl31. Read-write. 0=Edge trigger. 1=Level trigger.
30	SciLevl30. Read-write. 0=Edge trigger. 1=Level trigger.
29	SciLevl29. Read-write. 0=Edge trigger. 1=Level trigger.
28	SciLevl28. Read-write. 0=Edge trigger. 1=Level trigger.
27	SciLevl27. Read-write. 0=Edge trigger. 1=Level trigger.
26	SciLevl26. Read-write. 0=Edge trigger. 1=Level trigger.
25	SciLevl25. Read-write. 0=Edge trigger. 1=Level trigger.
24	SciLevl24. Read-write. 0=Edge trigger. 1=Level trigger.
23	SciLevl23. Read-write. 0=Edge trigger. 1=Level trigger.
22	SciLevl22. Read-write. 0=Edge trigger. 1=Level trigger.
21	SciLevl21. Read-write. 0=Edge trigger. 1=Level trigger.
20	SciLevl20. Read-write. 0=Edge trigger. 1=Level trigger.
19	SciLevl19. Read-write. 0=Edge trigger. 1=Level trigger.
18	SciLevl18. Read-write. 0=Edge trigger. 1=Level trigger.
17	SciLevl17. Read-write. 0=Edge trigger. 1=Level trigger.
16	SciLevl16. Read-write. 0=Edge trigger. 1=Level trigger.
15	SciLevl15. Read-write. 0=Edge trigger. 1=Level trigger.
14	SciLevl14. Read-write. 0=Edge trigger. 1=Level trigger.
13	SciLevl13. Read-write. 0=Edge trigger. 1=Level trigger.
12	SciLevl12. Read-write. 0=Edge trigger. 1=Level trigger.
11	SciLevl11. Read-write. 0=Edge trigger. 1=Level trigger.
10	SciLevl10. Read-write. 0=Edge trigger. 1=Level trigger.
9	SciLevl9. Read-write. 0=Edge trigger. 1=Level trigger.
8	SciLevl8. Read-write. 0=Edge trigger. 1=Level trigger.
7	SciLevl7. Read-write. 0=Edge trigger. 1=Level trigger.
6	SciLevl6. Read-write. 0=Edge trigger. 1=Level trigger.
5	SciLevl5. Read-write. 0=Edge trigger. 1=Level trigger.
4	SciLevl4. Read-write. 0=Edge trigger. 1=Level trigger.
3	SciLevl3. Read-write. 0=Edge trigger. 1=Level trigger.
2	SciLevl2. Read-write. 0=Edge trigger. 1=Level trigger.
1	SciLevl1. Read-write. 0=Edge trigger. 1=Level trigger.
0	SciLevl0. Read-write. 0=Edge trigger. 1=Level trigger.

SMIx10 SmiSciStatus

Bits	Description
31:0	SmiSciStatus. Read; write-1-to-clear. Reset: 0. Each bit indicates the corresponding SmiSci status. The input of each bit is controlled by the corresponding SMIx08 [SciTrig] bit. Note: this function can be considered as a superset of SMIx00 [Event_Status] . When one of the bits is set and its SMIx14 [SmiSciEn] is also set, it triggers a SMI to call the BIOS. After the BIOS has serviced the SMM and cleared its status, the internal logic automatically sets the corresponding SMIx00 [Event_Status] bit and thereby triggering a SCI.

SMIx14 SmiSciEn

Bits	Description
31:0	SmiSciEn. Read-write; S3-check-exclude. Reset: 0. Each bit controls if SMI message is generated when the corresponding SMIx10 [SmiSciStatus] bit is set to 1. For each bit, 0=Not to send SMI message when the corresponding SMIx10 [SmiSciStatus] bit is set. 1=Send SMI message when the corresponding SMIx10 [SmiSciStatus] bit is set.

SMIx18 SwSciEn

Bits	Description
31:0	SwSciEn. Read-write. Reset: 0. This register is used as a software mechanism to trigger SCI. For each bit, 1=Software can write to SMIx1C [SwSciData] and set the corresponding SMIx00 [Event_Status] bit. Note: the setting of this bit needs to match with SMIx08 [SciTrig] and SMIx0C [SciLevl] in order to set the status bit.

SMIx1C SwSciData

Bits	Description
31:0	SwSciData. Read-write. Reset: 0. This is the software data path to set the corresponding SMIx00 [Event_Status] bit when SMIx18 [SwSciEn] is set.

SMIx20 SciSleepDisable

Bits	Description
31:0	SciSleepDisable. Read-write. Reset: 0. This register is used to ignore EVENT pins that are powered in the main power domain instead of auxiliary power domain. For each bit, 1=The corresponding SMIx00 [Event_Status] bit is masked off whenever the system goes to S3 or higher sleep state.

SMIx30 CapturedData

Bits	Description
31:0	CapturedData . Read-only. Reset: X. This is the buffer to capture write data for the last transaction that caused an SMI. Note: this buffer has no meaning for a read trap.

SMIx34 CapturedValid

Bits	Description										
7:4	Reserved.										
3:0	CapturedValid . Read-only. Reset: X. This is the byte valid buffer to signal which byte is captured for the last transaction that caused the SMI. <table> <thead> <tr> <th>Bit</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>[0]</td> <td>byte 0</td> </tr> <tr> <td>[1]</td> <td>byte 1</td> </tr> <tr> <td>[2]</td> <td>byte 2</td> </tr> <tr> <td>[3]</td> <td>byte 3</td> </tr> </tbody> </table>	Bit	Definition	[0]	byte 0	[1]	byte 1	[2]	byte 2	[3]	byte 3
Bit	Definition										
[0]	byte 0										
[1]	byte 1										
[2]	byte 2										
[3]	byte 3										

SMIx38 EPBIF_AER_Straps

Bits	Description
31:28	Reserved.
27	StrapBifInternalErrEnFch . Read-write. Reset: 0. Internal error enable.
26	StrapBifPoisonedAdvisoryNonfatalAFch . Read-write. Reset: 1. Poisoned TLP as advisory nonfatal.
25	StrapBifAcsDirectTranslatedP2pFch . Read-write. Reset: 1. ACS direct translated P2P enable.
24	StrapBifAcsUpstreamForwardingFch . Read-write. Reset: 1. ACS upstream forwarding enable.
23	StrapBifAcsP2pCompletionRedirectFch . Read-write. Reset: 1. ACS P2P completion redirect enable.
22	StrapBifAcsP2pRequestRedirectFch . Read-write. Reset: 1. ACS P2P request redirect enable.
21	StrapBifAcsTranslationBlockingFch . Read-write. Reset: 1. ACS translation blocking enable.
20	StrapBifAcsSourceValidationFch . Read-write. Reset: 1. ACS source validation enable.
19	StrapBifAcsEnFch . Read-write. Reset: 1. ACS enable.
18	StrapBifFirstRcvdErrLogFch . Read-write. Reset: 1. First received error log.
17	StrapBifEcrcCheckEnFch . Read-write. Reset: 1. ECRC check enable.
16	StrapBifEcrcGenEnFch . Read-write. Reset: 1. ECRC generate enable.
15	StrapBifCplAbortErrEnFch . Read-write. Reset: 1. Completer abort error enable.
14	StrapBifRxIgnoreVend0UrFch . Read-write. Reset: 1. Ignore Vendor 0 error.
13	StrapBifRxIgnoreTcErrFch . Read-write. Reset: 1. Ignore traffic class error.
12	StrapBifRxIgnoreMsgErrFch . Read-write. Reset: 1. Ignore message error.
11	StrapBifRxIgnoreMaxPayloadErrFch . Read-write. Reset: 1. Ignore maximum payload error.

10	StrapBifRxIgnoreLenMismatchErrFch. Read-write. Reset: 1. Ignore length mismatch error.
9	StrapBifRxIgnoreIoUrErrFch. Read-write. Reset: 1. Ignore IO UR error.
8	StrapBifRxIgnoreIoErrFch. Read-write. Reset: 1. Ignore IO error.
7	StrapBifRxIgnoreEpErrFch. Read-write. Reset: 1. Ignore poisoned TLP error.
6	StrapBifRxIgnoreCplErrFch. Read-write. Reset: 1. Ignore completion error.
5	StrapBifRxIgnoreCfgUrFch. Read-write. Reset: 1. Ignore configuration UR error.
4	StrapBifRxIgnoreCfgErrFch. Read-write. Reset: 1. Ignore configuration error.
3	StrapBifRxIgnoreBeErrFch. Read-write. Reset: 1. Ignore byte enable error.
2	StrapBifErrReportingDisFch. Read-write. Reset: 1. Error reporting disable.
1	StrapBifAerEnFch. Read-write. Reset: 1. AER enable.
0	StrapBifStickyOverrideS5. Read-write. Reset: 0. 1=Values in this register would override straps loaded from EEPROM.

SMIx3C DataErrorStatus

Bits	Description
31:8	Reserved.
7	SIrqIochk. Read; write-1-to-clear; S3-check-exclude. Reset: 0. Serial Iochk error.
6	SataPerr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. BIOS: See 2.15.3.9 . SATA controller internal parity error status.
5	UmiUncorrectableErr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. UMI uncorrectable error status.
4	UmiCorrectableErr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. UMI correctable error status.
3	AbUmiGppPerr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. AB/UMI/GPP parity error status.
2	ApuGppSerr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. APU/GPP devices SERR error status.
1	InternalPerr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. Internal devices PERR error status.
0	InternalSerr. Read; write-1-to-clear; S3-check-exclude. Reset: 0. Internal devices SERR error status.

SMIx40 SciMap0

Bits	Description
31:29	Reserved.
28:24	SciMap3. Read-write. Reset: 0. Specifies the mapping of GEVENT3 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap0.
23:21	Reserved.
20:16	SciMap2. Read-write. Reset: 0. Specifies the mapping of GEVENT2 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap0.
15:13	Reserved.

12:8	SciMap1. Read-write. Reset: 0. Specifies the mapping of GEVENT1 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap0.
7:5	Reserved.
4:0	SciMap0. Read-write. Reset: 0. Specifies the mapping of GEVENT0 to one of the 32 bits in SMIx00 [Event_Status] .
	<u>Bits</u> <u>Definition</u>
	00000b map to the input of SMIx00 [Event_Status] bit [0]
	00001b map to the input of SMIx00 [Event_Status] bit [1]
	...
	11111b map to the input of SMIx00 [Event_Status] bit [31]

SMIx44 SciMap1

Bits	Description
31:29	Reserved.
28:24	SciMap7. Read-write. Reset: 0. Specifies the mapping of GEVENT7 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap4.
23:21	Reserved.
20:16	SciMap6. Read-write. Reset: 0. Specifies the mapping of GEVENT6 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap4.
15:13	Reserved.
12:8	SciMap5. Read-write. Reset: 0. Specifies the mapping of GEVENT5 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap4.
7:5	Reserved.
4:0	SciMap4. Read-write. Reset: 0. Specifies the mapping of GEVENT4 to one of the 32 bits in SMIx00 [Event_Status] .
	<u>Bits</u> <u>Definition</u>
	00000b map to the input of SMIx00 [Event_Status] bit [0]
	00001b map to the input of SMIx00 [Event_Status] bit [1]
	...
	11111b map to the input of SMIx00 [Event_Status] bit [31]

SMIx48 SciMap2

Bits	Description
31:29	Reserved.
28:24	SciMap11. Read-write. Reset: 0. Specifies the mapping of GEVENT11 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap8.
23:21	Reserved.
20:16	SciMap10. Read-write. Reset: 0. Specifies the mapping of GEVENT10 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap8.
15:13	Reserved.
12:8	SciMap9. Read-write. Reset: 0. Specifies the mapping of GEVENT9 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap8.

7:5	Reserved.										
4:0	<p>SciMap8. Read-write. Reset: 0. Specifies the mapping of GEVENT8 to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx4C SciMap3

Bits	Description										
31:29	Reserved.										
28:24	SciMap15. Read-write. Reset: 0. Specifies the mapping of GEVENT15 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap12.										
23:21	Reserved.										
20:16	SciMap14. Read-write. Reset: 0. Specifies the mapping of GEVENT14 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap12.										
15:13	Reserved.										
12:8	SciMap13. Read-write. Reset: 0. Specifies the mapping of GEVENT13 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap12.										
7:5	Reserved.										
4:0	<p>SciMap12. Read-write. Reset: 0. Specifies the mapping of GEVENT12 to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx50 SciMap4

Bits	Description
31:29	Reserved.
28:24	SciMap19. Read-write. Reset: 0. Specifies the mapping of GEVENT19 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap16.
23:21	Reserved.
20:16	SciMap18. Read-write. Reset: 0. Specifies the mapping of GEVENT18 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap16.
15:13	Reserved.
12:8	SciMap17. Read-write. Reset: 0. Specifies the mapping of GEVENT17 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap16.

7:5	Reserved.										
4:0	<p>SciMap16. Read-write. Reset: 0. Specifies the mapping of GEVENT16 to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx54 SciMap5

Bits	Description										
31:29	Reserved.										
28:24	SciMap23 . Read-write. Reset: 0. Specifies the mapping of GEVENT23 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap20.										
23:21	Reserved.										
20:16	SciMap22 . Read-write. Reset: 0. Specifies the mapping of GEVENT22 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap20.										
15:13	Reserved.										
12:8	SciMap21 . Read-write. Reset: 0. Specifies the mapping of GEVENT21 to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap20.										
7:5	Reserved.										
4:0	<p>SciMap20. Read-write. Reset: 0. Specifies the mapping of GEVENT20 to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx58 SciMap6

Bits	Description
31:21	Reserved.
20:16	SciMap26 . Read-write. Reset: 0. Specifies the mapping of USB_PME (device 16h) to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap24.
15:13	Reserved.
12:8	SciMap25 . Read-write. Reset: 0. Specifies the mapping of USB_PME (device 13h) to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap24.

7:5	Reserved.										
4:0	<p>SciMap24. Read-write. Reset: 0. Specifies the mapping of USB_PME (device 12h) to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx5C SciMap7

Bits	Description
31:0	Reserved.

SMIx60 SciMap8

Bits	Description
31:0	Reserved.

SMIx64 SciMap9

Bits	Description										
31:21	Reserved.										
20:16	SciMap38. Read-write. Reset: 0. Specifies the mapping of SATA1_PME to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap36.										
15:13	Reserved.										
12:8	SciMap37. Read-write. Reset: 0. Specifies the mapping of SATA0_PME to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap36.										
7:5	Reserved.										
4:0	<p>SciMap36. Read-write. Reset: 0. Specifies the mapping of HD_Audio_PME to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx68 SciMap10

Bits	Description
31:29	Reserved.
28:24	SciMap43. Read-write. Reset: 0. Specifies the mapping of WAKE# pin to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap40.

23:21	Reserved.
20:16	SciMap42 . Read-write. Reset: 0. Specifies the mapping of CIR_PME to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap40.
15:13	Reserved.
12:8	SciMap41 . Read-write. Reset: 0. Specifies the mapping of EC1_PME to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap40.
7:5	Reserved.
4:0	SciMap40 . Read-write. Reset: 0. Specifies the mapping of EC0_PME to one of the 32 bits in SMIx00 [Event_Status] .
	<u>Bits</u> <u>Definition</u>
	00000b map to the input of SMIx00 [Event_Status] bit [0]
	00001b map to the input of SMIx00 [Event_Status] bit [1]
	...
	11111b map to the input of SMIx00 [Event_Status] bit [31]

SMIx6C SciMap11

Bits	Description
31:29	Reserved.
28:24	SciMap47 . Read-write. Reset: 0. Specifies the mapping of SMBUS0 Interrupt event to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap44.
23:21	Reserved.
20:16	SciMap46 . Read-write. Reset: 0. Specifies the mapping of ASF slave interrupt event to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap44.
15:13	Reserved.
12:8	SciMap45 . Read-write. Reset: 0. Specifies the mapping of ASF master interrupt event to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap44.
7:5	Reserved.
4:0	SciMap44 . Read-write. Reset: 0. Specifies the mapping of internal FAN/THERMAL event to one of the 32 bits in SMIx00 [Event_Status] .
	<u>Bits</u> <u>Definition</u>
	00000b map to the input of SMIx00 [Event_Status] bit [0]
	00001b map to the input of SMIx00 [Event_Status] bit [1]
	...
	11111b map to the input of SMIx00 [Event_Status] bit [31]

SMIx70 SciMap12

Bits	Description
31:29	Reserved.
28:24	SciMap51 . Read-write. Reset: 0. Specifies the mapping of PWRBTN status to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap48.
23:21	Reserved.

20:16	SciMap50. Read-write. Reset: 0. Specifies the mapping of LLB# to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap48.										
15:13	Reserved.										
12:8	SciMap49. Read-write. Reset: 0. Specifies the mapping of internal traffic monitor to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap48.										
7:5	Reserved.										
4:0	SciMap48. Read-write. Reset: 0. Specifies the mapping of TWARN pin to one of the 32 bits in SMIx00 [Event_Status] . <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx74 SciMap13

Bits	Description										
31:29	Reserved.										
28:24	SciMap55. Read-write. Reset: 0. Specifies the mapping of RAS_event status to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap52.										
23:21	Reserved.										
20:16	SciMap54. Read-write. Reset: 0. Specifies the mapping of SCI assertion message from APU to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap52.										
15:13	Reserved.										
12:8	SciMap53. Read-write. Reset: 0. Specifies the mapping of HW assertion message from APU to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap52.										
7:5	Reserved.										
4:0	SciMap52. Read-write. Reset: 0. Specifies the mapping of PROHOT# pin to one of the 32 bits in SMIx00 [Event_Status] . <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx78 SciMap14

Bits	Description
31:29	Reserved.
23:21	Reserved.
20:16	SciMap58. Read-write. Reset: 0. Specifies the mapping of AcDcTimerEvent to one of the 32 bits in SMIx00 [Event_Status] . See: SciMap56.

15:5	Reserved.										
4:0	<p>SciMap56. Read-write. Reset: 0. Specifies the mapping of XHC0 (USB3 controller 0) pin to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx7C SciMap15

Bits	Description										
31:29	Reserved.										
28:24	<p>SciMap63. Read-write. Reset: 0. Specifies the mapping of TempStatus5 (auto-polling temperature) to one of the 32 bits in SMIx00 [Event_Status].</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00000b</td> <td>map to the input of SMIx00 [Event_Status] bit [0]</td> </tr> <tr> <td>00001b</td> <td>map to the input of SMIx00 [Event_Status] bit [1]</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>11111b</td> <td>map to the input of SMIx00 [Event_Status] bit [31]</td> </tr> </tbody> </table>	Bits	Definition	00000b	map to the input of SMIx00 [Event_Status] bit [0]	00001b	map to the input of SMIx00 [Event_Status] bit [1]	11111b	map to the input of SMIx00 [Event_Status] bit [31]
Bits	Definition										
00000b	map to the input of SMIx00 [Event_Status] bit [0]										
00001b	map to the input of SMIx00 [Event_Status] bit [1]										
...	...										
11111b	map to the input of SMIx00 [Event_Status] bit [31]										

SMIx80 SmiStatus0

Bits	Description
31:27	Reserved.
26	UsbWakeup2Event26 . Read; write-1-to-clear. Reset: 0. Status of USB device 16h PME.
25	UsbWakeup1Event25 . Read; write-1-to-clear. Reset: 0. Status of USB device 13h PME.
24	UsbWakeup0Event24 . Read; write-1-to-clear. Reset: 0. Status of USB device 12h PME.
23	Gevent23StatusEvent23 . Read; write-1-to-clear. Reset: 0. Status of Gevent23.
22	Gevent22StatusEvent22 . Read; write-1-to-clear. Reset: 0. Status of Gevent22.
21	Gevent21StatusEvent21 . Read; write-1-to-clear. Reset: 0. Status of Gevent21.
20	Gevent20StatusEvent20 . Read; write-1-to-clear. Reset: 0. Status of Gevent20.
19	Gevent19StatusEvent19 . Read; write-1-to-clear. Reset: 0. Status of Gevent19.
18	Gevent18StatusEvent18 . Read; write-1-to-clear. Reset: 0. Status of Gevent18.
17	Gevent17StatusEvent17 . Read; write-1-to-clear. Reset: 0. Status of Gevent17.
16	Gevent16StatusEvent16 . Read; write-1-to-clear. Reset: 0. Status of Gevent16.
15	Gevent15StatusEvent15 . Read; write-1-to-clear. Reset: 0. Status of Gevent15.
14	Gevent14StatusEvent14 . Read; write-1-to-clear. Reset: 0. Status of Gevent14.
13	Gevent13StatusEvent13 . Read; write-1-to-clear. Reset: 0. Status of Gevent13.
12	Gevent12StatusEvent12 . Read; write-1-to-clear. Reset: 0. Status of Gevent12.
11	Gevent11StatusEvent11 . Read; write-1-to-clear. Reset: 0. Status of Gevent11.
10	Gevent10StatusEvent10 . Read; write-1-to-clear. Reset: 0. Status of Gevent10.

9	Gevent9StatusEvent9 . Read; write-1-to-clear. Reset: 0. Status of Gevent9.
8	Gevent8StatusEvent8 . Read; write-1-to-clear. Reset: 0. Status of Gevent8.
7	Gevent7StatusEvent7 . Read; write-1-to-clear. Reset: 0. Status of Gevent7.
6	Gevent6StatusEvent6 . Read; write-1-to-clear. Reset: 0. Status of Gevent6.
5	Gevent5StatusEvent5 . Read; write-1-to-clear. Reset: 0. Status of Gevent5.
4	Gevent4StatusEvent4 . Read; write-1-to-clear. Reset: 0. Status of Gevent4.
3	Gevent3StatusEvent3 . Read; write-1-to-clear. Reset: 0. Status of Gevent3.
2	Gevent2StatusEvent2 . Read; write-1-to-clear. Reset: 0. Status of Gevent2.
1	Gevent1StatusEvent1 . Read; write-1-to-clear. Reset: 0. Status of Gevent1.
0	Gevent0StatusEvent0 . Read; write-1-to-clear. Reset: 0. Status of Gevent0.

SMIx84 SmiStatus1

Bits	Description
31	TempTsiStsEvent63 . Read; write-1-to-clear. Reset: 0. Status of TempTsi event.
26	AcDcTimerEventEvent58 . Read; write-1-to-clear. Reset: 0. Status of AcDcTimer wake up event.
25	Reserved.
24	Xhc0PmeEvent56 . Read; write-1-to-clear. Reset: 0. Status of XHC0 (device 10h, function 0) PME.
23	RasEvent55 . Read; write-1-to-clear. Reset: 0. BIOS: See 2.15.3.9 . Internal devices SERR error status.
22	ApuSciAssertionEvent54 . Read; write-1-to-clear. Reset: 0. Status of NB SCI request.
21	ApuHwAssertionEvent53 . Read; write-1-to-clear. Reset: 0. Status of APU HW assertion.
20	ProcHotEvent52 . Read; write-1-to-clear. Reset: 0. Status of ProcHot event.
19	PwrButtonEvent51 . Read; write-1-to-clear. Reset: 0. Status of PwrButton (rising edge).
18	IllbEvent50 . Read; write-1-to-clear. Reset: 0. Status of iLLB# assertion.
17	TrafficMonitorIntrEvent49 . Read; write-1-to-clear. Reset: 0. Status of FCH Traffic Monitor Interrupt.
16	TwarnEvent48 . Read; write-1-to-clear. Reset: 0. Status of FCH TWARN.
15	Smbus0Event47 . Read; write-1-to-clear. Reset: 0. Status of FCH SMBUS0 master interrupt.
14	AsfSlaveIntrEvent46 . Read; write-1-to-clear. Reset: 0. Status of FCH ASF slave interrupt.
13	AsfMasterIntrEvent45 . Read; write-1-to-clear. Reset: 0. Status of FCH ASF master interrupt.
12	FanThermalGeventEvent44 . Read; write-1-to-clear. Reset: 0. Status of FCH fan thermal.
11	AltMmTimerStsEvent43 . Read; write-1-to-clear. Reset: 0. Status of AltHpetTimer Alarm.
10	CirPmeEvent42 . Read; write-1-to-clear. Reset: 0. Status of FCH CIR PME.
9	EcGevent1Event41 . Read; write-1-to-clear. Reset: 0. Status of FCH IMC Gevent1.
8	EcGevent0Event40 . Read; write-1-to-clear. Reset: 0. Status of FCH IMC Gevent0.
7	Reserved.
6	SataGevent1Event38 . Read; write-1-to-clear. Reset: 0. Status of FCH SATA Gevent1.
5	SataGevent0Event37 . Read; write-1-to-clear. Reset: 0. Status of FCH SATA Gevent0.

4	AzaliaPmeEvent36 . Read; write-1-to-clear. Reset: 0. Status of FCH HD Audio PME.
3:0	Reserved.

SMIx88 SmiStatus2

Bits	Description
31	CmosEraseStsEvent95 . Read; write-1-to-clear. Reset: 0. Status of Cmos Erase event.
30	Reserved.
29	AzFlrEvent93 . Read; write-1-to-clear. Reset: 0. Status of Azalia FLR event.
28	SataFlrEvent92 . Read; write-1-to-clear. Reset: 0. Status of SATA FLR event.
27	UsbFlrEvent91 . Read; write-1-to-clear. Reset: 0. Status of USB FLR event.
26	Emulate64Event90 . Read; write-1-to-clear. Reset: 0. Status of Emulation IO Port 60h/64h.
25	ThermaltripEvent89 . Read; write-1-to-clear. Reset: 0. Status of ThermalTrip event.
24:22	Reserved.
21	Reserved.
20	PciSerrEvent84 . Read; write-1-to-clear. Reset: 0. Status of Serr assertion on PCI bus.
19	ProtHotEvent83 . Read; write-1-to-clear. Reset: 0. Status of ProtHot event.
18	VbatLowEvent82 . Read; write-1-to-clear. Reset: 0. Status of VBAT low.
17	Reserved.
16	XhcErrEvent80 . Read; write-1-to-clear. Reset: 0. Status of XHC error.
15	EcSmi0Event79 . Read; write-1-to-clear. Reset: 0. Status of IMC SMI request.
14	Smbus0IntrEvent78 . Read; write-1-to-clear. Reset: 0. Status of SMBUS0 interrupt request.
13	SerialIrqSmiEvent77 . Read; write-1-to-clear. Reset: 0. Status of SMI request from Serial IRQ.
12	UsbSmiEvent76 . Read; write-1-to-clear. Reset: 0. Status of USB SMI request.
11	SmiCmdportEvent75 . Read; write-1-to-clear. Reset: 0. Status of Writing SMI Command Port.
10	PwrbtnEvent74 . Read; write-1-to-clear. Reset: 0. Status of Power Button being pressed.
9	BiosRlsEvent73 . Read; write-1-to-clear. Reset: 0. Status of BIOS_RLS. See PMx74[BiosRls] .
8	GblRlsEvent72 . Read; write-1-to-clear. Reset: 0. Status of GBL event. See Acpipm1CntBlkx00[GblRls] .
7	AcpitimerEvent71 . Read; write-1-to-clear. Reset: 0. Status of ACPI timer rollover interrupt.
6	RtcIrqEvent70 . Read; write-1-to-clear. Reset: 0. Status of RTC IRQ.
5	ApuGpphpEvent69 . Read; write-1-to-clear. Reset: 0. Status of APU HP message.
4	ApuGpppmeEvent68 . Read; write-1-to-clear. Reset: 0. Status of APU GPP PME message.
3	SataAhciSmiEvent67 . Read; write-1-to-clear. Reset: 0. Status of SATA AHCI SMI request.
2	Reserved.
1	SlpTypeEvent65 . Read; write-1-to-clear. Reset: 0. Status of writing Acpipm1CntBlkx00[SlpTyp] .
0	KbRstEvent64 . Read; write-1-to-clear. Reset: 0. Status of KeyBoard Reset event.

SMIx8C SmiStatus3

Bits	Description
31:24	Reserved.
23	Irq23TrappingEvent119 . Read; write-1-to-clear. Reset: 0. Status of IRQ23 request.
22	Irq22TrappingEvent118 . Read; write-1-to-clear. Reset: 0. Status of IRQ22 request.
21	Irq21TrappingEvent117 . Read; write-1-to-clear. Reset: 0. Status of IRQ21 request.
20	Irq20TrappingEvent116 . Read; write-1-to-clear. Reset: 0. Status of IRQ20 request.
19	Irq19TrappingEvent115 . Read; write-1-to-clear. Reset: 0. Status of IRQ19 request.
18	Irq18TrappingEvent114 . Read; write-1-to-clear. Reset: 0. Status of IRQ18 request.
17	Irq17TrappingEvent113 . Read; write-1-to-clear. Reset: 0. Status of IRQ17 request.
16	Irq16TrappingEvent112 . Read; write-1-to-clear. Reset: 0. Status of IRQ16 request.
15	Irq15TrappingEvent111 . Read; write-1-to-clear. Reset: 0. Status of IRQ15 request.
14	Irq14TrappingEvent110 . Read; write-1-to-clear. Reset: 0. Status of IRQ14 request.
13	Irq13TrappingEvent109 . Read; write-1-to-clear. Reset: 0. Status of IRQ13 request.
12	Irq12TrappingEvent108 . Read; write-1-to-clear. Reset: 0. Status of IRQ12 request.
11	Irq11TrappingEvent107 . Read; write-1-to-clear. Reset: 0. Status of IRQ11 request.
10	Irq10TrappingEvent106 . Read; write-1-to-clear. Reset: 0. Status of IRQ10 request.
9	Irq9TrappingEvent105 . Read; write-1-to-clear. Reset: 0. Status of IRQ9 request.
8	Irq8TrappingEvent104 . Read; write-1-to-clear. Reset: 0. Status of IRQ8 request.
7	Irq7TrappingEvent103 . Read; write-1-to-clear. Reset: 0. Status of IRQ7 request.
6	Irq6TrappingEvent102 . Read; write-1-to-clear. Reset: 0. Status of IRQ6 request.
5	Irq5TrappingEvent101 . Read; write-1-to-clear. Reset: 0. Status of IRQ5 request.
4	Irq4TrappingEvent100 . Read; write-1-to-clear. Reset: 0. Status of IRQ4 request.
3	Irq3TrappingEvent99 . Read; write-1-to-clear. Reset: 0. Status of IRQ3 request.
2	Irq2TrappingEvent98 . Read; write-1-to-clear. Reset: 0. Status of IRQ2 request.
1	Irq1TrappingEvent97 . Read; write-1-to-clear. Reset: 0. Status of IRQ1 request.
0	Irq0TrappingEvent96 . Read; write-1-to-clear. Reset: 0. Status of IRQ0 request.

SMIx90 SmiStatus4

Bits	Description
31	CfgTrapping3Event159 . Read; write-1-to-clear. Reset: 0. Status of PCI configuration cycle Trapping3 SMI request.
30	CfgTrapping2Event158 . Read; write-1-to-clear. Reset: 0. Status of PCI configuration cycle Trapping2 SMI request.
29	CfgTrapping1Event157 . Read; write-1-to-clear. Reset: 0. Status of PCI configuration cycle Trapping1 SMI request.
28	CfgTrapping0Event156 . Read; write-1-to-clear. Reset: 0. Status of PCI configuration cycle Trapping0 SMI request.

27	MemTrapping3Event155. Read; write-1-to-clear. Reset: 0. Status of memory Trapping3 SMI request.
26	MemTrapping2Event154. Read; write-1-to-clear. Reset: 0. Status of memory Trapping2 SMI request.
25	MemTrapping1Event153. Read; write-1-to-clear. Reset: 0. Status of memory Trapping1 SMI request.
24	MemTrapping0Event152. Read; write-1-to-clear. Reset: 0. Status of memory Trapping0 SMI request.
23	IoTrapping3Event151. Read; write-1-to-clear. Reset: 0. Status of IO Trapping3 SMI request.
22	IoTrapping2Event150. Read; write-1-to-clear. Reset: 0. Status of IO Trapping2 SMI request.
21	IoTrapping1Event149. Read; write-1-to-clear. Reset: 0. Status of IO Trapping1 SMI request.
20	IoTrapping0Event148. Read; write-1-to-clear. Reset: 0. Status of IO Trapping0 SMI request.
19	PstateChangeEvent147. Read; write-1-to-clear. Reset: 0. Status of P state request.
18	PstateChangeEvent146. Read; write-1-to-clear. Reset: 0. Status of P state request.
17	SoftResetEvent145. Read; write-1-to-clear. Reset: 0. Status of soft reset request. The soft request can be: <ul style="list-style-type: none"> • CF9h PCI reset. • ASF remote reset. • sync flood reset. • KBRST. • watchdog timer reset.
16	AbSmiTrapEvent144. Read; write-1-to-clear. Reset: 0. Status of AB SMI trapping request.
15	LongTimerEvent143. Read; write-1-to-clear. Reset: 0. Status of Long Timer SMI request.
14	ShortTimerEvent142. Read; write-1-to-clear. Reset: 0. Status of Short Timer SMI request.
13	CStateMsgEvent141. Read; write-1-to-clear. Reset: 0. Status of C State Change message request.
12	Fake2StsEvent140. Read; write-1-to-clear. Reset: 0. Status of Fake2.
11	Fake1StsEvent139. Read; write-1-to-clear. Reset: 0. Status of Fake1.
10	Fake0StsEvent138. Read; write-1-to-clear. Reset: 0. Status of Fake0.
9:6	Reserved.
5	Fanin0stsEvent133. Read; write-1-to-clear. Reset: 0. Status of FanIn0 event.
4:0	Reserved.

SMIx94 SmiPointer

This register is meant as a faster mechanism to locate the SMI source. BIOS can examine this register to find out the SMI source instead of reading [SMIx80 \[SmiStatus0\]](#) through [SMIx90 \[SmiStatus4\]](#) individually.

Bits	Description
15:6	Reserved.
5	SmiStatusSource4. Read-only. Reset: 0. Indicates whether the SMI source is from SMIx90 [SmiStatus4] if the corresponding SMI enable is selected.
4	SmiStatusSource3. Read-only. Reset: 0. Indicates whether the SMI source is from SMIx8C [SmiStatus3] if the corresponding SMI enable is selected.

3	SmiStatusSource2 . Read-only. Reset: 0. Indicates whether the SMI source is from SMIx88 [SmiStatus2] if the corresponding SMI enable is selected.
2	SmiStatusSource1 . Read-only. Reset: 0. Indicates whether the SMI source is from SMIx84 [SmiStatus1] if the corresponding SMI enable is selected.
1	SmiStatusSource0 . Read-only. Reset: 0. Indicates whether the SMI source is from SMIx80 [SmiStatus0] if the corresponding SMI enable is selected.
0	SmiSciSource . Read-only. Reset: 0. Indicates whether the SMI source is from SMIx10 [SmiSciStatus] .

SMIx96 SmiTimer

There are two SMI timers: the short timer runs at 1 us unit time and the long timer runs at 1 ms unit time. This register is actually made up of two sets of registers depending on the setting of [SMIx98\[SmiTimerSel\]](#). If [SMIx98\[SmiTimerSel\]==0](#), then [SMIx96](#) is for the short timer. If [SMIx98\[SmiTimerSel\]==1](#), then [SMIx96](#) is for the long timer. The default setting selects this register as “SmiShortTimer”; software needs to set the “SmiTimerSel=1” to select this register as “SmiLongTimer”.

Bits	Description
15	TimerEn . Read-write. Reset: 0. 1=Enable the SMI short Timer or long timer, which is selected by SMIx98[SmiTimerSel] . 0=Disable.
14:0	SmiTimerCount . Read-write. Reset: 0. Actual timer duration = TimerTime + 1 unit.

SMIx98 SmiTrig0

Bit [23:0] defines the trigger mode for 24 GEVENTS in [SMIx80\[23:0\]](#). Note these are different from [SMIx08 \[SciTrig\]](#).

Bits	Description
31	SmiEnB . Read-write. Reset: 1. 0=Enable SMI function. 1=Disable.
30	Reserved.
29	SmiTimerSel . Read-write. Reset: 0. 0=Select SMIx96 [SmiTimer] to be SmiShortTimer register. 1=Select SMIx96 [SmiTimer] to be SmiLongTimer register.
28	Eos . Read-write. Reset: 1. 1=Allow SMI to be sent out to CPU. 0=SMI is blocked.
27	FakeSts2 . Read-write. Reset: 1. Program the value to emulate an SMI input event.
26	FakeSts1 . Read-write. Reset: 1. Program the value to emulate an SMI input event.
25	FakeSts0 . Read-write. Reset: 1. Program the value to emulate an SMI input event.
24	TrappingIrqOnPic . Read-write. Reset: 1. 0=SMI is generated when trapping IRQ0-15 of IOAPIC. 1=SMI is generated when trapping IRQ0-15 of PIC.
23	SmiTrig23 . Read-write. Reset: 1. 0=Active low. 1=Active high.
22	SmiTrig22 . Read-write. Reset: 1. 0=Active low. 1=Active high.
21	SmiTrig21 . Read-write. Reset: 1. 0=Active low. 1=Active high.
20	SmiTrig20 . Read-write. Reset: 1. 0=Active low. 1=Active high.
19	SmiTrig19 . Read-write. Reset: 1. 0=Active low. 1=Active high.
18	SmiTrig18 . Read-write. Reset: 1. 0=Active low. 1=Active high.

17	SmiTrig17 . Read-write. Reset: 1. 0=Active low. 1=Active high.
16	SmiTrig16 . Read-write. Reset: 1. 0=Active low. 1=Active high.
15	SmiTrig15 . Read-write. Reset: 1. 0=Active low. 1=Active high.
14	SmiTrig14 . Read-write. Reset: 1. 0=Active low. 1=Active high.
13	SmiTrig13 . Read-write. Reset: 1. 0=Active low. 1=Active high.
12	SmiTrig12 . Read-write. Reset: 1. 0=Active low. 1=Active high.
11	SmiTrig11 . Read-write. Reset: 1. 0=Active low. 1=Active high.
10	SmiTrig10 . Read-write. Reset: 1. 0=Active low. 1=Active high.
9	SmiTrig9 . Read-write. Reset: 1. 0=Active low. 1=Active high.
8	SmiTrig8 . Read-write. Reset: 1. 0=Active low. 1=Active high.
7	SmiTrig7 . Read-write. Reset: 1. 0=Active low. 1=Active high.
6	SmiTrig6 . Read-write. Reset: 1. 0=Active low. 1=Active high.
5	SmiTrig5 . Read-write. Reset: 1. 0=Active low. 1=Active high.
4	SmiTrig4 . Read-write. Reset: 1. 0=Active low. 1=Active high.
3	SmiTrig3 . Read-write. Reset: 1. 0=Active low. 1=Active high.
2	SmiTrig2 . Read-write. Reset: 1. 0=Active low. 1=Active high.
1	SmiTrig1 . Read-write. Reset: 1. 0=Active low. 1=Active high.
0	SmiTrig0 . Read-write. Reset: 1. 0=Active low. 1=Active high.

SMIx9C SmiTrig1

Bit [23:0] defines the trigger mode for 24 IRQs.

Bits	Description
31:24	Reserved. Read-write.
23	SmiIrq23Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
22	SmiIrq22Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
21	SmiIrq21Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
20	SmiIrq20Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
19	SmiIrq19Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
18	SmiIrq18Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
17	SmiIrq17Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
16	SmiIrq16Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
15	SmiIrq15Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
14	SmiIrq14Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
13	SmiIrq13Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
12	SmiIrq12Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
11	SmiIrq11Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
10	SmiIrq10Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
9	SmiIrq9Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.

8	SmiIrq8Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
7	SmiIrq7Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
6	SmiIrq6Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
5	SmiIrq5Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
4	SmiIrq4Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
3	SmiIrq3Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
2	SmiIrq2Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
1	SmiIrq1Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.
0	SmiIrq0Trig . Read-write. Reset: 0. 0=Active low. 1=Active high.

SMIxA0 SmiControl0

This register specifies the control mechanism for SMI sources in [SMIx80\[15:0\]](#).

Bits	Description										
31:30	Smicontrol15 . Read-write. Reset: 0. Control for GEVENT15. See: Smicontrol0.										
29:28	Smicontrol14 . Read-write. Reset: 0. Control for GEVENT14. See: Smicontrol0.										
27:26	Smicontrol13 . Read-write. Reset: 0. Control for GEVENT13. See: Smicontrol0.										
25:24	Smicontrol12 . Read-write. Reset: 0. Control for GEVENT12. See: Smicontrol0.										
23:22	Smicontrol11 . Read-write. Reset: 0. Control for GEVENT11. See: Smicontrol0.										
21:20	Smicontrol10 . Read-write. Reset: 0. Control for GEVENT10. See: Smicontrol0.										
19:18	Smicontrol9 . Read-write. Reset: 0. Control for GEVENT9. See: Smicontrol0.										
17:16	Smicontrol8 . Read-write. Reset: 0. Control for GEVENT8. See: Smicontrol0.										
15:14	Smicontrol7 . Read-write. Reset: 0. Control for GEVENT7. See: Smicontrol0.										
13:12	Smicontrol6 . Read-write. Reset: 0. Control for GEVENT6. See: Smicontrol0.										
11:10	Smicontrol5 . Read-write. Reset: 0. Control for GEVENT5. See: Smicontrol0.										
9:8	Smicontrol4 . Read-write. Reset: 0. Control for GEVENT4. See: Smicontrol0.										
7:6	Smicontrol3 . Read-write. Reset: 0. Control for GEVENT3. See: Smicontrol0.										
5:4	Smicontrol2 . Read-write. Reset: 0. Control for GEVENT2. See: Smicontrol0.										
3:2	Smicontrol1 . Read-write. Reset: 0. Control for GEVENT1. See: Smicontrol0.										
1:0	Smicontrol0 . Read-write. Reset: 0. Control for GEVENT0. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr><td>00b</td><td>Disable</td></tr> <tr><td>01b</td><td>SMI</td></tr> <tr><td>10b</td><td>NMI</td></tr> <tr><td>11b</td><td>IRQ13</td></tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxA4 SmiControl1

This register specifies the control mechanism for SMI sources in [SMIx80\[31:16\]](#).

Bits	Description
31:22	Reserved.

21:20	Smicontrol26 . Read-write. Reset: 0. Control for USB_PME (Device 14h). See: Smicontrol16.										
19:18	Smicontrol25 . Read-write. Reset: 0. Control for USB_PME (Device 13h). See: Smicontrol16.										
17:16	Smicontrol24 . Read-write. Reset: 0. Control for USB_PME (Device 12h). See: Smicontrol16.										
15:14	Smicontrol23 . Read-write. Reset: 0. Control for GEVENT23. See: Smicontrol16.										
13:12	Smicontrol22 . Read-write. Reset: 0. Control for GEVENT22. See: Smicontrol16.										
11:10	Smicontrol21 . Read-write. Reset: 0. Control for GEVENT21. See: Smicontrol16.										
9:8	Smicontrol20 . Read-write. Reset: 0. Control for GEVENT20. See: Smicontrol16.										
7:6	Smicontrol19 . Read-write. Reset: 0. Control for GEVENT19. See: Smicontrol16.										
5:4	Smicontrol18 . Read-write. Reset: 0. Control for GEVENT18. See: Smicontrol16.										
3:2	Smicontrol17 . Read-write. Reset: 0. Control for GEVENT17. See: Smicontrol16.										
1:0	Smicontrol16 . Read-write. Reset: 0. Control for GEVENT16. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxA8 SmiControl2

This register specifies the control mechanism for SMI sources in [SMIx84\[15:0\]](#).

Bits	Description										
31:30	Smicontrol47 . Read-write. Reset: 0. Control for SMBUS0 interrupt. See: Smicontrol36.										
29:28	Smicontrol46 . Read-write. Reset: 0. Control for ASF Slave interrupt. See: Smicontrol36.										
27:26	Smicontrol45 . Read-write. Reset: 0. Control for ASF Master interrupt. See: Smicontrol36.										
25:24	Smicontrol44 . Read-write. Reset: 0. Control for fan thermal GEvent. See: Smicontrol36.										
23:22	Reserved.										
21:20	Smicontrol42 . Read-write. Reset: 0. Control for CIR PME. See: Smicontrol36.										
19:18	Reserved.										
17:16	Smicontrol40 . Read-write. Reset: 0. Control for IMC Gevent0. See: Smicontrol36.										
15:14	Reserved.										
13:12	Smicontrol38 . Read-write. Reset: 0. Control for SATA Gevent1. See: Smicontrol36.										
11:10	Smicontrol37 . Read-write. Reset: 0. Control for SATA Gevent0. See: Smicontrol36.										
9:8	Smicontrol36 . Read-write. Reset: 0. Control for PME from HD Audio. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										
7:4	Reserved.										
3:0	Reserved.										

SMIxAC SmiControl3

This register specifies the control mechanism for SMI sources in [SMIx84\[31:16\]](#).

Bits	Description										
31:30	Smicontrol63. Read-write. Reset: 0. Control for TempTsi event. See: Smicontrol48.										
21:20	Smicontrol58. Read-write. Reset: 0. Control for AcDcTimer wake up event (Wake Device in ACPI4.0). See: Smicontrol48.										
19:18	Reserved.										
17:16	Smicontrol56. Read-write. Reset: 0. Control for XHC0 (device 10h, function 0) PME. See: Smicontrol48.										
15:14	Smicontrol55. Read-write. Reset: 0. Control for internal devices SERR error status. See: Smicontrol48.										
13:12	Smicontrol54. Read-write. Reset: 0. Control for APU SCI request. See: Smicontrol48.										
11:10	Smicontrol53. Read-write. Reset: 0. Control for APU HW assertion. See: Smicontrol48.										
9:8	Smicontrol52. Read-write. Reset: 0. Control for ProcHot event. See: Smicontrol48.										
7:6	Smicontrol51. Read-write. Reset: 0. Control for Power button event. See: Smicontrol48.										
5:4	Smicontrol50. Read-write. Reset: 0. Control for iLLB#. See: Smicontrol48.										
3:2	Smicontrol49. Read-write. Reset: 0. Control for internal Traffic monitor interrupt. See: Smicontrol48.										
1:0	Smicontrol48. Read-write. Reset: 0. Control for TWARN#. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxB0 SmiControl4

This register specifies the control mechanism for SMI sources in [SMIx88\[15:0\]](#).

Bits	Description
31:30	Smicontrol79. Read-write. Reset: 0. Control for IMC SMI request0. See: Smicontrol65.
29:28	Smicontrol78. Read-write. Reset: 0. Control for SMBUS0 interrupt. See: Smicontrol65.
27:26	Smicontrol77. Read-write. Reset: 0. Control for SMI request form serial IRQ. See: Smicontrol65.
25:24	Smicontrol76. Read-write. Reset: 0. Control for USB SMI request. See: Smicontrol65.
23:22	Smicontrol75. Read-write. Reset: 0. Control for writing SMI command port at SmiCmdBlkx00 . See: Smicontrol65.
21:20	Smicontrol74. Read-write. Reset: 0. Control for power button being pressed. See: Smicontrol65.
19:18	Smicontrol73. Read-write. Reset: 0. Control for writing PMx74[BiosRls] . See: Smicontrol65.
17:16	Smicontrol72. Read-write. Reset: 0. Control for writing AcpiPm1CntBlkx00[GblRls] . See: Smicontrol65.
15:14	Smicontrol71. Read-write. Reset: 0. Control for PM timer rollover. See: Smicontrol65.
13:12	Smicontrol70. Read-write. Reset: 0. Control for RTC IRQ. See: Smicontrol65.

11:10	Smicontrol69. Read-write. Reset: 0. Control for APU GPP hot plug. See: Smicontrol65.										
9:8	Smicontrol68. Read-write. Reset: 0. Control for APU GPP PME. See: Smicontrol65.										
7:6	Smicontrol67. Read-write. Reset: 0. Control for SATA AHCI event. See: Smicontrol65.										
5:4	Reserved.										
3:2	Smicontrol65. Read-write. Reset: 0. Control for writing AcpiPm1CntBlkx00[SlpTyp] to put the system in S state. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										
1:0	Reserved. Read-write.										

SMIxB4 SmiControl5

This register specifies the control mechanism for SMI sources in [SMIx88\[31:16\]](#).

Bits	Description										
31:30	Smicontrol95. Read-write. Reset: 0. Control for Cmos Erase. See: Smicontrol80.										
29:28	Reserved.										
27:26	Smicontrol93. Read-write. Reset: 0. Control for HD audio FLR. See: Smicontrol80.										
25:24	Smicontrol92. Read-write. Reset: 0. Control for SATA FLR. See: Smicontrol80.										
23:22	Smicontrol91. Read-write. Reset: 0. Control for USB FLR. See: Smicontrol80.										
21:20	Smicontrol90. Read-write. Reset: 0. Control for Emulation64. See: Smicontrol80.										
19:18	Smicontrol89. Read-write. Reset: 0. Control for ThermalTrip# assertion. See: Smicontrol80.										
17:12	Reserved.										
11:10	Reserved.										
9:8	Smicontrol84. Read-write. Reset: 0. Control for SERR#. See: Smicontrol80.										
7:6	Smicontrol83. Read-write. Reset: 0. Control for ProcHot. See: Smicontrol80.										
5:4	Smicontrol82. Read-write. Reset: 0. Control for VBAT low. See: Smicontrol80.										
3:2	Reserved.										
1:0	Smicontrol80. Read-write. Reset: 0. Control for IMC SMI request1. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxB8 SmiControl6

This register specifies the control mechanism for SMI sources in [SMIx8C\[15:0\]](#).

Bits	Description
31:30	Smicontrol111. Read-write. Reset: 0. Control for IRQ15. See: Smicontrol96.

29:28	Smicontrol110. Read-write. Reset: 0. Control for IRQ14. See: Smicontrol96.										
27:26	Smicontrol109. Read-write. Reset: 0. Control for IRQ13. See: Smicontrol96.										
25:24	Smicontrol108. Read-write. Reset: 0. Control for IRQ12. See: Smicontrol96.										
23:22	Smicontrol107. Read-write. Reset: 0. Control for IRQ11. See: Smicontrol96.										
21:20	Smicontrol106. Read-write. Reset: 0. Control for IRQ10. See: Smicontrol96.										
19:18	Smicontrol105. Read-write. Reset: 0. Control for IRQ9. See: Smicontrol96.										
17:16	Smicontrol104. Read-write. Reset: 0. Control for IRQ8. See: Smicontrol96.										
15:14	Smicontrol103. Read-write. Reset: 0. Control for IRQ7. See: Smicontrol96.										
13:12	Smicontrol102. Read-write. Reset: 0. Control for IRQ6. See: Smicontrol96.										
11:10	Smicontrol101. Read-write. Reset: 0. Control for IRQ5. See: Smicontrol96.										
9:8	Smicontrol100. Read-write. Reset: 0. Control for IRQ4. See: Smicontrol96.										
7:6	Smicontrol99. Read-write. Reset: 0. Control for IRQ3. See: Smicontrol96.										
5:4	Smicontrol98. Read-write. Reset: 0. Control for IRQ2. See: Smicontrol96.										
3:2	Smicontrol97. Read-write. Reset: 0. Control for IRQ1. See: Smicontrol96.										
1:0	Smicontrol96. Read-write. Reset: 0. Control for IRQ0. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxBC SmiControl7

This register specifies the control mechanism for SMI sources in [SMIx8C\[31:16\]](#).

Bits	Description										
31:16	Reserved.										
15:14	Smicontrol119. Read-write. Reset: 0. Control for IRQ23. See: Smicontrol112.										
13:12	Smicontrol118. Read-write. Reset: 0. Control for IRQ22. See: Smicontrol112.										
11:10	Smicontrol117. Read-write. Reset: 0. Control for IRQ21. See: Smicontrol112.										
9:8	Smicontrol116. Read-write. Reset: 0. Control for IRQ20. See: Smicontrol112.										
7:6	Smicontrol115. Read-write. Reset: 0. Control for IRQ19. See: Smicontrol112.										
5:4	Smicontrol114. Read-write. Reset: 0. Control for IRQ18. See: Smicontrol112.										
3:2	Smicontrol113. Read-write. Reset: 0. Control for IRQ17. See: Smicontrol112.										
1:0	Smicontrol112. Read-write. Reset: 0. Control for IRQ16. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ 13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ 13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ 13										

SMIxC0 SmiControl8

This register specifies the control mechanism for SMI sources in [SMIx90\[15:0\]](#).

Bits	Description										
31:30	Smicontrol143. Read-write. Reset: 0. Control for Long timer. See: Smicontrol133.										
29:28	Smicontrol142. Read-write. Reset: 0. Control for Short timer. See: Smicontrol133.										
27:26	Smicontrol141. Read-write. Reset: 0. Control for C state Message. See: Smicontrol133.										
25:24	Smicontrol140. Read-write. Reset: 0. Control for SMIx98[FakeSts2] generated interrupts. See: Smicontrol133.										
23:22	Smicontrol139. Read-write. Reset: 0. Control for SMIx98[FakeSts1] generated interrupts. See: Smicontrol133.										
21:20	Smicontrol138. Read-write. Reset: 0. Control for SMIx98[FakeSts0] generated interrupts. See: Smicontrol133.										
19:12	Reserved.										
11:10	Smicontrol133. Read-write. Reset: 0. Control for Fan0 Tach too slow event. <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ 13</td> </tr> </tbody> </table>	Bits	Definition	00b	Disable	01b	SMI	10b	NMI	11b	IRQ 13
Bits	Definition										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ 13										
9:0	Reserved.										

SMIxC4 SmiControl9

This register specifies the control mechanism for SMI sources in [SMIx90\[31:16\]](#).

Bits	Description
31:30	Smicontrol159. Read-write. Reset: 0. Control for configuration cycle trapping 3. See: Smicontrol144.
29:28	Smicontrol158. Read-write. Reset: 0. Control for configuration cycle trapping 2. See: Smicontrol144.
27:26	Smicontrol157. Read-write. Reset: 0. Control for configuration cycle trapping 1. See: Smicontrol144.
25:24	Smicontrol156. Read-write. Reset: 0. Control for configuration cycle trapping 0. See: Smicontrol144.
23:22	Smicontrol155. Read-write. Reset: 0. Control for memory trapping 3. See: Smicontrol144.
21:20	Smicontrol154. Read-write. Reset: 0. Control for memory trapping 2. See: Smicontrol144.
19:18	Smicontrol153. Read-write. Reset: 0. Control for memory trapping 1. See: Smicontrol144.
17:16	Smicontrol152. Read-write. Reset: 0. Control for memory trapping 0. See: Smicontrol144.
15:14	Smicontrol151. Read-write. Reset: 0. Control for IO trapping 3. See: Smicontrol144.
13:12	Smicontrol150. Read-write. Reset: 0. Control for IO trapping 2. See: Smicontrol144.
11:10	Smicontrol149. Read-write. Reset: 0. Control for IO trapping 1. See: Smicontrol144.
9:8	Smicontrol148. Read-write. Reset: 0. Control for IO trapping 0. See: Smicontrol144.
7:6	Smicontrol147. Read-write. Reset: 0. Control for P state message 2. See: Smicontrol144.
5:4	Smicontrol146. Read-write. Reset: 0. Control for P state message 1. See: Smicontrol144.

3:2	Smicontrol145. Read-write. Reset: 0. Control for P state message 0. See: Smicontrol144.										
1:0	Smicontrol144. Read-write. Reset: 0. Control for AB SMI trapping request. <table> <tr> <td><u>Bits</u></td> <td><u>Definition</u></td> </tr> <tr> <td>00b</td> <td>Disable</td> </tr> <tr> <td>01b</td> <td>SMI</td> </tr> <tr> <td>10b</td> <td>NMI</td> </tr> <tr> <td>11b</td> <td>IRQ13</td> </tr> </table>	<u>Bits</u>	<u>Definition</u>	00b	Disable	01b	SMI	10b	NMI	11b	IRQ13
<u>Bits</u>	<u>Definition</u>										
00b	Disable										
01b	SMI										
10b	NMI										
11b	IRQ13										

SMIxC8 IoTrapping0

Bits	Description
15:0	IoTrapping0. Read-write. Reset: 0. Specifies the IO address which causes SMI event.

SMIxCA IoTrapping1

Bits	Description
15:0	IoTrapping1. Read-write. Reset: 0. Specifies the IO address which causes SMI event.

SMIxCC IoTrapping2

Bits	Description
15:0	IoTrapping2. Read-write. Reset: 0. Specifies the IO address which causes SMI event.

SMIxCE IoTrapping3

Bits	Description
15:0	IoTrapping3. Read-write. Reset: 0. Specifies the IO address which causes SMI event.

SMIxD0 MemTrapping0

Bits	Description
31:2	MemTrapping. Read-write. Reset: 0. Specifies the 30-bit memory address which causes SMI event. The lowest 2 bits are ignored.
1	MemRdOvrEn. Read-write. Reset: 0. 1=Force read data to be replaced by SMIxD4 [MemRdOvrData0] .
0	MemTrappingRw. Read-write. Reset: 0. 0=Trap on read access at the address specified by [MemTrapping]. 1=Trap on write access.

SMIxD4 MemRdOvrData0

Bits	Description
31:0	MemRdOvrData . Read-write. Reset: 0. This 32-bit data is used as the return data when the memory read trapping is enabled through SMIxD0[MemRdOvrEn] .

SMIxD8 MemTrapping1

Bits	Description
31:2	MemTrapping . Read-write. Reset: 0. Specifies the 30-bit memory address which causes SMI event. The lowest 2 bits are ignored.
1	MemRdOvrEn . Read-write. Reset: 0. 1=Force read data to be replaced by SMIxDC[MemRdOvrData1] .
0	MemTrappingRw . Read-write. Reset: 0. 0=Trap on read access at the address specified by [Mem-Trapping]. 1=Trap on write access.

SMIxDC MemRdOvrData1

Bits	Description
31:0	MemRdOvrData . Read-write. Reset: 0. This 32-bit data is used as the return data when the memory read trapping is enabled through SMIxD8[MemRdOvrEn] .

SMIxE0 MemTrapping2

Bits	Description
31:2	MemTrapping . Read-write. Reset: 0. Specifies the 30-bit memory address which causes SMI event. The lowest 2 bits are ignored.
1	MemRdOvrEn . Read-write. Reset: 0. 1=Force read data to be replaced by SMIxE4[MemRdOvrData2] .
0	MemTrappingRw . Read-write. Reset: 0. 0=Trap on read access at the address specified by [Mem-Trapping]. 1=Trap on write access.

SMIxE4 MemRdOvrData2

Bits	Description
31:0	MemRdOvrData . Read-write. Reset: 0. This 32-bit data is used as the return data when the memory read trapping is enabled through SMIxE0[MemRdOvrEn] .

SMIxE8 MemTrapping3

Bits	Description
31:2	MemTrapping . Read-write. Reset: 0. Specifies the 30-bit memory address which causes SMI event. The lowest 2 bits are ignored.
1	MemRdOvrEn . Read-write. Reset: 0. 1=Force read data to be replaced by SMIxEC [MemRdOvrData3] .
0	MemTrappingRw . Read-write. Reset: 0. 0=Trap on read access at the address specified by [Mem-Trapping]. 1=Trap on write access.

SMIxEC MemRdOvrData3

Bits	Description
31:0	MemRdOvrData . Read-write. Reset: 0. This 32-bit data is used as the return data when the memory read trapping is enabled through SMIxE8[MemRdOvrEn] .

SMIxF0 CfgTrapping0

Bits	Description
31:2	CfgTrapping . Read-write. Reset: 0. Specifies the AD[31:2] value during configure cycle which causes SMI event.
1	IoTrappingRw0 . Read-write. Reset: 0. 0=Trap on IO read access on the address specified in SMIxC8 [IoTrapping0] . 1=Trap on IO write access on the address specified in SMIxC8 [IoTrapping0] .
0	CfgTrappingRw . Read-write. Reset: 0. 0=Trap on read access at the address specified in [CfgTrapping]. 1=Trap on write access.

SMIxF4 CfgTrapping1

Bits	Description
31:2	CfgTrapping . Read-write. Reset: 0. Specifies the AD[31:2] value during configure cycle which causes SMI event.
1	IoTrappingRw1 . Read-write. Reset: 0. 0=Trap on IO read access on the address specified in SMIxCA [IoTrapping1] . 1=Trap on IO write access on the address specified in SMIxCA [IoTrapping1] .
0	CfgTrappingRw . Read-write. Reset: 0. 0=Trap on read access at the address specified in [CfgTrapping]. 1=Trap on write access.

SMIxF8 CfgTrapping2

Bits	Description
31:2	CfgTrapping . Read-write. Reset: 0. Specifies the AD[31:2] value during configure cycle which causes SMI event.

1	IoTrappingRw2. Read-write. Reset: 0. 0=Trap on IO read access on the address specified in SMIxCC [IoTrapping2] . 1=Trap on IO write access on the address specified in SMIxCC [IoTrapping2] .
0	CfgTrappingRw. Read-write. Reset: 0. 0=Trap on read access at the address specified in [CfgTrapping]. 1=Trap on write access.

SMIxFC CfgTrapping3

Bits	Description
31:2	CfgTrapping. Read-write. Reset: 0. Specifies the AD[31:2] value during configure cycle which causes SMI event.
1	IoTrappingRw3. Read-write. Reset: 0. 0=Trap on IO read access at the address specified in SMIxCE [IoTrapping3] . 1=Trap on IO write access at the address specified in SMIxCE [IoTrapping3] .
0	CfgTrappingRw. Read-write. Reset: 0. 0=Trap on read access at the address specified in [CfgTrapping]. 1=Trap on write access.

3.26.17 Watchdog Timer (WDT) Registers

Watchdog timer registers are accessed through two methods:

- Memory access through watchdog timer base address defined by [PMx48 \[WatchdogTimerEn\]](#):
 - Program the watchdog timer base address through [PMx48\[WatchdogBase\]](#).
 - Enable watchdog timer address decoding through [PMx48\[WatchdogDecodeEn\]](#).
- Memory mapped or IO mapped access through the AcpiMmio region. The WDT registers start from [PMx24\[AcpimMmioAddr\]+B00h](#). See [PMx24 \[AcpimMmioEn\]](#).

WDTx00 WatchdogControl

Bits	Description
31:8	Reserved.
7	WatchdogTrigger . RAZ; write-1-only. Reset: 0. Writing 1 to this bit triggers the watchdog to start a new count interval, counting down from the value that was last written to WDTx04 . Setting this bit has no effect if the watchdog is disabled or stopped.
6:4	Reserved.
3	WatchdogDisable . Read-only. Reset: 1. This bit reflects the state of the watchdog timer hardware. 0=Enable. 1=Disable. This bit reflects the state of PMx48[WatchdogFuncDisable] .
2	WatchdogAction . Read-write. Reset: 0. This bit determines the action to be taken when the watchdog timer expires. 0=System reset. 1=System power off. The bit is only valid when the watchdog is enabled.
1	WatchdogFired . Read; write-1-to-clear. Cold reset: 0. 1=The watchdog timer has expired and caused the current restart. The bit is cleared by a power cycle or by the operating system and it must remain cleared for any restart that is not caused by the watchdog timer firing. The bit is only valid when the watchdog is enabled.
0	WatchdogRunStopB . Read-write. Reset: 0. 1=Watchdog is in the running state. 0=Watchdog is in the stopped state. This bit is used to control or indicate whether the watchdog is in the running or stopped states. If the watchdog is in the stopped state and a 1 is written to this bit, the watchdog moves to the running state, but a count interval is not started until a 1 is written to bit [7]. If the watchdog is in the running state, writing 1 to this bit has no effect. The bit is only valid when the watchdog is enabled.

WDTx04 WatchdogCount

Bits	Description
31:16	Reserved.
15:0	WatchdogCount . Read-write. Reset: X. Writing this register specifies the countdown time for the counter. Reading this register returns the current counter value. The units are defined in the Units field in the Watchdog Resource Table (WDRT). The maximum value is defined in the Max Count field in the WDRT.

3.26.18 Wake Alarm Device (AcDcTimer) Registers

The AC/DC timer registers are used to control the wake alarm device. They are accessed through the AcpiMmio region, which can be memory mapped or IO mapped. The AC DC timer registers range from [PMx24\[AcpimMmioAddr\]+1D00h](#) to [PMx24\[AcpimMmioAddr\]+1DFFh](#). See [PMx24 \[AcpimMmioEn\]](#).

AcDcTimerx00 AcTimerValue

Bits	Description								
31:0	<p>AcTimerValue. Read-write; updated-by-hardware. Reset: FFFF_FFFFh. Writing the register with a value other than FFFF_FFFFh starts the AC timer. Reading this register returns the current value of the AC timer.</p> <p>When the AC or DC timer generates a wake up event, this register is reset to FFFF_FFFFh by hardware.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>FFFF_FFFFh</td> <td>Disable the AC timer.</td> </tr> <tr> <td>FFFF_FFFEh-0000_0001h</td> <td>The value indicates the number of seconds between the time when the AC timer is programmed and the time when it expires.</td> </tr> <tr> <td>0000_0000h</td> <td>The AC timer wakes up the system instantly.</td> </tr> </tbody> </table>	Bits	Definition	FFFF_FFFFh	Disable the AC timer.	FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the AC timer is programmed and the time when it expires.	0000_0000h	The AC timer wakes up the system instantly.
Bits	Definition								
FFFF_FFFFh	Disable the AC timer.								
FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the AC timer is programmed and the time when it expires.								
0000_0000h	The AC timer wakes up the system instantly.								

AcDcTimerx04 AcExpiredTimerPolicy

Bits	Description								
31:0	<p>AcExpiredTimerPolicy. Read-write; updated-by-hardware. Reset: FFFF_FFFFh. When the AC timer expires, the wake signal is asserted if the current power source is AC; the wake signal is not asserted if the current power source is DC. If the power source is switched from DC to AC after the AC timer expired, we wait for the number of seconds defined in this register and then wake up the system. When the AC or DC timer generates a wakeup event, this register is reset to FFFF_FFFFh by hardware.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>FFFF_FFFFh</td> <td>Disable the AC expired timer policy.</td> </tr> <tr> <td>FFFF_FFFEh-0000_0001h</td> <td>The value indicates the number of seconds between the time when the power is switched to AC and the time when it generates the wake-up event.</td> </tr> <tr> <td>0000_0000h</td> <td>The expired AC timer wakes up the system instantly once the power source is switched to AC.</td> </tr> </tbody> </table>	Bits	Definition	FFFF_FFFFh	Disable the AC expired timer policy.	FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the power is switched to AC and the time when it generates the wake-up event.	0000_0000h	The expired AC timer wakes up the system instantly once the power source is switched to AC.
Bits	Definition								
FFFF_FFFFh	Disable the AC expired timer policy.								
FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the power is switched to AC and the time when it generates the wake-up event.								
0000_0000h	The expired AC timer wakes up the system instantly once the power source is switched to AC.								

AcDcTimerx08 AcTimerStatus

Bits	Description
31:2	Reserved.
1	AcTimerWakeup. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Wake up was caused by AC timer expiration. 0=Wake-up was not caused by AC timer expiration.
0	AcTimerExpired. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=AC timer expired. 0=AC timer has not expired.

AcDcTimerx10 DcTimerValue

Bits	Description								
31:0	<p>DcTimerValue. Read-write; updated-by-hardware. Reset: FFFF_FFFFh. Writing the register with a value other than FFFF_FFFFh starts the DC timer. Reading this register returns the current value of the DC timer.</p> <p>When the AC or DC Timer generates a wake up event, this register is reset to FFFF_FFFFh by hardware.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>FFFF_FFFFh</td> <td>Disable the DC timer.</td> </tr> <tr> <td>FFFF_FFFEh-0000_0001h</td> <td>The value indicates the number of seconds between the time when the DC timer is programmed and the time when it expires.</td> </tr> <tr> <td>0000_0000h</td> <td>The DC timer wakes up the system instantly.</td> </tr> </tbody> </table>	Bits	Definition	FFFF_FFFFh	Disable the DC timer.	FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the DC timer is programmed and the time when it expires.	0000_0000h	The DC timer wakes up the system instantly.
Bits	Definition								
FFFF_FFFFh	Disable the DC timer.								
FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the DC timer is programmed and the time when it expires.								
0000_0000h	The DC timer wakes up the system instantly.								

AcDcTimerx14 DcExpiredTimerPolicy

Bits	Description								
31:0	<p>DcExpiredTimerPolicy. Read-write; updated-by-hardware. Reset: FFFF_FFFFh. When the DC timer expires, the wake signal is asserted if the current power source is DC; the wake signal is not asserted if the current power source is AC. If the power source is switched from AC to DC after the DC timer expired, we wait for the number of seconds defined in this register and then wake up the system. When the AC or DC timer generates a wakeup event, this register is reset to FFFF_FFFFh by hardware.</p> <table> <thead> <tr> <th>Bits</th> <th>Definition</th> </tr> </thead> <tbody> <tr> <td>FFFF_FFFFh</td> <td>Disable the DC expired timer policy.</td> </tr> <tr> <td>FFFF_FFFEh-0000_0001h</td> <td>The value indicates the number of seconds between the time when the power is switched to DC and the time when it generates the wake-up event.</td> </tr> <tr> <td>0000_0000h</td> <td>The expired DC timer wakes up the system instantly once the power source is switched to DC.</td> </tr> </tbody> </table>	Bits	Definition	FFFF_FFFFh	Disable the DC expired timer policy.	FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the power is switched to DC and the time when it generates the wake-up event.	0000_0000h	The expired DC timer wakes up the system instantly once the power source is switched to DC.
Bits	Definition								
FFFF_FFFFh	Disable the DC expired timer policy.								
FFFF_FFFEh-0000_0001h	The value indicates the number of seconds between the time when the power is switched to DC and the time when it generates the wake-up event.								
0000_0000h	The expired DC timer wakes up the system instantly once the power source is switched to DC.								

AcDcTimerx18 DcTimerStatus

Bits	Description
31:2	Reserved.
1	DcTimerWakeup. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=Wake-up was caused by DC timer expiration. 0=Wake-up was not caused by DC timer expiration.
0	DcTimerExpired. Read; set-by-hardware; write-1-to-clear. Reset: 0. 1=DC timer expired. 0=DC timer has not expired.

AcDcTimerx20 AcDcTimerCtrl

Bits	Description
31:10	Reserved.

9	DcTimerEventEn . Read-write. Reset: 0. 1=Enable DC Timer to wake up system. 0=Disable.
8	AcTimerEventEn . Read-write. Reset: 0. 1=Enable AC Timer to wake up system. 0=Disable.
7:1	Reserved.
0	Busy . Read-only; updated-by-hardware. Reset: 0h. Right after AcDcTimerx00 [AcTimerValue] or AcDcTimerx10 [DcTimerValue] is programed, the hardware sets this bit to 1. The hardware will clear this bit once the programming is done and the corresponding timer is started properly. Before the software writes to AcDcTimerx00 [AcTimerValue] or AcDcTimerx10 [DcTimerValue] , it has to read this bit and make sure it is 0. Otherwise, the hardware will just ignore the programming action from software. For the registers other than AcDcTimerx00 [AcTimerValue] or AcDcTimerx10 [DcTimerValue] , there is no such limitation.

4 Register List

The following is a list of all storage elements, context, and registers provided in this document. Page numbers, register mnemonics, and register names are provided.

45	SMMFEC0: SMM IO Trap Offset	202	D0F0x98_x4[A,9]: ORB LCLK Clock Control 1-0
45	SMMFEC4: Local SMI Status	203	D0F0xB8: SMU Index Address
45	SMMFEC8: SMM IO Restart Byte	203	D0F0xBC: SMU Index Data
46	SMMFEC9: Auto Halt Restart Offset	203	D0F0xBC_x3F800: FIRMWARE_FLAGS
46	SMMFEC9A: NMI Mask	203	D0F0xBC_x3F804: FIRMWARE_VID
46	SMMFED8: SMM SVM State	204	D0F0xBC_x3F820: PM_INTERVAL_CNTL_0
47	SMMFEFC: SMM-Revision Identifier	204	D0F0xBC_x3F828: PM_TIMER_PERIOD
47	SMMFF00: SMM Base Address (SMM_BASE)	204	D0F0xBC_x3F9D8: PM_CONFIG
116	MR0: DDR3 MR0	205	D0F0xBC_x3F9E8: NB_DPM_CONFIG_1
118	MR1: DDR3 MR1	205	D0F0xBC_x3F9EC: NB_DPM_CONFIG_2
118	MR2: DDR3 MR2	206	D0F0xBC_x3F9F4: CSR_GNB_1
119	MR3: DDR3 MR3	206	D0F0xBC_x3F9F8: CSR_GNB_3
189	IOCF8: IO-Space Configuration Address	206	D0F0xBC_x3FD[8C:00:step14]: LCLK DPM Control 0
190	IOCFC: IO-Space Configuration Data Port	207	D0F0xBC_x3FD[94:08:step14]: LCLK DPM Control 2
191	D0F0x00: Device/Vendor ID	207	D0F0xBC_x3FD[9C:10:step14]: LCLK DPM Activity Thresholds
191	D0F0x04: Status/Command	208	D0F0xBC_x3FDC8: SMU_LCLK_DPM_CNTL
191	D0F0x08: Class Code/Revision ID	208	D0F0xBC_x3FDD0:
191	D0F0x0C: Header Type	208	SMU_LCLK_DPM_THERMAL_THROTTLING_CNTL
192	D0F0x2C: Subsystem and Subvendor ID	208	D0F0xBC_x3FDD4:
192	D0F0x34: Capabilities Pointer	209	SMU_LCLK_DPM_THERMAL_THROTTLING_THRESHOLDS
192	D0F0x48: NB Header Write Register	209	D0F0xBC_xC020_008C: LCLK_DEEP_SLEEP_CNTL
192	D0F0x4C: PCI Control	209	D0F0xBC_xC020_0110: Activity Monitor Control
193	D0F0x60: Miscellaneous Index	209	D0F0xBC_xC210_0000: CPU Interrupt Request
193	D0F0x64: Miscellaneous Index Data	209	D0F0xBC_xC210_0004: CPU Interrupt Status
193	D0F0x64_x00: Northbridge Control	210	D0F0xBC_xC210_003C: CPU Interrupt Argument
193	D0F0x64_x0C: IOC Bridge Control	210	D0F0xBC_xC210_0040: CPU Interrupt Response
193	D0F0x64_x0D: IOC PCI Configuration	210	D0F0xC8: DEV Index Address
193	D0F0x64_x16: IOC Advanced Error Reporting Control	210	D0F0xCC: DEV Index Data
194	D0F0x64_x17: Memory Mapped IO Base Address	210	D0F0xCC_x01: IOC Bridge Control
194	D0F0x64_x18: Memory Mapped IO Limit	211	D0F0xD4_x0109_14C3: Bif Doorbell Control Ind
194	D0F0x64_x19: Top of Memory 2 Low	211	D0F0xD4_x0109_14E1: CC Bif Bx Strap0 Ind
194	D0F0x64_x1A: Top of Memory 2 High	211	D0F0xD4_x0109_14E2: CC Bif Bx Strap1 Ind
194	D0F0x64_x1D: Internal Graphics PCI Control	212	D0F0xD4_x0109_1507: CC Bif Bx Pinstrap0 Ind
195	D0F0x64_x1F: FCH Location	212	D0F0xE0: Link Index Address 1
195	D0F0x64_x22: LCLK Control 0	212	D0F0xE4: Link Index Data 1
196	D0F0x64_x23: LCLK Control 1	213	D0F0xE4_x0110_0010: PIF Control (GPPSB_PIF0_CNTL)
196	D0F0x64_x3[4:0]: Programmable Device Remap Register	213	D0F0xE4_x0110_0011: PIF Pairing (PIF0_PAIRING)
196	D0F0x64_x46: IOC Features Control	214	D0F0xE4_x0110_001[8:7,3:2]: PIF Power Down Control [3:0] (PIF0_PWRDOWN)
197	D0F0x7C: IOC Configuration Control	215	D0F0xE4_x0120_0004: Phy Global Control 0
197	D0F0x84: Link Arbitration	215	D0F0xE4_x0120_4440: Phy RO PLL Control
197	D0F0x90: Northbridge Top of Memory	215	D0F0xE4_x0120_4450: PhyRO PLL Override Control 0
198	D0F0x94: Northbridge ORB Configuration Offset	216	D0F0xE4_x0130_0046: Subsystem and Vendor ID
198	D0F0x98: Northbridge ORB Configuration Data Port	216	D0F0xE4_x0130_0080: Link Configuration (PCIE_LINK_CONFIG)
198	D0F0x98_x06: ORB Downstream Control 0	216	D0F0xE4_x0130_0[C:8]00: Link Hold Training Control (PCIE_HOLD_TRAINING)
198	D0F0x98_x07: ORB Upstream Arbitration Control 0	217	D0F0xE4_x0130_0[C:8]03: Link Deemphasis Control (LC_MISC_PORT)
199	D0F0x98_x08: ORB Upstream Arbitration Control 1	217	D0F0xE4_x0130_0[C:8]04: Link AER Control
199	D0F0x98_x09: ORB Upstream Arbitration Control 2	217	D0F0xE4_x0130_0[C:8]05: Link Training Control
199	D0F0x98_x0C: ORB Upstream Arbitration Control 5	217	D0F0xE4_x0130_8002: IO Link Wrapper Scratch
200	D0F0x98_x1E: ORB Receive Control 0	218	D0F0xE4_x0130_8011: Link Transmit Clock Gating Control
200	D0F0x98_x26: ORB IOMMU Control 0	218	D0F0xE4_x0130_8012: Link Idle-Resume Clock Gating Control
200	D0F0x98_x27: ORB IOMMU Control 1	218	D0F0xE4_x0130_8013: Transmit Clock Pll Control
201	D0F0x98_x28: ORB Transmit Control 0	219	D0F0xE4_x0130_8014: Link Transmit Clock Gating Control 2
201	D0F0x98_x2C: ORB Clock Control	220	D0F0xE4_x0130_8015: IO Link IOC Control
201	D0F0x98_x37: ORB Allow LDTSTOP Control 0	220	D0F0xE4_x0130_8016: Link Clock Switching Control
201	D0F0x98_x3A: ORB Source Tag Translation Control 2	221	D0F0xE4_x0130_802[4:1]: Transmitter Lane Mux
202	D0F0x98_x3B: ORB Source Tag Translation Control 3	222	D0F0xE4_x0130_802[8:5]: Receiver Lane Mux (LM_PCIERXMUX)
		223	D0F0xE4_x0130_8029: Lane Enable (LM_LANEENABLE)
		223	D0F0xE4_x0130_8060: Soft Reset Command 0
		223	D0F0xE4_x0130_8062: Soft Reset Control 0
		223	D0F0xE4_x0130_80F0: BIOS Timer

224	D0F0xE4_x0130_80F1: BIOS Timer Control	244	D1F1x0C: Header Type
224	D0F0xE4_x0140_0002: IO Link Hardware Debug	244	D1F1x10: Audio Registers Base Address
224	D0F0xE4_x0140_0010: IO Link Control 1	244	D1F1x14: Base Address 1
225	D0F0xE4_x0140_0011: IO Link Config Control	245	D1F1x18: Base Address 2
225	D0F0xE4_x0140_001C: IO Link Control 2 (PCIE_CNTL2)	245	D1F1x1C: Base Address 3
225	D0F0xE4_x0140_0020: IO Link Chip Interface Control (PCIE_CI_CNTL)	245	D1F1x20: Base Address 4
225	D0F0xE4_x0140_0040: IO Link Phy Control (PCIE_P_CNTL)	245	D1F1x24: Base Address 5
226	D0F0xE4_x0140_00B0: IO Link Strap Control (PCIE_STRAP_F0)	245	D1F1x2C: Subsystem and Subvendor ID
226	D0F0xE4_x0140_00C0: IO Link Strap Miscellaneous (PCIE_STRAP_MISC)	245	D1F1x30: Expansion ROM Base Address
226	D0F0xE4_x0140_00C1: IO Link Strap Miscellaneous2 (PCIE_STRAP_MISC2)	246	D1F1x34: Capabilities Pointer
226	D0F0xF8: Northbridge IOAPIC Index	246	D1F1x3C: Interrupt Line
226	D0F0xFC: Northbridge IOAPIC Data	246	D1F1x4C: Subsystem and Subvendor ID Mirror
226	D0F0xFC_x00: IOAPIC Feature Control Register	246	D1F1x50: Power Management Capability
227	D0F0xFC_x01: IOAPIC Base Address Lower	247	D1F1x54: Power Management Control and Status
227	D0F0xFC_x02: IOAPIC Base Address Upper	247	D1F1x58: PCI Express Capability
227	D0F0xFC_x0F: IOAPIC GBIF Interrupt Routing Register	247	D1F1x5C: Device Capability
227	D0F0xFC_x1[4:0]: IOAPIC BR Interrupt Routing Register	248	D1F1x60: Device Control and Status
228	D0F0xFC_x30: IOAPIC Serial IRQ Status	249	D1F1x64: Link Capability
228	D0F0xFC_x3[3:0]: IOAPIC Scratch [1:0] Register	249	D1F1x68: Link Control and Status
229	D0F2xF8: PCIe Client Interface Index	250	D1F1x7C: Device Capability 2
229	D0F2xFc: PCIe Client Interface Data	250	D1F1x80: Device Control and Status 2
229	D0F2xFc_x32_L1i: L1_CNTRL_4	251	D1F1x84: Link Capability 2
230	D0F2xFc_x33_L1i: L1_CLKCNTRL_0	251	D1F1x88: Link Control and Status 2
231	D1F0x00: Device/Vendor ID	251	D1F1xA0: MSI Capability
231	D1F0x04: Status/Command Register	252	D1F1xA4: MSI Message Address Low
232	D1F0x08: Class Code/Revision ID Register	252	D1F1xA8: MSI Message Address High
232	D1F0x0C: Header Type Register	252	D1F1xAC: MSI Message Data
232	D1F0x10: Graphic Memory Base Address	252	D1F1x100: Vendor Specific Enhanced Capability
233	D1F0x14: Graphics Memory Base Address 64	252	D1F1x104: Vendor Specific Header
233	D1F0x18: Graphics Doorbell Base Address	253	D1F1x108: Vendor Specific 1
233	D1F0x1C: Graphics Doorbell Base Address 64	253	D1F1x10C: Vendor Specific 2
233	D1F0x20: Graphics IO Base Address	254	D2F0x00: Device/Vendor ID (Host Bridge)
234	D1F0x24: Graphics Memory Mapped Registers Base Address	254	D2F0x04: Status/Command
234	D1F0x2C: Subsystem and Subvendor ID Register	254	D2F0x08: Class Code/Revision ID
234	D1F0x30: Expansion ROM Base Address	254	D2F0x0C: Header Type
234	D1F0x34: Capabilities Pointer	255	D2F0x40: Header Type Write
234	D1F0x3C: Interrupt Line	255	D2F[5:1]x00: Device/Vendor ID
235	D1F0x4C: Subsystem and Subvendor ID Mirror	255	D2F[5:1]x04: Status/Command Register
235	D1F0x50: Power Management Capability	256	D2F[5:1]x08: Class Code/Revision ID Register
235	D1F0x54: Power Management Control and Status	256	D2F[5:1]x0C: Header Type Register
236	D1F0x58: PCI Express Capability	257	D2F[5:1]x18: Bus Number and Secondary Latency Register
236	D1F0x5C: Device Capability	257	D2F[5:1]x1C: IO Base and Secondary Status Register
237	D1F0x60: Device Control and Status	258	D2F[5:1]x20: Memory Limit and Base Register
237	D1F0x64: Link Capability	258	D2F[5:1]x24: Prefetchable Memory Limit and Base Register
238	D1F0x68: Link Control and Status	258	D2F[5:1]x28: Prefetchable Memory Base High Register
239	D1F0x7C: Device Capability 2	258	D2F[5:1]x2C: Prefetchable Memory Limit High Register
239	D1F0x80: Device Control and Status 2	258	D2F[5:1]x30: IO Base and Limit High Register
240	D1F0x84: Link Capability 2	259	D2F[5:1]x34: Capabilities Pointer Register
240	D1F0x88: Link Control and Status 2	259	D2F[5:1]x3C: Bridge Control Register
241	D1F0xA0: MSI Capability	259	D2F[5:1]x50: Power Management Capability Register
241	D1F0xA4: MSI Message Address Low	260	D2F[5:1]x54: Power Management Control and Status Register
241	D1F0xA8: MSI Message Address High	260	D2F[5:1]x58: PCI Express Capability Register
241	D1F0xAC: MSI Message Data	261	D2F[5:1]x5C: Device Capability Register
242	D1F0x100: Vendor Specific Enhanced Capability	261	D2F[5:1]x60: Device Control and Status Register
242	D1F0x104: Vendor Specific Header	262	D2F[5:1]x64: IO Link Capability Register
242	D1F0x108: Vendor Specific 1	263	D2F[5:1]x68: IO Link Control and Status Register
242	D1F0x10C: Vendor Specific 2	265	D2F[5:1]x6C: Slot Capability Register
243	D1F1x00: Device/Vendor ID	266	D2F[5:1]x70: Slot Control and Status Register
243	D1F1x04: Status/Command	266	D2F[5:1]x74: Root Complex Capability and Control Register
244	D1F1x08: Class Code/Revision ID	267	D2F[5:1]x78: Root Complex Status Register
		267	D2F[5:1]x7C: Device Capability 2
		268	D2F[5:1]x80: Device Control and Status 2
		269	D2F[5:1]x84: IO Link Capability 2

269	D2F[5:1]x88: IO Link Control and Status 2	295	D18F0x[11C,118,114,110]: Link Clumping Enable
270	D2F[5:1]x8C: Slot Capability 2	296	D18F0x150: Link Global Retry Control
270	D2F[5:1]x90: Slot Control and Status 2	296	D18F0x168: Extended Link Transaction Control
270	D2F[5:1]xA0: MSI Capability Register	296	D18F0x16C: Link Global Extended Control
271	D2F[5:1]xA4: MSI Message Address Low	296	D18F0x[18C:170]: Link Extended Control
271	D2F[5:1]xA8: MSI Message Address High	297	D18F0x1A0: Link Initialization Status
271	D2F[5:1]xAC: MSI Message Data	297	D18F0x1DC: Core Enable
271	D2F[5:1]xB0: Subsystem and Subvendor Capability ID Register	299	D18F1x00: Device/Vendor ID
271	D2F[5:1]xB4: Subsystem and Subvendor ID Register	299	D18F1x08: Class Code/Revision ID
272	D2F[5:1]xB8: MSI Capability Mapping	299	D18F1x0C: Header Type
272	D2F[5:1]xBC: MSI Mapping Address Low	299	D18F1x[17C:140,7C:40]: DRAM Base/Limit
272	D2F[5:1]xC0: MSI Mapping Address High	301	D18F1x[2CC:2A0,1CC:180,BC:80]: MMIO Base/Limit
272	D2F[5:1]xE0: Root Port Index	303	D18F1x[DC:C0]: IO-Space Base/Limit
272	D2F[5:1]xE4: Root Port Data	305	D18F1x[1DC:1D0,EC:E0]: Configuration Map
273	D2F[5:1]xE4_x20: Root Port TX Control	306	D18F1xF0: DRAM Hole Address
273	D2F[5:1]xE4_x50: Root Port Lane Status	306	D18F1xF4: VGA Enable
273	D2F[5:1]xE4_x6A: Root Port Error Control	307	D18F1x10C: DCT Configuration Select
273	D2F[5:1]xE4_x70: Root Port Receiver Control	308	D18F1x120: DRAM Base System Address
274	D2F[5:1]xE4_xA0: Per Port Link Controller (LC) Control	308	D18F1x124: DRAM Limit System Address
274	D2F[5:1]xE4_xA1: LC Training Control	309	D18F1x2[1C:00]: DRAM Controller Base/Limit
274	D2F[5:1]xE4_xA2: LC Link Width Control	311	D18F2x00: Device/Vendor ID
275	D2F[5:1]xE4_xA3: LC Number of FTS Control	311	D18F2x08: Class Code/Revision ID
275	D2F[5:1]xE4_xA4: LC Link Speed Control	311	D18F2x0C: Header Type
276	D2F[5:1]xE4_xA5: LC State 0	311	D18F2x[5C:40]_dct[0]: DRAM CS Base Address
277	D2F[5:1]xE4_xB1: LC Control 2	313	D18F2x[6C:60]_dct[0]: DRAM CS Mask
277	D2F[5:1]xE4_xB5: LC Control 3	313	D18F2x78_dct[0]: DRAM Control
277	D2F[5:1]xE4_xC0: LC Strap Override	314	D18F2x7C_dct[0]: DRAM Initialization
277	D2F[5:1]xE4_xC1: Root Port Miscellaneous Strap Override	315	D18F2x80_dct[0]: DRAM Bank Address Mapping
278	D2F[5:1]xE4_xD0: Root Port ECC Skip OS Feature	316	D18F2x84_dct[0]: DRAM MRS
278	D2F[5:1]x100: Vendor Specific Enhanced Capability Register	317	D18F2x88_dct[0]: DRAM Timing Low
278	D2F[5:1]x104: Vendor Specific Header Register	317	D18F2x8C_dct[0]: DRAM Timing High
279	D2F[5:1]x108: Vendor Specific 1 Register	318	D18F2x90_dct[0]: DRAM Configuration Low
279	D2F[5:1]x10C: Vendor Specific 2 Register	320	D18F2x94_dct[0]: DRAM Configuration High
279	D2F[5:1]x128: Virtual Channel 0 Resource Status Register	323	D18F2x98_dct[0]: DRAM Controller Additional Data Offset
279	D2F[5:1]x150: Advanced Error Reporting Capability	323	D18F2x9C_dct[0]: DRAM Controller Additional Data Port
279	D2F[5:1]x154: Uncorrectable Error Status	324	D18F2x9C_x0000_0000_dct[0]_mp[1:0]: DRAM Output Driver Compensation Control
280	D2F[5:1]x158: Uncorrectable Error Mask	326	D18F2x9C_x0000_0[3:0]0[3:1]_dct[0]_mp[1:0]: DRAM Write Data Timing
281	D2F[5:1]x15C: Uncorrectable Error Severity	327	D18F2x9C_x0000_0004_dct[0]_mp[1:0]: DRAM Address/Command Timing Control
282	D2F[5:1]x160: Correctable Error Status	328	D18F2x9C_x0000_0[3:0]0[7:5]_dct[0]_mp[1:0]: DRAM Read DQS Timing
282	D2F[5:1]x164: Correctable Error Mask	329	D18F2x9C_x0000_0008_dct[0]_mp[1:0]: DRAM Phy Control
282	D2F[5:1]x168: Advanced Error Control	331	D18F2x9C_x0000_000B_dct[0]: DRAM Phy Status Register
283	D2F[5:1]x16C: Header Log DW0	331	D18F2x9C_x0000_000C_dct[0]: DRAM Phy Miscellaneous
283	D2F[5:1]x170: Header Log DW1	332	D18F2x9C_x0000_000D_dct[0]_mp[1:0]: DRAM Phy DLL Control
283	D2F[5:1]x174: Header Log DW2	333	D18F2x9C_x0000_00[2A:10]_dct[0]_mp[1:0]: DRAM DQS Receiver Enable Timing
284	D2F[5:1]x178: Header Log DW3	335	D18F2x9C_x0000_00[4A:30]_dct[0]_mp[1:0]: DRAM DQS Write Timing
284	D2F[5:1]x17C: Root Error Command	336	D18F2x9C_x0000_00[52:50]_dct[0]: DRAM Phase Recovery Control
284	D2F[5:1]x180: Root Error Status	337	D18F2x9C_x0D0F_0[F,8:0]02_dct[0]: Data Byte Transmit PreDriver Calibration
285	D2F[5:1]x184: Error Source ID	338	D18F2x9C_x0D0F_0[F,8:0]0[B,7,3]_dct[0]: Data Byte PoDt Configuration
286	D18F0x00: Device/Vendor ID	339	D18F2x9C_x0D0F_0[F,8:0]04_dct[0]_mp[1:0]: Data Byte 1.5X Pad Configuration
286	D18F0x04: Status/Command	340	D18F2x9C_x0D0F_0[F,8:0]0[A,6]_dct[0]: Data Byte Transmit PreDriver Calibration 2
286	D18F0x08: Class Code/Revision ID	340	D18F2x9C_x0D0F_0[F,8:0]10_dct[0]_mp[1:0]: Data Byte DLL Power Management
286	D18F0x0C: Header Type		
286	D18F0x34: Capabilities Pointer		
286	D18F0x[5C:40]: Routing Table		
287	D18F0x60: Node ID		
287	D18F0x64: Unit ID		
288	D18F0x68: Link Transaction Control		
290	D18F0x6C: Link Initialization Control		
291	D18F0x[E4,C4,A4,84]: Link Control		
291	D18F0x[EC,CC,AC,8C]: Link Feature Capability		
292	D18F0x[F0,D0,B0,90]: Link Base Channel Buffer Count		
294	D18F0x[F4,D4,B4,94]: Link Isochronous Channel Buffer Count		
295	D18F0x[F8,D8,B8,98]: Link Type		

341	D18F2x9C_x0D0F_0[F,8:0]13_dct[0]_mp[1:0]: Data Byte DLL Configuration	374	D18F2x210_dct[0]_nbp[3:0]: DRAM NB P-state
342	D18F2x9C_x0D0F_0[F,8:0]1C_dct[0]_mp[1:0]: Data Byte DLL Power Management	376	D18F2x218_dct[0]_mp[1:0]: DDR3 DRAM Timing 4
343	D18F2x9C_x0D0F_0[F,8:0]1E_dct[0]_mp[1:0]: Data Byte Receiver Bias Current Control	377	D18F2x21C_dct[0]_mp[1:0]: DDR3 DRAM Timing 5
343	D18F2x9C_x0D0F_0[F,8:0]1F_dct[0]_mp[1:0]: Data Byte Receiver Configuration	378	D18F2x220_dct[0]: DDR3 DRAM Timing 6
344	D18F2x9C_x0D0F_0[F,8:0]2[3:0]_dct[0]_mp[1:0]: Data Byte RxDqs DLL Configuration	378	D18F2x224_dct[0]: DDR3 DRAM Timing 7
345	D18F2x9C_x0D0F_0[8:0]2[9:4]_dct[0]_mp[1:0]: Data Byte DLL Configuration	379	D18F2x228_dct[0]: DDR3 DRAM Timing 8
346	D18F2x9C_x0D0F_0[F,8:0]30_dct[0]: Data Byte DLL Configuration and Power Down	380	D18F2x22C_dct[0]_mp[1:0]: DDR3 DRAM Timing 9
346	D18F2x9C_x0D0F_0[F,8:0]31_dct[0]: Data Byte Fence2 Threshold	380	D18F2x234_dct[0]_mp[1:0]: DDR3 DRAM Read ODT Pattern [High:Low]
347	D18F2x9C_x0D0F_0[F,8:0]38_dct[0]: Data Byte DLL Control Register	380	D18F2x[234:230]_dct[0]: DDR3 DRAM Write ODT Pattern [High:Low]
348	D18F2x9C_x0D0F_1C00_dct[0]: Clock Transmit PreDriver Calibration	381	D18F2x240_dct[0]_mp[1:0]: DDR3 DRAM ODT Control
348	D18F2x9C_x0D0F_2[2:0]02_dct[0]: Clock Transmit PreDriver Calibration	382	D18F2x244_dct[0]: DRAM Controller Miscellaneous 3
349	D18F2x9C_x0D0F_[C,8,2][2:0]1E_dct[0]_mp[1:0]: Phy Control	382	D18F2x248_dct[0]_mp[1:0]: DRAM Power Management 0
349	D18F2x9C_x0D0F_[C,8,2][2:0]1F_dct[0]: Receiver Configuration	383	D18F2x24C_dct[0]: DDR3 DRAM Power Management 1
350	D18F2x9C_x0D0F_[C,8,2][2:0]20_dct[0]_mp[1:0]: DLL Delay and Configuration	384	D18F2x250_dct[0]: DRAM Loopback and Training Control
350	D18F2x9C_x0D0F_2[F,2:0]30_dct[0]: Clock DLL Configuration and Power Down	386	D18F2x25[8,4]_dct[0]: DRAM Target [B, A] Base
351	D18F2x9C_x0D0F_4006_dct[0]: DRAM Phy MemVref Observation Configuration	386	D18F2x25C_dct[0]: DRAM Command 0
351	D18F2x9C_x0D0F_4007_dct[0]: DRAM Phy MemVref Configuration	387	D18F2x260_dct[0]: DRAM Command 1
352	D18F2x9C_x0D0F_4009_dct[0]: Phy Cmp MemReset Configuration	387	D18F2x264_dct[0]: DRAM Status 0
352	D18F2x9C_x0D0F_[C,8][1:0]02_dct[0]: Transmit PreDriver Calibration	388	D18F2x268_dct[0]: DRAM Status 1
352	D18F2x9C_x0D0F_[C,8][1:0][12,0E,0A,06]_dct[0]: Transmit PreDriver Calibration 2	388	D18F2x26C_dct[0]: DRAM Status 2
353	D18F2x9C_x0D0F_812F_dct[0]: Tristate Configuration	389	D18F2x270_dct[0]: DRAM PRBS
353	D18F2x9C_x0D0F_[C,8][F,0]30_dct[0]: Cmd/Addr DLL Configuration and Power Down	389	D18F2x274_dct[0]: DRAM DQ Mask Low
354	D18F2x9C_x0D0F_C021_dct[0]_mp[1:0]: DLL Delay and Configuration	390	D18F2x278_dct[0]: DRAM DQ Mask High
354	D18F2x9C_x0D0F_E000_dct[0]_mp[1:0]: Phy Master Configuration	390	D18F2x27C_dct[0]: DRAM ECC and EDC Mask
354	D18F2x9C_x0D0F_E006_dct[0]: Phy PLL Lock Time	390	D18F2x280_dct[0]: DRAM DQ Pattern Override 0
355	D18F2x9C_x0D00_E008_dct[0]: Phy Master Configuration	390	D18F2x284_dct[0]: DRAM DQ Pattern Override 1
355	D18F2x9C_x0D04_E008_dct[0]: Phy Master Configuration	391	D18F2x288_dct[0]: DRAM DQ Pattern Override 2
355	D18F2x9C_x0D0F_E00A_dct[0]: Phy Dynamic Power Mode	391	D18F2x28C_dct[0]: DRAM Command 2
355	D18F2x9C_x0D0F_E013_dct[0]: Phy PLL Regulator Wait Time	392	D18F2x290_dct[0]: DRAM Status 3
355	D18F2x9C_x0D0F_E019_dct[0]: Fence2	392	D18F2x294_dct[0]: DRAM Status 4
356	D18F2x9C_x0D0F_E01A_dct[0]: M1 Fence Value	393	D18F2x298_dct[0]: DRAM Status 5
357	D18F2xA4: DRAM Controller Temperature Throttle	393	D18F2x29C_dct[0]: DRAM Status 6
358	D18F2xA8_dct[0]: DRAM Controller Miscellaneous 2	394	D18F2x2[B4,B0,AC,A8]_dct[0]: DRAM User Data Pattern
359	D18F2xAC: DRAM Controller Temperature Status	394	D18F2x2B8_dct[0]: DRAM Command 3
360	D18F2xF8: P-state Power Information 1	395	D18F2x2[C0,BC]_dct[0]: DRAM Command 4 & 5
360	D18F2xFC: P-state Power Information 2	395	D18F2x2E0_dct[0]: Memory P-state Control and Status
360	D18F2x104: P-state Power Information 3	396	D18F2x2E8_dct[0]_mp[1:0]: MRS Buffer
361	D18F2x110: DRAM Controller Select Low	396	D18F2x2EC_dct[0]_mp[1:0]: MRS Buffer
361	D18F2x114: DRAM Controller Select High	397	D18F2x2F0_dct[0]_mp[1:0]: DRAM Controller Misc 3
362	D18F2x118: Memory Controller Configuration Low	397	D18F2x400_dct[0]: GMC to DCT Control 0
364	D18F2x11C: Memory Controller Configuration High	397	D18F2x404_dct[0]: GMC to DCT Control 1
366	D18F2x1B0: Extended Memory Controller Configuration Low	398	D18F2x408_dct[0]: GMC to DCT Control 2
368	D18F2x1B4: Extended Memory Controller Configuration High Register	399	D18F2x420_dct[0]: GMC to DCT FIFO Config 1
370	D18F2x1BC_dct[0]: DRAM CKE to CS Map	400	D18F3x00: Device/Vendor ID
371	D18F2x200_dct[0]_mp[1:0]: DDR3 DRAM Timing 0	400	D18F3x04: Status/Command
372	D18F2x204_dct[0]_mp[1:0]: DDR3 DRAM Timing 1	400	D18F3x08: Class Code/Revision ID
373	D18F2x208_dct[0]: DDR3 DRAM Timing 2	400	D18F3x0C: Header Type
373	D18F2x20C_dct[0]_mp[1:0]: DDR3 DRAM Timing 3	400	D18F3x34: Capability Pointer
		400	D18F3x40: MCA NB Control
		402	D18F3x44: MCA NB Configuration
		405	D18F3x48: MCA NB Status Low
		405	D18F3x4C: MCA NB Status High
		405	D18F3x50: MCA NB Address Low
		406	D18F3x54: MCA NB Address High
		406	D18F3x58: Scrub Rate Control
		406	D18F3x5C: DRAM Scrub Address Low
		407	D18F3x60: DRAM Scrub Address High
		407	D18F3x64: Hardware Thermal Control (HTC)
		408	D18F3x68: Software P-state Limit
		409	D18F3x6C: Data Buffer Count

409	D18F3x70: SRI to XBAR Command Buffer Count	448	D18F5x80: Compute Unit Status 1
410	D18F3x74: XBAR to SRI Command Buffer Count	449	D18F5x84: Northbridge Capabilities 2
412	D18F3x78: MCT to XBAR Buffer Count	450	D18F5x88: NB Configuration 4 (NB_CFG4)
413	D18F3x7C: Free List Buffer Count	450	D18F5x8C: NB Configuration 5 (NB_CFG5)
414	D18F3x[84:80]: ACPI Power State Control	450	D18F5xE0: Processor TDP Running Average
416	D18F3x88: NB Configuration 1 Low (NB_CFG1_LO)	451	D18F5xE8: TDP Limit 3
416	D18F3x8C: NB Configuration 1 High (NB_CFG1_HI)	451	D18F5xEC: Load Step Throttle Control
417	D18F3xA0: Power Control Miscellaneous	451	D18F5x128: Clock Power/Timing Control 3
418	D18F3xA4: Reported Temperature Control	452	D18F5x12C: Clock Power/Timing Control 4
419	D18F3xA8: Pop Up and Down P-states	453	D18F5x16[C:0]: Northbridge P-state [3:0]
419	D18F3xB8: NB Array Address	455	D18F5x170: Northbridge P-state Control
419	D18F3xBC: NB Array Data Port	456	D18F5x174: Northbridge P-state Status
420	D18F3xBC_x8: DRAM ECC	457	D18F5x178: Northbridge Fusion Configuration
420	D18F3xD4: Clock Power/Timing Control 0	458	D18F5x17C: Miscellaneous Voltages
422	D18F3xD8: Clock Power/Timing Control 1	458	D18F5x188: Clock Power/Timing Control 5
423	D18F3xDC: Clock Power/Timing Control 2	459	D18F5x18C: Clock Power/Timing Control 6
425	D18F3xE4: Thermtrip Status	459	D18F5x194: Name String Address Port
425	D18F3xE8: Northbridge Capabilities	459	D18F5x198: Name String Data Port
426	D18F3xFC: CPUID Family/Model/Stepping	459	D18F5x198_x[B:0]: Name String Data
426	D18F3x138: DCT0 Bad Symbol Identification	460	D18F5x240: ECC Exclusion Base Address Low
427	D18F3x13C: DCT1 Bad Symbol Identification	460	D18F5x244: ECC Exclusion Base Address High
427	D18F3x140: SRI to XCS Token Count	460	D18F5x248: ECC Exclusion Limit Address Low
428	D18F3x144: MCT to XCS Token Count	460	D18F5x24C: ECC Exclusion Limit Address High
428	D18F3x1[54:48]: Link to XCS Token Count	461	D18F5x260: Clock Power/Timing Control 8
429	D18F3x160: NB Machine Check Misc (DRAM Thresholding) 0 (MC4_MISC0)	462	NBIOAPICx00: IO Register Select
430	D18F3x168: NB Machine Check Misc (Link Thresholding) 1 (MC4_MISC1)	462	NBIOAPICx10: IO Window
430	D18F3x17C: Extended Freelist Buffer Count	462	NBIOAPICx10_x00: IOAPIC ID
431	D18F3x180: Extended NB MCA Configuration	462	NBIOAPICx10_x01: IOAPIC Version
433	D18F3x188: NB Configuration 2 (NB_CFG2)	462	NBIOAPICx10_x02: IOAPIC Arbitration
433	D18F3x190: Downcore Control	463	NBIOAPICx10_x[4E:10:step2]: Redirection Table Entry [31:0]
433	D18F3x1A0: Core Interface Buffer Count	463	NBIOAPICx20: IRQ Pin Assertion
434	D18F3x1CC: IBS Control	463	NBIOAPICx40: EOI
435	D18F3x1FC: Product Information Register 1	464	APIC20: APIC ID
435	D18F3x200: Performance Mode Control Register	464	APIC30: APIC Version
435	D18F3x238: DCT2 Bad Symbol Identification	464	APIC80: Task Priority (TPR)
435	D18F3x23C: DCT3 Bad Symbol Identification	464	APIC90: Arbitration Priority (APR)
436	D18F3x2B4: DCT and Fuse Power Gate Control	465	APICA0: Processor Priority (PPR)
437	D18F4x00: Device/Vendor ID	465	APICB0: End of Interrupt
437	D18F4x04: Status/Command	465	APICC0: Remote Read
437	D18F4x08: Class Code/Revision ID	465	APICD0: Logical Destination (LDR)
437	D18F4x0C: Header Type	465	APICE0: Destination Format
437	D18F4x34: Capabilities Pointer	466	APICF0: Spurious-Interrupt Vector (SVR)
438	D18F4x110: Sample and Residency Timers	466	APIC[170:100]: In-Service (ISR)
438	D18F4x11[C:8]: C-state Control	466	APIC[1F0:180]: Trigger Mode (TMR)
442	D18F4x124: C-state Interrupt Control	467	APIC[270:200]: Interrupt Request (IRR)
442	D18F4x128: C-state Policy Control 1	467	APIC280: Error Status
443	D18F4x13C: SMU P-state Control	468	APIC300: Interrupt Command Low (ICR Low)
444	D18F4x15C: Core Performance Boost Control	469	APIC310: Interrupt Command High (ICR High)
445	D18F4x164: Fixed Errata	470	APIC320: LVT Timer
445	D18F4x16C: APM TDP Control	470	APIC330: LVT Thermal Sensor
446	D18F4x1C0: Node Cac Register 1	470	APIC340: LVT Performance Monitor
446	D18F4x250: TDP Limit 8	471	APIC3[60:50]: LVT LINT[1:0]
447	D18F5x00: Device/Vendor ID	471	APIC370: LVT Error
447	D18F5x04: Status/Command	471	APIC380: Timer Initial Count
447	D18F5x08: Class Code/Revision ID	472	APIC390: Timer Current Count
447	D18F5x0C: Header Type	472	APIC3E0: Timer Divide Configuration
447	D18F5x34: Capabilities Pointer	472	APIC400: Extended APIC Feature
447	D18F5x[70,60,50,40]: Northbridge Performance Event Select Low	473	APIC410: Extended APIC Control
448	D18F5x[74,64,54,44]: Northbridge Performance Event Select High	473	APIC420: Specific End Of Interrupt
448	D18F5x[78,68,58,48]: Northbridge Performance Event Counter Low	473	APIC[4F0:480]: Interrupt Enable
448	D18F5x[7C,6C,5C,4C]: Northbridge Performance Event Counter High	473	APIC[530:500]: Extended Interrupt [3:0] Local Vector Table
		474	CPUID Fn0000_0000_EAX: Processor Vendor and Largest Standard Function Number

475	CPUID Fn0000_0000_E[D,C,B]X: Processor Vendor	490	CPUID Fn8000_0007_EBX: RAS Capabilities
475	CPUID Fn0000_0001_EAX: Family, Model, Stepping Identifiers	490	CPUID Fn8000_0007(ECX): Advanced Power Management Information
475	CPUID Fn0000_0001_EBX: LocalApicId, LogicalProcessorCount, CLFlush	490	CPUID Fn8000_0007_EDX: Advanced Power Management Information
476	CPUID Fn0000_0001(ECX): Feature Identifiers	491	CPUID Fn8000_0008_EAX: Long Mode Address Size Identifiers
477	CPUID Fn0000_0001_EDX: Feature Identifiers	491	CPUID Fn8000_0008_EBX: Reserved
478	CPUID Fn0000_000[4:2]: Reserved	492	CPUID Fn8000_0008(ECX): Size Identifiers
478	CPUID Fn0000_0005_EAX: Monitor/MWait	492	CPUID Fn8000_0008_EDX: Reserved
478	CPUID Fn0000_0005_EBX: Monitor/MWait	492	CPUID Fn8000_0009: Reserved
478	CPUID Fn0000_0005(ECX): Monitor/MWait	492	CPUID Fn8000_000A_EAX: SVM Revision and Feature Identification
479	CPUID Fn0000_0005_EDX: Monitor/MWait	492	CPUID Fn8000_000A_EBX: SVM Revision and Feature Identification
479	CPUID Fn0000_0006_EAX: Thermal and Power Management	493	CPUID Fn8000_000A(ECX): SVM Revision and Feature Identification
479	CPUID Fn0000_0006_EBX: Thermal and Power Management	493	CPUID Fn8000_000A_EDX: SVM Revision and Feature Identification
479	CPUID Fn0000_0006(ECX): Thermal and Power Management	493	CPUID Fn8000_00[18:0B]: Reserved
479	CPUID Fn0000_0006_EDX: Thermal and Power Management	493	CPUID Fn8000_0019_EAX: L1 TLB 1G Identifiers
479	CPUID Fn0000_0007_EAX_x0: Structured Extended Feature Identifiers (ECX=0)	494	CPUID Fn8000_0019_EBX: L2 TLB 1G Identifiers
479	CPUID Fn0000_0007_EBX_x0: Structured Extended Feature Identifiers (ECX=0)	494	CPUID Fn8000_0019_E[D,C]X: Reserved
480	CPUID Fn0000_0007(ECX): Structured Extended Feature Identifiers	494	CPUID Fn8000_001A_EAX: Performance Optimization Identifiers
480	CPUID Fn0000_0007_EDX_x0: Structured Extended Feature Identifiers (ECX=0)	495	CPUID Fn8000_001A_E[D,C,B]X: Reserved
480	CPUID Fn0000_0007(ECX): Structured Extended Feature Identifiers	495	CPUID Fn8000_001B_EAX: Instruction Based Sampling Identifiers
480	CPUID Fn0000_0007_EDX_x0: Structured Extended Feature Identifiers (ECX=0)	495	CPUID Fn8000_001B_E[D,C,B]X: Instruction Based Sampling Identifiers
480	CPUID Fn0000_0008_EAX: Cache Properties	496	CPUID Fn8000_001C_EAX: Lightweight Profiling Capabilities 0
480	CPUID Fn0000_0008_EBX: Cache Properties	496	CPUID Fn8000_001C_EBX: Lightweight Profiling Capabilities 0
480	CPUID Fn0000_0008(ECX): Cache Properties	496	CPUID Fn8000_001C(ECX): Lightweight Profiling Capabilities 0
480	CPUID Fn0000_0008_EDX: Cache Properties	496	CPUID Fn8000_001C_EDX: Lightweight Profiling Capabilities 0
481	CPUID Fn0000_0009_EAX_x0: Processor Extended State Enumeration (ECX=0)	496	CPUID Fn8000_001D_EAX_x0: Cache Properties
481	CPUID Fn0000_0009_EBX_x0: Processor Extended State Enumeration (ECX=0)	497	CPUID Fn8000_001D_EAX_x1: Cache Properties
481	CPUID Fn0000_0009(ECX): Processor Extended State Enumeration	497	CPUID Fn8000_001D_EAX_x2: Cache Properties
481	CPUID Fn0000_0009_EDX_x0: Processor Extended State Enumeration (ECX=0)	498	CPUID Fn8000_001D_EAX_x3: Cache Properties
481	CPUID Fn0000_0010_EAX_x0: Processor Extended State Enumeration (ECX=0)	498	CPUID Fn8000_001D_EBX_x0: Cache Properties
481	CPUID Fn0000_0010_EBX_x0: Processor Extended State Enumeration (ECX=0)	499	CPUID Fn8000_001D_EBX_x1: Cache Properties
481	CPUID Fn0000_0010(ECX): Processor Extended State Enumeration	499	CPUID Fn8000_001D_EBX_x2: Cache Properties
481	CPUID Fn0000_0010_EDX_x0: Processor Extended State Enumeration (ECX=0)	499	CPUID Fn8000_001D_EBX_x3: Cache Properties
481	CPUID Fn0000_0011_EAX_x0: Processor Extended State Enumeration (ECX=1)	500	CPUID Fn8000_001D_ECX_x0: Cache Properties
482	CPUID Fn0000_0011_E[D,C,B]X_x1: Processor Extended State Enumeration (ECX=1)	500	CPUID Fn8000_001D_ECX_x1: Cache Properties
482	CPUID Fn0000_0011_ECX_x1: Processor Extended State Enumeration (ECX=1)	500	CPUID Fn8000_001D_ECX_x2: Cache Properties
482	CPUID Fn0000_0011_EDX_x0: Processor Extended State Enumeration (ECX=1)	500	CPUID Fn8000_001D_EDX_x0: Cache Properties
482	CPUID Fn0000_0012_EAX_x0: Processor Extended State Enumeration (ECX=2)	500	CPUID Fn8000_001D_EDX_x1: Cache Properties
482	CPUID Fn0000_0012_EBX_x0: Processor Extended State Enumeration (ECX=2)	501	CPUID Fn8000_001D_EDX_x2: Cache Properties
482	CPUID Fn0000_0012(ECX): Processor Extended State Enumeration	501	CPUID Fn8000_001D_EDX_x3: Cache Properties
482	CPUID Fn0000_0012_EDX_x0: Processor Extended State Enumeration (ECX=2)	501	CPUID Fn8000_001E_EAX: Extended APIC ID
482	CPUID Fn0000_0013_EAX_x0: Processor Extended State Enumeration (ECX=2)	501	CPUID Fn8000_001E_EBX: Compute Unit Identifiers
482	CPUID Fn0000_0013_EBX_x0: Processor Extended State Enumeration (ECX=2)	502	CPUID Fn8000_001E(ECX): Node Identifiers
482	CPUID Fn0000_0013(ECX): Processor Extended State Enumeration	502	CPUID Fn8000_001E_EDX: Reserved
482	CPUID Fn0000_0014_EAX_x0: Load-Store MCA Address	503	MSR0000_0000: Load-Store MCA Address
482	CPUID Fn0000_0014_EBX_x0: Load-Store MCA Status	503	MSR0000_0001: Load-Store MCA Status
482	CPUID Fn0000_0014(ECX): Time Stamp Counter (TSC)	503	MSR0000_0010: Time Stamp Counter (TSC)
483	CPUID Fn0000_0015_EAX_x0: APIC Base Address (APIC_BAR)	503	MSR0000_001B: APIC Base Address (APIC_BAR)
483	CPUID Fn0000_0015_EBX_x0: Cluster ID (EBL_CR_POWERON)	504	MSR0000_002A: Cluster ID (EBL_CR_POWERON)
483	CPUID Fn0000_0015(ECX): Max Performance Frequency Clock Count (MPERF)	504	MSR0000_00E7: Max Performance Frequency Clock Count (MPERF)
485	CPUID Fn0000_0016_EAX_x0: Actual Performance Frequency Clock Count (APERF)	504	MSR0000_00E8: Actual Performance Frequency Clock Count (APERF)
486	CPUID Fn0000_0016_EBX_x0: MTRR Capabilities (MTRRCap)	504	MSR0000_00FE: MTRR Capabilities (MTRRCap)
486	CPUID Fn0000_0016(ECX): SYSENTER CS (SYSENTER_CS)	504	MSR0000_0174: SYSENTER CS (SYSENTER_CS)
486	CPUID Fn0000_0016_EDX_x0: SYSENTER ESP (SYSENTER_ESP)	505	MSR0000_0175: SYSENTER ESP (SYSENTER_ESP)
487	CPUID Fn0000_0016_ECX_x0: SYSENTER EIP (SYSENTER_EIP)	505	MSR0000_0176: SYSENTER EIP (SYSENTER_EIP)
487	CPUID Fn0000_0016(ECX): Global Machine Check Capabilities (MCG_CAP)	505	MSR0000_0179: Global Machine Check Capabilities (MCG_CAP)
488	CPUID Fn0000_0017_EAX_x0: Global Machine Check Status (MCG_STAT)	505	MSR0000_017A: Global Machine Check Status (MCG_STAT)
488	CPUID Fn0000_0017_EBX_x0: Global Machine Check Exception Reporting Control (MCG_CTL)	506	MSR0000_017B: Global Machine Check Exception Reporting Control (MCG_CTL)
488	CPUID Fn0000_0017(ECX): Debug Control (DBG_CTL_MSR)	506	MSR0000_01D9: Debug Control (DBG_CTL_MSR)
488	CPUID Fn0000_0017_EDX_x0: Last Branch From IP (BR_FROM)	506	MSR0000_01DB: Last Branch From IP (BR_FROM)
489	CPUID Fn0000_0017_ECX_x0: Last Branch To IP (BR_TO)	506	MSR0000_01DC: Last Branch To IP (BR_TO)

507	MSR0000_01DD: Last Exception From IP	552	MSRC001_0046: BU Machine Check Control Mask (MC2_CTL_MASK)
507	MSR0000_01DE: Last Exception To IP	552	MSRC001_0047: Reserved (MC3_CTL_MASK)
507	MSR0000_020[0:F]: Variable-Size MTRRs Base/Mask	553	MSRC001_0048: NB Machine Check Control Mask (MC4_CTL_MASK)
508	MSR0000_02[6F:68,59:58,50]: Fixed-Size MTRRs	553	MSRC001_0049: FR Machine Check Control Mask (MC5_CTL_MASK)
510	MSR0000_0277: Page Attribute Table (PAT)	554	MSRC001_00[53:50]: IO Trap (SMI_ON_IO_TRAP_[3:0])
511	MSR0000_02FF: MTRR Default Memory Type (MTRRdefType)	555	MSRC001_0054: IO Trap Control (SMI_ON_IO_TRAP_CTL_STS)
511	MSR0000_0400: MC0 Machine Check Control (MC0_CTL)	555	MSRC001_0055: Interrupt Pending
512	MSR0000_0401: MC0 Machine Check Status (MC0_STATUS)	555	MSRC001_0056: SMI Trigger IO Cycle
515	MSR0000_0402: MC0 Machine Check Address (MC0_ADDR)	556	MSRC001_0058: MMIO Configuration Base Address
516	MSR0000_0403: MC0 Machine Check Miscellaneous (MC0_MISC)	556	MSRC001_0060: BIST Results
516	MSR0000_0404: MC1 Machine Check Control (MC1_CTL)	557	MSRC001_0061: P-state Current Limit
516	MSR0000_0405: MC1 Machine Check Status (MC1_STATUS)	557	MSRC001_0062: P-state Control
518	MSR0000_0406: MC1 Machine Check Address (MC1_ADDR)	557	MSRC001_0063: P-state Status
518	MSR0000_0407: MC1 Machine Check Miscellaneous (MC1_MISC)	558	MSRC001_00[6B:64]: P-state [7:0]
519	MSR0000_0408: MC2 Machine Check Control (MC2_CTL)	560	MSRC001_0070: COVID Control
519	MSR0000_0409: MC2 Machine Check Status (MC2_STATUS)	561	MSRC001_0071: COVID Status
522	MSR0000_040A: MC2 Machine Check Address (MC2_ADDR)	562	MSRC001_0073: C-state Base Address
523	MSR0000_040B: MC2 Machine Check Miscellaneous (MC2_MISC)	563	MSRC001_0074: CPU Watchdog Timer (CpuWdtCfg)
523	MSR0000_040C: MC3 Machine Check Control (MC3_CTL)	564	MSRC001_0080: Frequency Sensitivity Feedback Monitor Actual Count 0
523	MSR0000_040D: MC3 Machine Check Status (MC3_STATUS)	564	MSRC001_0081: Frequency Sensitivity Feedback Monitor Reference Count 0
523	MSR0000_040E: MC3 Machine Check Address (MC3_ADDR)	564	MSRC001_0111: SMM Base Address (SMM_BASE)
523	MSR0000_040F: MC3 Machine Check Miscellaneous (MC3_MISC)	564	MSRC001_0112: SMM TSeg Base Address (SMMAddr)
523	MSR0000_0410: MC4 Machine Check Control (MC4_CTL)	565	MSRC001_0113: SMM TSeg Mask (SMMMask)
525	MSR0000_0411: MC4 Machine Check Status (MC4_STATUS)	566	MSRC001_0114: Virtual Machine Control (VM_CR)
528	MSR0000_0412: MC4 Machine Check Address (MC4_ADDR)	567	MSRC001_0115: IGNNE
531	MSR0000_0413: NB Machine Check Misc 4 (DRAM Thresholding) 0 (MC4_MISC0)	567	MSRC001_0116: SMM Control (SMM_CTL)
533	MSR0000_0414: MC5 Machine Check Control (MC5_CTL)	567	MSRC001_0117: Virtual Machine Host Save Physical Address (VM_HSAVE_PA)
533	MSR0000_0415: MC5 Machine Check Status (MC5_STATUS)	567	MSRC001_0118: SVM Lock Key
534	MSR0000_0416: MC5 Machine Check Address (MC5_ADDR)	568	MSRC001_011A: Local SMI Status
534	MSR0000_0417: MC5 Machine Check Miscellaneous (MC5_MISC)	568	MSRC001_0140: OS Visible Work-around MSR0 (OSVW_ID_Length)
536	MSRC000_0080: Extended Feature Enable (EFER)	568	MSRC001_0141: OS Visible Work-around MSR1 (OSVW_Status)
536	MSRC000_0081: SYSCALL Target Address (STAR)	568	MSRC001_023[6,4,2,0]: L2I Performance Event Select (L2I_PERF_CTL[3:0])
536	MSRC000_0082: Long Mode SYSCALL Target Address (STAR64)	570	MSRC001_023[7,5,3,1]: L2I Performance Event Counter (L2I_PERF_CTR[3:0])
537	MSRC000_0083: Compatibility Mode SYSCALL Target Address (STARCOMPAT)	570	MSRC001_024[6,4,2,0]: Northbridge Performance Event Select (NB_PERF_CTL[3:0])
537	MSRC000_0084: SYSCALL Flag Mask (SYSCALL_FLAG_MASK)	571	MSRC001_024[7,5,3,1]: Northbridge Performance Event Counter (NB_PERF_CTR[3:0])
537	MSRC000_0100: FS Base (FS_BASE)	572	MSRC001_1004: CPUID Features (Features)
537	MSRC000_0101: GS Base (GS_BASE)	573	MSRC001_1005: Extended CPUID Features (ExtFeatures)
537	MSRC000_0102: Kernel GS Base (KernelGSbase)	575	MSRC001_101[B:9]: Address Mask For DR[3:1] Breakpoints
537	MSRC000_0103: Auxiliary Time Stamp Counter (TSC_AUX)	575	MSRC001_1020: Load-Store Configuration (LS_CFG)
538	MSRC000_0104: Time Stamp Counter Ratio (TscRateMsr)	576	MSRC001_1021: Instruction Cache Configuration (IC_CFG)
538	MSRC000_0408: NB Machine Check Misc 4 (Link Thresholding) 1 (MC4_MISC1)	576	MSRC001_1022: Data Cache Configuration (DC_CFG)
540	MSRC000_0409: Reserved	576	MSRC001_1023: Bus Unit Configuration (BU_CFG)
541	MSRC000_040[F:A]: Reserved	576	MSRC001_1027: Address Mask For DR0 Breakpoints (DR0_ADDR_MASK)
542	MSRC001_00[03:00]: Performance Event Select (PERF_CTL[3:0])	577	MSRC001_1028: Floating Point Configuration (FP_CFG)
543	MSRC001_00[07:04]: Performance Event Counter (PERF_CTR[3:0])	577	MSRC001_102A: Bus Unit Configuration 2 (BU_CFG2)
544	MSRC001_0010: System Configuration (SYS_CFG)	577	MSRC001_1030: IBS Fetch Control (IbsFetchCtl)
545	MSRC001_0015: Hardware Configuration (HWCR)	578	MSRC001_1031: IBS Fetch Linear Address (IbsFetchLinAd)
547	MSRC001_00[18,16]: IO Range Base (IORR_BASE[1:0])	578	MSRC001_1032: IBS Fetch Physical Address (IbsFetchPhysAd)
547	MSRC001_00[19,17]: IO Range Mask (IORR_MASK[1:0])	579	MSRC001_1033: IBS Execution Control (IbsOpCtl)
548	MSRC001_001A: Top Of Memory (TOP_MEM)	580	MSRC001_1034: IBS Op Logical Address (IbsOpRip)
548	MSRC001_001D: Top Of Memory 2 (TOM2)	580	MSRC001_1035: IBS Op Data (IbsOpData)
548	MSRC001_001F: Northbridge Configuration 1 (NB_CFG1)	581	MSRC001_1036: IBS Op Data 2 (IbsOpData2)
549	MSRC001_0022: Machine Check Exception Redirection		
549	MSRC001_00[35:30]: Processor Name String		
550	MSRC001_003E: Hardware Thermal Control (HTC)		
551	MSRC001_0044: DC Machine Check Control Mask (MC0_CTL_MASK)		
551	MSRC001_0045: IC Machine Check Control Mask (MC1_CTL_MASK)		

581	MSRC001_1037: IBS Op Data 3 (IbsOpData3)	597	PMCx0C3: Retired Mispredicted Branch Instructions
583	MSRC001_1038: IBS DC Linear Address (IbsDcLinAd)	597	PMCx0C4: Retired Taken Branch Instructions
583	MSRC001_1039: IBS DC Physical Address (IbsDcPhysAd)	598	PMCx0C5: Retired Taken Branch Instructions Mispredicted
583	MSRC001_103A: IBS Control	598	PMCx0C6: Retired Far Control Transfers
584	MSRC001_103B: IBS Branch Target Address (BP_IBSTGT_RIP)	598	PMCx0C7: Retired Branch Resyncs
584	MSRC001_1090: Processor Feedback Constants 0 (CU_PROCFB_SCALE_0)	598	PMCx0C8: Retired Near Returns
584	MSRC001_10A0: L2I Configuration (L2I_CFG)	598	PMCx0C9: Retired Near Returns Mispredicted
586	PMCx000: Dispatched FPU Operations	598	PMCx0CA: Retired Mispredicted Taken Branch Instructions due to Target Mismatch
586	PMCx001: FP Scheduler Empty	598	PMCx0CB: Retired MMX/FP Instructions
586	PMCx002: Dispatched Fast Flag FPU Operations	598	PMCx0CD: Interrupts-Masked Cycles
586	PMCx003: Retired SSE/AVX Operations	598	PMCx0CE: Interrupts-Masked Cycles with Interrupt Pending
587	PMCx005: Retired Serializing Ops	599	PMCx0CF: Interrupts Taken
587	PMCx011: Retired x87 Floating Point Operations	599	PMCx0DB: FPU Exceptions
587	PMCx020: Segment Register Loads	599	PMCx0D[F:C]: DR[3:0] Breakpoint Matches
587	PMCx021: Pipeline Restart Due to Self-Modifying Code	599	PMCx1CF: Tagged IBS Ops
588	PMCx022: Pipeline Restart Due to Probe Hit	599	PMCx1D0: Tagged IBS Ops Retired
588	PMCx024: Locked Operations	600	L2IPMCx060: Command Related to Victim Buffers
588	PMCx026: Retired CLFLUSH Instructions	600	L2IPMCx061: Command Related to Masked Operations
588	PMCx027: Retired CPUID Instructions	600	L2IPMCx062: Command Related to Read Block Operations
588	PMCx029: LS Dispatch	600	L2IPMCx063: Command Related to Change to Dirty Operations
588	PMCx02A: Canceled Store to Load Forward Operations	601	L2IPMCx06C: Response From System on Cache Refills
589	PMCx040: Data Cache Accesses	601	L2IPMCx07D: Requests to L2 Cache
589	PMCx041: Data Cache Misses	601	L2IPMCx07E: L2 Cache Misses
589	PMCx042: Data Cache Refills from L2 or Northbridge	602	L2IPMCx07F: L2 Fill/Writeback
589	PMCx043: Data Cache Refills from the northbridge	602	NBPMCx0E4: Memory Controller Bypass Counter Saturation and DCQ Occupancy
590	PMCx044: Data Cache Lines Evicted	602	NBPMCx0E8: Thermal Status
590	PMCx045: L1 DTLB Miss and L2 DTLB Hit	603	NBPMCx0E9: CPU/IO Requests to Memory/IO
590	PMCx046: DTLB Miss	603	NBPMCx0EA: Cache Block Commands
590	PMCx047: Misaligned Accesses	604	NBPMCx0EB: Sized Commands
590	PMCx04B: Prefetch Instructions Dispatched	604	NBPMCx0EC: Probe Responses and Upstream Requests
591	PMCx04C: DCACHE Misses by Locked Instructions	605	NBPMCx1E0: CPU to DRAM Requests to Target Node
591	PMCx04D: L1 DTLB Hit	605	NBPMCx1E1: IO to DRAM Requests to Target Node
591	PMCx052: Ineffective Software Prefetches	606	NBPMCx1E2: CPU Read Command Latency to Target Node 0-3
591	PMCx054: Global Page Invalidations	606	NBPMCx1E3: CPU Read Command Requests to Target Node 0-3
591	PMCx062: Command Related to Read Block Operations	606	NBPMCx1E4: CPU Read Command Latency to Target Node 4-7
592	PMCx063: Command Related to Change to Dirty Operations	607	NBPMCx1E5: CPU Read Command Requests to Target Node 4-7
592	PMCx065: Memory Requests by Type	607	NBPMCx1E6: CPU Command Latency to Target Node 0-3/4-7
592	PMCx067: Data Cache Prefetches	608	NBPMCx1E7: CPU Requests to Target Node 0-3/4-7
593	PMCx068: MAB Requests	608	NBPMCx1EB: Request Cache Status 1
593	PMCx069: MAB Wait Cycles	608	NBPMCx1F0: Memory Controller Requests
593	PMCx06C: System Response by Coherence State	609	NBPMCx3EC: DRAM Accesses
594	PMCx06D: Data Written to System	609	NBPMCx3ED: DRAM Controller Page Table Overflows
594	PMCx075: Cache Cross-invalidates	610	NBPMCx3EE: Memory Controller DRAM Command Slots Missed
594	PMCx076: CPU Clocks not Halted	610	NBPMCx3EF: Memory Controller Turnarounds
595	PMCx162: PDC Miss	611	IO000: Dma_Ch 0
595	PMCx080: Instruction Cache Fetches	611	IO002: Dma_Ch 1
595	PMCx081: Instruction Cache Misses	611	IO004: Dma_Ch 2
595	PMCx082: Instruction Cache Refills from L2	611	IO006: Dma_Ch 3
595	PMCx083: Instruction Cache Refills from System	611	IO008: Dma_Status
596	PMCx084: L1 ITLB Miss, L2 ITLB Hit	611	IO009: Dma_WriteRequest
596	PMCx085: ITLB Miss	611	IO00A: Dma_WriteMask
596	PMCx087: Instruction Fetch Stall	612	IO00B: Dma_WriteMode
596	PMCx088: Return Stack Hits	612	IO00C: Dma_Clear
596	PMCx089: Return Stack Overflows	612	IO00D: Dma_MasterClr
596	PMCx08B: Instruction Cache Victims	612	IO00E: Dma_ClrMask
596	PMCx08C: Instruction Cache Lines Invalidated	612	IO00F: Dma_AllMask
597	PMCx099: ITLB Reloads	612	IO020: IntrCntrl1Reg1
597	PMCx09A: ITLB Reloads Aborted	612	IO021: IntrCntrl1Reg2
597	PMCx19A: Retired Indirect Branch Info	613	IO022: IMCR_Index
597	PMCx0C0: Retired Instructions	613	IO023: IMCR_Data
597	PMCx0C1: Retired uops	613	IO040: TimerCh0
597	PMCx0C2: Retired Branch Instructions		

613	IO041: TimerCh1	625	IO0DC: Dma_ClrMask
613	IO042: TimerCh2	625	IO0DE: Dma_AllMask
613	IO043: Tmr1CntrlWord	625	IO0F0: NCP Error
614	IO060: Keyboard Data	625	IO4D0: IntrEdgeControl
614	IO061: Nmi Status	626	IOC00: Pci_Intr_Index
614	IO064: Keyboard Status/Control	626	IOC01: Pci_Intr_Data
615	IO070: RtcAddrPort and NmiMask	627	IOC01_x0[7:0]: PCI INT[H#,G#,F#,E#,D#,C#,B#,A#] Map
615	IO071: RtcDataPort	627	IOC01_x08: Intr Misc Map
615	IO072: Alternate RTC AddrPort	627	IOC01_x09: Intr Misc 0 Map
615	IO073: Alternate RTC DataPort	628	IOC01_x0A: IntrMisc1Map
615	IO073_x00: RTC Seconds	628	IOC01_x0B: IntrMisc2Map
616	IO073_x01: RTC Seconds Alarm	628	IOC01_x0[7F:C]: PCI Interrupt Map
616	IO073_x02: RTC Minutes	628	IOC14: Pci_Error
616	IO073_x03: RTC Minutes Alarm	629	IOCD0: PM2_Index
616	IO073_x04: RTC Hours	629	IOCD1: PM2_Data
616	IO073_x05: RTC Hours Alarm	629	IOCD4: BIO SRAMIndex
617	IO073_x06: RTC Day of Week	629	IOCD5: BIO SRAM Data
617	IO073_x07: RTC Date of Month	629	IOCD6: PM_Index
617	IO073_x08: RTC Month	629	IOCD7: PM_Data
617	IO073_x09: RTC Year	629	IOCF9: System Reset Register
617	IO073_x0A: RTC Register A	631	ABx00: AB Index Register
618	IO073_x0B: RTC Register B	631	ABx04: AB Data Register
619	IO073_x0C: RTC Register C	631	ABx04_x54: Misc Control 1
619	IO073_x0D: RTC Date Alarm	632	ABx04_x58: B-Link RAB Control
619	IO073_x32: RTC AltCentury	632	ABx04_x80: B-Link DMA Prefetch Control
619	IO073_x48: RTC Century	632	ABx04_x90: BIF Control 0
620	IO073_x50: RTC Extended RAM Address Port	632	ABx04_x94: MSI Control
620	IO073_x53: RTC Extended RAM Data Port	633	ABx04_x204: SBG Upstream Control
620	IO073_x7E: RTC Time Clear	633	ABx04_x10054: A-Link Arbitration Control and Clock Control (AL_Arb_Ctl, AL_Clk_Ctl)
620	IO073_x7F: RTC RAM Enable	633	ABx04_x10090: Misc Control 3
620	IO080: PostCode	634	D11F0x00: Device/Vendor ID
620	IO081: Dma_PageCh2	634	D11F0x04: Status/Command
621	IO082: Dma_PageCh3	635	D11F0x08: Revision ID/Class Code
621	IO083: Dma_PageCh1	636	D11F0x0C: Header Type Register
621	IO084: Dma_Page_Reserved1	637	D11F0x10: Primary IDE CS0 Base Address (BAR0)
621	IO085: Dma_Page_Reserved2	637	D11F0x14: Primary IDE CS1 Base Address (BAR1)
621	IO086: Dma_Page_Reserved3	637	D11F0x18: Secondary IDE CS0 Base Address (BAR2)
621	IO087: Dma_PageCh0	637	D11F0x1C: Secondary IDE CS1 Base Address (BAR3)
621	IO088: Dma_Page_Reserved4	638	D11F0x20: Bus Master Interface Register Base Address (BAR4)
621	IO089: Dma_PageCh6	638	D11F0x24: AHCI Base Address (BAR5)
622	IO08A: Dma_PageCh7	638	D11F0x2C: Subsystem ID and Subsystem Vendor ID
622	IO08B: Dma_PageCh5	638	D11F0x34: Capabilities Pointer
622	IO08C: Dma_Page_Reserved5	638	D11F0x3C: Interrupt Line
622	IO08D: Dma_Page_Reserved6	639	D11F0x40: Misc Control
622	IO08E: Dma_Page_Reserved7	639	D11F0x44: Watch Dog Control And Status
622	IO08F: Dma_Refresh	640	D11F0x50: MSI Control
622	IO092: FastInit	640	D11F0x54: MSI Address
623	IO0A0: IntrCntrl2Reg1	640	D11F0x58: MSI Upper Address
623	IO0A1: IntrCntrl2Reg2	640	D11F0x5C: MSI Data
623	IO0C0: Dma2_Ch4Addr	641	D11F0x60: Power Management Capability
623	IO0C2: Dma2_Ch4Cnt	641	D11F0x64: PCI Power Management Control And Status
623	IO0C4: Dma2_Ch5Addr	642	D11F0x70: Serial ATA Capability Register 0
623	IO0C6: Dma2_Ch5Cnt	642	D11F0x74: Serial ATA Capability Register 1
623	IO0C8: Dma2_Ch6Addr	643	D11F0x78: IDP Index Register
624	IO0CA: Dma2_Ch6Cnt	643	D11F0x7C: IDP Data Register
624	IO0CC: Dma2_Ch7Addr	643	D11F0x7C_x00: HBA Capabilities (CAP)
624	IO0CE: Dma_Ch7Cnt	643	D11F0x7C_x04: Global HBA Control (GHC)
624	IO0D0: Dma_Status	643	D11F0x7C_x08: Interrupt Status (IS)
624	IO0D2: Dma_WriteRequest	643	D11F0x7C_x0C: Ports Implemented (PI)
624	IO0D4: Dma_WriteMask	644	D11F0x7C_x10: AHCI Version (VS)
624	IO0D6: Dma_WriteMode	644	D11F0x7C_x14: Command Completion Coalescing Control (CCC_CTL)
624	IO0D8: Dma_Clear		
625	IO0DA: Dma_MasterClr		

644	D11F0x7C_x18: Command Completion Coalescing Ports (CCC_PORTS)	662	SATAx1[8,0]C: Port 1,0 FIS Base Address Upper (PxFBU)
644	D11F0x7C_x1C: Enclosure Management Location (EM_LOC)	662	SATAx1[9,1]0: Port 1,0 Interrupt Status (PxIS)
644	D11F0x7C_x20: Enclosure Management Control (EM_CTL)	664	SATAx1[9,1]4: Port 1,0 Interrupt Enable (PxIE)
644	D11F0x7C_x24: HBA Capabilities Extended (CAP2)	665	SATAx1[9,1]8: Port 1,0 Command and Status (PxCMD)
644	D11F0x7C_x28: BIOS/OS Handoff Control and Status (BOHC)	667	SATAx1[A,2]0: Port 1,0 Task File Data (PxTFD)
644	D11F0x7C_x1[8,0]0: Port 1,0 Command List Base Address (PxCLB)	668	SATAx1[A,2]4: Port 1,0 Signature (PxSIG)
645	D11F0x7C_x1[8,0]4: Port 1,0 Command List Base Upper Address (PxCLBU)	668	SATAx1[A,2]8: Port 1,0 Serial ATA Status (PxSSTS)
645	D11F0x7C_x1[8,0]8: Port 1,0 FIS Base Address (PxFB)	669	SATAx1[A,2]C: Port 1,0 Serial ATA Control (PxSCTL)
645	D11F0x7C_x1[8,0]C: Port 1,0 FIS Base Address Upper (PxFBU)	671	SATAx1[B,3]0: Port 1,0 Serial ATA Error(PxSERR)
645	D11F0x7C_x1[9,1]0: Port 1,0 Interrupt Status (PxIS)	673	SATAx1[B,3]4: Port 1,0 Serial ATA Active (PxSACT)
645	D11F0x7C_x1[9,1]4: Port 1,0 Interrupt Enable (PxIE)	674	SATAx1[B,3]8: Port 1,0 Command Issue (PxCI)
645	D11F0x7C_x1[9,1]8: Port 1,0 Command and Status (PxCMD)	674	SATAx1[B,3]C: Port 1,0 SNotification (PxSNTF)
645	D11F0x7C_x1[A,2]0: Port 1,0 Task File Data (PxTFD)	674	SATAx1[C,4]0: Port 1,0 FIS-based Switching Control (PxFBS)
645	D11F0x7C_x1[A,2]4: Port 1,0 Signature (PxSIG)	675	SATAx1[C,4]4: Port 1,0 Device Sleep (PxDEVSLP)
646	D11F0x7C_x1[A,2]8: Port 1,0 Serial ATA Status (PxSSTS)	676	SATA_EMx00: Message Header
646	D11F0x7C_x1[A,2]C: Port 1,0 Serial ATA Control (PxSCTL)	677	SATA_EMx04: Write SGPIO Register Request (I)
646	D11F0x7C_x1[B,3]0: Port 1,0 Serial ATA Error (PxSERR)	678	SATA_EMx08: Write SGPIO Register Request (II)
646	D11F0x7C_x1[B,3]4: Port 1,0 Serial ATA Active (PxSACT)	678	SATA_EMx0C: Write SGPIO Register Request (III)
646	D11F0x7C_x1[B,3]8: Port 1,0 Command Issue (PxCI)	679	D[16,13,12]F0x00: Device/Vendor ID
646	D11F0x7C_x1[B,3]C: Port 1,0 SNotification (PxSNTF)	679	D[16,13,12]F0x04: Status/Command
646	D11F0x7C_x1[C,4]0: Port 1,0 FIS-based Switching Control (PxFBS)	680	D[16,13,12]F0x08: Class Code/Revision ID
646	D11F0x80: PHY Core Control 1	680	D[16,13,12]F0x0C: Miscellaneous
647	D11F0x84: PHY Core Control 2	681	D[16,13,12]F0x10: OHCI Base Address
647	D11F0x88: PHY Global Control 1	681	D[16,13,12]F0x2C: Subsystem and Subvendor ID
648	D11F0x8C: PHY Global Control 2	681	D[16,13,12]F0x34: Capabilities Pointer
648	D11F0x98: PHY Fine Tune PortX GenX Setting	681	D[16,13,12]F0x3C: Interrupt Line
648	D11F0x9C: PortX Setting 2	681	D[16,13,12]F0x40: Miscellaneous 2
648	D11F0xB4: PortX BIST Control/Status	682	D[16,13,12]F0x44: USB Battery Charger
649	D11F0xB7: PortX BIST Port Select	682	D[16,13,12]F0x48: Port Force Reset
650	D11F0xBC: T-Mode BIST Transit Pattern DW1	682	D[16,13,12]F0x50: OHCI Misc Control
650	D11F0xC0: T-Mode BIST Transit Pattern DW2	683	D[16,13,12]F0x58: Over-Current Control 1
650	D11F0xC4: T-Mode BIST Transit Control	684	D[16,13,12]F0x68: OHCI Over-Current PME Enable
650	D11F0xD0: Advanced Features Capability Register 0	684	D[16,13,12]F0x74: Target Timeout Control
651	D11F0xD4: Advanced Features Capability Register 1	684	D[16,13,12]F0x80: OHCI Spare 1
651	D11F0xE0: PCI Target Control TimeOut Counter	685	D[16,13,12]F0xD0: MSI Control
652	IDE[1:0]x00: IDE DATA	685	D[16,13,12]F0xD4: MSI Address
652	IDE[1:0]x01: Feature and Error	685	D[16,13,12]F0xD8: MSI Data
652	IDE[1:0]x02: Sector Count	686	D[16,13,12]F0xE4: HT MSI Support
652	IDE[1:0]x03: Sector Number	686	D[16,13,12]F0xF0: Function Level Reset Capability
652	IDE[1:0]x04: Cylinder Low	686	D[16,13,12]F0xF4: Function Level Reset Control
653	IDE[1:0]x05: Cylinder High	687	OHCI[3:1]x00: HC Revision
653	IDE[1:0]x06: Drive and Head	687	OHCI[3:1]x04: HC Control
653	IDE[1:0]x07: Command and Status	688	OHCI[3:1]x08: HC Command Status
653	IDEA[1:0]x02: Device Control and Alternate Status	689	OHCI[3:1]x0C: HC Interrupt Status
653	IDE_BMx0[8,0]: Bus Master IDE Command	690	OHCI[3:1]x10: HC Interrupt Enable
654	IDE_BMx0[A,2]: Bus-master IDE Status	690	OHCI[3:1]x14: HC Interrupt Disable
654	IDE_BMx0[C,4]: Descriptor Table Pointer	691	OHCI[3:1]x18: HC HCCA
655	SATAx00: HBA Capabilities (CAP)	691	OHCI[3:1]x1C: HC Period Current ED
657	SATAx04: Global HBA Control (GHC)	691	OHCI[3:1]x20: HC Control Head ED
658	SATAx08: Interrupt Status (IS)	691	OHCI[3:1]x24: HC Control Current ED
658	SATAx0C: Ports Implemented (PI)	691	OHCI[3:1]x28: HC Bulk Head ED
658	SATAx10: AHCI Version (VS)	692	OHCI[3:1]x2C: HC BulkCurrent ED
658	SATAx14: Command Completion Coalescing Control (CCC_CTL)	692	OHCI[3:1]x30: HC Done Head
659	SATAx18: Command Completion Coalescing Ports (CCC_PORTS)	692	OHCI[3:1]x34: HC Frame Interval
659	SATAx1C: Enclosure Management Location (EM_LOC)	692	OHCI[3:1]x38: HC Frame Remaining
660	SATAx20: Enclosure Management Control (EM_CTL)	693	OHCI[3:1]x3C: HC Frame Number
661	SATAx24: HBA Capabilities Extended (CAP2)	693	OHCI[3:1]x40: HC Periodic Start
661	SATAx28: BIOS/OS Handoff Control and Status (BOHC)	693	OHCI[3:1]x44: HC LS Threshold
662	SATAx1[8,0]0: Port 1,0 Command List Base Address (PxCLB)	693	OHCI[3:1]x48: HC RH Descriptor A
662	SATAx1[8,0]4: Port 1,0 Command List Base Upper Address (PxCLBU)	694	OHCI[3:1]x4C: HC RH Descriptor B
662	SATAx1[8,0]8: Port 1,0 FIS Base Address (PxFB)	695	OHCI[3:1]x50: HC RH Status
662	SATAx1[8,0]C: Port 1,0 FIS Base Address Upper (PxFBU)	696	OHCI[3:1]x[60:54:step4]: HC RH Port Status [4:1]
662	SATAx1[8,0]F0: HC Loopback Control	698	

699	OHCI[3:1]x100: HCE Control	729	D10F0x4C_x14: USB DCLK Event Counter 1
699	OHCI[3:1]x104: HCE Input	729	D10F0x4C_x18: USB DCLK Event Counter Select
699	OHCI[3:1]x108: HCE Output	730	D10F0x4C_x1C: USB DCLK Event Counter Control
700	OHCI[3:1]x10C: HCE Status	730	D10F0x4C_x4000_0000: UTMI Control
700	D[16,13,12]F2x00: Device/Vendor ID	730	D10F0x4C_x4000_0004: USB PHY Status
700	D[16,13,12]F2x04: Status/Command	731	D10F0x4C_x4000_0008: USB Common PHY Calibration and Control
702	D[16,13,12]F2x08: Revision ID / Class Code	731	D10F0x4C_x4000_000C: USB Common PHY Control
702	D[16,13,12]F2x0C: Miscellaneous	732	D10F0x4C_x4000_0010: HS Loopback Test
702	D[16,13,12]F2x10: BAR_EHCI	732	D10F0x4C_x4000_0014: CL Loopback Control
702	D[16,13,12]F2x2C: Subsystem ID / Subsystem Vendor ID	733	D10F0x4C_x4000_0018: Misc Control
703	D[16,13,12]F2x34: Capability Pointer	733	D10F0x4C_x4000_0020: USB SCLK Event Counter 0
703	D[16,13,12]F2x3C: Interrupt Line	733	D10F0x4C_x4000_0024: USB SCLK Event Counter 1
703	D[16,13,12]F2x50: EHCI Misc Control	734	D10F0x4C_x4000_0028: USB SCLK Event Counter Select
704	D[16,13,12]F2x54: EHCI Spare 1	734	D10F0x4C_x4000_002C: USB SCLK Event Counter Control
705	D[16,13,12]F2x60: Serial Bus Release Number / FLADJ	734	D10F0x4C_x4000_0048: LPM Control
705	D[16,13,12]F2xA0: USB Legacy Support Extended Capability	735	D10F0x4C_x4000_0050: USB Common PHY Control 2
706	D[16,13,12]F2xA4: USB Legacy Support Control / Status	735	D10F0x4C_x4000_0054: USB Common PHY Control 3
707	D[16,13,12]F2xC0: PME Capability	735	D10F0x50: PME Capability
707	D[16,13,12]F2xC4: PME Control / Status	736	D10F0x54: PME Control / Status
708	D[16,13,12]F2xD0: MSI Control	737	D10F0x60: SBRN
708	D[16,13,12]F2xD4: MSI Address	738	D10F0x70: MSI Control
708	D[16,13,12]F2xD8: MSI Upper Address	738	D10F0x74: MSI Address
708	D[16,13,12]F2xDC: MSI Data	738	D10F0x78: MSI Upper Address
709	D[16,13,12]F2xF0: Function Level Reset Capability	738	D10F0x7C: MSI Data
709	D[16,13,12]F2xF4: Function Level Reset Control	739	D10F0x80: MSI Mask Bits
710	EHCI[3:1]x00: Capability Length	739	D10F0x90: MSI-X Control
710	EHCI[3:1]x02: HC Interface Version	739	D10F0x94: MSI-X Table Offset/Table BIR
710	EHCI[3:1]x04: HC Structural Parameters	739	D10F0x98: MSI-X PBA Offset/PBA BIR
711	EHCI[3:1]x08: HC Capability Parameters	740	D10F0xA0: PCIe Capability List
712	EHCI[3:1]x20: USB Command	740	D10F0xA4: Device Capability
714	EHCI[3:1]x24: USB Status	741	D10F0xA8: Device Control/Status
716	EHCI[3:1]x28: USB Interrupt Enable	742	D10F0xC4: Device Capabilities 2
717	EHCI[3:1]x2C: Frame Index	743	D10F0xC8: Device Control/Status 2
717	EHCI[3:1]x30: Control Data Structure Segment	743	D10F0x100: LTR Extended Capability Header
717	EHCI[3:1]x34: Periodic Frame List Base Address	743	D10F0x104: Max Latency
717	EHCI[3:1]x38: Current Async List Address	744	XHCI_CAPx02: HC Interface Version
718	EHCI[3:1]x60: Configure Flag	744	XHCI_PMx00: xHCI Config 0
718	EHCI[3:1]x[70,6C,68,64]: Port Status Control [4:1]	745	XHCI_PMx04: xHCI Firmware Addr 0
720	EHCI[3:1]xA4: Packet Buffer Threshold Values	745	XHCI_PMx08: xHCI Firmware Addr 1
721	EHCI[3:1]xB4: UTMI Control	745	XHCI_PMx10: xHCI Memory Config
721	EHCI[3:1]xB8: Loopback Test	746	XHCI_PMx14: PLL Control
722	EHCI[3:1]xBC: EOR MISC Control	746	XHCI_PMx20: USB2.0 Wake Control
723	EHCI[3:1]xC0: USB Common PHY CAL and Control	746	XHCI_PMx30: xHCI 1.0 Enable
723	EHCI[3:1]xC4: USB Common PHY Control 1	747	XHCI_PMx48: SSPHY ACPI Indirect Index
724	EHCI[3:1]xD0: USB Common PHY Control 2	747	XHCI_PMx4C: SSPHY ACPI IndirectData
724	EHCI[3:1]xD4: USB Common PHY Control 3	748	XHCI_PMx8C: SSPHY Common Control 0
724	EHCI[3:1]xDC: USB Battery Charger Enable	748	XHCI_PMxA0: SPI BAR0
725	D10F0x00: Device/Vendor ID	748	XHCI_PMxA4: SPI BAR1
725	D10F0x04: Status/Command	748	XHCI_PMxA8: SPI BAR2
726	D10F0x08: Revision ID / Class Code	748	XHCI_PMxAC: SPI BAR3
726	D10F0x0C: Miscellaneous	748	XHCI_PMxB0: SPI Valid Base
727	D10F0x10: Bar 0	749	XHCI_PMxB4: SPI Misc
727	D10F0x14: Bar 1	749	XHCI_PMx[FC:C0]: SPI Data Block N
727	D10F0x2C: Subsystem Vendor ID / Subsystem ID	750	D14F2x00: Device/Vendor ID
727	D10F0x34: Capability Pointer	750	D14F2x04: Status/Command
727	D10F0x3C: Interrupt Line	750	D14F2x08: Class Code/Revision ID
728	D10F0x40: IDP Index Register	751	D14F2x0C: Header Type
728	D10F0x44: IDP Data Register	751	D14F2x10: Lower Base Address Register
728	D10F0x48: Indirect PCI Index Register	751	D14F2x14: Upper Base Address Register
728	D10F0x4C: Indirect PCI Data Register	751	D14F2x2C: Subsystem and Subvendor ID
729	D10F0x4C_x08: Port Disable Write Once	752	D14F2x34: Capabilities Pointer
729	D10F0x4C_x0C: Port Disable RW	752	D14F2x3C: Interrupt Line
729	D10F0x4C_x10: USB DCLK Event Counter 0	752	D14F2x40: Misc Control

753	D14F2x44: Interrupt Pin/Capability/Debug Control	780	D14F0x34: Capability Pointer
753	D14F2x50: Power Management Capability	780	D14F0x3C: Interrupt Line
754	D14F2x54: Power Management Control and Status	780	ASFx00: HostStatus
754	D14F2x60: MSI Capability	781	ASFx02: HostControl
755	D14F2x64: MSI Message Address Low	781	ASFx03: HostCommand
755	D14F2x68: MSI Message Address High	781	ASFx04: SlaveAddress
755	D14F2x6C: MSI Message Data	781	ASFx05: Data0
755	D14F2x70: Advanced Features Capability	782	ASFx06: Data1
756	D14F2x74: Advanced Features Control and Status	782	ASFx07: DataIndex
757	D14F7x00: Device/Vendor ID	782	ASFx08: PEC
757	D14F7x04: Status/Command	782	ASFx09: ListenAdr
758	D14F7x08: Revision ID/Class Code	782	ASFx0A: ASFStatus
758	D14F7x0C: Cache Line Size	783	ASFx0B: StatusMask0
758	D14F7x10: Base Address Reg 0	783	ASFx0C: StatusMask1
759	D14F7x14: Upper Base Address Reg 0	783	ASFx0D: SlaveStatus
759	D14F7x2C: Subsystem ID and Subsystem Vendor ID	783	ASFx0E: RemoteCtrlAdr
759	D14F7x34: Capabilities Pointer	783	ASFx0F: SensorAdr
759	D14F7x3C: Interrupt Line	783	ASFx10: DataReadPointer
759	D14F7x40: Slot Information	784	ASFx11: DataWritePointer
760	D14F7x80: SD PCI MSI Capability Header	784	ASFx12: SetDataReadPointer
760	D14F7x84: SD PCI MSI Address	784	ASFx13: DataBaseSel
760	D14F7x88: SD PCI MSI Upper Address	784	ASFx14: Semaphore
760	D14F7x8C: SD PCI MSI Data	785	ASFx15: SlaveEn
761	D14F7x90: Power Management Capability Header	785	ASFx16: DelayMasterTimer
761	D14F7x94: Power Management Control and Status Register	785	SMBUSx00: SMBusStatus
762	SDHCx00: SDHC System Address / Argument 2	786	SMBUSx01: SMBusSlaveStatus
762	SDHCx04: SDHC Block CS	786	SMBUSx02: SMBusControl
763	SDHCx08: SDHC Command Argument	787	SMBUSx03: SMBusHostCmd
763	SDHCx0C: SDHC Command/Transfer Mode	787	SMBUSx04: SMBusAddress
764	SDHCx10: SDHC_RESP1_0	787	SMBUSx05: SMBusData0
764	SDHCx14: SDHC_RESP3_2	787	SMBUSx06: SMBusData1
764	SDHCx18: SDHC_RESP5_4	787	SMBUSx07: SMBusBlockData
764	SDHCx1C: SDHC_RESP7_6	788	SMBUSx08: SMBusSlaveControl
764	SDHCx20: SDHC_BUFFER	788	SMBUSx09: SMBusShadowCmd
765	SDHCx24: SDHC_PRSNT_STATE	788	SMBUSx0A: SMBusSlaveEvent
765	SDHCx28: SDHC_CTRL1	789	SMBUSx0C: SlaveData
766	SDHCx2C: SDHC_CTRL2	789	SMBUSx0E: SMBusTiming
767	SDHCx30: SDHC_INT_STATUS	789	SMBUSx10: I2CbusConfig
769	SDHCx34: SDHC_INT_MASK	789	SMBUSx11: I2CCommand
769	SDHCx38: SDHC_SIG_MASK	789	SMBUSx12: I2CShadow1
770	SDHCx3C: SDHC_ACMD12 Error/Host Control 2	789	SMBUSx13: I2Cshadow2
771	SDHCx40: SDHC_CAPABILITY	790	SMBUSx14: SMBusAutoPoll
772	SDHCx44: SDHC_CAPABILITY 2	790	SMBUSx15: SMBusCounter
773	SDHCx48: SDHC_CURR_CAPABILITY	790	SMBUSx16: SMBusStop
773	SDHCx50: SDHC_FORCE_EVT	791	SMBUSx17: SMBusHostCmd2
774	SDHCx54: SDHC_ADMA_ERR	792	IOAPICx00: IO Register Select Register
774	SDHCx58: SDHC_ADMA_SAD	792	IOAPICx10: IO Window Register
774	SDHCx6[C:0:step4]: Preset Value	792	IOAPICx10_x00: IOAPIC ID Register
775	SDHCxE0: Shared Bus Control Register	792	IOAPICx10_x01: IOAPIC Version Register
776	SDHCxF0: SDHC_VER_SLOT	792	IOAPICx10_x02: IOAPIC Arbitration Register
777	D14F0x00: Device/Vendor ID	793	IOAPICx10_x[3E:10:step2]: Redirection Table Entry [23:0]
777	D14F0x04: Status/Command	793	IOAPICx20: IRQ Pin Assertion Register
778	D14F0x08: Revision ID/Class Code	793	IOAPICx40: EOI Register
778	D14F0x0C: Cache Line Size	794	D14F3x00: Device/Vendor ID
778	D14F0x10: Base Address 0	794	D14F3x04: Status/Command
778	D14F0x14: Base Address 1	795	D14F3x08: Revision ID/Class Code
779	D14F0x18: Base Address 2	795	D14F3x0C: Cache Line Size
779	D14F0x1C: Base Address 3	795	D14F3x10: Base Address Reg 0
779	D14F0x20: Base Address 4	795	D14F3x2C: Subsystem ID and Subsystem Vendor ID
779	D14F0x24: Base Address 5	795	D14F3x34: Capabilities Pointer
779	D14F0x28: Cardbus CIS Pointer	796	D14F3x40: PCI Control
779	D14F0x2C: Subsystem Vendor ID	796	D14F3x44: IO Port Decode Enable
779	D14F0x30: Expansion ROM Base Address	798	D14F3x48: IO/Mem Port Decode Enable

799	D14F3x4C: Memory Range	818	HPETx1[4:0:Step2]8: Timer[2:0] Comparator
799	D14F3x[5C,58,54,50]: ROM Protect 3, 2, 1, 0	820	MISCx00: GPPClkCntrl
799	D14F3x60: PCI Memory Address for LPC Target Cycles	822	MISCx04: ClkOutputCntrl
800	D14F3x64: PCI IO base Address for Wide Generic Port	824	MISCx08: CGPLLConfig1
800	D14F3x68: ROM Address Range 1	825	MISCx0C: CGPLLConfig2
800	D14F3x6C: ROM Address Range 2	826	MISCx10: CGPLLConfig3
801	D14F3x74: Alternative Wide IO Range Enable	826	MISCx14: CGPLLConfig4
801	D14F3x78: Miscellaneous Control Bits	827	MISCx18: CGPLLConfig5
801	D14F3x7C: TPM	827	MISCx1C: CGPLLConfig6
802	D14F3x84: TMKBC_BaseAddrLow	828	MISCx20: IMPCalibration
803	D14F3x88: TMKBC_BaseAddrHigh	830	MISCx24: ClkDrvStr1
803	D14F3x8C: TMKBC_Remap	831	MISCx28: ClkDrvStr2
803	D14F3x90: Wide IO 2	832	MISCx2C: ClkGatedCntrl
803	D14F3x98: EC_LPC_Cntrl	833	MISCx30: CGPLLConfig7
803	D14F3xA0: SPI_Base_Addr	834	MISCx34: CGPLLConfig8
804	D14F3xA4: EC_PortAddress	834	MISCx38: CGPLLConfig9
804	D14F3xB0: RomDmaSrcAddr	834	MISCx3C: CGPLLConfig10
804	D14F3xB4: RomDmaDstAddr	835	MISCx40: MiscClkCntrl1
804	D14F3xB8: RomDmaControl/EcControl/HostControl	836	MISCx44: MiscClkCntrl2
806	D14F3xC0: EcRomWrOffset	837	MISCx48: MiscClkCntrl3
806	D14F3xC4: EcRomRdOffset	838	MISCx4C: MiscClkCntrl4
806	D14F3xC8: ClientRomProtect	838	MISCx60: IdleCntrl
806	D14F3xCC: AutoRomCfg	839	MISCx68: Memory Power Saving Control (MemPwrSavCntrl)
807	D14F3xD0: ClkCntrl	839	MISCx70: OscFreqCounter
807	D14F3xD4: ClkRunOption	839	MISCx74: HpetClkPeriod
808	SPIx00: SPI_Cntrl0	839	MISCx78: PostCode
809	SPIx04: SPI_RestrictedCmd	839	MISCx80: StrapStatus
809	SPIx08: SPI_RestrictedCmd2	840	MISCx90: AutoTransaction/Allow EC
809	SPIx0C: SPI_Cntrl11	841	MISCx94: AutoAddrLow
810	SPIx10: SPI_CmdValue0	841	MISCx98: AutoAddrHigh
810	SPIx14: SPI_CmdValue1	841	MISCx9C: AutoData
811	SPIx18: SPI_CmdValue2	841	MISCxC0: CPU Pstate0
811	SPIx1C: Reserved	842	MISCxC4: CPU Pstate1
811	SPIx1D: Alt_SPI_CS	842	MISCxD0: CPU Cstate0
812	SPIx1E: SpiExtRegIndx	842	MISCxD4: CPU Cstate1
812	SPIx1F: SpiExtRegData	842	MISCxF0: SataPortSts
812	SPIx1F_x00: DDR_CMD	843	MISCxF4: ClkCntrlSts
812	SPIx1F_x01: QDR_CMD	843	GPIOx[E4:00]: GPIO
812	SPIx1F_x02: DPR_CMD	844	IOMUXx[E4:00]: IoMux
812	SPIx1F_x03: QPR_CMD	845	PMx00: DecodeEn
813	SPIx1F_x04: ModeByte	845	PMx04: IsaControl
813	SPIx1F_x05: TxByteCount	846	PMx08: PciControl
813	SPIx1F_x06: RxByteCount	847	PMx0C: StpClkSmf
813	SPIx1F_x07: SPIDataFifoPtr	847	PMx20: BiosRamEn
813	SPIx20: SPI100 Enable	847	PMx24: AcpiMmioEn
813	SPIx22: SPI100 Speed Config	848	PMx28: AsfEn
814	SPIx40: DDRCmdCode	849	PMx2C: Smbus0En
814	SPIx41: QDRCmdCode	849	PMx2E: Smbus0Sel
814	SPIx42: DPRCmdCode	849	PMx2F: SmbusSlpGate
815	SPIx43: QPRCcmdCode	849	PMx34: IoApicEn
815	SPIx44: ModeByte	850	PMx44: BootTimerEn
815	SPIx45: CmdCode	850	PMx48: WatchdogTimerEn
815	SPIx47: CmdTrigger	850	PMx4C: WatchdogTimerConfig
815	SPIx48: TxByteCount	851	PMx50: HPETEn
815	SPIx4B: RxByteCount	851	PMx54: SerialIrqConfig
815	SPIx4C: SpiStatus	851	PMx56: RTC Control
816	SPIx[C6:80]: FIFO[70:0]	852	PMx58: VRT_T1
817	HPETx000: ID	852	PMx59: VRT_T2
817	HPETx004: ClkPeriod	852	PMx5B: RTC Shadow
817	HPETx010: Config	853	PMx5C: LLBCntrl
817	HPETx020: Interrupt Status	853	PMx5E: RTC ExtIndex
818	HPETx0F0: Main Counter	853	PMx5F: RTC ExtData
818	HPETx1[4:0:Step2]0: Timer[2:0] Config Capability	853	PMx5F_x00: RTCEXT DltSavEnable

853	PMx5F_x01: RTCEXT SprFwdCtrl	874	PMxEF: USB Enable
854	PMx5F_x02: RTCEXT SprFwdMonth	875	PMxF0: USB Control
854	PMx5F_x03: RTCEXT FallBackCtrl	876	PM2x00: Fan0InputControl
854	PMx5F_x04: RTCEXT FallBackMonth	876	PM2x01: Fan0Control
854	PMx5F_x10: RTCEXT WeekTimerControl	877	PM2x02: Fan0Freq
855	PMx5F_x11: RTCEXT WeekTimerReloadLow	877	PM2x03: LowDuty0
855	PMx5F_x12: RTCEXT WeekTimerReloadHigh	877	PM2x04: MedDuty0
855	PMx5F_x13: RTCEXT WeekTimerDataLow	878	PM2x05: Multiplier0
855	PMx5F_x14: RTCEXT WeekTimerDataHigh	878	PM2x06: LowTemp0Lo
855	PMx60: AcpnPm1EvtBlk	878	PM2x07: LowTemp0Hi
855	PMx62: AcpnPm1CntBlk	878	PM2x08: MedTemp0Lo
856	PMx64: AcpnPmTmrBlk	879	PM2x09: MedTemp0Hi
856	PMx66: CpuCntBlk	879	PM2x0A: HighTemp0Lo
856	PMx68: AcpGpe0Blk	879	PM2x0B: HighTemp0Hi
856	PMx6A: AcpSmiCmd	879	PM2x0C: LinearRange0
856	PMx6E: AcpnPm2CntBlk	879	PM2x0D: LinearHoldCount0
857	PMx74: AcpConfig	879	PM2x0E: Fan0Hysteresis
857	PMx78: WakeIoAddr	879	PM2x50: Med2Temp0Lo
857	PMx7A: HaltCountEn	880	PM2x51: Med2Temp0Hi
858	PMx7C: C1eWrPortAddr	880	PM2x52: Med2Duty0
858	PMx7E: CStateEn	880	PM2x53: Multiplier2_0
858	PMx80: Break Event	880	PM2x60: FanStatus
859	PMx88: CStateControl	880	PM2x61: FanINTRouteLo
860	PMx8E: PopUpEndTime	881	PM2x63: SampleFreqDiv
860	PMx94: CStateTiming0	881	PM2x64: FanDebounceCounterLo
860	PMx98: CStateTiming1	881	PM2x65: FanDebounceCounterHi
861	PMx9C: C2Count	881	PM2x66: Fan0DetectorControl
861	PMx9D: C3Count	882	PM2x67: Fan0SpeedLimitLo
861	PMxA0: MessageCState	882	PM2x68: Fan0SpeedLimitHi
862	PMxA4: Traffic Monitor and Status	882	PM2x69: Fan0SpeedLo
863	PMxA4_x0: TrafficMonitorEn	882	PM2x6A: Fan0SpeedHi
864	PMxA4_x1: TrafficStatus	882	PM2x8A: TempTsiLo
865	PMxA8: TrafficMonitorIdleTime	882	PM2x8B: TempTsiHi
865	PMxAA: TrafficMonitorIntTime	883	PM2x8C: TempTsiLimitLo
865	PMxAC: TrafficMonitorTrafficCount	883	PM2x8D: TempTsiLimitHi
865	PMxAE: TrafficMonitorIntrCount	883	PM2x8E: TempTsiChangeLimit
865	PMxB0: DeferTimeTick / OBFF Control	883	PM2x8F: TempTsiWe
866	PMxB4: AcpMiscDebug / Tpreset1b	883	PM2x90: TempTsiStatus
866	PMxB8: Tpreset2	884	PM2x92: TempTsiControl
866	PMxB9: LpcMisc	884	PM2x94: TempTsiINTRoute
867	PMxBA: S_StateControl	884	PM2xDF: TempTsiRstSel
867	PMxBC: ThrottlingControl	884	PM2xE0: AlertThermaltripStatus
868	PMxBE: ResetControl1	885	PM2xE1: AlertLimitLo
868	PMxC0: S5/Reset Status	885	PM2xE2: AlertLimitHi
869	PMxC4: ResetCommand	885	PM2xE3: ThermalTripLimitLo
870	PMxC5: CF9 Shadow	885	PM2xE4: ThermalTripLimitHi
870	PMxC8: Misc	885	PM2xE5: AlertThermaltripControl
871	PMxD0: RstCntrl	886	AcpnPmEvtBlkx00: Pm1Status
871	PMxD1: Reset Function	886	AcpnPmEvtBlkx02: Pm1Enable
871	PMxD1_x0: RstLength	887	AcpnPm1CntBlkx00: PmControl
871	PMxD1_x1: APURstLength	887	AcpnPm2CntBlkx00: Pm2Control
872	PMxD1_x3: APUPwrGdLength	888	AcpnPmTmrBlkx00: TmrValue/ETmrValue
872	PMxD3: ManualReset	888	CpuCntBlkx00: ClkValue
872	PMxD6: IMC Gating	888	CpuCntBlkx04: PLvl2
872	PMxD8: Eprom/Efuse Index	888	CpuCntBlkx05: PLvl3
872	PMxD9: Eprom/Efuse Data	889	AcpGpe0Blkx00: EventStatus
873	PMxDA: SataConfig	889	AcpGpe0Blkx04: EventEnable
873	PMxDC: SataConfig2	889	SmiCmdBlkx00: SmiCmdPort
873	PMxE0: ABRegBar	889	SmiCmdBlkx01: SmiCmdStatus
874	PMxE8: SDFlashCntrl	890	SMIx00: Event_Status
874	PMxEB: AzEn	890	SMIx04: Event_Enable
874	PMxEC: LpcGating	890	SMIx08: SciTrig
874	PMxED: USB Gating	892	SMIx0C: SciLevl

893	SMIx10: SmiSciStatus	920	AcDcTimerx04: AcExpiredTimerPolicy
893	SMIx14: SmiSciEn	920	AcDcTimerx08: AcTimerStatus
893	SMIx18: SwSciEn	921	AcDcTimerx10: DcTimerValue
893	SMIx1C: SwSciData	921	AcDcTimerx14: DeExpiredTimerPolicy
893	SMIx20: SciSleepDisable	921	AcDcTimerx18: DcTimerStatus
894	SMIx30: CapturedData	921	AcDcTimerx20: AcDcTimerCtrl
894	SMIx34: CapturedValid		
894	SMIx38: EPBIF_AER_Straps		
895	SMIx3C: DataErrorStatus		
895	SMIx40: SciMap0		
896	SMIx44: SciMap1		
896	SMIx48: SciMap2		
897	SMIx4C: SciMap3		
897	SMIx50: SciMap4		
898	SMIx54: SciMap5		
898	SMIx58: SciMap6		
899	SMIx5C: SciMap7		
899	SMIx60: SciMap8		
899	SMIx64: SciMap9		
899	SMIx68: SciMap10		
900	SMIx6C: SciMap11		
900	SMIx70: SciMap12		
901	SMIx74: SciMap13		
901	SMIx78: SciMap14		
902	SMIx7C: SciMap15		
902	SMIx80: SmiStatus0		
903	SMIx84: SmiStatus1		
904	SMIx88: SmiStatus2		
905	SMIx8C: SmiStatus3		
905	SMIx90: SmiStatus4		
906	SMIx94: SmiPointer		
907	SMIx96: SmiTimer		
907	SMIx98: SmiTrig0		
908	SMIx9C: SmiTrig1		
909	SMIxA0: SmiControl0		
909	SMIxA4: SmiControl1		
910	SMIxA8: SmiControl2		
911	SMIxAC: SmiControl3		
911	SMIxB0: SmiControl4		
912	SMIxB4: SmiControl5		
912	SMIxB8: SmiControl6		
913	SMIxBC: SmiControl7		
914	SMIxC0: SmiControl8		
914	SMIxC4: SmiControl9		
915	SMIxC8: IoTrapping0		
915	SMIxCA: IoTrapping1		
915	SMIxCC: IoTrapping2		
915	SMIxCE: IoTrapping3		
915	SMIxD0: MemTrapping0		
916	SMIxD4: MemRdOvrData0		
916	SMIxD8: MemTrapping1		
916	SMIxDC: MemRdOvrData1		
916	SMIxE0: MemTrapping2		
916	SMIxE4: MemRdOvrData2		
917	SMIxE8: MemTrapping3		
917	SMIxEC: MemRdOvrData3		
917	SMIxF0: CfgTrapping0		
917	SMIxF4: CfgTrapping1		
917	SMIxF8: CfgTrapping2		
918	SMIxFC: CfgTrapping3		
919	WDTx00: WatchdogControl		
919	WDTx04: WatchdogCount		
920	AcDcTimerx00: AcTimerValue		