RTL8762D Hardware Instruction

V1.0

2021/4/25

Revision History

Date	Version	modification	Author
2021/01/25	Draft v0.1	First Draft	

Catalogue

1 Special Instruction

In this document, all the statements that are not specially noted are applicable to all the RTL8762D series ICs. Generally, “RTL8762D” refers to all of these ICs in this document.

2 Feature Table

RTL8762D feature table

	RTL8762DGF	RTL8752DJF RTL8762DJF RTL8762DDF	RTL8762DW	RTL8762DK	RTL8762DKF
package	QFN40	QFN40	QFN56	QFN48	QFN48
Flash type	**internal**	**internal**	external	external	**internal**
VBAT range (1)	1.8~3.3V				
IO number(2)	18(3)	26(3)	38(3)	32(3)	34(3)
AUX ADC channel number(4)	4	6	6	8	8
SPI	2				
UART	2+1(5)				
I2C	2				
IR T/RX	1				
Key scan	1				
I8080 interface	No		1		NO
MIC BIAS	N0	1			
SPIC	0	0	3(6)	1(6)	0

1. With external flash, VBAT will be limited by the Flash voltage;
2. External 32.786KHz crystal occupies 2 IO pins，MIC BIAS occupies 1 IO pin, external Flash 4-bit mode occupies 2 IO pins; SWD & UART port pins have been included.
3. P0_3 (log pin) must keep not connected, and cannot be multiplexed;
4. Audio ADC occupies P2_6, P2_7; there is also 1 Channel Low power competitor;
5. 1 UART has been used for log;
6. SPIC0 is fixedly connected to external flash;

3 Reset

HW_RST_N pin is used as RESET and is active-low. It is a high impedance port with an internal weakly pull high (~100K ohm) resistance. It is recommended to add an external capacitor to this pin. If the IC reset function is not needed, it is required to add a 10K pull-up resistor externally.

4 Crystal Requirements

40MHz crystal: Clock source for MCU in active state. RTL8762D could use the 40M crystal with CL of 7 or 9 pf. Please refer to the rBom list in the HDK documentation for crystal oscillator specifications.

With the CL=7/9pF crystal, it is possible to only use the internal capacitance of the chip as a matching capacitor, but it requires to calibrate each IC separately during mass production.

If applying a uniform capacitor value without performing a separate frequency offset calibration for each PCB, it is recommended to adjust the frequency offset using crystal with CL=9pF, external capacitor C1, C2 and chip internal capacitor.

Please refer to "4.1 Production Frequency Offset Calibration Instructions" for information about how to choose the appropriate internal & external capacitor value.

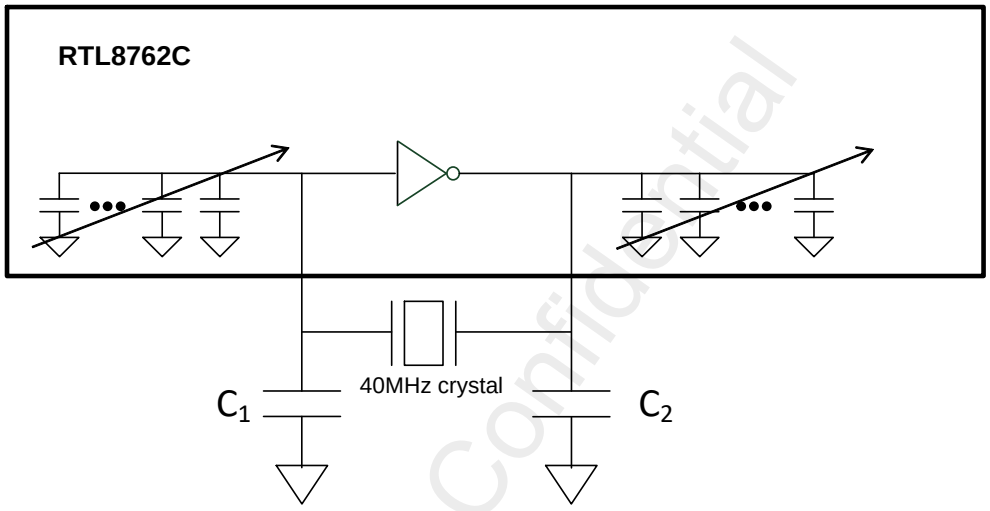


Figure4.1 40MHz crystal

32.768KHz crystal: For details of crystal specifications, please refer to the rBom list in the HDK document. If a 32.768KHz crystal with CL=7pF is used, C1/C2 could be removed.

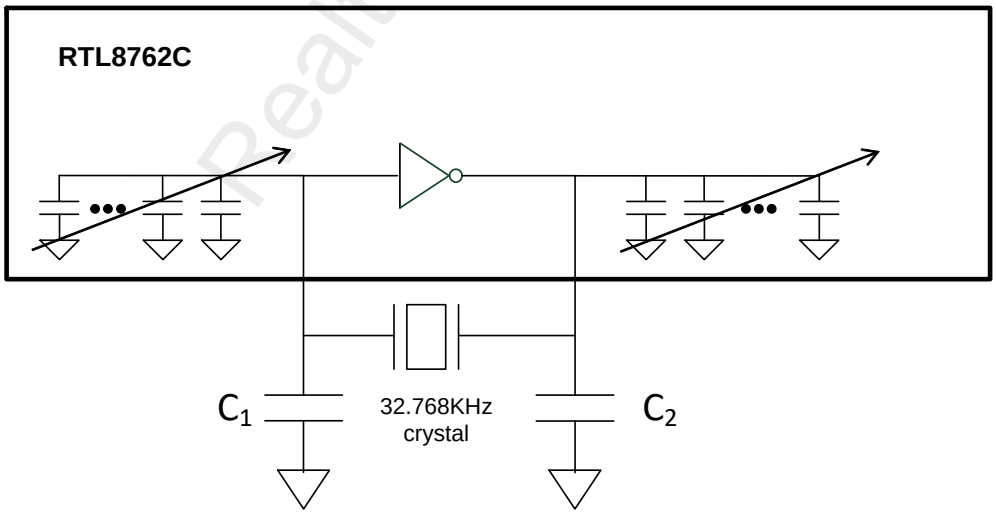


Figure4.2 32.768KHz crystal

4.1 Frequency Offset Calibration Instruction

According to the mass production calibration strategy, frequency offset calibration is processed in two cases.

4.1.1 Same capacitance settings for all PCBs

If all PCBs use a uniform capacitor setting, follow the procedure below to find the optimum capacitor setting value.

1. Set the internal cap to a relatively small value (about 10 levels from the lowest one)
2. Calculate and adjust the external capacitor value to change the frequency offset to ±10KHz.
3. Adjust the internal cap value again, and try to change the absolute value of the frequency offset to 0KHz.
4. Test multiple PCBs to confirm the accuracy of the frequency offset setting.

Test the frequency offset of multiple PCBs with the same settings (more than 5 recommended). Calculate the frequency offset values of all boards, the closer to 0KHz, the better. In general, the average value could be adjusted to ±5KHz, the smaller, the better. For example, in the table below, the average frequency offset is ±3.2KHz.

	Frequency (GHz)	Frequency Offset (KHz)
1	2.442003	3
2	2.442004	4
3	2.442007	7
4	2.441998	-2
5	2.442004	4
avg		3.2

The recommended frequency offset test standard is set at ±35KHz ~ ±40KHz. The capacitor setting value needs to be re-adjusted after changing the material. During production, it is necessary to pay attention to whether the frequency offset is abnormally floating. Assuming that the standard of the frequency offset test is ±35KHz, it is recommended to check whether the capacitance value and the internal CL value of the chip need to be readjusted under the following conditions:

- There are batch changes in the crystal material.
- The average value of the sampling boards' frequency deviation is greater than ±15KHz (or ±20KHz).
- The number of products exceeding ±35KHz is abnormally increased during production, for example, the proportion of failed frequency offset is significantly increased.
- It is found that the frequency offset distribution drifts obviously in a certain direction, for example, the frequency offset is +XX KHz.
- The proportion of products in the range of +25KHz ~ +30KHz or -25KHz ~ -30KHz begins to increase.

4.1.2 Individual calibration for each PCB

If the frequency offset calibration is performed separately for each PCB, the frequency offset can be controlled within a smaller range. There are several points worth being noted shown as below:

- Crystal with CL=7/9pF can adjust the frequency offset only by internal capacitor.

- The smaller the CL is, the larger the frequency offset step of each internal capacitor level is.

4.2 Crystal Start-up Waiting Time Settings

The start-up waiting time is to ensure that the crystal oscillator has sufficient start-up time. When the crystal start-up time is greater than the start-up waiting time set by the IC, the SW will crash. The IC crystal start-up time can be set by MP TOOL, and the start-up time is directly related to the value of XTAL capacitor. The larger the XTAL capacitor is, the longer time the crystal oscillator start-up takes. In addition, the PCBA crystal start-up time can be measured by an oscilloscope.

The crystal start-up time test procedure is as follows:

Set up the corresponding test platform as shown below, the steps are as follows:

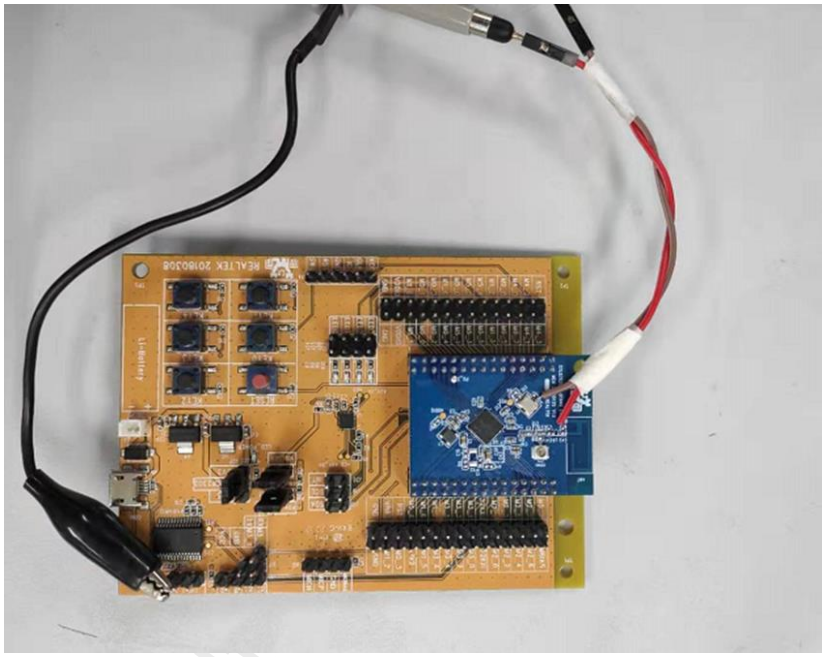


Figure4.3 crystal start-up time test platform

1. Tightly twist two DuPont lines together to form a twisted pair, one of which is soldered to the xo pin of 40MHz XTAL (the gray DuPont line in Figure 4.3), and the other one is not connected (the red DuPont line in Figure 4.3).
2. Connect Micro USB to EVB Mother Board as power supply.
3. Connect the oscilloscope probe to the red DuPont line (the one that is not connected to xo pin) in the twisted pair.

After the corresponding test platform is built according to the operation steps above, the EVB is powered by 3V. When the RTL8762D chips are switched from the DLPS state to the active state, observe the waveform on the red DuPont line, which is coupled from the waveform of 40MHz XTAL xo pin on the gray DuPont line in the twisted pair, and measure the corresponding start-up time (it is suggested to set the horizontal axis scale to 500ms first, and then adjust the horizontal axis to 500us after the waveform is captured). The result is as shown in the figure below. The start-up time is about 2T=750*2=1500us=1.5ms. Note that the external capacitor connected to the 40MHz XTAL is 10pF here. Part of the crystal start-up time data is attached.

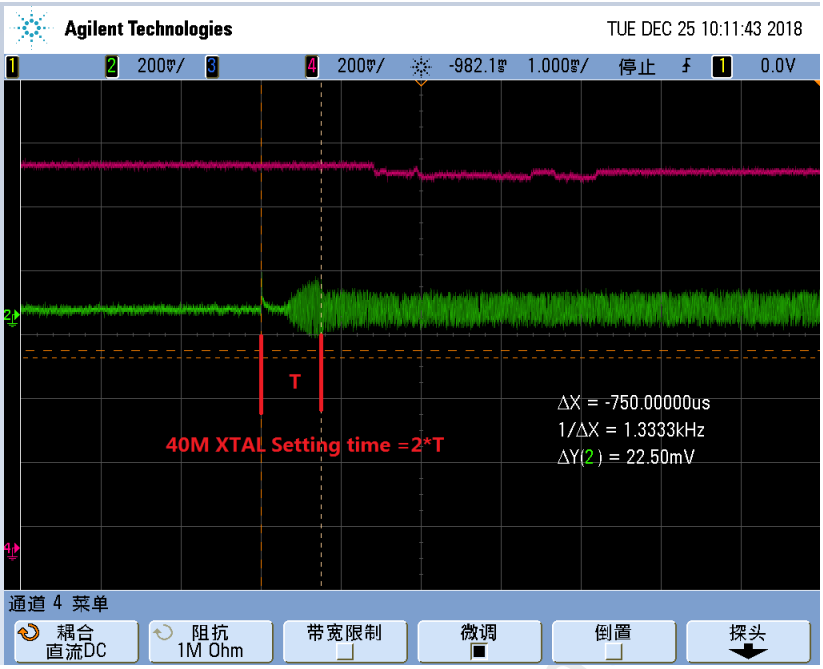


Figure4.4 Start-up time waveform (external cap = 10pF)

To ensure the IC working normally, the LOP_xtal_delay time must be set greater than the XTAL setting time to avoid IC crash. The default value of 40MHz XTAL LOP Delay in patch 264 is 0x60(3ms), and the value of LOP_Xtal_delay time can be set through MP TOOL config file. The value can be selected from 0~0xC0, 32us per step.

default value of Internal Cap setting（12pF）					
Vendor	Model	Bypass Cap (pF)	Frequency Offset (KHz)	Start-up Time (ms)	LOP Xtal delay time setting (ms)
TST	TZ0308D（CL=9pF）	1.3	-45	0.51*2	>1.02
		1.5	-63	0.52*2	>1.04
		1.6	-65	0.53*2	>1.06
		3	-72.5	0.55*2	>1.1

Xtal CL was the parameter in crystal datasheet.

Shunt Capacitance (Co)	3.0 pF max
Load Capacitance (CL)	9 pF
Aging	+/-2ppm/year

5 PAD

RTL8762D has 3 types of IO PAD: Digital IO, analog/digital IO and special/digital;

Digital IO: Only used for digital signal, supports all function in pin mux table.

Analog/Digital IO: supports ADC (include AUXADC and Audio ADC) and all digital IO function. Audio ADC was dedicated for Microphone application，fixed at P2_6,P2_7.

Special/Digital: Shared by 32.768KHz crystal & MIC BIAS, it could be switched to digital mode and supports all digital IO functions.

All IOs support Wakeup function. Different resistors can be connected to pull-up and pull-down to achieve strong pull and weak pull.

Incorrect setting of PAD in DLPS mode would cause abnormal current leakage. Refer to the following precautions:

- Exactly reach VDD when pulling high. Similarly, fully touch GND while pulling down. Otherwise, the intermediate voltage will cause current leakage.
- The output is either High or Low, and the external circuit needs to be cut off.
- “Pull none + PAD shut down” can be used when the PAD voltage is between VDD and GND.
- Boot code might modify the status of some pins during the boot phase.
- Part of GPIO has overlapping mapping to PAD. Pay attention when using GPIO.
- SWD, UART, and P0_3 are the default settings, which needs to be noticed when multiplexing them. In PCB design, it is necessary to set test points out from these pins.
- I8080 pin and 45MHz SPI signal pin are located in fixed positons. They cannot be modified by PINMUX.

PAD electrical characteristics are listed in Datasheet. PAD could avoid current flowing backward when $V_{PAD} > V_{BAT}$. However, the PAD voltage must not exceed 3.3V

PAD is weakly pulled by default. According to different PADs, there are two states, weakly pull up and weakly pull down. The pull setting is also valid in the Reset mode.

For more details, refer to RTL8762D_IOPin_Information_XXXXXX.xls in HDK.

6 Flash

RTL8762DW, RTL8762DK needs external flash, and available Flash is mentioned in Flash QVL.RTL8762DGF, RTL8752DJF, RTL8762DJF/DDF, RTL8762DKF contains internal Flash.

6.1 Bypass Flash Code

- When RTL8762D power on or reset, if P0_3 is pulled low, the code in flash would be bypassed (not be erased) and IC would execute Rom code.
  (Note: P0_3 will be changed to Log output after power-on. It is necessary to return P0_3 to the floating state as soon as possible after power-on, or pull P0_3 down to GND with 500ohm series resistor.)
- When RTL8762D power on or reset, if P0_3 is not connected (P0_3 internally pull high by default), IC would execute flash code.

6.2 External Flash

External Flash should be connected to RTL8762DW/DK SPIC interface. It could support 1-bit mode (Standard SPI), 2-bit mode and 4-bit mode (QSPI). In QSP mode, P1_3 and P1_4 need to be connected to Flash, and cannot be used as normal IO. The corresponding circuit is shown in the figure below. Please refer to reference design for details.

For external Flash, running SPI CLK 20MHz is required during XIP. At the same time, it is necessary to pay more attention to layout.

If the Flash is a normal voltage Flash, the rise time of the power supply voltage from 1.8V to 3.3V should be controlled within 15ms.

For FM series Flash, WP and HOLD pin do not have internal pull high. Therefore, when applying 1-bit mode, it is required to externally pull high the two pins.

SPIC is limited to flash, and multiplexing is not allowed.

Please refer to RT8762D Flash AVL document for Flash selection.

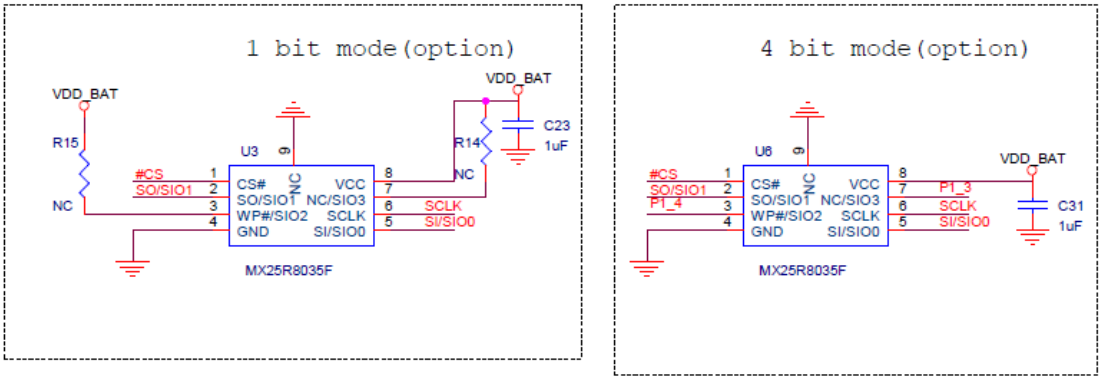


Figure6.1 Flash reference circuit

7 Special Notes

Additional attention should be paid under following circumstances:

- There must not be any voltage drop placed on ADC pin before IC is powered, because current input that over 1mA will damage ADC channel connect to this pin. (Digital function will not be affected).
- If IC produces VDDIO pin, the voltage on VDDIO must not exceed voltage on VBAT
- Voltage drop placed on IO pin must not exceed 3.6V
- 1.2V & 1.8V output of IC are only available for internal use, any external connection is not allowed.
- GPIO to PAD mapping has multiplexing, for detailed information refer to RTL8762D_IOPin_Information.
- SPI run@45MHz must use specified Pin, refer to RTL8762D_IOPin_Information for details of signal definition
- Some IO pins have default function while powered on, for detailed information refer to RTL8762D_IOPin_Information.

8 Audio Microphone

- RTL8762D has built-in audio EQ for adjusting audio frequency response.
- RTL8762D has built-in MIC_BIAS（1.5V-2.2V）adjustable output with adjustable step of ~150mV. Detailed information about voltage range is contained in Datasheet. This pin needs a bypass capacitor when used as MIC_BIAS. In addition, MIC_BIAS pin can be used as digital IO in applications where MIC_BIAS output is not required.
- It is suggested that differential circuits should be used in Microphone application to avoid common-mode noise at PCB. To obtain better audio performance, capacitances of X5R type should be used for MIC_P/MIC_N DC blocking.

8.1 Analog MEMS MIC

MEMS MIC differential connection to RTL8762D is shown in the following schematic. It is suggested to use differential connection from the MEMs to the BT chip to suppress common-mode noise on PCB. P2_7 is MIC_P, P2_ 6 is MIC_N, and these two signals ports could not be swapped.

Special Note: The resistance of R12 and R13 should be equal to the output impedance of MEMS mic. Otherwise, it will seriously affect the performance of Microphone.

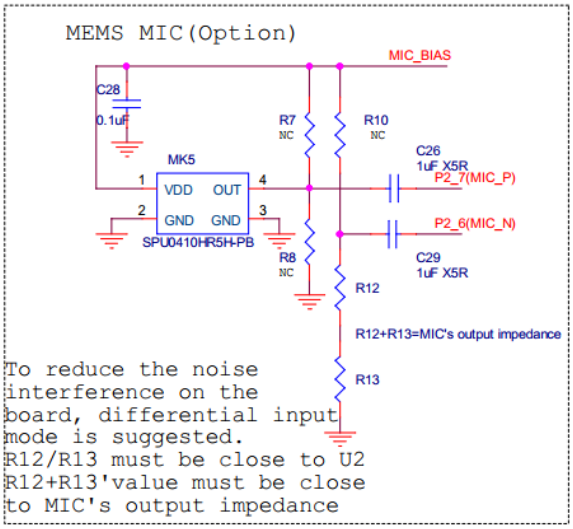


Figure 8.1 Analog MEMS MIC

8.2 Digital MIC

Digital MIC connection to RTL8762D is shown in the following schematic. Any IO can be used to connect to digital MIC CLK and DATA pin, because RTL8762D can use PINMUX function to switch DMIC interface to any IO pin in IC.

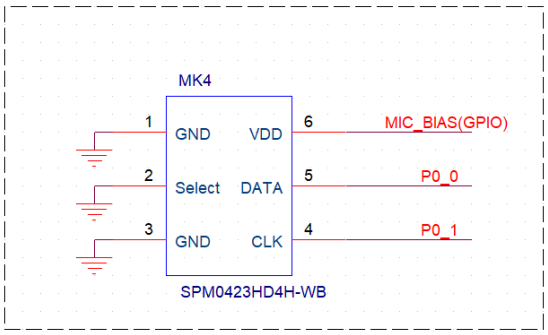


Figure8.2 Digital MIC

8.3 Omnidirectional Condenser MIC

For condenser microphones, it is recommended to use differential mode connection. The reference circuit is shown as below.

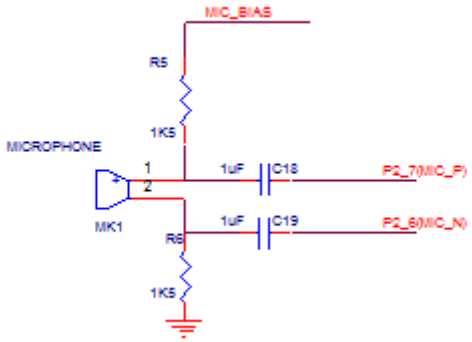


Figure8.3 ECM MIC

9 AUXADC & LPC

RTL8762D integrates a 12bits SAR ADC module (max 400kbps), which is time-divisionally switched to different channels by Analog Mux for general analog-to-digital conversion. The ADC pin can be multiplexed as normal IO.

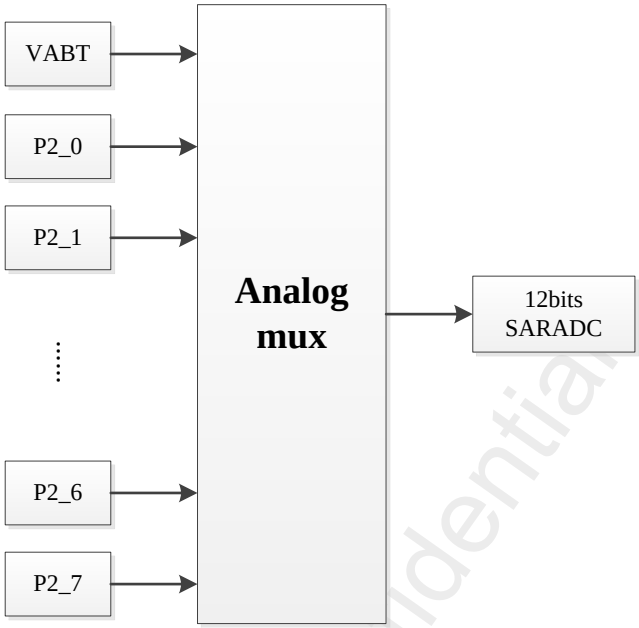


Figure9.1 AUXADC Structure

ADC of RTL8762D can work in single-ended input mode and differential input mode. The VBAT channel can directly detect the voltage of VBAT pin. ADC must be used with RTK ADC lib. Only RTK ADC lib could use internal K value to correctly obtain the actual voltage value. ADC measured voltage must not exceed min{VBAT,VDDIO} level. ADC pin does not have an anti-backflow function. If the ADC pin is powered on during shutdown, it may be reversed to VBAT and the IC may start unexpectedly.

The RTL8762D has a built-in low-power comparator that can wakeup the chip when the voltage is greater or less than the setting value. It can be switched to either ADC Channel or VBAT Channel.

There are two modes for RTL8762D AUXADC:

Bypass mode (range: 0~0.9V):

ADC maximum input voltage cannot exceed 0.9V in this mode, and AUXADC full-scale voltage is about 0.9V. If the input voltage exceeds the ADC range, IC will be damaged.

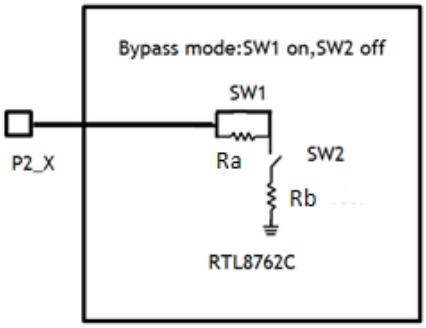


Figure9.2 Bypass mode

For example, when measuring lithium batteries, it is recommended to use the following circuit, where R1=220K, R2=1000K, C1=0.1uF. Because the ADC impedance is large, the first sample value may be unstable. It is recommended to calculate average value after sampling multiple times. If VCC itself fluctuates, it is suggested to place a larger capacitor on C2 to suppress fluctuations.

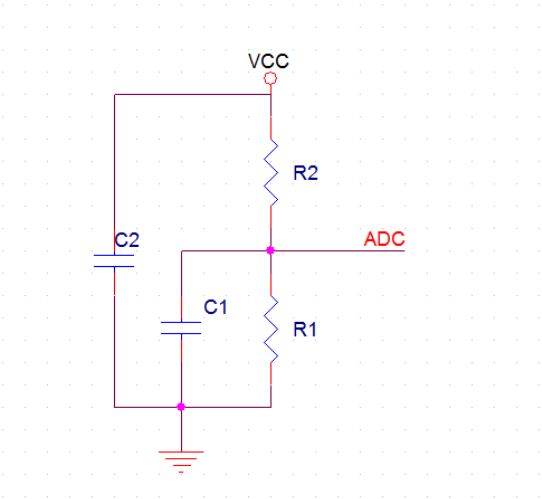


Figure9.3 Bypass mode voltage divider circuit

Divide mode (range: 0~3.3V):

In this mode, at the moment of AUXADC sampling, the impedance between ADC pin P2_X and Ground is the sum of Ra + Rb. AUXADC full-scale is 3.3V in this mode. When the input voltage is 3.3~3.6V, the ADC value may be out of range, causing measurement error. Moreover, the internal load impedance of ADC pin is ~500K. In the continuous sampling mode, the resistance of Ra+Rb will be affected by the sampling rate. The higher the sampling rate is, the lower the resistance is. Because the ADC load impedance is large, the sampled value is possible to fluctuate under conditions of large external impedance. Hence, divide mode is not suitable for the application which is connected to large external impedance.

VBAT channel is only available in Divide mode. Power supply voltage of VBAT pin can be tested inside the chip.

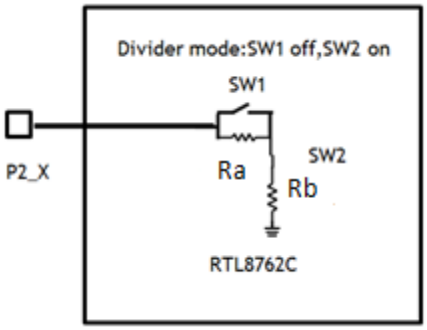


Figure9.4 Divide mode

10 DC/DC Buck Converter

RTL8762D integrates a DC/DC Buck converter. HVD pin is used as Buck input pin, while LX pin is used as Buck output pin. A 4.7uF cap must be attached to HVD pin, and LX pin must be connected to a 2.2uH power inductor. More information about inductor specification is described in HDK. Moreover, this power inductor need be placed as close as possible to LX pin on PCB layout.

The combination of L1, C8, and C7 values may vary. Please strictly follow the component values in HDK reference design for hardware design.

VBAT pin of RTL8762DW and RTL8752CK supplies power to IO PAD, SWR and chip AON at the same time. It is important to note that the bypass capacitor value on this pin should not be reduced.

Note: Do not modify the component values in the relevant circuit, otherwise, the RF performance might deteriorate or the chip might be damaged. Inductor material specifications affect RF performance and power consumption. Please refer to the HDK rBom to select material.

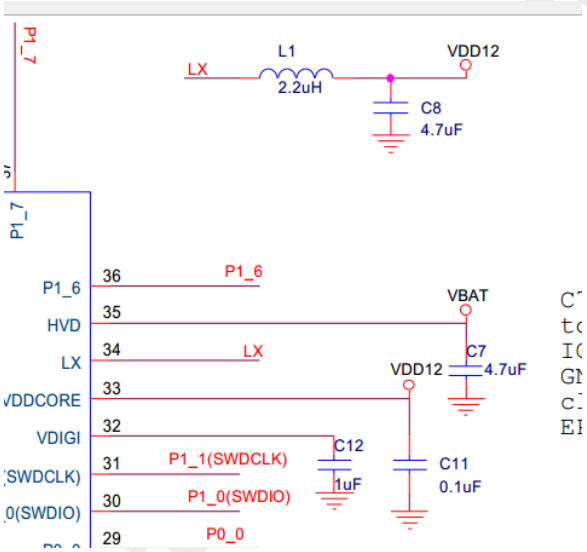


Figure10.1 BUCK Circuit

11 eFuse Programming

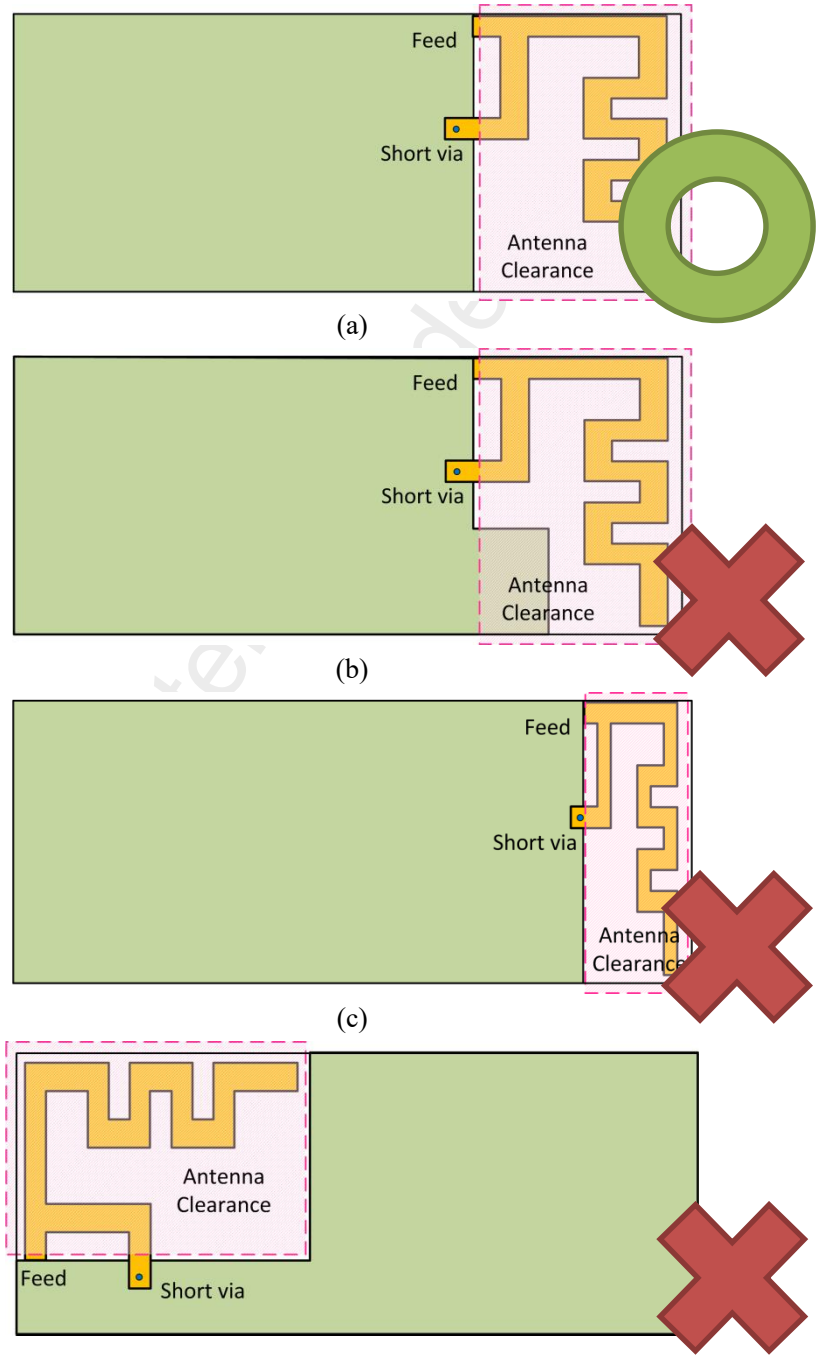
RTL8762D has internal eFuse. The security mechanism requires to program the eFuse inside the IC during mass production. VBAT must be exactly 2.5V (±10%) when programming eFuse. eFuse area can only be written once. Hence, make sure that the data to be burnt is correct before programming eFuse. As to when to write eFuse, refer to the RTL8762D Security Mechanism User Guide.

12 Antenna

12.1 PCB Antenna

Although the PCB antenna occupies a large area, it has the advantage of low cost, easy production and sufficient wireless communication distance, etc.

An antenna is usually a straight line of 1/4 wavelengths. In mobile devices, antennas are usually designed as a curve to reduce the size of the mobile devices. For the PCB antenna, there is trade-off between size and performance of antenna. Small antennas and large bandwidth, high-quality performance are difficult to be achieved at the same time. Therefore, the clearance area of the antenna is an importance factor and is highly recommended to refer to the following pictures.



(d)

Figure11.1 Antenna design

The clearance area means that no other component is allowed to be placed except antenna itself. In the four different designs shown in Fig.(a)-Fig.(d), Fig.(a) has the best performance, because the design deletes the redundant GND area to ensure sufficient clearance area.

When allowed clearance area is not large enough, refer to Fig.(c). Although the antenna length is about 1/4 wavelength, the performance and bandwidth are also be limited.

According to the experience, all metal should be prohibited from being placed in the clearance area; otherwise, the antenna performance will be greatly disturbed.

Although Fig.(d) satisfies the requirements above, its antenna performance is not as good as the one in Fig.(a). The reason is that the GND plane is located right in the direction of the antenna radiation, which influences the antenna performance.

12.2 Thimble Antenna

The thimble antenna is also a common antenna scheme, but it will be affected by the shell. To guarantee the antenna radiation performance, the distance between the shell and PCB board should be greater than 10mm. In addition, for using a thimble antenna, the RF trace requires a DC block capacitor to prevent damage to the chip RF when soldering the thimble.

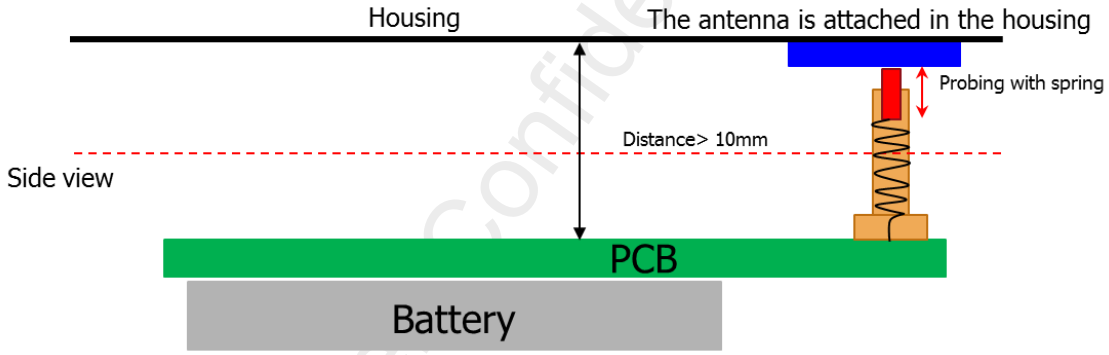


Figure11.2 Thimble antenna model

13 RF Circuit

13.1 RF Power Pin

VD12_PA, VD12_SYN and VD12_TRX are the power input pins for RF transmitter and receiver. The normal working voltage is 1.2V, which can be directly drawn from the VDDCORE of the chip.

Decoupling capacitors should be added separately to these three pins, and placed right in front of the power input pin.

13.2 RF Matching Circuit

In order to achieve efficient power transmission from RFIO to antenna, a matching circuit is required. A return loss greater than 10 dB means that 90% of the power is transmitted to the antenna.

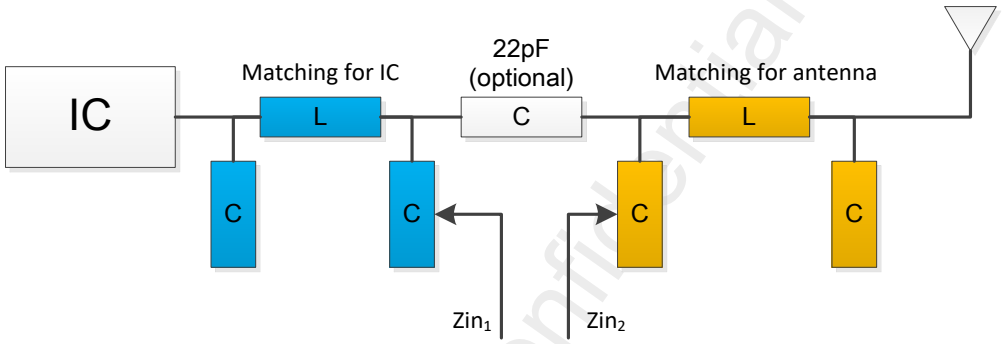


Figure13.1 RF matching circuit

In the figure above, 3 components are used for matching the IC RF trace and 3 components are used for matching the antenna. The purpose is to obtain 50 ohm input impedance for both Zin,1 and Zin,2. The 22pF capacitor for DC blocking may be optional only if the chosen antenna is PCB antenna or chip antenna.

The matching network in IC RF trace is also designed for harmonic suppression. It is strongly recommended to follow Realtek HDK instruction, and choose exactly the same products as those in QVL. Otherwise, the performance cannot be guaranteed.

The chosen value for antenna matching depends on the design. Sometimes, antenna matching can be achieved by using only 2 components. However, the space for 3 components should be reserved, so fine-tuning is allowed to be performed at the later stage of the design.

13.3 RF Trace Impedance

The impedance of trace for RF signal should be designed at 50 ohm. The impedance depends on the following factors and should be designed carefully:

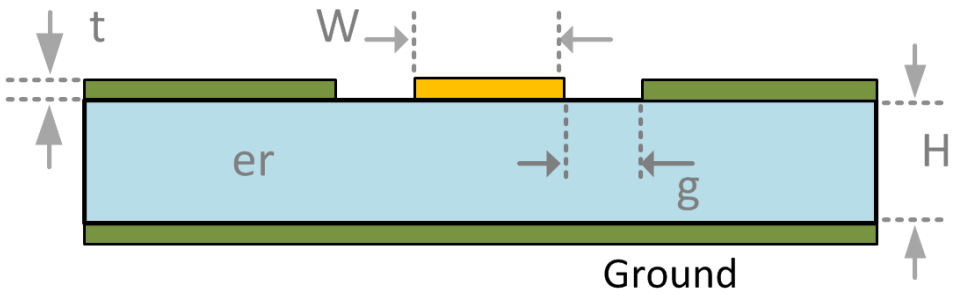


Figure13.2 RF trace impedance

1. **Trace width W:**
   Smaller W will lead to higher impedance.
2. **Height from trace to ground H:**
   The impedance decreases when H is increased.
3. **The gap between RF trace and adjacent ground G:**
   The impedance decreases when gap is decreases. Notice that gap must be symmetrical on both sides of the trace.
4. **Copper thickness t:**
   The impedance increases as thickness decreases.
5. **Substrate dielectric constant:**
   Larger dielectric constant will leads to smaller impedance.

The above parameters for RF trace should be taken into consideration when designing the RF trace. Several free impedance calculator software could be found online. Use these software to find out a proper geometry design for RF trace.

The impedance must be constant throughout the RF signal trace. Therefore, trace width and the gap between RF trace and adjacent ground should be maintained, and the copper laid at both sides of the trace shall be intact.

Different from other signal traces, the RF trace must be guarded with ground, so that it forms a CPWG guided wave structure. Any other traces must not be placed close to the RF trace. Otherwise, mutual coupling between traces will cause severe interference problem.

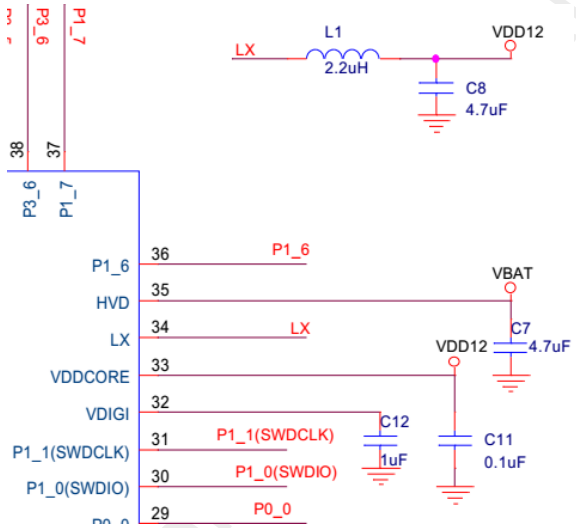
14 PCB Layout Guide

14.1 Component Layout Order

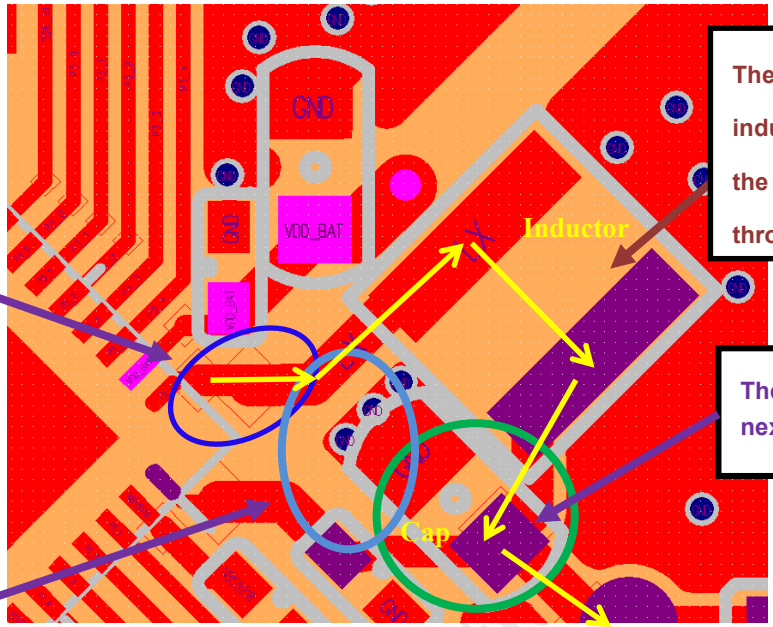
Arranging the components should follow the order below. The higher priority indicates that the component should be closer to IC.

1. DC/DC circuit components
2. VBAT bypass capacitor
3. RF circuit components
4. 40MHz Crystal
5. RF VDD bypass capacitor
6. Other bypass capacitors

14.2 DC/DC Circuit Components Placement & Layout



1. The input power trace connected to HVD/VBAT must be as wide as possible; it's recommended to be 20 or 25mil.
2. The inductor of switching regulator (buck) and capacitor is suggested to be close to BT chip.
3. The switching regulator power pin LX goes through the2.2uH inductor and a 4.7uF capacitor to form a stable, low noise power source. It is strictly prohibited to pull out the power without going through the 4.7uF capacitor (like the yellow line in the figure below). The trace of LX should be short and wide for the consideration of EMI issue; the trace width is suggested to be at least 15mil.
4. The ground terminal of the 4.7uF capacitor should be close to the chip's E-PAD to shorten the ground loop. If the space is sufficient, place more ground via around the ground pin of 4.7uF capacitor.



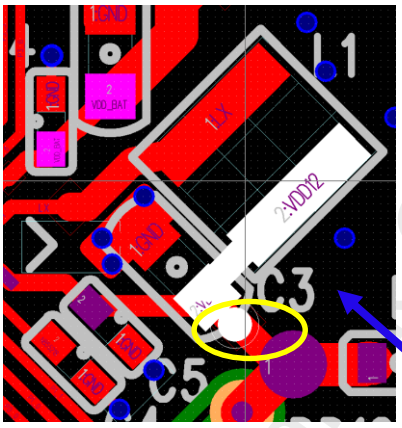
The switching signal LX must be short and wide.

The LX must go through the inductor first, then through the capacitor and finally through branch out!!

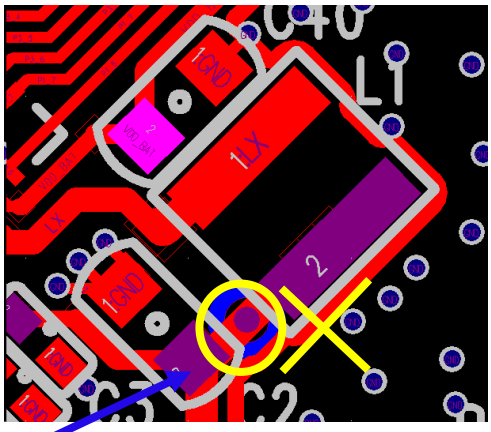
The capacitor must place next to the inductor

Put more than one ground via at the ground

CORRECT



NG

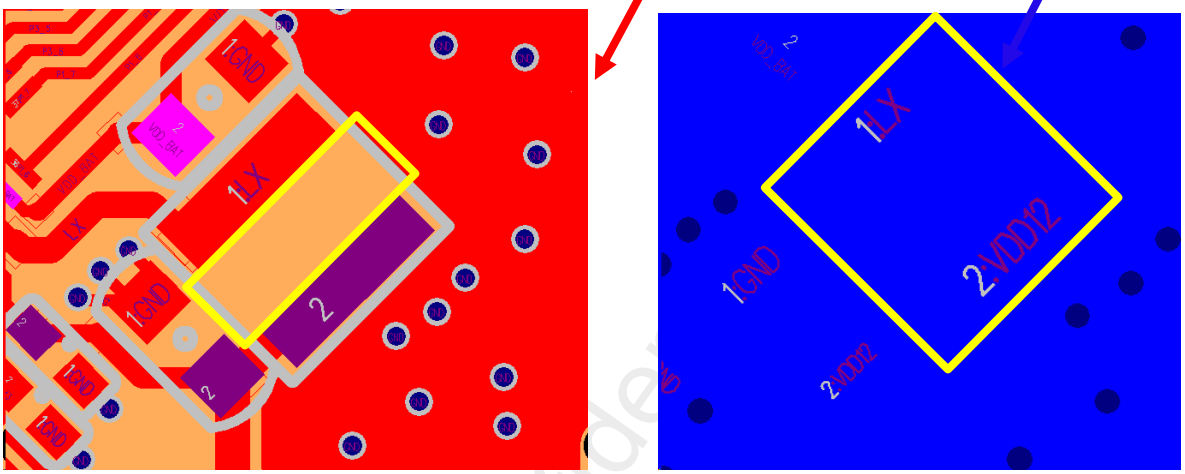


Buck SWR LX goes through inductor and capacitor first → power via should be after the capacitor.

Buck SWR through inductor → add via before the capacitor.

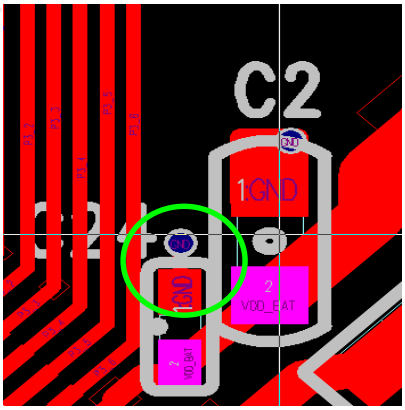
- There should be no signal trace under the buck inductor body, which means keeping copper plane of the back layer (BOT) complete.

- There is no GND copper between the pads of wire wound inductor. (as yellow rectangular mark shown)

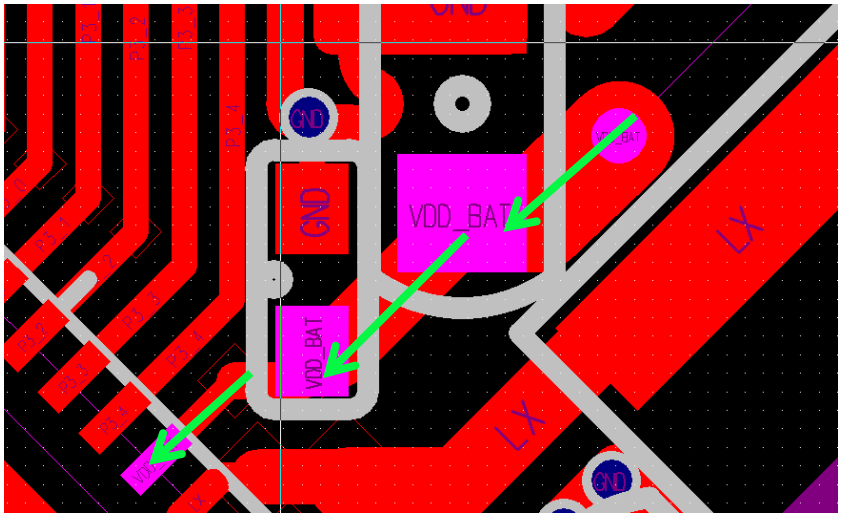


14.3 Power Bypass Capacitor Layout

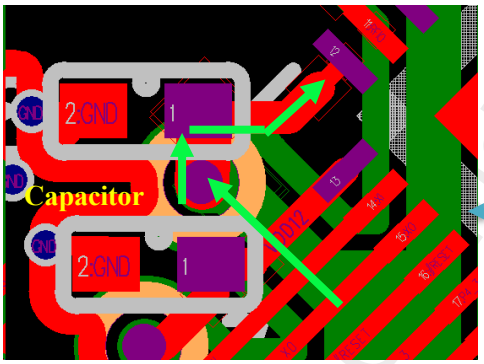
1. The decoupling capacitor of VBAT must be placed near the input port of IC CHIP to ensure return path back to GND without blocking.
2. The capacitor of VBAT should be connected to the GND layer through GND Via. Furthermore, GND Via should be as close to the pad as possible in order to shorten the ground loop. (as shown in the picture below)



3. The trace route must go to the capacitor first, and then go into the input pin of chip. It is suggested that trace width is larger than 15mil.



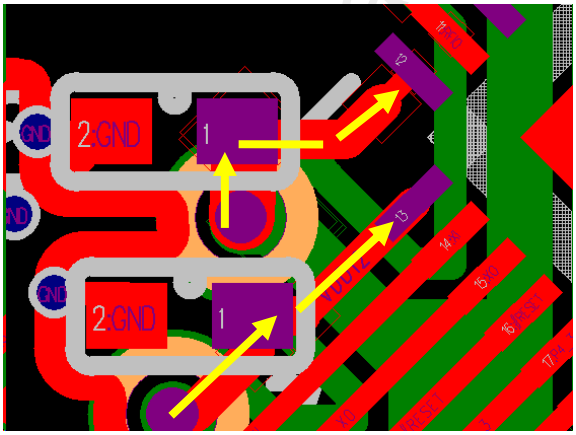
4. The bypass capacitor of the power supply should be placed close to the power pin. All of the power trace should go through capacitor first, then go into IC, and finally go outside for other branches.

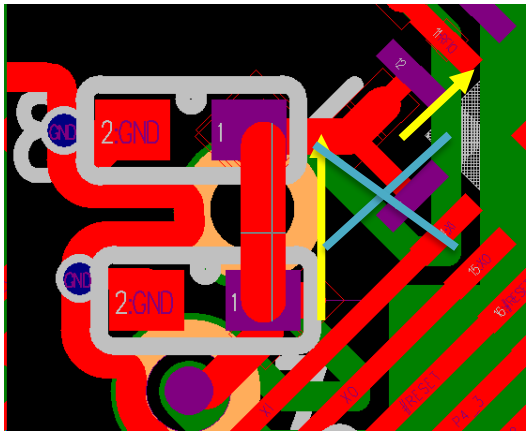


Be sure to follow current flow direction

5. If there are two pins nearby with the same net name, there should be two bypass capacitors, one for each individual pin and the power trace should be routed separately. Do not use the NG example.

CORRECT **NG**

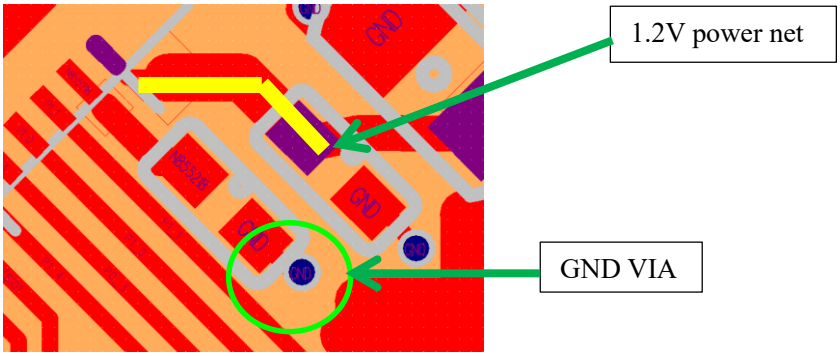




The capacitor component must connect with CHIP pin individually.

Do not connect together before reaching the chip.

6. The bypass capacitors of the VDIGI or VDDIO pins should be placed far away from the 1.2V power net.



14.4 External Flash & I8080

RTL8762D main clock is 90MHz maximum. The rate of Flash in QSPI mode is 45MHz, while the one of I8080 is 20MHz. These clock rates are relatively high. Hence, it is required to route matched length trace as much as possible when designing PCB. The recommendations of layout & routing are as follows:

External Flash QSPI Mode Routing

- The spacing (H) between the QSPI trace and adjacent signals must be at least 2 times wider than the trace width (H=2W);
- The length difference of QSPI traces (CLK, #CS, SIO0~SIO3) should be less than +/-100mil, and the total length should be less than 2.5 inches;
- There should be no stubs on each QSPI trace;
- The 0ohm resistors in series with QSPI traces (CLK, #CS, SIO0~SIO3) must be close to SOC;

I8080 Routing

- The spacing (H) between the I8080 trace and adjacent signals must be at least 2 times wider than the line width (H=2W);
- The length difference of I8080 traces (WR#, CS#, DCX, RD#, Vsync, D0~D7) should be less than +/-100mil, and the total length should be less than 2.5 inches;
- There should be no stubs on each I8080 trace;
- The 0ohm resistors in series with I8080 traces (CLK, #CS, SIO0~SIO3) must be close to SOC;

14.5 RF Trace Layout

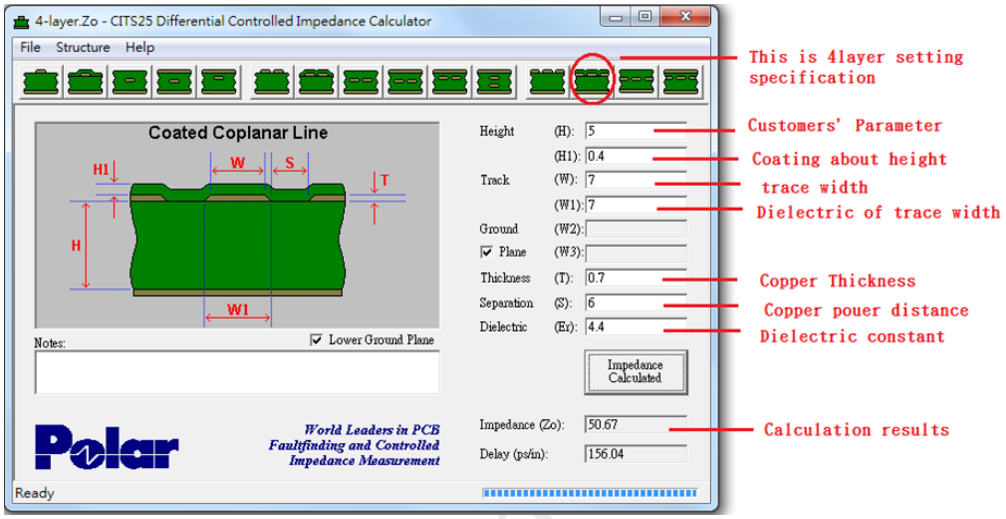
RF impedance calculation

RF trace refers to the connection between IC RFIO Pin and the antenna, which must be carefully controlled. If the RF impedance is not within 50Ω ± 10%, RF performance might be greatly affected. RF impedance calculation tool can be used to obtain 50 ohm impedance, trace width and trace spacing for routing.

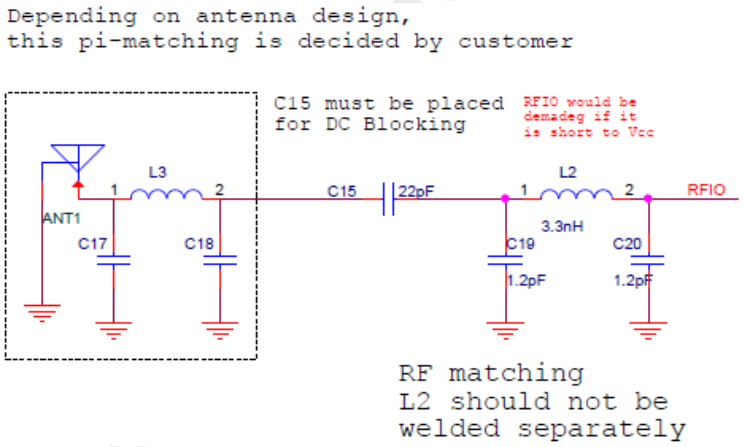
The parameters include the distance from the RF trace to the reference layer (H), the coating thickness (H1), trace width (W), deviation of trace width due to PCB etching (W1), copper thickness

(T), ground copper separation from the RF trace (S) and dielectric constant (Er).

Example: Select appropriate parameters according to the PCB maker's capability, and use the tool to calculate impedance (Zo). It is important to select all the parameters reasonably; otherwise, it may be necessary to seek a better PCB maker causing higher cost.



- It is suggested that the RF trace should be no less than 8mil to avoid the large variation of RF impedance.

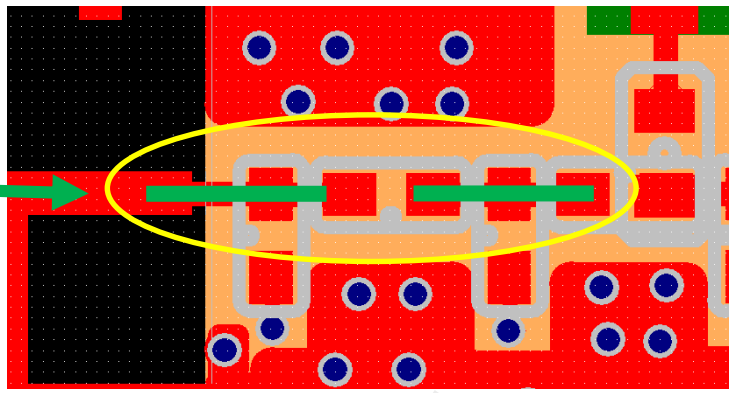


- Communicate with the PCB maker to ensure that the parameters are appropriate.
- The RF test point, TP10, is not suggested to be placed on an extra branch. If it is on bottom layer, via should be added on the path for connection.
- The RF matching components must be as close to IC RFIO pin as possible.

The component and trace should be placed following the rules example below, and the RF trace should go straight forward and appropriately routed.

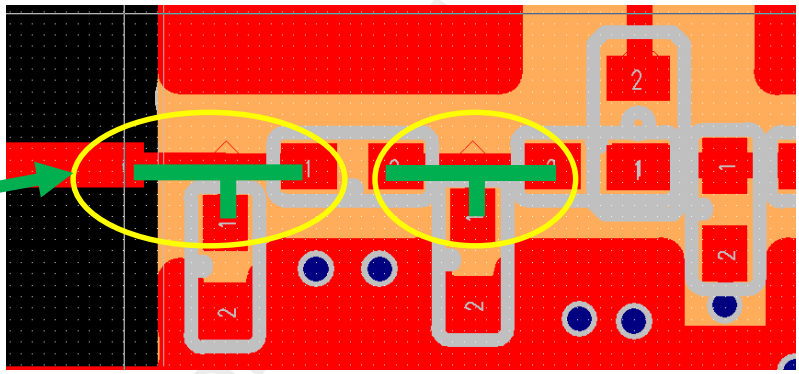
CORRECT

Follow the route example, the trace must be straight forward.

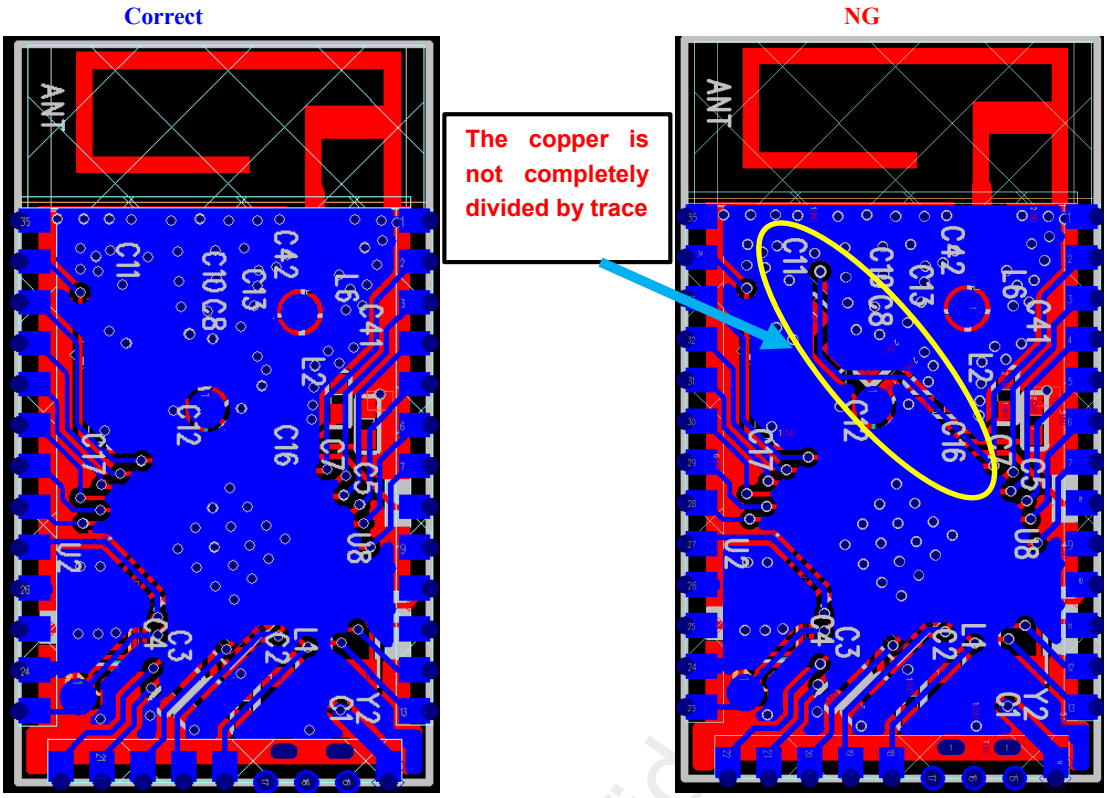


NG

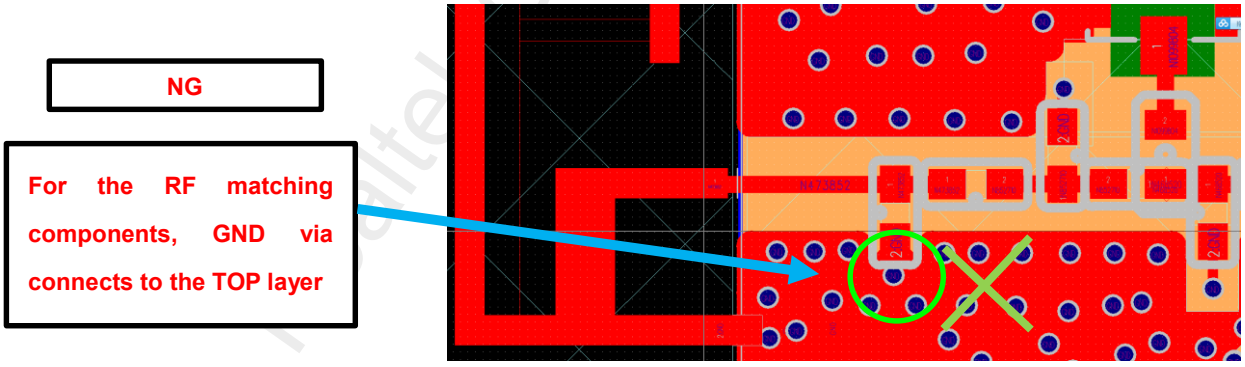
An extra branch trace to the matching is not allowed.



- The PCB layer with BT CHIP is defined as top layer, the layer next to top layer must be ground layer as a reference in a 2-layer or 4-layer PCB design.
- There should be no other signal trace that goes through the reference layer under the RF area (especially in 2-Layer PCB).
- Keep clear in the antenna area. No copper or trace is permitted under the antenna.
- The Reference GND of ANT should be returned to IC EPAD as soon as possible. The ANT return path needs to be as short as possible and cannot be blocked to ensure good connection. Examples: The copper on the right side is not completely divided by trace, and the other one is more appropriate.

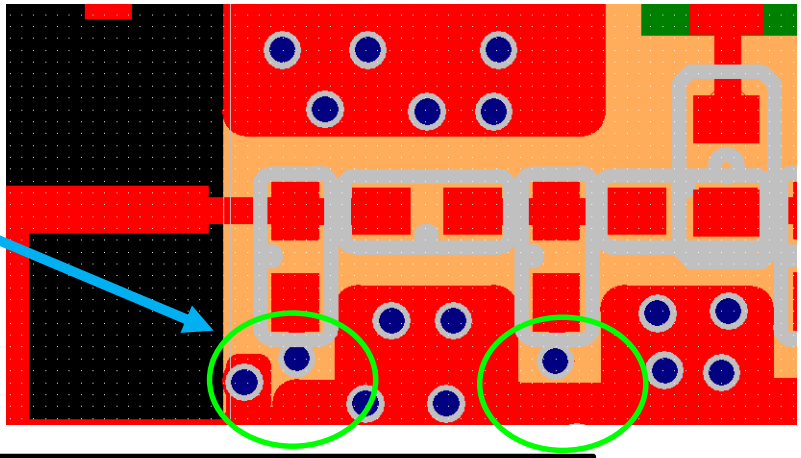


- The ground via of the RF components should be as close to the soldering pad as possible. GND Via should be connected to the GND layer directly instead of TOP layer. The copper grounding should be covered.

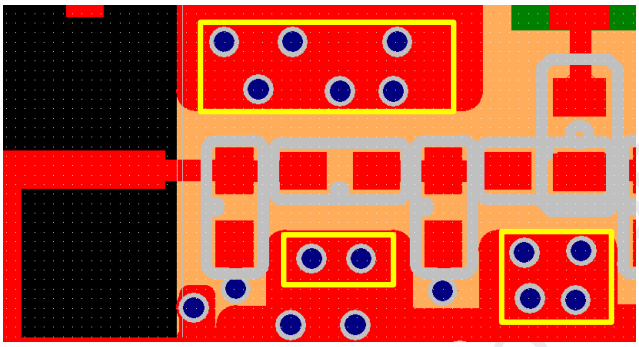


Correct

For the RF matching components, GND Via should be connected to the GND layer directly, instead of TOP layer



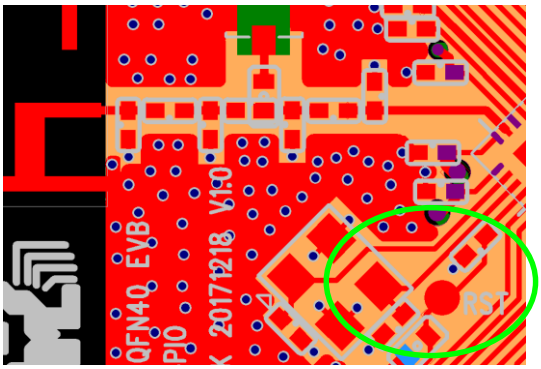
It is suggested that a complete GND via array should be placed to protect the RF trace (shown in yellow rectangular marked below).

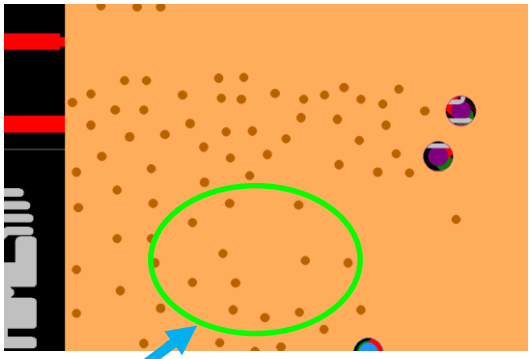


- The layout and component placement should be as concentrated as possible to reserve more space for a bigger antenna, and keep more RF clearance area.

14.6 40MHz Crystal Layout

- If there is no mechanical restrictions, crystal and BT CHIP should be on the same layer.
- Crystal should be far away from RF trace to avoid interference with RF signal.
- Crystal should be close to BT CHIP to keep a short routing path; the trace width should be at least 6mil.
- If it is a 2-layer PCB, avoid tracing on the back layer of crystal, and try to keep a complete ground reference at the next reference layer (bottom side).



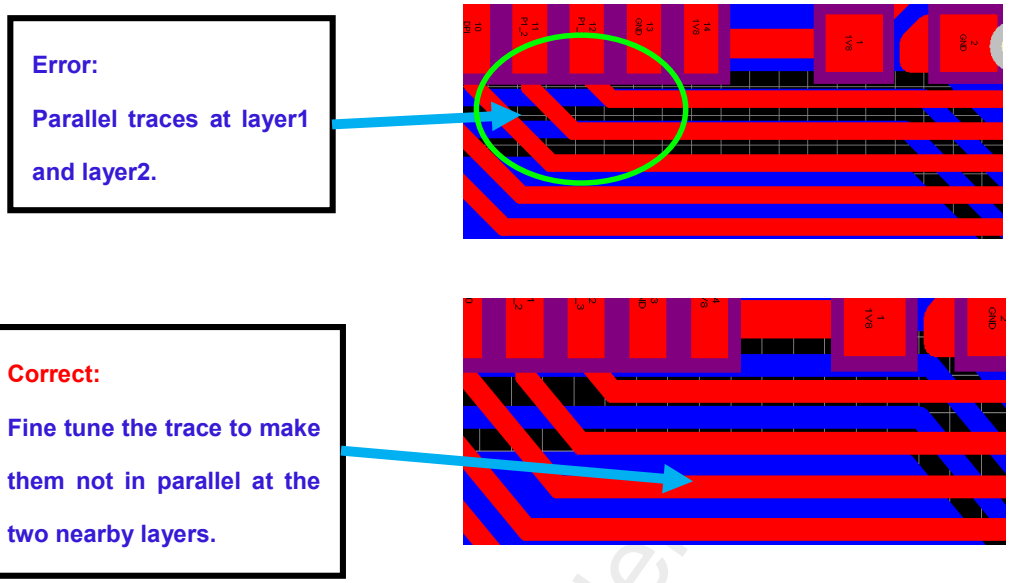


TOP Layer range of crystal:
Note the distance from RF trace

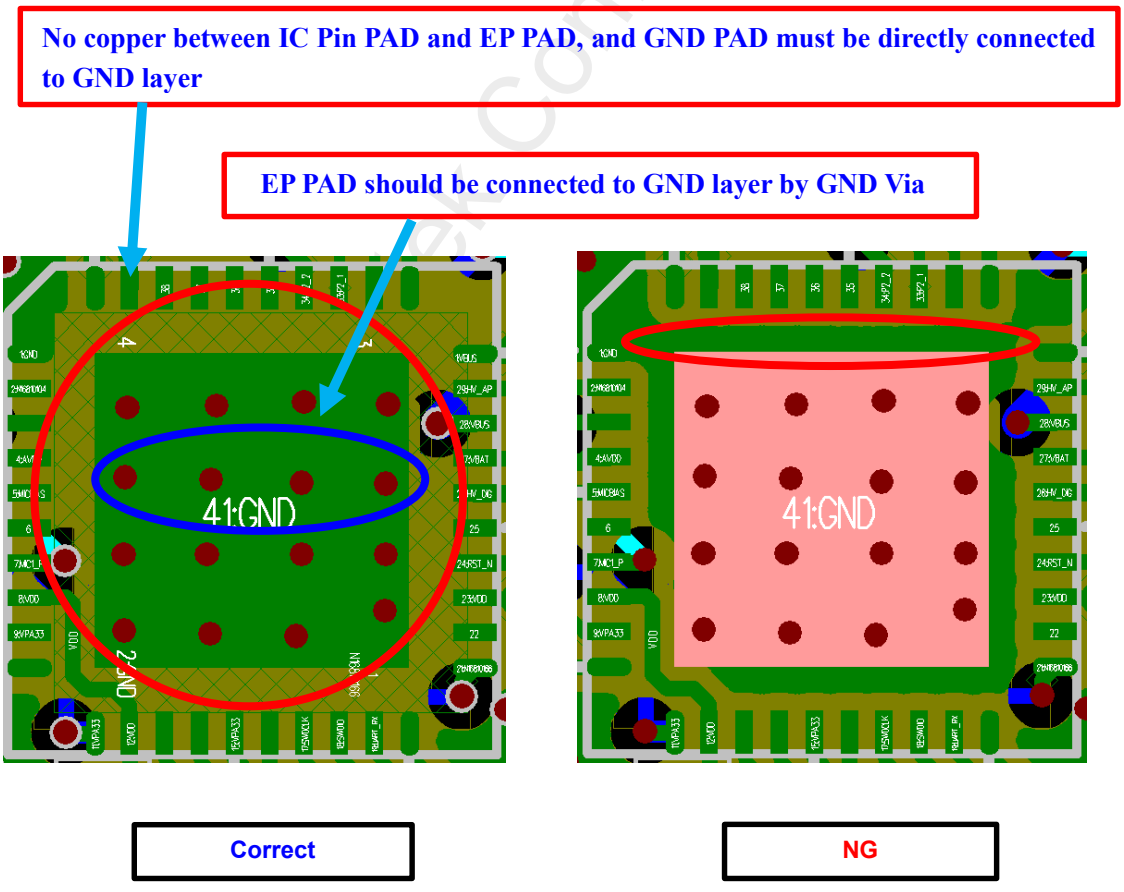
Bottom layer range of crystal:
Forbidden any trace, and keep the copper plane complete.

14.7 MISC

- Avoid the situation that traces on two adjacent layers are overlapped.



- External Flash must be placed as close as possible to IC.



14.8 ESD Layout

In order to protect IC from ESD, the following items should be noted in the PCB design:

- ESD protection tubes (TVS usually) should be added for sensitive devices and sensitive signal traces. TVS should be placed as close as possible to the ESD source (connector, etc.) and farther away from the protected IC than the ESD source. The ESD source needs to be directly connected to the TVS during routing to reduce the parasitic inductance between the TVS tube and backflow GND.

- When splitting the ground plane, pay attention to shortening the return path of signal trace, and wire with star topology to realize grounding in parallel.

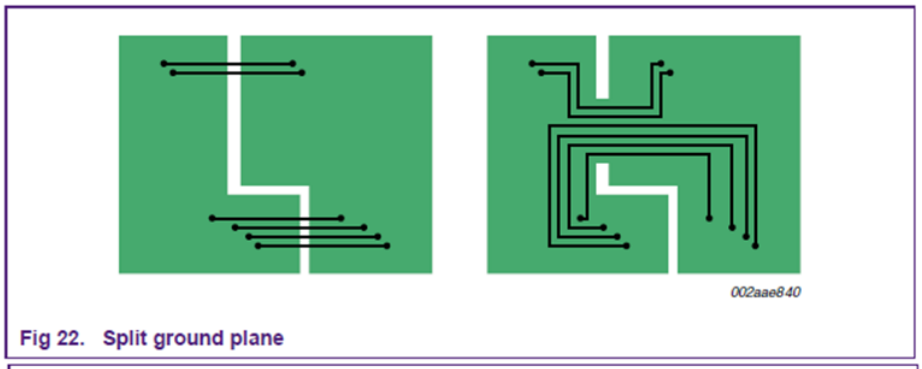


Fig 22. Split ground plane

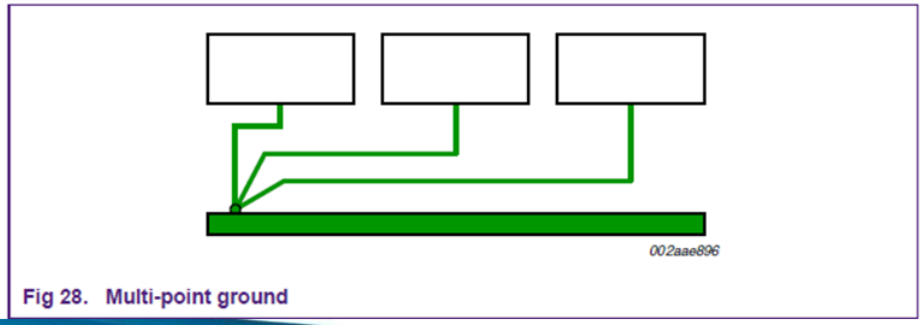


Fig 28. Multi-point ground

- Remove floating GND copper, wrap sensitive signals with the ground to prevent radiation interference from other signals.

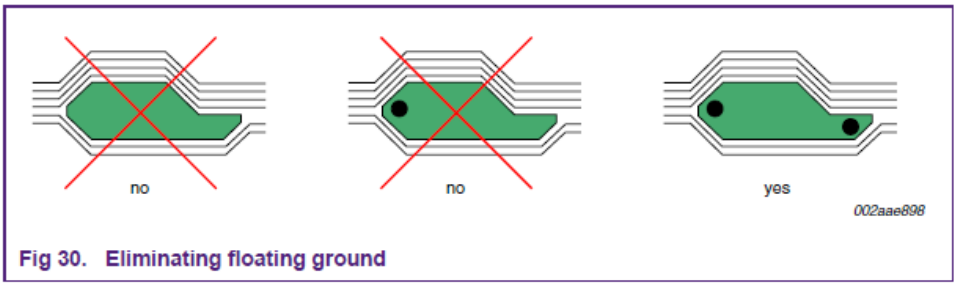


Fig 30. Eliminating floating ground

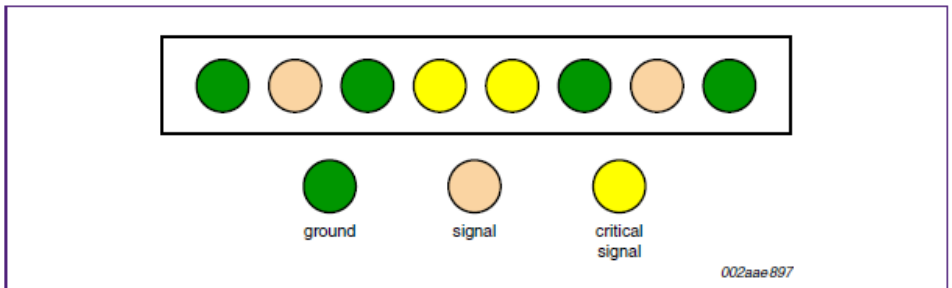
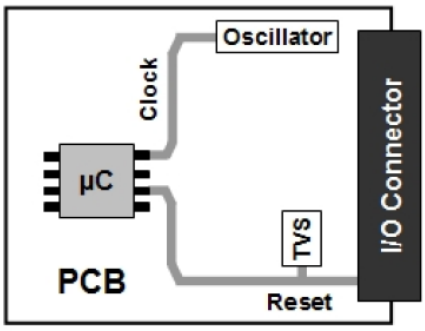


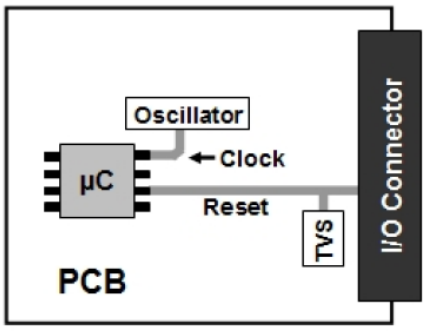
Fig 29. Use of interspersed grounds

- Try to shorten the trace length to reduce parasitic inductance. Since the right angle traces would produce more electromagnetic radiation, it is suggested to avoid the right angle traces connected to the device or trace, especially in the design of high-speed circuits.
- Increase the diameter of the hole and the diameter of the pad as much as possible to reduce the parasitic inductance caused by via.
- For routing, sensitive signal traces should be kept away from the edge of the PCB. In order to avoid crosstalk between trace and antenna, trace should be far away from antenna, and antenna should be placed far away from connector. For layout, all connectors and board-edge wiring could be placed on one side of the PCB board edge, while ESD sensitive components could be placed in the center of PCB.

Poor PCB Layout



Good PCB Layout



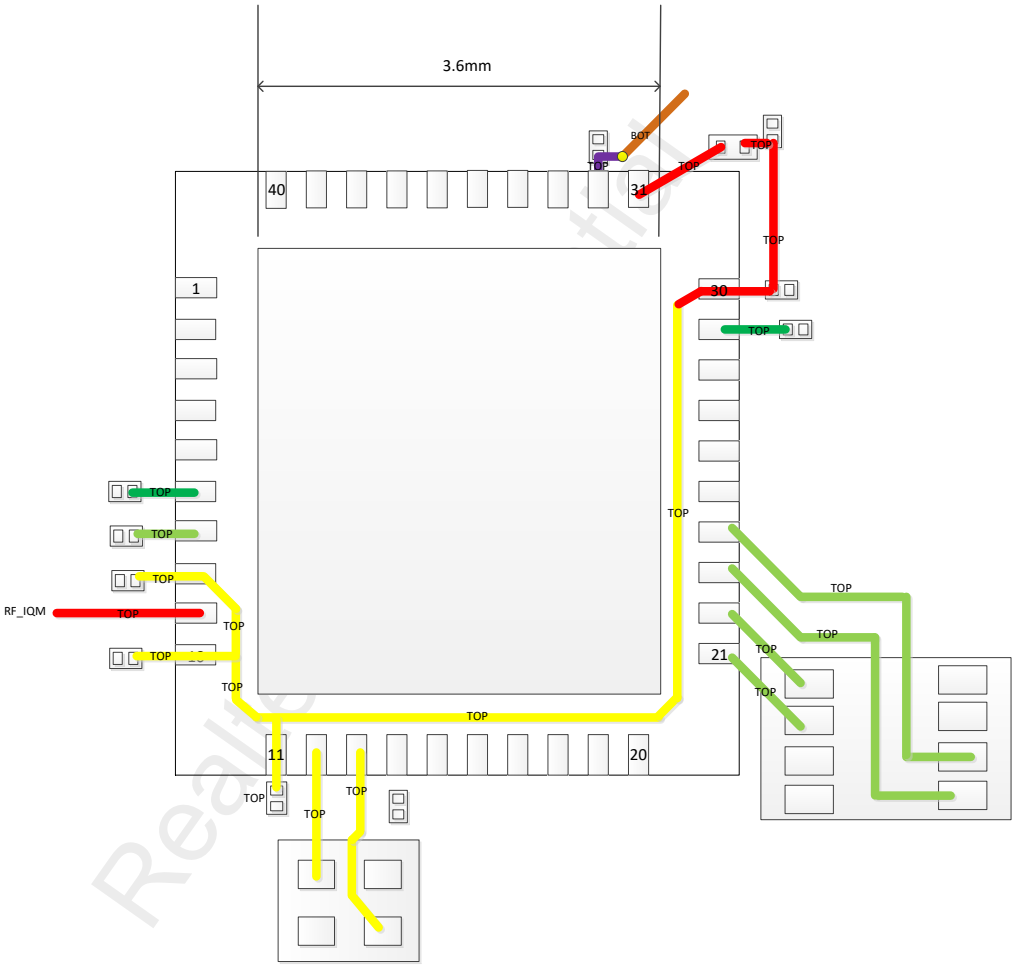
14.9 MP Test Points

To match the mass production test platform, designers need to reserve the following test points during designing PCB.

Test point	Source & Signal	Description
1	VBAT	Power
2	GND	Ground
3	LOG（P0_3）	Debug and erase program
4	TX/RX(P3_0/P3_1)	Debug IC/Download port

15 Layout Rules for Two-layer Board

- Avoid routing in these areas: BT CHIP, RF, Crystal and Buck area.
- **The traces of 2-layer board should be routed at the same layer.**
- The traces must run through the bottom layer, and the traces on the back side should be as short and concentrated as possible to maintain the integrity of the copper.
- The VDD12 trace can pass through the IC package gap by reducing the EPAD size to 3.6mm.
- Other layout guide is mentioned above (Just for reference, VDD1V2 might be short to ground if the PCB manufacturing technique is not good).



16 ESD Protection for MP

- The machine that brushes the solder paste needs to be grounded.
- The PCB to be processed needs to be placed on the insulating tray. If it is placed on a metal plane or a tabletop, the plane (table) surface needs to be grounded.
- On-site personnel need to wear a grounded electrostatic wristband (effect of wireless wristband anti-static is limited, which is not recommended to wear)
- Avoid using mirror board.
- The side where IC is to be placed should be left until the second time of PCB SMT to reduce the number of times that IC touches the metal or the machine.
- If the operator needs to visually check PCBA, the PCBA needs to be placed on the insulating plane. The operator needs to wear an electrostatic wristband, and metal tweezers used need to be covered with an insulating sleeve.
- After the IC is processed by the tin furnace, the operator needs to place the PCBA on a separate insulation tray.
- Rework workbench, welding torch, electrostatic wristband and operation table mat need to be grounded.
- The SMT machine is strung together by metal wires, and then connected to the earth by pipelines.
- Persons who could get contact with the PCB should wear non-conductive finger sleeve.
- When correcting the positions of components or boards, do not touch the IC pins with metal tweezers.
- Apply antistatic liquid on loading board regularly.
- PCBA semi-finished products must be placed on an insulating tray with separate grids. Only one PCBA per grid. In order to avoid CDM collision, it is prohibited to stack PCBA.

17 Debug Process

1. Power on the IC after P0_3 is pulled low. (Flash bypass)
2. Check the correctness of VBAT/VDDIO voltages which should be within the range specified in the Datasheet.
3. Check whether the 1.2V of SWR has an output and the voltage is correct or not.
4. Check whether the 40MHz crystal has started to oscillate or not.
5. Check whether the log UART has an output or not.
6. Check whether the UART is available or not.
7. Check whether the external flash is working properly or not (for the IC using external flash).

18 Differences between RTL8762C & RTL8762D

- 40MHz Crystal request is changed, RTL8762D can only use crystal with CL=7/9pF；
- Support 3 sets of SPIC interfaces, and the speed is faster;
- RTL8762D RAM is greater than RTL8762C;
- RTL8762D Maximum Clock 90MHz, while RTL8762C only 40MHz;
- RTL8762D supports dual PDM input DMIC;