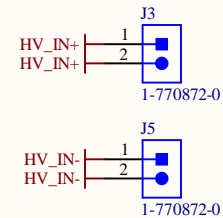
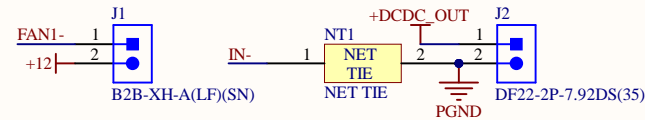
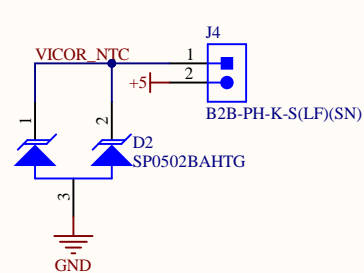
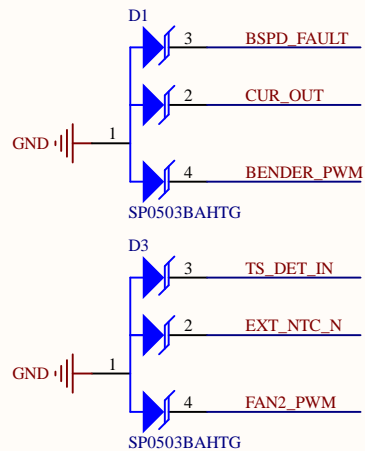
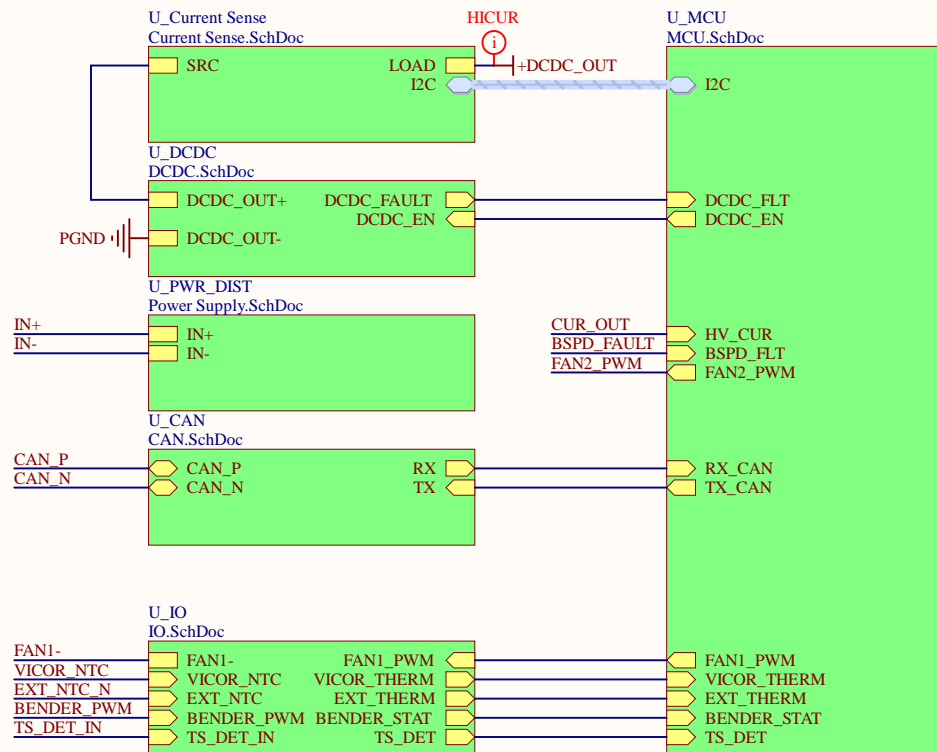


A



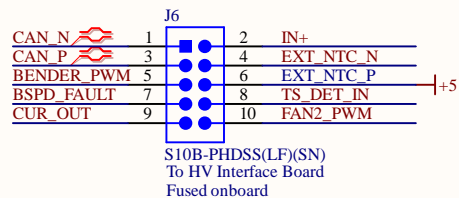
A

B



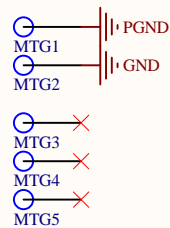
B

C



C

D



D

Title: **Top.SchDoc**

Desc: \*

Size: Letter

Auth: \*

Proj: \*

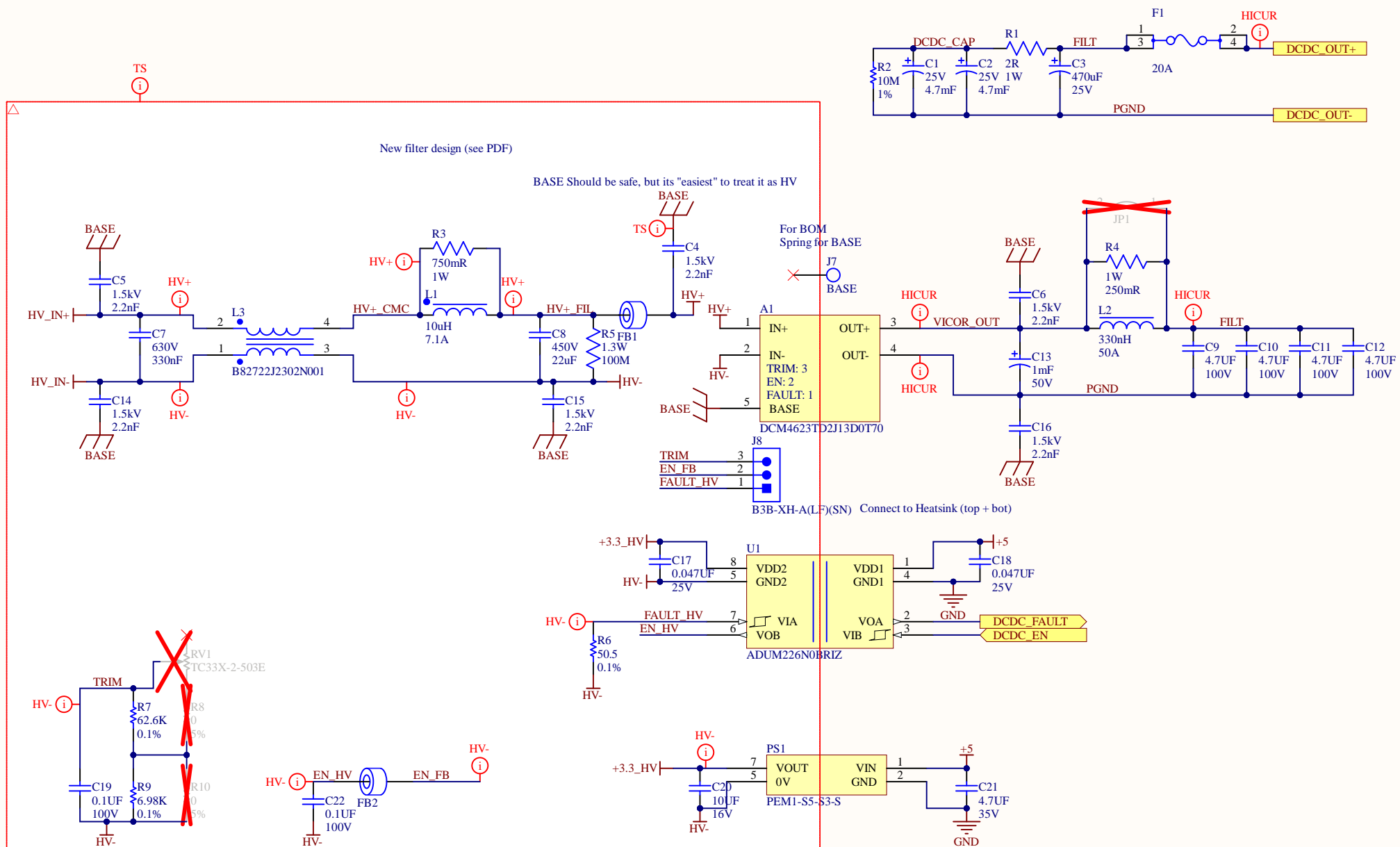
Date: 2/29/2020

10:59:27 PM

Sheet 1 of 7

File: C:\git\AERO\_2019-2020\HV Interface\Top.SchDoc

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△  
Add info about chip

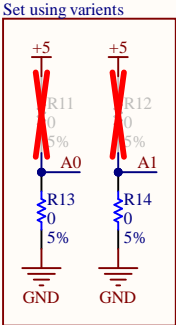
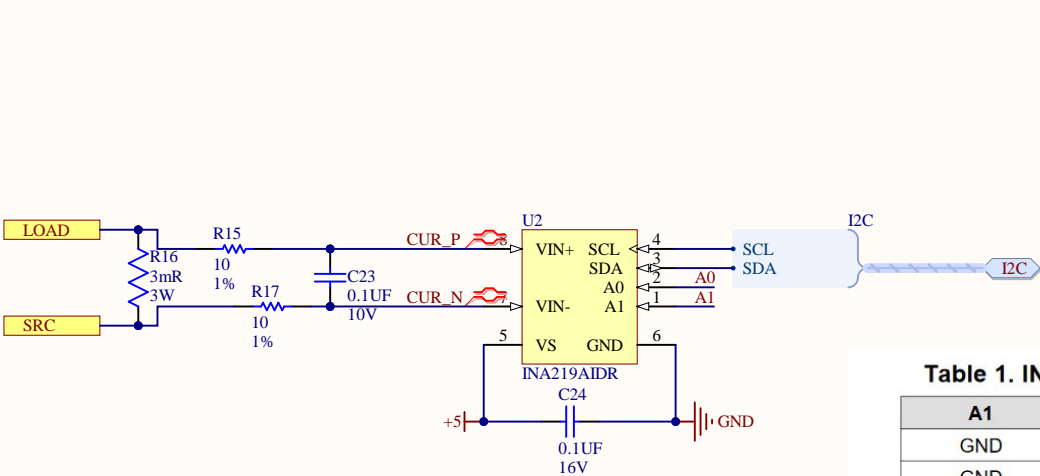


Table 1. INA219 Address Pins and Slave Addresses

| A1              | A0              | SLAVE ADDRESS |
|-----------------|-----------------|---------------|
| GND             | GND             | 1000000       |
| GND             | V <sub>S+</sub> | 1000001       |
| GND             | SDA             | 1000010       |
| GND             | SCL             | 1000011       |
| V <sub>S+</sub> | GND             | 1000100       |
| V <sub>S+</sub> | V <sub>S+</sub> | 1000101       |
| V <sub>S+</sub> | SDA             | 1000110       |
| V <sub>S+</sub> | SCL             | 1000111       |
| SDA             | GND             | 1001000       |
| SDA             | V <sub>S+</sub> | 1001001       |
| SDA             | SDA             | 1001010       |
| SDA             | SCL             | 1001011       |
| SCL             | GND             | 1001100       |
| SCL             | V <sub>S+</sub> | 1001101       |
| SCL             | SDA             | 1001110       |
| SCL             | SCL             | 1001111       |

Consider testing with adafruit board first??

Title: **Current Sense.SchDoc**

Desc: \*

Size: Letter

Auth: \*

Proj: \*

Date: 2/29/2020

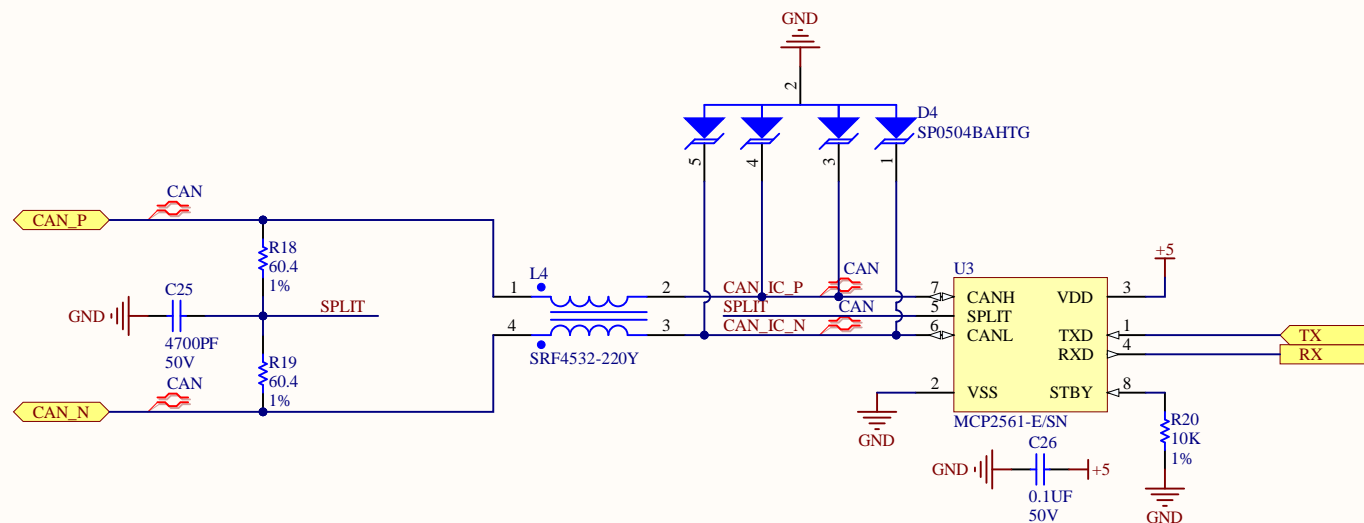
10:59:27 PM

Sheet 3 of 7

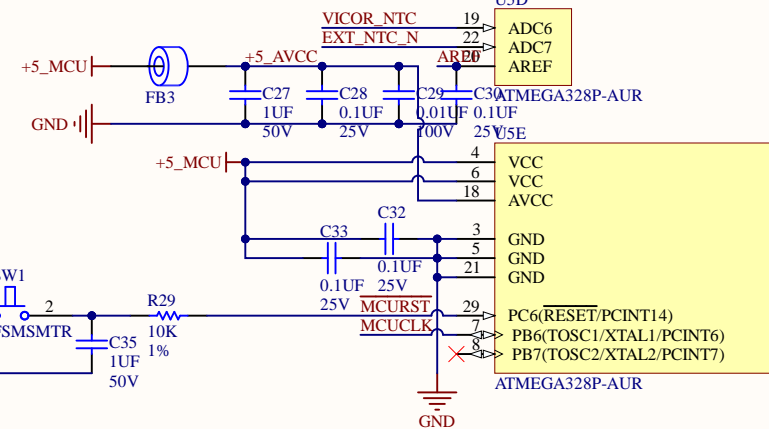
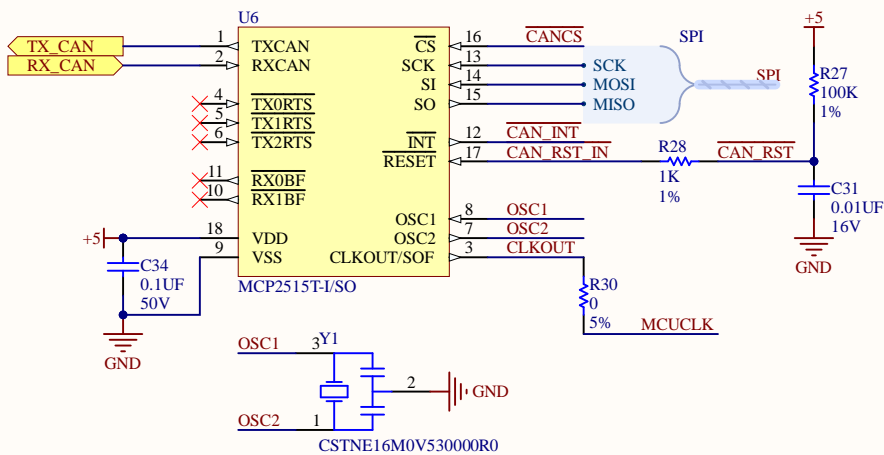
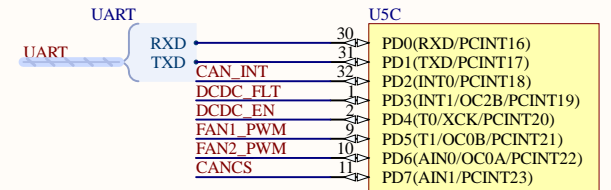
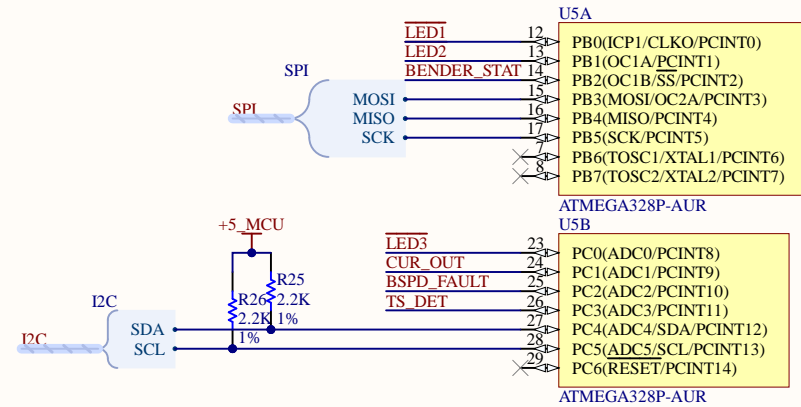
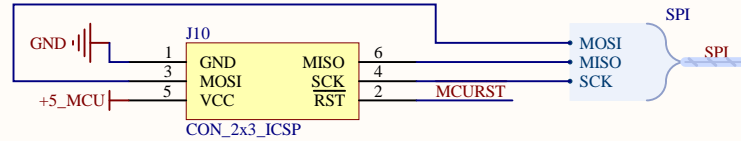
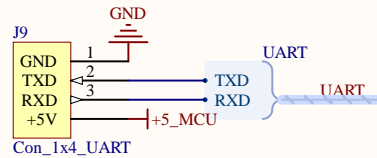
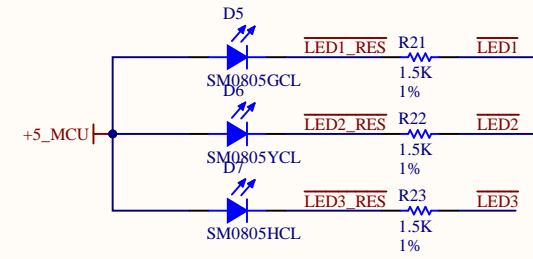
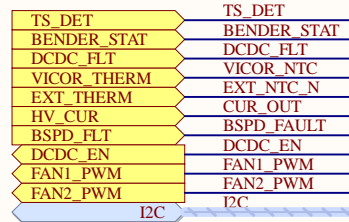
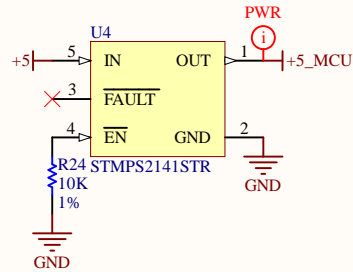
File: C:\git\AERO\_2019-2020\HV Interface\Current Sense.SchDoc



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Power for upload wont power the rest of board  
Prevents killing programmer



Title: **MCU.SchDoc**

Desc:

Size: Letter

Auth: \*

Proj: \*

Date: 2/29/2020

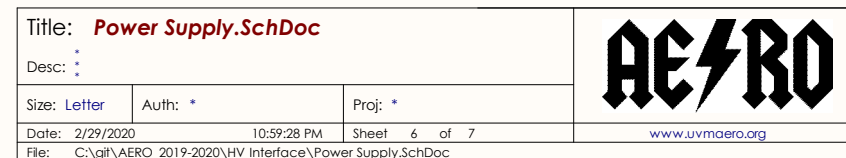
10:59:28 PM

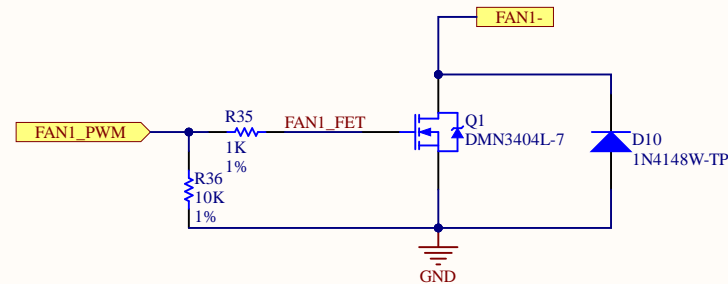
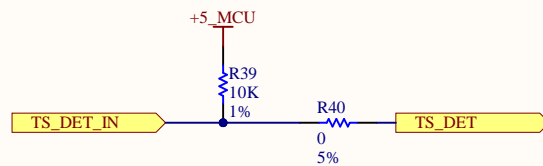
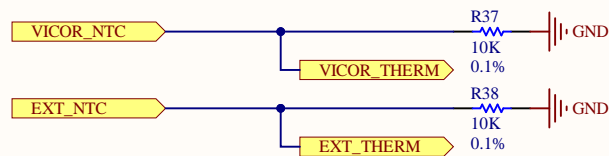
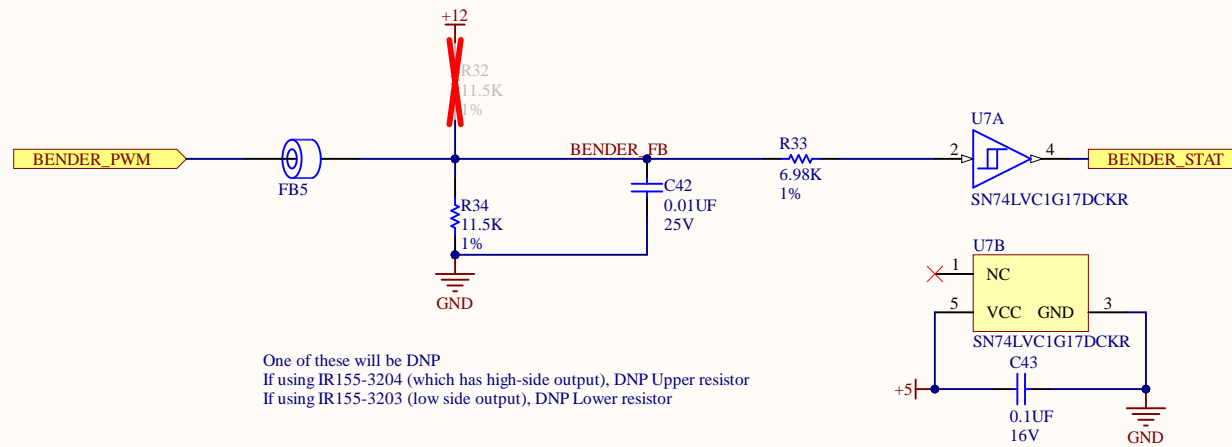
Sheet 5 of 7

File: C:\git\AERO\_2019-2020\HV Interface\MCU.SchDoc

**AERO**

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Title: **IO.SchDoc**

Desc: \*

Size: Letter

Auth: \*

Proj: \*

Date: 2/29/2020

10:59:28 PM

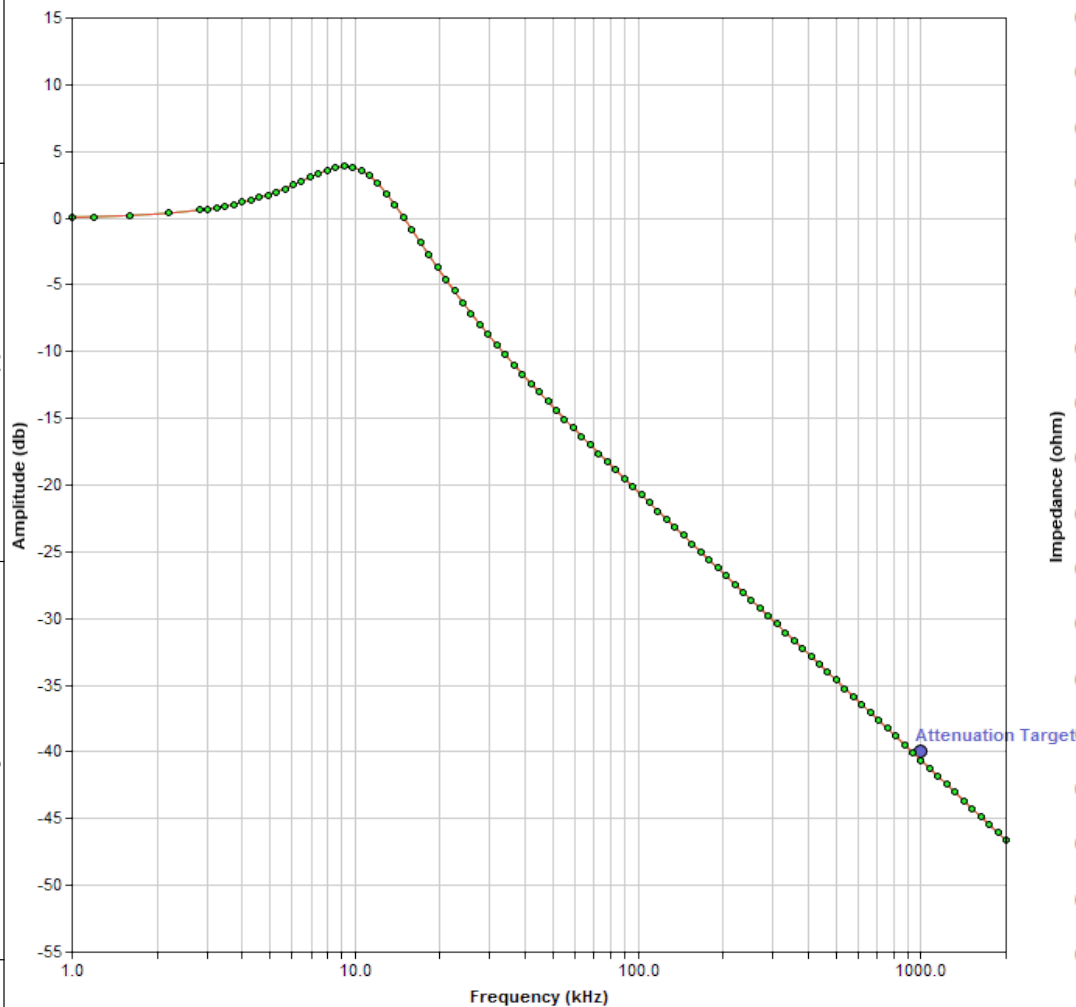
Sheet 7 of 7

File: C:\git\AERO\_2019-2020\HV Interface\IO.SchDoc

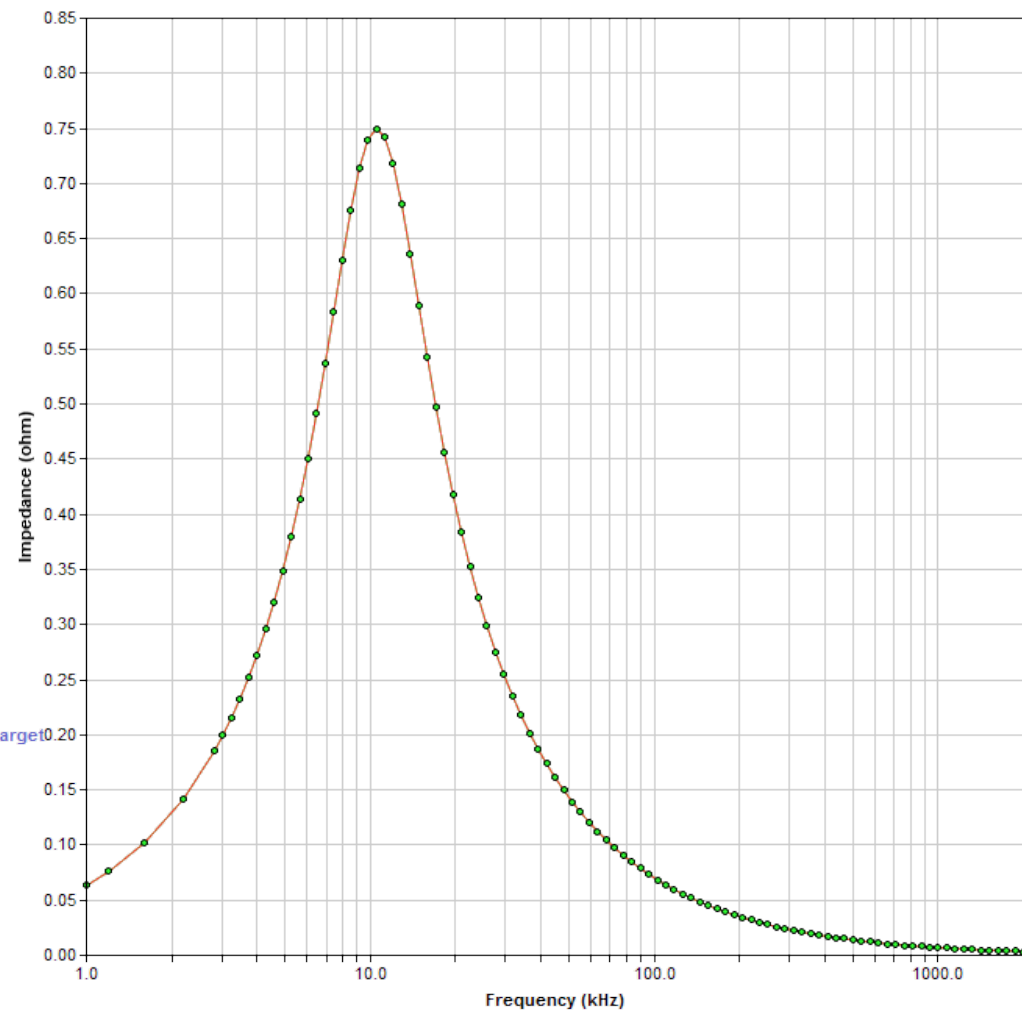
[www.uvmaero.org](http://www.uvmaero.org)

# Input Filtering

## Transfer Function

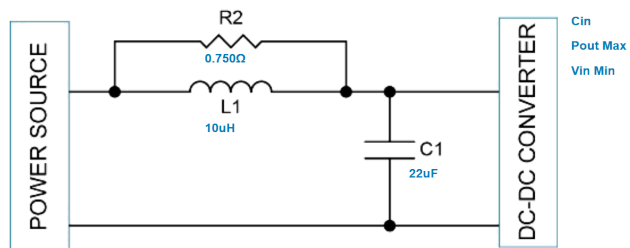


## Output Impedance



### Filter Goal

Attenuation  dB  
Frequency  Hz  
Topology   
Regulated



Cin 0.8uF  
Pout Max 470.0W  
Vin Min 36.0V

### Result

Meets attenuation Goal Yes  
Optimally Damped Yes  
Stable Yes  
Message

<http://app2.vicorpower.com/filterDesign/intiFilter.do>

You have a working filter now! See Transfer Function graph to see the filtering effect.