

Title: **CAN.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:28 PM

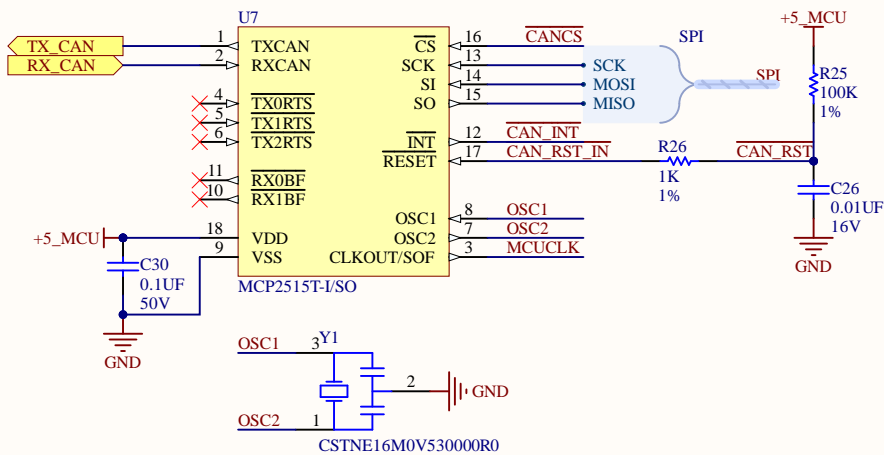
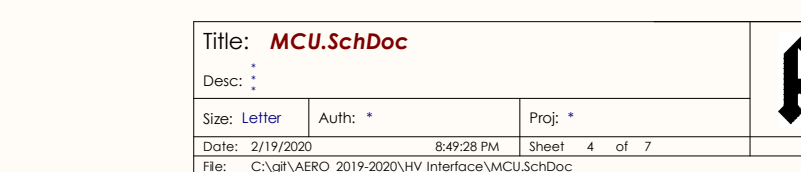
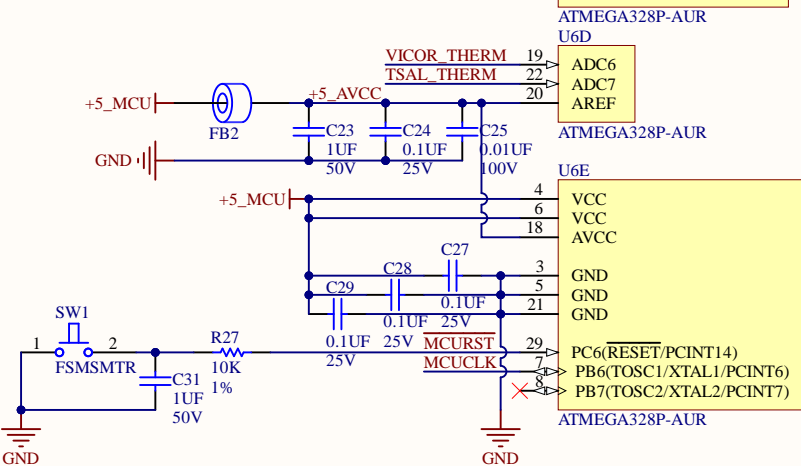
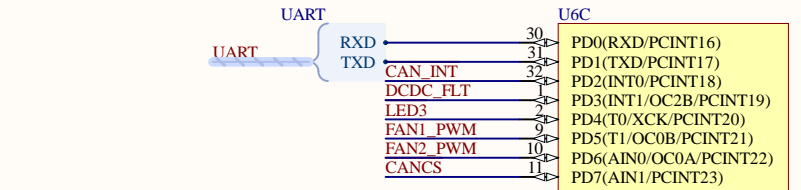
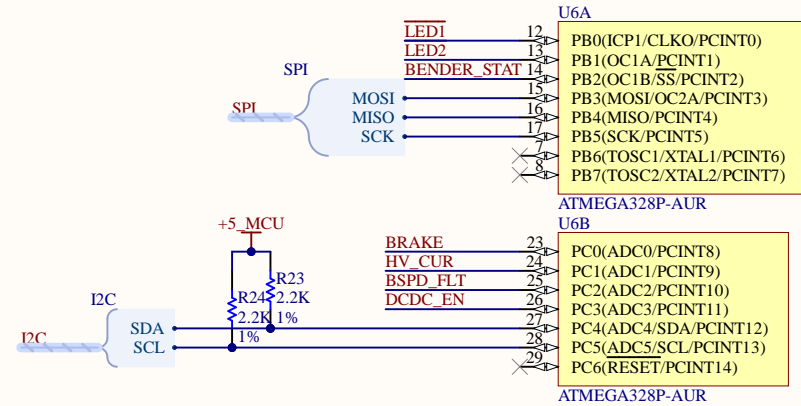
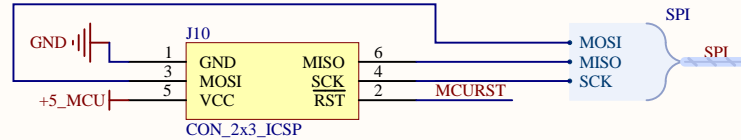
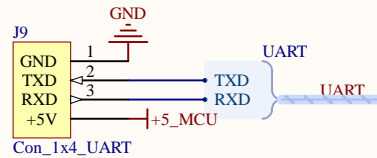
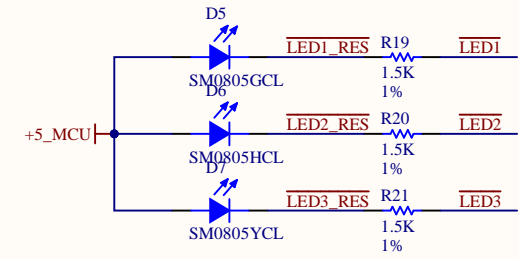
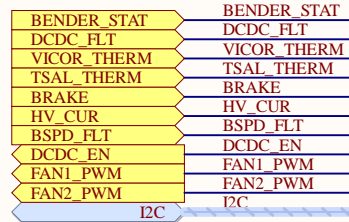
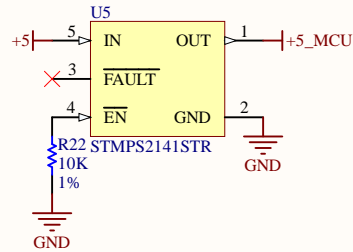
Sheet 3 of 7

File: C:\git\AERO_2019-2020\HV Interface\CAN.SchDoc

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Power for upload wont power the rest of board
Prevents killing programmer



Title: **MCU.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

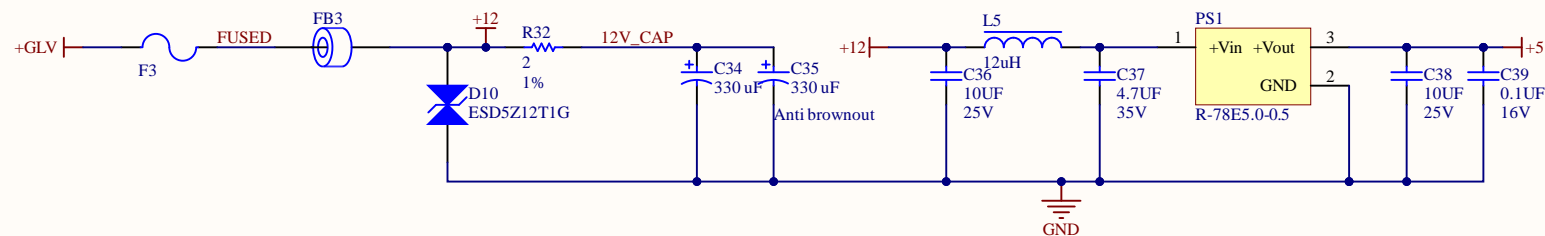
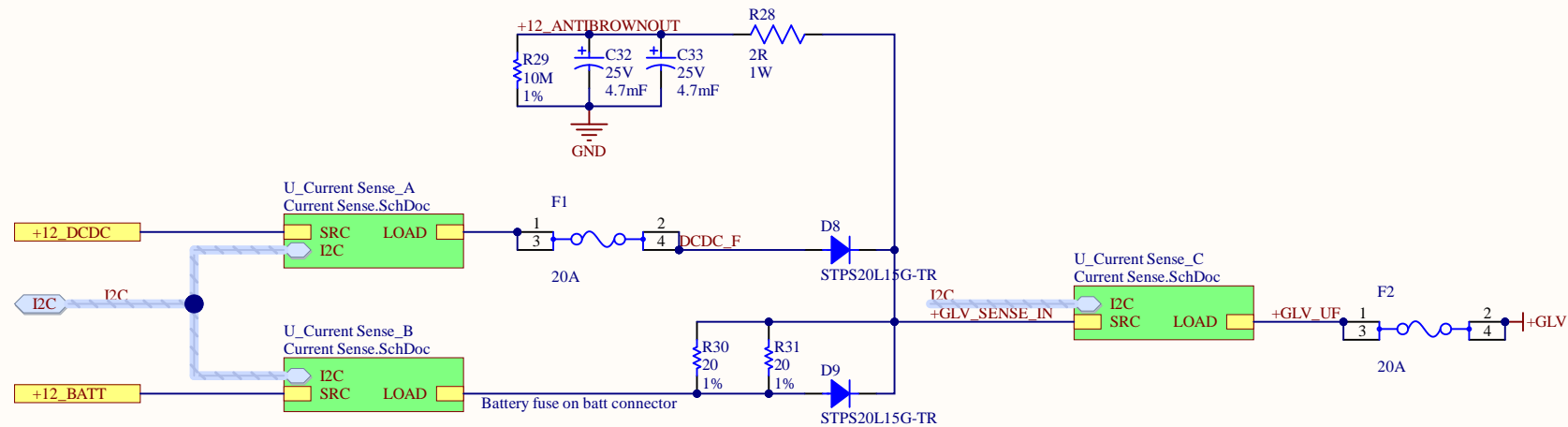
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Sheet 4 of 7

File: C:\git\AERO_2019-2020\HV Interface\MCU.SchDoc



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Title: **PWR_DIST.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:28 PM

Sheet 5 of 7

File: C:\git\AERO_2019-2020\HV Interface\PWR_DIST.SchDoc

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△
Add info about chip

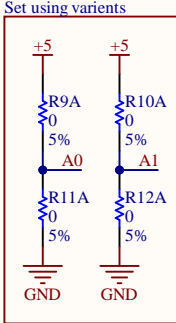
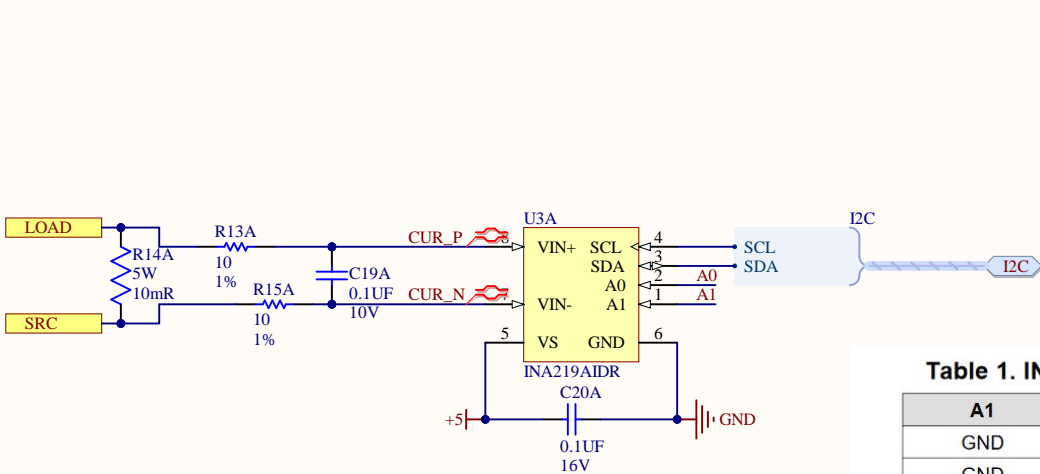


Table 1. INA219 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V _{S+}	GND	1000100
V _{S+}	V _{S+}	1000101
V _{S+}	SDA	1000110
V _{S+}	SCL	1000111
SDA	GND	1001000
SDA	V _{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Consider testing with adafruit board first??

Title: **Current Sense.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:28 PM

Sheet 6 of 7

File: C:\git\AERO_2019-2020\HV Interface\Current Sense.SchDoc



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△
Add info about chip

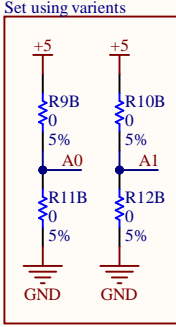
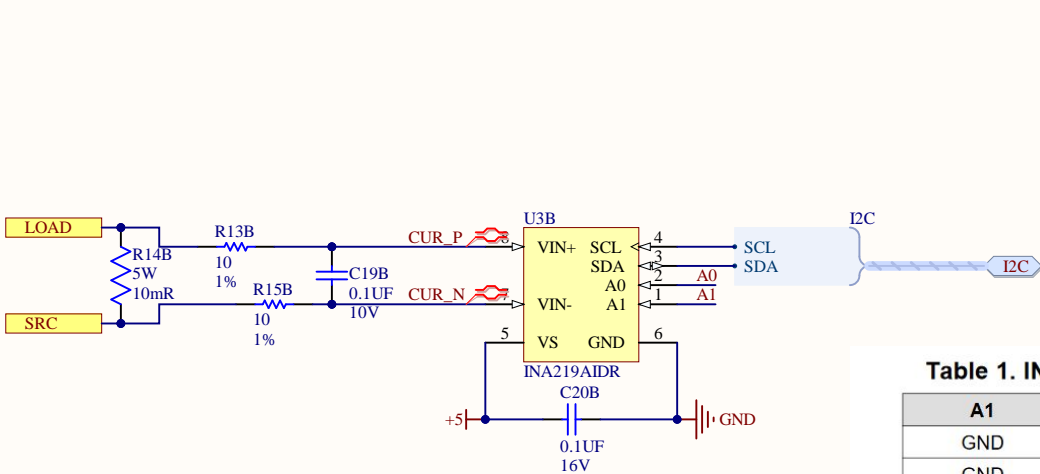


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A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V _{S+}	GND	1000100
V _{S+}	V _{S+}	1000101
V _{S+}	SDA	1000110
V _{S+}	SCL	1000111
SDA	GND	1001000
SDA	V _{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Consider testing with adafruit board first??

Title: **Current Sense.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:28 PM

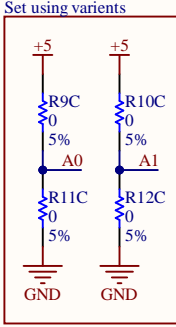
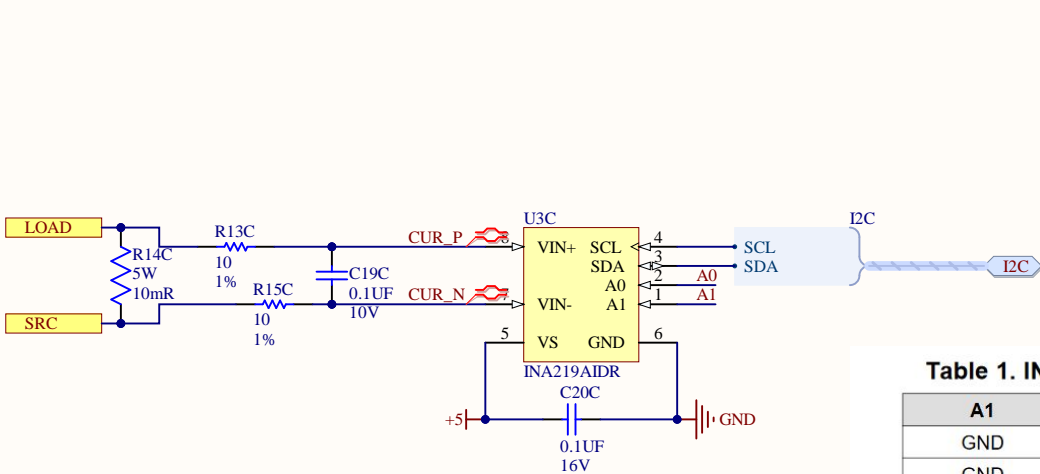
Sheet 6 of 7

File: C:\git\AERO_2019-2020\HV Interface\Current Sense.SchDoc



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△
Add info about chip



Consider testing with adafruit board first??

Table 1. INA219 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V _{S+}	GND	1000100
V _{S+}	V _{S+}	1000101
V _{S+}	SDA	1000110
V _{S+}	SCL	1000111
SDA	GND	1001000
SDA	V _{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Title: **Current Sense.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

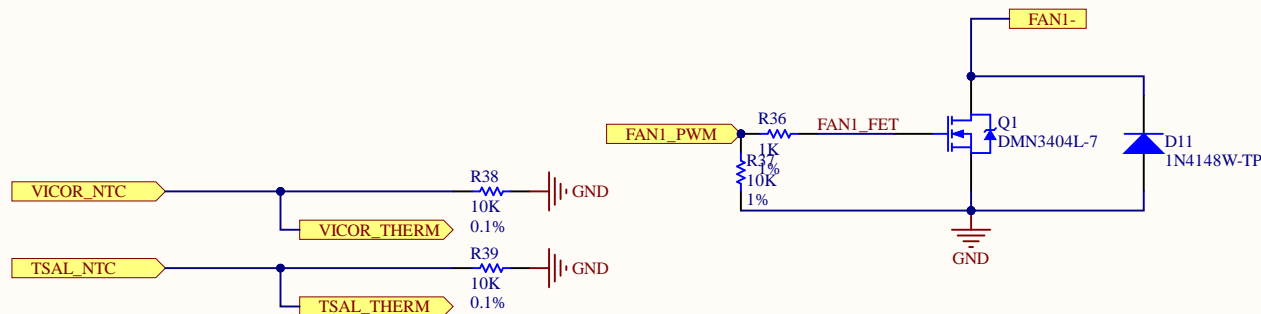
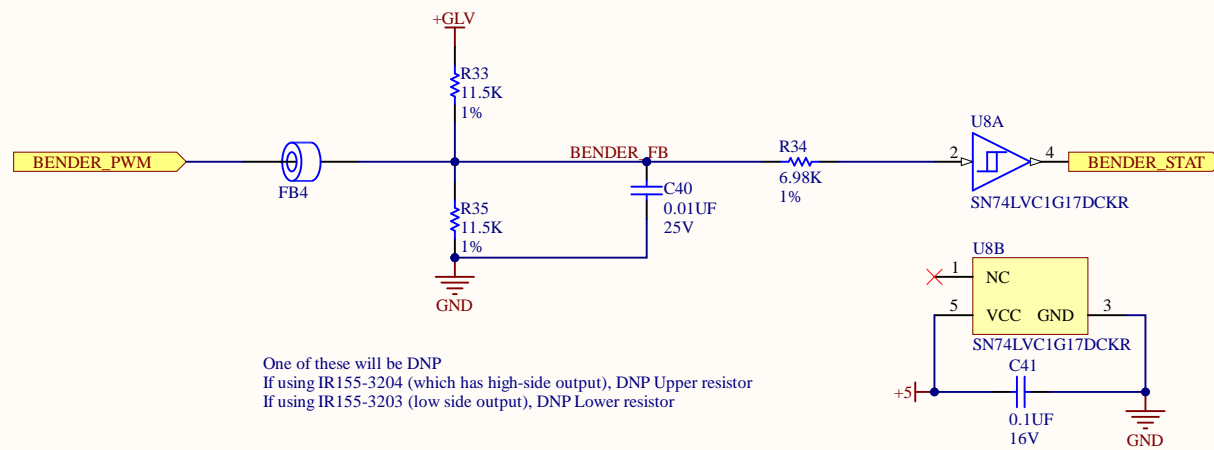
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Sheet 6 of 7

File: C:\git\AERO_2019-2020\HV Interface\Current Sense.SchDoc



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Title: **IO.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

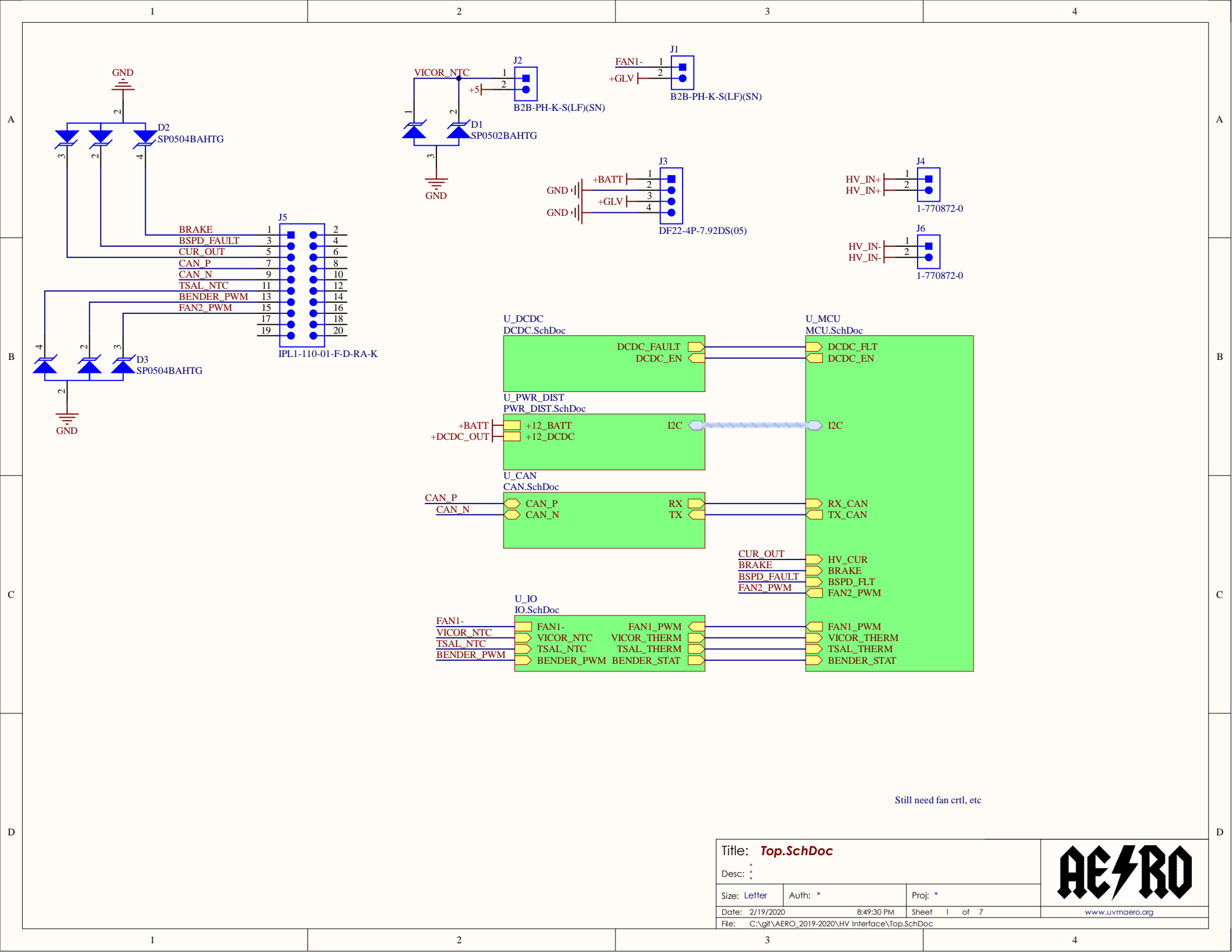
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Sheet 7 of 7

File: C:\git\AERO_2019-2020\HV Interface\IO.SchDoc

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Title: **Top.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

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Sheet 1 of 7

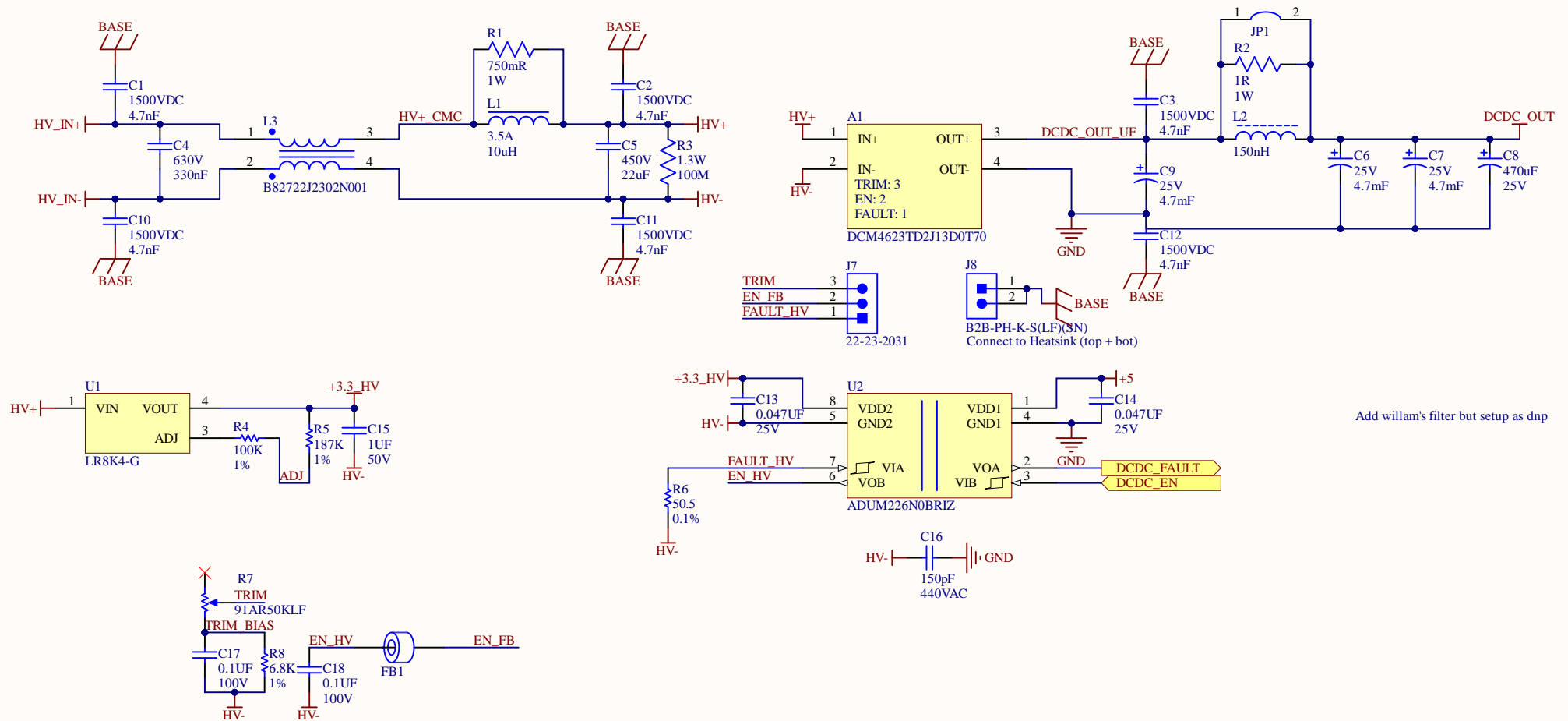
File: C:\git\AERO_2019-2020\HV Interface\Top.SchDoc



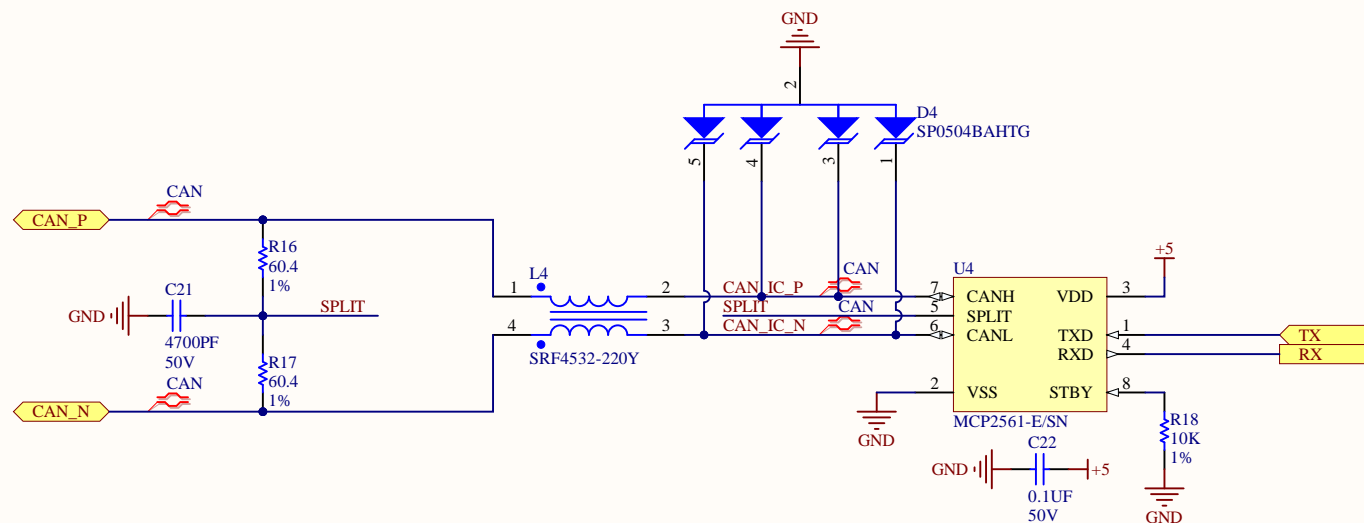
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Vicor says no output filter, just cap. Adding bulk storage anyway tho
 Should really bench test this tbh
 bench test willam's filter if i can
 Then again willam's DID work so....

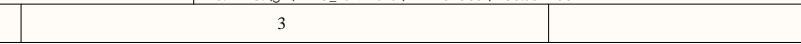
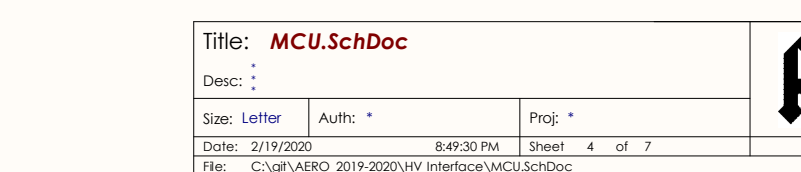
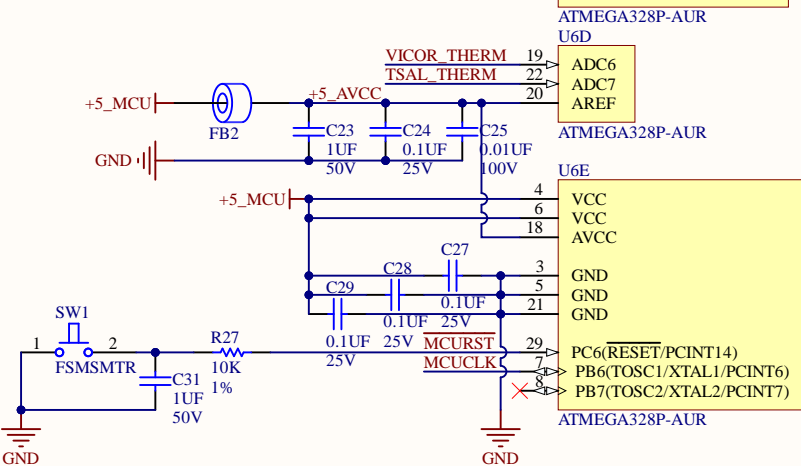
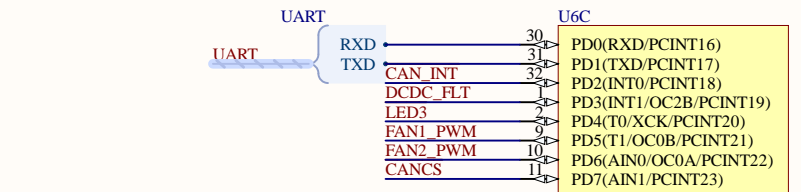
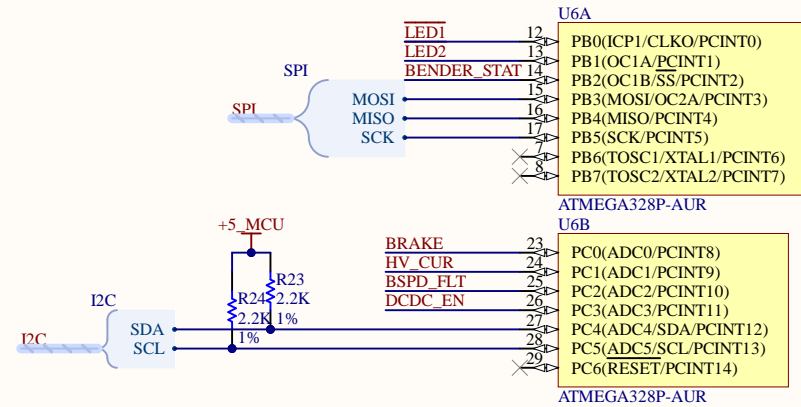
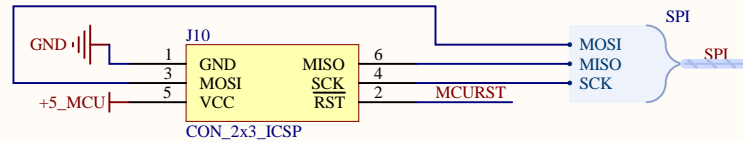
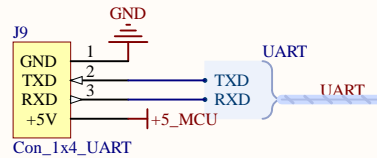
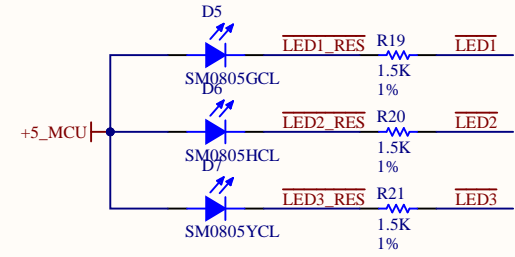
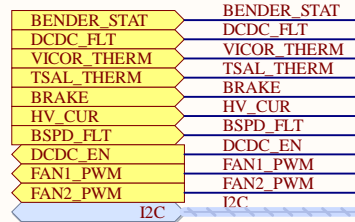
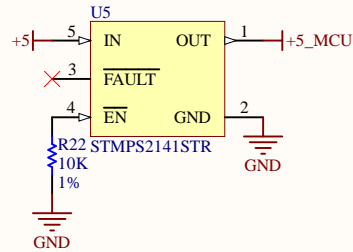
New filter design (see PDF)

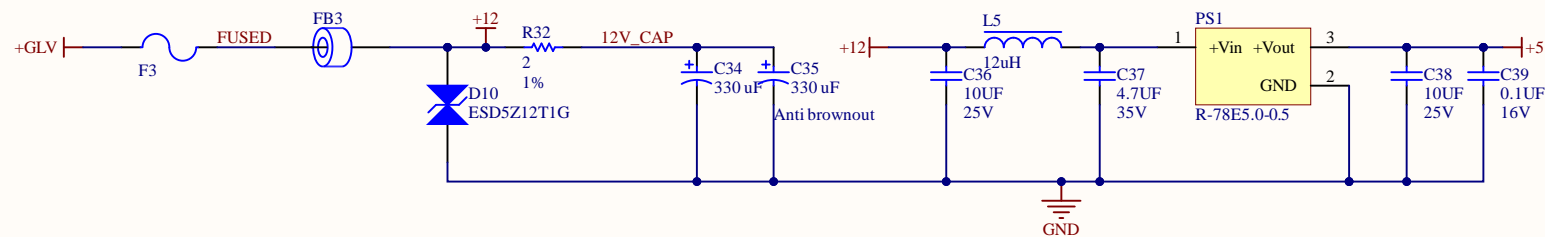
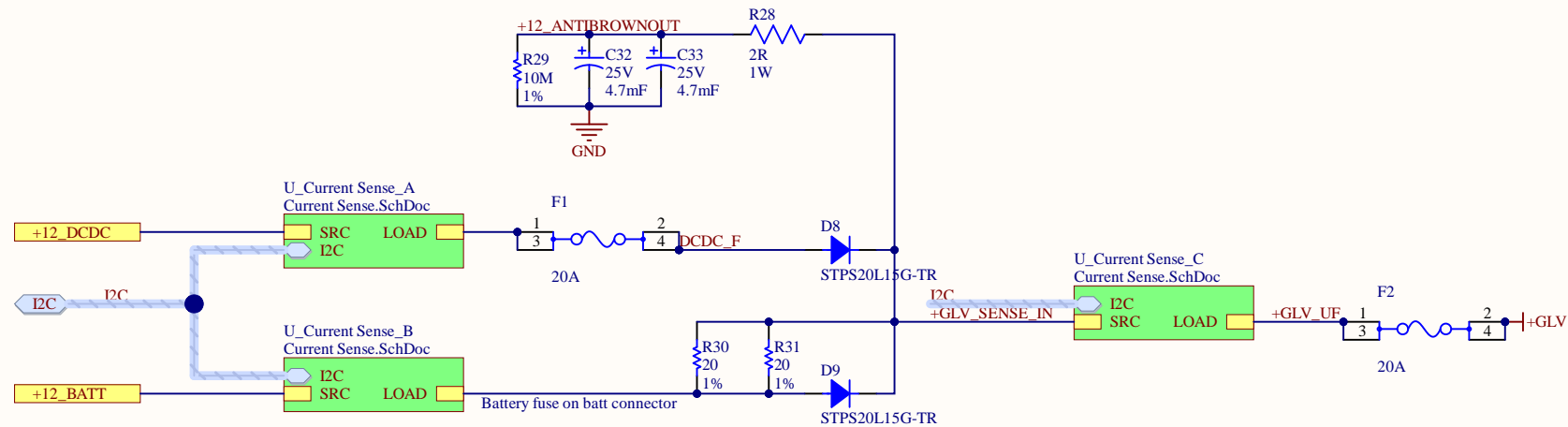


Add willam's filter but setup as dnp



Power for upload wont power the rest of board
Prevents killing programmer





Title: **PWR_DIST.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:30 PM

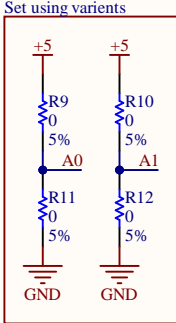
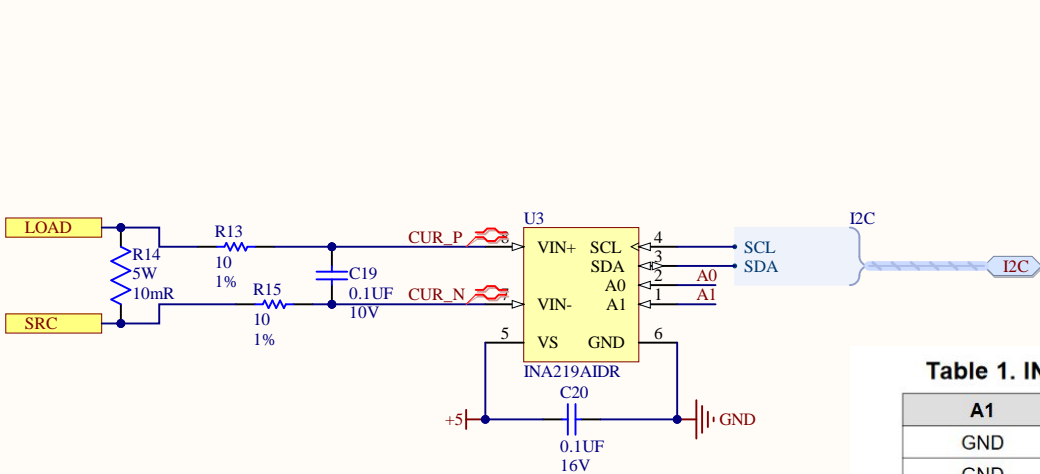
Sheet 5 of 7

File: C:\git\AERO_2019-2020\HV Interface\PWR_DIST.SchDoc

AERO

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△
Add info about chip



Consider testing with adafruit board first??

Table 1. INA219 Address Pins and Slave Addresses

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V _{S+}	V _{S+}	1000101
V _{S+}	SDA	1000110
V _{S+}	SCL	1000111
SDA	GND	1001000
SDA	V _{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Title: **Current Sense.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

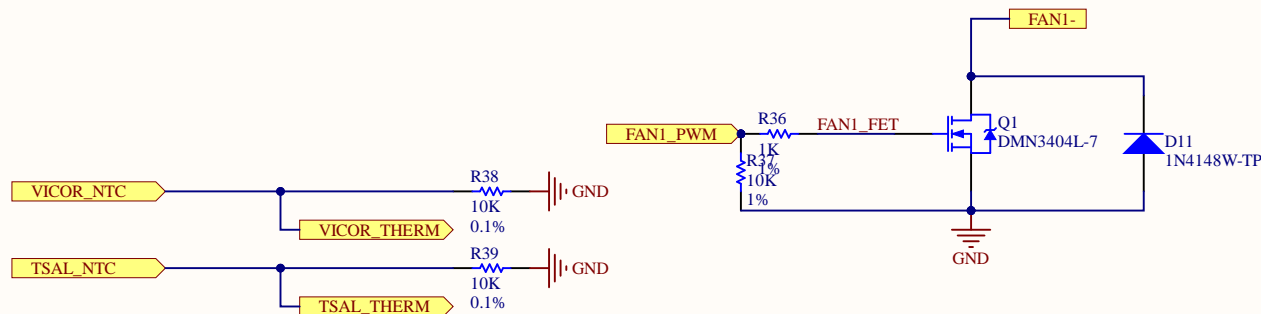
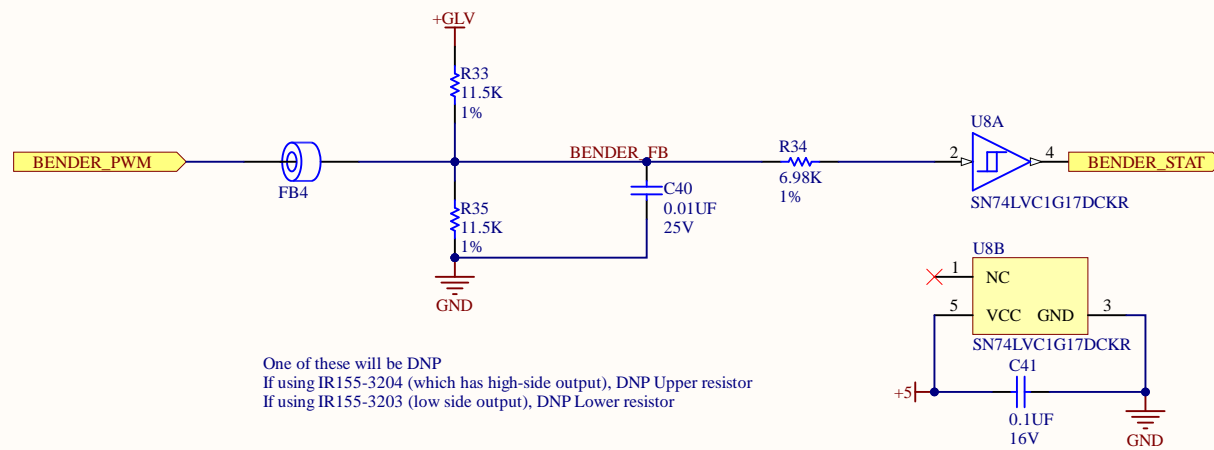
8:49:30 PM

Sheet 6 of 7

File: C:\git\AERO_2019-2020\HV Interface\Current Sense.SchDoc



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Title: **IO.SchDoc**

Desc: *

Size: Letter

Auth: *

Proj: *

Date: 2/19/2020

8:49:30 PM

Sheet 7 of 7

File: C:\git\AERO_2019-2020\HV Interface\IO.SchDoc

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