

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
❖	2	39.37mil (1.000mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c100hn100m0p354
∇	2	125.00mil (3.175mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c318hn318
	4	55.00mil (1.397mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	8 Total							

	Top Solder	SM-001	1.00mil	4	
1	Top Layer	Copper	1.40mil		
	Dielectric 1	FR-4	56.00mil	4.2	
2	Bottom Layer	Copper	1.40mil		
	Bottom Solder	SM-001	1.00mil	4	
	Bottom Overlay				

Material Thickness Constant Board Layer Stack

40.647mm	R 1.600mm
I VII VII I I I I I I I I I I I I I I I	
1 S S S S S S S S S S S S S S S S S S S	326mm
10 Muldicatar	
Andrewide HV — O O O O O O O O O O O O O O O O O O	V
	R 1.905mm

Title 60U	HV Indicator	Designer: Andrew Katz	
Size: Letter	Number:	Revision:	aakatz3@gmail.com *
Date:	Time: 2/7/2020	Sheet of	*
File: 60V_Ind.	PcbDoc		

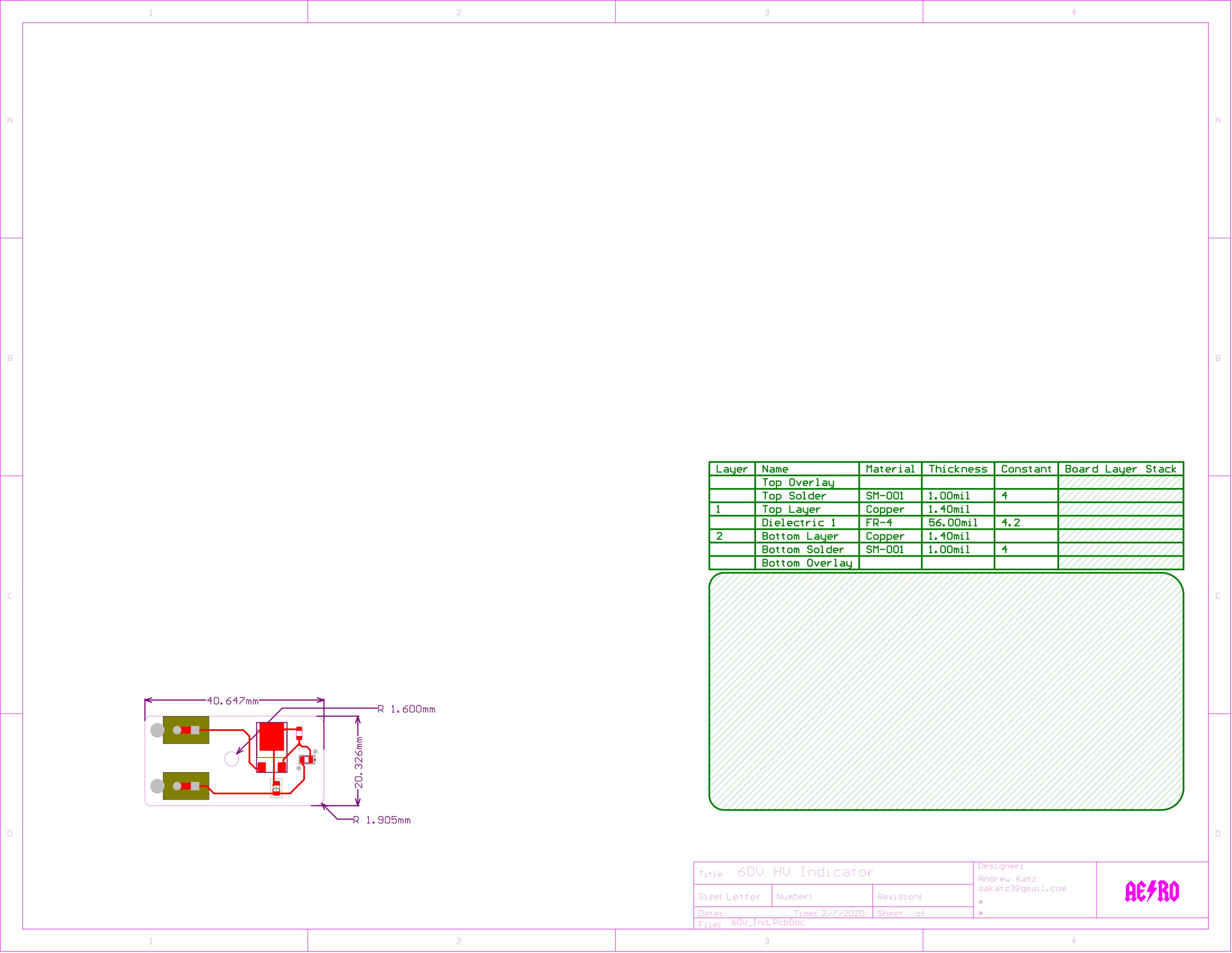
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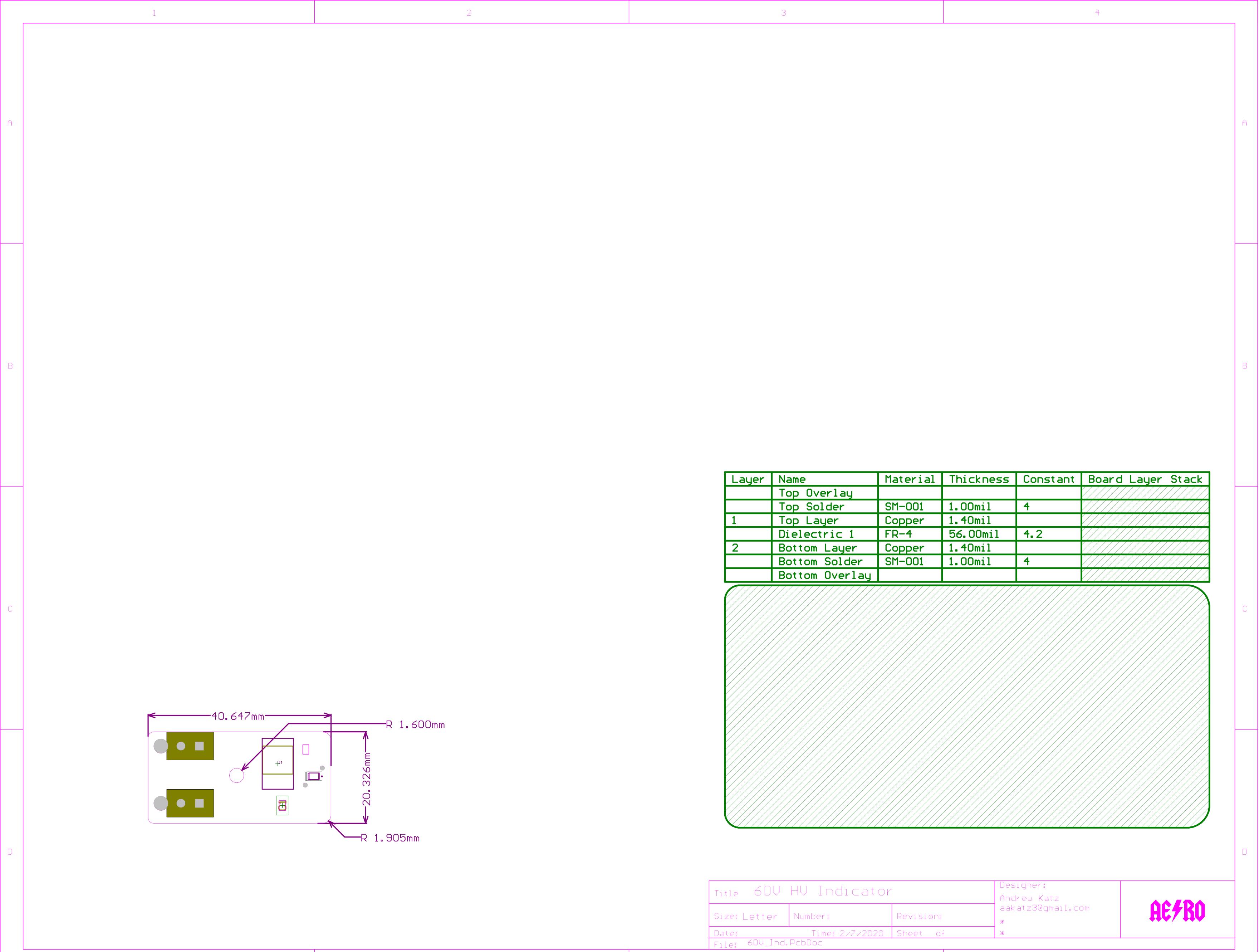
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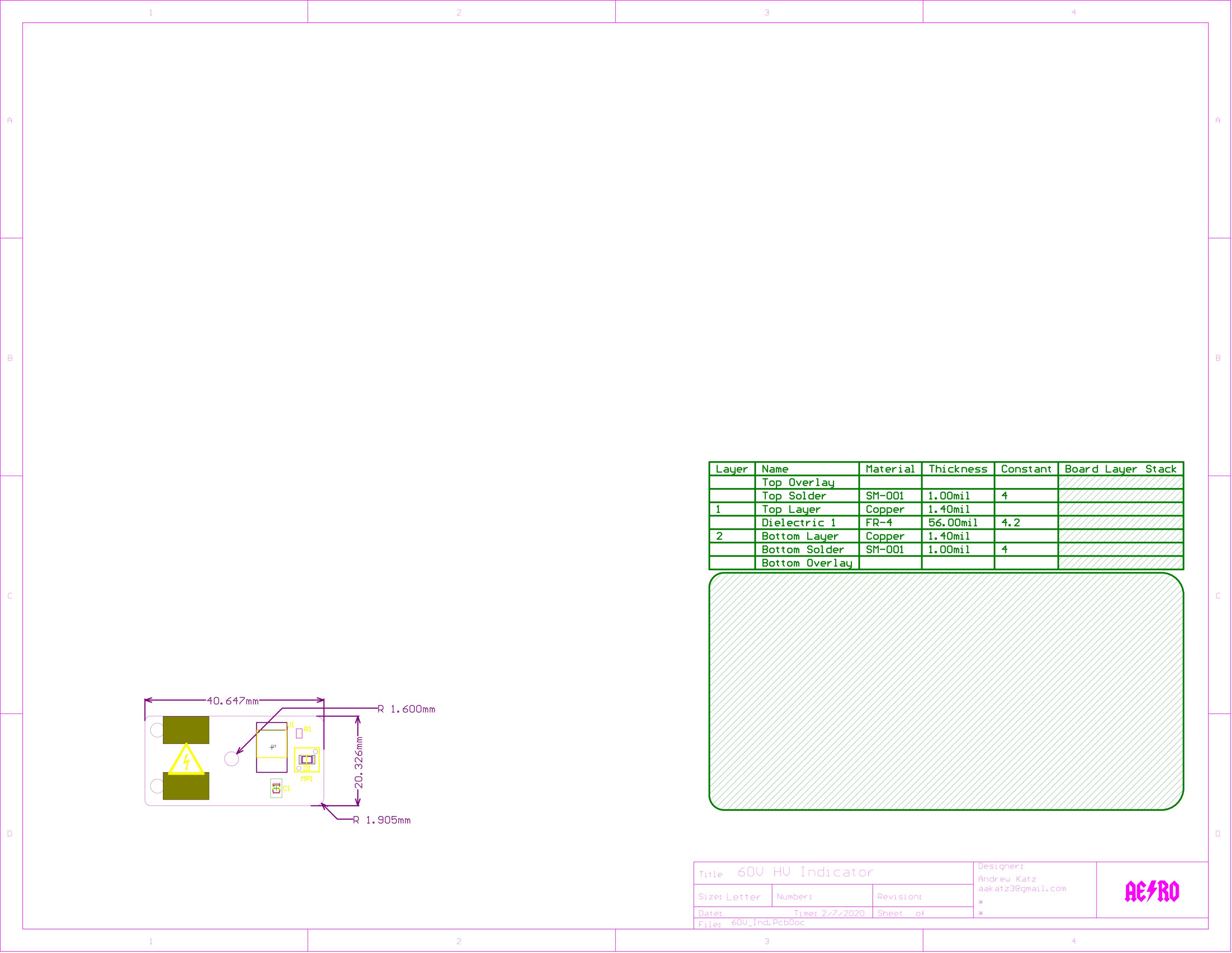
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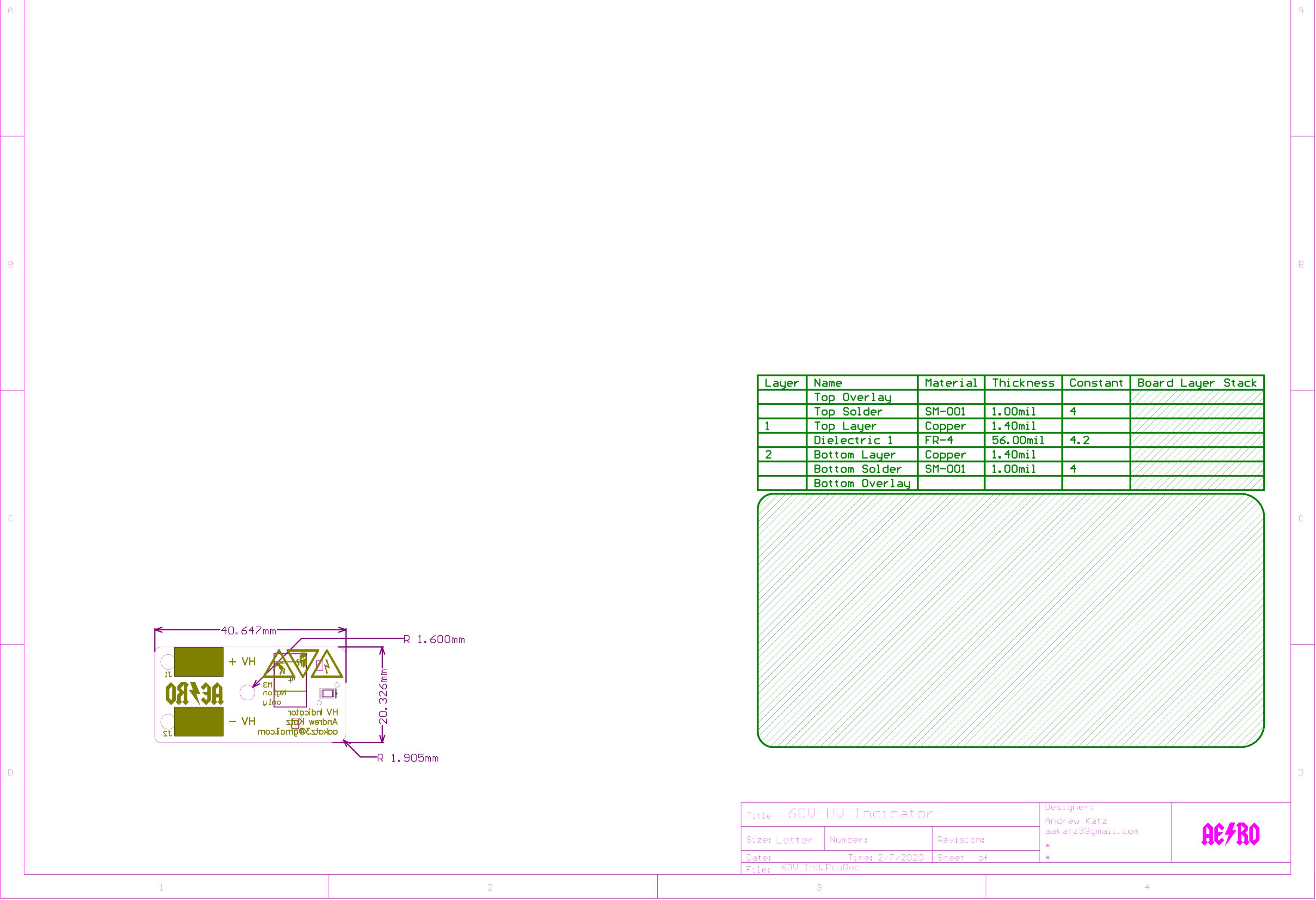
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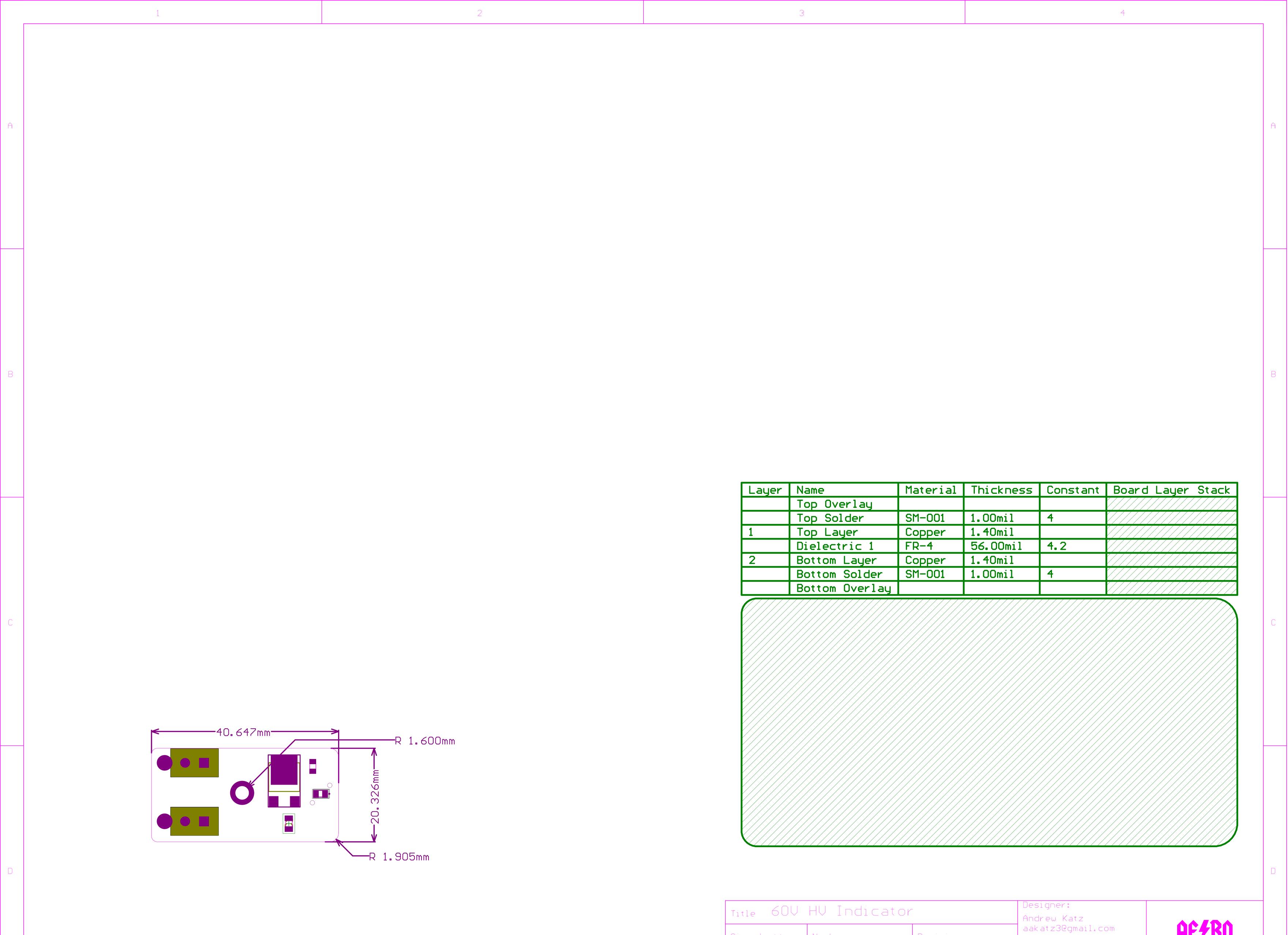
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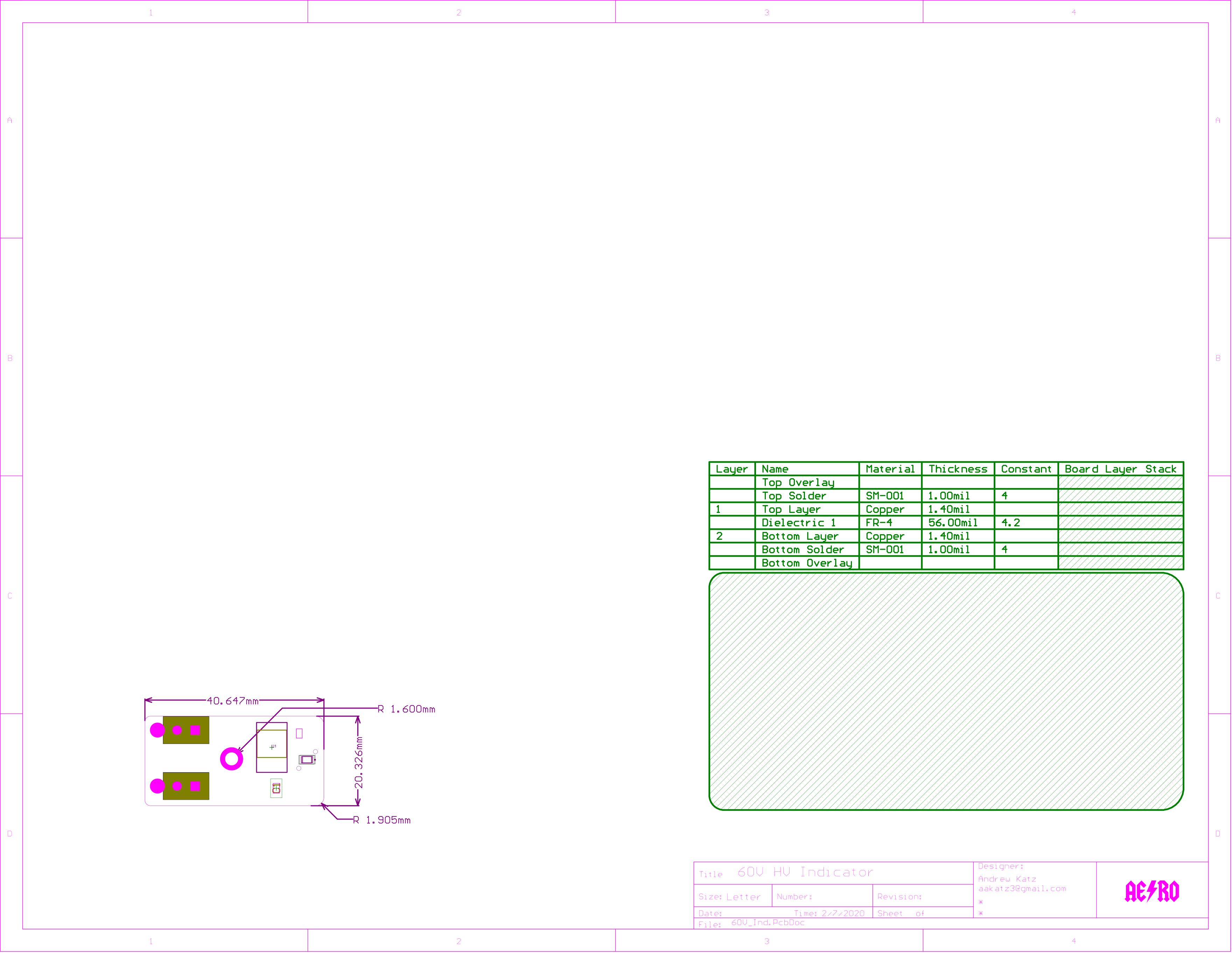


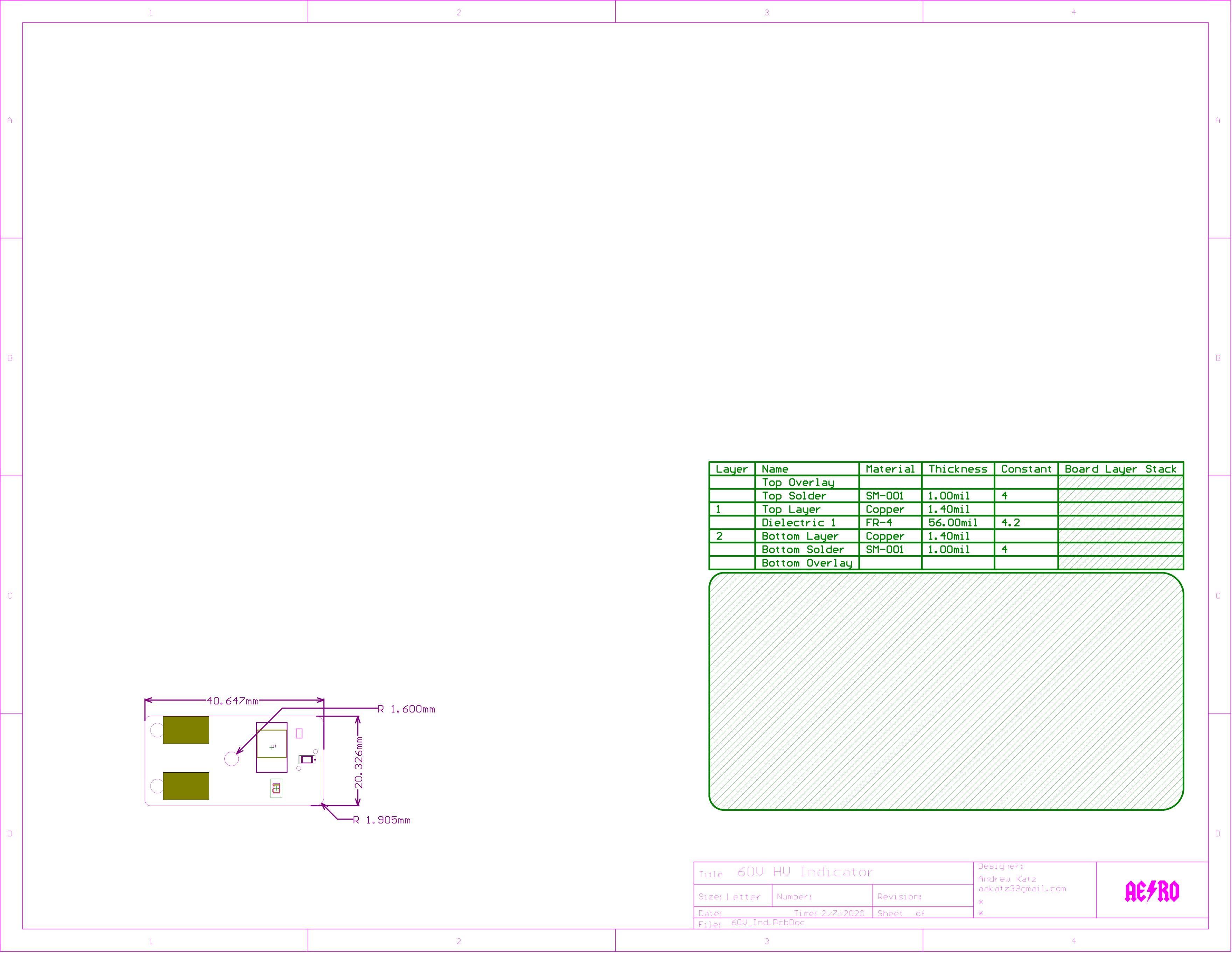
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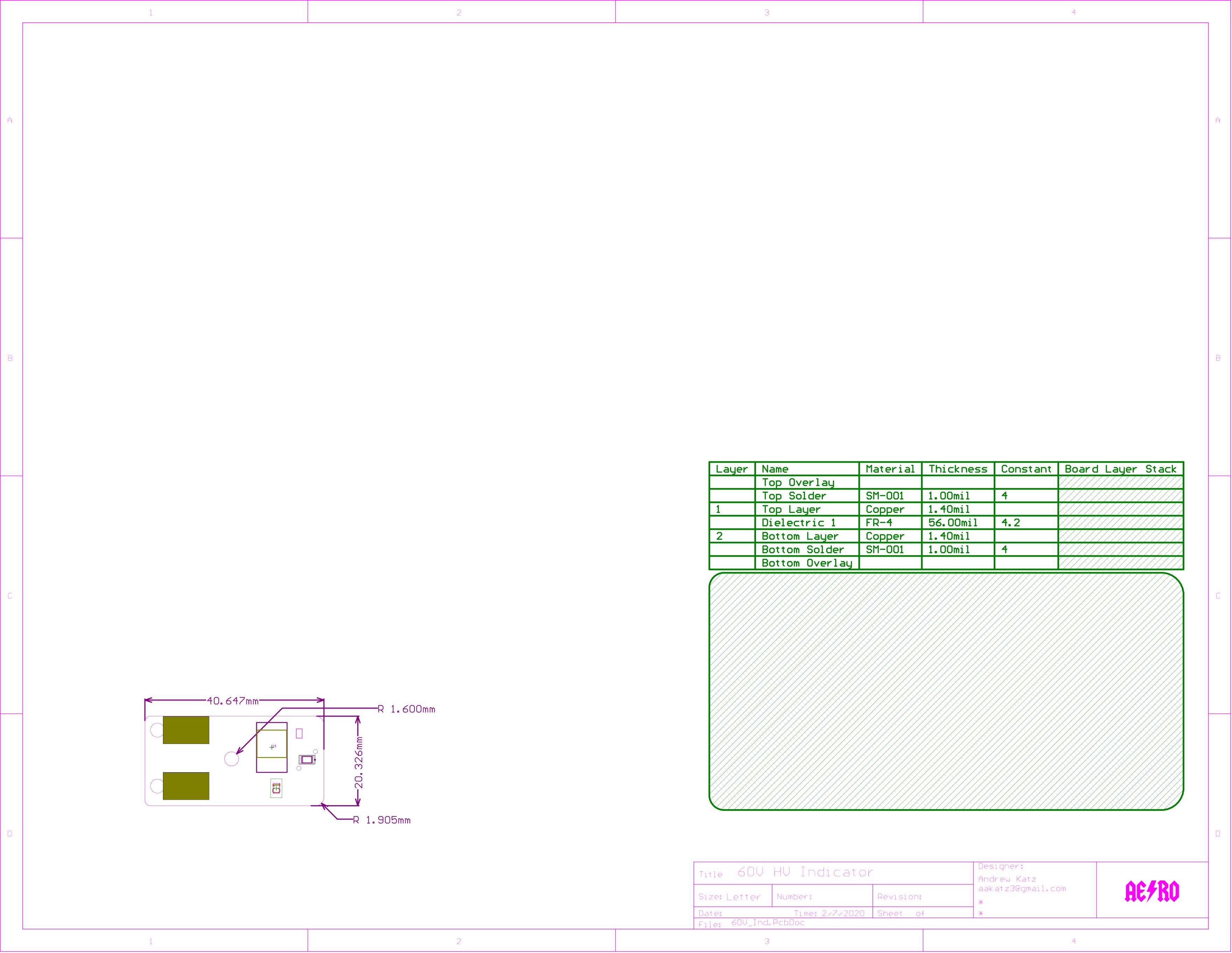
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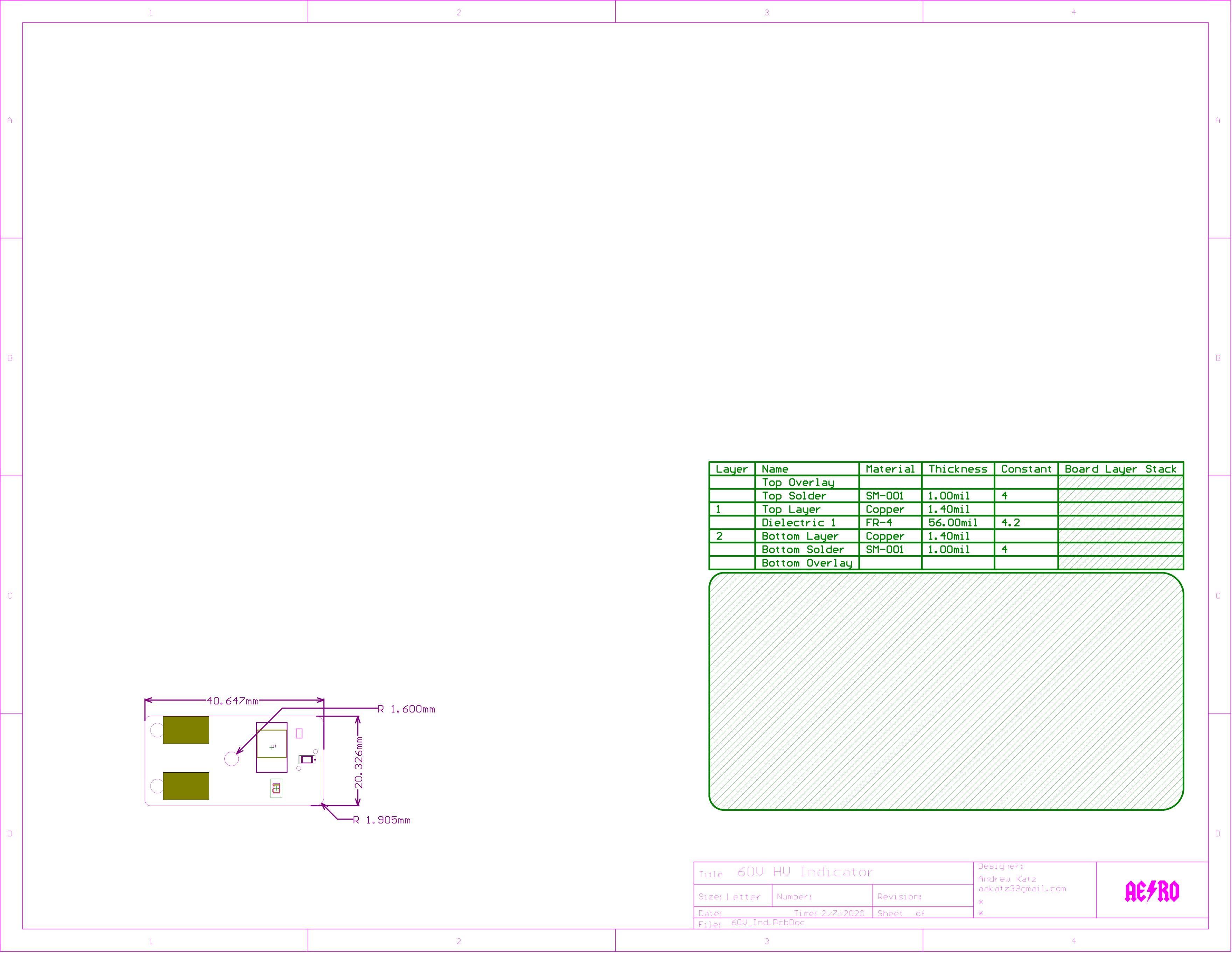
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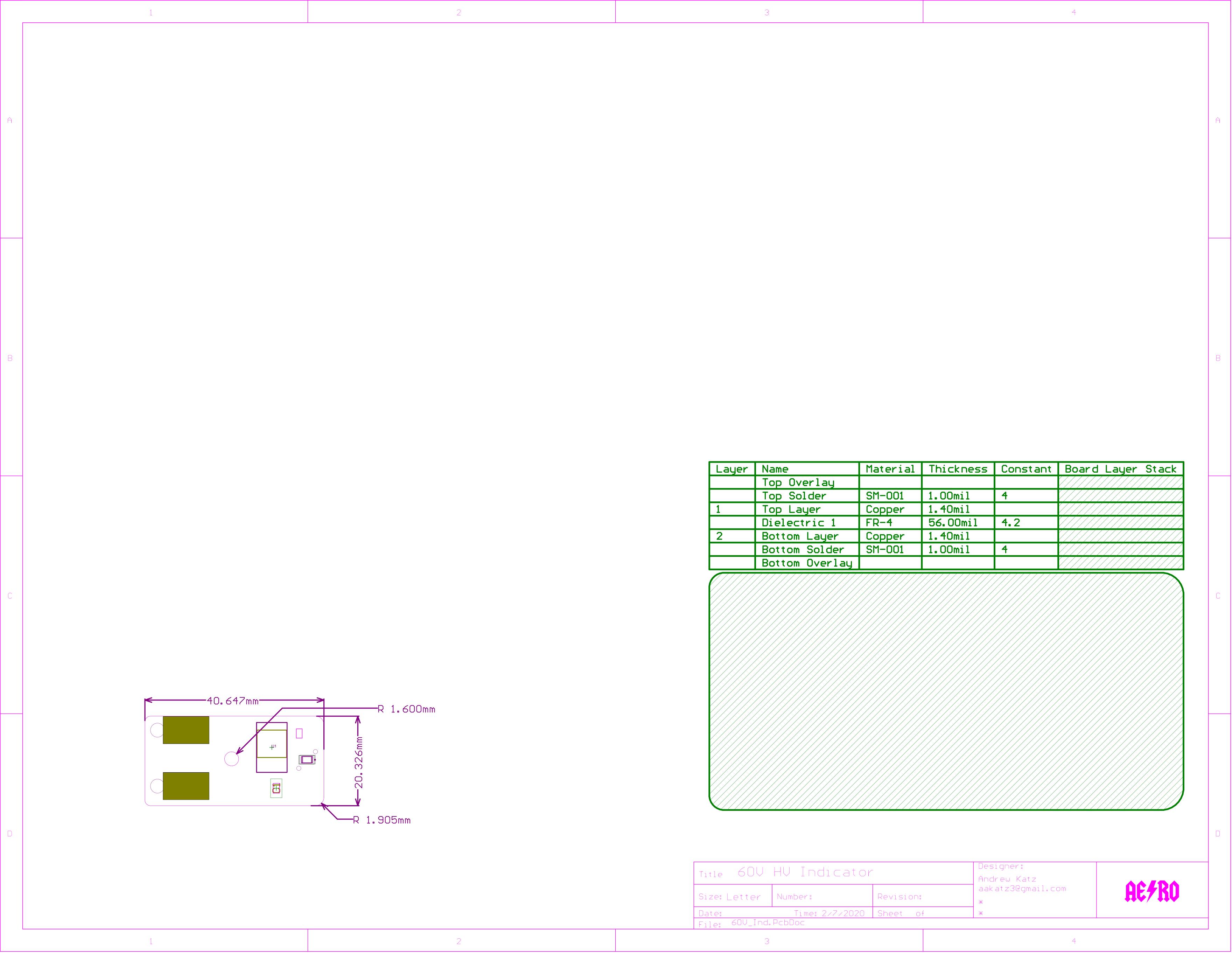
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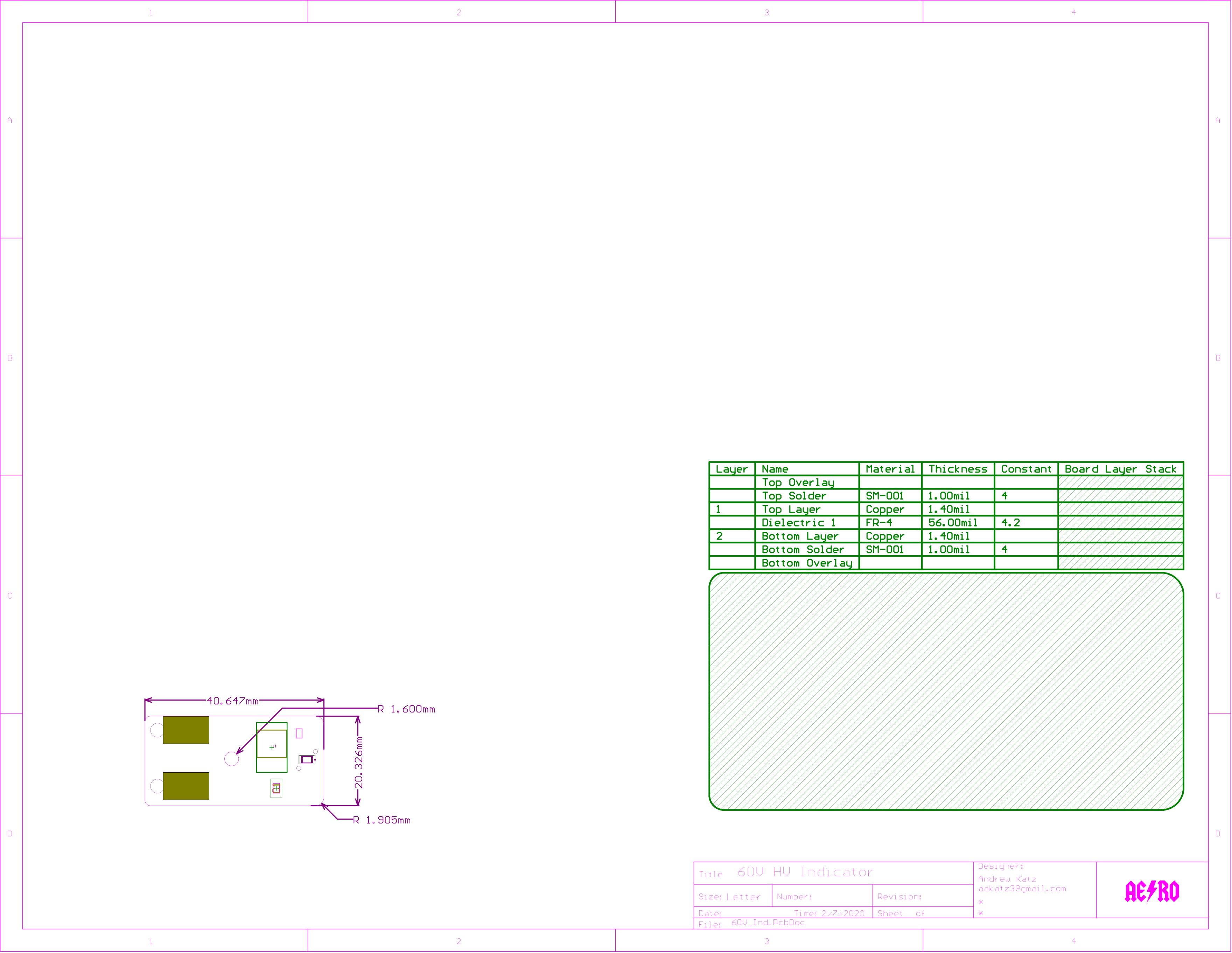


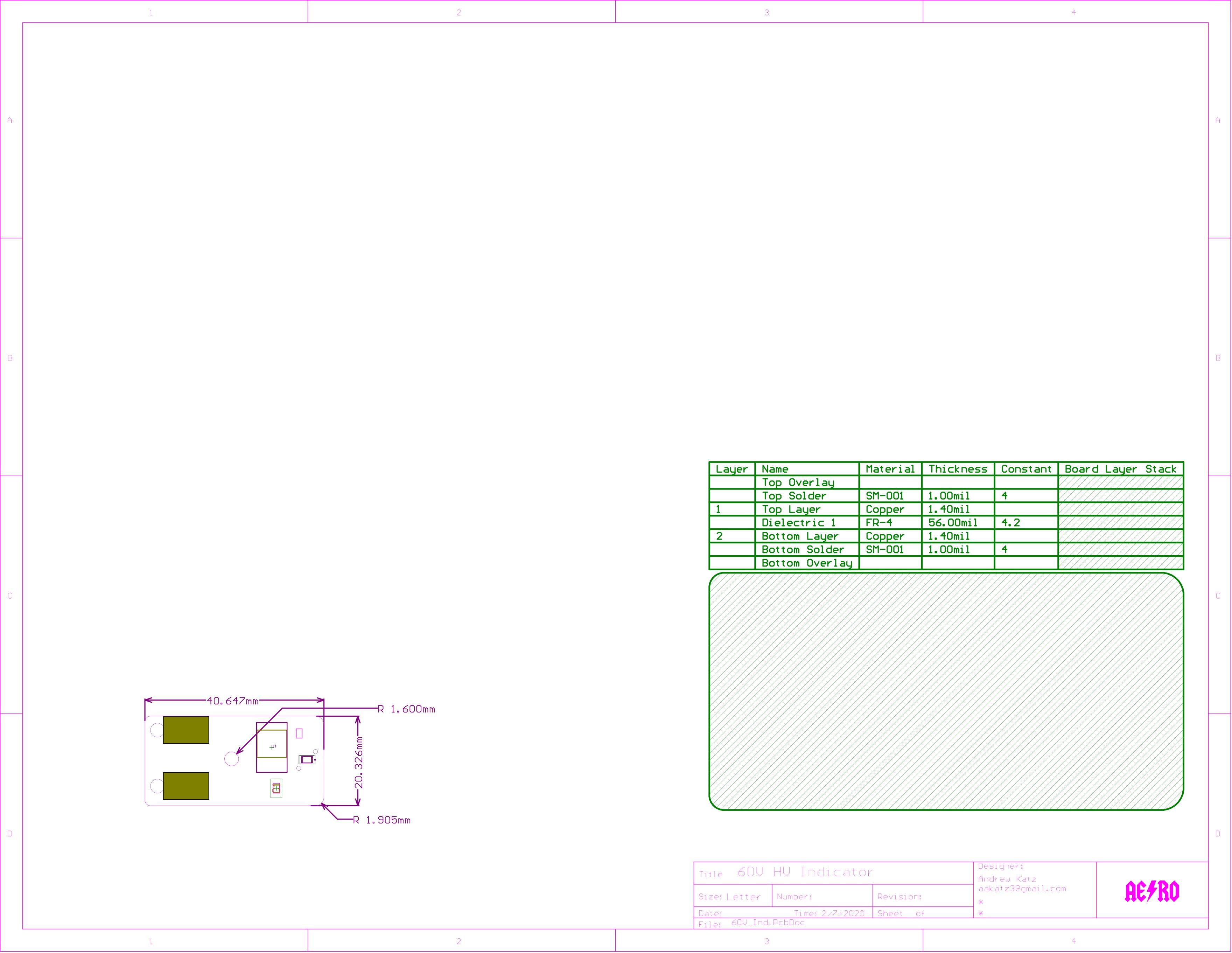


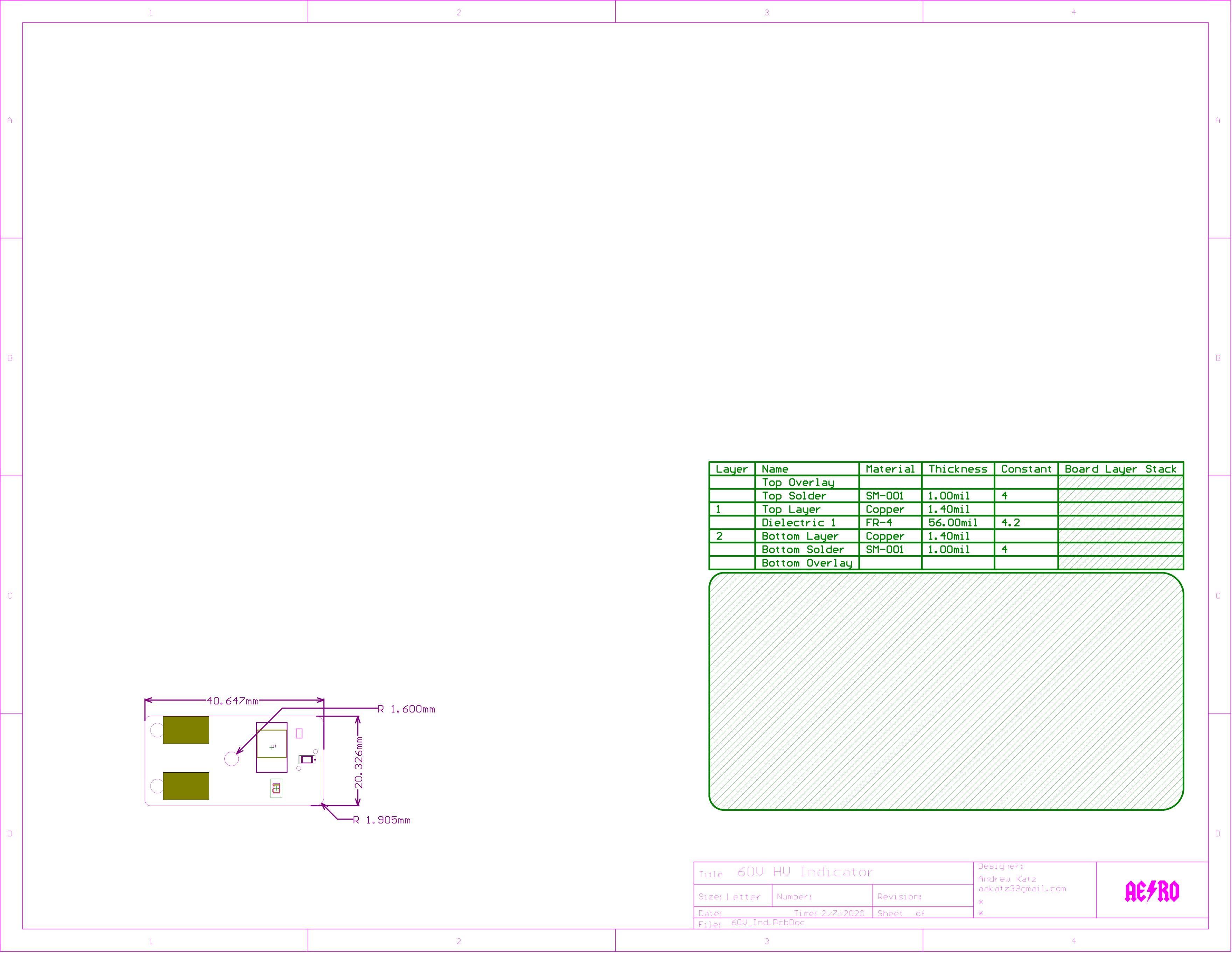


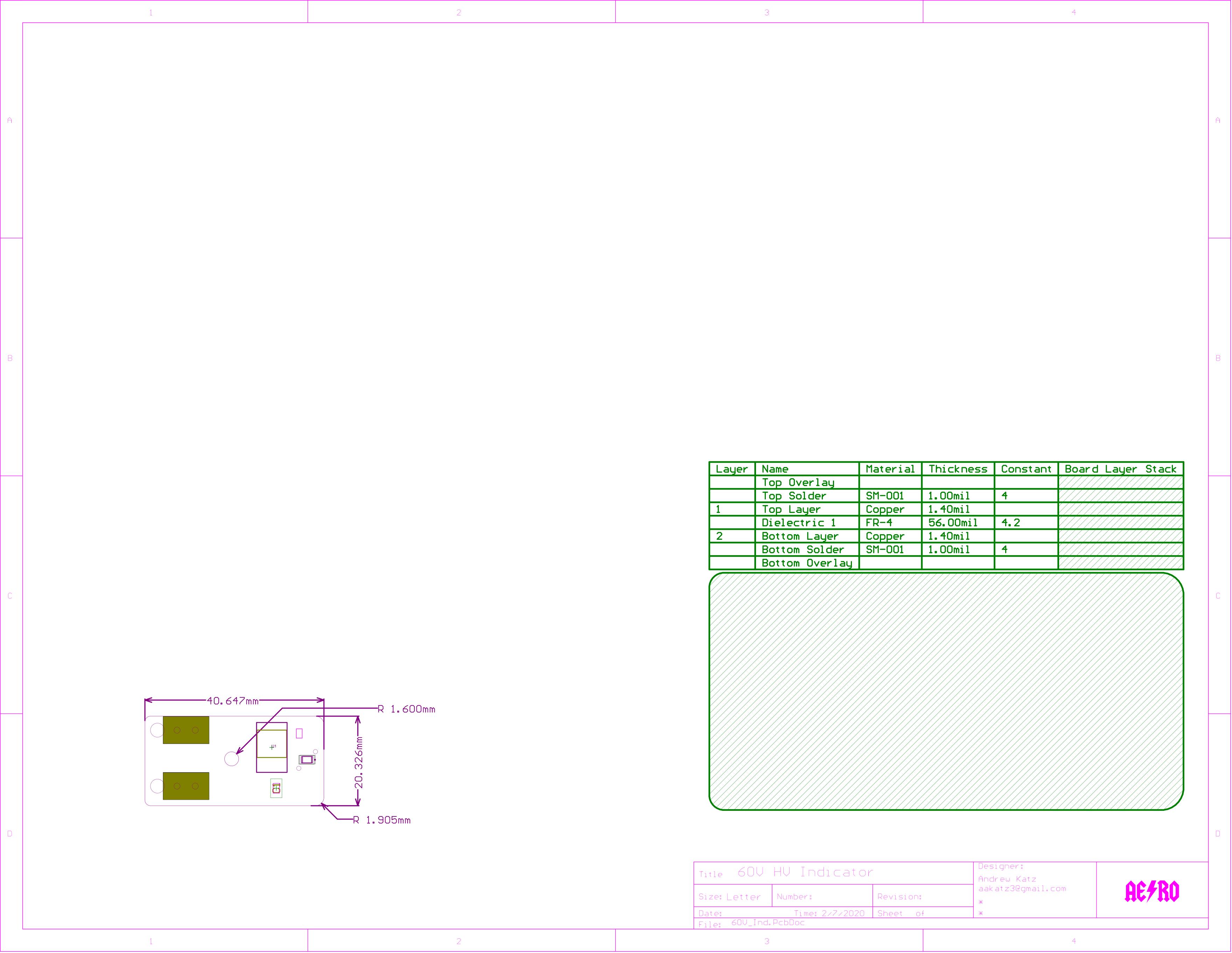


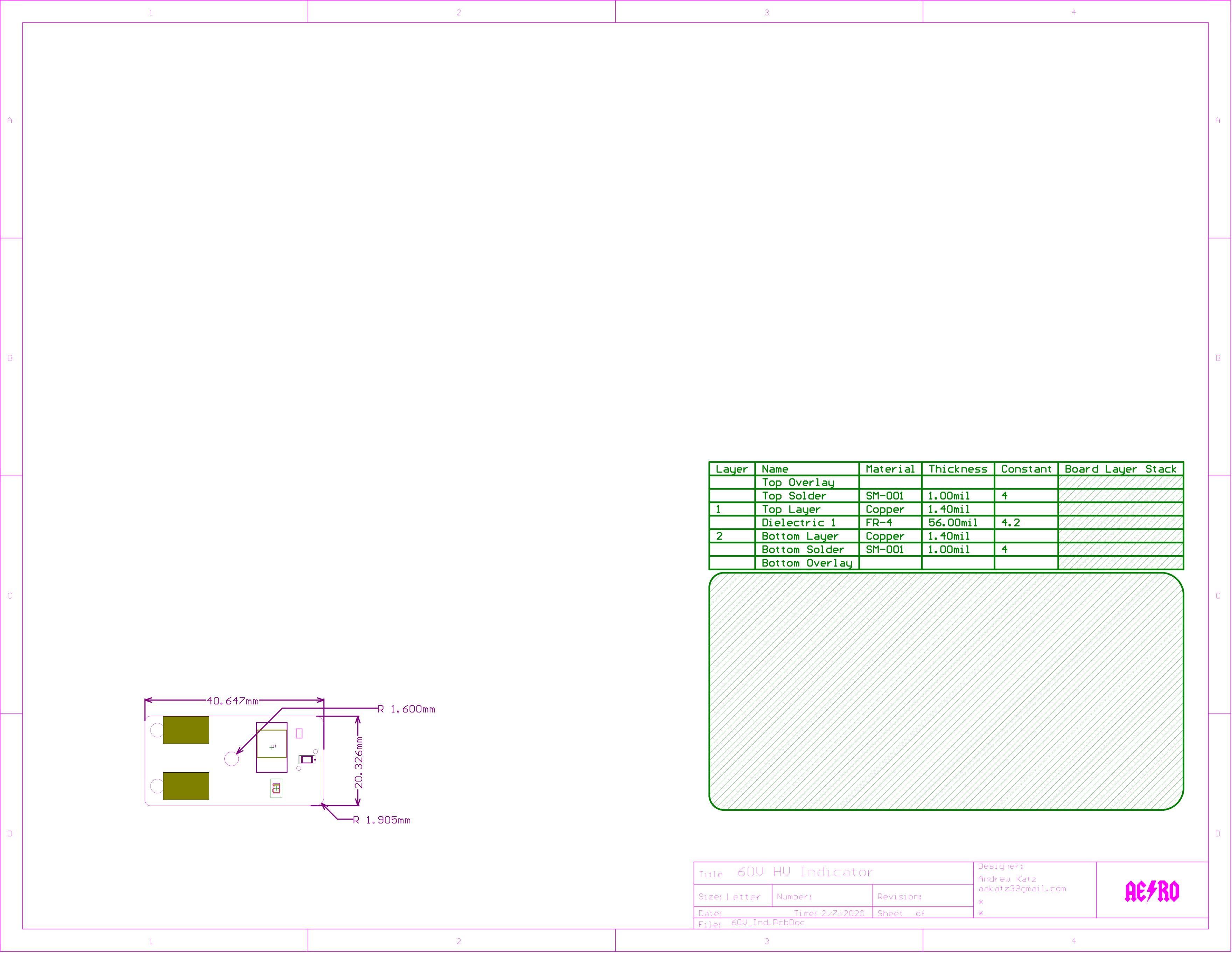


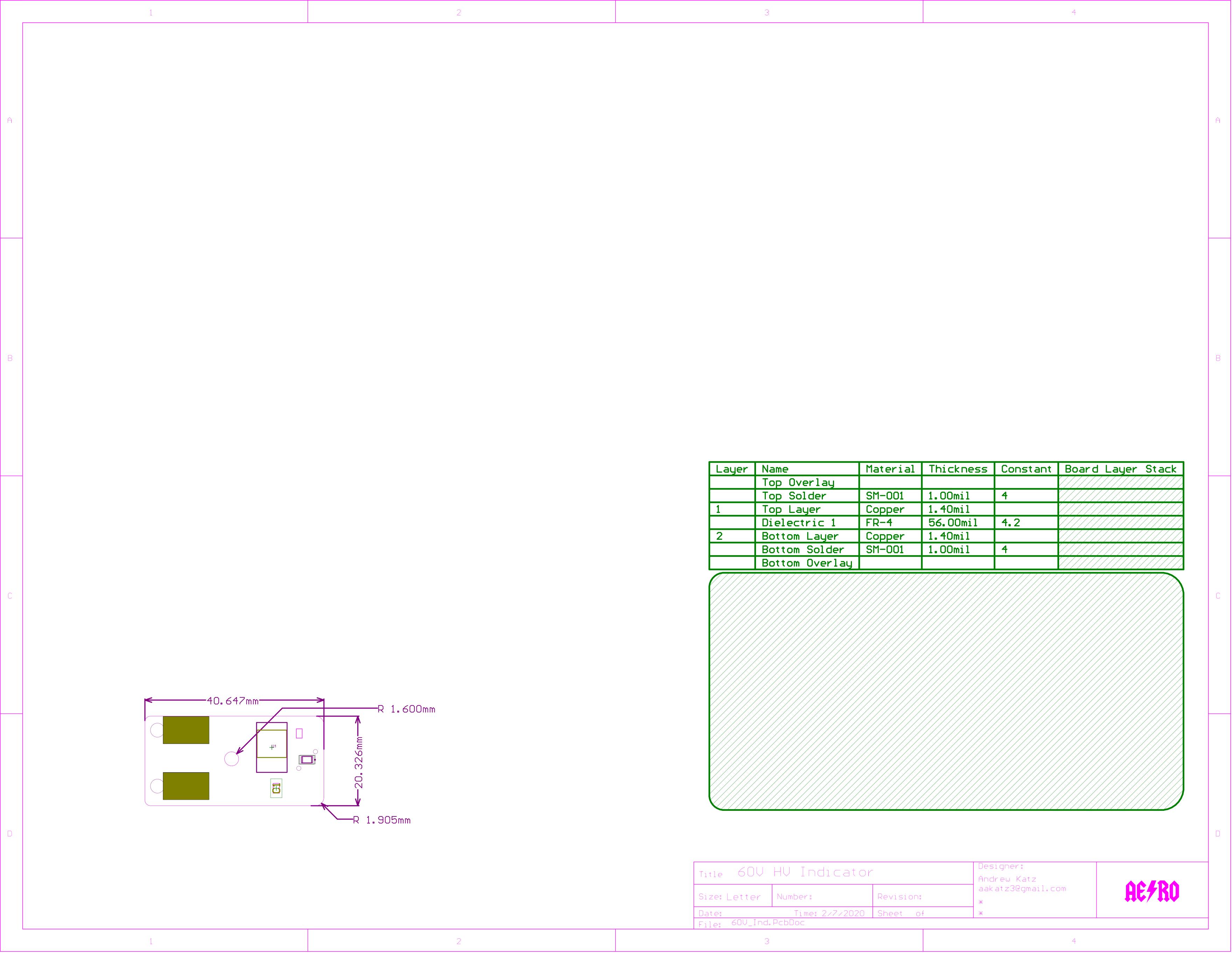


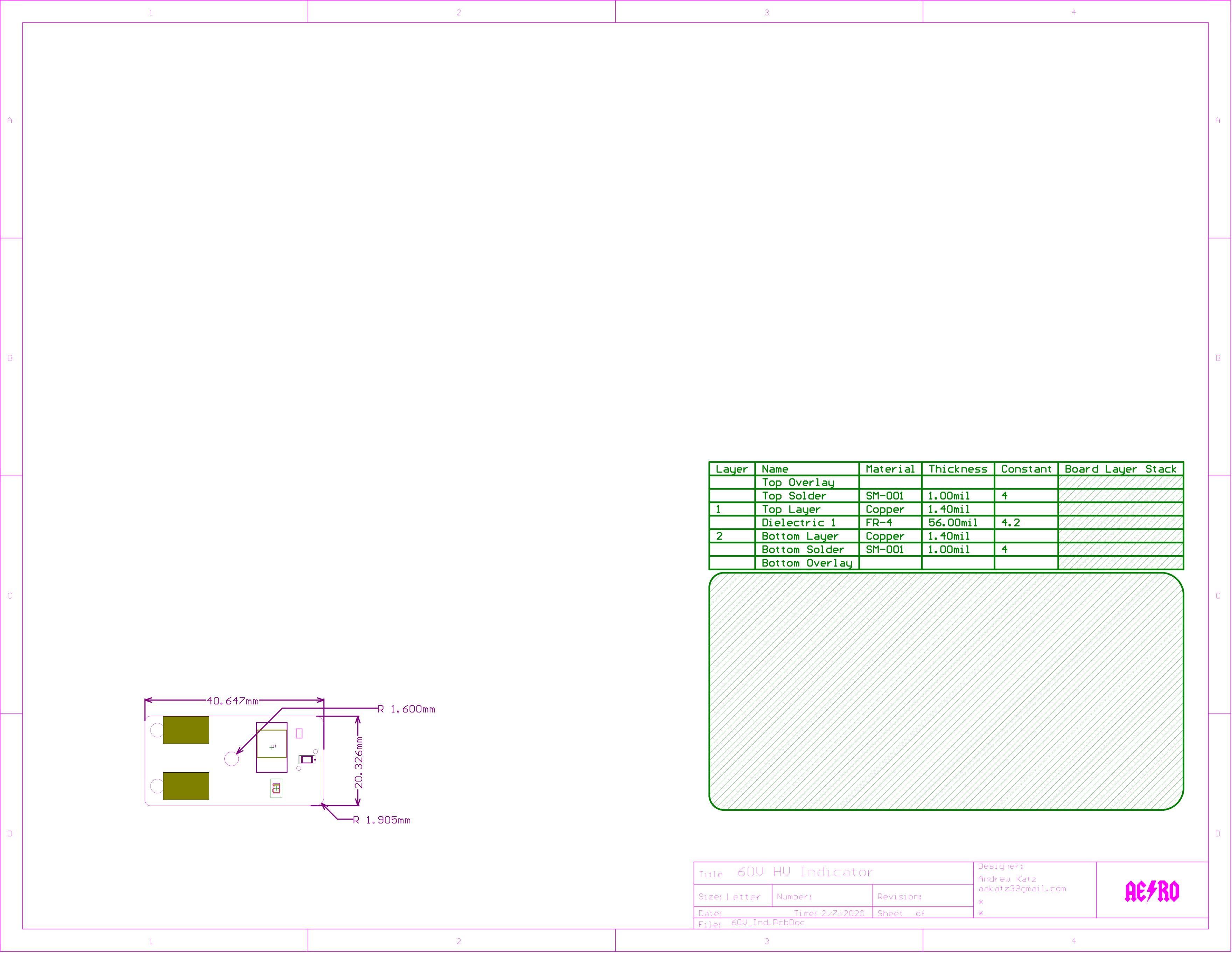


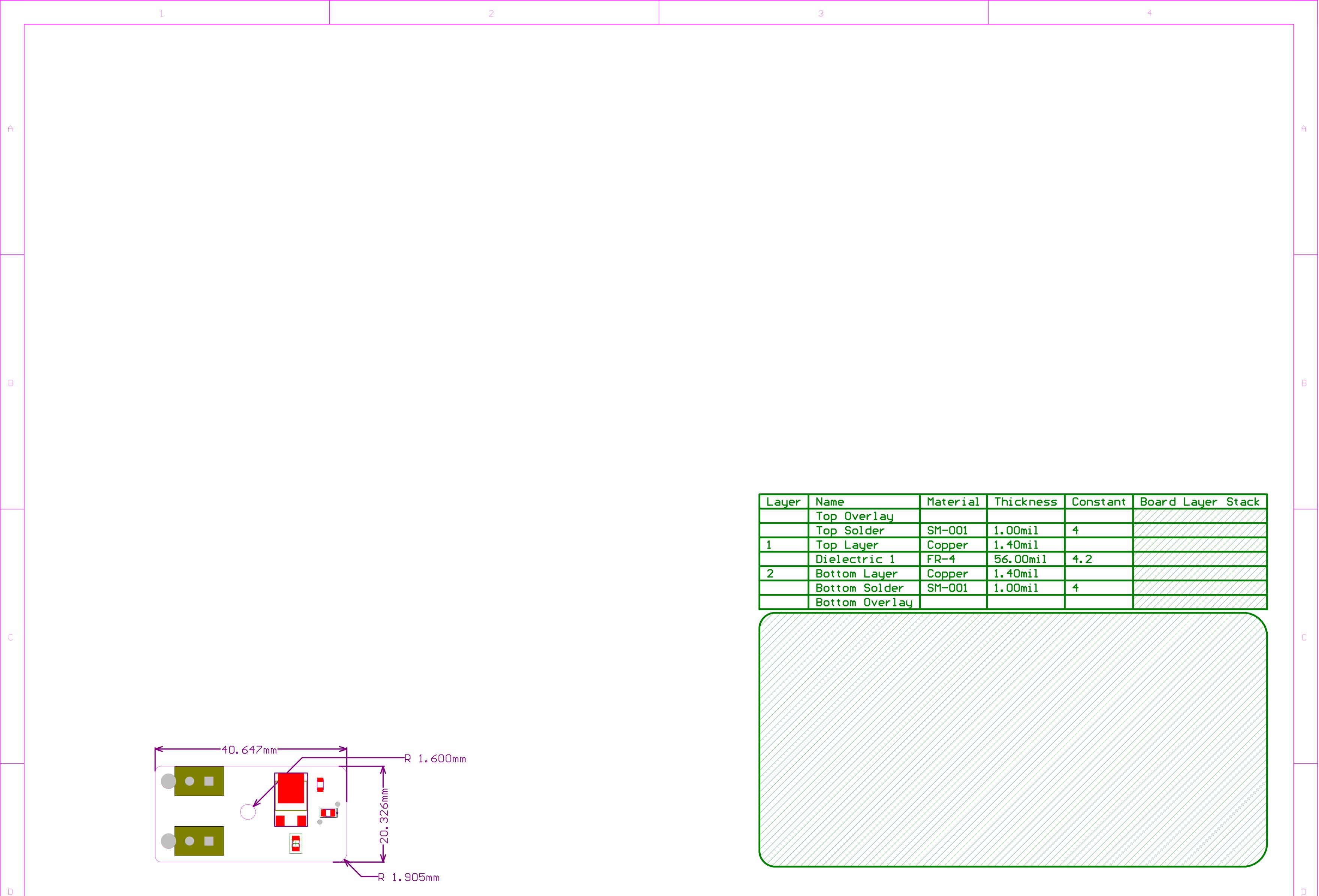












Title 60V HV Indicator

Size: Letter Number: Revision:

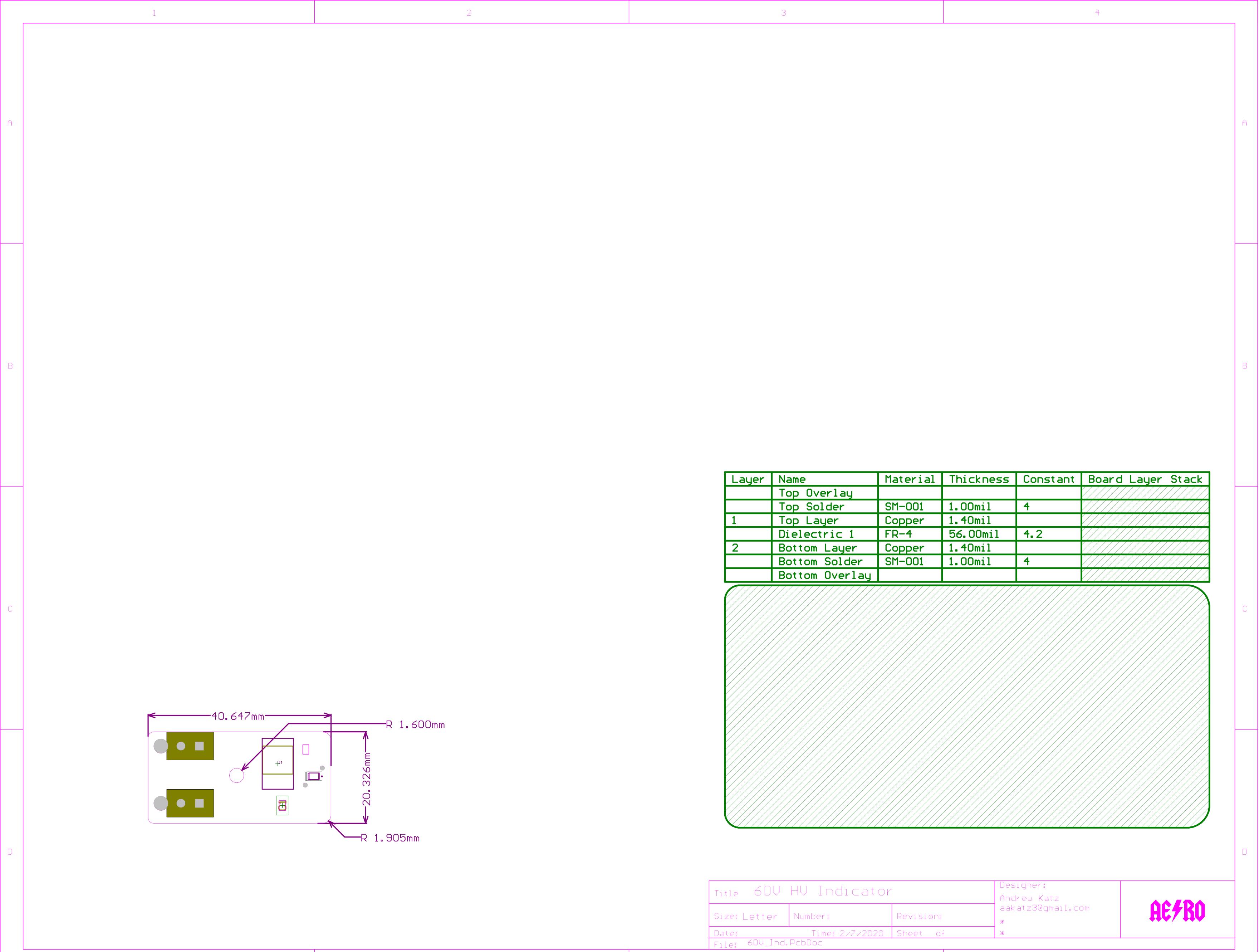
Designer:
Andrew Katz
aakatz3@gmail.com

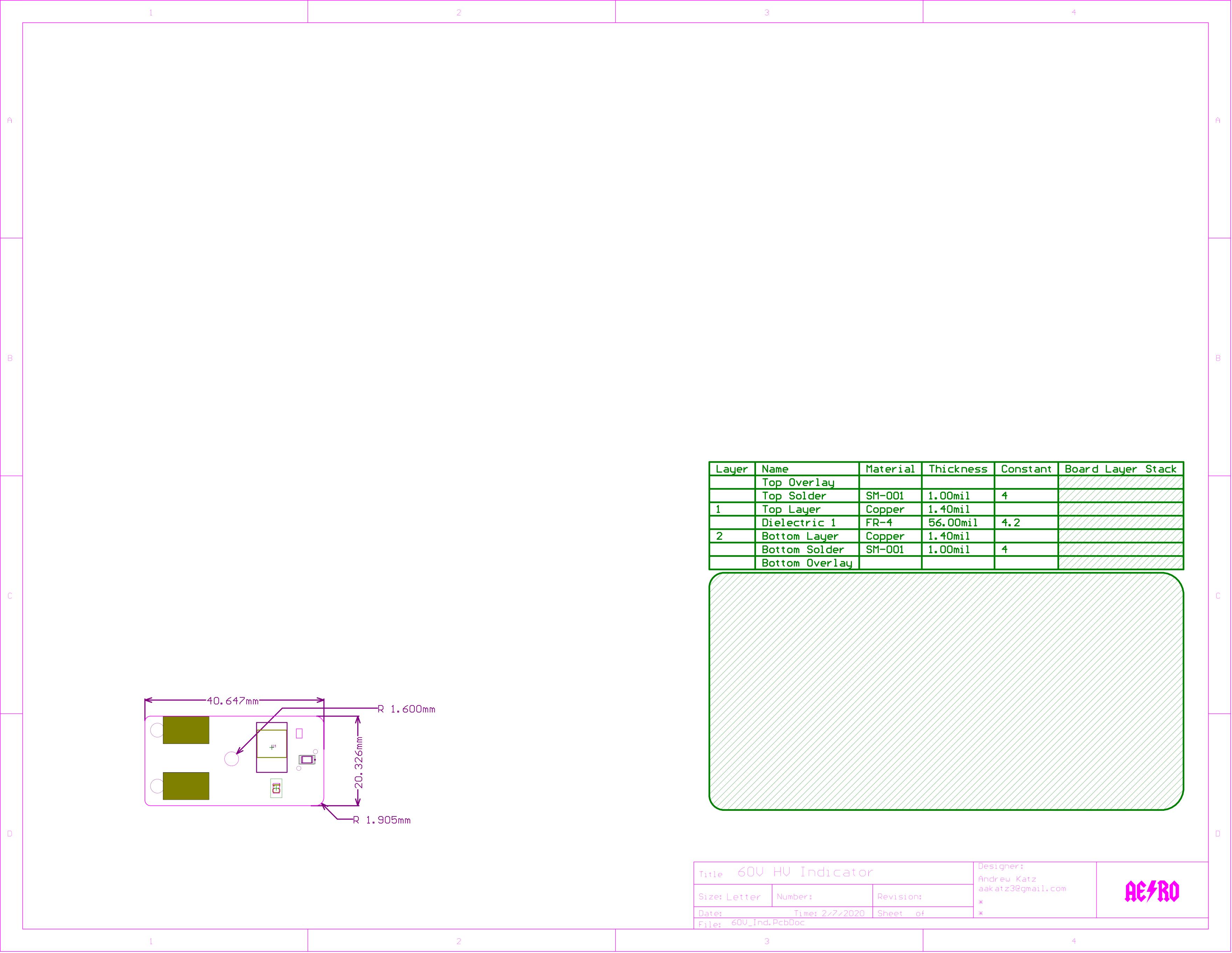
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Date: Time: 2/7/2020 Sheet of *

File: 60V_Ind.PcbDoc

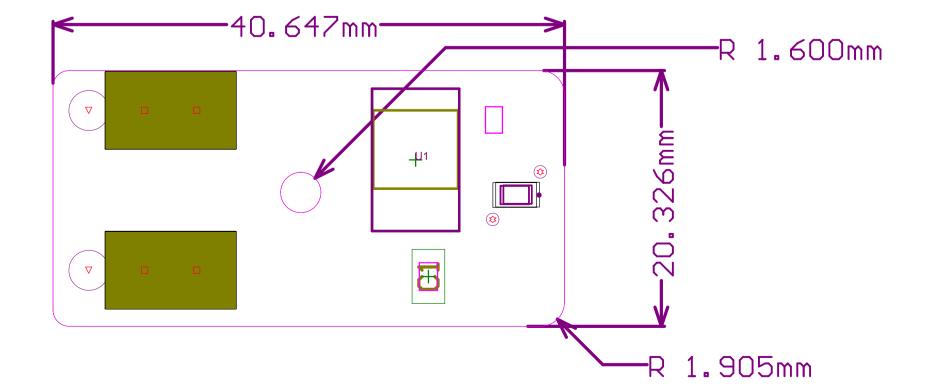
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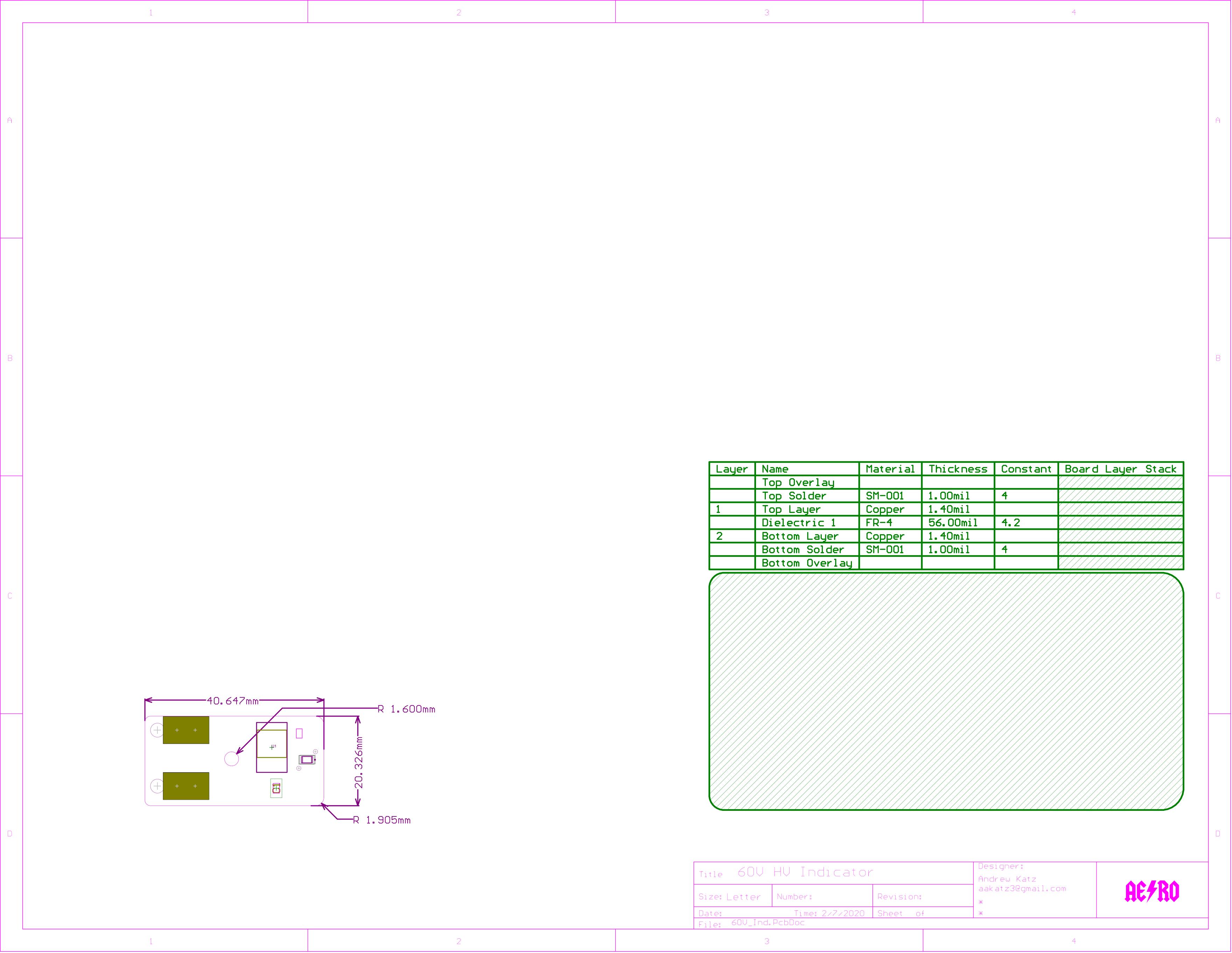


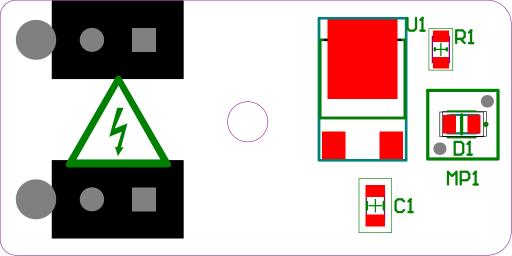
Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
\$	2	39.37mil (1.000mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c100hn100m0p354
∇	2	125.00mil (3.175mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c318hn318
	4	55.00mil (1.397mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	8 Total							

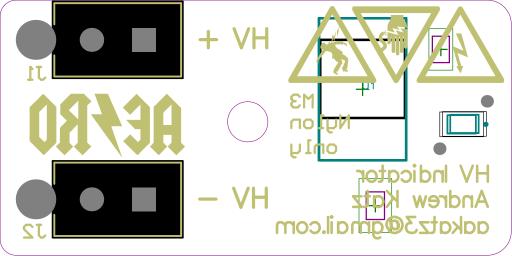
Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	SM-001	1.00mil	4	
1	Top Layer	Copper	1.40mil		
	Dielectric 1	FR-4	56.00mil	4.2	
2	Bottom Layer	Copper	1.40mil		
	Bottom Solder	SM-001	1.00mil	4	
	Bottom Overlay				



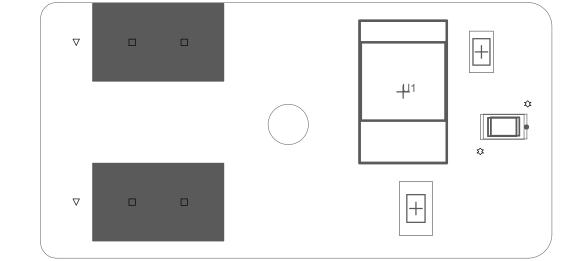
Title 60V	Designer: Andrew Katz		
Size: Letter	Number:	Revision:	aakatz3@gmail.com *
Date:	Time: 2/7/2020	Sheet of	*
File: 60V_Ind.	PcbDoc		

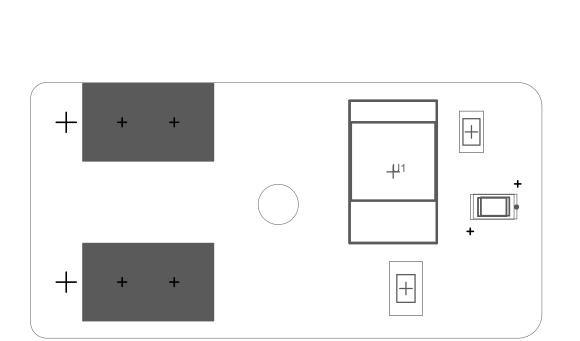






Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template
❖	2	39.37mil (1.000mm)	NPTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c100hn100m0p354
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	4	55.00mil (1.397mm)	PTH	Round	Top Layer - Bottom Layer	Pad	(Mixed)	(Mixed)
	8 Total							





Board Stack Report

	Stack Up	Layer Stack					
Layer	Board Layer Stack	Name	Material	Thickness	Constant		
1		Top Paste					
2		Top Overlay					
3		Top Solder	SM-001	1.00mil	4		
4		Top Layer	Copper	1.40mil			
5		Dielectric 1	FR-4	56.00mil	4.2		
6		Bottom Layer	Copper	1.40mil			
7		Bottom Solder	SM-001	1.00mil	4		
8		Bottom Overlay					
9		Bottom Paste					
	Height : 60.80mil						

Name	Description	Designator	Footprint	Quantity	Manufacturer Part Number 1
1-172165-2	2 Position Rectangular Housing Connector Plug Red 0.163" (4.14mm)	P1		1	1-172165-2
1-172165-9	2 Position Rectangular Housing Connector Plug Black 0.163" (4.14mm)	P2		1	1-172165-9
1-770872-0	Connector Header Through Hole 2 position 0.163" (4.14mm)	J1, J2	CON2_1X2_P163_VM	2	1-770872-0
C2012X7S2A105K125A B	Chip Capacitor, 1 uF, +/- 10%, 100 V, -55 to 125 degC, 0805 (2012 Metric), RoHS, Tape and Reel	C1	CAPC2013X145X20ML 20	1	C2012X7S2A105K1 25AB
770904-1	Socket Contact Crimp 18-22 AWG Stamped	PIN1, PIN2, PIN3, PIN4		4	770904-1
KTR10EZPF40R2	40.2 Ohms ±1% 0.125W, 1/8W Chip Resistor 0805 (2012 Metric) Automotive AEC-Q200, High Voltage Thick Film	R1	RESC2012X06N_HV	1	KTR10EZPF40R2
LPA-C011301S-10	Light Pipe Single Clear Rigid Round with Flat Top, 3mm Board Mount, Press Fit	MP1	LPA-C011301S-10	1	LPA-C011301S-10
LR8K4-G	Linear Voltage Regulator IC Positive Adjustable 1 Output 10mA TO-252, (D- Pak)	U1	Microchip_C04- 189_MFG	1	LR8K4-G
SM0805HCL	Red 631nm LED Indication - Discrete 1.9V 0805 (2012 Metric)	D1	LEDC2012X135N_SM0 805UGC(Primary)	1	SM0805HCL

Design Rules Verification ReportFilename: C:\git\AERO_2019-2020\60V_IND\AItium\60V_Ind.PcbDoc

Warnings 0 Rule Violations 0

Warnings	
Total	0
Rule Violations	
Clearance Constraint (Gap=20mil) (All),(All)	0
Clearance Constraint (Gap=118.11mil) (InNetClass(TS')),(InNetClass(TS'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((AII))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Creepage Distance Constraint =(40mil) (InNetClass(TS')), (InNetClass(TS'))	0
Width Constraint (Min=10mil) (Max=60mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=500mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=5mil) (IsPad),(All)	0
Silk to Silk (Clearance=5mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0

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Electrical Rules Check Report

Class	Document	Message
		Successful Compile for

Friday 7 Feb 2020 2:13:23 PN