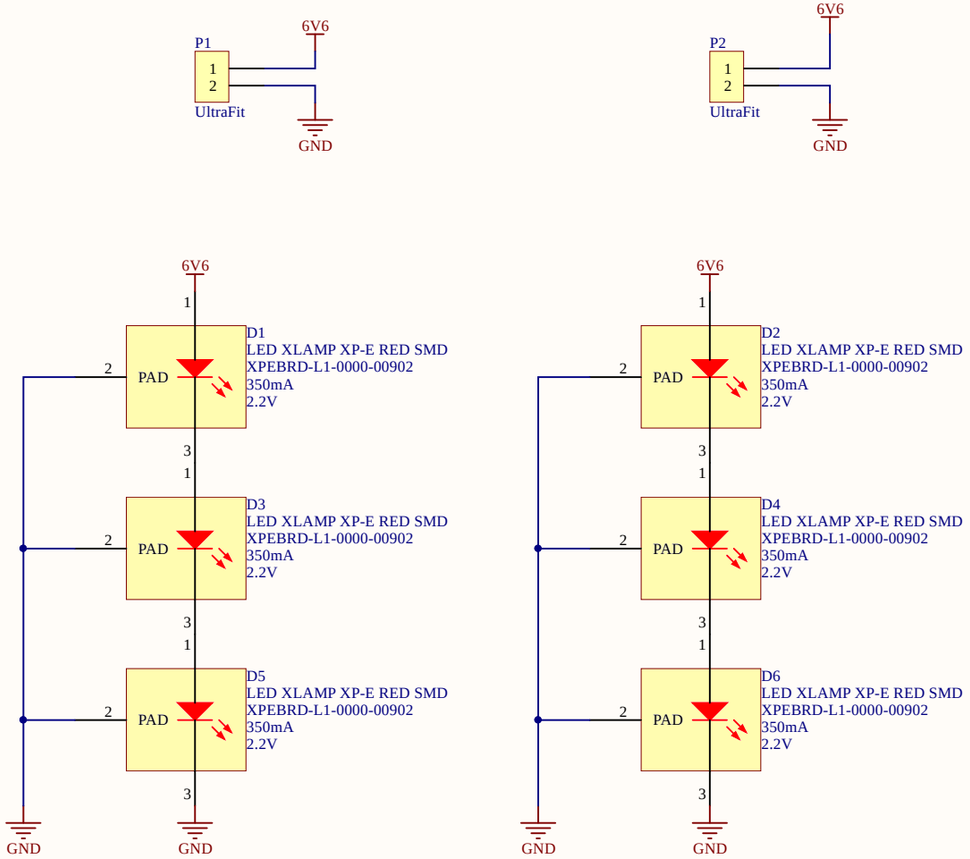
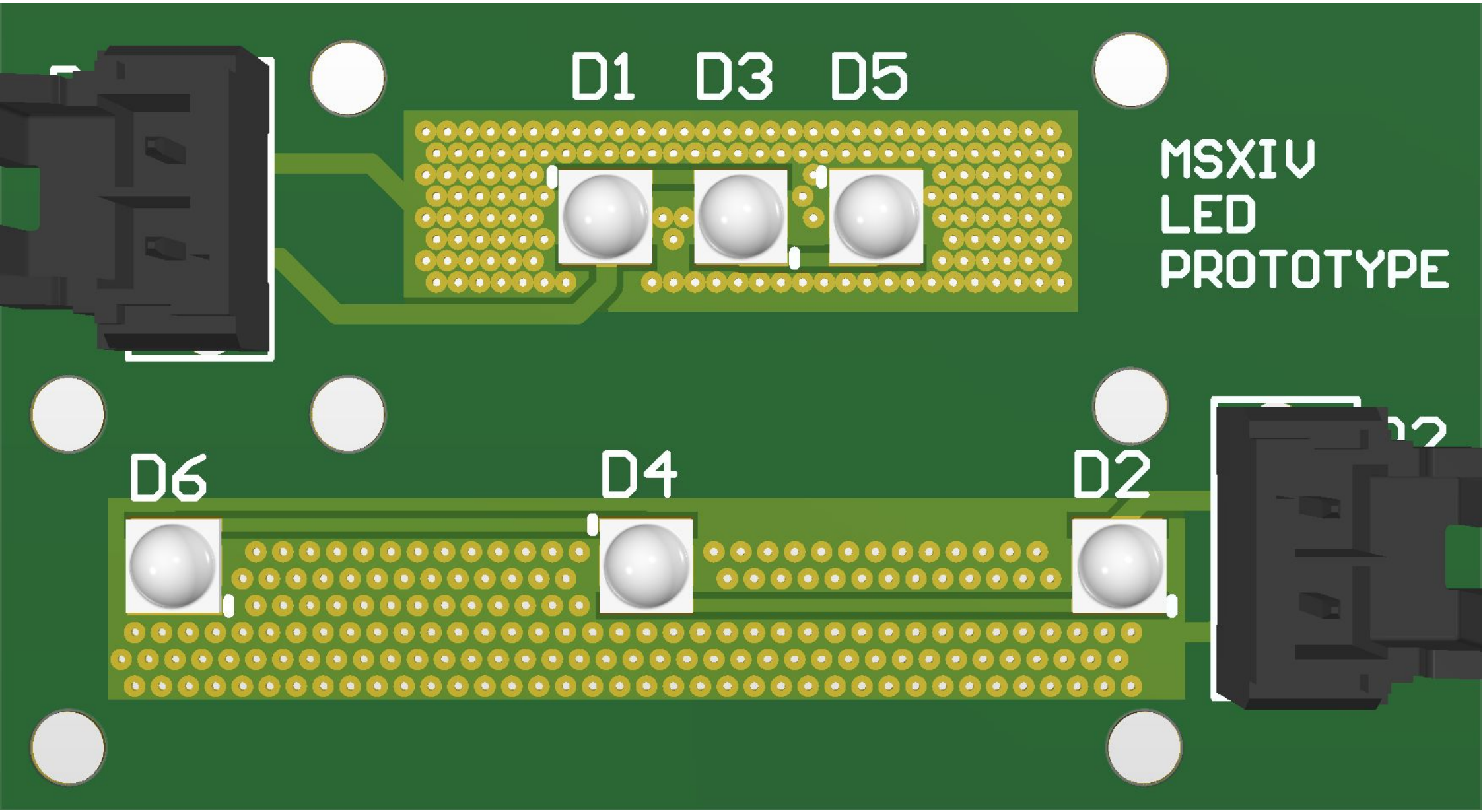


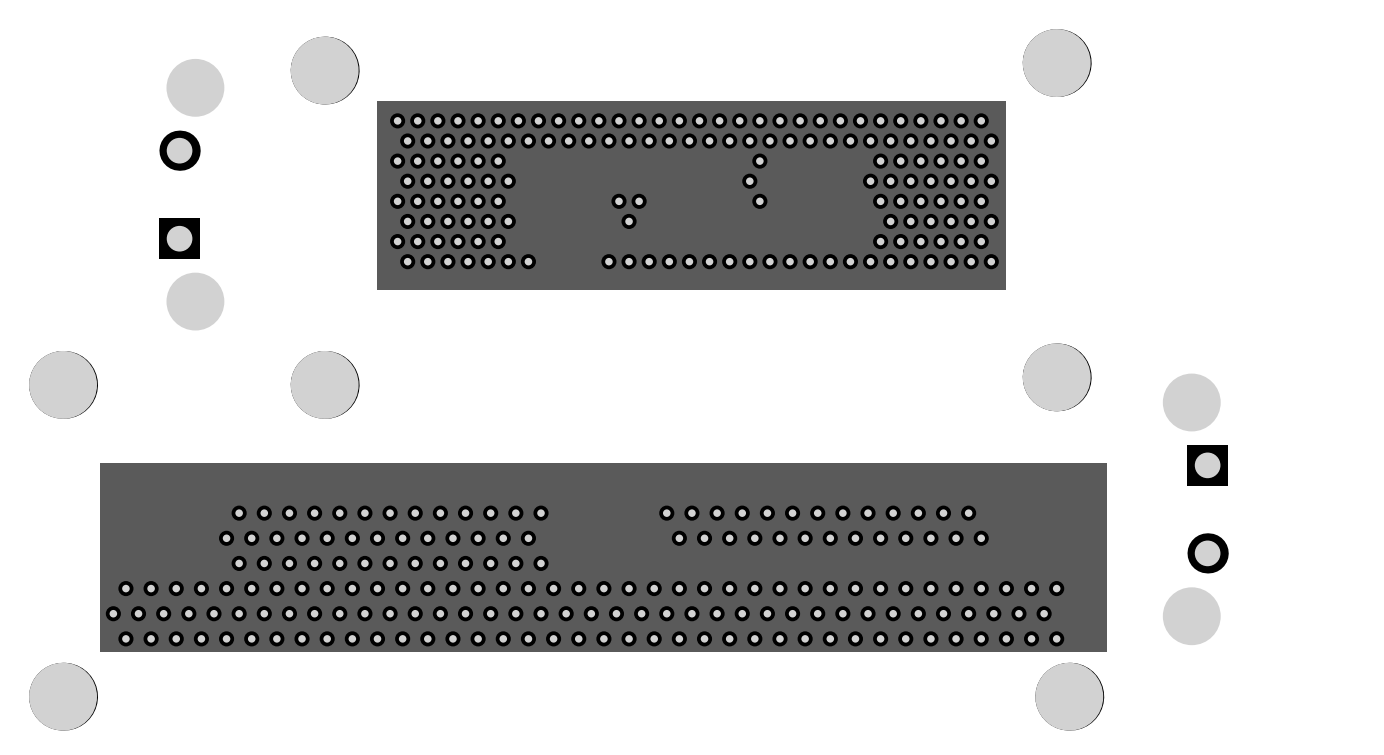
PROJECT	TailLightsPrototype.PrjPCB		MIDNIGHT SUN
DOCUMENT	LED prototype		
PART NUMBER		VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
DRAWN BY	Nita E, Jenny Xia	REVISION 1.0	
LAST MODIFIED	2019/3/16	SHEET 1 OF 1	

Bill of Materials

Project:	TailLightsPrototype.PrjPCB
Revision:	1
Project Lead:	Nita E, Jenny Xia
Generated On:	2019/3/16 下午 3:09
Production Quantity:	1
Currency	CAD
Total Parts Count:	8

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
LED XLAMP XP-E RED SMD	D1, D2, D3, D4, D5, D6	Cree	XPEBRD-L1-0000-00902	Digi-Key	EBRD-L1-0000-00902CT-	2.67	6	$ 16.00
CONN 2POS ULTRA-FIT 0.138"	P1, P2	Molex	1722861302	Digi-Key	WM11673-ND	1.95	2	$ 3.89
							Total:	$ 19.89


D1
D3
D5
MSXIV
LED
PROTOTYPE
D6
D4
D2



Electrical Rules Check Report

Class	Document	Message
		Successful Compile for TailLightsPrototype.PrjPCB

Design Rules Verification Report

Filename : C:\Users\jieni\Documents\Github\hardware\MSXIV_TailLightsPrototype\TailLightF

Warnings 0

Rule Violations 63

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	2
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=10mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	48
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	6
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	63

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net 6V6 Between Pad D1-1(22.5mm,20.5mm) on Top Layer And Pad D2-1(41.5mm,10.6mm) on Top Layer
Un-Routed Net Constraint: Net GND Between Via (35.4mm,19.6mm) from Top Layer to Bottom Layer And Via (35.5mm,9.6mm) from Top Layer to Bottom

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(12.9mm,14.7mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,14.7mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(42mm,15mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-1(2.5mm,2.3mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-2(42.5mm,2.3mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-3(42mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-4(12.9mm,27.2mm) on Multi-Layer Actual Hole Size = 2.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad D1-1(22.5mm,20.5mm) on Top Layer And Via (20.2mm,21.2mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-1(22.5mm,20.5mm) on Top Layer And Via (21mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-1(22.5mm,20.5mm) on Top Layer And Via (24.2mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.149mm < 0.254mm) Between Pad D1-2(22.5mm,22mm) on Top Layer And Via (20.2mm,21.2mm) from Top
Minimum Solder Mask Sliver Constraint: (0.149mm < 0.254mm) Between Pad D1-2(22.5mm,22mm) on Top Layer And Via (20.2mm,22.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (20.2mm,22.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (21.8mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (21mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (22.6mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (23.4mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Via (24.2mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D2-3(41.5mm,7.6mm) on Top Layer And Via (40mm,6.6mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D2-3(41.5mm,7.6mm) on Top Layer And Via (41mm,6.6mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D2-3(41.5mm,7.6mm) on Top Layer And Via (42mm,6.6mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (25.8mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (26.6mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (27.4mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (28.2mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (29.8mm,22.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-1(27.5mm,23.5mm) on Top Layer And Via (29mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.149mm < 0.254mm) Between Pad D3-2(27.5mm,22mm) on Top Layer And Via (29.8mm,22.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Via (25.8mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Via (26.6mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Via (27.4mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Via (28.2mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Via (29mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D4-1(24mm,7.6mm) on Top Layer And Via (23mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D4-1(24mm,7.6mm) on Top Layer And Via (24mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D4-1(24mm,7.6mm) on Top Layer And Via (25mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.166mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (30.6mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (31.4mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (32.2mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (33.8mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (33mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad D5-1(32.5mm,20.5mm) on Top Layer And Via (34.6mm,19.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-2(32.5mm,22mm) on Top Layer And Via (30.2mm,22mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (30.2mm,23.6mm) from Top
Minimum Solder Mask Sliver Constraint: (0.167mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (30.6mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (31.4mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (32.2mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (33.8mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (33mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.091mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (34.6mm,22.8mm) from Top
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Via (34.6mm,24.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D6-3(6.5mm,7.6mm) on Top Layer And Via (5mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D6-3(6.5mm,7.6mm) on Top Layer And Via (6mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D6-3(6.5mm,7.6mm) on Top Layer And Via (7mm,6.6mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad D6-3(6.5mm,7.6mm) on Top Layer And Via (8mm,6.6mm) from Top Layer to

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D1-3(22.5mm,23.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D2-3(41.5mm,7.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D3-3(27.5mm,20.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D4-3(24mm,10.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D5-3(32.5mm,23.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad D6-3(6.5mm,7.6mm) on Top Layer And Track