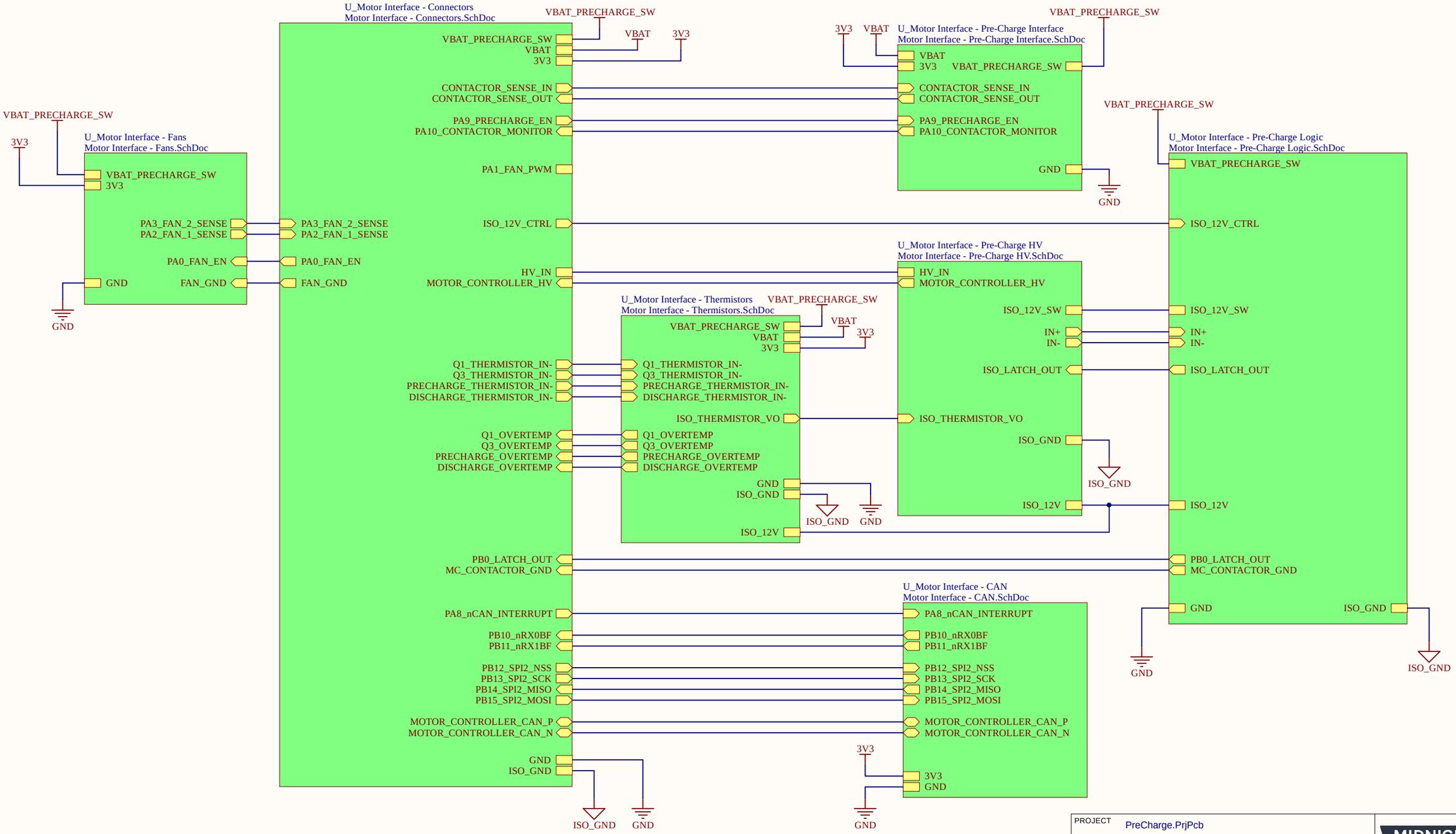

PROJECT	PreCharge.PrjPcb
DOCUMENT	Title
PART NUMBER	MS14005
VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin
REVISION	5.0
LAST MODIFIED	2019-12-01
SHEET	1 OF 6

MIDNIGHT SUN

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(519) 888-4567 x32978
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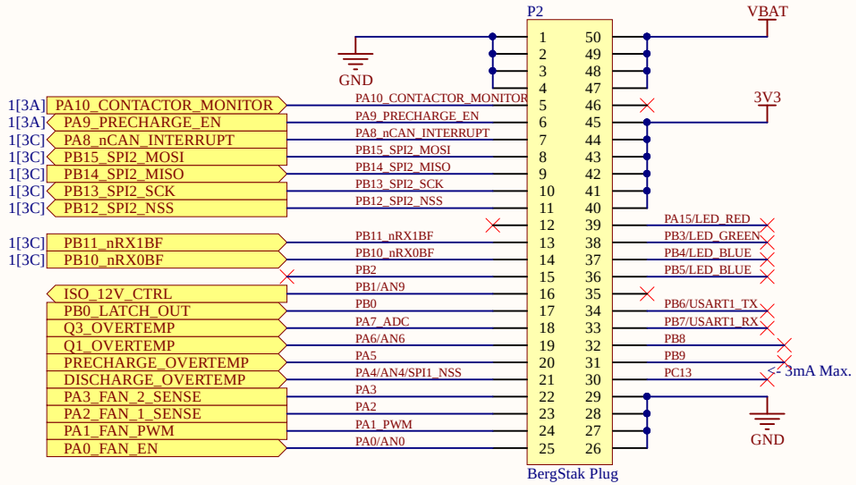
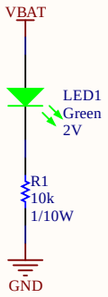
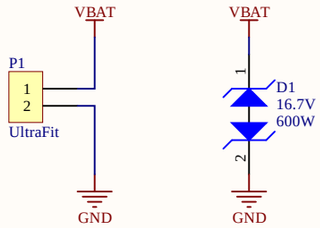
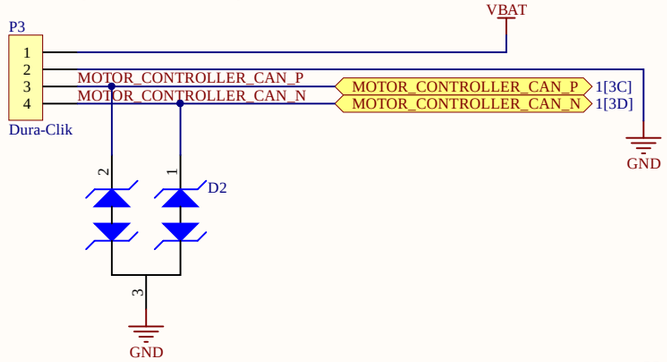
Connectors

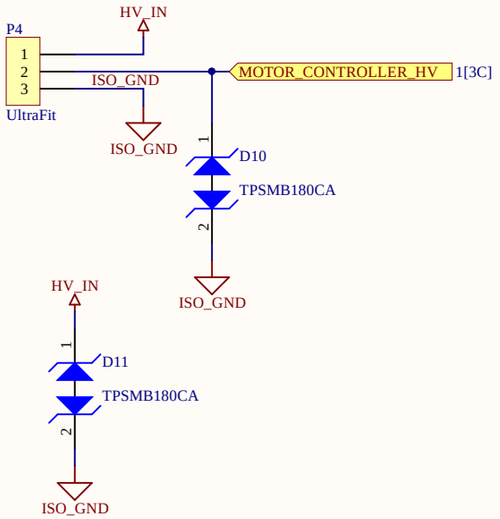


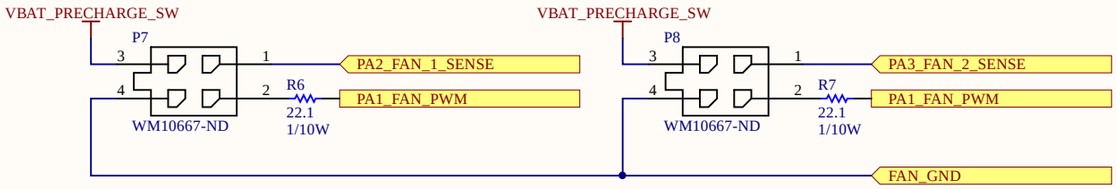


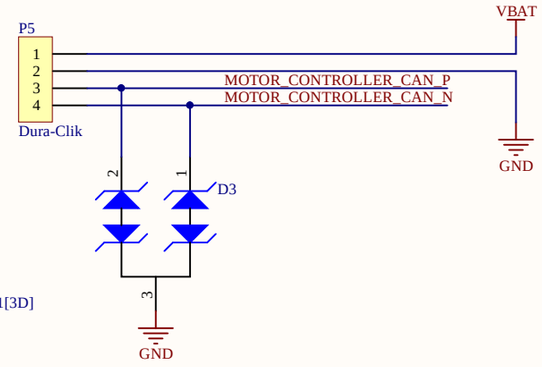


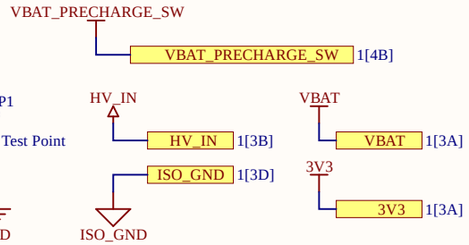


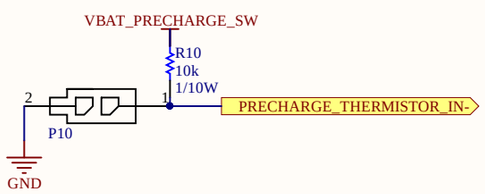
HV Connector

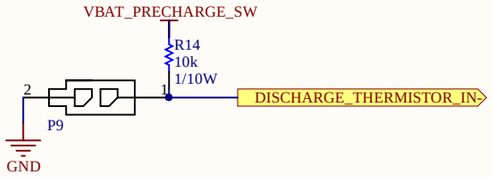


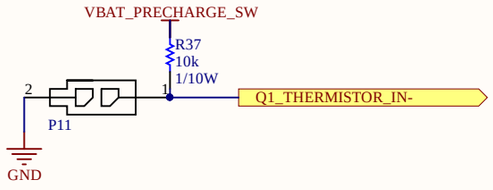


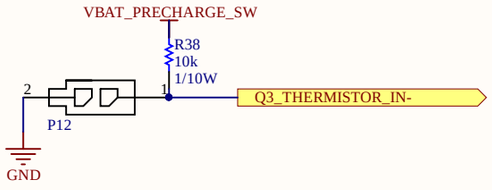


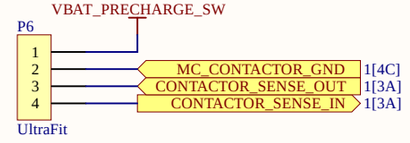












PROJECT	PreCharge.PrjPcb		MIDNIGHT SUN
DOCUMENT	Motor Interface - Connectors		
PART NUMBER	MS14005	VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin	REVISION	5.0
LAST MODIFIED	2019-12-01	SHEET	2 OF 6

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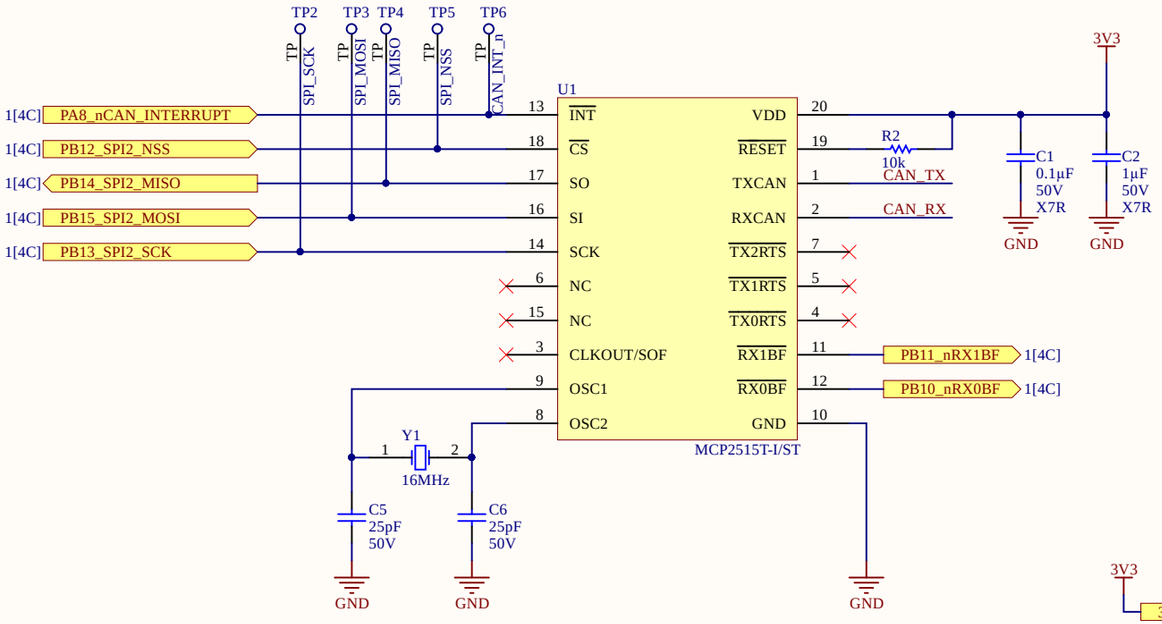
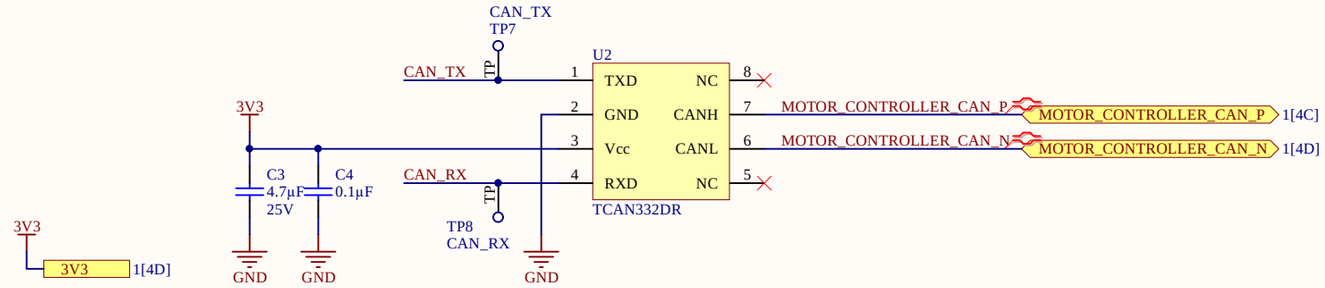
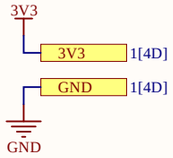
CAN Controller



CAN Transceiver





PROJECT	PreCharge.PrjPcb	MIDNIGHT SUN	
DOCUMENT	Motor Interface - CAN		
PART NUMBER	MS14005	VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin	REVISION	5.0
LAST MODIFIED	2019-12-01	SHEET	3 OF 6

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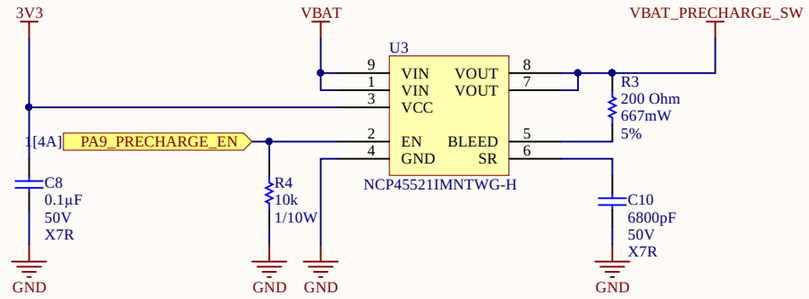
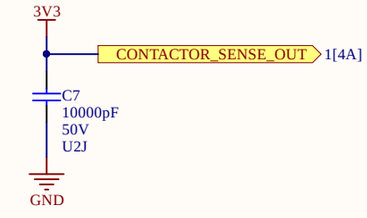
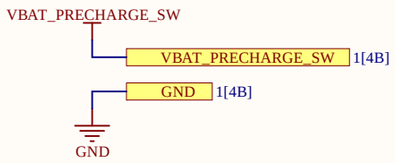
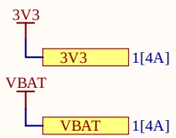
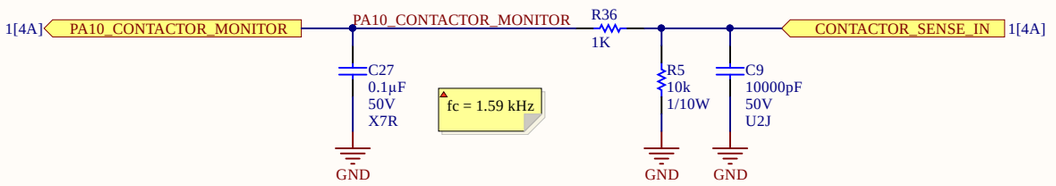
Precharge Control



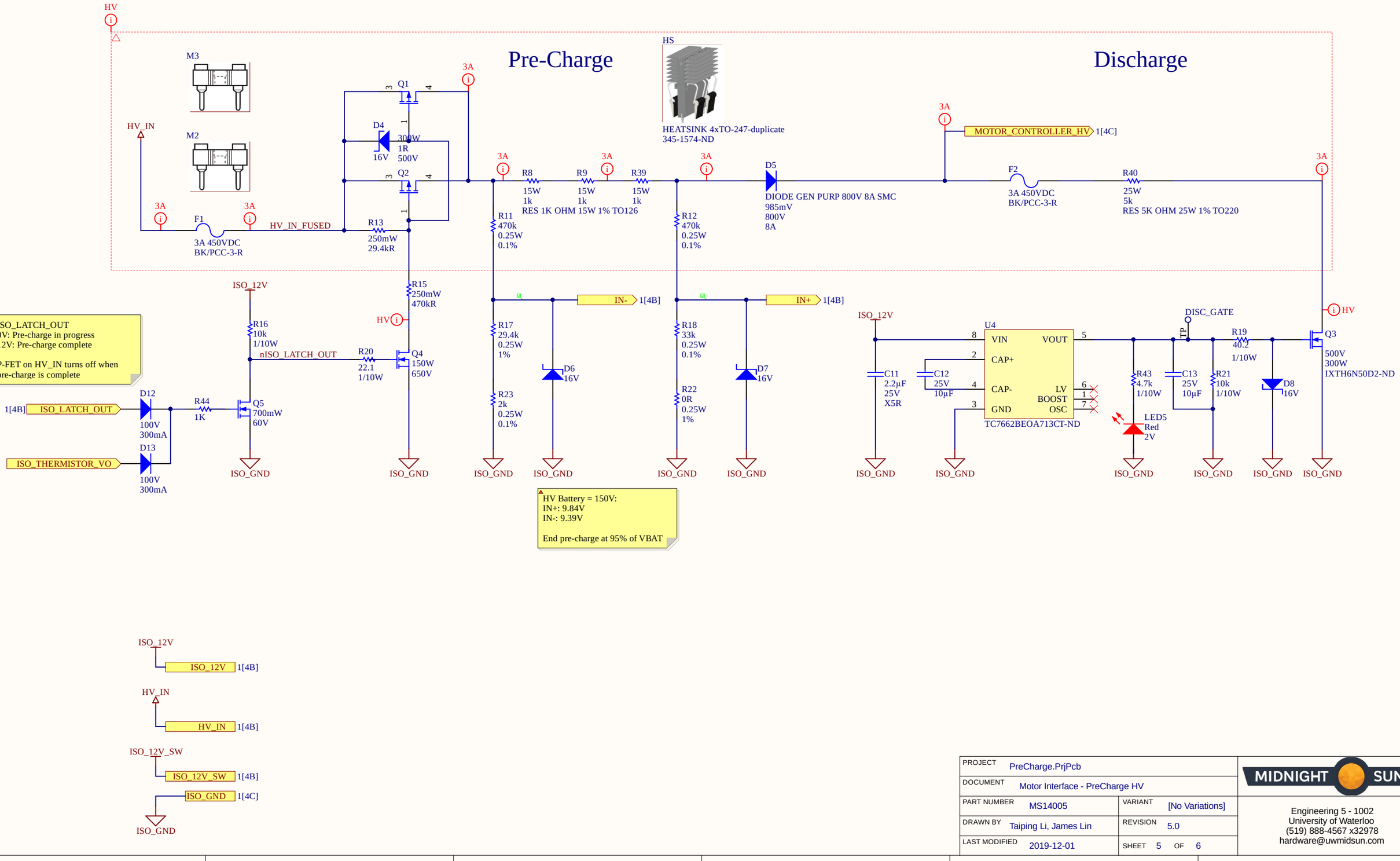








PROJECT	PreCharge.PrjPcb		MIDNIGHT SUN
DOCUMENT	Motor Interface - PreCharge Interface		
PART NUMBER	MS14005	VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
DRAWN BY	Taiping Li, James Lin	REVISION 5.0	
LAST MODIFIED	2019-12-01	SHEET 4 OF 6	



PROJECT	PreCharge.PrjPcb
DOCUMENT	Motor Interface - PreCharge HV
PART NUMBER	MS14005
VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin
REVISION	5.0
LAST MODIFIED	2019-12-01
SHEET	5 OF 6

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Logic

Motor Controller Contactor Driver

Isolated DC/DC

ISO_12V_SW
ISO_12V_SW
5
U7B
V+
V-
2
C26
0.1µF
50V
X7R
ISO_GND
ISO_GND
Placeholder resistor for hysteresis if needed
R26
1M
1/10W
IN+
TP
1[4B]
IN+
IN+
C19
680pF
50V
1
U7A
4
COMP_OUT
TP
1[4B]
IN-
IN-
TP
IN-
3
TLV1701QDBVRQ1
ISO_12V_SW
C18
50V
0.1µF
X7R
ISO_GND
AND_OUT
TP
U8
5
VDD
VSS
1
2
3
4
R29
10k
ISO_GND
ISO_GND
ISO_12V
C17
0.1µF
50V
X7R
ISO_GND
ISO_12V
296-31496-1-ND
16
U6
S-R Latch
S1
R1
S2
R2
S3
R3
S4
R4
ENA
Vdd
Vss
Q1
Q2
Q3
Q4
NC
4
3
6
7
12
11
14
15
5
2
9
10
1
13
8
ISO_GND
ISO_12V
ISO_GND
ISO_LATCH_OUT
R30
10k
ISO_GND
ISO_12V
C20
1µF
50V
R31
10k
±1%
ISO_GND
Hold reset low (<8.4V) for 12ms
ISO_LATCH_OUT
TP
ISO_LATCH_OUT
1[4B]
ISO_12V
U5
2
AN
CAT
NC
NC
VCC
VO
GND
NC
3
1
4
8
7
5
6
HCPL-0211-000E
R28
1K
±5%
Q7
700mW
60V
ISO_GND
VBAT_PRECHARGE_SW
C16
50V
0.1µF
X7R
GND
LATCH_OUT
GND
GND
R25
22.1
1/10W
R27
10k
1/10W
3
4
8
1
2
5
6
7
Q6
8.7A
2.1W
VBAT_PRECHARGE_SW
R24
10k
1/10W
LED2
Blue
2.8V
D9
60V
3A
C14
100UF
C15
0.1µF
50V
X7R
GND
GND
MC_CONTACTOR_GND
PB0_LATCH_OUT
TP
LATCH_OUT
ISO_12V_SW
ISO_12V_SW
R32
10k
1/10W
3
4
Q8
6
5
2
1
IN+
Q9
700mW
60V
R33
10k
1/10W
ISO_GND
ISO_GND
ISO_12V
R34
10k
1/10W
LED3
Blue
2.8V
ISO_GND
ISO_12V_SW
R35
10k
1/10W
LED4
Yellow
2V
ISO_GND
Input: 10.80 V to 13.20 V
VBAT_PRECHARGE_SW
L1
6.8µH
U9
+Vin
-Vin
+Vout
N.C
GND
2
1
5
8
4
Isolated DCDC
ISO_12V
ISO_1
ISO_12V_SW
TP
ISO_2
Test Point
C21
0.1µF
50V
X7R
C22
X5R
50V
4.7uF
C23
0.1µF
50V
X7R
C24
100V
2.2µF
X7R
Q10
3
2
4
1
C25
25V
10µF
3A
-60V
ISO_LATCH_OUT
R42
10k
1/10W
ISO_ON
TP
GND
GND
ISO_GND
ISO_GND
3
1
Q13
2
ISO_12V_CTRL
1
Q14
2
R60
1K
GND
GND
ISO_12V
ISO_12V
1[4B]
VBAT_PRECHARGE_SW
VBAT_PRECHARGE_SW
1[4B]
GND
1[4C]
ISO_12V_SW
ISO_12V_SW
1[4B]
ISO_GND
1[4C]
GND
ISO_GND

PROJECT	PreCharge.PrjPcb		
DOCUMENT	Motor Interface - PreCharge Logic		
PART NUMBER	MS14005	VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin	REVISION	5.0
LAST MODIFIED	2019-12-01	SHEET	6 OF 6

MIDNIGHT SUN

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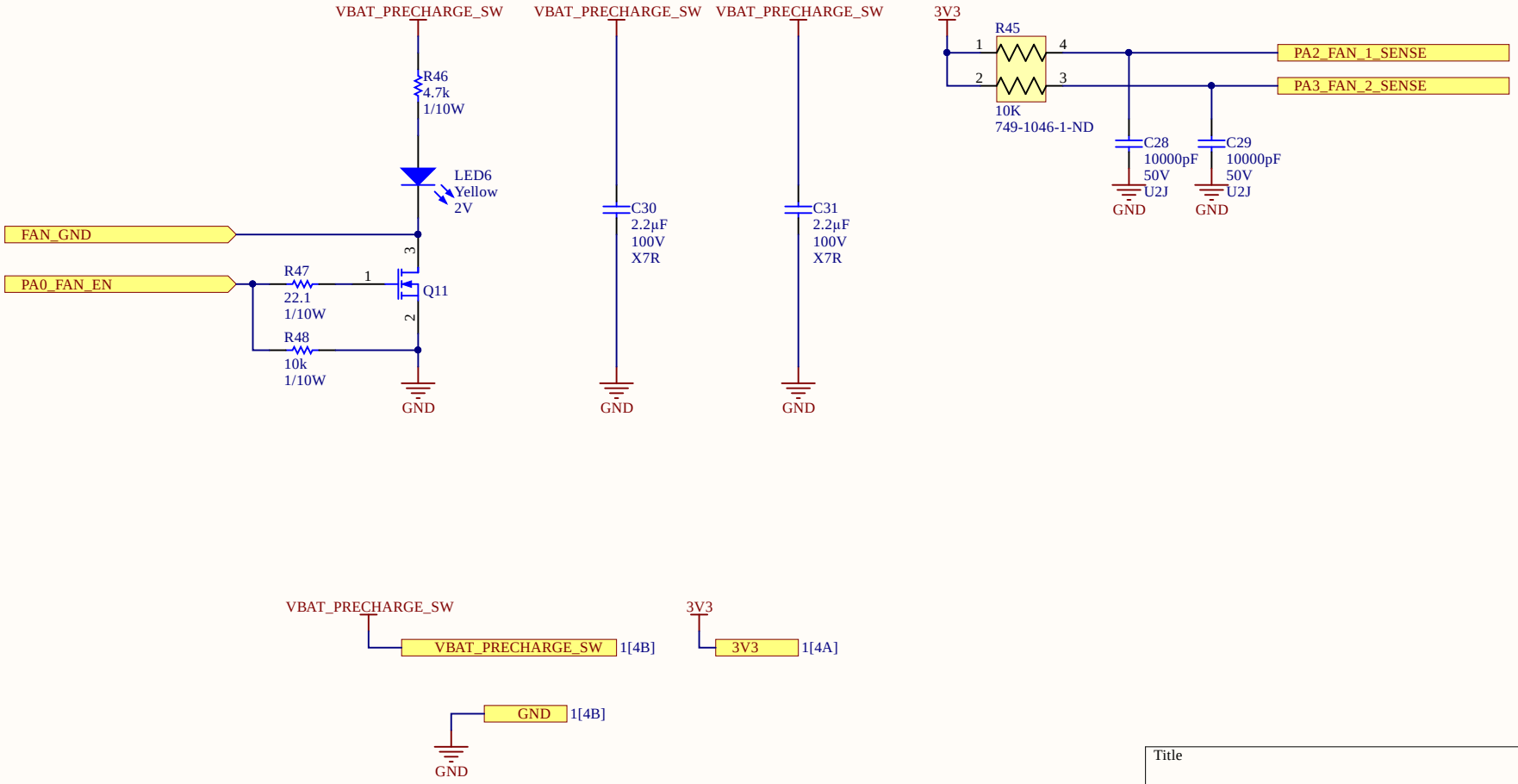

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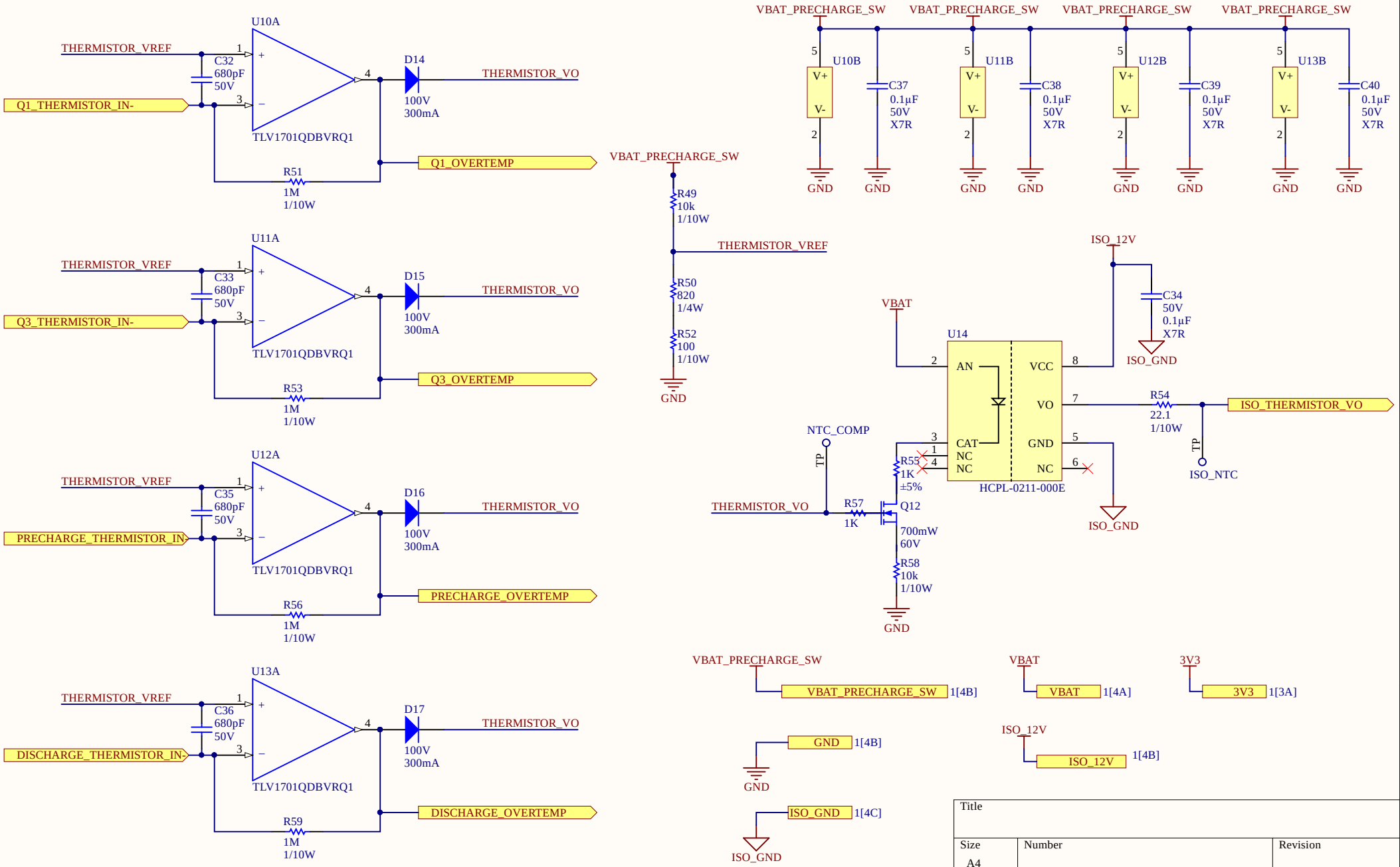
U10A
THERMISTOR_VREF
C32
680pF
50V
Q1_THERMISTOR_IN-
TLV1701QDBVRQ1
D14
100V
300mA
THERMISTOR_VO
Q1_OVERTEMP
R51
1M
1/10W
U11A
THERMISTOR_VREF
C33
680pF
50V
Q3_THERMISTOR_IN-
TLV1701QDBVRQ1
D15
100V
300mA
THERMISTOR_VO
Q3_OVERTEMP
R53
1M
1/10W
U12A
THERMISTOR_VREF
C35
680pF
50V
PRECHARGE_THERMISTOR_IN-
TLV1701QDBVRQ1
D16
100V
300mA
THERMISTOR_VO
PRECHARGE_OVERTEMP
R56
1M
1/10W
U13A
THERMISTOR_VREF
C36
680pF
50V
DISCHARGE_THERMISTOR_IN-
TLV1701QDBVRQ1
D17
100V
300mA
THERMISTOR_VO
DISCHARGE_OVERTEMP
R59
1M
1/10W
VBAT_PRECHARGE_SW
R49
10k
1/10W
THERMISTOR_VREF
R50
820
1/4W
R52
100
1/10W
GND
VBAT_PRECHARGE_SW
VBAT_PRECHARGE_SW
VBAT_PRECHARGE_SW
VBAT_PRECHARGE_SW
U10B
U11B
U12B
U13B
V+
V-
C37
0.1µF
50V
X7R
C38
0.1µF
50V
X7R
C39
0.1µF
50V
X7R
C40
0.1µF
50V
X7R
GND
ISO_12V
C34
50V
0.1µF
X7R
ISO_GND
VBAT
U14
AN
CAT
NC
NC
VCC
VO
GND
NC
HCPL-0211-000E
R54
22.1
1/10W
ISO_THERMISTOR_VO
TP
ISO_NTC
NTC_COMP
TP
R55
1K
±5%
THERMISTOR_VO
R57
1K
Q12
700mW
60V
R58
10k
1/10W
GND
ISO_GND
VBAT_PRECHARGE_SW
VBAT_PRECHARGE_SW 1[4B]
VBAT
VBAT 1[4A]
3V3
3V3 1[3A]
GND
GND 1[4B]
ISO_12V
ISO_12V 1[4B]
ISO_GND
ISO_GND 1[4C]
Title
Size
A4
Number
Revision
Date:
2019-12-01
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of
File:
C:\Users\..\Motor Interface - Thermistors.SchDoc
Drawn By:

Bill of Materials

Project:	PreCharge.PrjPcb
Revision:	5.0
Project Lead:	Taiping Li, James Lin
Generated On:	2019-12-01 10:19 PM
Production Quantity:	1
Currency:	USD
Total Parts Count:	170

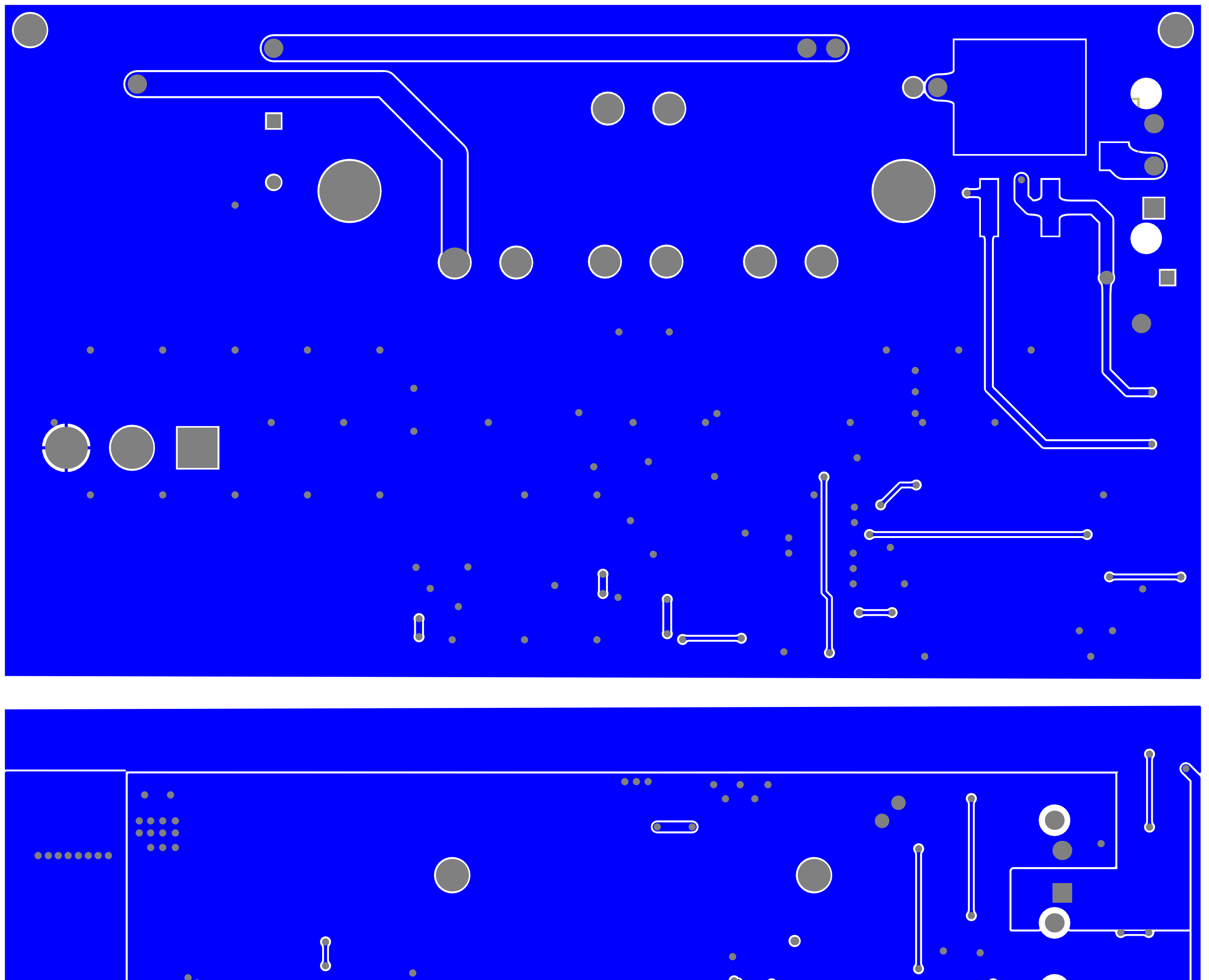
LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1
CAP CER 0.1UF 50V 10% X7R 0603	C16, C17, C18, C21, C23, C26, C27, C34, C3	AVX Corporation	06035C104KAT2A	Digi-Key	478-5052-1-ND	
CAP CER 1UF 50V 10% X7R 0603	C2, C20	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	
CAP CER 4.7UF 25V 10% X5R 0603	C3	Murata Electronics North America	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	
CAP CER 25PF 50V ±5% C0G/NP0 0603	C5, C6			Digi-Key	1276-2244-1-ND	
CAP CER 10nF 50V 5% X7R 0603	C7, C9, C28, C29	KEMET	C0603C103J5JAC7867	Digi-Key	399-13384-1-ND	
CAP CER 6800pF 50V 10% X7R 0603	C10	Samsung Electro-Mechanics	CL10B682KB8SFNC	Digi-Key	1276-2103-1-ND	
CAP CER 2.2UF 25V 10% X5R 0603	C11	Murata Electronics North America	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	
CAP CER 10uF 25V 10% X5R 0805	C12, C13, C25			Digi-Key	490-5523-1-ND	
CAP ALUM 100UF 20% 35V SMD	C14	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951CT-ND	
CAP CER 680PF 50V C0G 0603	C19, C32, C33, C35, C36			Digi-Key	1276-1820-1-ND	
CAP CER 4.7UF 50V 10% X5R 0805	C22	Murata Electronics North America	GRT21BR61H475ME13L	Digi-Key	490-12395-1-ND	
CAP CER 2.2UF 100V ±20% X7R 1206	C24, C30, C31	Murata Electronics North America	GRM31CR72A225MA73L	Digi-Key	490-12773-1-ND	
DIODE TVS 15VWM 24.4VC DO-214AA (SMB)	D1	Fairchild/ON Semiconductor	SMBJ15CA	Digi-Key	SMBJ15CAFSCT-ND	
DIODE TVS 24VWM 70VC SOT23	D2, D3	Nexperia USA Inc.	PESD1CAN,215	Digi-Key	1727-3817-1-ND	
DIODE ZENER 16V 5W DO-214AA (SMB)	D4, D6, D7, D8			Digi-Key	SMBJ5353B-TPMSCT-ND	
DIODE GEN PURP 800V 8A SMC	D5			Digi-Key	S8KCDICT-ND	
DIODE SCHOTTKY 60V 3A SMA	D9	Diodes Incorporated	B360A-13-F	Digi-Key	B360A-FDICT-ND	
DIODE TVS 154V 246V DO-214AA (SMB)	D10, D11			Digi-Key	F10356CT-ND	
DIODE GEN PURP 100V 300MA SOD123	D12, D13, D14, D15, D16, D17			Digi-Key	1N4148WQ-7-FDICT-ND	
FUSE 3A 250VAC/450VDC RADIAL	F1, F2			Digi-Key	283-2768-ND	
HEATSINK 4xTO-247-duplicate	HS			Digi-Key	345-1574-ND	
IND 6.8uH 260mA 20% 1210	L1	TDK Corporation	NLFV32T-6R8M-EF	Digi-Key	445-15776-1-ND	
LED GREEN CLEAR 2V 0603	LED1			Digi-Key	732-4980-1-ND	
LED BLUE CLEAR 2.8V 0603	LED2, LED3	Lite-On Inc.	LTST-C193TBKT-5A	Digi-Key	160-1827-1-ND	
LED YELLOW CLEAR 2.1V 0603	LED4, LED6			Digi-Key	732-4981-1-ND	
LED RED CLEAR 2V 0603	LED5			Digi-Key	732-4978-1-ND	
FUSE HOLDER PC-TRON RADIAL	M2, M3			Digi-Key	283-2356-ND	
CONN 2POS ULTRA-FIT 0.138"	P1	Molex, LLC	1722861302	Digi-Key	WM11673-ND	
CONN 50POS Bergstak Plug 0.02"	P2	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	
CONN 4POS DURA-CLIK 0.079"	P3, P5			Digi-Key	WM10864CT-ND	
CONN 3POS ULTRA-FIT 0.138"	P4	Molex, LLC	1722871103	Digi-Key	WM11702-ND	
CONN 4POS ULTRA-FIT 0.138"	P6	Molex, LLC	1722871104	Digi-Key	WM11703-ND	
CONN 4POS MICRO-FIT 3mm	P7, P8			Digi-Key	WM10667-ND	
CONN 2POS MICRO-FIT 3mm	P9, P10, P11, P12			Digi-Key	WM10657-ND	
MOSFET P-CH 500V 10A 300W TO-263	Q1, Q2			Digi-Key	IXTA10P50P-ND	
MOSFET DEPLETION N-CH 500V 6A TO247	Q3			Digi-Key	IXTH6N50D2-ND	
MOSFET N-CH 650V 8A X2 TO-263	Q4			Digi-Key	IXTA8N65X2-ND	
MOSFET N-CH 60V 310MA SOT23	Q5, Q7, Q9, Q12			Digi-Key	DMN65D8L-7DICT-ND	
MOSFET N-CH 30V 8.7A 2.1W 6-PQFN (2x2)	Q6	Infineon Technologies	IRLHS6342TRPBF	Digi-Key	IRLHS6342TRPBFCT-ND	
MOSFET P-CH 30V 4A 1.6W SOT-23-6	Q8	STMicroelectronics	STT4P3LLH6	Digi-Key	497-15521-1-ND	
MOSFET P-CH 60V 3A SOT223	Q10			Digi-Key	KMP6A17GQTADIDKR-ND	
MOSFET N-CH 30V 6.2A 0.9W SOT-23	Q11, Q13, Q14			Digi-Key	DMN3023L-7DICT-ND	
RES 10K OHM 1% 1/10W 0603	1, R24, R27, R29, R30, R31, R32, R33, R34, R	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	
RES 200 OHM 5% 2/3W 1206	R3			Digi-Key	P200ALCT-ND	
RES 22.1 OHM 1% 1/10W 0603	R6, R7, R20, R25, R47, R54	Yageo	RC0603FR-0722R1L	Digi-Key	311-22.1HRCT-ND	
RES 1K OHM 15W 1% TO126	R8, R9, R39	CaddockElectronics Inc.	MP915-1.00K-1%	Digi-Key	MP915-1.00KF-ND	
RES SMD 470K OHM 0.1% 1/4W 1206	R11, R12, R15			Digi-Key	RG322P470K0DKR-ND	
RES SMD 29.4K OHM 1% 1/4W 1206	R13, R17			Digi-Key	P29.4KFCT-ND	
RES SMD 33K OHM 0.1% 1/4W 1206	R18			Digi-Key	YAG2038CT-ND	
RES 40.2 OHM 0.5% 1/10W 0603	R19	Yageo	RT0603DRE0740R2L	Digi-Key	311-2576-1-ND	
RES SMD 0 OHM JUMPER 1/4W 1206	R22			Digi-Key	541-0.0ECT-ND	
RES SMD 2K OHM 0.1% 1/4W 1206	R23			Digi-Key	P2.0KBCCT-ND	
RES 1M OHM 1% 1/10W 0603	R26, R51, R53, R56, R59	Yageo	RC0603FR-071ML	Digi-Key	311-1.00MHRCT-ND	
RES 1K OHM 5% 1/10W 0603	R28, R36, R44, R55, R57, R60			Digi-Key	311-1.0KGRCT-ND	
RES 5K OHM 25W 1% TO220	R40	CaddockElectronics Inc.	MP925-5.00K-1%	Digi-Key	MP925-5.00KF-ND	
RES 4.7K OHM 1% 1/10W 0603	R43, R46	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	
RES ARRAY 10K OHM 0.1% 2RES 0606	R45			Digi-Key	749-1046-1-ND	
RES 820 OHM 5% 1/4W 0603	R50	Rohm Semiconductor	ESR03EZPJ821	Digi-Key	RHM820DCT-ND	
RES 100 OHM 1% 1/10W 0603	R52	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	
TestPoint	TP1					
CAN SPI CONTROLLER MCP2515T-I/ST 20-TSS	U1			Digi-Key	MCP2515T-I/STCT-ND	
IC CAN Tranceiver TCAN332DR	U2			Digi-Key	296-43711-1-ND	
IC LOAD SWITCH ACT-HI 10.5A 8DFN	U3			Digi-Key	455211MNTWG-HOSDKR-ND	
IC REG SWITCHED CAP INV 20MA 8MSOP	U4			Digi-Key	LTC1966EMS8#TRPBFCT-ND	

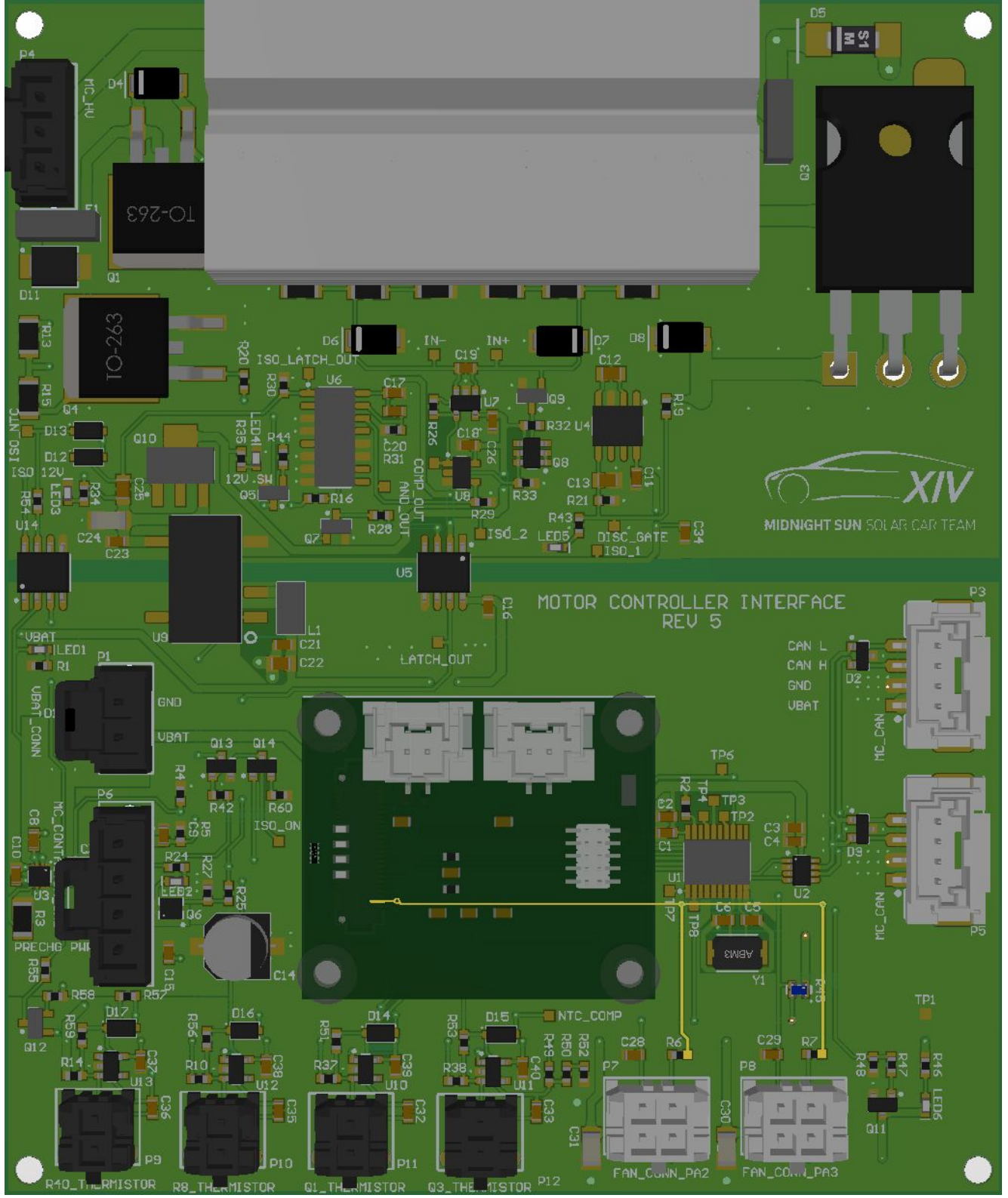
R26

U5

TP5

C6


MS40014 REV 4.0


MOTOR CONTROLLER INTERFACE
REV 5
MIDNIGHT SUN SOLAR CAR TEAM
XIV
CAN L
CAN H
GND
VBAT
MC_CAN
MC_CAN
MC_HV
MC_CONT
VBAT_CONN
PRECHG PWR
ISO_LATCH_OUT
ISO_ON
LATCH_OUT
COMP_OUT
AND_OUT
ISO_2
ISO_1
DISC_GATE
12V_SW
NTC_COMP
FAN_CONN_PA2
FAN_CONN_PA3
R40_THERMISTOR
R8_THERMISTOR
Q1_THERMISTOR
Q3_THERMISTOR
TO-263
TO-263
ABM3

Design Rules Verification Report

Filename : C:\Users\James\Documents\hardware-master\MSXII_PreChargeController\

Warnings 0
Rule Violations 180

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=10mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	117
Silk to Silk (Clearance=0.254mm) (All),(All)	60
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	3
Height Constraint (Min=0mm) (Max=200mm) (Prefered=12.7mm) (All)	0
Total	180

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C1-2(65.557mm,16.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-1(39.779mm,60.525mm) on Top Layer And Text "C17"
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-2(38.429mm,60.525mm) on Top Layer And Text "C17"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C2-2(65.575mm,18mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C37-1(13.689mm,-7.304mm) on Top Layer And Text "C37"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C37-2(13.689mm,-5.954mm) on Top Layer And Text "C37"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C38-1(26.285mm,-7.72mm) on Top Layer And Text "C38"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C38-2(26.285mm,-6.37mm) on Top Layer And Text "C38"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C39-1(39.215mm,-7.77mm) on Top Layer And Text "C39"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C39-2(39.215mm,-6.42mm) on Top Layer And Text "C39"
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad C40-1(51.85mm,-7.97mm) on Top Layer And Text "U11"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C7-2(8.333mm,13.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.098mm < 0.178mm) Between Pad DISC_GATE-TP(61.02mm,47.15mm) on Top Layer And Tex
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad LED2-1(18mm,11.5mm) on Top Layer And Text "LED2"
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad LED2-2(16.5mm,11.5mm) on Top Layer And Text "LED2"
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P10-0(18.9mm,-16.09mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P10-0(18.9mm,-16.09mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P10-0(24.9mm,-16.09mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P10-0(24.9mm,-16.09mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P11-0(31.746mm,-16.23mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P11-0(31.746mm,-16.23mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P11-0(37.746mm,-16.23mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P11-0(37.746mm,-16.23mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P12-0(44.65mm,-16.339mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P12-0(44.65mm,-16.339mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P12-0(50.65mm,-16.339mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P12-0(50.65mm,-16.339mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P3-7(95mm,25.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P3-7(95mm,38.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P5-7(95mm,21.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad P5-7(95mm,8.05mm) on Top Layer And Text "P5"
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P5-7(95mm,8.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P9-0(12.375mm,-15.799mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P9-0(12.375mm,-15.799mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P9-0(6.375mm,-15.799mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P9-0(6.375mm,-15.799mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q11-1(88.795mm,-9.873mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q11-2(86.995mm,-9.873mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q13-1(20.875mm,22.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q13-2(22.675mm,22.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q14-1(24.935mm,22.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q14-2(26.735mm,22.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Q5-2(26.025mm,51.635mm) on Top Layer And Text "12V SW"
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-1(17.656mm,8.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-3(17.656mm,9.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-4(15.806mm,9.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-6(15.806mm,8.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.178mm) Between Pad R15-2(2.492mm,58.695mm) on Top Layer And Text "ISO_NTC"

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.067mm < 0.178mm) Between Pad R29-2(47.2mm,49.575mm) on Top Layer And Text "U8"
Silk To Solder Mask Clearance Constraint: (0.103mm < 0.178mm) Between Pad R45-1(80.2mm,0.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.103mm < 0.178mm) Between Pad R45-2(80.2mm,1.09mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.103mm < 0.178mm) Between Pad R45-3(78.85mm,1.09mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.103mm < 0.178mm) Between Pad R45-4(78.85mm,0.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.115mm < 0.178mm) Between Pad TP3-TP(70.989mm,19.609mm) on Top Layer And Text "TP4
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U10-1(35.063mm,-6.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U10-2(35.063mm,-7.345mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U10-3(35.063mm,-8.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U10-4(37.363mm,-8.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U10-5(37.363mm,-6.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U11-1(47.82mm,-6.645mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U11-2(47.82mm,-7.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U11-3(47.82mm,-8.545mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U11-4(50.12mm,-8.545mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U11-5(50.12mm,-6.645mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U12-1(22.124mm,-6.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U12-2(22.124mm,-7.345mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U12-3(22.124mm,-8.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U12-4(24.424mm,-8.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U12-5(24.424mm,-6.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U13-1(9.589mm,-6.095mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U13-2(9.589mm,-7.045mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U13-3(9.589mm,-7.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U13-4(11.889mm,-7.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U13-5(11.889mm,-6.095mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U14-1(2.078mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U14-2(3.348mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U14-3(4.618mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U14-4(5.888mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U14-5(5.888mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U14-6(4.618mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U14-7(3.348mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U14-8(2.078mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-1(78.425mm,13.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-2(78.425mm,12.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-3(78.425mm,12.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-4(78.425mm,11.625mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-5(81.075mm,11.625mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-6(81.075mm,12.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-7(81.075mm,12.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-8(81.075mm,13.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.162mm < 0.178mm) Between Pad U3-1(4.3mm,12.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad U3-4(2.8mm,12.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad U3-5(2.8mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad U3-8(4.05mm,11.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad U3-8(4.3mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U3-9(3.55mm,12mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-1(45.939mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-2(44.669mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-3(43.399mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-4(42.129mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-5(42.129mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-6(43.399mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-7(44.669mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-8(45.939mm,39.705mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-1(47.2mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-2(46.25mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-3(45.3mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-4(45.3mm,58.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-5(47.2mm,58.35mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.055mm < 0.254mm) Between Arc (14.306mm,50.35mm) on Top Overlay And Text "C25"
Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Arc (4.65mm,13.45mm) on Top Overlay And Text "MC_CONTACTOR_GND"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (22.1mm,-17.55mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.165mm < 0.254mm) Between Text "1" (34.946mm,-17.69mm) on Top Overlay And Text "Q1_THERMISTOR"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (34.946mm,-17.69mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "1" (47.85mm,-17.799mm) on Top Overlay And Text "Q3_THERMISTOR"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (47.85mm,-17.799mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (9.575mm,-17.259mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C15" (16.128mm,2.618mm) on Top Overlay And Text "R57"
Silk To Silk Clearance Constraint: (0.208mm < 0.254mm) Between Text "C25" (13.126mm,51.935mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.208mm < 0.254mm) Between Text "C25" (13.126mm,51.935mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.246mm < 0.254mm) Between Text "C38" (27.035mm,-6.017mm) on Top Overlay And Text "U12"
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "C40" (52.77mm,-6.17mm) on Top Overlay And Text "U11"
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "C7" (7.749mm,14.382mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D11" (1.667mm,70mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "D17" (10.339mm,-1.986mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D17" (10.339mm,-1.986mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.227mm < 0.254mm) Between Text "D2" (84.366mm,31.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.126mm < 0.254mm) Between Text "D4" (10.5mm,91.193mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "D7" (59.124mm,65.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "D8" (62.696mm,65.687mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.192mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.156mm < 0.254mm) Between Text "ISO_LATCH_OUT" (25.475mm,63.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "ISO_ON" (25.18mm,16.712mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "LED1" (5.4mm,34.355mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.211mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.007mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.097mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.095mm < 0.254mm) Between Text "LED4" (24.8mm,58.547mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.18mm < 0.254mm) Between Text "MC_CONTACTOR_GND" (5.005mm,19.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.136mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.117mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "P5" (96.83mm,6.152mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.177mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.173mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.217mm < 0.254mm) Between Text "Q5" (23.75mm,49.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "Q6" (18.356mm,7.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.242mm < 0.254mm) Between Text "R25" (23.342mm,10.85mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "R9" (49.363mm,75.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "U10" (38.288mm,-9.359mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.252mm < 0.254mm) Between Text "U10" (38.288mm,-9.359mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.103mm < 0.254mm) Between Text "U12" (25.349mm,-9.345mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.107mm < 0.254mm) Between Text "U12" (25.349mm,-9.345mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "U13" (12.725mm,-9.017mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "U13" (12.725mm,-9.017mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.232mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.147mm < 0.254mm) Between Text "U4" (57.2mm,56.82mm) on Top Overlay And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "U6" (32.398mm,61.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.206mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "Q1_THERMISTOR" (30.2mm,-19.6mm) on Top
Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "Q3_THERMISTOR" (42.6mm,-19.6mm) on Top
Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "R8_THERMISTOR" (17mm,-19.6mm) on Top