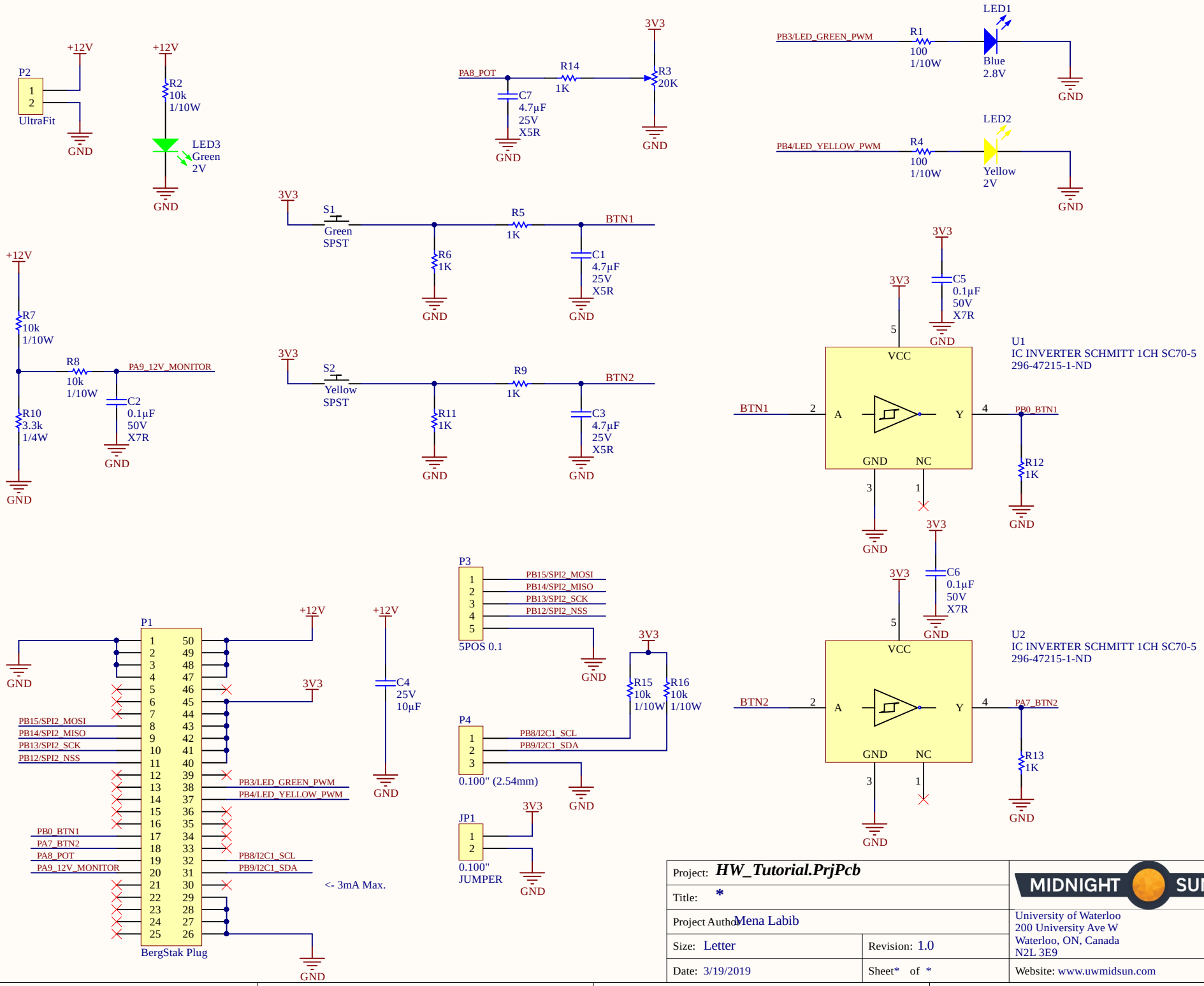
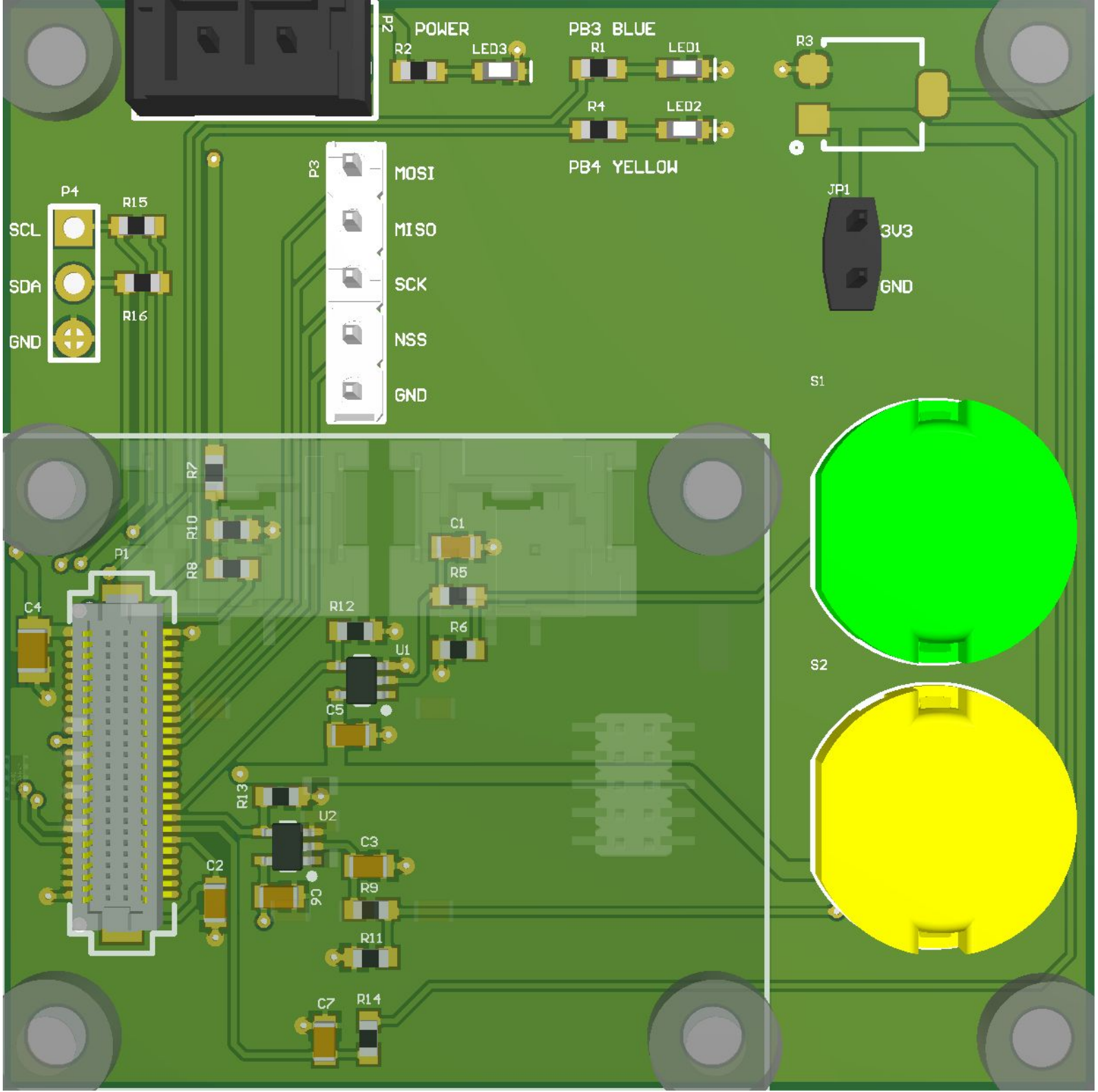
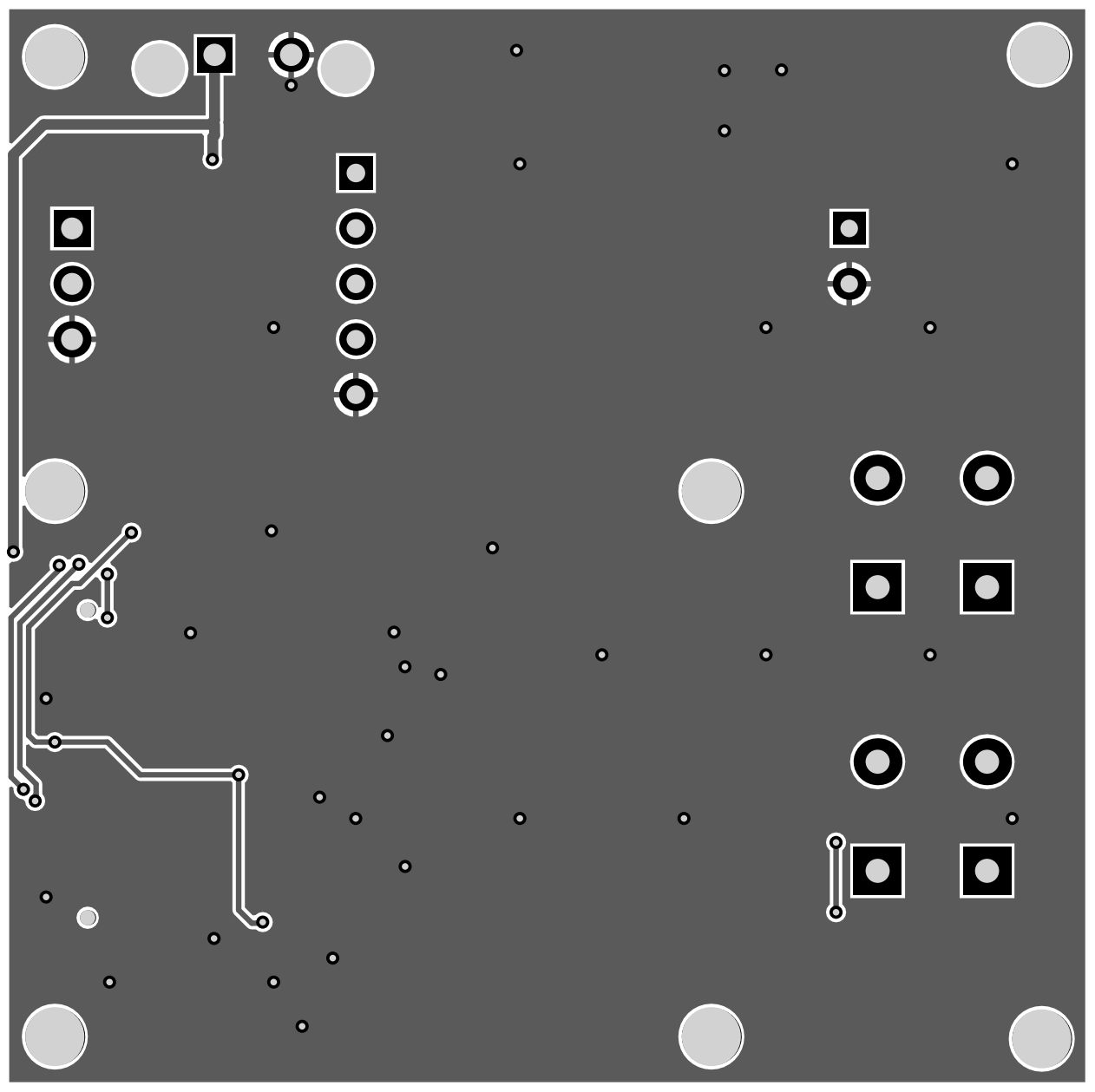

P2
UltraFit
+12V
GND
R2
10k
1/10W
LED3
Green
2V
PA8_POT
R14
1K
R3
20K
C7
4.7µF
25V
X5R
3V3
PB3/LED_GREEN_PWM
R1
100
1/10W
LED1
Blue
2.8V
PB4/LED_YELLOW_PWM
R4
100
1/10W
LED2
Yellow
2V
S1
Green
SPST
R5
1K
BTN1
R6
1K
C1
4.7µF
25V
X5R
R7
10k
1/10W
R8
10k
1/10W
PA9_12V_MONITOR
C2
0.1µF
50V
X7R
R10
3.3k
1/4W
S2
Yellow
SPST
R9
1K
BTN2
R11
1K
C3
4.7µF
25V
X5R
C5
0.1µF
50V
X7R
U1
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
VCC
A
Y
GND
NC
PB0_BTN1
R12
1K
C6
0.1µF
50V
X7R
U2
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
PA7_BTN2
R13
1K
P1
BergStak Plug
PB15/SPI2_MOSI
PB14/SPI2_MISO
PB13/SPI2_SCK
PB12/SPI2_NSS
PB0_BTN1
PA7_BTN2
PA8_POT
PA9_12V_MONITOR
PB3/LED_GREEN_PWM
PB4/LED_YELLOW_PWM
PB8/I2C1_SCL
PB9/I2C1_SDA
C4
25V
10µF
<- 3mA Max.
P3
5POS 0.1
R15
10k
1/10W
R16
10k
1/10W
P4
0.100" (2.54mm)
JP1
0.100"
JUMPER
Project: HW_Tutorial.PrjPcb
Title: *
Project Author: Mena Labib
Size: Letter
Revision: 1.0
Date: 3/19/2019
Sheet* of *
MIDNIGHT SUN
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9
Website: www.uwmidsun.com


P2
POWER
R2
LED3
PB3 BLUE
R1
LED1
R4
LED2
PB4 YELLOW
R3
P3
MOSI
MISO
SCK
NSS
GND
P4
SCL
SDA
GND
R15
R16
JP1
3V3
GND
S1
S2
P1
C4
R7
R10
R8
C1
R5
R12
R6
U1
C5
R13
U2
C3
R9
R11
C2
C6
C7
R14



Electrical Rules Check Repor

Class	Document	Message
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 (Inferred) in Alternate 1 of part R
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 in Normal of part R?
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 (Inferred) in Alternate 1 of part R
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 in Normal of part R?

Design Rules Verification Repor

Filename : \\Mac\Home\Documents\midsun\hardware\MSXII_HW_Tutorial\hw_tutorial.Pcb

Warnings 0
Rule Violations 112

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All	0
Short-Circuit Constraint (Allowed=No) (All),(All	0
Un-Routed Net Constraint ((All)	0
Modified Polygon (Allow modified: No), (Allow shelved: Nc	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (Al	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mr	0
Minimum Annular Ring (Minimum=0.152mm) (Al	47
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All	0
Hole To Hole Clearance (Gap=0.254mm) (All),(Al	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All	38
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(Al	8
Silk to Silk (Clearance=0.254mm) (All),(All	1
Net Antennae (Tolerance=0mm) (All	0
Board Clearance Constraint (Gap=0mm) (All	18
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (Al	0
Total	112

Minimum Annular Ring (Minimum=0.152mm) (Al
Minimum Annular Ring: (0.15mm < 0.152mm) Via (0.606mm,24.719mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.068mm,13.832mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.6mm,13.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (10.9mm,14.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.4mm,25.68mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12mm,7.75mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.3mm,46.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.8mm,2.975mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.6mm,13.475mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.2mm,6.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (17.7mm,16.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.508mm,10.3mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.5mm,19.45mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18mm,21.037mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.101mm,8.9mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.1mm,18mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.5mm,16mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.7mm,24.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (20.133mm,19.1mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (22.5mm,24.9mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.6mm,47.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (3.6mm,24.15mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,44.012mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,46.77mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35.708mm,46.802mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.2mm,11.4mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.2mm,8.2mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (4.9mm,21.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (4.9mm,23.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,12.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,42.5mm) from Top Layer to Bottom Layer (Annu
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (6mm,25.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.7mm,21mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.775mm,7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.7mm,42.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15m

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(20.133mm,24.9mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.089mm < 0.3mm) Between Pad C1-2(21.483mm,24.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(9.8mm,9.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C2-2(9.8mm,7.95mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(16.125mm,10.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad C3-2(17.475mm,10.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.3mm) Between Pad C4-2(1.476mm,19.295mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(15.325mm,16.3mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad C5-2(16.675mm,16.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(12.025mm,8.9mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad C6-1(12.025mm,8.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(14.8mm,1.625mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C7-2(14.8mm,2.975mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED1-2(31.939mm,46.805mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED2-2(31.939mm,44.012mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad LED3-2(23.55mm,46.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.112mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And P
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad P1-(5.5mm,22.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P1-1(7.3mm,21mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad P1-2(7.3mm,20.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-39(3.7mm,15.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-41(3.7mm,16.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad P1-44(3.7mm,18mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.237mm < 0.3mm) Between Pad P1-50(3.7mm,21mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.3mm) Between Pad P2-2(13.3mm,47.495mm) on Multi-Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad R10-2(11.325mm,25.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad R12-1(16.975mm,21.075mm) on Top Layer A
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad R13-1(13.575mm,13.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.239mm < 0.3mm) Between Pad R3-3(37.1mm,46.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad R6-1(20.133mm,20.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-1(17.6mm,18.15mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-2(17.6mm,18.8mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.126mm < 0.3mm) Between Pad U1-2(17.6mm,18.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-1(14.2mm,10.55mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-2(14.2mm,11.2mm) on Top Layer And F
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.3mm) Between Via (2.7mm,24.1mm) from Top Layer to Bottom La

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(Al
Silk To Solder Mask Clearance Constraint: (0.082mm < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P4-2(3.286mm,37mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P4-2(3.286mm,37mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer A
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer A

Silk to Silk (Clearance=0.254mm) (All),(All
Silk To Silk Clearance Constraint: (0.183mm < 0.254mm) Between Text "P2" (17.477mm,49.2mm) on Top Overlay And Tr

Board Clearance Constraint (Gap=0mm) (All
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "GND" (0.4mm,34.06mm) on T
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "SCL" (0.4mm,39.2mm) on T
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "SDA" (0.4mm,36.6mm) on T
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm)
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30m
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,30m
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Tra
Board Outline Clearance(Outline Edge): (0.306mm < 0.406mm) Between Board Edge And Via (0.606mm,24.719mm) from T