

A

B

C

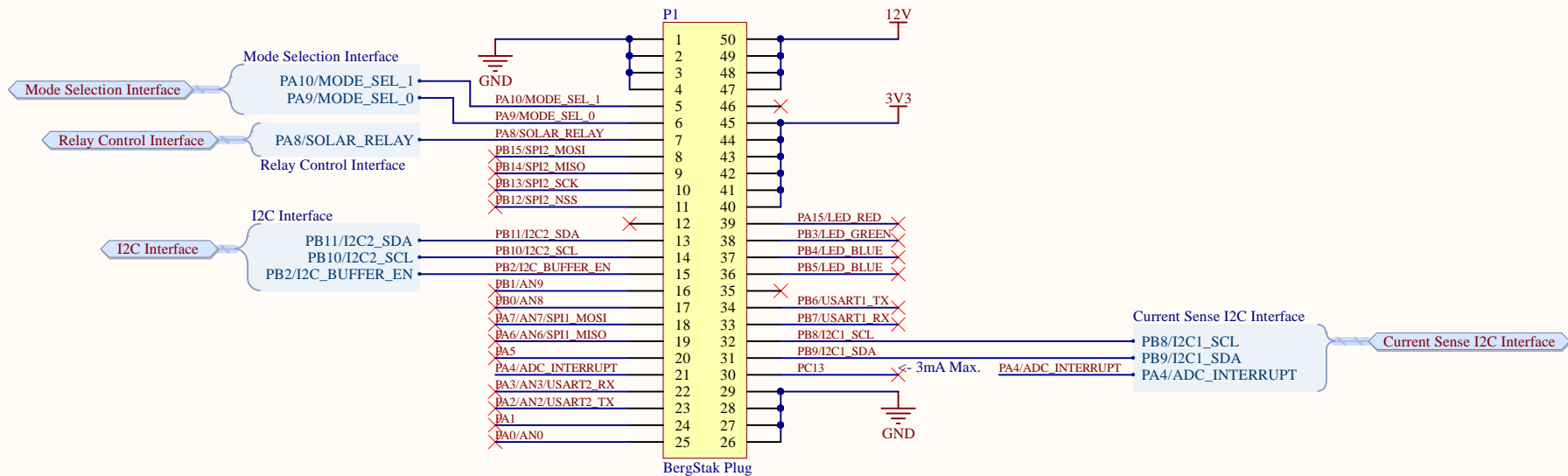
D


A

B

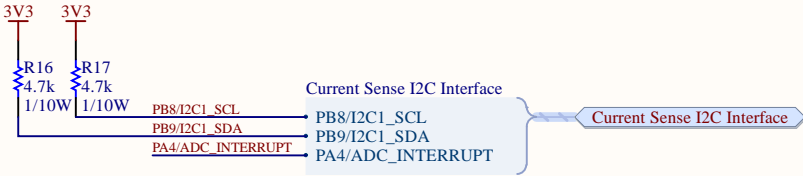
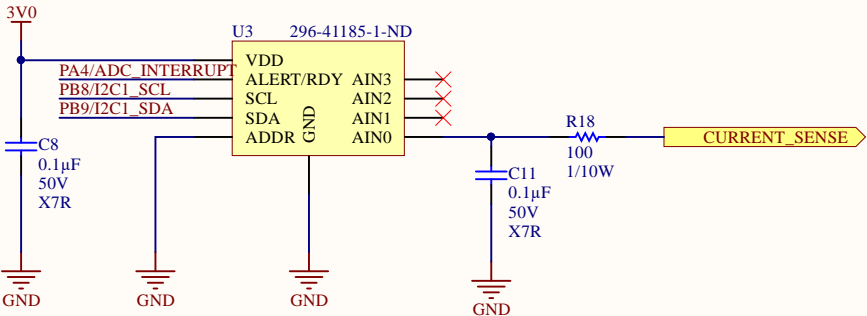
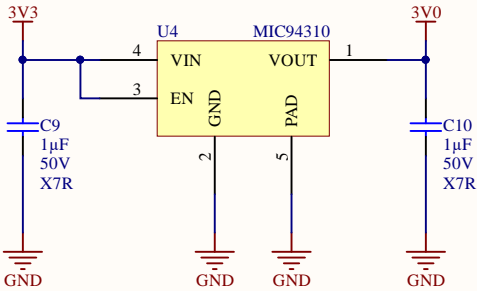
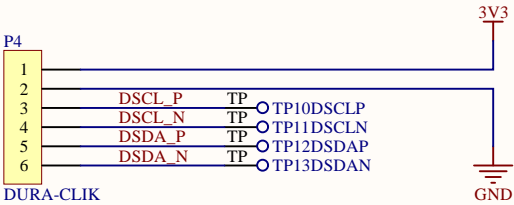
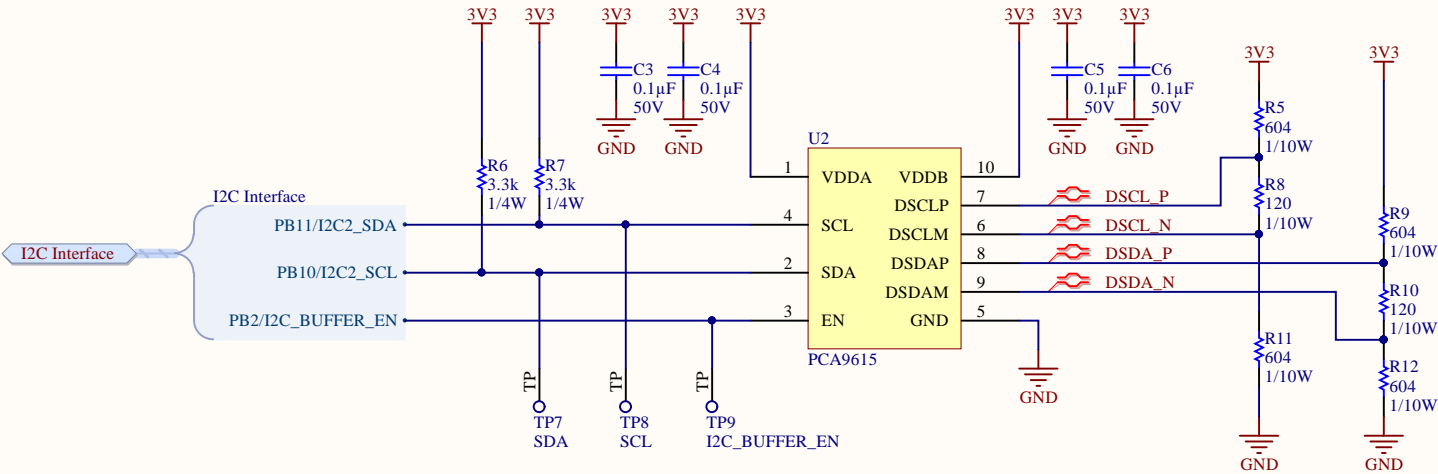
C


D



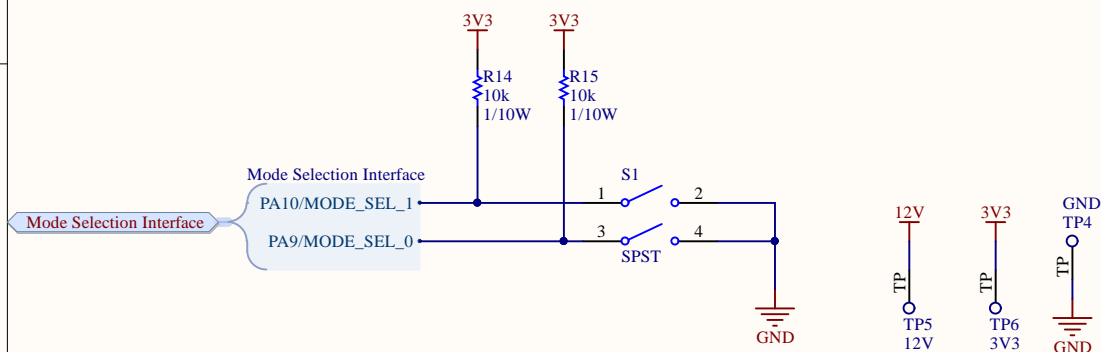
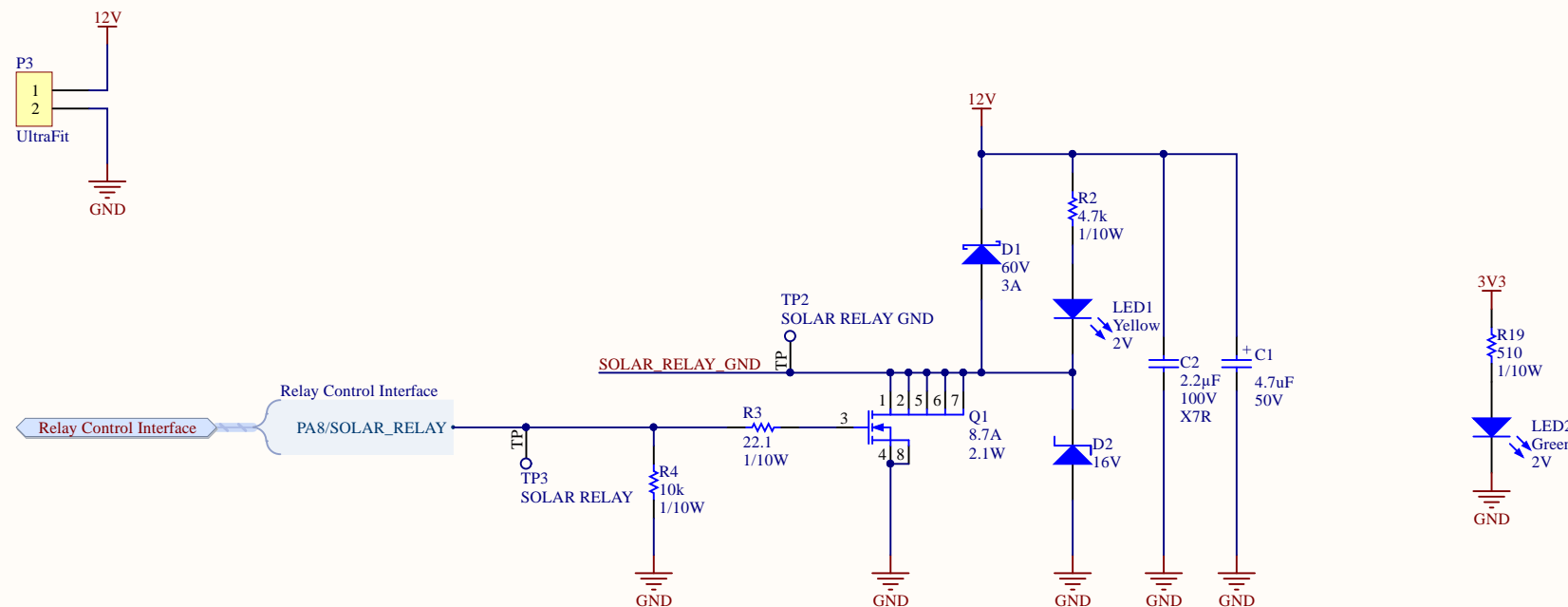
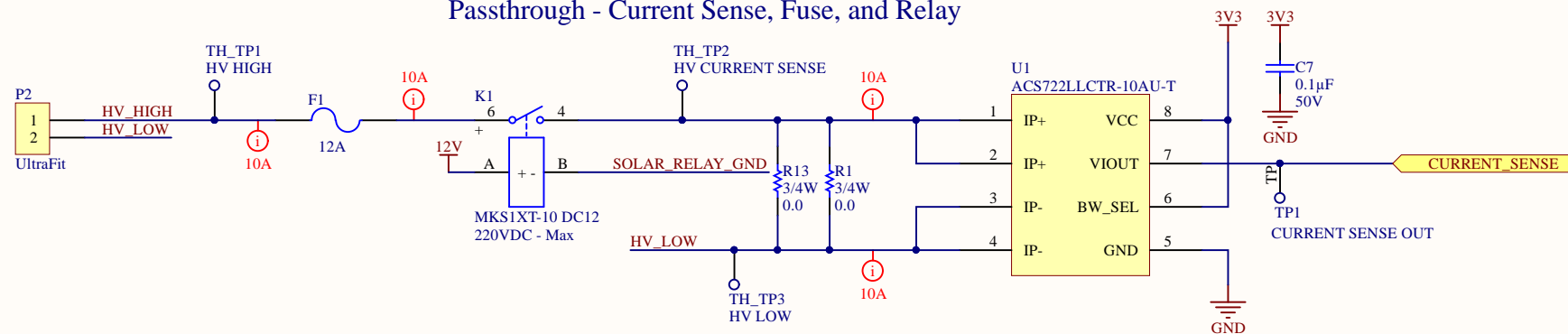
Project: <i>MSXII_SolarSenseMaster.PrjPcb</i>		
Title: *		
Project Author: <i>Peiliang Guo</i>		<i>University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9</i>
Size: <i>Letter</i>	Revision: <i>1.0</i>	
Date: <i>2018-07-08</i>	Sheet* of *	
		Website: <i>www.uwmidsun.com</i>


I2C Interface

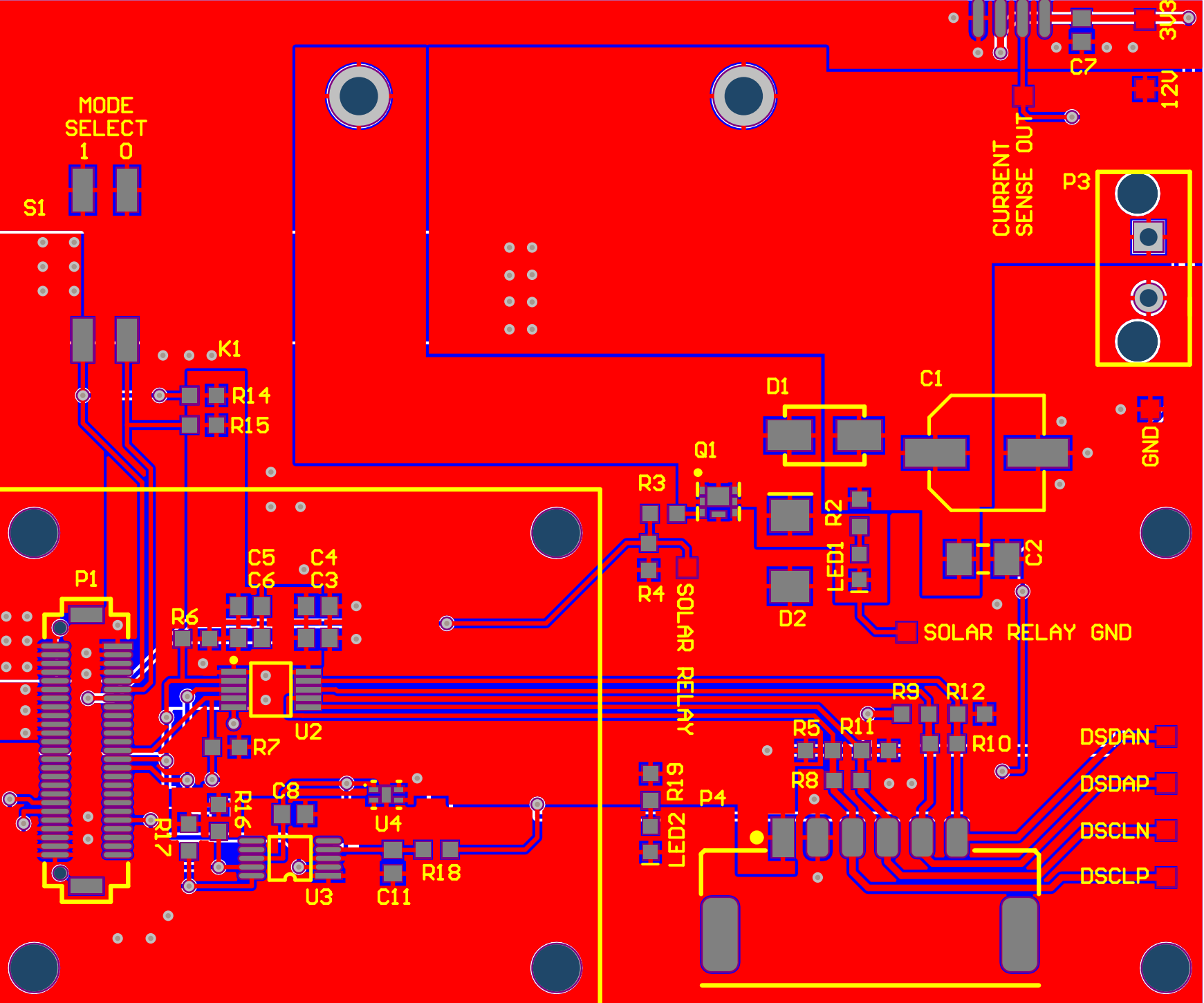
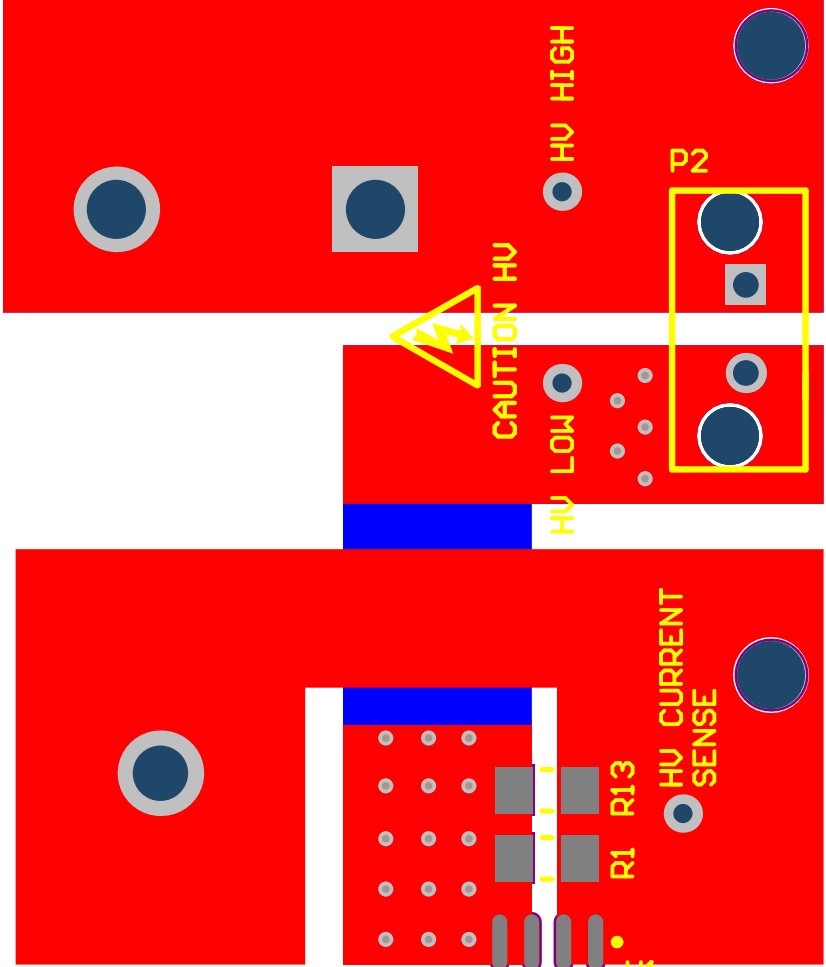
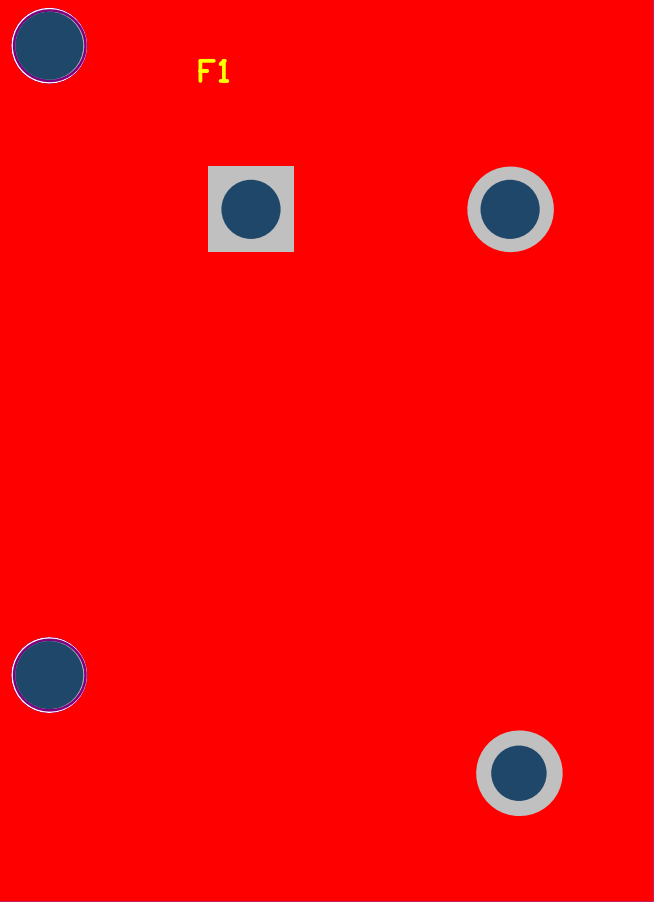


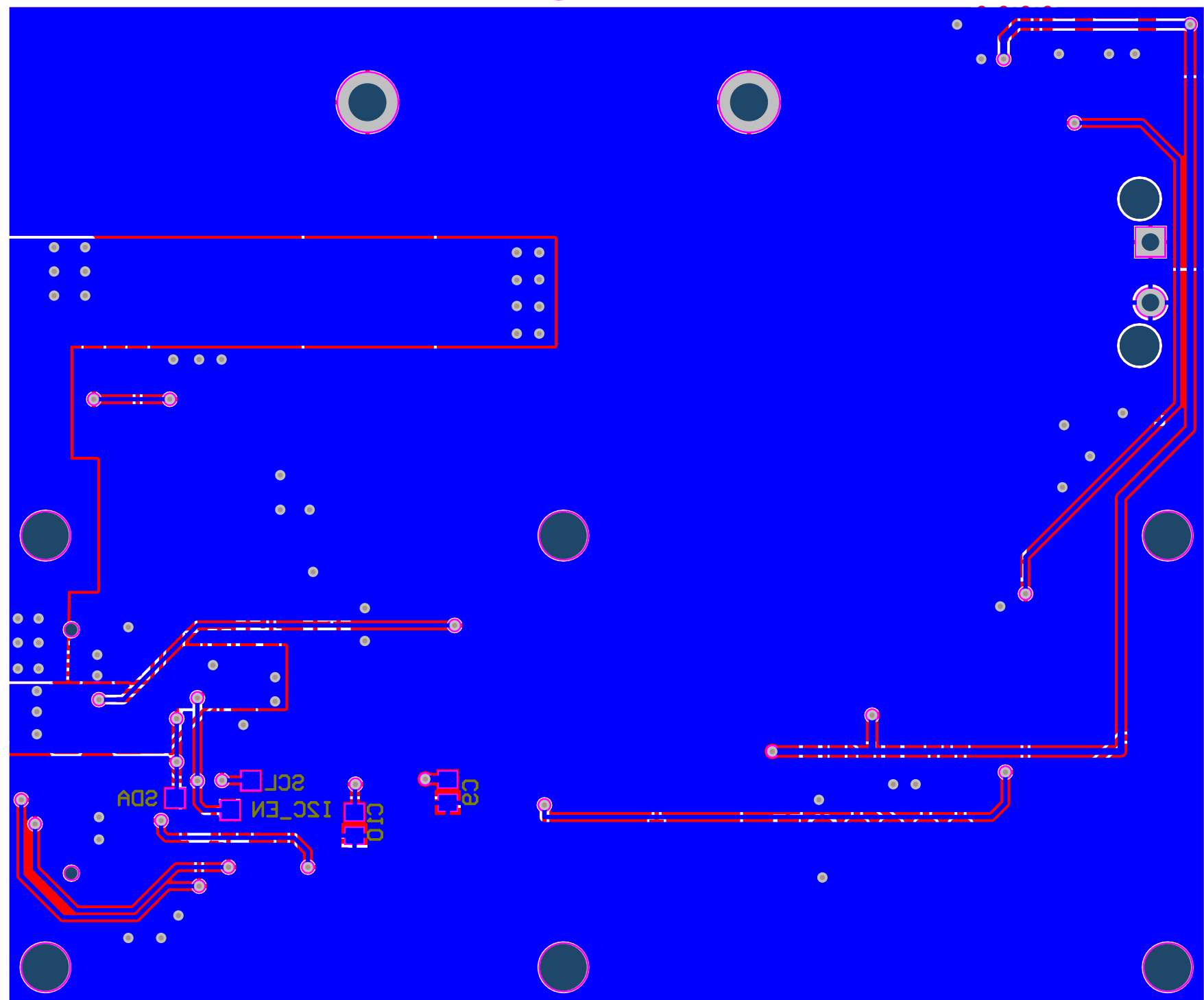
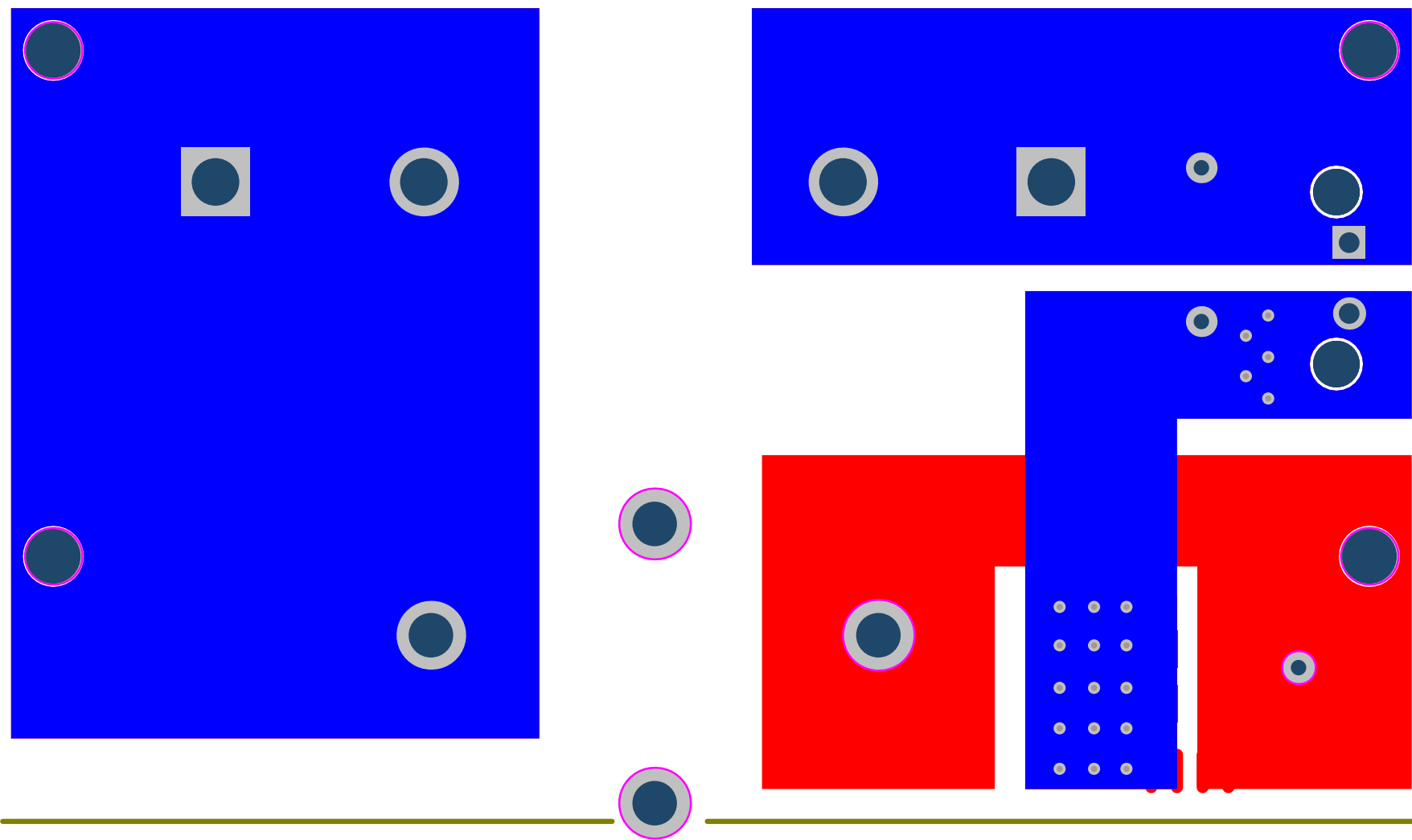
Project: <i>MSXII_SolarSenseMaster.PrjPcb</i>		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: *		
Project Author: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-07-08	Sheet* of *	Website: www.uwmidsun.com

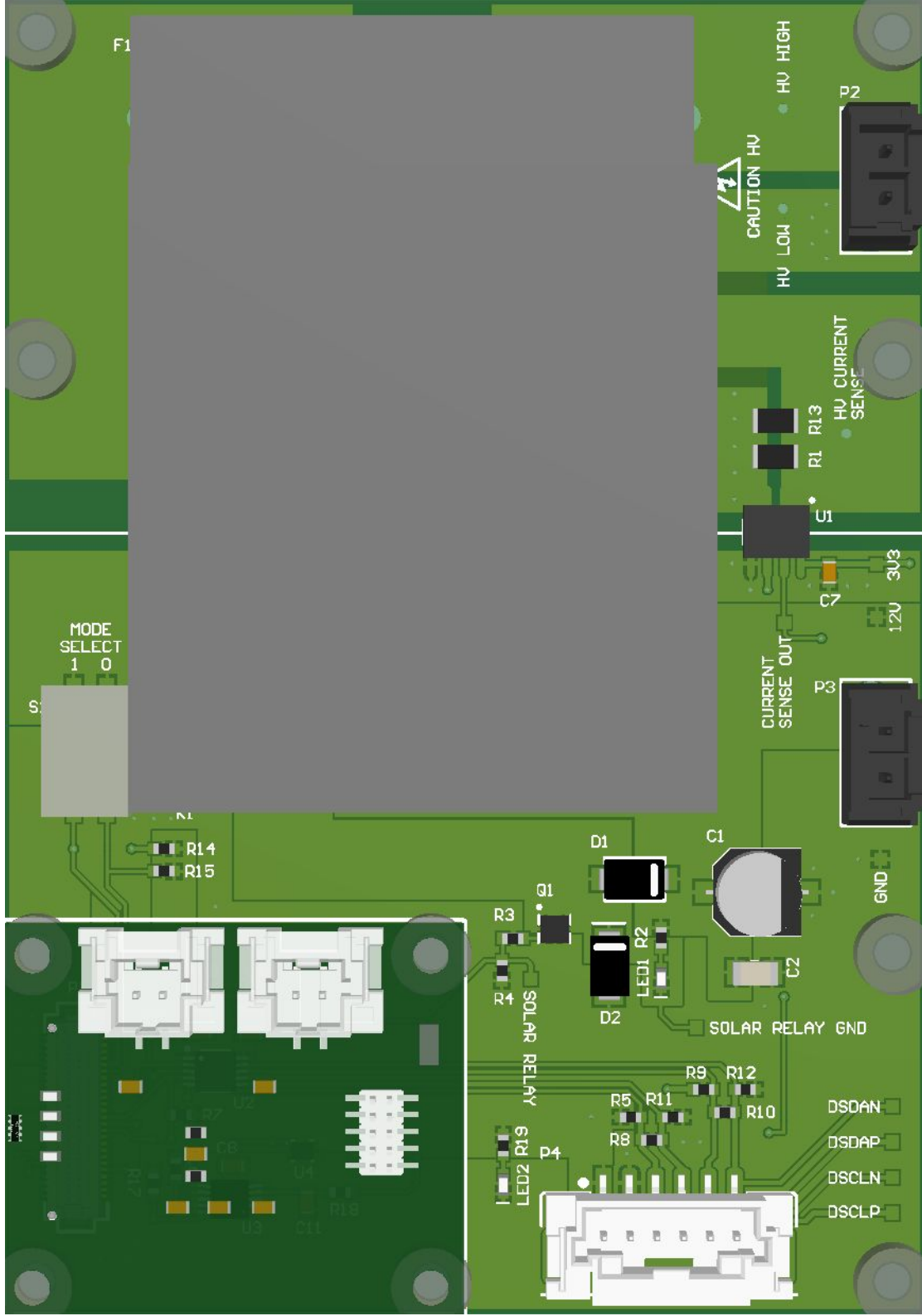
Passthrough - Current Sense, Fuse, and Relay



Project: <i>MSXII_SolarSenseMaster.PrpjPcb</i>		
Title: *		
Project Author: Peiliang Guo		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2018-07-08	Sheet* of *	
		Website: www.uwmidsun.com







Electrical Rules Check Report

Class	Document	Message
		Successful Compile for MSXII_SolarSenseMaster.PrjPcb

Design Rules Verification Report

Filename : C:\Users\peiliang.guo\uw-midsun\hardware\MSXII_SolarSenseMaster\SolarSense

Warnings 0

Rule Violations 66

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.4mm) (Preferred=0.4mm) (InNet('3V3'))	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	36
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	22
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	8
Height Constraint (Min=0mm) (Max=70mm) (Preferred=12.7mm) (InComponent('K1') OR InComponent('K2'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	66

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(20.4mm,11.475mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(23.1mm,9.275mm) on Top Layer And Pad C11-2(23.1mm,7.925mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(18.125mm,21.469mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(18.125mm,23.274mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(14.225mm,23.274mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(14.225mm,21.469mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(62.664mm,57.075mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(16.725mm,11.329mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(25.8mm,13.375mm) on Bottom Layer And Pad C9-2(25.8mm,12.025mm)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And Pad P1-(5.5mm,22.8mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And Pad P1-(5.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-1(40.875mm,29.95mm) on Top Layer And Pad Q1-2(40.875mm,29.3mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-2(40.875mm,29.3mm) on Top Layer And Pad Q1-3(40.875mm,28.65mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-2(40.875mm,29.3mm) on Top Layer And Pad Q1-8(41.8mm,28.56mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-3(40.875mm,28.65mm) on Top Layer And Pad Q1-7(41.8mm,29.6mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-3(40.875mm,28.65mm) on Top Layer And Pad Q1-8(41.8mm,28.56mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(42.725mm,28.65mm) on Top Layer And Pad Q1-5(42.725mm,29.3mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-4(42.725mm,28.65mm) on Top Layer And Pad Q1-7(41.8mm,29.6mm) on
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.3mm) Between Pad Q1-4(42.725mm,28.65mm) on Top Layer And Pad Q1-8(41.8mm,28.56mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad Q1-5(42.725mm,29.3mm) on Top Layer And Pad Q1-6(42.725mm,29.95mm) on
Minimum Solder Mask Sliver Constraint: (0.275mm < 0.3mm) Between Pad Q1-5(42.725mm,29.3mm) on Top Layer And Pad Q1-8(41.8mm,28.56mm) on
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.3mm) Between Pad Q1-7(41.8mm,29.6mm) on Top Layer And Pad Q1-8(41.8mm,28.56mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-1(13.96mm,19.5mm) on Top Layer And Pad U2-2(13.96mm,19mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-10(18.24mm,19.5mm) on Top Layer And Pad U2-9(18.24mm,19mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-2(13.96mm,19mm) on Top Layer And Pad U2-3(13.96mm,18.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-3(13.96mm,18.5mm) on Top Layer And Pad U2-4(13.96mm,18mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-4(13.96mm,18mm) on Top Layer And Pad U2-5(13.96mm,17.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-6(18.24mm,17.5mm) on Top Layer And Pad U2-7(18.24mm,18mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-7(18.24mm,18mm) on Top Layer And Pad U2-8(18.24mm,18.5mm) on Top
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad U2-8(18.24mm,18.5mm) on Top Layer And Pad U2-9(18.24mm,19mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-1(22.014mm,12.75mm) on Top Layer And Pad U4-2(22.014mm,12.15mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U4-1(22.014mm,12.75mm) on Top Layer And Pad U4-5(22.729mm,12.45mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U4-2(22.014mm,12.15mm) on Top Layer And Pad U4-5(22.729mm,12.45mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U4-3(23.454mm,12.15mm) on Top Layer And Pad U4-4(23.454mm,12.75mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U4-3(23.454mm,12.15mm) on Top Layer And Pad U4-5(22.729mm,12.45mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U4-4(23.454mm,12.75mm) on Top Layer And Pad U4-5(22.729mm,12.45mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-1(45.869mm,33.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-1(45.869mm,33.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-2(49.869mm,33.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D1-2(49.869mm,33.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-1(40.875mm,29.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(40.875mm,29.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-2(40.875mm,29.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-3(40.875mm,28.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-4(42.725mm,28.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(42.725mm,29.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q1-5(42.725mm,29.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q1-6(42.725mm,29.95mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U3-1(19.4mm,7.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-10(15mm,7.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-2(19.4mm,8.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-3(19.4mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-4(19.4mm,9.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-5(19.4mm,9.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-6(15mm,9.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-7(15mm,9.3mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-8(15mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad U3-9(15mm,8.3mm) on Top Layer And Track

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,59.4mm)(30.1mm,59.4mm) on Bottom Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,59.4mm)(30.1mm,59.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (34.8mm,59.4mm)(70mm,59.4mm) on Bottom Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (34.8mm,59.4mm)(70mm,59.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,30mm) on Top Overlay