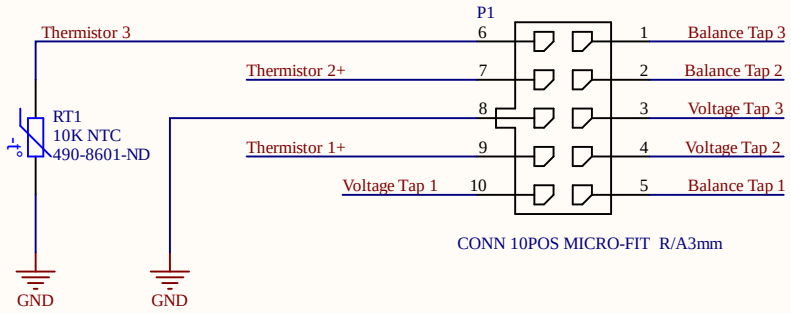
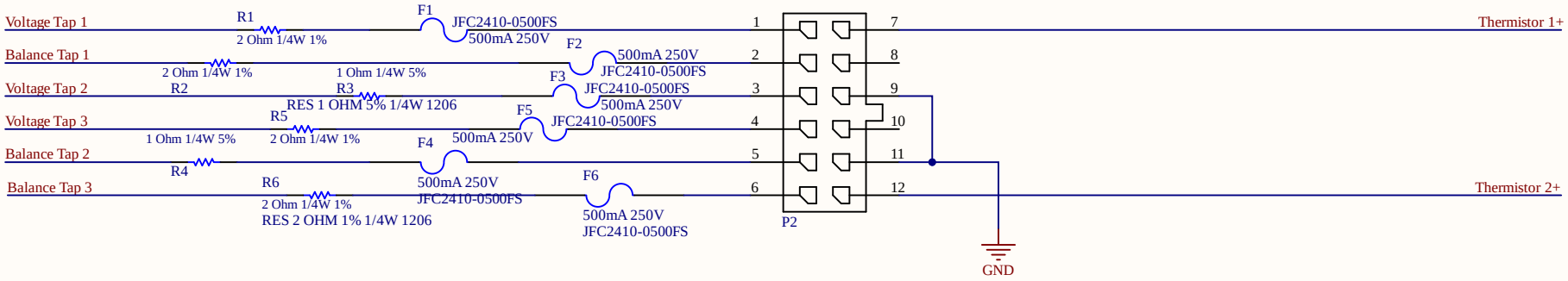
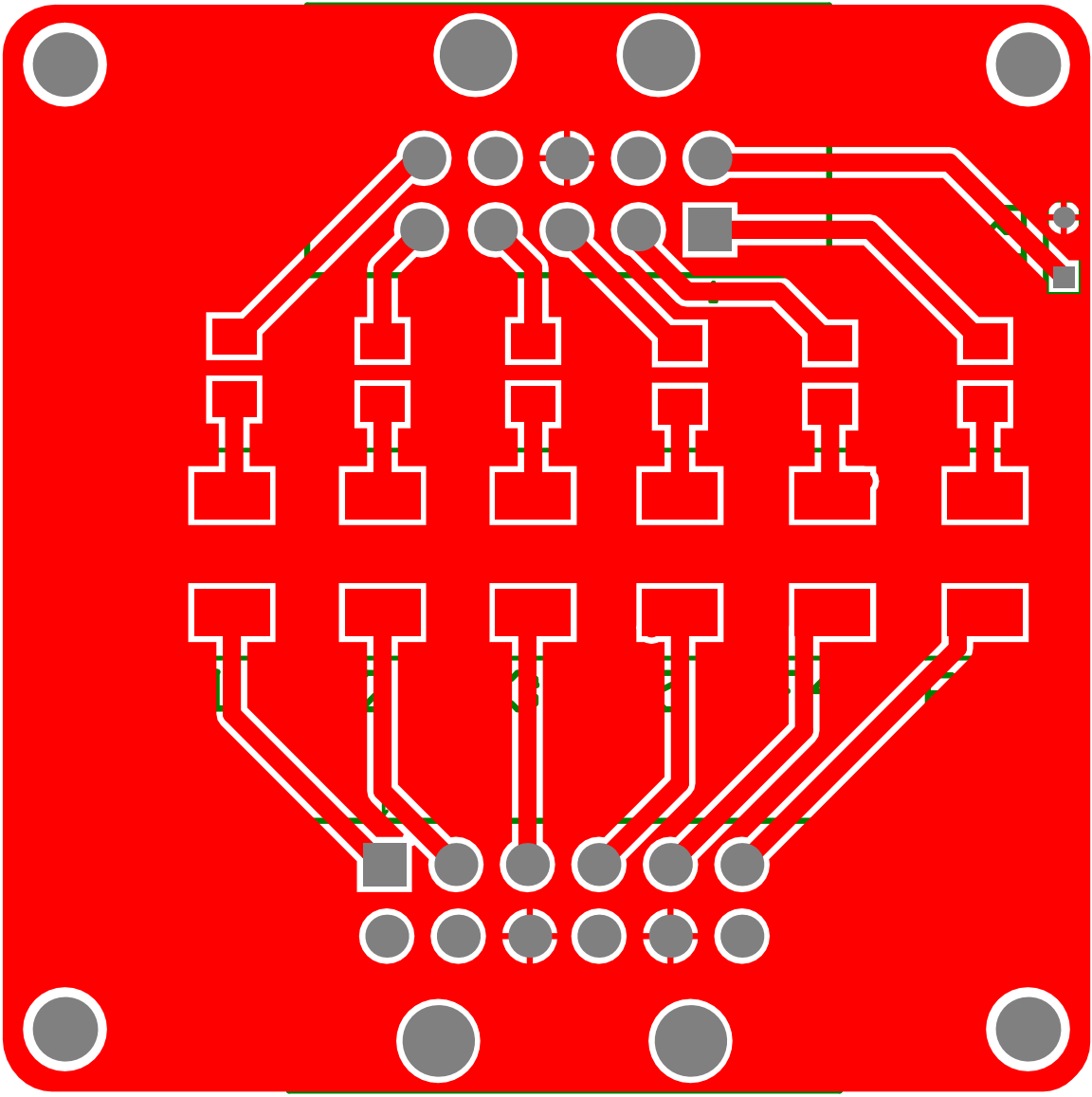
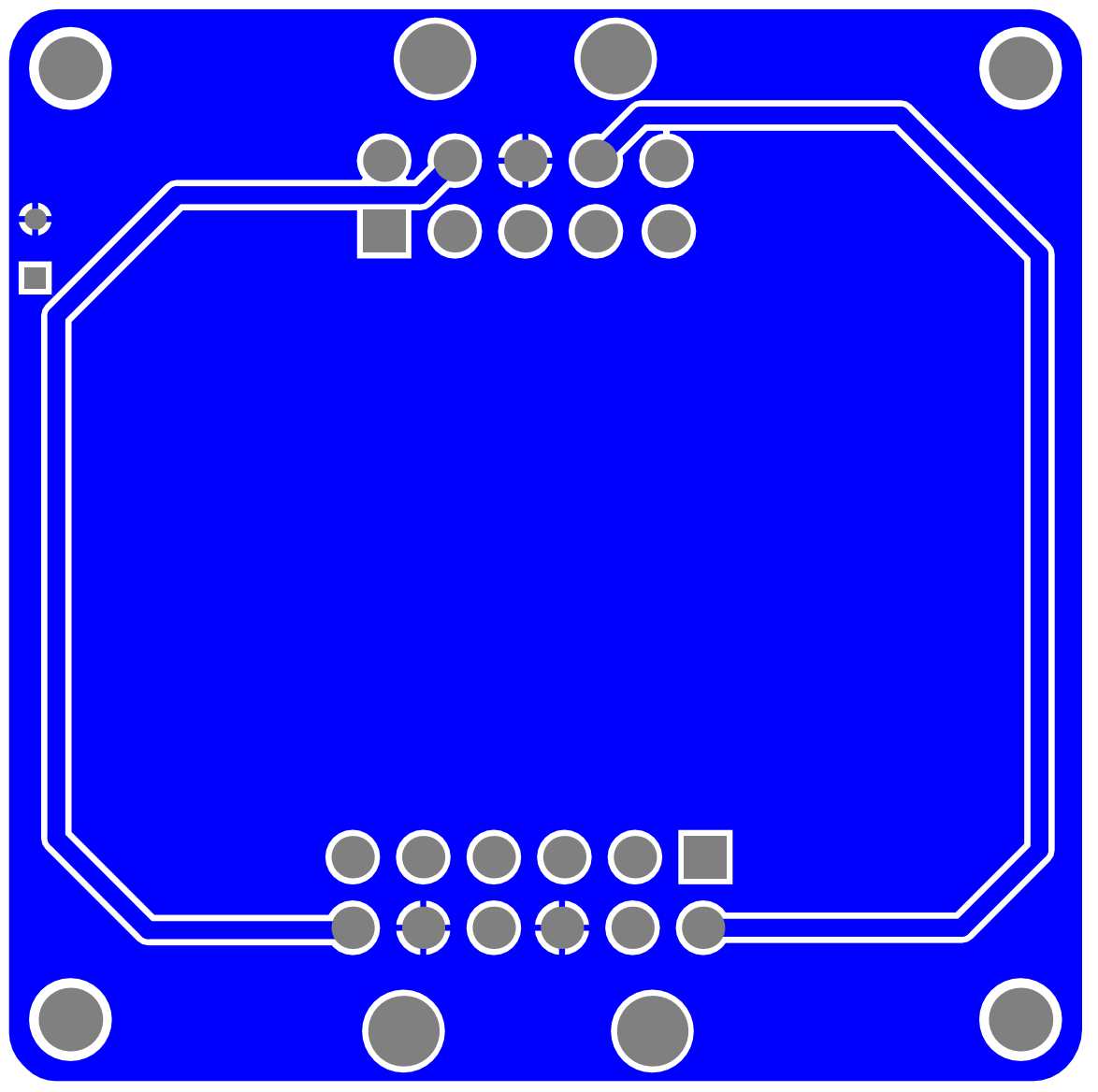


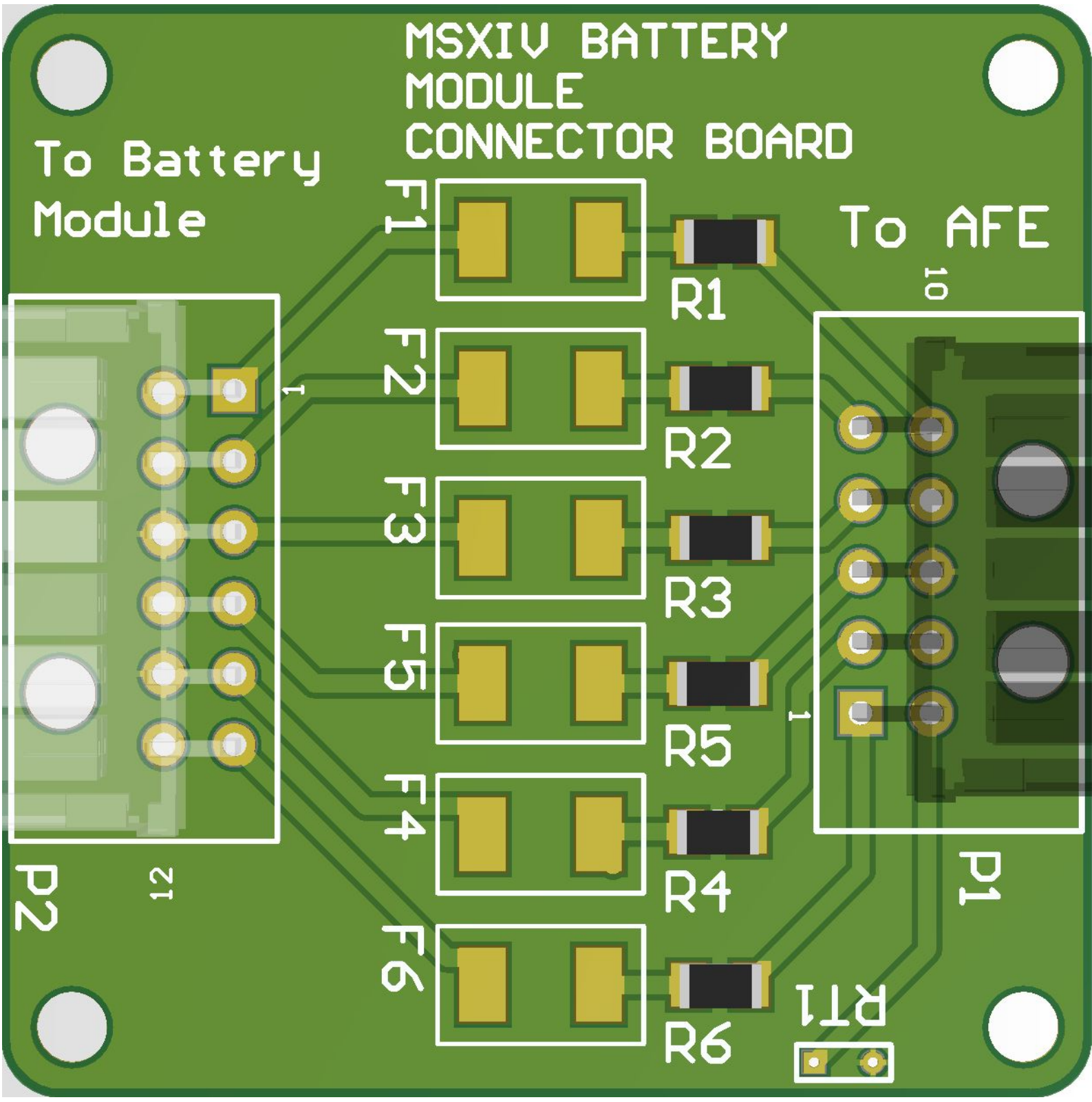


Project: *MSXIV_BatteryModuleConnectorBoard.Prj*		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Aashmika Mali		
Size: Letter	Revision: 1.0	
Date: 2019-12-01	Sheet * of *	Website: uwmidsun.com

Comment	Description	Designator	Footprint	LibRef	Quantity
500mA 250V	2410 Surface Mount Fuses RoHS	F1, F2, F3, F4, F5, F6	FUSE JFC2410-0500FS	FUSE 500MA LCSC	6
CONN 10POS MICRO-FIT R/A3mm	CONN HEADER R/A 10POS 3MM	P1	CONN, 10POS R/A Microfit	CONN 10POS MICRO-FIT R/A3mm	1
CONN 12POS HEADER R/A MICROFIT 3MM	Conn Power HDR 12 POS 3mm Solder RA Thru-Hole 12 Terminal 1 Port Micro-Fit 3.0™ Tray	P2	CONN, 12POS R/A Microfit	CONN 12POS HEADER R/A 3MM	1
RES 2 OHM 1% 1/4W 1206	2 ±1% 1/4W 1206 Chip Resistor - Surface Mount RoHS	R1, R2, R5, R6	RES 1206	RES 2 OHM 1% 1/4W 1206	4
RES 1 OHM 5% 1/4W 1206	1 ±5% 1/4W 1206 Chip Resistor - Surface Mount RoHS	R3, R4	RES 1206	RES 1 OHM 5% 1/4W 1206	2
10K NTC	NTC Thermistor 10k Bead	RT1	NTC THERMISTOR BEAD	NTC THERMISTOR 10K 1% BEAD	1






MSXIV BATTERY
MODULE
CONNECTOR BOARD
To Battery
Module
To AFE
F1
F2
F3
F5
F4
F6
R1
R2
R3
R5
R4
R6
RT1
P2
P1
1
12
10
1

Design Rules Verification Report

Filename : C:\Users\Midnight Sun\Documents\Midnight Sun\hardware\MSXIV_BatteryM

Warnings 0
Rule Violations 17

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.762mm) (Preferred=0.508mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	8
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	6
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	17

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.184mm < 0.254mm) Between Pad P1-6(30.06mm,39.48mm) on Multi-Layer And Track

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(3mm,3mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(3mm,43.4mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(43.4mm,3mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(43.4mm,43.4mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P1-(20.22mm,43.8mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P1-(27.9mm,43.8mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P2-(18.66mm,2.51mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P2-(29.24mm,2.51mm) on Multi-Layer Actual Hole Size = 3mm

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.068mm < 0.254mm) Between Text "1" (16.5mm,12.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (30.06mm,33.48mm) on Top Overlay And Track