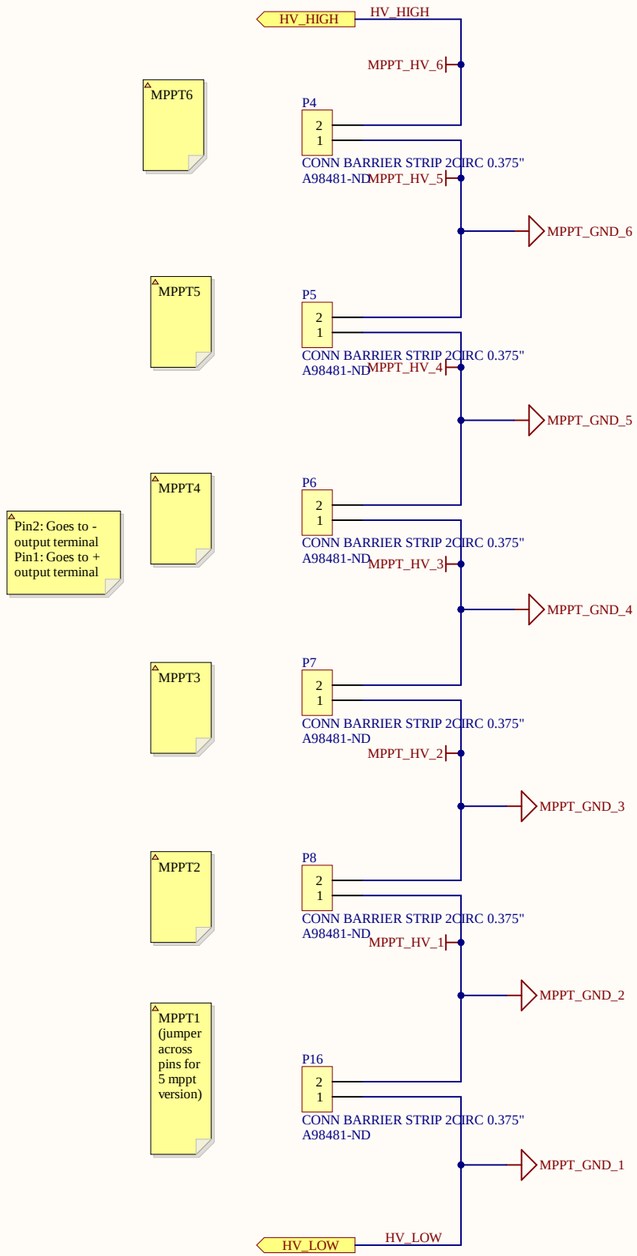
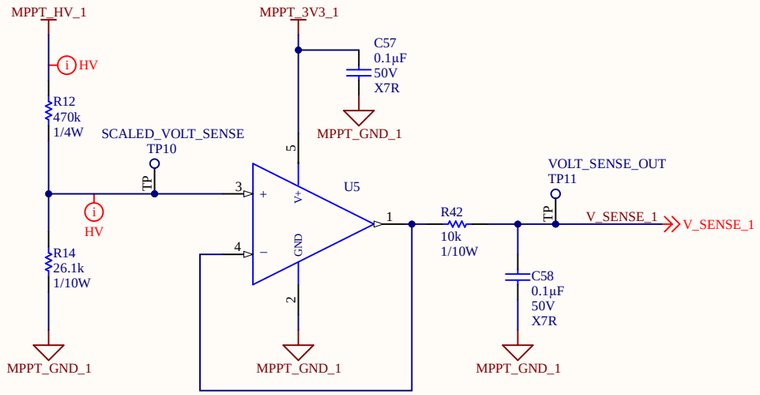
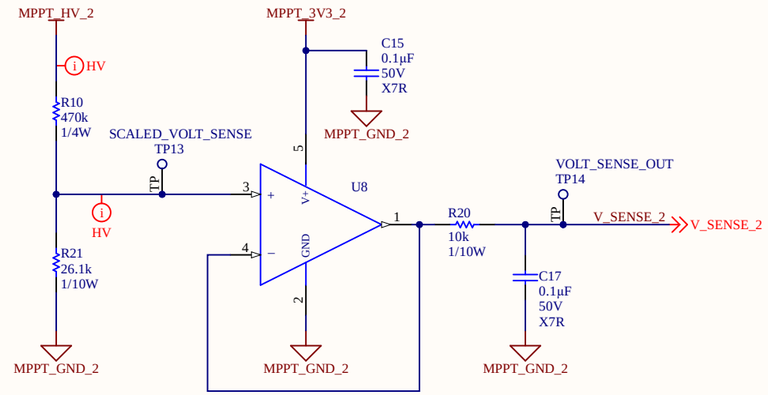
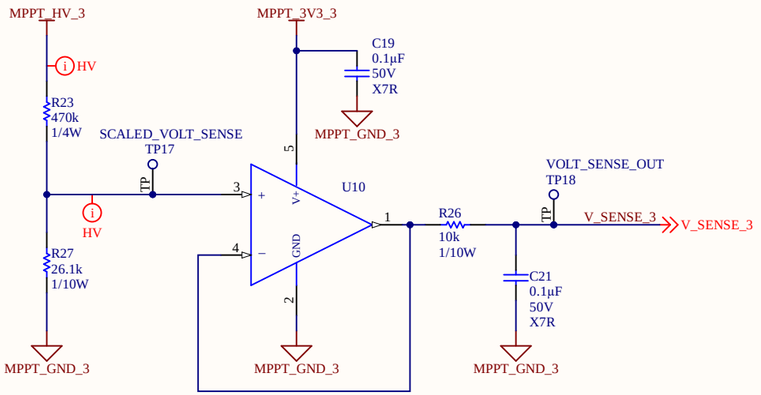
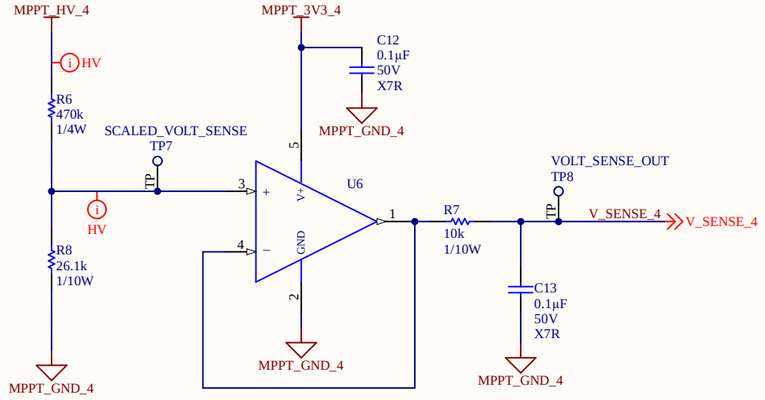
Voltage Sense

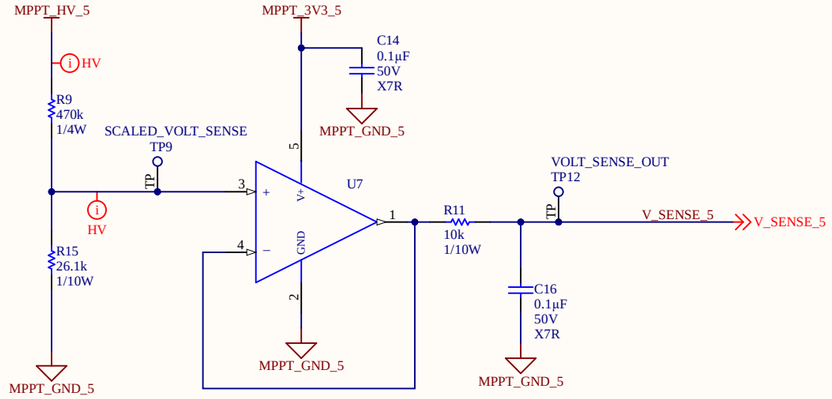


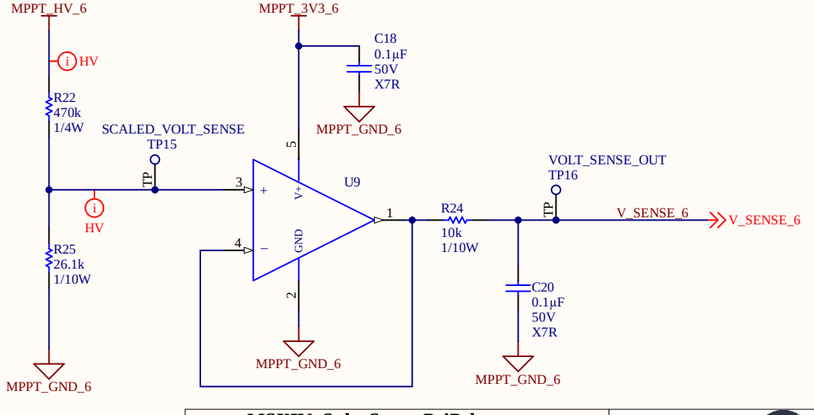




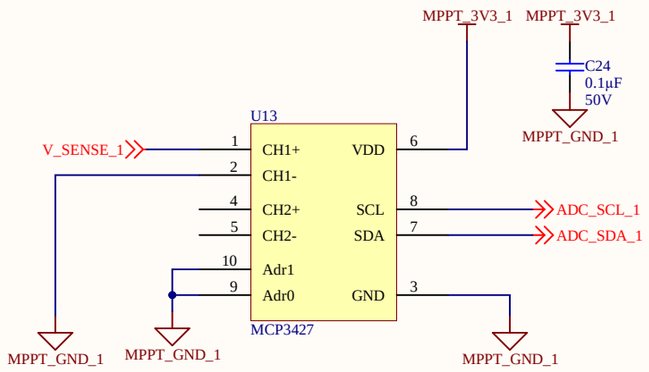


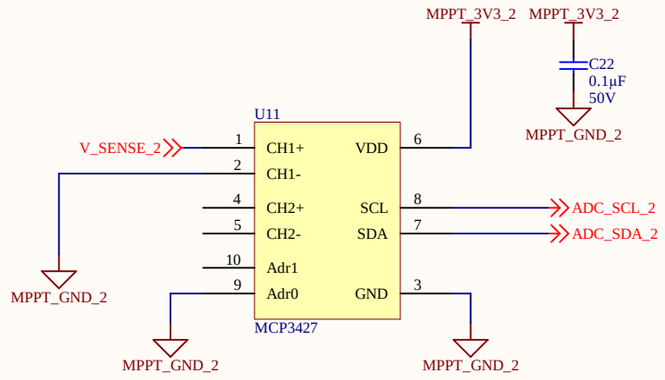


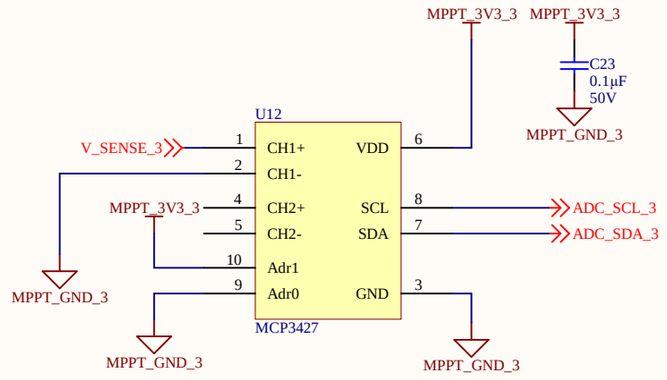




Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: **Solar Sense Slave**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Lead: *		
Size: Letter	Revision: *	
Date: 2020-02-09	Sheet 3 of 4	Website: www.uwmidsun.com

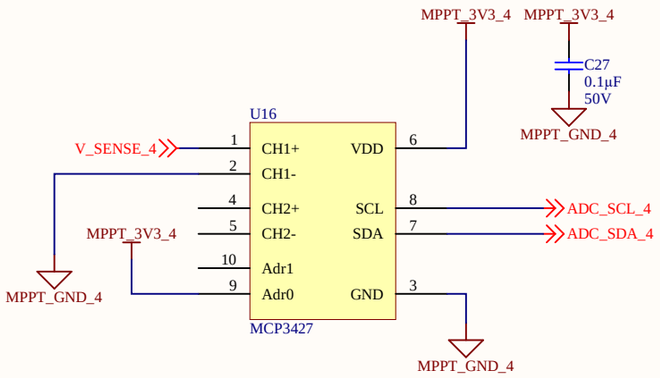


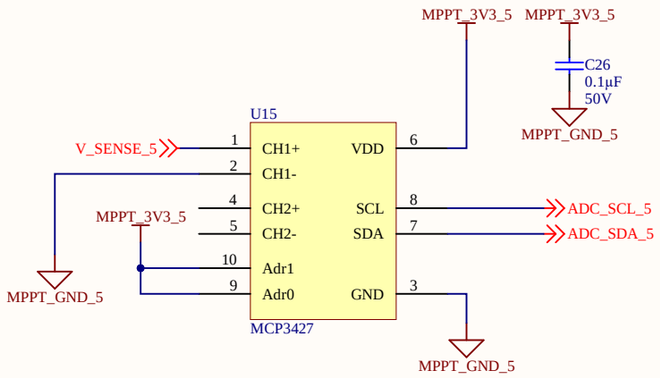


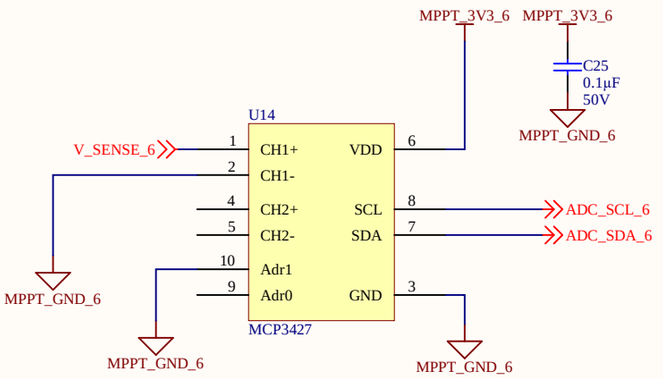


ADCs

I²C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float







Make combination of pulled high, low and floating (for address pins)

PROJECT	MSXIV_SolarSense.PrjPcb
DOCUMENT	*
PART NUMBER	
VARIANT	[No Variations]
DRAWN BY	Aashmika Mali
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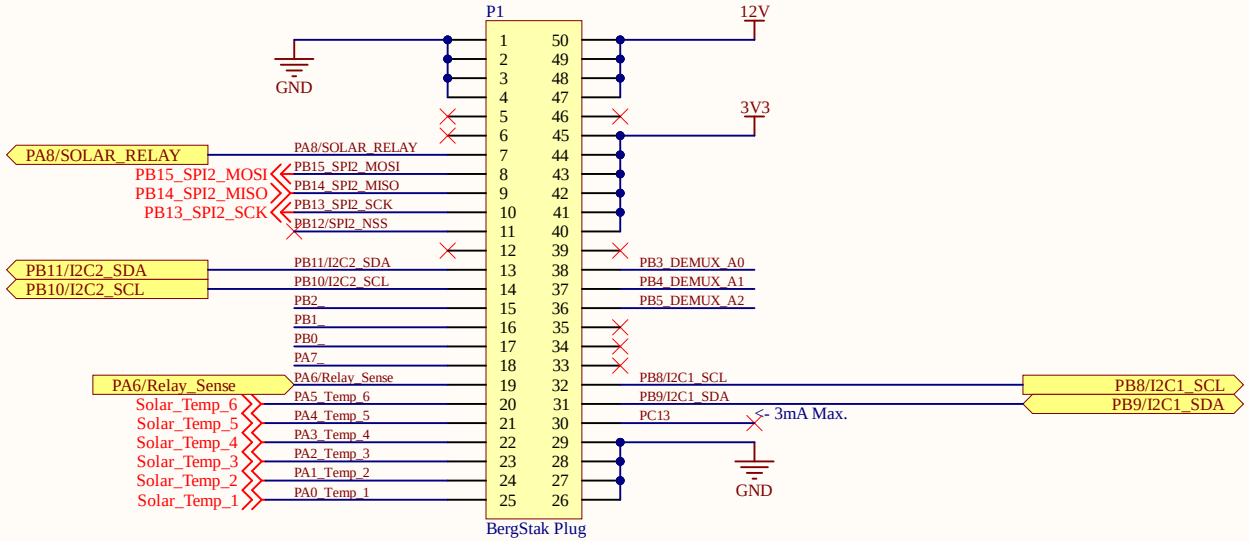
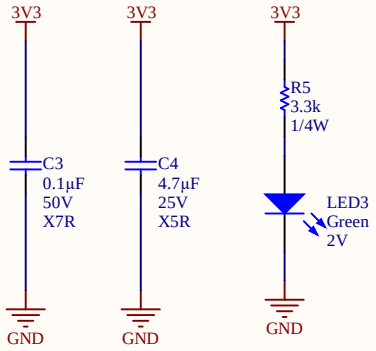
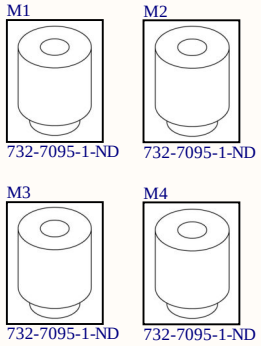
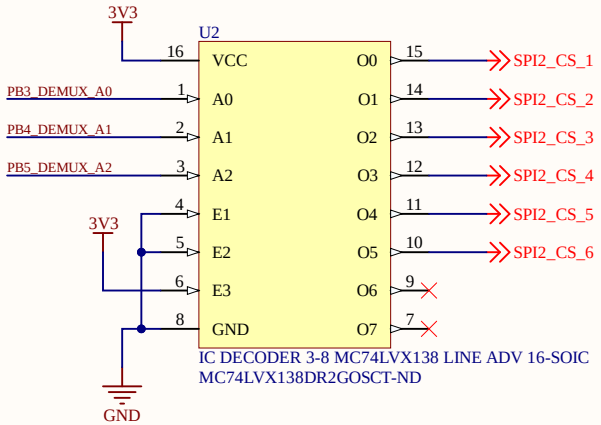
Add 6 gpio pins for slave select on spi, and 6 gpios for temperature sensing

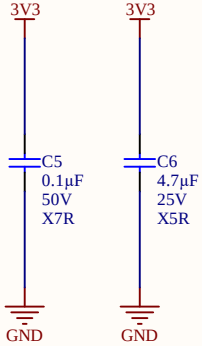




Standoffs

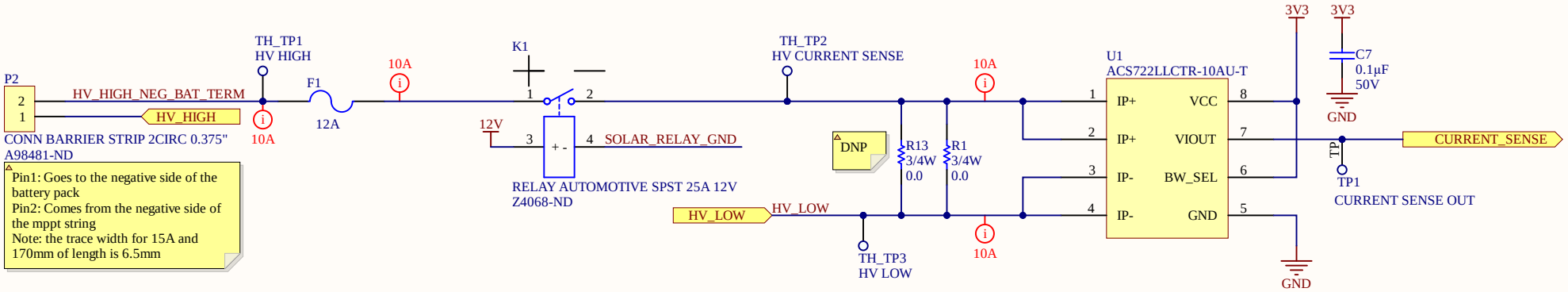


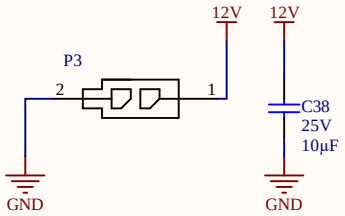


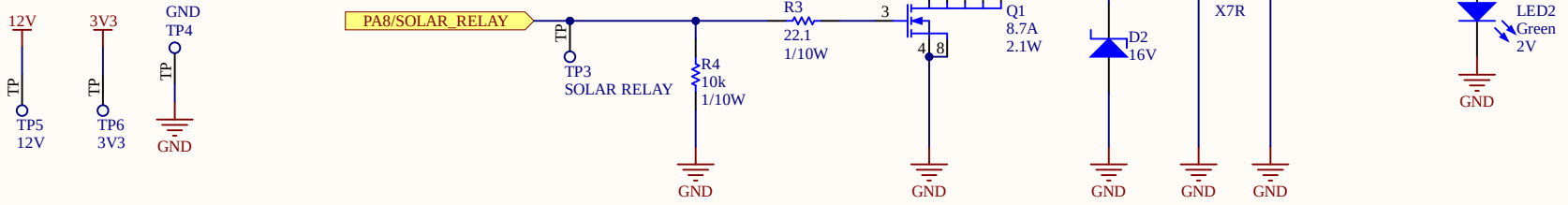


Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Aashmika Mali		
Size: Letter	Revision: 1.0	
Date: 2020-02-09	Sheet * of *	Website: www.uwmidsun.com

Passthrough - Current Sense, Fuse, and Relay







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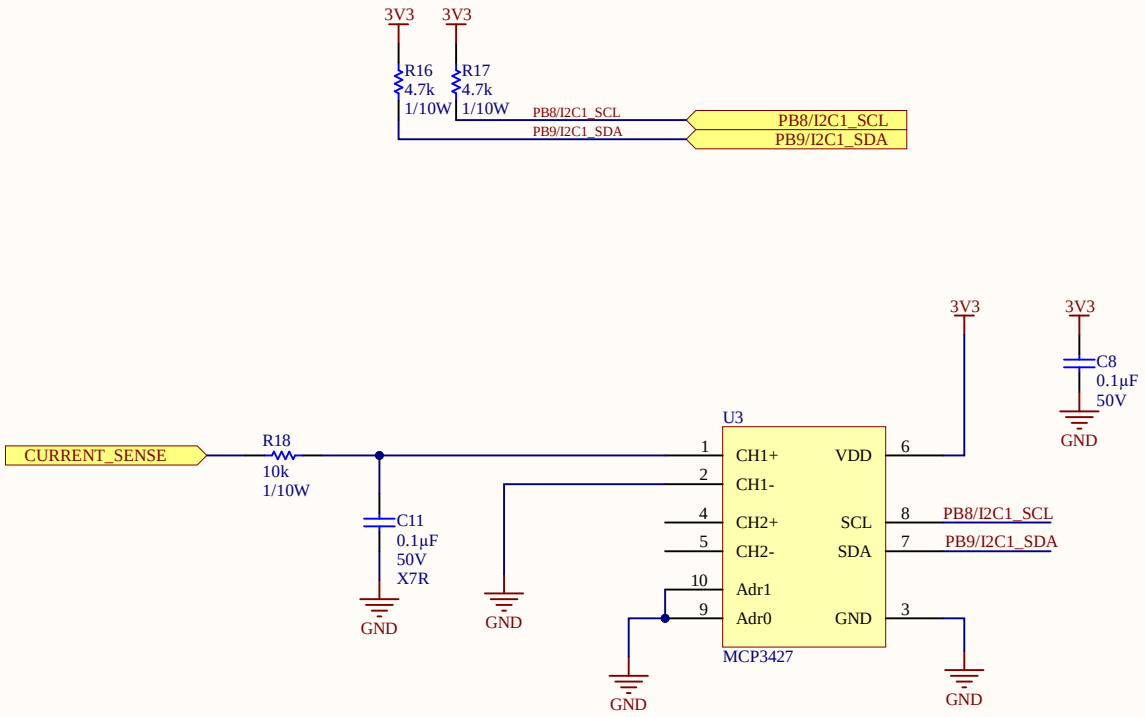
I2C Interface (for Current Sense)



Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
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Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
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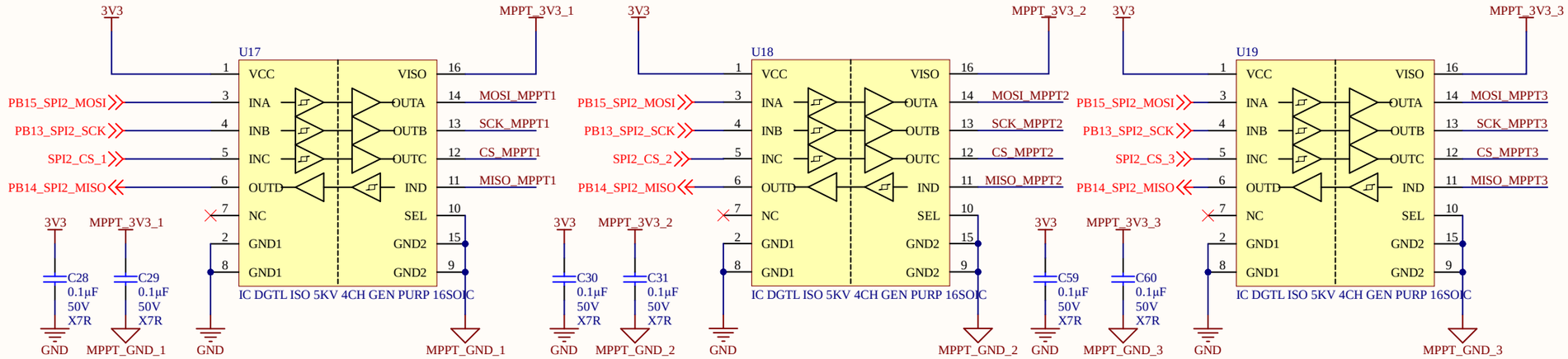
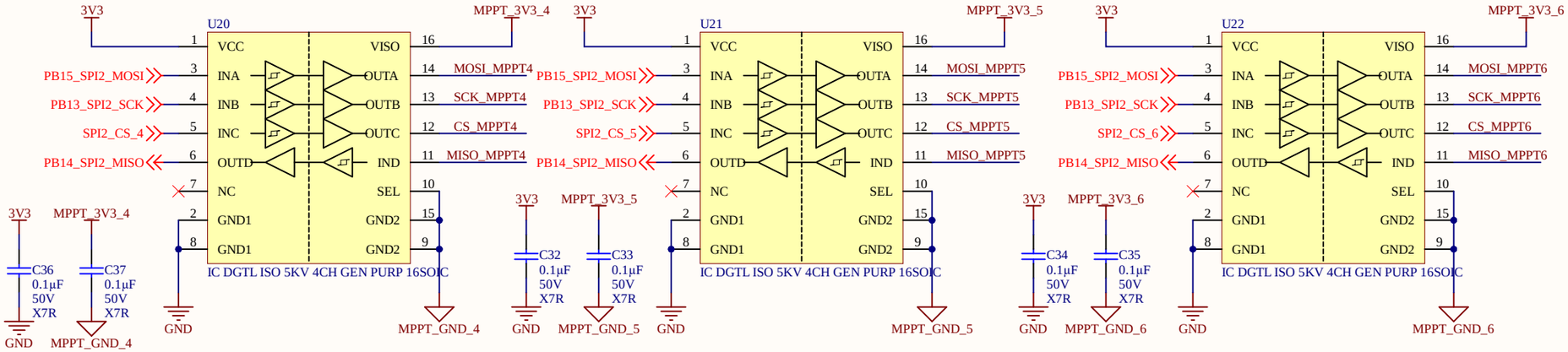
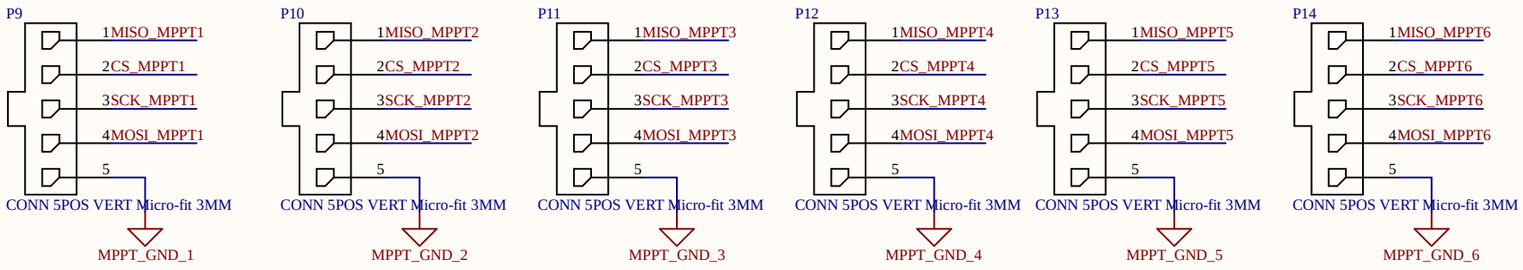
SPI Isolators







PROJECT	MSXIV_SolarSense.PrjPcb		
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
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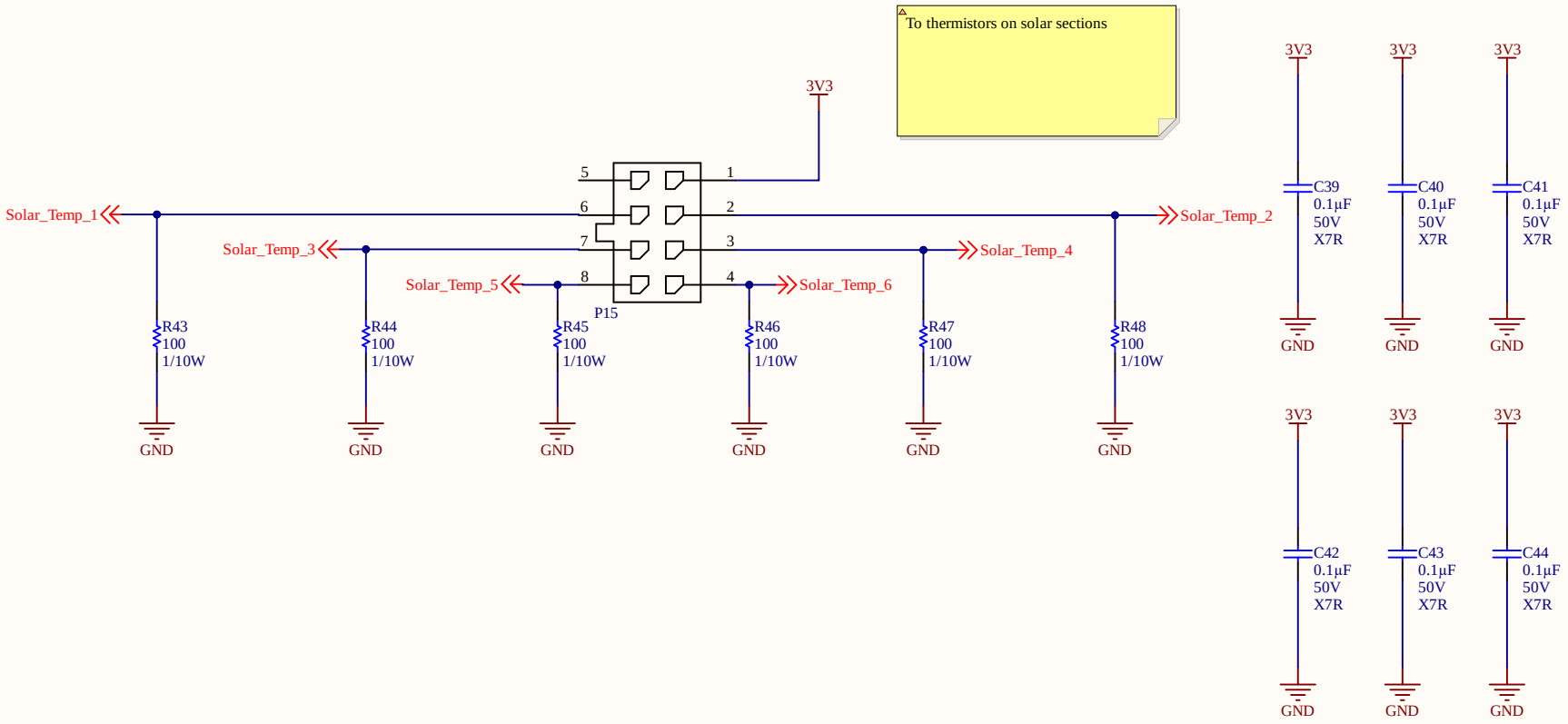
Temperature Sense for Array Sections



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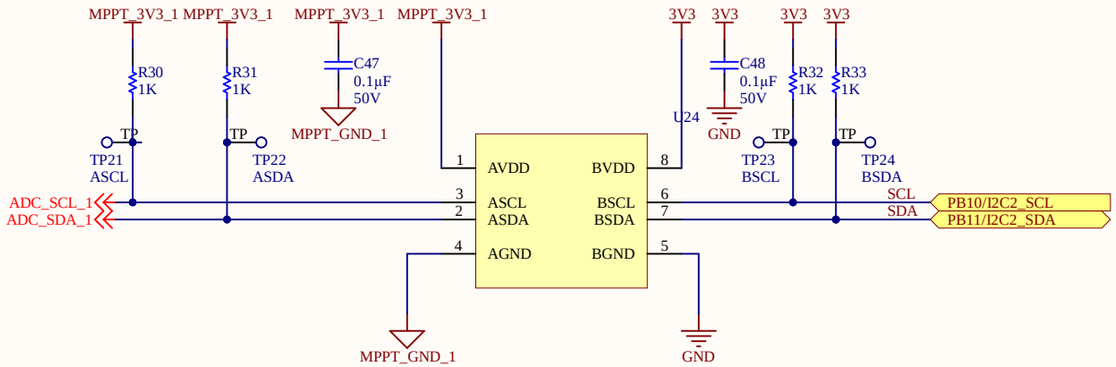
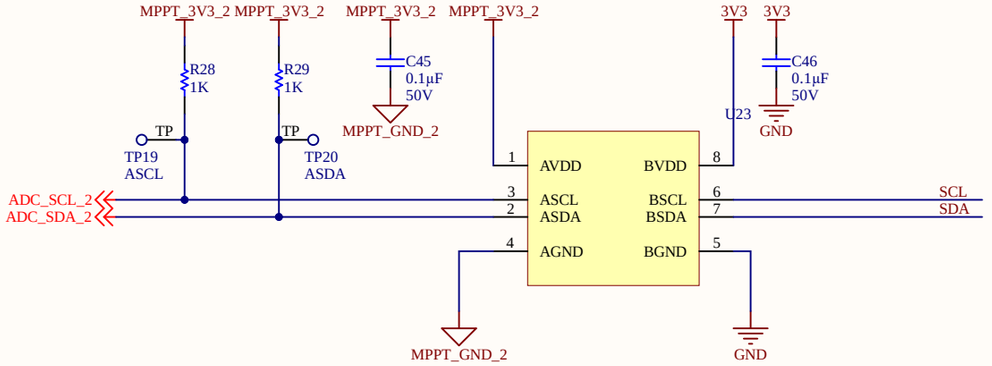
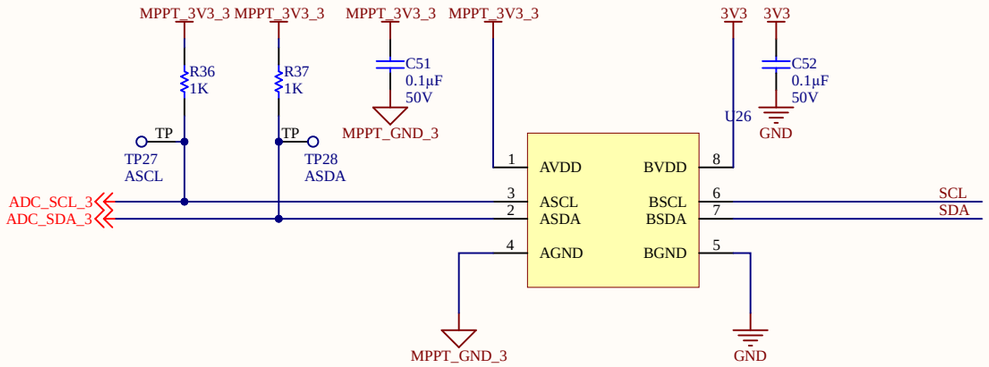
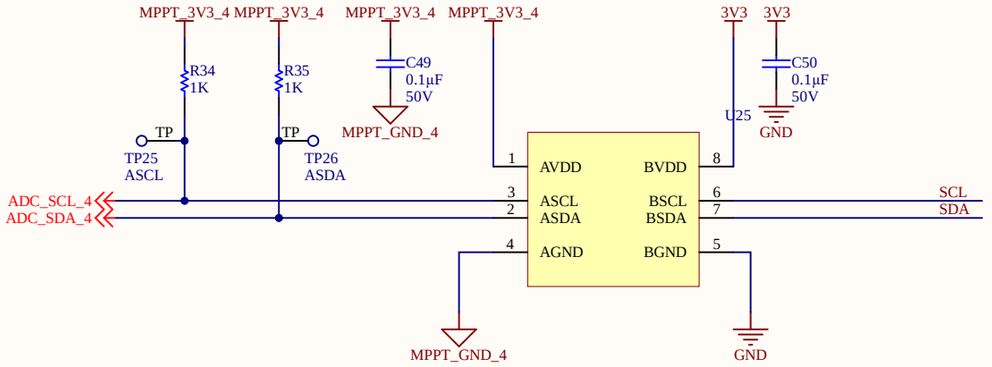
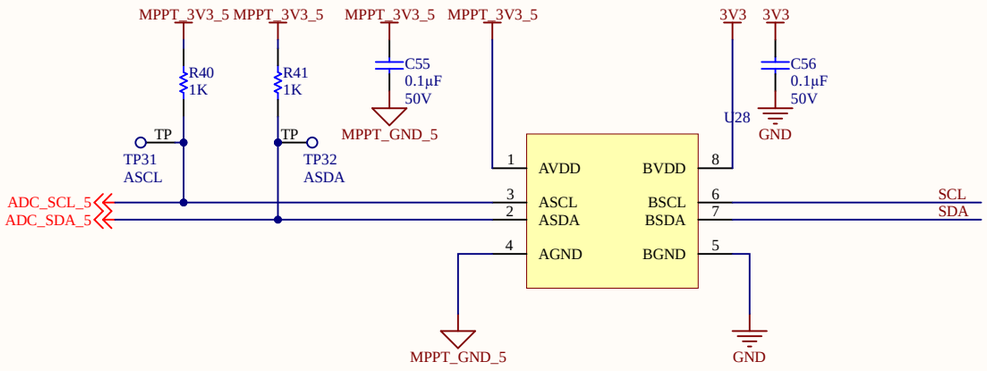
I2C Isolators for V-Sense

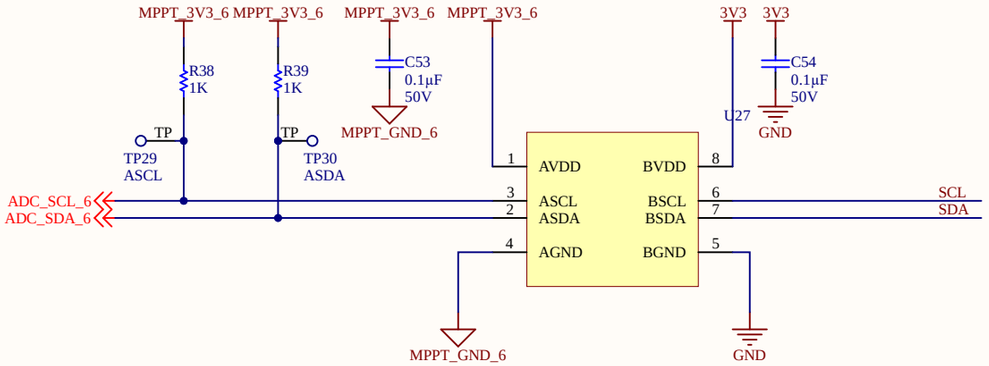












PROJECT	MSXIV_SolarSense.PrjPcb		MIDNIGHT SUN
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-09	SHEET	* OF *

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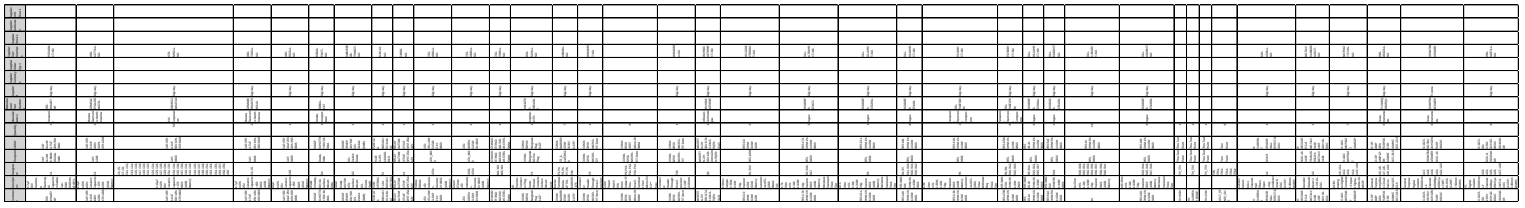

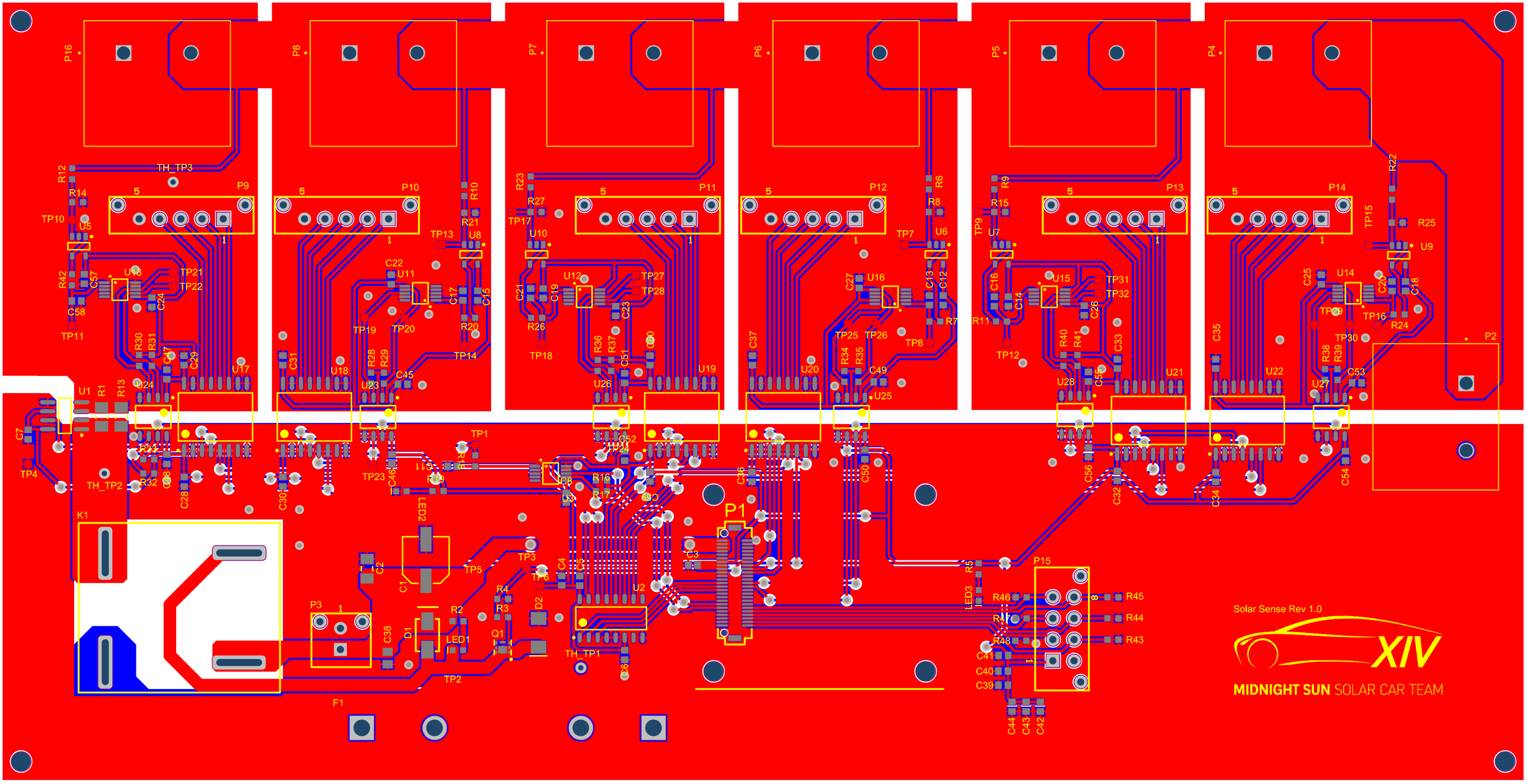
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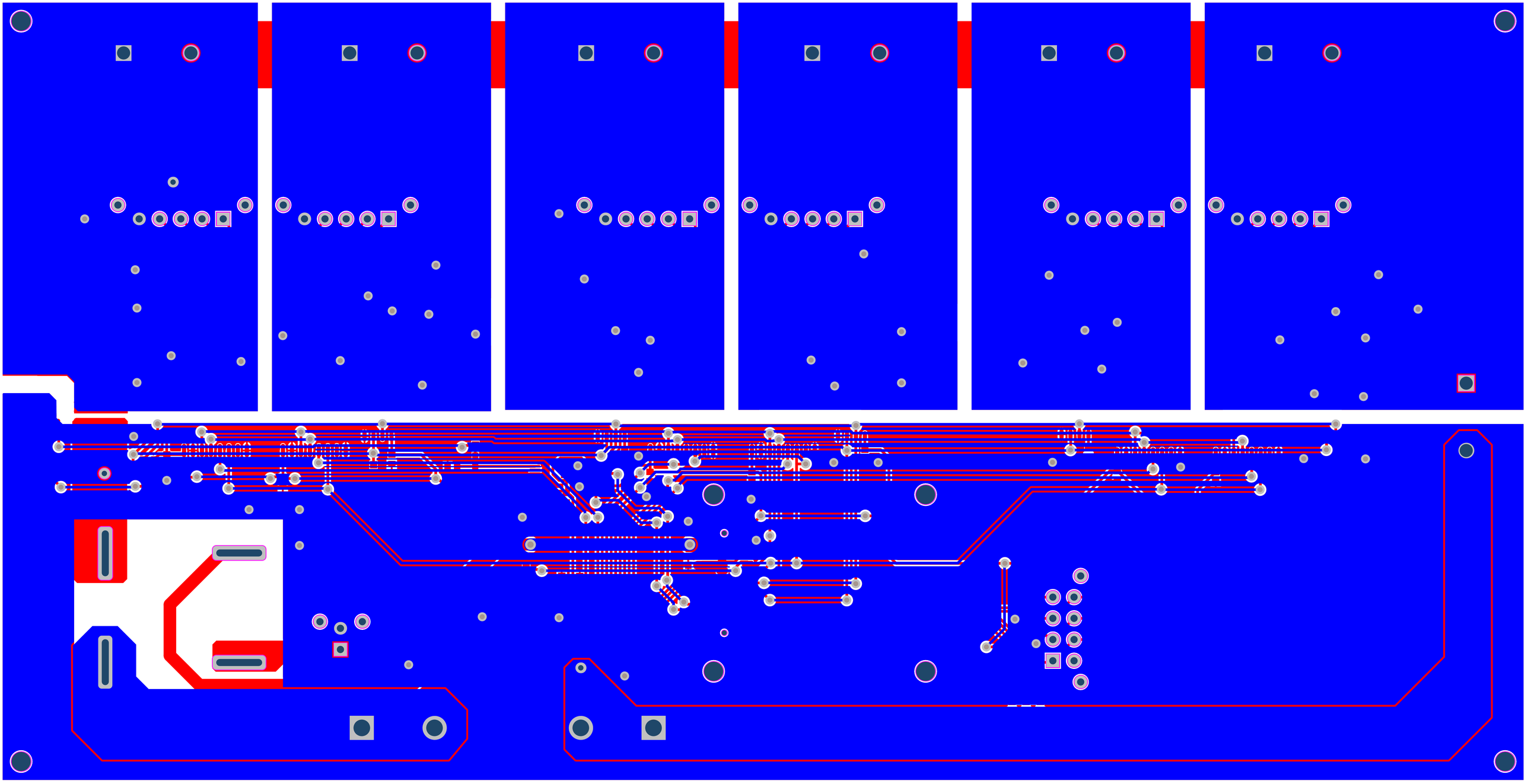
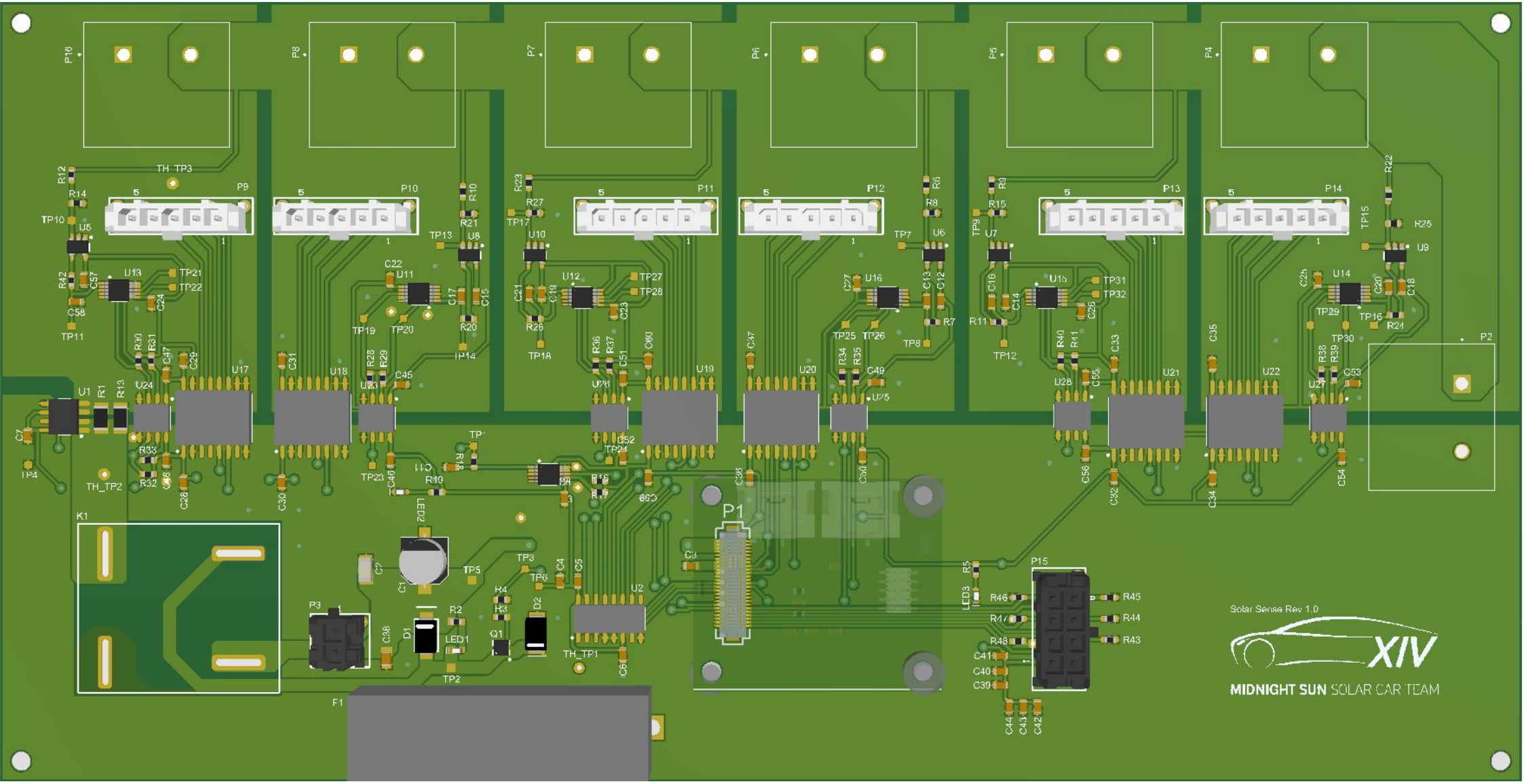
XIV
MIDNIGHT SUN SOLAR CAR TEAM




Solar Sense Rev 1.0
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Electrical Rules Check Report

Class	Document	Message
Error	Voltage_Sense.SchDoc	HV_LOW contains Power Pin and Output Port objects (Pin U5-2, Port HV_LOW).
Error	Controller_Board_Interface.SchDoc	Net PA6/Relay_Sense has only one pin (Pin P1-19)
Error	Controller_Board_Interface.SchDoc	Net PA7_ has only one pin (Pin P1-18)
Error	Controller_Board_Interface.SchDoc	Net PB0_ has only one pin (Pin P1-17)
Error	Controller_Board_Interface.SchDoc	Net PB1_ has only one pin (Pin P1-16)
Error	Controller_Board_Interface.SchDoc	Net PB2_ has only one pin (Pin P1-15)
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_GND_1 at 3650mil,1830mil has been reduced to local level by presence of port at 2000mil,1300mil
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_HV_6 at 3350mil,9100mil has been reduced to local level by presence of port at 2000mil,9400mil
Warning	Voltage_Sense.SchDoc	Net NetR6_2 has no driving source (Pin R6-2, Pin R8-1, Pin TP7-TP, Pin U6-3)
Warning	Voltage_Sense.SchDoc	Net NetR9_2 has no driving source (Pin R9-2, Pin R15-1, Pin TP9-TP, Pin U7-3)
Warning	Voltage_Sense.SchDoc	Net NetR10_2 has no driving source (Pin R10-2, Pin R21-1, Pin TP13-TP, Pin U8-3)
Warning	Voltage_Sense.SchDoc	Net NetR12_2 has no driving source (Pin R12-2, Pin R14-1, Pin TP10-TP, Pin U5-3)
Warning	Voltage_Sense.SchDoc	Net NetR22_2 has no driving source (Pin R22-2, Pin R25-1, Pin TP15-TP, Pin U9-3)
Warning	Voltage_Sense.SchDoc	Net NetR23_2 has no driving source (Pin R23-2, Pin R27-1, Pin TP17-TP, Pin U10-3)
Warning	Controller_Board_Interface.SchDoc	Net PB3_DEMUX_A0 has no driving source (Pin P1-38, Pin U2-1)
Warning	Controller_Board_Interface.SchDoc	Net PB4_DEMUX_A1 has no driving source (Pin P1-37, Pin U2-2)
Warning	Controller_Board_Interface.SchDoc	Net PB5_DEMUX_A2 has no driving source (Pin P1-36, Pin U2-3)
Warning	Current_and_Relay_Sense.SchDoc	Nets Wire HV_HIGH has multiple names (Net Label HV_HIGH, Power Object MPPT_HV_6, Power Object MPPT_HV_6)
Warning	ADCs.SchDoc	Nets Wire HV_LOW has multiple names (Net Label HV_LOW, Net Label HV_LOW, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_2 has multiple names (Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_HV_1, Power Object MPPT_HV_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_3 has multiple names (Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_HV_2, Power Object MPPT_HV_2)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_4 has multiple names (Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_HV_3, Power Object MPPT_HV_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_5 has multiple names (Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_HV_4, Power Object MPPT_HV_4)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_6 has multiple names (Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_HV_5, Power Object MPPT_HV_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA0_Temp_1 has multiple names (Cross-Sheet Connector Solar_Temp_1, Cross-Sheet Connector Solar_Temp_1, Net Label PA0_Temp_1)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA1_Temp_2 has multiple names (Cross-Sheet Connector Solar_Temp_2, Cross-Sheet Connector Solar_Temp_2, Net Label PA1_Temp_2)

Class	Document	Message
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA2_Temp_3 has multiple names (Cross-Sheet Connector Solar_Temp_3, Cross-Sheet Connector Solar_Temp_3, Net Label PA2_Temp_3)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA3_Temp_4 has multiple names (Cross-Sheet Connector Solar_Temp_4, Cross-Sheet Connector Solar_Temp_4, Net Label PA3_Temp_4)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA4_Temp_5 has multiple names (Cross-Sheet Connector Solar_Temp_5, Cross-Sheet Connector Solar_Temp_5, Net Label PA4_Temp_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA5_Temp_6 has multiple names (Cross-Sheet Connector Solar_Temp_6, Cross-Sheet Connector Solar_Temp_6, Net Label PA5_Temp_6)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB10/I2C2_SCL has multiple names (Net Label PB10/I2C2_SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB11/I2C2_SDA has multiple names (Net Label PB11/I2C2_SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA)
Warning	ADCs.SchDoc	Off grid C24 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SCL_1 at 3600mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SDA_1 at 3600mil,7544.41mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB13_SPI2_SCK at 6574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB14_SPI2_MISO at 6574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB15_SPI2_MOSI at 6574.41mil,6851.811mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_2 at 7837.008mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_4 at 6687.008mil,4596.063mil
Warning	Controller_Board_Interface.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 2247.008mil,4300mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 5650mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_1 at 1350mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_2 at 6281.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_3 at 11381.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_4 at 1631.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_5 at 6531.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_6 at 11231.89mil,3400mil
Warning	Controller_Board_Interface.SchDoc	Off grid M1 at 1693.983mil,2899.713mil
Warning	Controller_Board_Interface.SchDoc	Off grid M2 at 2406.601mil,2898.306mil
Warning	Controller_Board_Interface.SchDoc	Off grid M3 at 1693.983mil,1949.714mil
Warning	Controller_Board_Interface.SchDoc	Off grid M4 at 2406.601mil,1948.306mil
Warning	SPI_Interface.SchDoc	Off grid Net Label CS_MPPT2 at 8674.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT2 at 8624.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT3 at 12055.512mil,6250mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT2 at 8674.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT3 at 12055.512mil,6850mil
Warning	SPI_Interface.SchDoc	Off grid Net Label SCK_MPPT2 at 8674.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid No ERC at 6774.41mil,6051.811mil
Warning	TemperatureSense.SchDoc	Off grid P15 at 4521.654mil,5096.063mil
Warning	ADCs.SchDoc	Off grid Pin C24-1 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Pin C24-2 at 3818.11mil,8374.41mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-1 at 5421.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-2 at 5421.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-3 at 5421.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-4 at 5421.654mil,4396.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-5 at 4521.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-6 at 4521.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-7 at 4521.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-8 at 4521.654mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Pin U13-1 at 1658.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-2 at 1658.11mil,7894.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-3 at 3108.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil

Class	Document	Message
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-8 at 6774.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-9 at 8574.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-10 at 8574.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_

Warnings 0
Rule Violations 127

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=70mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	12
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	27
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	77
Silk to Silk (Clearance=10mil) (All),(All)	11
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	127

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,4242.299mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-3346.457mil,1604.504mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-3346.457mil,620.252mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4527.559mil,1604.504mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4527.559mil,620.252mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-8385.827mil,117.961mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-8385.827mil,4242.299mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (255.905mil > 100mil) Pad K1-1(-7916.969mil,671.433mil) on Multi-Layer Actual Slot Hole Height = 255.905mi
Hole Size Constraint: (255.905mil > 100mil) Pad K1-2(-7916.969mil,1277.732mil) on Multi-Layer Actual Slot Hole Height = 255.905mi
Hole Size Constraint: (255.905mil > 100mil) Pad K1-3(-7170.906mil,669.465mil) on Multi-Layer Actual Slot Hole Height = 255.905mi
Hole Size Constraint: (255.905mil > 100mil) Pad K1-4(-7170.906mil,1279.701mil) on Multi-Layer Actual Slot Hole Height = 255.905mi

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-4409.449mil,1419.464mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-4409.449mil,805.291mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.842mil < 10mil) Between Pad Q1-1(-5666.198mil,727.228mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad Q1-2(-5666.198mil,752.819mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad Q1-3(-5666.198mil,778.409mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (7.945mil < 10mil) Between Pad Q1-3(-5666.198mil,778.409mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad Q1-4(-5739.032mil,778.409mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad Q1-4(-5739.032mil,778.409mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (7.945mil < 10mil) Between Pad Q1-4(-5739.032mil,778.409mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (1.842mil < 10mil) Between Pad Q1-5(-5739.032mil,752.819mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (7.354mil < 10mil) Between Pad Q1-7(-5702.615mil,741.008mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (7.669mil < 10mil) Between Pad R13-1(-7827.756mil,1985.409mil) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (4.559mil < 10mil) Between Pad R48-1(-2785.591mil,790.501mil) on Top Layer And Via (-2731.3mil,774.74mil)
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U10-1(-5476.378mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U10-2(-5513.78mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.631mil < 10mil) Between Pad U3-10(-5349.269mil,1761.984mil) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (5.935mil < 10mil) Between Pad U3-9(-5349.269mil,1742.299mil) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U5-1(-8026.969mil,3042.732mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U5-2(-8064.37mil,3042.732mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U6-1(-3250mil,2997.22mil) on Top Layer And Pad U6-2(-3287.402mil,2997.22mil)
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U6-2(-3287.402mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U7-1(-2884.843mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U7-2(-2922.244mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U8-1(-5842.323mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U8-2(-5879.725mil,2997.22mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U9-1(-673.229mil,2992.299mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U9-2(-710.63mil,2992.299mil) on Top Layer And Pac

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-6130.938mil,1124.268mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-6130.938mil,1124.268mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C11-1(-5956.356mil,1761.984mil) on Top Layer And Text "R18'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-6130.938mil,1356.551mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-6130.938mil,1356.551mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.995mil < 10mil) Between Pad C15-1(-5842.323mil,2739.74mil) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (7.941mil < 10mil) Between Pad C15-2(-5842.323mil,2686.59mil) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C52-1(-5023.425mil,1847.614mil) on Top Layer And Text "TP24'
Silk To Solder Mask Clearance Constraint: (9.475mil < 10mil) Between Pad C6-2(-5023.425mil,685.213mil) on Top Layer And Text "C6'
Silk To Solder Mask Clearance Constraint: (9.655mil < 10mil) Between Pad C7-1(-8346.457mil,1965.724mil) on Top Layer And Text "C7'
Silk To Solder Mask Clearance Constraint: (9.7mil < 10mil) Between Pad C7-2(-8346.457mil,1912.575mil) on Top Layer And Text "C7'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C8-1(-5349.269mil,1613.984mil) on Top Layer And Text "U3'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C8-2(-5349.269mil,1560.835mil) on Top Layer And Text "U3'
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D1-1(-6122.047mil,741.992mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D1-1(-6122.047mil,741.992mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D1-2(-6122.047mil,899.472mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D1-2(-6122.047mil,899.472mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.724mil < 10mil) Between Pad D2-2(-5502.812mil,755.002mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED1-2(-5982.284mil,738.363mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED2-2(-6296.634mil,1624.189mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(-3051.181mil,1013.953mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P10-0(-6216.536mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-6216.536mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P10-0(-6925.197mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-6925.197mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.78mil < 10mil) Between Pad P1-1(-4338.583mil,1348.597mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P11-0(-4539.37mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-4539.37mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P11-0(-5248.032mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-5248.032mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P12-0(-3618.11mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-3618.11mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P12-0(-4326.772mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-4326.772mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.767mil < 10mil) Between Pad P1-25(-4338.583mil,876.157mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.4mil < 10mil) Between Pad P1-26(-4480.315mil,876.157mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P13-0(-1937.992mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-1937.992mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P13-0(-2646.654mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-2646.654mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-1019.685mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P14-0(-1019.685mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P14-0(-1728.347mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-1728.347mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-2482.677mil,1151.748mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.918mil < 10mil) Between Pad P15-0(-2482.677mil,1151.748mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-2482.677mil,561.197mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.376mil < 10mil) Between Pad P15-0(-2482.677mil,561.197mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.401mil < 10mil) Between Pad P1-50(-4480.315mil,1348.597mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P3-0(-6484.827mil,897.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-6484.827mil,897.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P3-0(-6721.048mil,897.11mil) on Multi-Layer And Track

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-6721.048mil,897.11mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P9-0(-7137.795mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-7137.795mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P9-0(-7846.457mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-7846.457mil,3217.89mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (1.969mil < 10mil) Between Pad Q1-1(-5666.198mil,727.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (4.415mil < 10mil) Between Pad Q1-2(-5666.198mil,752.819mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (4.415mil < 10mil) Between Pad Q1-2(-5666.198mil,752.819mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (1.969mil < 10mil) Between Pad Q1-3(-5666.198mil,778.409mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (1.969mil < 10mil) Between Pad Q1-4(-5739.032mil,778.409mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (4.415mil < 10mil) Between Pad Q1-5(-5739.032mil,752.819mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (4.415mil < 10mil) Between Pad Q1-5(-5739.032mil,752.819mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (1.969mil < 10mil) Between Pad Q1-6(-5739.032mil,727.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.68mil < 10mil) Between Pad R16-1(-5121.654mil,1624.189mil) on Top Layer And Text "R17'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R16-2(-5182.677mil,1624.189mil) on Top Layer And Text "R17'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R17-1(-5121.654mil,1683.244mil) on Top Layer And Text "R16'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R17-2(-5182.677mil,1683.244mil) on Top Layer And Text "R16'
Silk To Solder Mask Clearance Constraint: (2.51mil < 10mil) Between Pad R28-2(-6437.008mil,2223.598mil) on Top Layer And Text "U23'
Silk To Solder Mask Clearance Constraint: (9.584mil < 10mil) Between Pad R38-2(-1122.047mil,2243.283mil) on Top Layer And Text "U27'
Silk To Solder Mask Clearance Constraint: (9.791mil < 10mil) Between Pad U13-1(-7922.111mil,2785.606mil) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (9.797mil < 10mil) Between Pad U13-2(-7922.111mil,2765.921mil) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (9.965mil < 10mil) Between Pad U26-7(-5073.425mil,1930.291mil) on Top Layer And Text "C52'
Silk To Solder Mask Clearance Constraint: (9.921mil < 10mil) Between Pad U26-8(-5023.425mil,1930.291mil) on Top Layer And Text "C52'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad U3-6(-5349.269mil,1683.244mil) on Top Layer And Text "C8'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad U3-7(-5349.269mil,1702.929mil) on Top Layer And Text "C8'

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (-2783.465mil,683.244mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (3.858mil < 10mil) Between Text "1" (-6610.811mil,954.591mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-1633.858mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-2552.165mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-4232.283mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-5153.543mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-6830.709mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-7751.968mil,3279.307mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (-2421.26mil,1041.512mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (6.423mil < 10mil) Between Text "C46" (-6299.695mil,1650.657mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.714mil < 10mil) Between Text "C8" (-5379.536mil,1662mil) on Top Overlay And Track