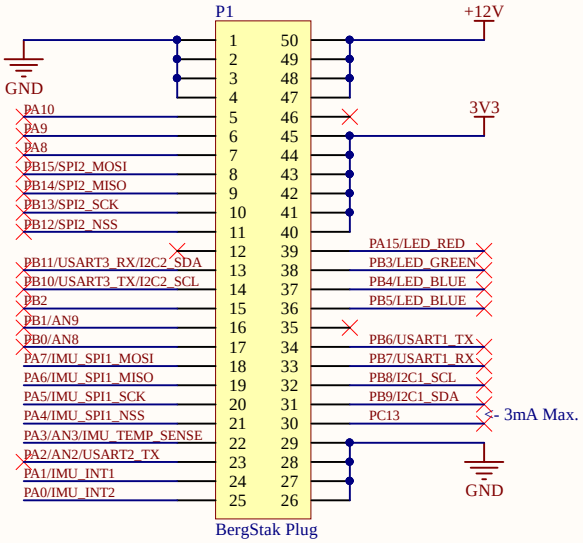
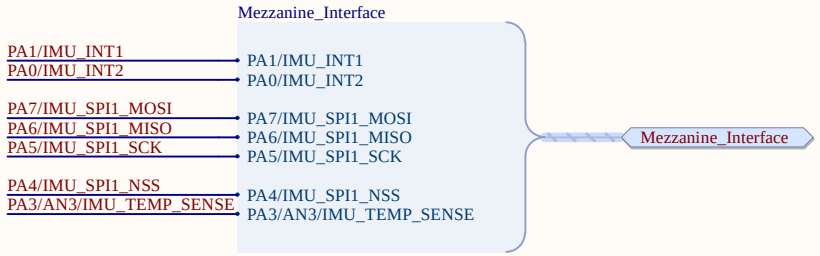
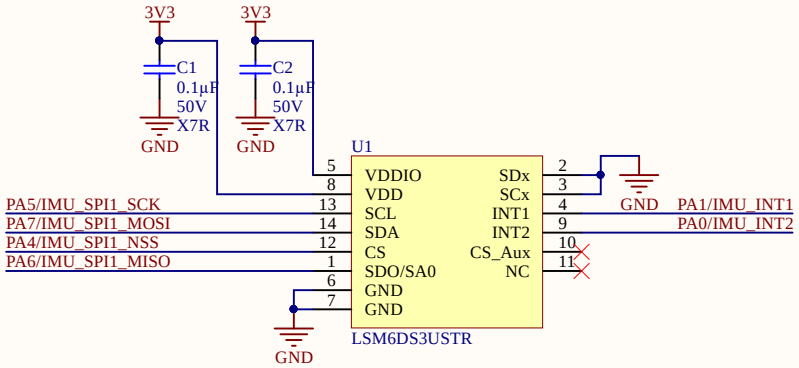
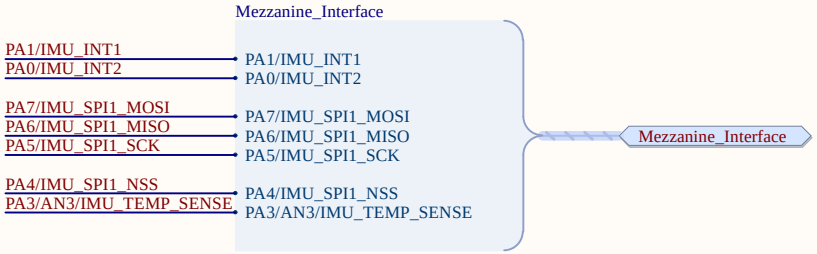




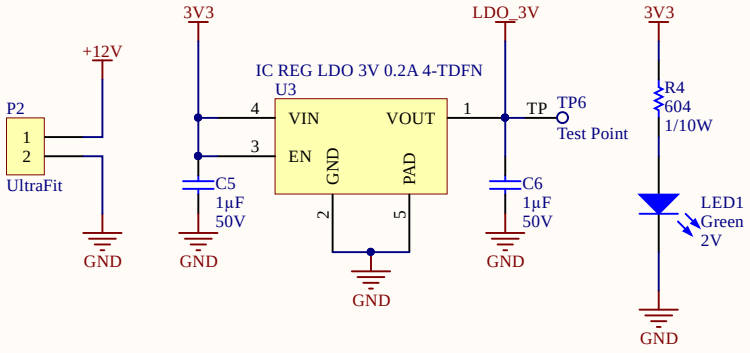
Project: ***IMU_Board.PrjPcb***		MIDNIGHT SUN
Title: **IMU Controller Board Interface**		
Project Lead: George Mardari		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.7	
Date: 2018-02-27	Sheet 1 of 2	Website: www.uwmidsun.com

Inertial Measurement Unit

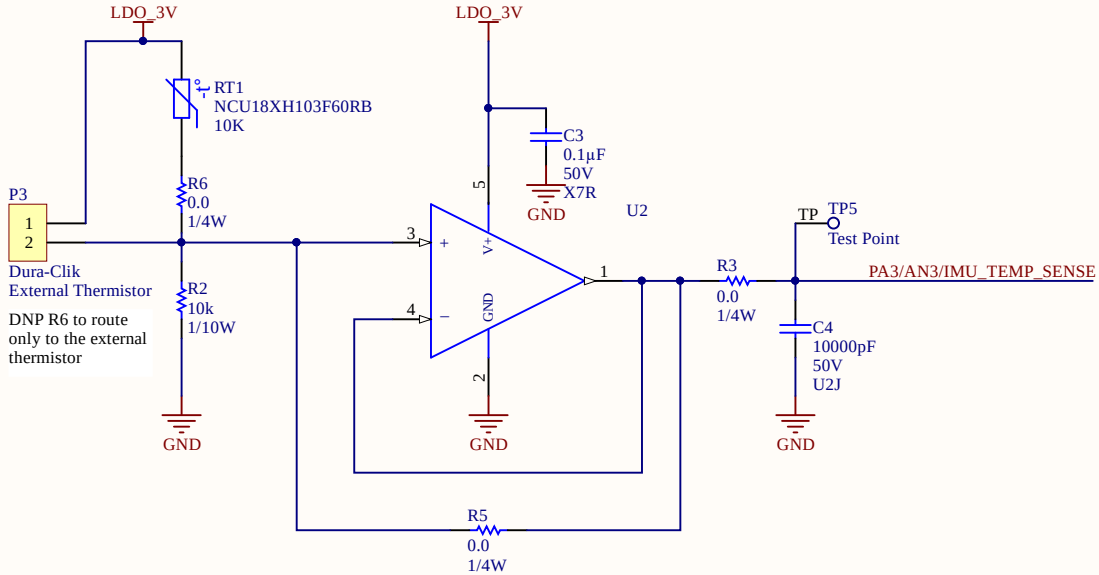




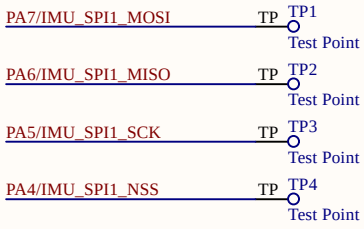
POWER



TEMP SENSE



TEST POINTS

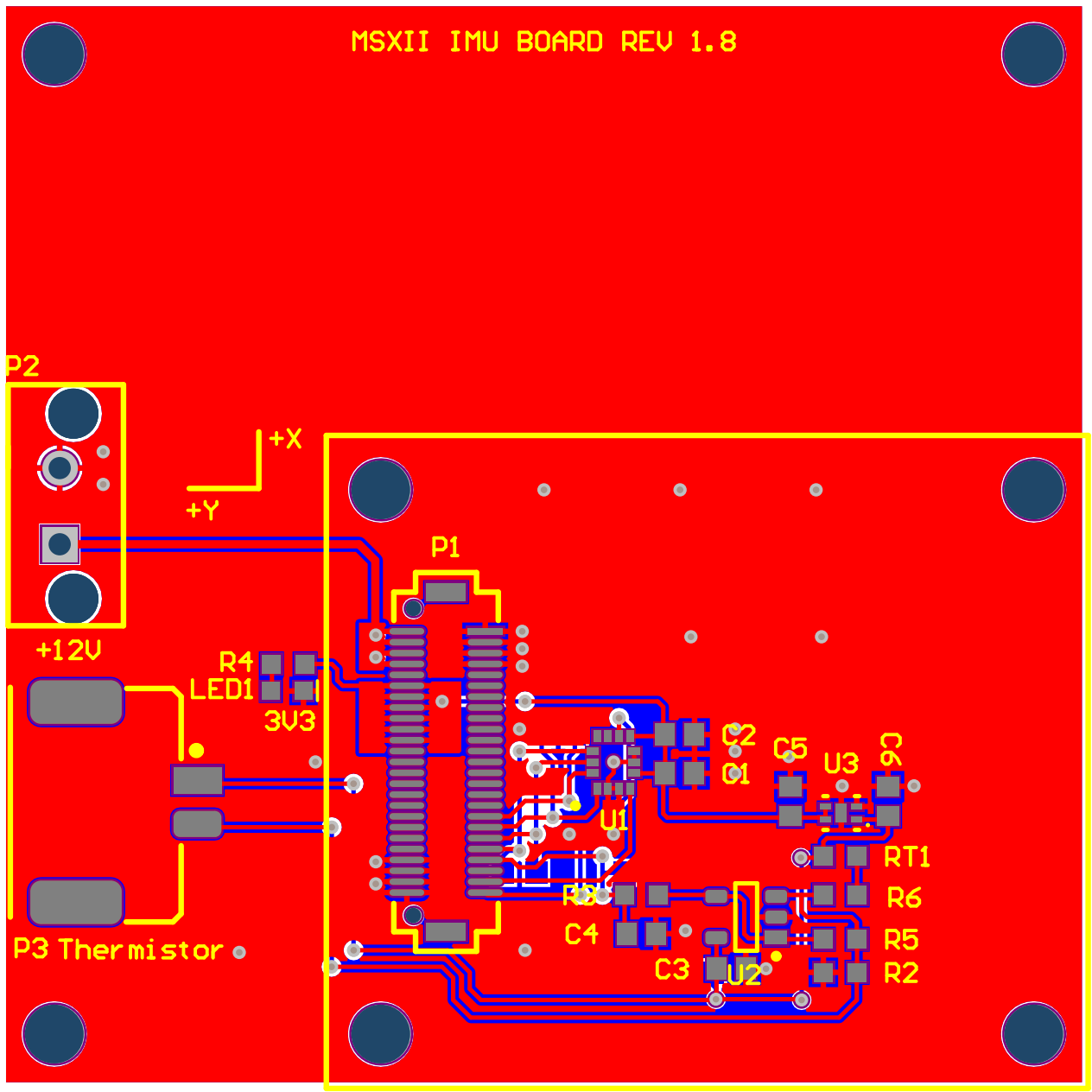


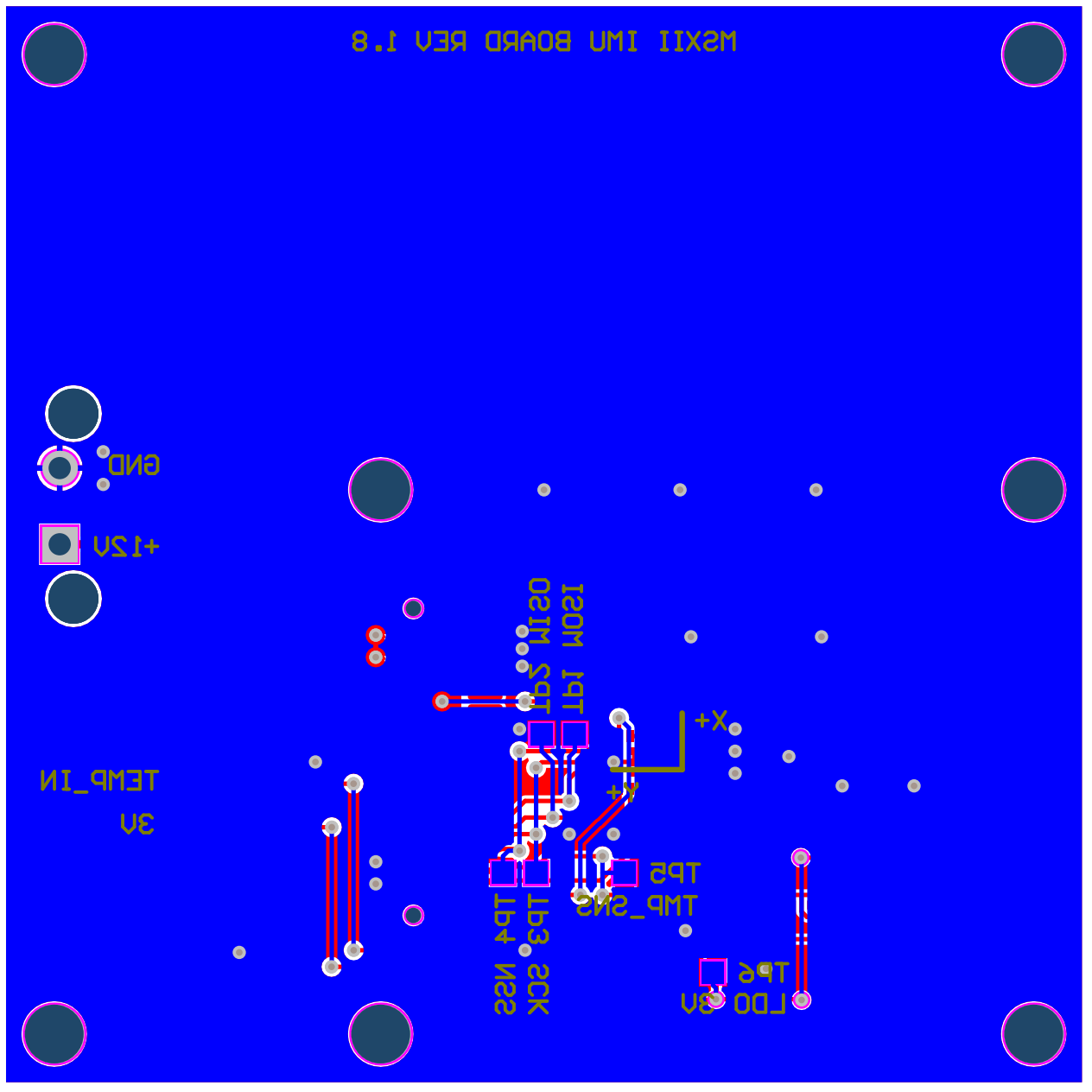
Project: ***IMU_Board.PrjPcb***		MIDNIGHT SUN
Title: **IMU Board**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Lead: George Mardari		
Size: Letter	Revision: 1.7	
Date: 2018-02-27	Sheet 2 of 2	Website: www.uwmidsun.com

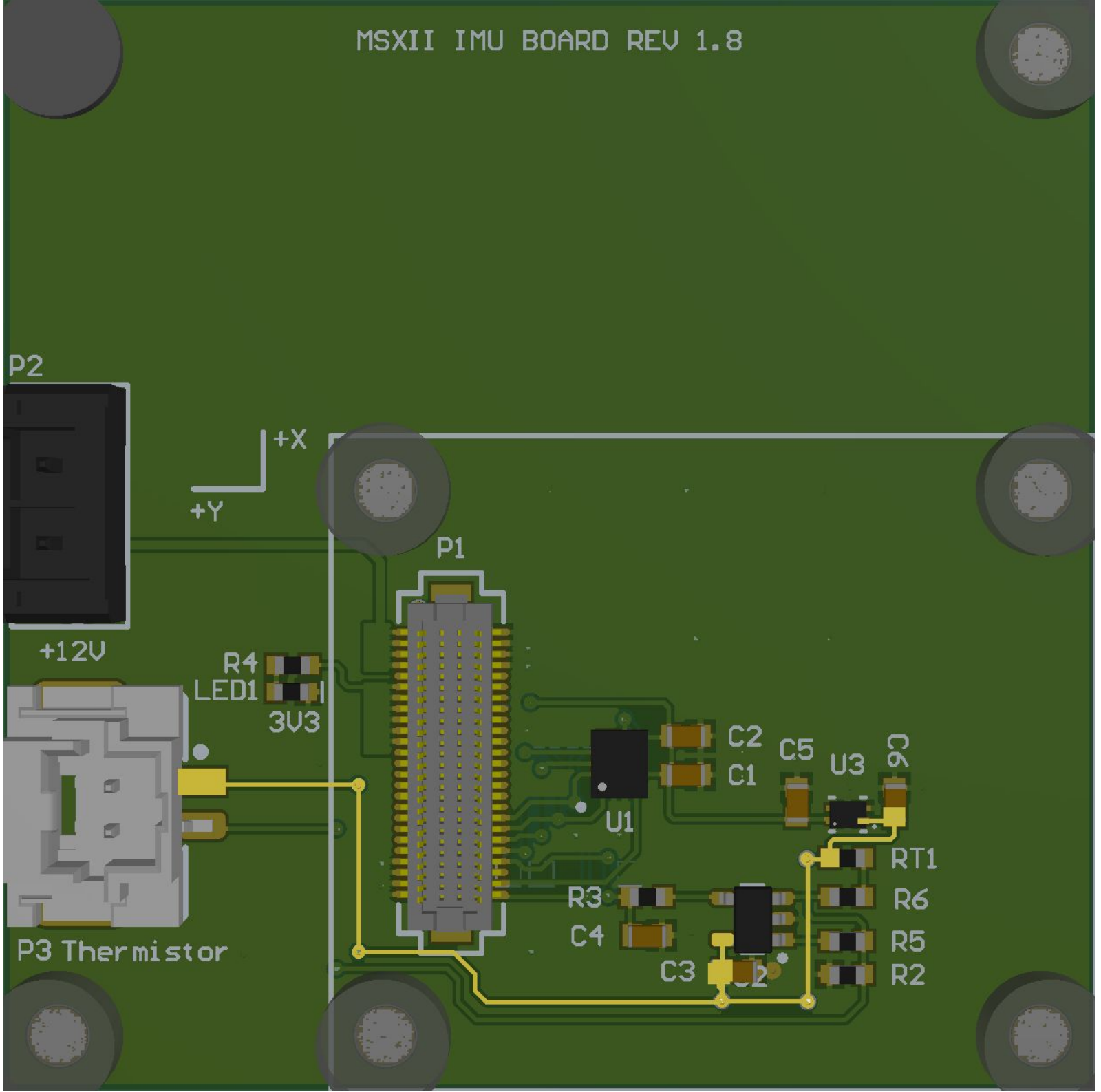
Bill of Materials

Project:	IMU_Board.PrjPcb
Revision:	1.7
Project Lead:	George Mardari
Generated On:	2018-02-27 8:47:01 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	24

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C1, C2, C3	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.13	3	$ 0.38
CAP CER 10nF 50V 5% X7R 0603	C4	KEMET	C0603C103J5JAC7867	Digi-Key	399-13384-1-ND	0.33	1	$ 0.33
CAP CER 1UF 50V 10% X7R 0603	C5, C6	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.34	2	$ 0.69
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18	1	$ 0.18
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.78	1	$ 1.78
CONN 2POS ULTRA-FIT 0.138"	P2	Molex	1722861302	Digi-Key	WM11673-ND	1.76	1	$ 1.76
CONN 2POS DURA-CLIK 0.079" VERT	P3	Molex	560020-0220	Digi-Key	WM10862CT-ND	1.04	1	$ 1.04
RES 10K OHM 1% 1/10W 0603	R2	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13	1	$ 0.13
RES 0.0 OHM 1/4W 0603	R3, R6	Vishay Dale	CRCW06030000Z0EAHP	Digi-Key	541-0.0SBCT-ND	0.22	2	$ 0.43
RES 604 OHM 1% 1/10W 0603	R4	Yageo	RC0603FR-07604RL	Digi-Key	311-604HRCT-ND	0.13	1	$ 0.13
NTC THERMISTORS 10KOHM 1608 SMD	RT1			Digi-Key				
Test Point	TP1, TP2, TP3, TP4, TP5, TP6							
IC SENSOR IMU LGA-14L	U1	STMicroelectronics	LSM6DS3USTR	Digi-Key	497-16910-1-ND	3.82	1	$ 3.82
IC OP AMP GEN PURPOSE RR 10MHZ SOT-23-5	U2	Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND	1.08	1	$ 1.08
IC REG LDO 3V 0.2A 4-TDFN	U3			Digi-Key				
							Total:	$ 11.75


MSXII IMU BOARD REV 1.8
P2
+X
+Y
+12V
P1
R4
LED1
3V3
C2
C1
C5
U3
C6
U1
RT1
R6
R5
R2
C4
C3
U2
P3 Thermistor


MSXII IMU BOARD REV 1.8
GND
+12V
TEMP_IN
3V
TP1 MOSI
TP2 MISO
TP3 SCK
TP4 NSS
TP5 TMP_SNS
TP6 LDO 5V
X+
Y+


MSXII IMU BOARD REV 1.8
P2
+X
+Y
P1
+12V
R4
LED1
3V3
C2
C1
C5
U3
C6
U1
RT1
R3
R6
C4
R5
C3
R2
P3 Thermistor

Electrical Rules Check Report

Class	Document	Message
Warning	IMU_Board.SchDoc	Net NetP3_2 has no driving source (Pin P3-2,Pin R2-2,Pin R5-1,Pin R6-2,Pin U2-3)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_IMUBoard\IMU_Boa

Warnings 0
Rule Violations 43

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.203mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.152mm) (All)	5
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	34
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	4
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	43

Minimum Annular Ring (Minimum=0.152mm) (All)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.2mm,15mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (32.9mm,4.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35.2mm,5.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (36.836mm,4.064mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (36.8mm,10.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(30.567mm,14.478mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(30.567mm,16.256mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(32.925mm,5.5mm) on Top Layer And Pad C3-2(34.275mm,5.5mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(28.789mm,7.112mm) on Top Layer And Pad C4-2(30.139mm,7.112mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(36.322mm,12.533mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(40.8mm,12.533mm) on Top Layer And Pad C6-2(40.8mm,13.883mm) on
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.3mm) Between Pad LED1-1(12.45mm,18.26mm) on Top Layer And Pad R4-2(12.475mm,19.5mm)
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.3mm) Between Pad LED1-2(13.95mm,18.26mm) on Top Layer And Pad R4-1(14.025mm,19.5mm)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(19mm,22.05mm) on Multi-Layer And Pad P1-(20.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(19mm,7.95mm) on Multi-Layer And Pad P1-(20.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad RT1-2(37.833mm,10.668mm) on Top Layer And Via (36.8mm,10.6mm) from
Minimum Solder Mask Sliver Constraint: (0.231mm < 0.3mm) Between Pad TP6-TP(32.766mm,5.334mm) on Bottom Layer And Via (32.9mm,4.1mm) from
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U1-1(27.444mm,13.786mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.066mm < 0.3mm) Between Pad U1-10(27.944mm,16.186mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U1-11(27.444mm,16.186mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.214mm < 0.3mm) Between Pad U1-12(27.244mm,15.486mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.3mm) Between Pad U1-13(27.244mm,14.986mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.066mm < 0.3mm) Between Pad U1-14(27.244mm,14.486mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.225mm < 0.3mm) Between Pad U1-14(27.244mm,14.486mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.066mm < 0.3mm) Between Pad U1-3(28.444mm,13.786mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U1-4(28.944mm,13.786mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.213mm < 0.3mm) Between Pad U1-5(29.144mm,14.486mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.166mm < 0.3mm) Between Pad U1-6(29.144mm,14.986mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.3mm) Between Pad U1-7(29.144mm,15.486mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.066mm < 0.3mm) Between Pad U1-7(29.144mm,15.486mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.203mm < 0.3mm) Between Pad U1-7(29.144mm,15.486mm) on Top Layer And Via (28.2mm,15mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U2-1(35.665mm,6.924mm) on Top Layer And Pad U2-2(35.665mm,7.874mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U2-2(35.665mm,7.874mm) on Top Layer And Pad U2-3(35.665mm,8.824mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U3-1(39.37mm,12.354mm) on Top Layer And Pad U3-2(39.37mm,12.954mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U3-1(39.37mm,12.354mm) on Top Layer And Pad U3-5(38.655mm,12.654mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.3mm) Between Pad U3-2(39.37mm,12.954mm) on Top Layer And Pad U3-5(38.655mm,12.654mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad U3-3(37.93mm,12.954mm) on Top Layer And Pad U3-4(37.93mm,12.354mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U3-3(37.93mm,12.954mm) on Top Layer And Pad U3-5(38.655mm,12.654mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad U3-4(37.93mm,12.354mm) on Top Layer And Pad U3-5(38.655mm,12.654mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C3-1(32.925mm,5.5mm) on Top Layer And Text "U2"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C3-2(34.275mm,5.5mm) on Top Layer And Text "U2"
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Pad LED1-2(13.95mm,18.26mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.17mm < 0.178mm) Between Pad P3-3(3.5mm,17.75mm) on Top Layer And Track