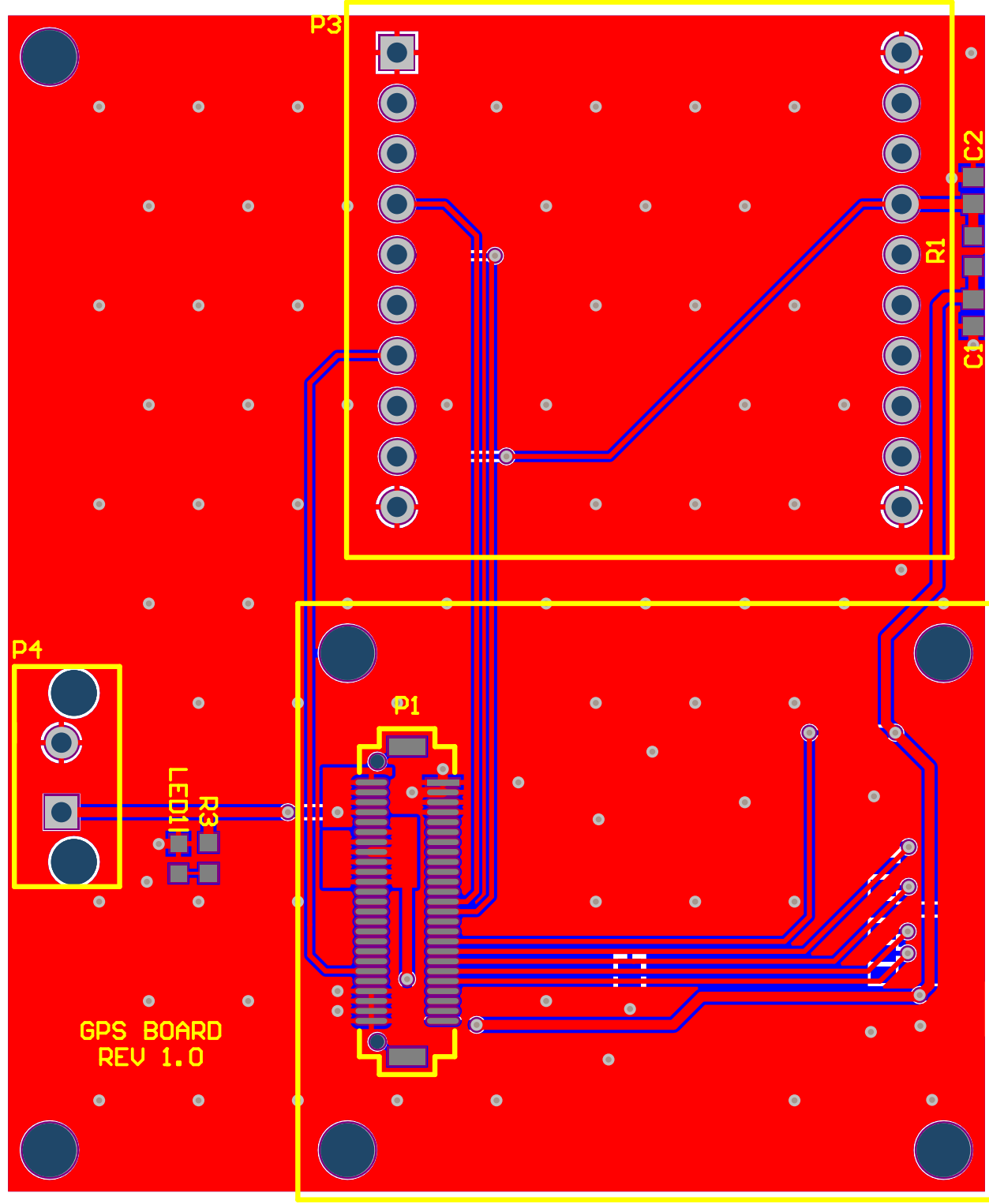


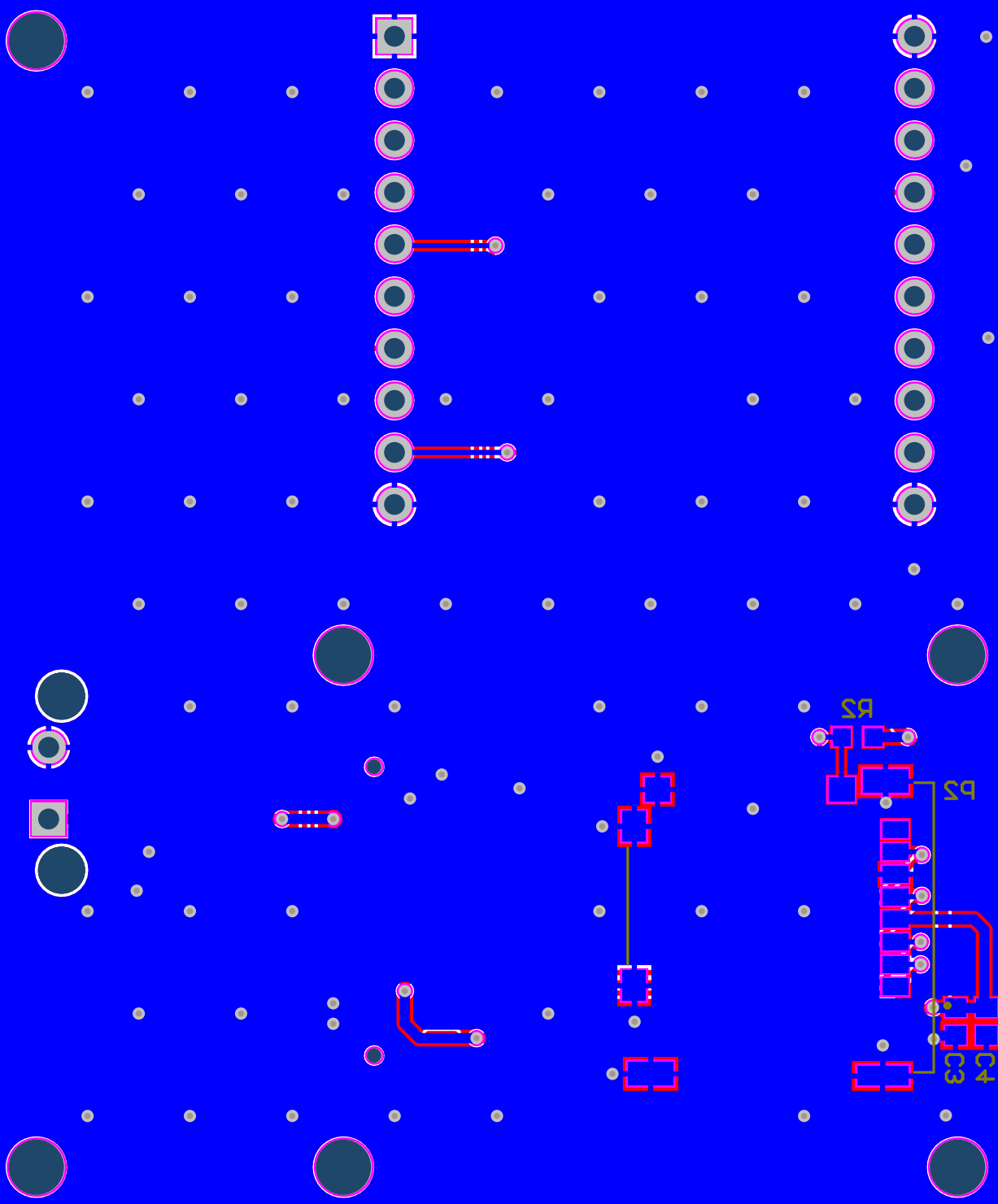
Bill of Materials

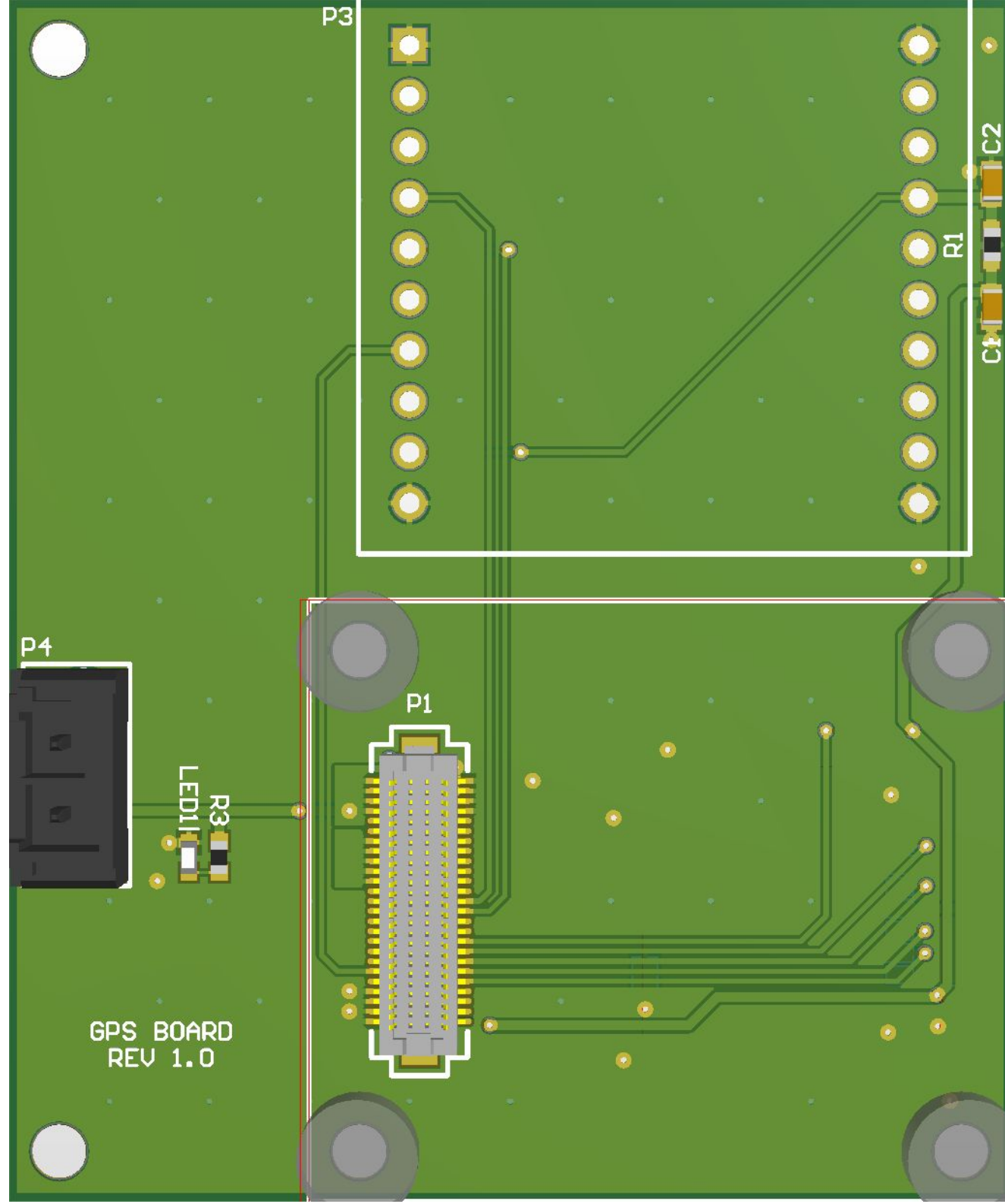
Project:	GPS Board.PrjPcb
Revision:	1
Project Lead:	Mena Labib
Generated On:	2019-01-23 23:10
Production Quantity:	1
Currency:	CAD
Total Parts Count:	12



LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C1, C4	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.22691	2	\$ 0.45
CAP CER 10uF 25V 20% X5R 0603	C2	Murata	GRM188R61E106MA73D	Digi-Key	490-7202-1-ND	0.56059	1	\$ 0.56
CAP CER 4.7UF 25V 10% X5R 0603	C3	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.49386	1	\$ 0.49
LED GREEN CLEAR 2V 0603	LED1	Würth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18686	1	\$ 0.19
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND			
CONN MICRO-SD ULTRA-LOW 8CKT	P2	Molex	503182-1852	Digi-Key	WM12834CT-ND	3.27	1	\$ 3.27
EVAL GPS EVM-GPS-F4	P3	Linx	EVM-GPS-F4	Digi-Key	EVM-GPS-F4-ND	84.3	1	\$ 84.30
CONN 2POS ULTRA-FIT 0.138"	P4	Molex	1722861302	Digi-Key	WM11673-ND	1.95	1	\$ 1.95
RES 100 OHM 1% 1/10W 0603	R1	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13347	1	\$ 0.13
RES 10K OHM 1% 1/10W 0603	R2	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13347	1	\$ 0.13
RES 4.7K OHM 1% 1/10W 0603	R3	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13347	1	\$ 0.13
							Total:	\$ 91.62







Electrical Rules Check Report

Class	Document	Message
Warning	GPS Board.SchDoc	Net PB10/USART1_TX_GPS_RX has no driving source (Pin P1-14,Pin P3-5)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\Midnight Sun\hardware\MSXI_GPS_Board\GPS Board.PcbDoc

Warnings 0
Rule Violations 140

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.152mm) (All)	95
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	31
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	1
Silk to Silk (Clearance=0.254mm) (All),(All)	5
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	8
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	140

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)

Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(34mm,43.95mm) on Top Layer And Pad C1-2(34mm,45.3mm) on Top
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C1-1(34mm,43.95mm) on Top Layer And Via (34mm,43mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(34mm,50.1mm) on Top Layer And Pad C2-2(34mm,51.45mm) on Top
Minimum Solder Mask Sliver Constraint: (0.11mm < 0.3mm) Between Pad C2-2(34mm,51.45mm) on Top Layer And Via (32.912mm,51.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(32.4mm,10.275mm) on Bottom Layer And Pad C3-2(32.4mm,8.925mm)
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.3mm) Between Pad C3-1(32.4mm,10.275mm) on Bottom Layer And Via (31.3mm,10.3mm) from
Minimum Solder Mask Sliver Constraint: (0.088mm < 0.3mm) Between Pad C3-2(32.4mm,8.925mm) on Bottom Layer And Via (31.334mm,8.75mm) from
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(33.9mm,8.925mm) on Bottom Layer And Pad C4-2(33.9mm,10.275mm)
Minimum Solder Mask Sliver Constraint: (0.087mm < 0.3mm) Between Pad LED1-2(-6.01mm,17.918mm) on Top Layer And Via (-7mm,17.9mm) from Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And Pad P1-(5.5mm,22.8mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And Pad P1-(5.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.293mm < 0.3mm) Between Pad P1-1(7.3mm,21mm) on Top Layer And Via (5.75mm,20.5mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.3mm) Between Pad P1-1(7.3mm,21mm) on Top Layer And Via (7.3mm,21.67mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad P1-2(7.3mm,20.5mm) on Top Layer And Via (5.75mm,20.5mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-1(29.464mm,11.3mm) on Bottom Layer And Pad P2-2(29.464mm,12.4mm)
Minimum Solder Mask Sliver Constraint: (0.267mm < 0.3mm) Between Pad P2-10(17.834mm,20.94mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.262mm < 0.3mm) Between Pad P2-11(17.504mm,7.055mm) on Bottom Layer And Via (15.639mm,7.055mm)
Minimum Solder Mask Sliver Constraint: (0.222mm < 0.3mm) Between Pad P2-11(28.984mm,21.345mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-2(29.464mm,12.4mm) on Bottom Layer And Pad P2-3(29.464mm,13.5mm)
Minimum Solder Mask Sliver Constraint: (0.112mm < 0.3mm) Between Pad P2-2(29.464mm,12.4mm) on Bottom Layer And Via (30.7mm,12.4mm) from Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-3(29.464mm,13.5mm) on Bottom Layer And Pad P2-4(29.464mm,14.6mm)
Minimum Solder Mask Sliver Constraint: (0.112mm < 0.3mm) Between Pad P2-3(29.464mm,13.5mm) on Bottom Layer And Via (30.7mm,13.5mm) from Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-4(29.464mm,14.6mm) on Bottom Layer And Pad P2-5(29.464mm,15.7mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-5(29.464mm,15.7mm) on Bottom Layer And Pad P2-6(29.464mm,16.8mm)
Minimum Solder Mask Sliver Constraint: (0.162mm < 0.3mm) Between Pad P2-5(29.464mm,15.7mm) on Bottom Layer And Via (30.75mm,15.75mm) from
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-6(29.464mm,16.8mm) on Bottom Layer And Pad P2-7(29.464mm,17.9mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P2-7(29.464mm,17.9mm) on Bottom Layer And Pad P2-8(29.464mm,19mm) on
Minimum Solder Mask Sliver Constraint: (0.162mm < 0.3mm) Between Pad P2-7(29.464mm,17.9mm) on Bottom Layer And Via (30.75mm,17.75mm) from
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad R2-1(26.825mm,23.5mm) on Bottom Layer And Via (25.75mm,23.5mm) from
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Via (2mm,10.5mm) from Top Layer to Bottom Layer And Via (2mm,9.5mm) from Top
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Via (30.7mm,12.4mm) from Top Layer to Bottom Layer And Via (30.7mm,13.5mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (31.999mm,10.39mm) on Bottom Overlay And Pad

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.235mm < 0.254mm) Between Text "LED1" (-6.41mm,21.652mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.167mm < 0.254mm) Between Text "P3" (0.75mm,58.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.249mm < 0.254mm) Between Text "P4" (-14.27mm,27.281mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.249mm < 0.254mm) Between Text "P4" (-14.27mm,27.281mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "R1" (32.49mm,47.217mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "P3" (0.75mm,58.75mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (2.452mm,32.32mm)(2.452mm,60.26mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (2.452mm,60.26mm)(32.932mm,60.26mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (32.932mm,32.32mm)(32.932mm,60.26mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,30mm) on Top Overlay