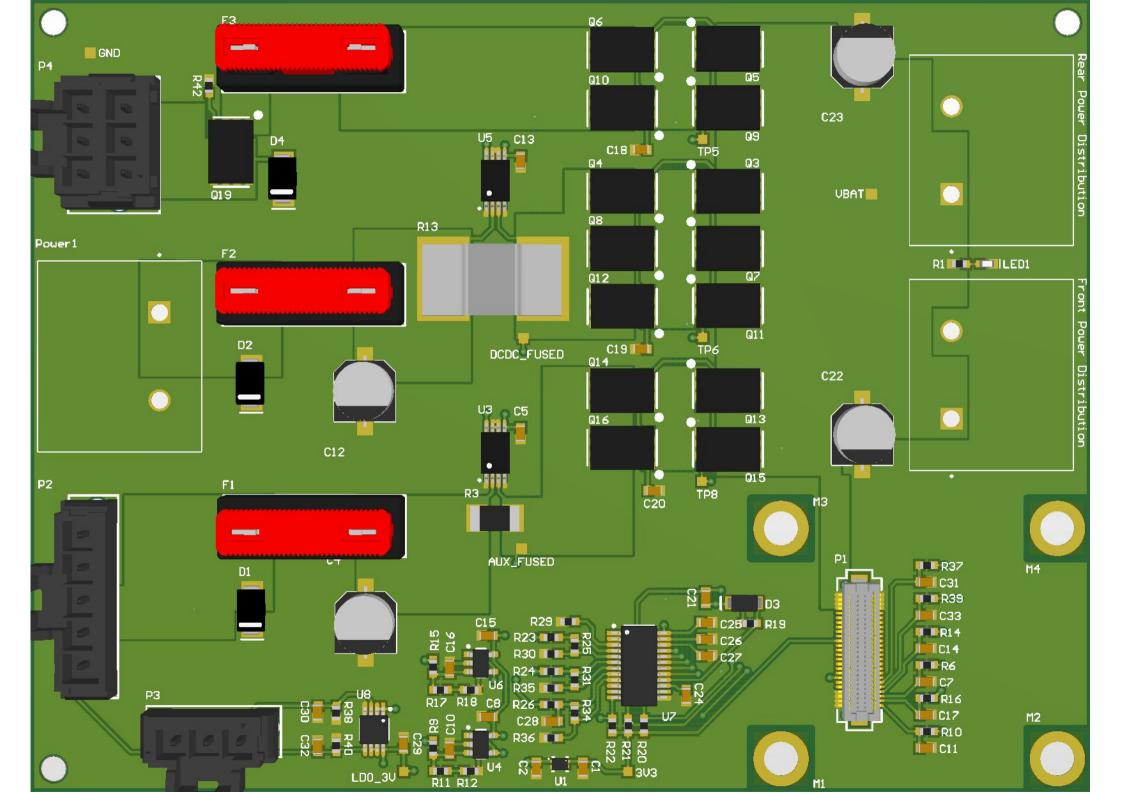
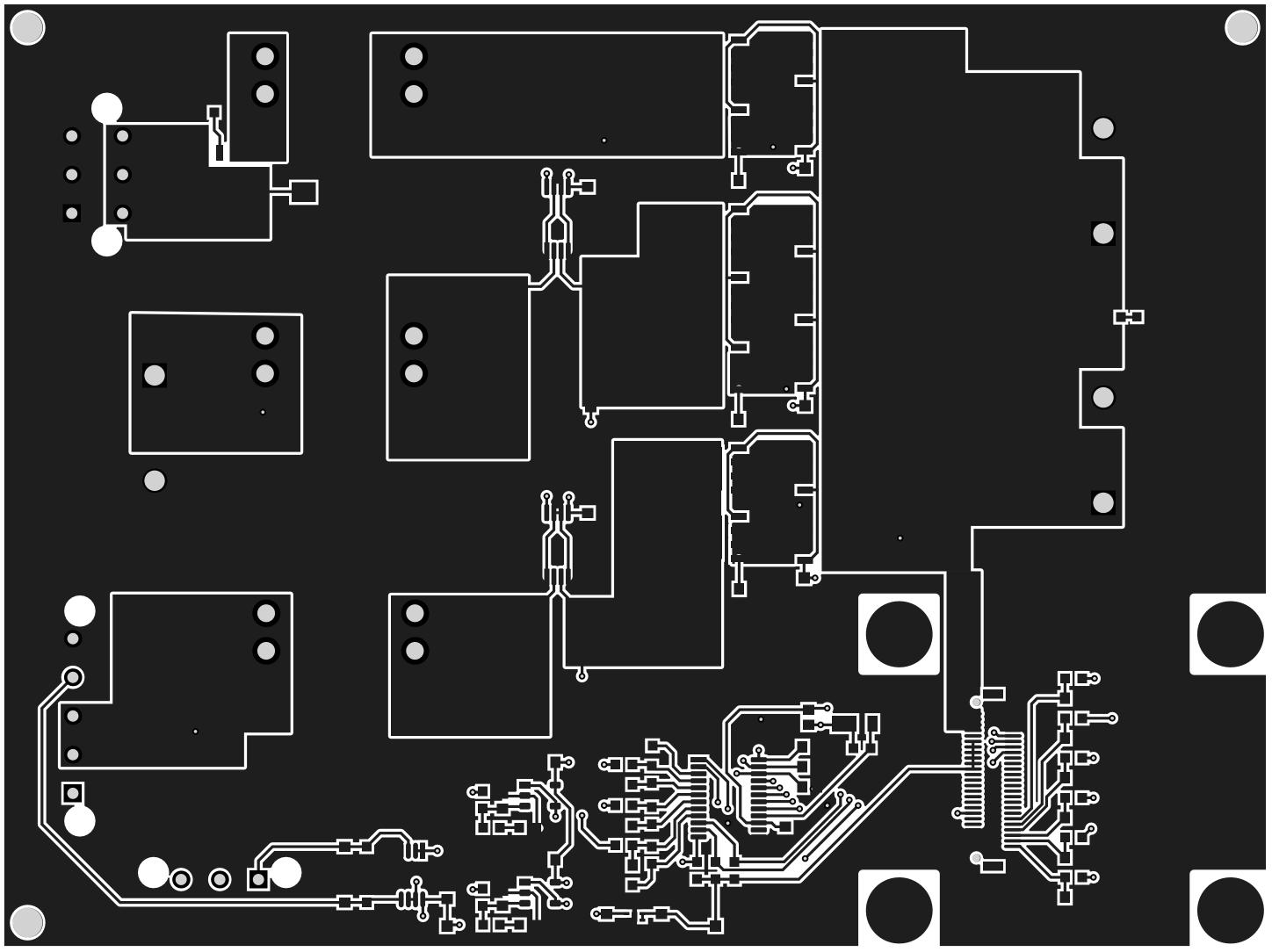


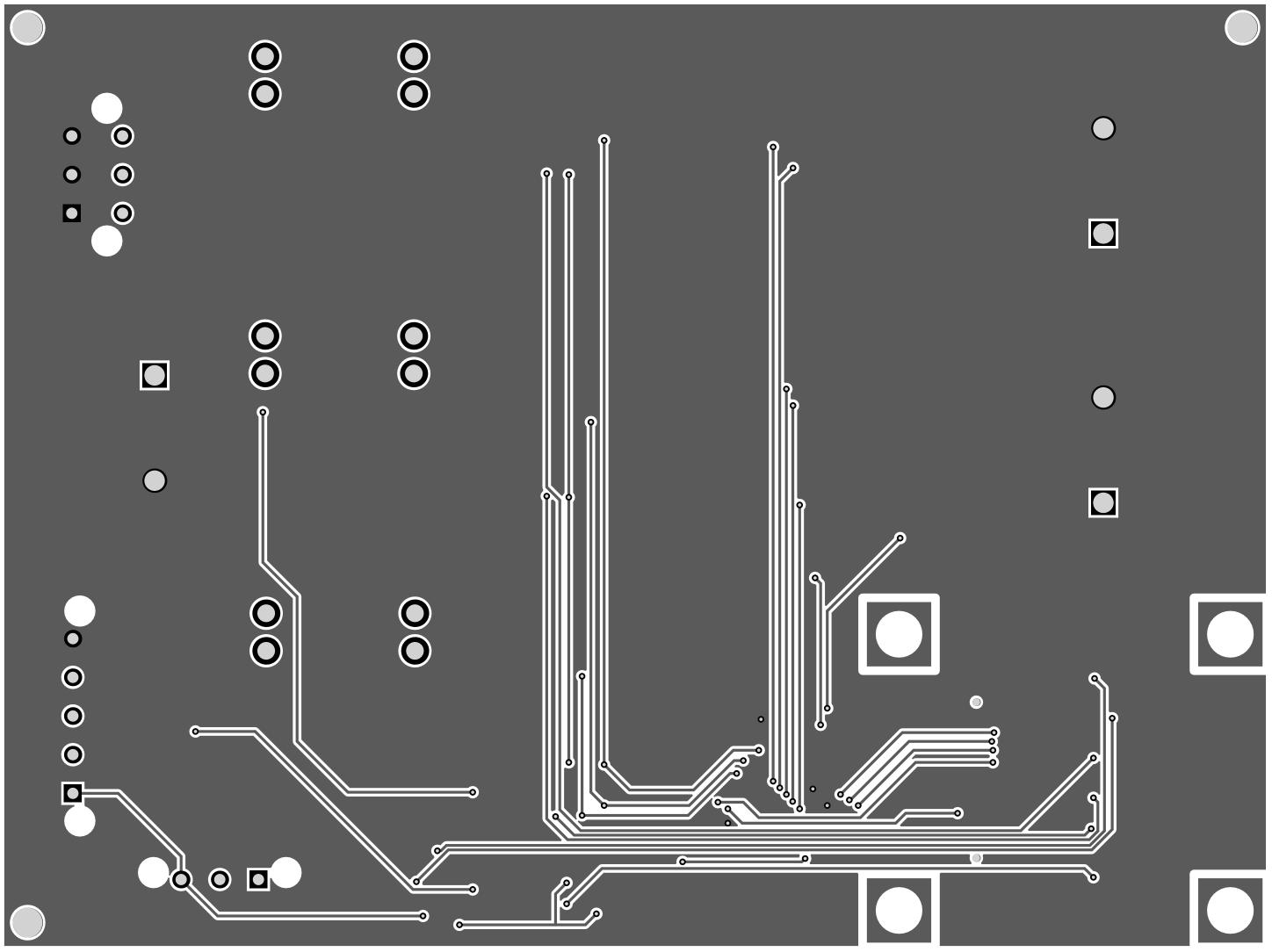
Bill of Ma	aterials
Project:	MSXIV_Pow erSelection.PrjPcb
Revision:	Parameter ProjectRevision not found:
Project Lead:	<parameter found="" not="" projectauthor=""></parameter>
Generated On:	2020-03-09 9:23 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	102



LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Suppl	lier Subtotal 1
CAPCER1UF50V10%X7R0603	C1,C2	TaiyoYuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.34007	2	\$	0.68
C AP ALUM47UF 20% 35V SMD	C4, C12	Panasonic	EEE-1VA470WP	Digi-Key	PCE3961CT-ND	0.55772	2	\$	1.12
C AP CER 0.1UF 50V 10% X7R 0603	28, C13, C15, C18, C19, C24, C25, C26, C27,	Kyocera AVX	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.09522	11	\$	1.05
CAP CER 10nF 50V 5% X7R 0603	,C10,C11,C14,C16,C17,C30,C31,C32,C	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.30471	10	\$	3.05
C AP CER 0.068UF 10% 50V X7R 0603	C20	Murata	GCM188R71H683KA57D	Digi-Key	490-8027-1-ND	0.24485	1	\$	0.24
CAP CER 6800pF 50V 10% X7R 0603	C21	Samsung	CL10B682KB8SFNC	Digi-Key	1276-2103-1-ND		1		
C AP ALUM100UF 20% 35V SMD	C22	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951CT-ND	0.63934	1	\$	0.64
C AP CER 0.022UF 50V 10% X7R 0603	C28	Murata	GRM188R71H223KA01D	Digi-Key	490-1517-1-ND		1		
DIODETVS 15VWM24.4VC DO-214AA (SMB)	D1, D2, D4	Taiwan Semiconductor	SMBJ15CA	Digi-Key	SMBJ15CAFSCT-ND	0.66655	3	\$	2.00
DIODESCHOTTKY 30V 1A POWERDI123	D3	Diodes	DFLS130L-7	Digi-Key	DFLS130LDICT-ND	0.59853	1	\$	0.60
FUSE ATO FUSE HOLDER	F1,F2,F3	Keystone Electronics	3557-2	Digi-Key	36-3557-2-ND	1.4	3	\$	4.20
CONN BARRIER STRIP 2CIRC 0.375"	Power Distribution, Power1, Rear Power Distri	BUCHANAN-TECONNECTIVITY	6PCV-02-006	Digi-Key	A98481-ND	2.22	3	\$	6.65
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.19044	1	\$	0.19
STANDOFF RND M2.5X0.45 STEEL 5MM	M1, M2, M3, M4	Wurth Electronics	9774050151R	Digi-Key	732-7095-1-ND	1.48	4	\$	5.93
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.96	1	\$	1.96
CONN 5POS ULTRA-FIT 0.138"	P2	Molex	1722871105	Digi-Key	WM11704-ND	1.41	1	\$	1.41
CONN 3POS ULTRA-FIT 0.138"	P3	Molex	172287-1103	Digi-Key	WM11702-ND	1.12	1	\$	1.12
CONN 6POS ULTRA-FIT 0.138"	P4	Molex	1722991106	Digi-Key	WM11778-ND	1.62	1	\$	1.62
MOSFETP-CH PWR56 40V 4.9 MOHM	Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q1	ON Semiconductor	FDWS9508L_F085	Digi-Key	DWS9508L-F085OSCT-N	VD.	15		
R ES 4.7K OHM1% 1/10W 0603	R1	Yageo Phycomp	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13603	1	\$	0.14
R ES 0.003 OHM1% 1.5W 2010	R3	Stackpole Electronics	CSNL2010FT3L00	Digi-Key	CSNL2010FT3L00CTNI	0.88419	1	\$	0.88
R E S 100 OHM 1% 1/10W 0603	R6,R10,R14,R16,R37,R39	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13603	6	\$	0.82
R ES 470K OHM1% 1/4W 0603	R9, R15	Panasonic	ERJ-PA3F4703V	Digi-Key	P470KBYCT-ND	0.19044	2	\$	0.38
R ES 100K OHM5% 1/8W 0603	R11,R17	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCT-ND	0.13603	2	\$	0.27
R ES 10K OHM1% 1/10W 0603	R12, R18, R20, R21, R22, R38, R40, R42	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13603	8	\$	1.09
R ES 0.004 OHM 1% 7W 5931	R13	Yageo	PU5931FKMP70R004L	Digi-Key	YAG4096CT-ND	2.73	1	\$	2.73
R ES 2.21K OHM1% 1/10W 0603	R19	Yageo	AC0603FR-072K21L	Digi-Key	YAG3586CT-ND	0.13603	1	\$	0.14
RES 1M OHM 1% 1/10W 0603	R23, R24, R26	Yageo	RC0603FR-071ML	Digi-Key	311-1.00MHRCT-ND	0.13603	3	\$	0.41
R ES SMD 11.3KOHM0.1% 1/10W 0603	R25, R31	Panasonic	ERA-3AEB1132V	Digi-Key	P11.3KDBCT-ND	0.4625	2	\$	0.93
R ES 255K OHM1% 1/10W 0603	R29	Yageo	RC0603FR-07255KL	Digi-Key	311-255KHRCT-ND	0.13603	1	\$	0.14
R E S SMD 75K OHM 0.1% 1/10W 0603	R30, R35	Panasonic	ERA-3AEB753V	Digi-Key	P75KDBCT-ND	0.4761	2	\$	0.95
RES SMD 48.7KOHM0.1% 1/10W 0603	R34, R36	Panasonic	ERA-3AEB4871V	Digi-Key	P4.87KDBCT-ND	0.4761	2	\$	0.95
IC REG LDO3V 0.2A 4-TDFN	U1	Microchip	MIC94310-PYMT-TR	Digi-Key	576-4761-1-ND	0.38088	1	\$	0.38
IC CURRENTAMPLIFIER INA240 8-TSSOP	U3	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.78	1	\$	3.78
C OP AMP GEN PUR POSE RR 10MHZ SOT-23-5		Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND	1.27	2	\$	2.53
IC CURRENTAMPLIFIER INA240 8-TSSOP	U5	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.78	1	\$	3.78
CORCONTROLLER SOURCE SELECT 24SSO	U7	Analog Devices/Linear	LTC4417CGN#PBF	Digi-Key	LTC4417CGN#PBF-ND	10.66	1	\$	10.66
IC OP AMP DUAL GPRR 10MHZ 8-VSSOP	U8	Texas Instruments	OPA2197IDGKR	Digi-Key	296-47349-1-ND	3.18	1	\$	3.18
							Total:	\$	66.59







Design Rules Verification ReportFilename: D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_PowerSelection\Power Sel

Warnings 0 Rule Violations 184

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	12
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	164
Silk to Silk (Clearance=0.254mm) (AII),(AII)	1
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	184

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(112.5mm,83.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,83.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M1-(81.4mm,3.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M2-(111.4mm,3.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M3-(81.4mm,28.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M4-(111.4mm,28.6mm) on Multi-Layer Actual Hole Size = 3.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(88.4mm,22.45mm) on Multi-Layer And Pad P1-(89.9mm,23.2mm) on Top.
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(88.4mm,8.35mm) on Multi-Layer And Pad P1-(89.9mm,7.6mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(56.735mm,3.325mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-1(56.735mm,3.325mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-2(56.735mm,2.725mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-4(58.175mm,3.325mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(47.525mm,6.15mm) on Top Layer And Pad U4-2(47.525mm,5.2mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(47.525mm,5.2mm) on Top Layer And Pad U4-3(47.525mm,4.25mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-1(47.525mm,14.95mm) on Top Layer And Pad U6-2(47.525mm,14mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-2(47.525mm,14mm) on Top Layer And Pad U6-3(47.525mm,13.05mm)

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Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.188mm < 0.254mm) Between Arc (56.227mm, 3.579mm) on Top Overlay And Pad U1-1(56.735mm, 3.325mm)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-1(36.3mm,46.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-1(36.3mm,46.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-2(36.3mm, 40.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-2(36.3mm, 40.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(90.2mm,41.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(90.2mm,41.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(90.2mm, 35.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(90.2mm, 35.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-1(90.2mm,76.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-1(90.2mm,76.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-2(90.2mm,82.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-2(90.2mm,82.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(36.4mm,21.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(36.4mm,21.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(36.4mm, 15.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(36.4mm, 15.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-2(24.1mm,17.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D2-2(24mm, 42.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D4-2(27.5mm,64.536mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.234mm) Between Pad B4-2(27.3mm, 04.330mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-3(24.1mm, 27.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-4(37.37mm, 27.1mm) on Multi-Layer And Track Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-3(24mm, 52.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-4(37.47mm,52.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F3-3(24mm,77.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F3-4(37.47mm,77.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(104.45mm,57.31mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(91.7mm,21.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(91.7mm,9.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(88.1mm, 9.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(88.1mm,21.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.259mm) Detween Pad Q10-1(66.895mm, 72.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-1(06.895mm, 73.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-3(66.895mm, 74.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.254mm) Between Pad Q10-4(66.895mm,76.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-5(61.405mm, 76.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-6(61.405mm, 74.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-7(61.405mm, 73.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-8(61.405mm, 72.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-1(72.895mm, 54.665mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1791mm < 0.254mm) Between Pad Q11-1(72.895mm,53.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1791ml < 0.254mm) Between Pad Q11-2(72.895mm,52.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-4(72.895mm,50.855mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-5(78.385mm,50.855mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-5(78.385mm,52.125mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-6(78.385mm,52.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-0(78.385mm,53.395mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-7(78.385mm,53.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-7(78.385mm,54.665mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-8(78.385mm,54.665mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-6(78.385mm, 50.765mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-1(66.9mm, 50.765mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-2(66.9mm,52.035mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-3(66.9mm,53.305mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-3(06.9mm,54.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-4(00.9mm),54.575mm) on Top Layer And Track Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-5(61.41mm,54.575mm) on Top Layer And Track
Silk to Solder wrask Cicarance Constraint to 224min Setween Fau Q12-5(01.41min,34.373min) on top Layer And mack

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Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-6(61.41mm,53.305mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-7(61.41mm,52.035mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-8(61.41mm,50.765mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-1(72.895mm, 45.465mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-2(72.895mm,44.195mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-3(72.895mm, 42.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-4(72.895mm,41.655mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-5(78.385mm,41.655mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-6(78.385mm, 42.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-7(78.385mm,44.195mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-8(78.385mm, 45.465mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-1(66.895mm,41.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-2(66.895mm,42.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-2(00.695mm,44.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-3(o6.895mm, 45.47mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-5(61.405mm, 45.47mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-6(61.405mm,44.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-7(61.405mm, 42.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-8(61.405mm,41.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-1(72.895mm, 39.105mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-2(72.895mm, 37.835mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-3(72.895mm, 36.565mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-4(72.895mm, 35.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-5(78.385mm, 35.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-6(78.385mm, 36.565mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-7(78.385mm, 37.835mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-8(78.385mm,39.105mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-1(66.895mm, 35.455mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-2(66.895mm, 36.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-3(66.895mm, 37.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-4(66.895mm,39.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-5(61.405mm,39.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-6(61.405mm,37.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-7(61.405mm, 36.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-8(61.405mm,35.455mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-1(23.7mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-2(22.43mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-3(21.16mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-4(19.89mm, 72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-5(19.89mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-6(21.16mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-7(22.43mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-8(23.7mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-1(72.895mm,67.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-2(72.895mm,65.795mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-3(72.895mm,64.525mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-4(72.895mm,63.255mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-5(78.385mm,63.255mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-6(78.385mm,64.525mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-7(78.385mm, 65.795mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-8(78.385mm,67.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-1(66.895mm,63.265mm) on Top Layer And Track

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Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-2(66.895mm,64.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-3(66.895mm,65.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-4(66.895mm,67.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-5(61.405mm,67.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-6(61.405mm,65.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-7(61.405mm,64.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-8(61.405mm,63.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-1(72.895mm,82.505mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-2(72.895mm,81.235mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-3(72.895mm,79.965mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-4(72.895mm, 78.695mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-5(78.385mm, 78.695mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-6(78.385mm, 79.965mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-0(78.385mm,81.235mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-7(76.385mm,82.505mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-1(66.895mm, 78.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-2(66.895mm, 79.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-3(66.895mm,81.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-4(66.895mm,82.405mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-5(61.405mm,82.405mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-6(61.405mm,81.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-7(61.405mm,79.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-8(61.405mm, 78.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-1(72.895mm,60.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-2(72.895mm,59.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-3(72.895mm,58.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-4(72.895mm,57.055mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-5(78.385mm,57.055mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-6(78.385mm, 58.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-7(78.385mm,59.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-8(78.385mm,60.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-1(66.895mm,57.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-2(66.895mm,58.335mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-3(66.895mm,59.605mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-4(66.895mm,60.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-5(61.405mm,60.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-6(61.405mm,59.605mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-7(61.405mm,58.335mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-8(61.405mm,57.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-1(72.895mm, 76.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-2(72.895mm,74.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-3(72.895mm, 73.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-4(72.895mm, 72.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-5(78.385mm, 72.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-6(78.385mm, 73.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-7(78.385mm, 74.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-8(78.385mm, 76.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R19-1(77.25mm,18.3mm) on Top Layer And Text "C25" (74.9mm,17.8mm)
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-1(56.735mm, 3.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-2(56.735mm,2.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-4(58.175mm,3.325mm) on Top Layer And Track

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Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U8-1(38.275mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-2(37.625mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-3(36.975mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-4(36.325mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-5(36.325mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-6(36.975mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-7(37.625mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-8(38.275mm,4.6mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C4" (32.233mm,24.79mm) on Top Overlay And Track

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