


Project: MSXIV_ConnectorTestingBoard.PrjPcb		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: Connector Testing Board		
Project Author Ricky Huang		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	Website: www.uwmidsun.com
Date: 2020-05-23	Sheet* of *	

Bill of Materials

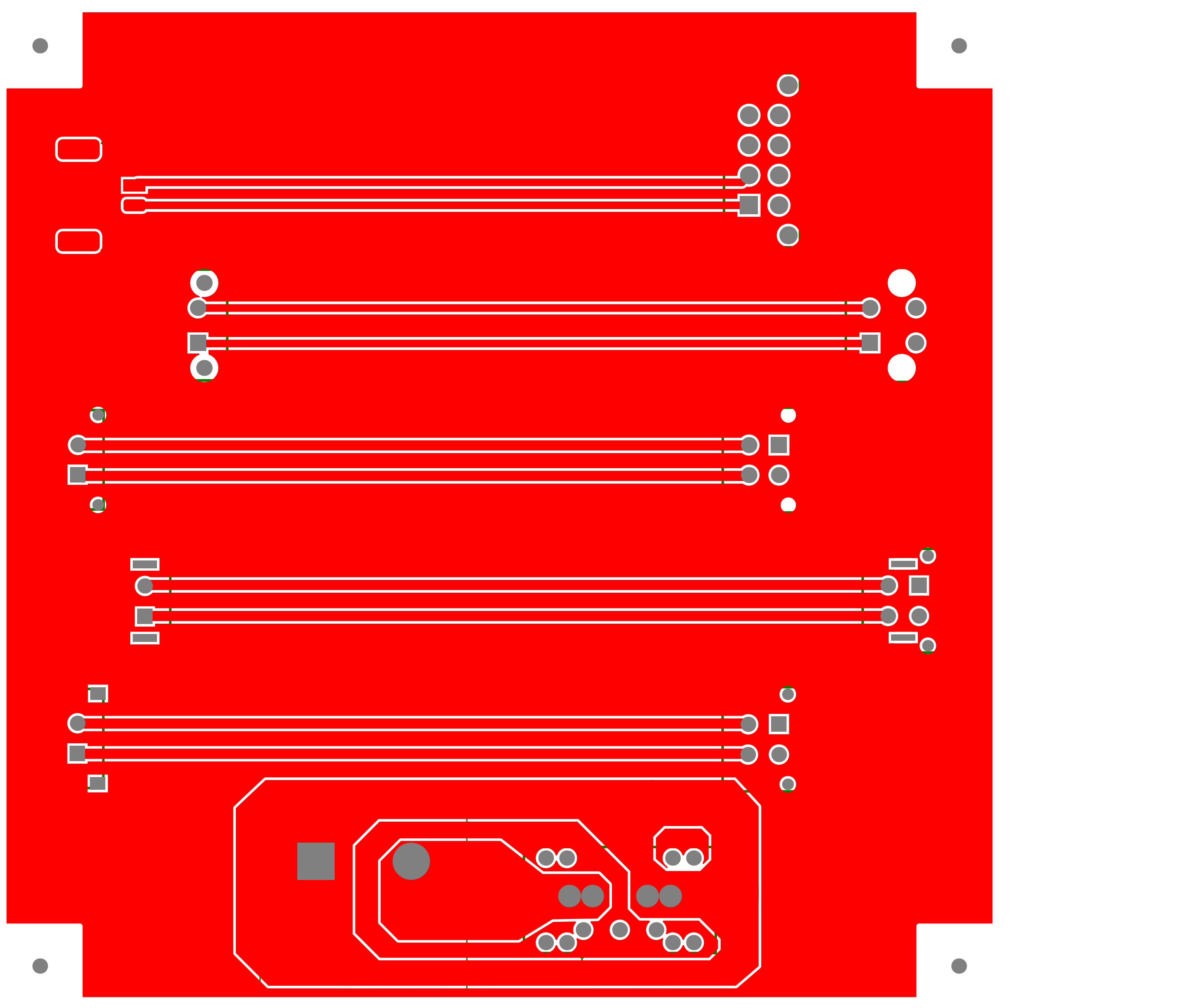
Project:	MSXIV_ConnectorTestingBoard.PrjPcb
Revision:	1.0
Project Lead:	Ricky Huang
Generated On:	2020-05-23 7:21 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	13

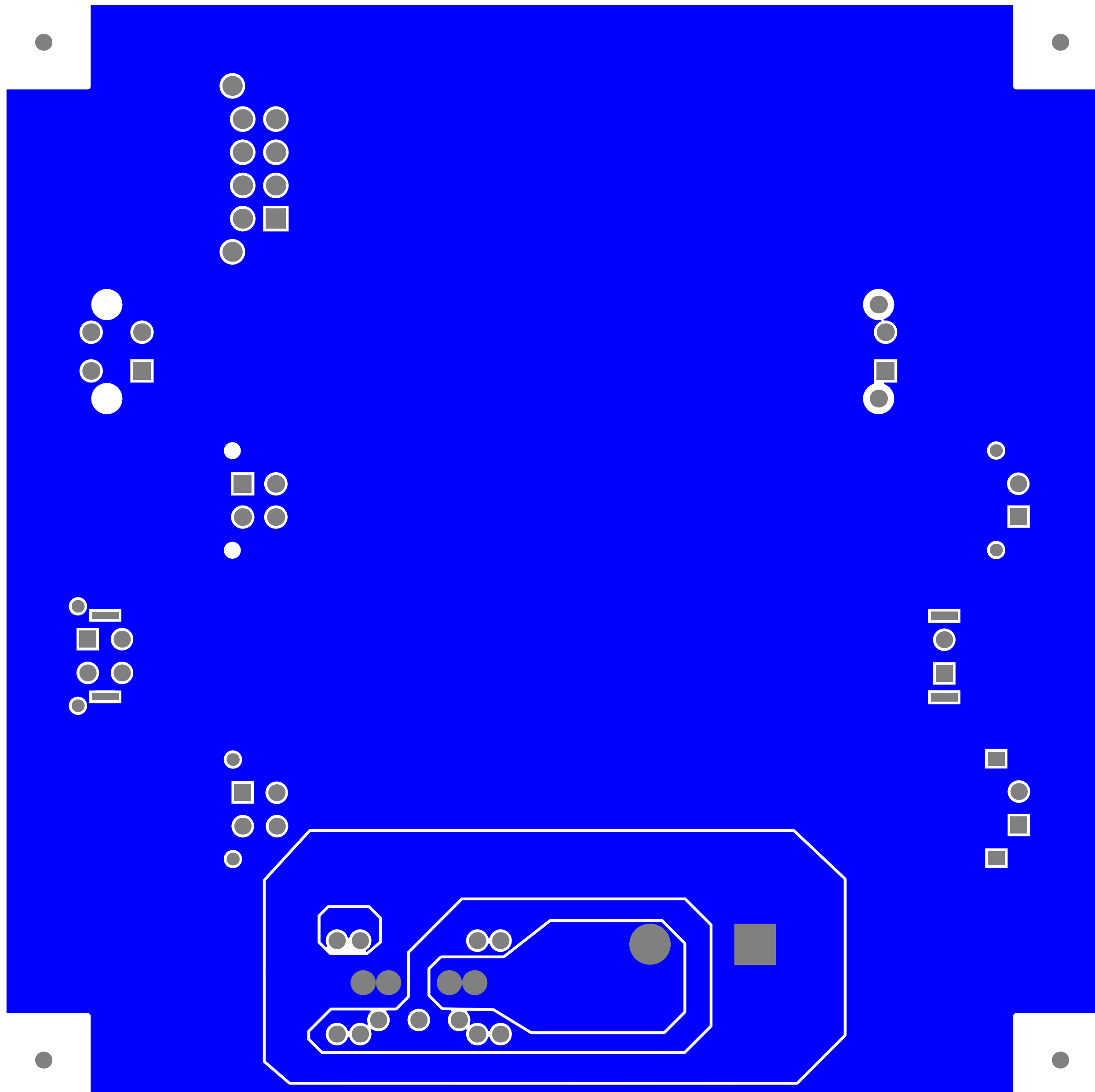
MIDNIGHT



S

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Name Error:' S	Supplier Part Number 1	Name Error:' Suppl
-00074-8, CMP-002-00072-6, CMP-002-00073-4,	Designator1, P3, P4, P5, P7, P8, P9, P10, P12	[NoParam], Molex, LLC, Molex	Param], 1722861302, 1722991104			
CMP-007-0025-1	P1					
CMP-007-0004-1	P2					
CMP-003-0105-1	P6					
CMP-007-0031-3	P11					





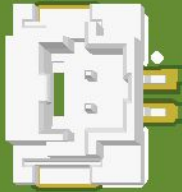
Single Row

MSXIV_ConnectorTestingBoard Rev 1.0

Dual Row

P1

Duraclik



MIDNIGHT SUN SOLAR CAR TEAM

P2



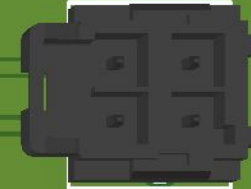
8 Pin
MicroFit

P3



UltraFit

P4

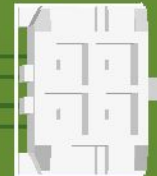


P5



MicroFit Tin

P6

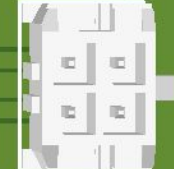


P7



MicroFit Gold Board Lock

P8



P9



MicroFit Gold Guide Peg

P10



P11



Barrier Term

P12



TE Power Term

Electrical Rules Check Report

Class	Document	Message
Warning	MSXIV_ConnectorTestingBoard.Sch Doc	Component P10 at 6250mil,3200mil: Component revision is Out of Date.

Design Rules Verification Report

Filename : C:\Users\ricky\Downloads\Projects\Midnight Sun\Midnight Sun Hardware\Winter

Warnings 0

Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	1
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	1

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-0(4mm,96mm) on Multi-Layer Actual Hole Size = 2.7mm	