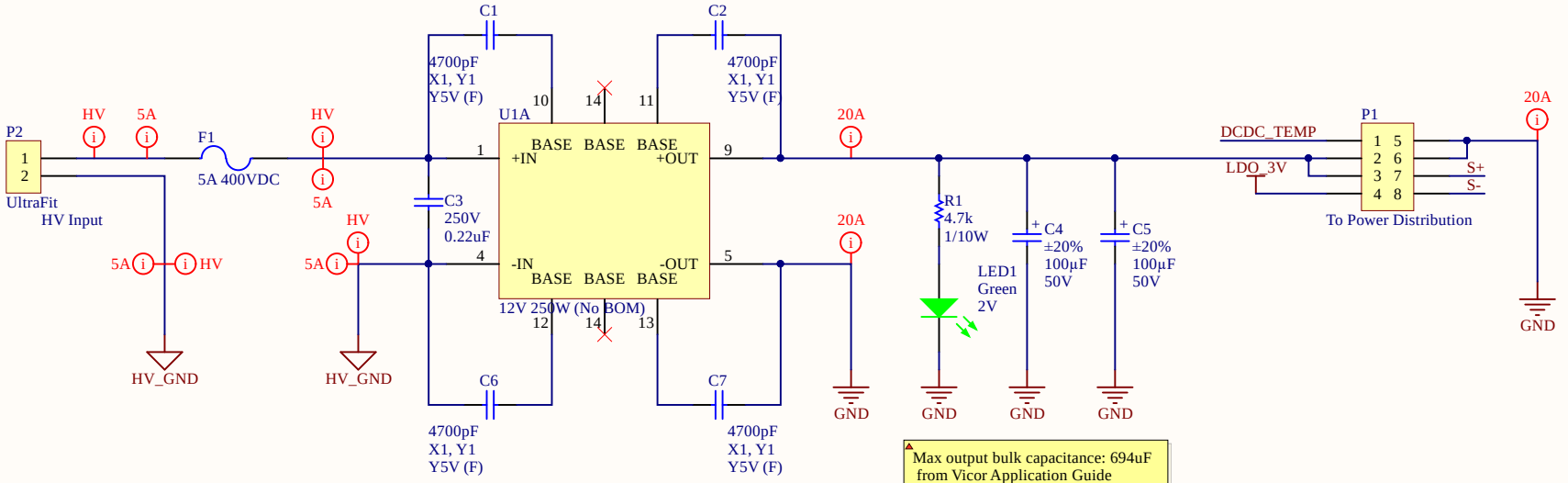
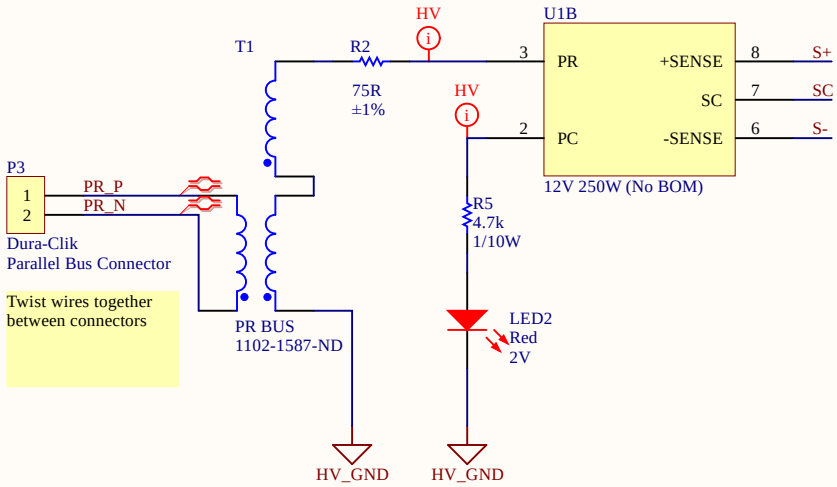
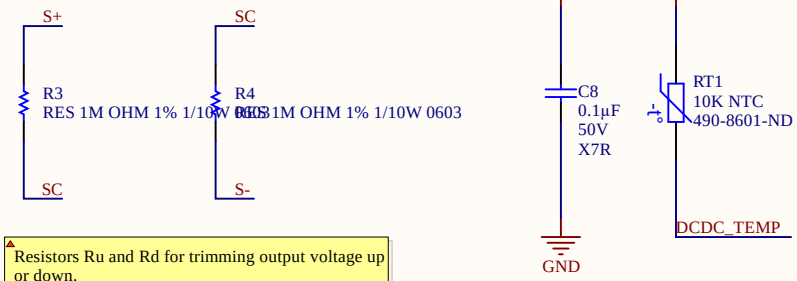
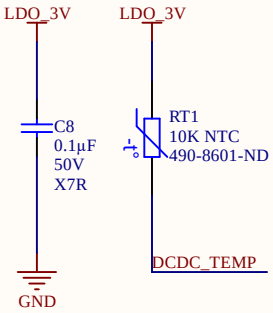








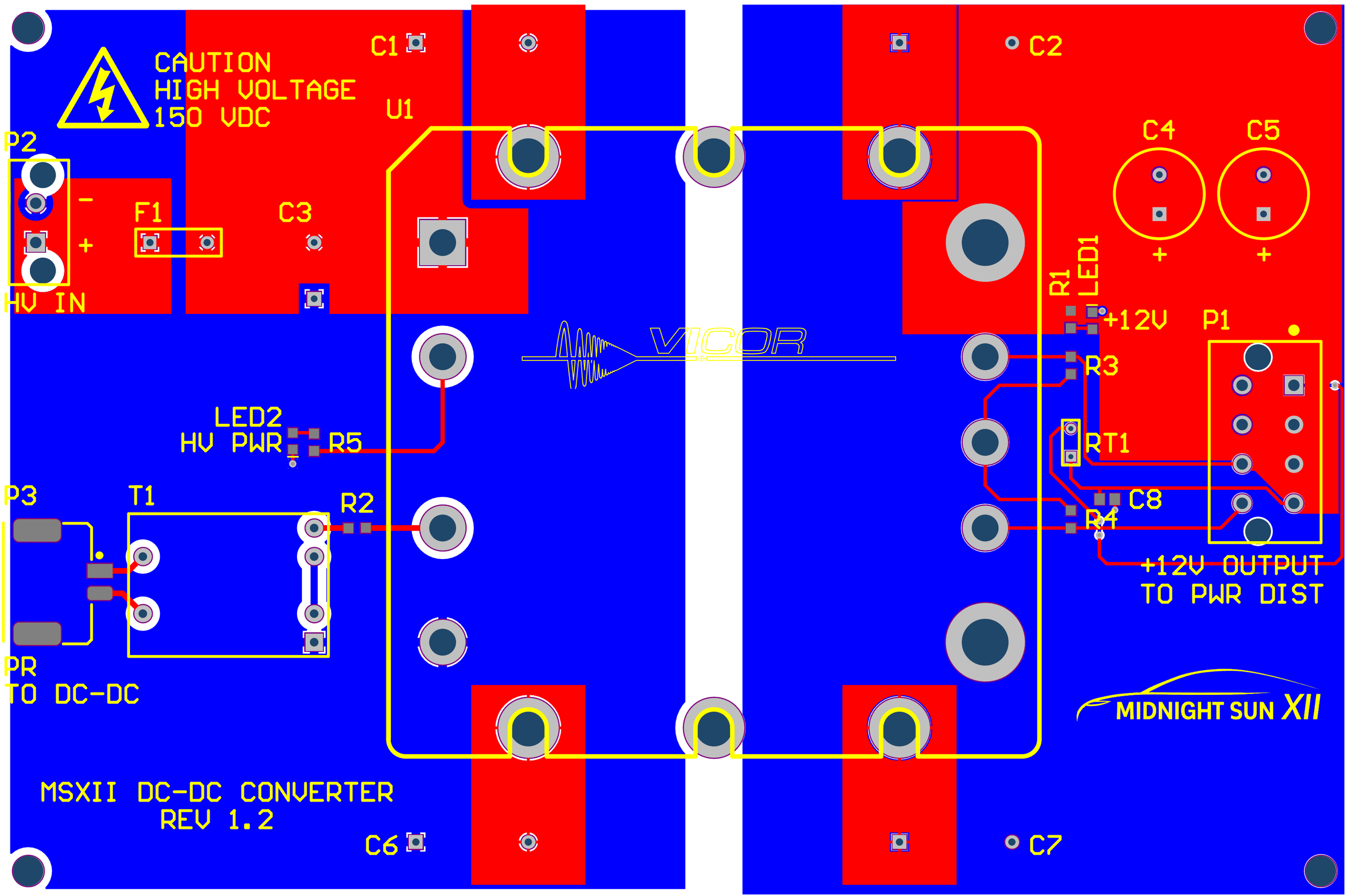
FAB Note: Use 2 oz copper for top and bottom layer

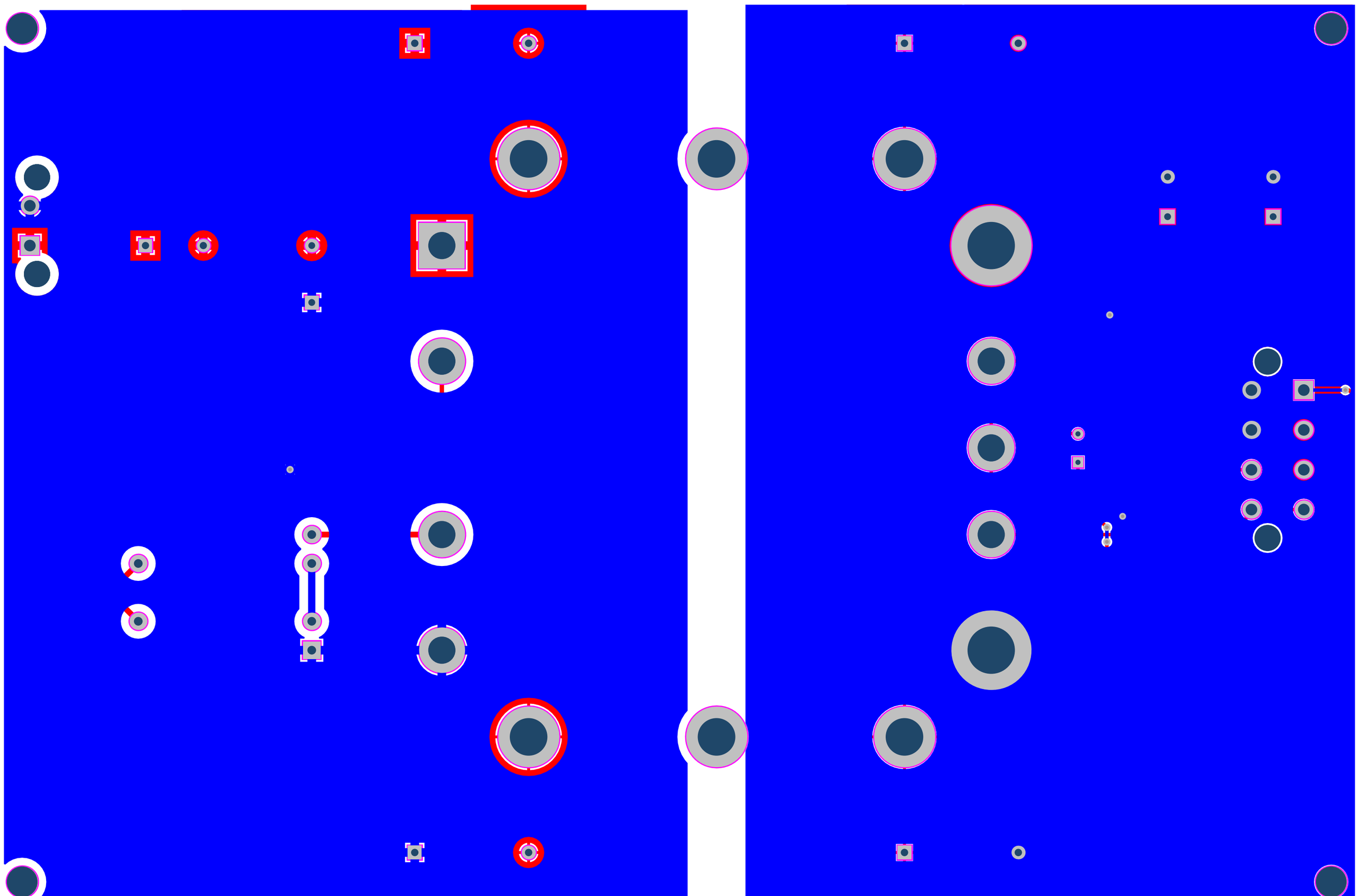
Project:	*MSXII_DC-DC_Converter.PrjPcb*	MIDNIGHT SUN
Title:	**MSXII DC-DC Converter**	
Project Lead:	Taiping Li	University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.2	
Date: 2018-02-23	Sheet 1 of 1	Website: www.uwmidsun.com

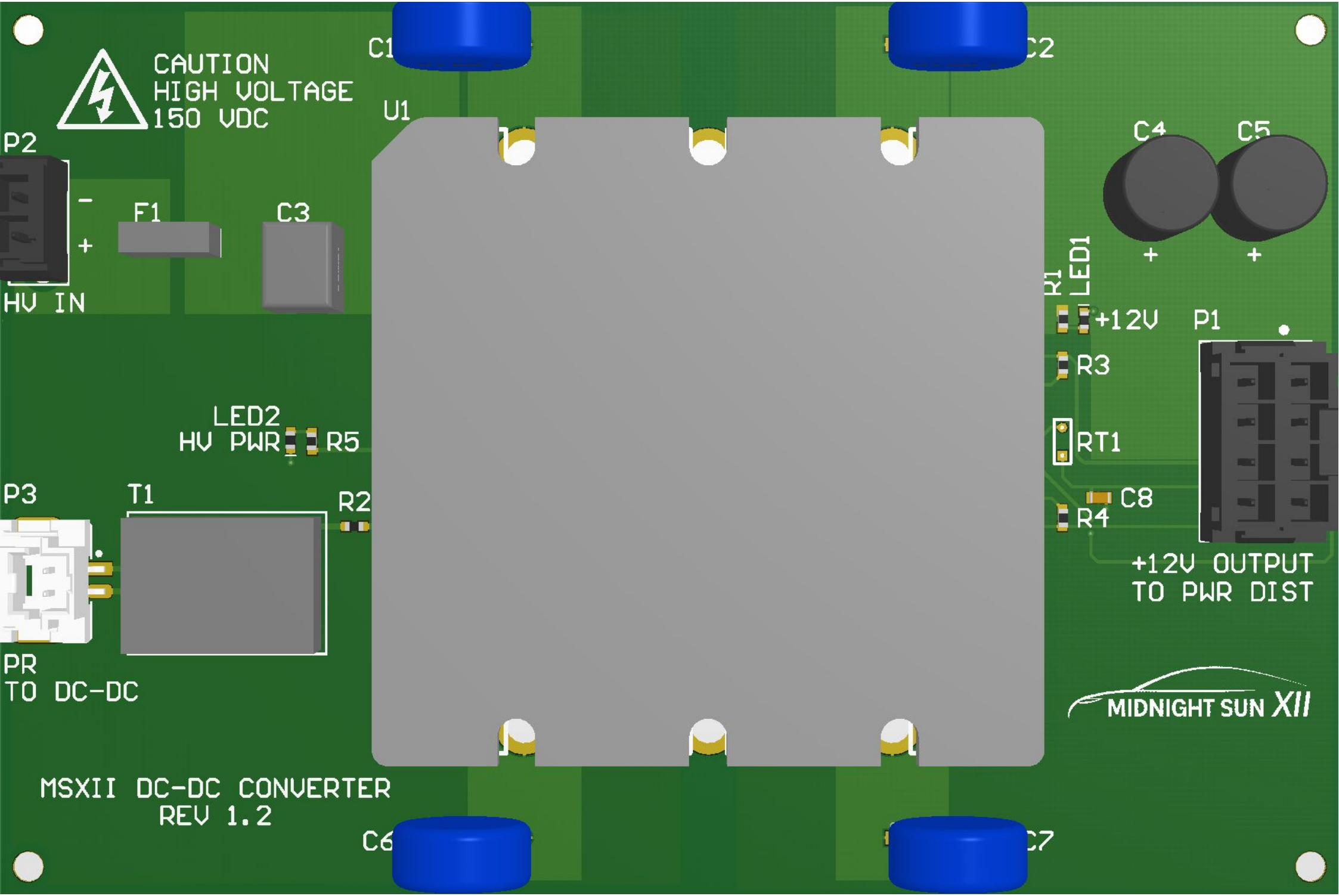
Bill of Materials

Project:	MSXII_DC-DC_Converter.PrjPcb
Revision:	1.2
Project Lead:	Taiping Li
Generated On:	2018-02-23 9:32:50 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	18

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 4700PF 400VAC Y5V RADIAL	C1, C2, C6, C7	KEMET	C951U472MVVDBA7317	Digi-Key	399-9517-1-ND	1.09	4	$ 4.36
CAP FILM 0.22UF 5% 250VDC RADIAL	C3	KEMET	R82IC3220AA60J	Digi-Key	399-6046-ND	0.8	1	$ 0.80
CAP ALUM 100UF 20% 50V RADIAL	C4, C5	KEMET	ESY107M050AG3AA	Digi-Key	399-6119-ND	0.45	2	$ 0.90
CAP CER 0.1UF 50V 10% X7R 0603	C8	AVX Corporation	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.13	1	$ 0.13
FUSE 5A 125VAC/400VDC RADIAL	F1	Eaton	BK/PCE-5-R	Digi-Key	283-2770-ND	2.99	1	$ 2.99
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics Inc.	150060VS75000	Digi-Key	732-4980-1-ND	0.19	1	$ 0.19
LED RED CLEAR 2V 0603	LED2	Wurth Electronics Inc.	150060RS75000	Digi-Key	732-4978-1-ND	0.19	1	$ 0.19
CONN 8POS ULTRA-FIT 0.138"	P1	Molex, LLC	1722991108	Digi-Key	WM11779-ND	1.92	1	$ 1.92
CONN 2POS ULTRA-FIT 0.138"	P2	Molex, LLC	1722861302	Digi-Key	WM11673-ND	1.84	1	$ 1.84
CONN 2POS DURA-CLIK 0.079" VERT	P3	Molex, LLC	5600200220	Digi-Key	WM10862CT-ND	1.09	1	$ 1.09
RES 4.7K OHM 1% 1/10W 0603	R1, R5	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.14	2	$ 0.28
RES 75R OHM 1% 1/10W 0603	R2	Yageo	AC0603FR-0775RL	Digi-Key	YAG3630CT-ND	0.14	1	$ 0.14
NTC THERMISTOR 10K 1% BEAD	RT1	Murata Electronics North America	NXRT15XH103FA1B030	Digi-Key	490-8601-ND	0.93	1	$ 0.93
							Total:	$ 15.76


CAUTION
HIGH VOLTAGE
150 VDC
C1
C2
U1
P2
F1
C3
HV IN
C4
C5
R1
LED1
+12V
P1
R3
VICOR
LED2
HV PWR
R5
RT1
P3
T1
R2
C8
R4
+12V OUTPUT
TO PWR DIST
PR
TO DC-DC
MIDNIGHT SUN XII
MSXII DC-DC CONVERTER
REV 1.2
C6
C7




CAUTION
HIGH VOLTAGE
150 VDC
C1
C2
U1
P2
–
+
F1
C3
HV IN
C4
C5
+
+
R1
LED1
+12V
P1
R3
LED2
HV PWR
R5
RT1
P3
T1
R2
C8
R4
+12V OUTPUT
TO PWR DIST
PR
TO DC-DC
MIDNIGHT SUN XII
MSXII DC-DC CONVERTER
REV 1.2
C6
C7

Electrical Rules Check Report

Class	Document	Message
Warning	MSXII_DC-DC_Converter.SchDoc	Duplicate pins in component Pin U1-14 and Pin U1-14

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_DC-DC_Converter\MSXII_DC-DC_Converter.PcbDoc

Warnings 0
Rule Violations 46

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.762mm) (InNetClass('HV')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.381mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.152mm) (All)	1
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	1
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	39
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	5
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	46

Minimum Annular Ring (Minimum=0.152mm) (All)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (59.805mm,-23.795mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer)

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-2(59.805mm,-22.82mm) on Top Layer And Pad C8-1(58.455mm,-22.82mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (24.13mm,-43.18mm) on Top Overlay And Pad U1-14(24.13mm,-43.18mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (7.62mm,7.62mm) on Top Overlay And Pad U1-10(7.62mm,7.62mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (24.13mm,7.62mm) on Top Overlay And Pad U1-14(24.13mm,7.62mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (40.64mm,-43.18mm) on Top Overlay And Pad U1-13(40.64mm,-43.18mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (40.64mm,7.62mm) on Top Overlay And Pad U1-11(40.64mm,7.62mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (7.62mm,-43.18mm) on Top Overlay And Pad U1-12(7.62mm,-43.18mm) on
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (55.13mm,-19.8mm)(55.13mm,-15.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (56.63mm,-19.8mm)(56.63mm,-15.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (55.13mm,-19.8mm)(56.63mm,-19.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (55.13mm,-19.8mm)(55.13mm,-15.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (56.63mm,-19.8mm)(56.63mm,-15.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Track (55.13mm,-15.8mm)(56.63mm,-15.8mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (22.492mm,-45.72mm)(22.492mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (25.768mm,-45.72mm)(25.768mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (9.258mm,-45.72mm)(22.492mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (25.768mm,-45.72mm)(39.002mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (22.492mm,7.62mm)(22.492mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (25.768mm,7.62mm)(25.768mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (9.258mm,10.16mm)(22.492mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (25.768mm,10.16mm)(39.002mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (5.982mm,-45.72mm)(5.982mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (9.258mm,-45.72mm)(9.258mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (9.258mm,-45.72mm)(22.492mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (-3.302mm,-45.72mm)(5.982mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (39.002mm,-45.72mm)(39.002mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (42.278mm,-45.72mm)(42.278mm,-43.18mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (42.278mm,-45.72mm)(51.562mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (25.768mm,-45.72mm)(39.002mm,-45.72mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (39.002mm,7.62mm)(39.002mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (42.278mm,7.62mm)(42.278mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (42.278mm,10.16mm)(51.562mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (25.768mm,10.16mm)(39.002mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (5.982mm,7.62mm)(5.982mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Track (9.258mm,7.62mm)(9.258mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (9.258mm,10.16mm)(22.492mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.178mm) Between Track (-1.016mm,10.16mm)(5.982mm,10.16mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.114mm < 0.178mm) Between Track (-33.73mm,-24.985mm)(-31.605mm,-24.985mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Track (57.315mm,-5.562mm)(58.225mm,-5.562mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Track (-13.775mm,-19.063mm)(-12.865mm,-19.063mm) on Top Overlay And

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.163mm < 0.406mm) Between Track (-39.08mm,-35.485mm)(-39.08mm,-24.935mm) on Top Overlay And Board
Board Outline Clearance(Outline Edge): (0.273mm < 0.406mm) Between Text "PR

TO DC-DC" (-39.097mm,-41.158mm) on Top Overlay And Board Edge

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.273mm < 0.406mm) Between Text "P2" (-38.843mm,8.223mm) on Top Overlay And Board Edge
Board Outline Clearance(Outline Edge): (0.273mm < 0.406mm) Between Text "P3" (-38.843mm,-23.247mm) on Top Overlay And Board Edge
Board Outline Clearance(Outline Edge): (0.273mm < 0.406mm) Between Text "HV IN" (-38.843mm,-6.096mm) on Top Overlay And Board Edge