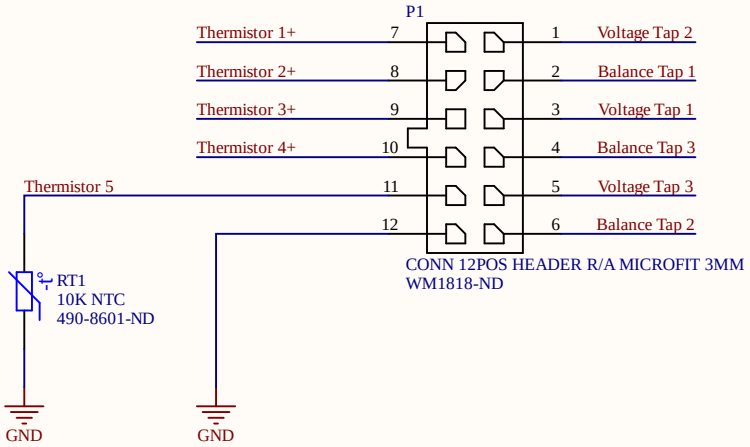
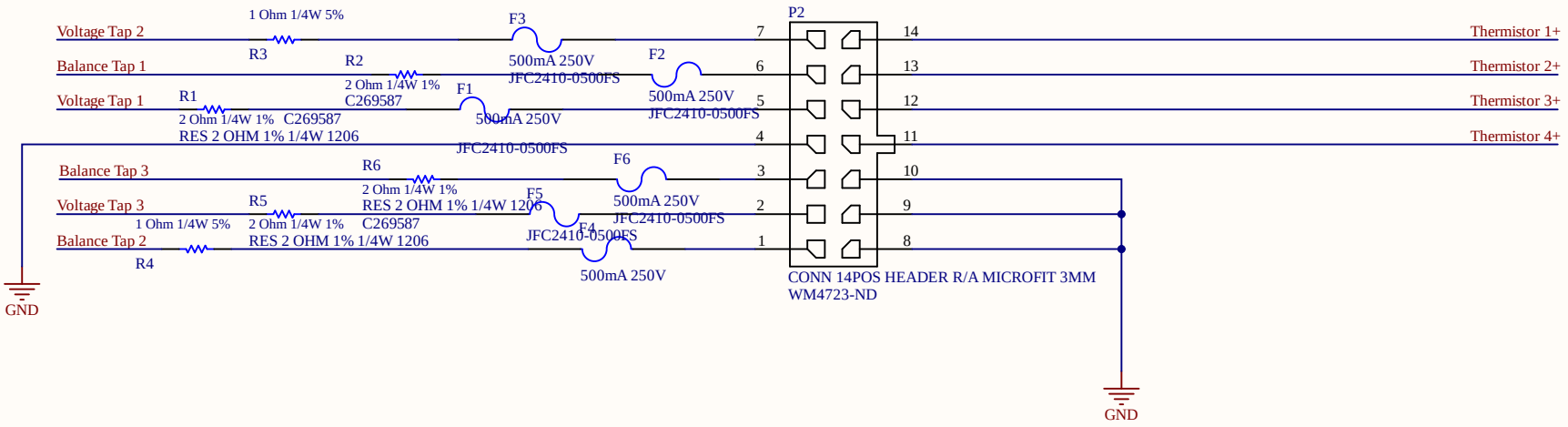


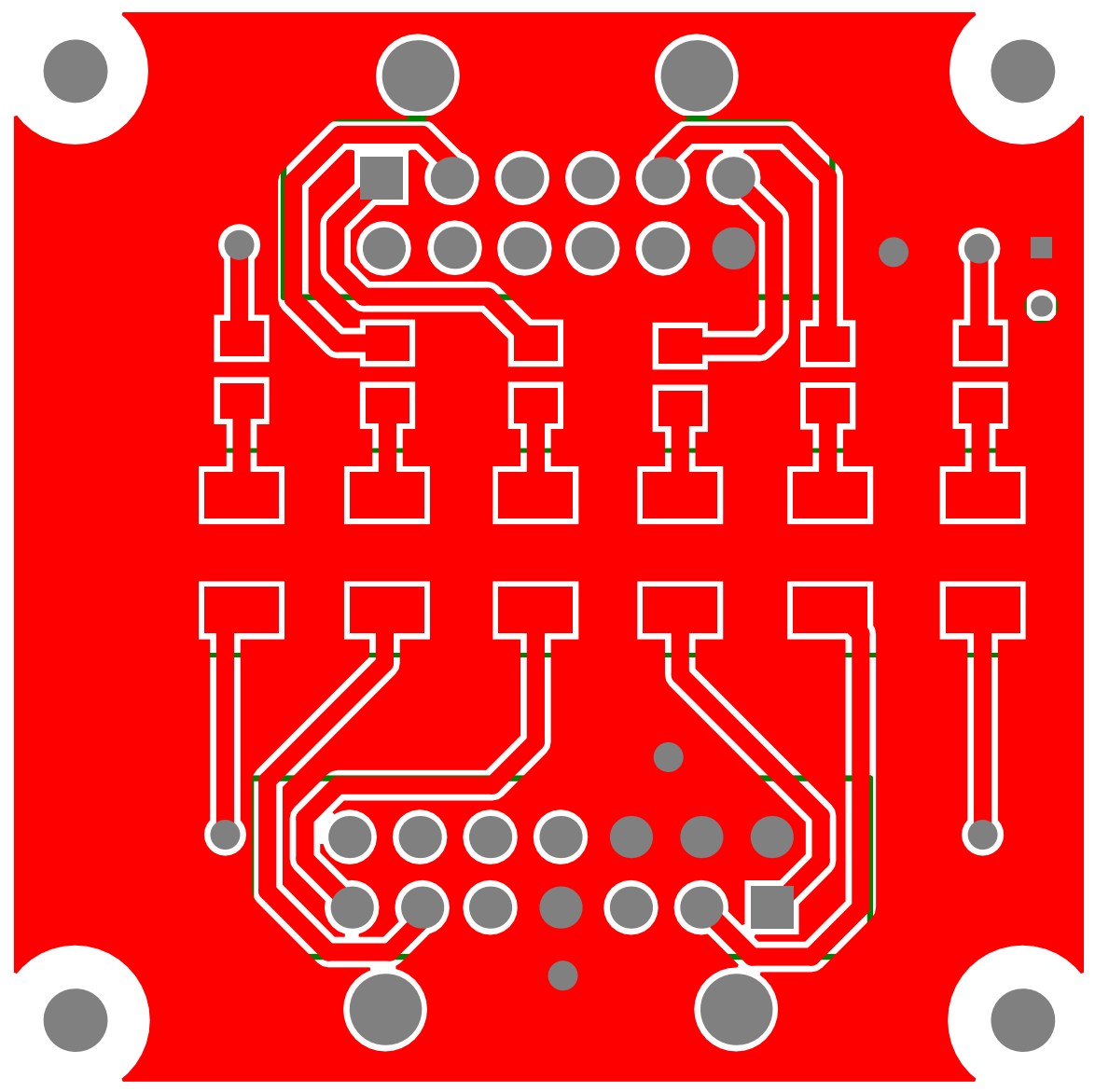


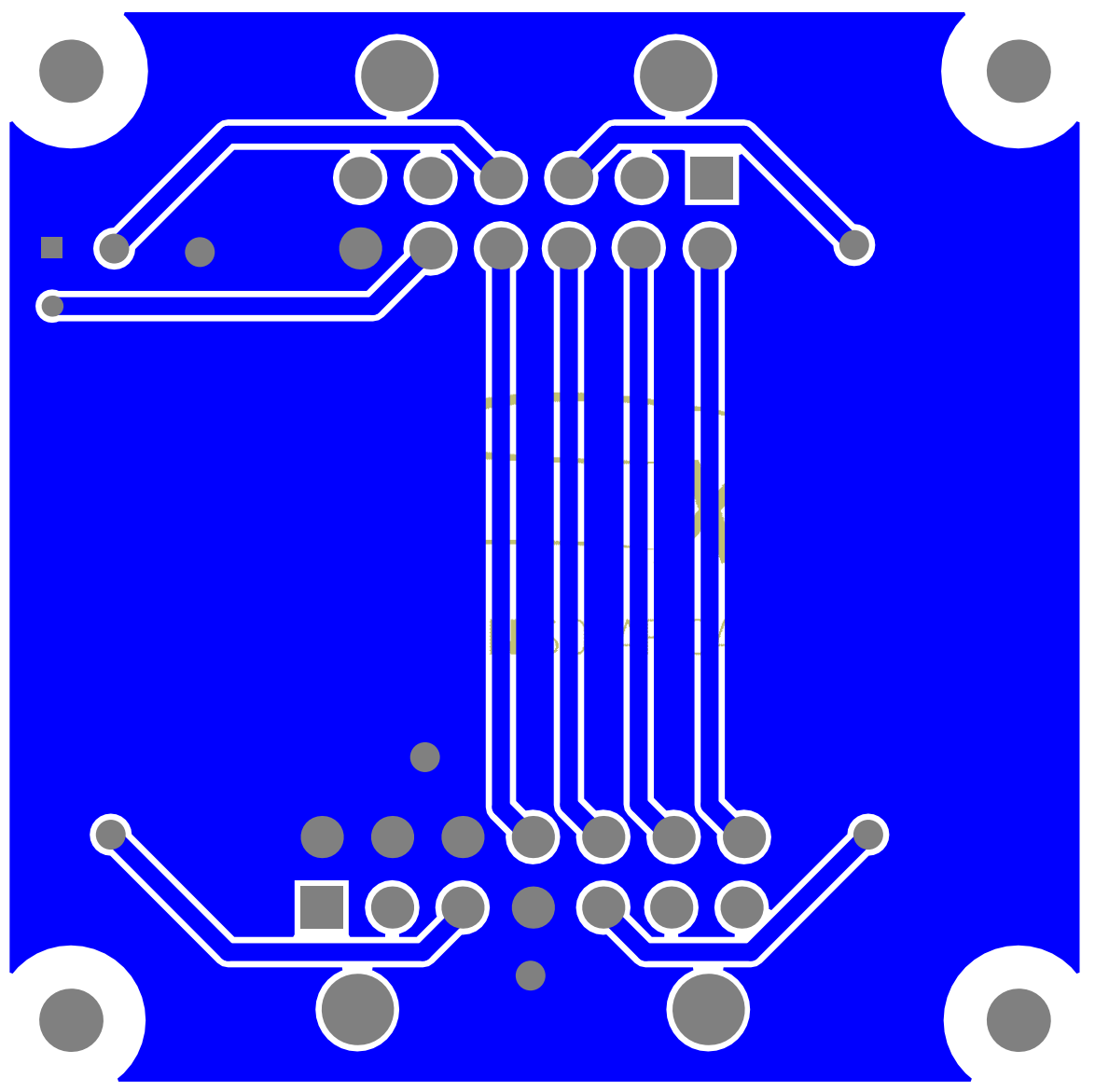
Project: ***MSXIV_BatteryModuleConnectorBoard.Pr***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Ricky Huang		
Size: Letter	Revision: 3.0	
Date: 2020-04-09	Sheet * of *	Website: uwmidsun.com

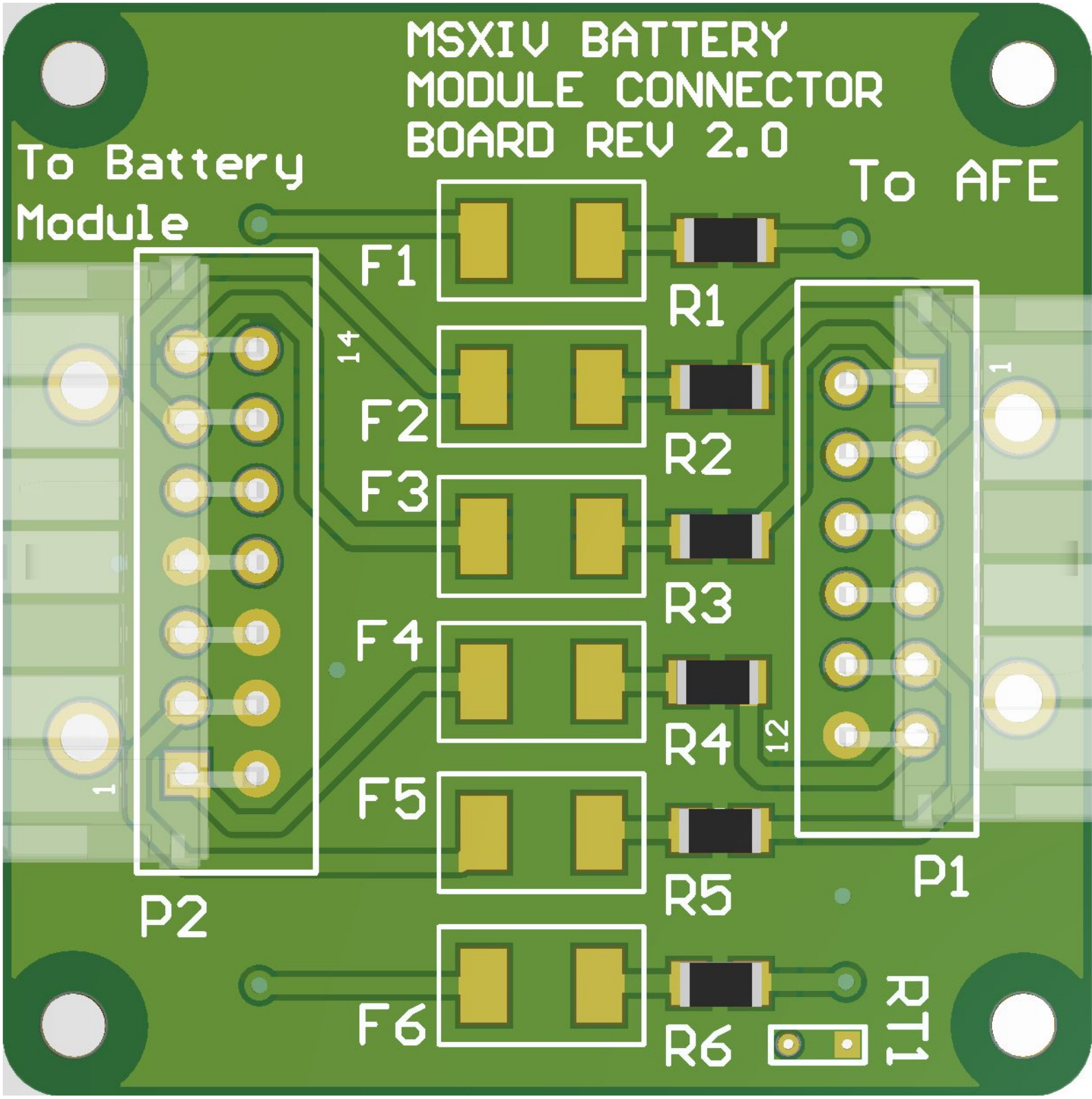
Bill of Materials

Project:	XIV_BatteryModuleConnectorBoard.PrjPcb
Revision:	3.0
Project Lead:	Ricky Huang
Generated On:	2020-04-09 11:21 AM
Production Quantity:	1
Currency	USD
Total Parts Count:	15

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
FUSE 500MA LCSC	F1, F2, F3, F4, F5, F6	Shenzen JDT Fuse	JFC2410-0500FS	LCSC	C136360		6	
CONN 12POS HEADER R/A MICROFIT 3MM	P1	Molex	430451200	Digi-Key	WM1818-ND		1	
CONN 14POS HEADER R/A MICROFIT 3MM	P2	Molex	430451400	Digi-Key	WM4723-ND		1	
RES 2 OHM 1% 1/4W 1206	R1, R2, R5, R6	TyoHM	RMC120621%N	LCSC	C269587		4	
RES 1 OHM 5% 1/4W 1206	R3, R4	TyoHM	RMC120615%N	LCSC	C325901		2	
NTC THERMISTOR 10K 1% BEAD	RT1			Digi-Key	490-8601-ND		1	
							Total:	$ -






MSXIV BATTERY
MODULE CONNECTOR
BOARD REV 2.0
To Battery
Module
To AFE
F1
F2
F3
F4
F5
F6
R1
R2
R3
R4
R5
R6
RT1
P1
P2
14
1
12
1

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXI\

Warnings 0
Rule Violations 12

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=20mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	8
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	12

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mi

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(1161.417mil,1700.787mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(693.417mil,1700.787mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_BatteryModuleConnectorBoard\MSXIV_BatteryModule

Warnings 0
Rule Violations 12

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=20mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	8
Silk to Silk (Clearance=10mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	12

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mil

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(1161.417mil,1700.787mil) on Multi-Layer And Track (468.063mil,1629.213mil)(1389.323mil,1629.213mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(693.417mil,1700.787mil) on Multi-Layer And Track (468.063mil,1629.213mil)(1389.323mil,1629.213mil) on Top Overlay [Top Overlay] to [Top
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track (1710.63mil,1285.433mil)(1710.63mil,1442.913mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track (1710.63mil,1442.913mil)(1769.685mil,1442.913mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track (1769.685mil,1285.433mil)(1769.685mil,1442.913mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track (1710.63mil,1285.433mil)(1710.63mil,1442.913mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track (1710.63mil,1285.433mil)(1769.685mil,1285.433mil) on Top Overlay [Top Overlay] to
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track (1769.685mil,1285.433mil)(1769.685mil,1442.913mil) on Top Overlay [Top Overlay] to