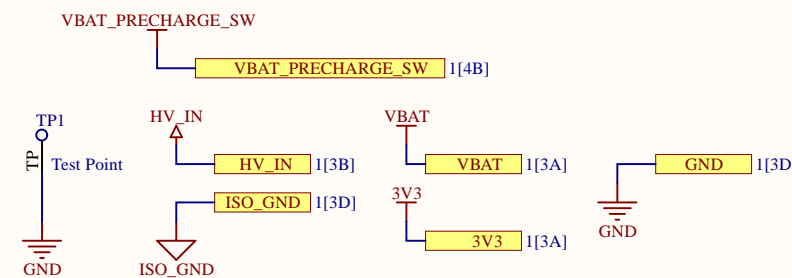
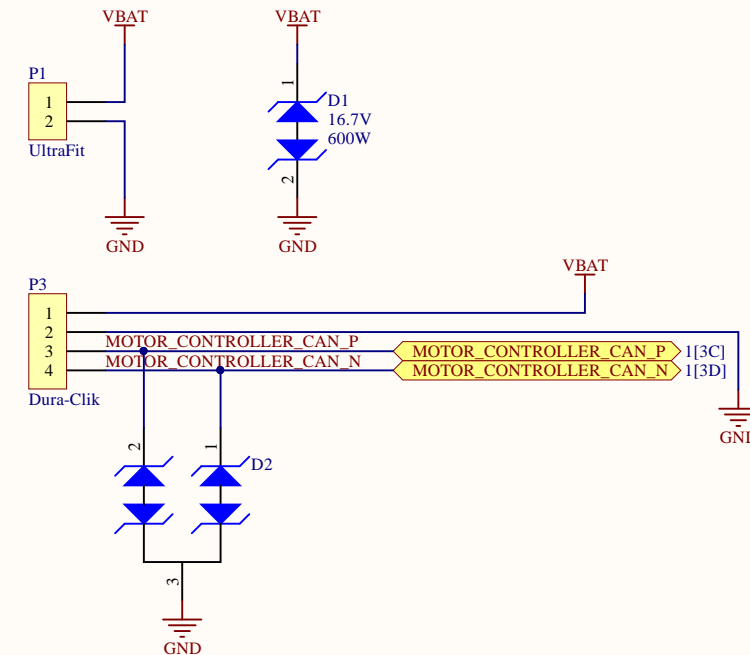
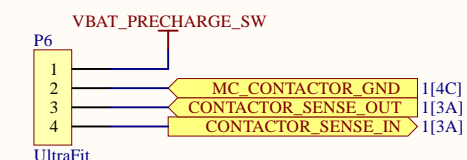
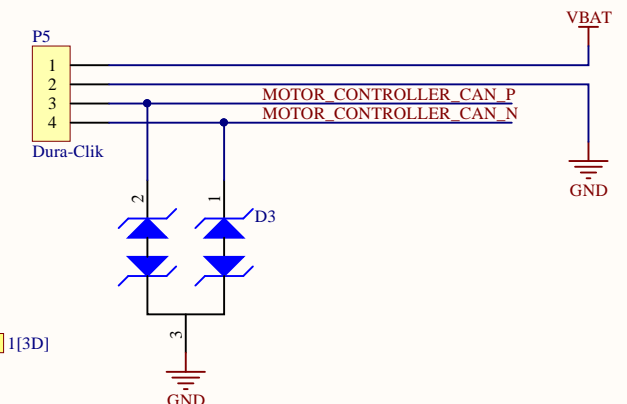
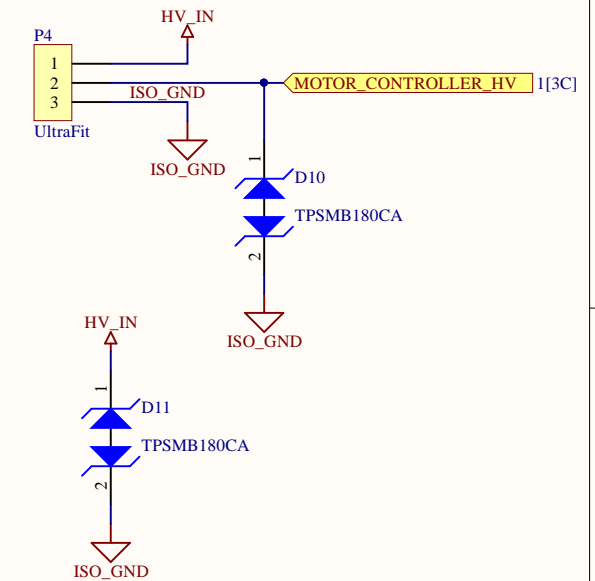


Connectors

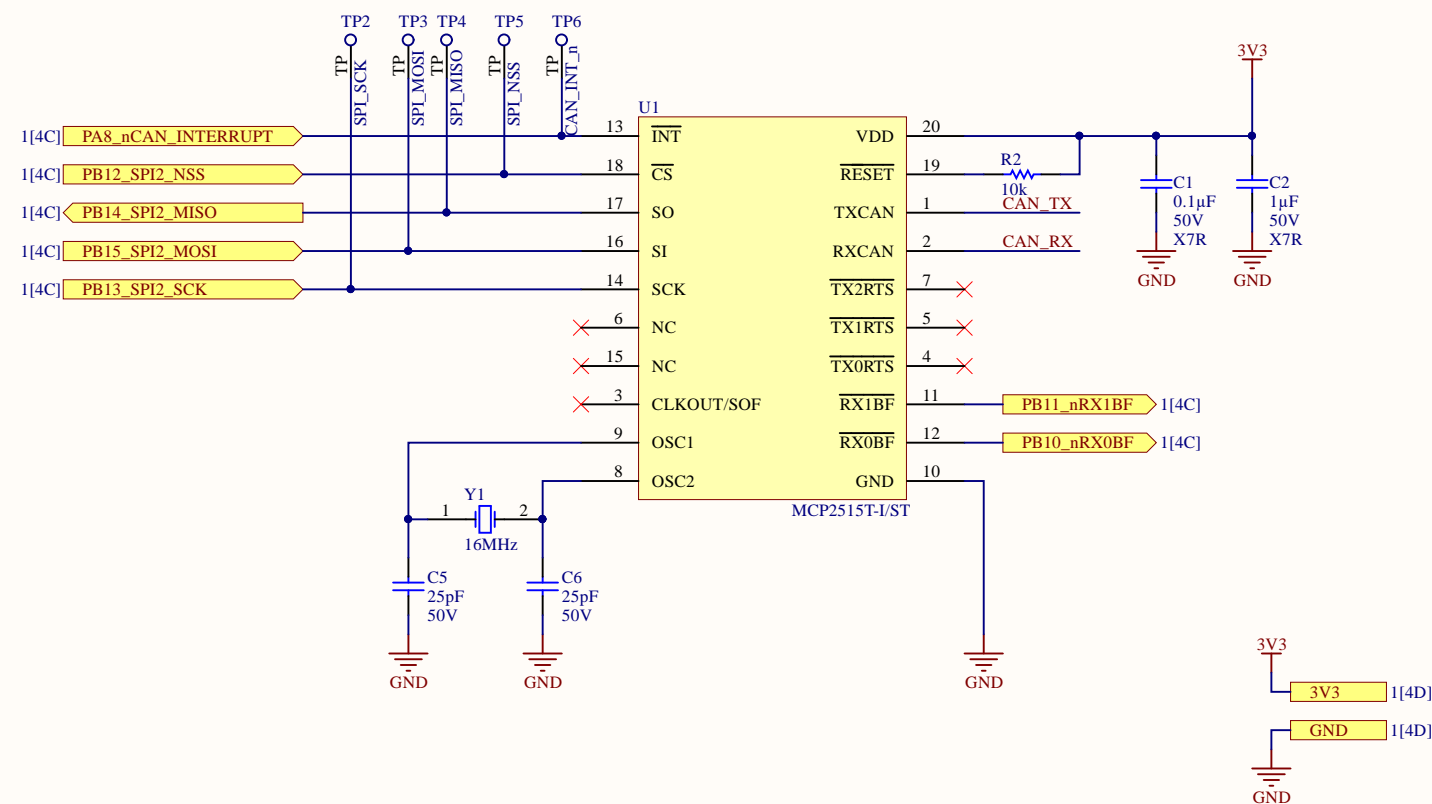


HV Connector

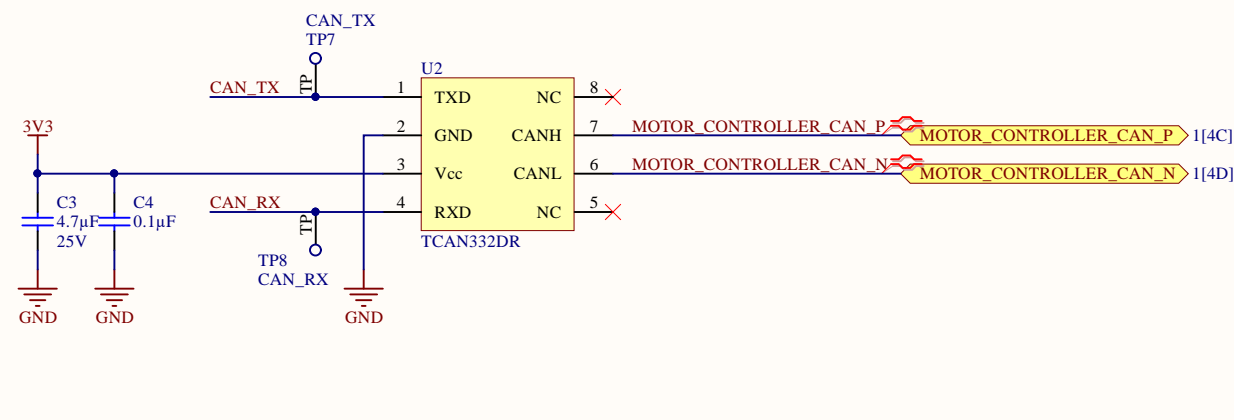


PROJECT	PreCharge.PrjPcb		
DOCUMENT	Motor Interface - Connectors		
PART NUMBER	MS14005	VARIANT	[No Variations]
DRAWN BY	Taiping Li, James Lin	REVISION	5.0
LAST MODIFIED	2019-12-01	SHEET	2 OF 6

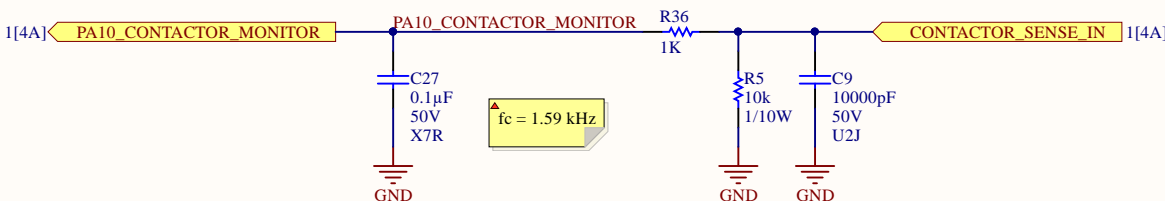
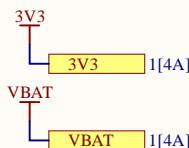
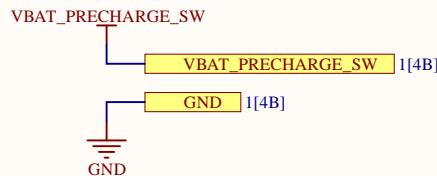
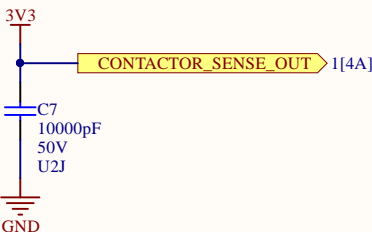
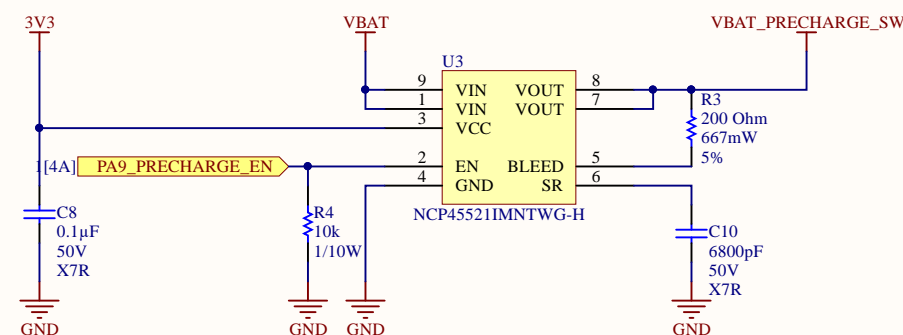
CAN Controller



CAN Transceiver



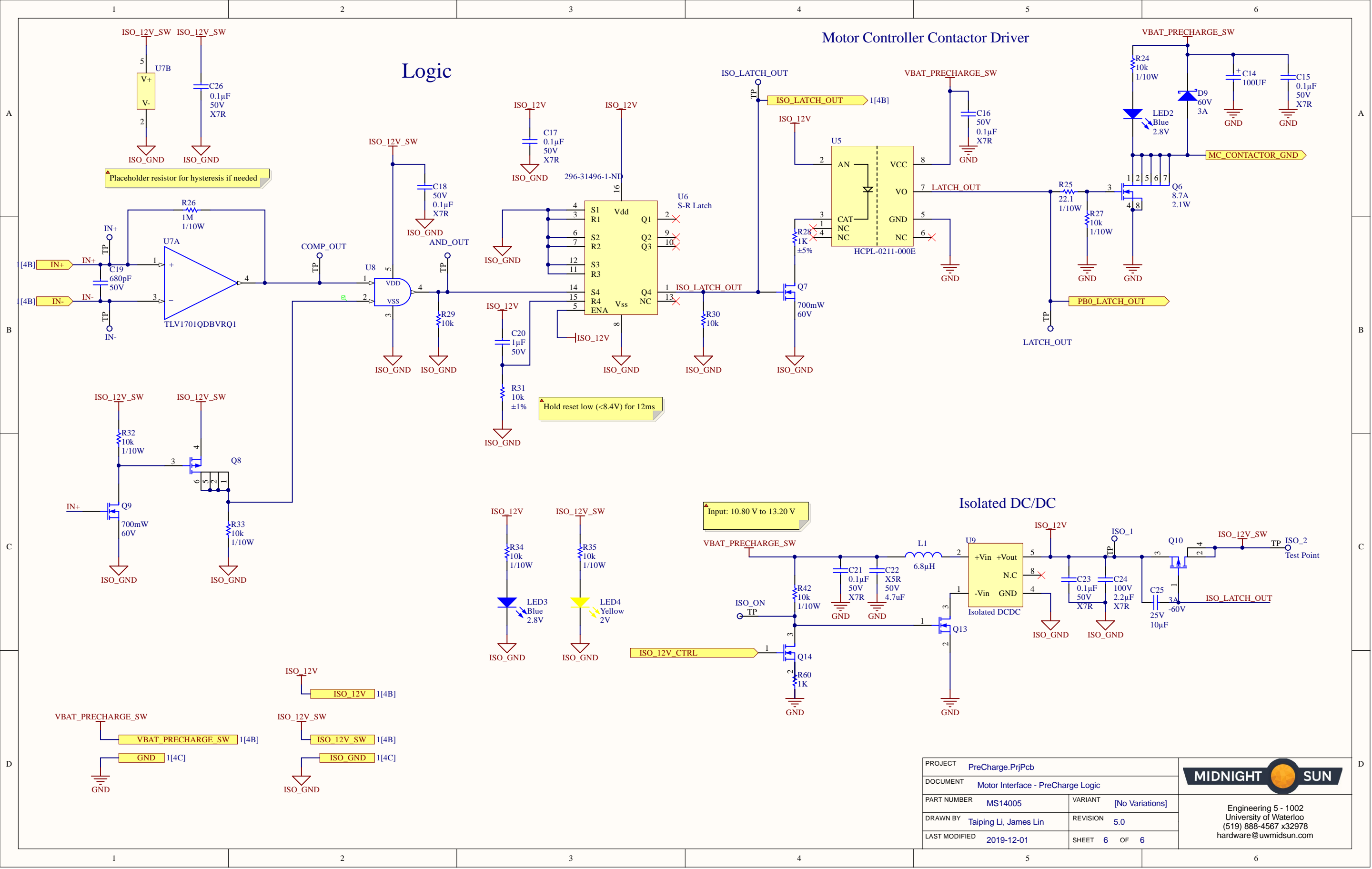
Precharge Control

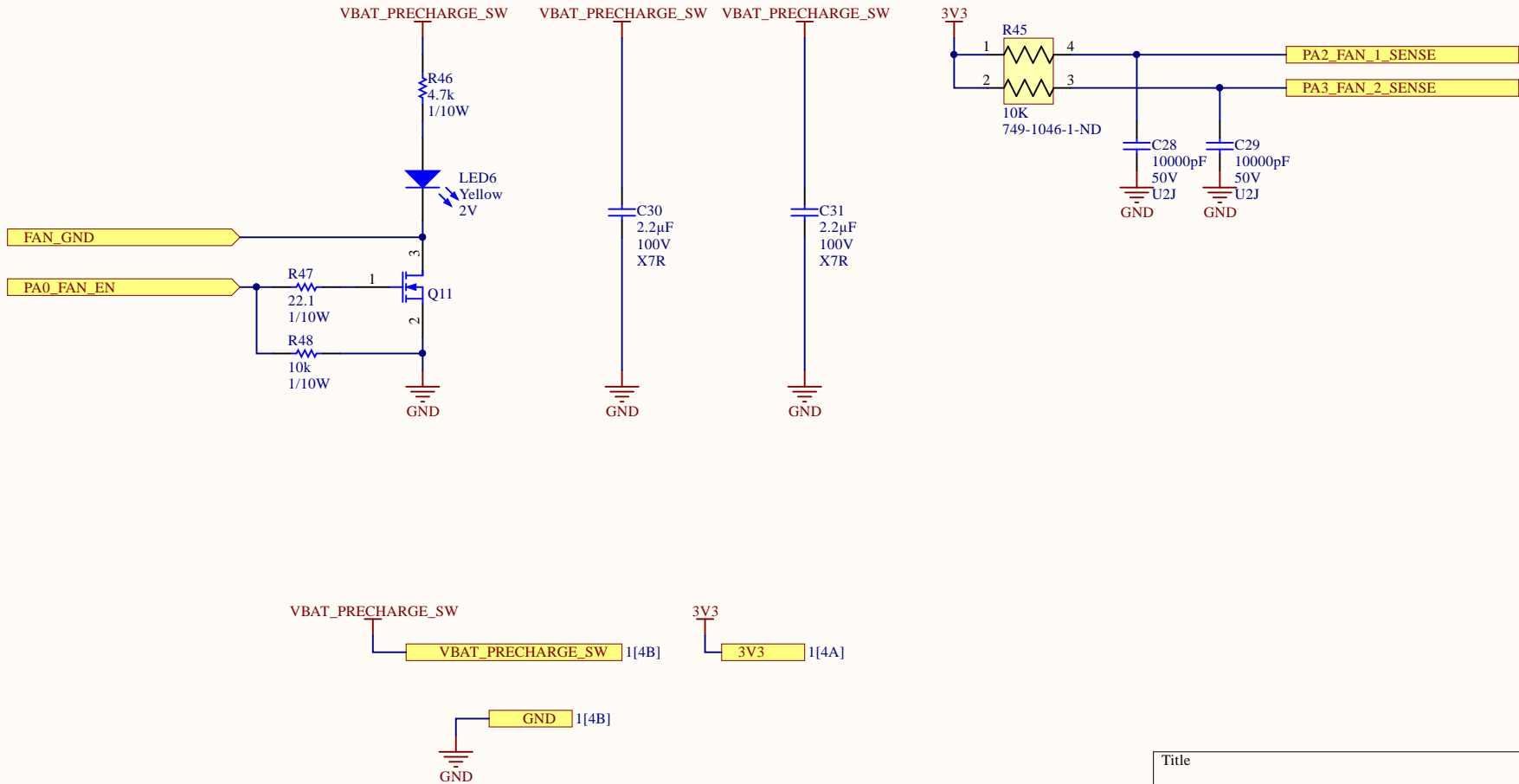


PROJECT	PreCharge.PrjPcb	
DOCUMENT	Motor Interface - PreCharge Interface	
PART NUMBER	MS14005	VARIANT [No Variations]
DRAWN BY	Taiping Li, James Lin	REVISION 5.0
LAST MODIFIED	2019-12-01	SHEET 4 OF 6

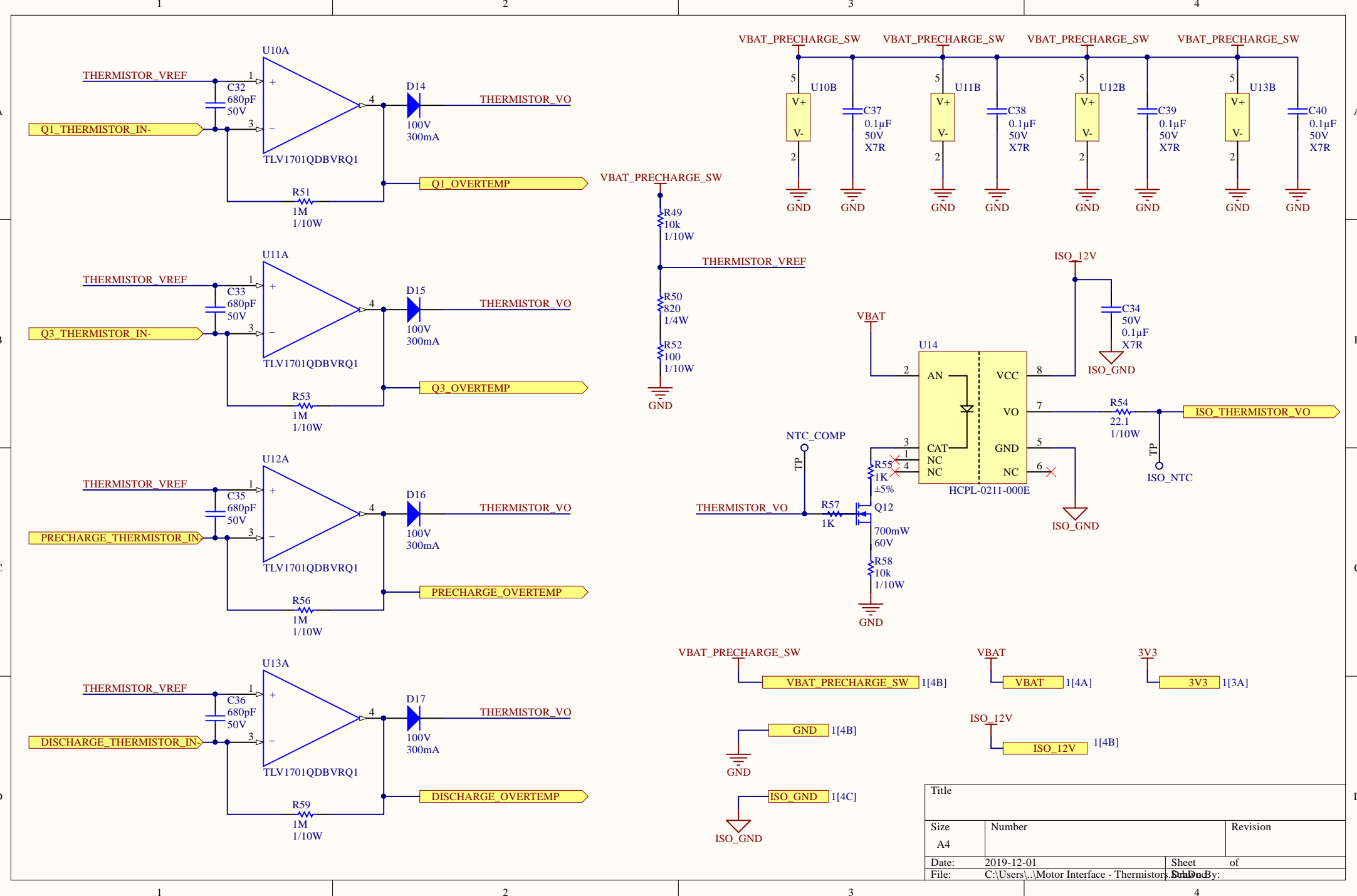


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University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com





Title		
Size	Number	Revision
A4		
Date:	2019-12-01	Sheet of
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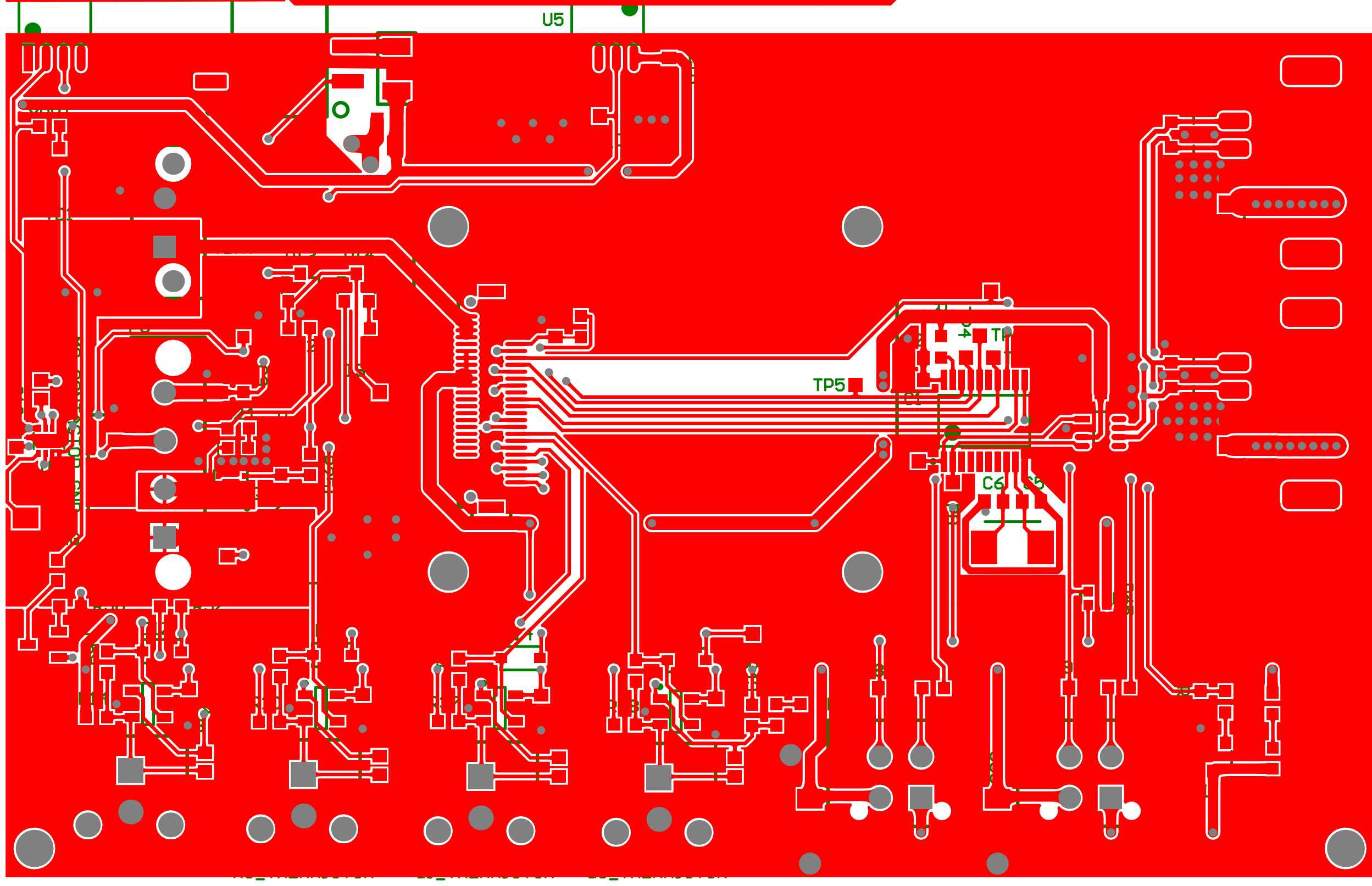
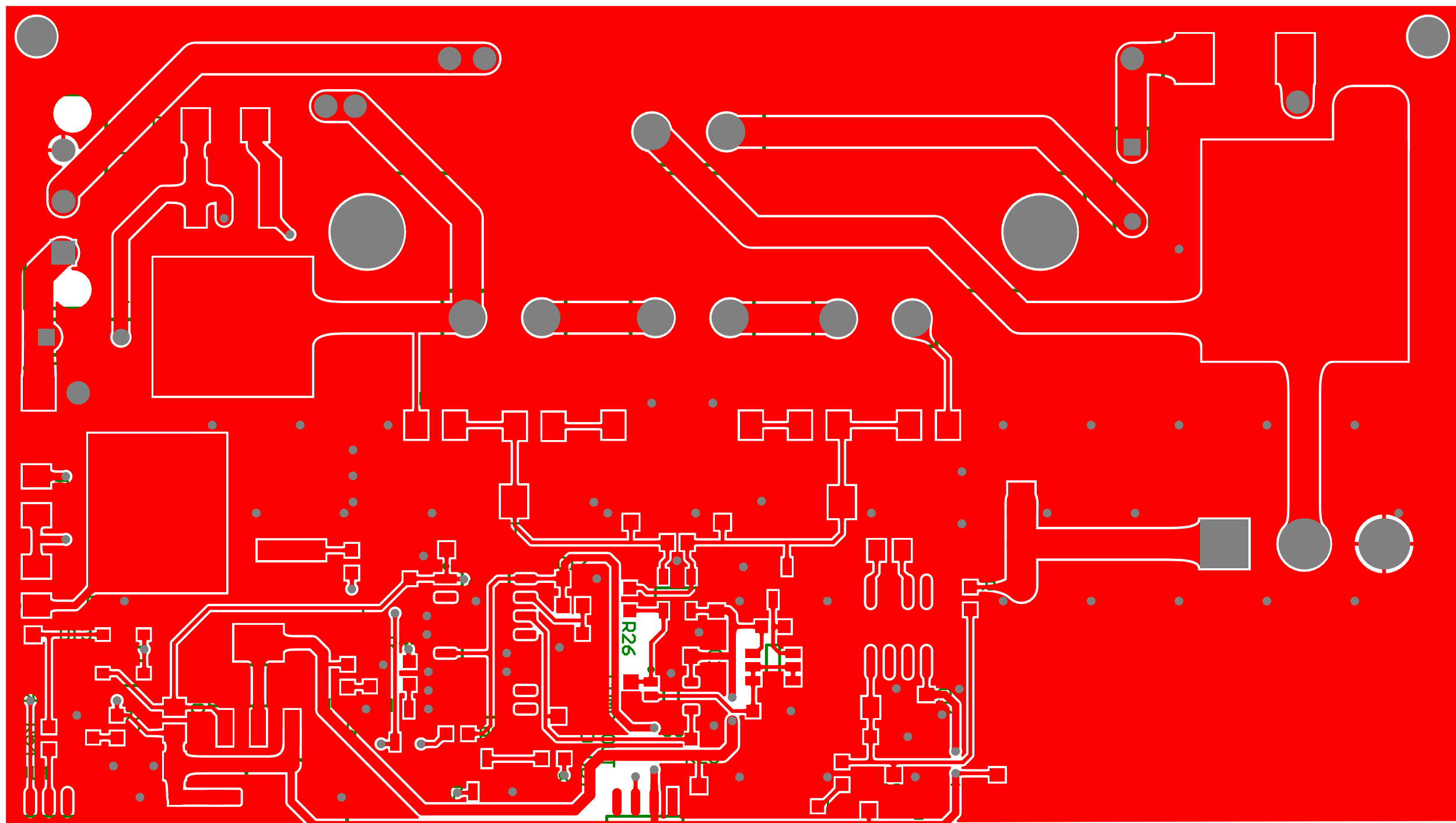


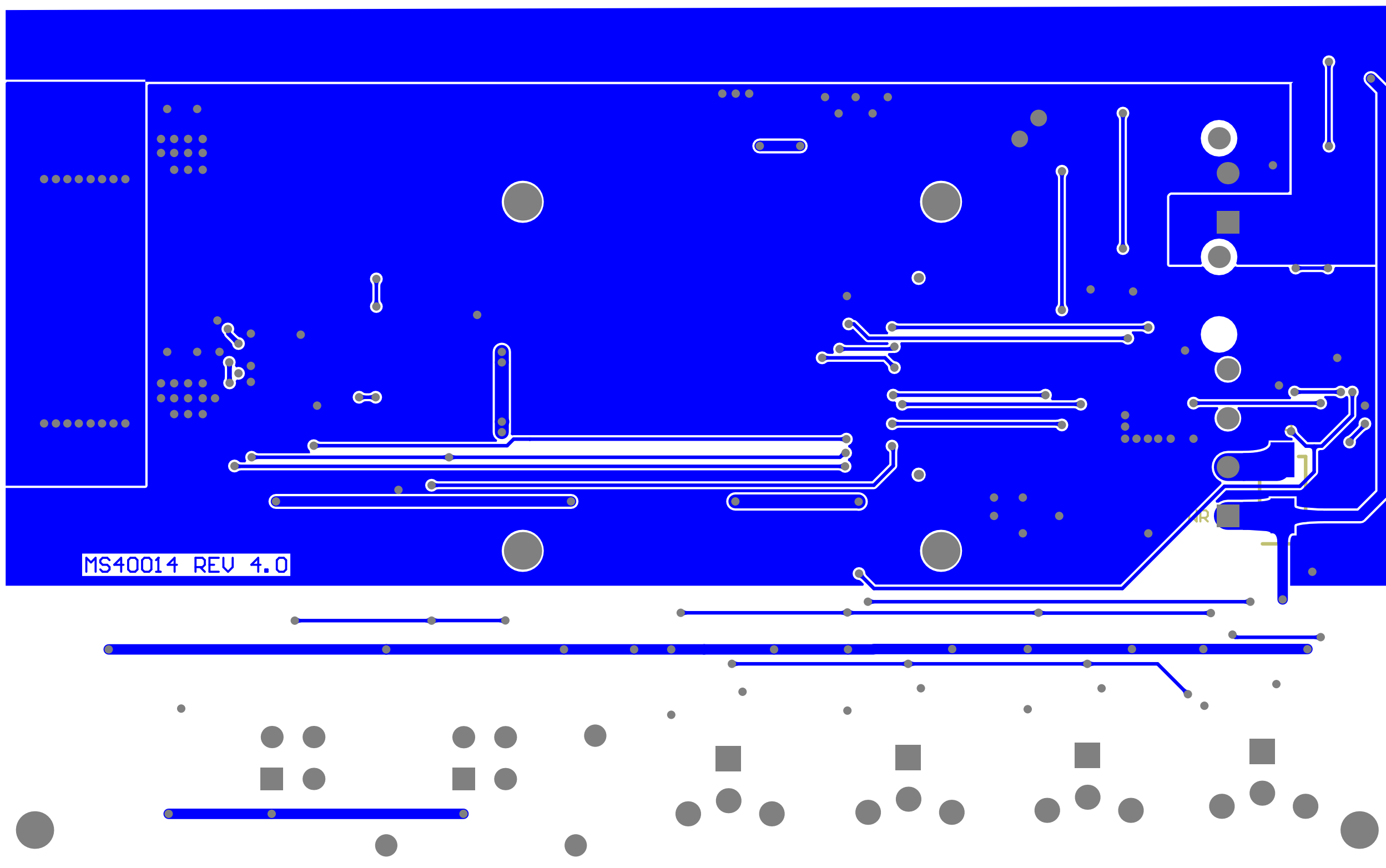
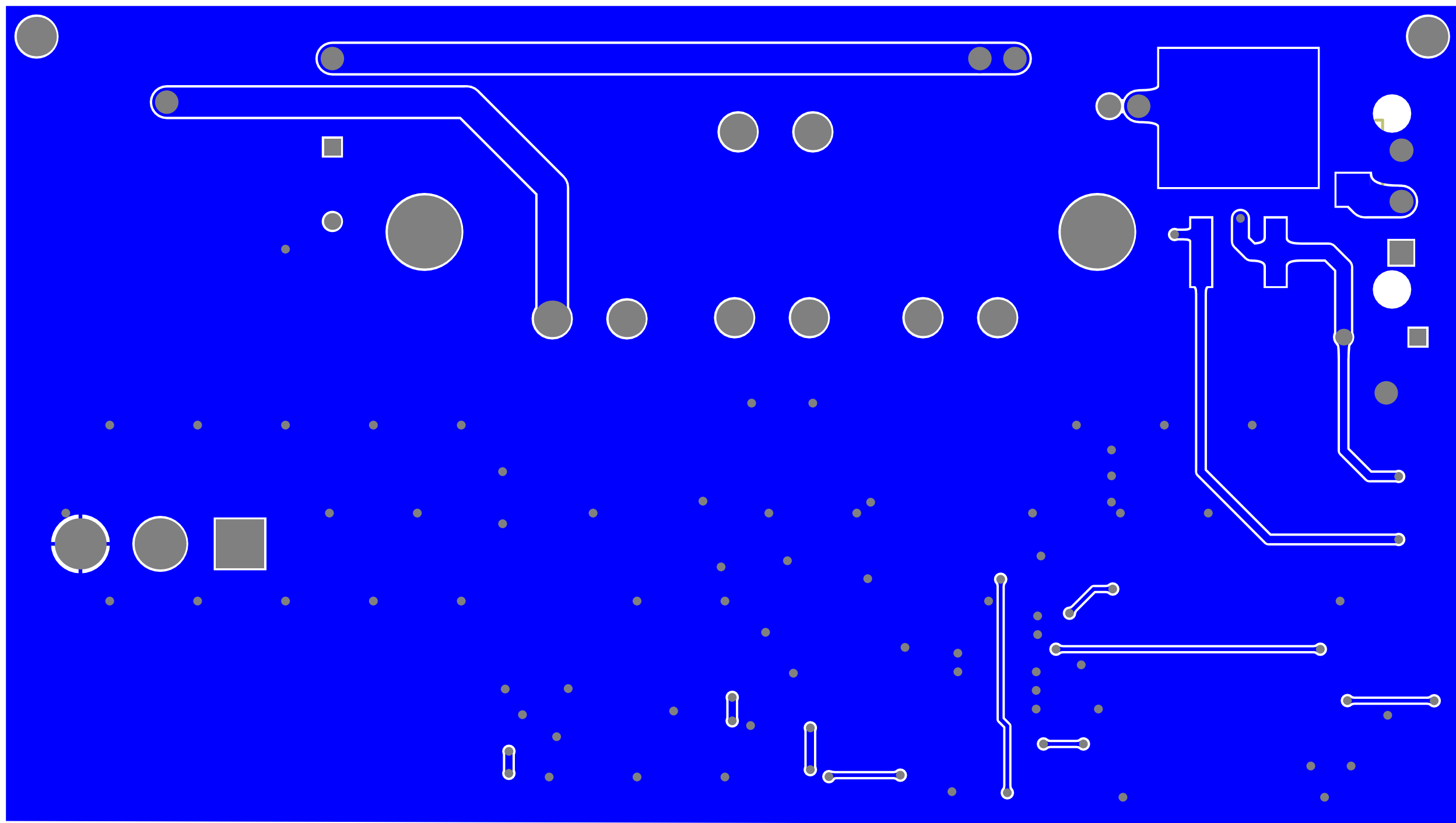
Bill of Materials

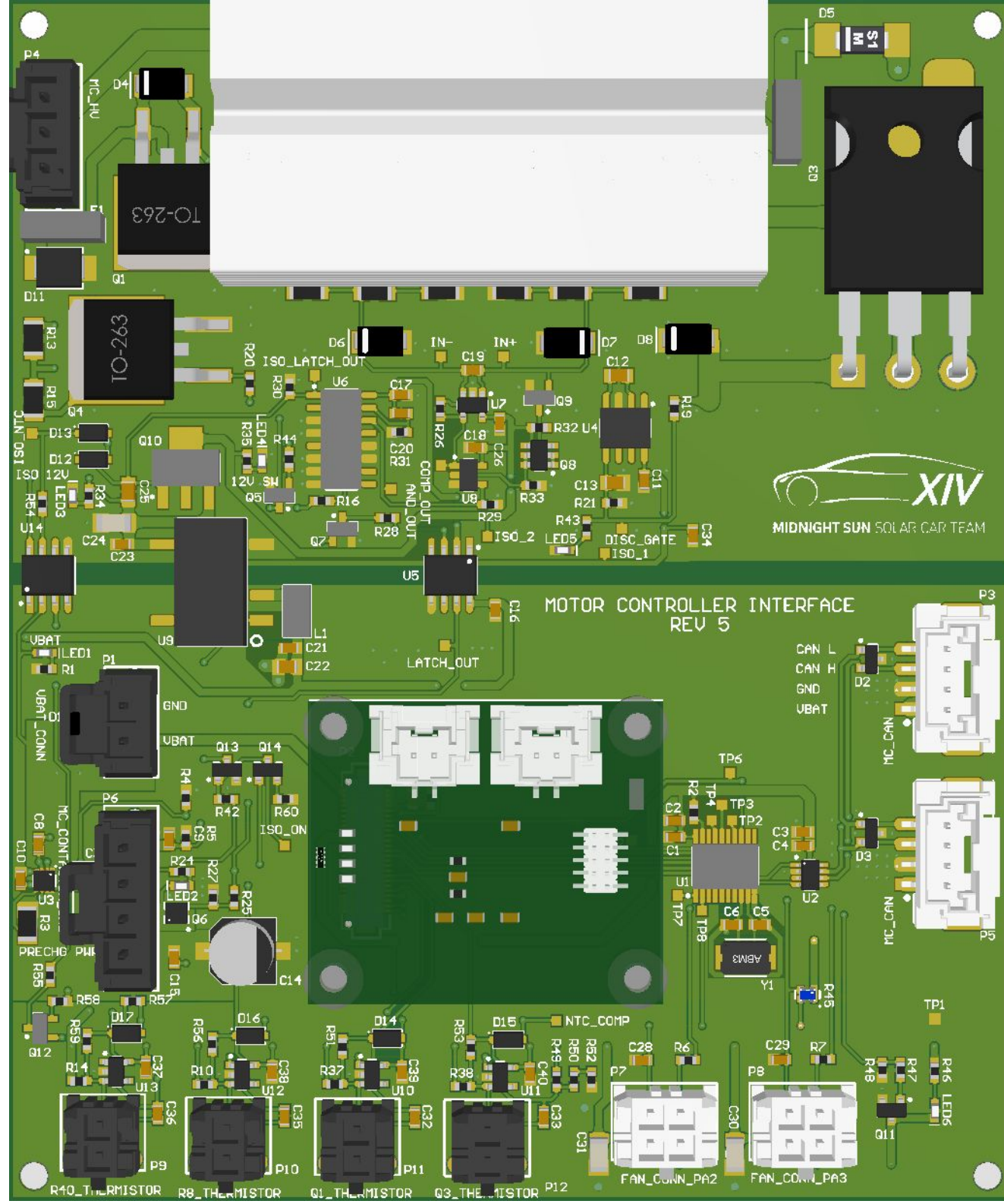
Project:	PreCharge.PrjPcb
Revision:	5.0
Project Lead:	Talping Li, James Lin
Generated On:	2019-12-01 10:06 PM
Production Quantity:	1
Currency:	USD
Total Parts Count:	170

MIDNIGHT SU

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1
CAP CER 0.1UF 50V 10% X7R 0603	C16, C17, C18, C21, C23, C26, C27, C34, C35	AVX Corporation	060355C104KAT2A	Digi-Key	478-50524-1-ND	
CAP CER 1UF 50V 10% X7R 0603	C2	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-32471-1-ND	
CAP CER 4.7UF 25V 10% X5R 0603	C3	Murata Electronics North America	GRM188R61E475KE1TD	Digi-Key	490-72031-1-ND	
CAP CER 25PF 50V ±5% COGNF0 0603	C5	C6		Digi-Key	1276-2444-1-ND	
CAP CER 10NF 50V 5% X7R 0603	C7, C8, C28, C29	KEMET	C0603C103J5JAC7867	Digi-Key	398-13384-1-ND	
CAP CER 6800PF 50V 10% X7R 0603	C10	Samsung Electro-Mechanics	CL10B822KB85FNC	Digi-Key	1276-21031-1-ND	
CAP CER 2.2UF 25V 10% X5R 0603	C11	Murata Electronics North America	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	
CAP CER 10UF 25V 10% X5R 0603	C12, C13, C25			Digi-Key	490-85231-1-ND	
CAP ALUM 100UF 35V 30% SMD	C14	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951-1-ND	
CAP CER 680PF 50V C0G 0603	C19, C32, C33, C35, C36			Digi-Key	1276-18201-1-ND	
CAP CER 4.7UF 50V 10% X5R 0805	C22	Murata Electronics North America	GRT218R61H475ME13L	Digi-Key	490-12395-1-ND	
CAP CER 2.2UF 100V 20% X7R 1206	C24, C30, C31	Murata Electronics North America	GRM31CR72A225MA73L	Digi-Key	490-12773-1-ND	
DIODE TVS 15V1WM 24A VCD 20-2144A (SMB)	D2	Fairchild/ON Semiconductor	SMB1J5CA	Digi-Key	SMB1J5CAFSCT-ND	
DIODE TVS 24VWM70VC SOT23	D2, D3	Neptunia USA Inc.	PESD1CAN215	Digi-Key	1727-3817-1-ND	
DIODE ZENER 16V 5W D20-2144A (SMB)	D6, D6, D7, D8			Digi-Key	3MBJ53338-1PMSCT-ND	
DIODE GEN PURP 800V 3A SMC	D5			Digi-Key	589CDN1-1-ND	
DIODE SCHOTTKY 60V 3A SMD	D9	Diodes Incorporated	B360A-13-F	Digi-Key	B360A-FD1C-1-ND	
DIODE TVS 154V 246V D20-2144A (SMB)	D10, D11			Digi-Key	F10356CT-ND	
DIODE GEN PURP 100V 300MA SOD123	D12, D13, D14, D15, D16, D17			Digi-Key	1N4148BV1-FD1C1-ND	
FUSE 3A 250VAC450VDC RADIAL	F1, F2			Digi-Key	283-2768-1-ND	
HEAT SINK 4x7-0.247-duplicate	HS			Digi-Key	345-1574-ND	
IND 6.8uH 260mA 20% 1210	L1	TDK Corporation	NLFV32T-6R8MEF	Digi-Key	445-15776-1-ND	
LED GREEN CLEAR 2V 0603	LED1			Digi-Key	732-4860-1-ND	
LED BLUE CLEAR 2.8V 0603	LED2, LED3	Lite-On Inc.	LTST-C193T8TKT6A	Digi-Key	160-1827-1-ND	
LED YELLOW CLEAR 2.1V 0603	LED4, LED6			Digi-Key	732-49811-1-ND	
LED RED CLEAR 2V 0603	LED5			Digi-Key	732-4978-1-ND	
FUSE HOLDER P-TON RADIAL	M2, M3			Digi-Key	283-2356-1-ND	
CONN 2POS ULTRA-FIT 0.138"	P1	Moblex, LLC	1722861302	Digi-Key	WM11673-ND	
CONN 50POS Bergstak Plug 0.02"	P2	Amphenol FCI	10132797-055100LF	Digi-Key	608-5226-1-ND	
CONN 4POS DURA-CLIK 0.079"	P3, P5			Digi-Key	WM1066CT-ND	
CONN 5POS ULTRA-FIT 0.138"	P4			Digi-Key	WM11702-ND	
CONN 4POS ULTRA-FIT 0.138"	P6	Moblex, LLC	1722871104	Digi-Key	WM11703-ND	
CONN 4POS MICRO-FIT 3mm	P7, P8			Digi-Key	WM1066-ND	
CONN 2POS MICRO-FIT 3mm	P9, P10, P11, P12			Digi-Key	WM1065-ND	
MOSFET P-CH 500V 10A 300W TO263	Q1, Q2			Digi-Key	IXTA10P50P-ND	
MOSFET DEPLETION N-CH 500V 6A TO247	Q3			Digi-Key	IXTH6N5002-ND	
MOSFET N-CH 650V 8A X2 TO-263	Q4			Digi-Key	IXTA8N65C2-ND	
MOSFET N-CH 60V 310MA SOT23	Q5, Q7, Q9, Q12			Digi-Key	DMN603L-70JCT-ND	
MOSFET N-CH 30V 8.7A 2.1W EP09M (2x2)	Q6	Infineon Technologies	IRLH56342T1RPF8	Digi-Key	RLH56342T1RPFCT-ND	
MOSFET P-CH 30V 4A 1.6W SOT-23-6	Q8	STMicroelectronics	STT4P3LL4L	Digi-Key	497-15521-1-ND	
MOSFET P-CH 60V 3A SOT23	Q10			Digi-Key	KPQ6347120AIDXRND	
MOSFET N-CH 30V 6.2A 0.9W SOT23	Q11, Q13, Q14			Digi-Key	DMN603L-70JCT-ND	
RES 10K OHM 1% 1/10W 0603	R1, R24, R27, R29, R30, R31, R32, R33, R34, R35	Yageo	RC0603FR-0710KL	Digi-Key	311-10K0RCT-ND	
RES 200 OHM 5% 23W 1206	R3			Digi-Key	P20A0ALCT-ND	
RES 22 1 OHM 1% 1/10W 0603	R6, R7, R20, R25, R47, R54	Yageo	RC0603FR-0722RL	Digi-Key	311-220RCT-ND	
RES 1K OHM 15W 1% T0126	R8, R9, R39	Caddock Electronics Inc.	MP915-1.00K-1%	Digi-Key	MP915-1.00KFD-ND	
RES SMD 470K OHM 0.1% 1/4W 1206	R11, R12, R15			Digi-Key	RG32P470KRBKDR-ND	
RES SMD 28.4K OHM 0.1% 1/4W 1206	R13, R17			Digi-Key	P28.4KCFCT-ND	
RES SMD 33K OHM 0.1% 1/4W 1206	R18			Digi-Key	YAG2033R1-ND	
RES 40.2 OHM 0.5% 1/10W 0603	R19	Yageo	RT0603DRE0740R2L	Digi-Key	311-2576-1-ND	
RES SMD 0 OHM JUMPER 1/4W 1206	R22			Digi-Key	541-0.0ECT-ND	
RES SMD 2K OHM 0.1% 1/4W 1206	R23			Digi-Key	P2.0K0RCT-ND	
RES 100K OHM 1% 1/10W 0603	R26, R51, R53, R56, R59	Yageo	RC0603FR-071ML	Digi-Key	311-100K0RCT-ND	
RES 1K OHM 5% 1/10W 0603	R28, R36, R44, R45, R57, R60			Digi-Key	311-1.0K0RCT-ND	
RES 5K OHM 25W 1% T0220	R40	Caddock Electronics Inc.	MP925-5.00K-1%	Digi-Key	MP925-5.00KFD-ND	
RES 4.7K OHM 1% 1/10W 0603	R43, R46			Digi-Key	311-4.7K0RCT-ND	
RES ARRAY 10K OHM 0.1% 2RES 0606	R45			Digi-Key	Y49-1046-1-ND	
RES 820 OHM 5% 1/4W 0603	R50	Rohm Semiconductor	ESR03E2PJ821	Digi-Key	RH820DCT-ND	
RES 100 OHM 1% 1/10W 0603	R52	Yageo	RC0603FR-07100RL	Digi-Key	311-100R0RCT-ND	
TestPoint	TP1			Digi-Key	MCP2515T-1JSTCT-ND	
CAN SPI CONTROLLER MCP2515T-JST 20-TSSOP	U1			Digi-Key	296-43711-1-ND	
IC CAN Transceiver TCAN332DR	U2			Digi-Key	46521MM1YVCHDSBDR-ND	
IC LOAD SWITCH AS774 10-5A 30PN	U3			Digi-Key	CZ7686-007A13C1-ND	
IC REG SVR 5V 1A CAN INTP 20MA RSOC	U4					







Design Rules Verification Report

Filename : C:\Users\James\Documents\hardware-master\MSXII_PreChargeController\

Warnings 0
Rule Violations 180

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=10mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	117
Silk to Silk (Clearance=0.254mm) (All),(All)	60
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	3
Height Constraint (Min=0mm) (Max=200mm) (Preferred=12.7mm) (All)	0
Total	180

Silk To Solder Mask (Clearance=0.178mm) (IsPad), (All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C1-2(65.557mm,16.374mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-1(39.779mm,60.525mm) on Top Layer And Text "C17
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-2(38.429mm,60.525mm) on Top Layer And Text "C17
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C2-2(65.575mm,18mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C37-1(13.689mm,-7.304mm) on Top Layer And Text "C37
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C37-2(13.689mm,-5.954mm) on Top Layer And Text "C37
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C38-1(26.285mm,-7.72mm) on Top Layer And Text "C38
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C38-2(26.285mm,-6.37mm) on Top Layer And Text "C38
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C39-1(39.215mm,-7.77mm) on Top Layer And Text "C39
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C39-2(39.215mm,-6.42mm) on Top Layer And Text "C39
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad C40-1(51.85mm,-7.97mm) on Top Layer And Text "U11"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C7-2(8.333mm,13.35mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.098mm < 0.178mm) Between Pad DISC_GATE-TP(61.02mm,47.15mm) on Top Layer And Text
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad LED2-1(18mm,11.5mm) on Top Layer And Text "LED2
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad LED2-2(16.5mm,11.5mm) on Top Layer And Text "LED2
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P10-0(18.9mm,-16.09mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P10-0(18.9mm,-16.09mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P10-0(24.9mm,-16.09mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P10-0(24.9mm,-16.09mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P11-0(31.746mm,-16.23mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P11-0(31.746mm,-16.23mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P11-0(37.746mm,-16.23mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P11-0(37.746mm,-16.23mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P12-0(44.65mm,-16.339mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P12-0(44.65mm,-16.339mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P12-0(50.65mm,-16.339mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P12-0(50.65mm,-16.339mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P3-7(95mm,25.55mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P3-7(95mm,38.75mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P5-7(95mm,21.25mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad P5-7(95mm,8.05mm) on Top Layer And Text "P5"
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P5-7(95mm,8.05mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P9-0(12.375mm,-15.799mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P9-0(12.375mm,-15.799mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P9-0(6.375mm,-15.799mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P9-0(6.375mm,-15.799mm) on Multi-Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q11-1(88.795mm,-9.873mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q11-2(86.995mm,-9.873mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q13-1(20.875mm,22.1mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q13-2(22.675mm,22.1mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q14-1(24.935mm,22.1mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q14-2(26.735mm,22.1mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Q5-2(26.025mm,51.635mm) on Top Layer And Text "12V SW
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-1(17.656mm,8.15mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-3(17.656mm,9.45mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-4(15.806mm,9.45mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-6(15.806mm,8.15mm) on Top Layer And Tract
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.178mm) Between Pad R15-2(2.492mm,58.695mm) on Top Layer And Text "ISO_NTC"

Silk To Solder Mask (Clearance=0.178mm) (IsPad), (All)

Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-1(47.2mm,60.65mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-2(46.25mm,60.65mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-3(45.3mm,60.65mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-4(45.3mm,58.35mm) on Top Layer And Trac
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-5(47.2mm,58.35mm) on Top Layer And Trac

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.055mm < 0.254mm) Between Arc (14.306mm,50.35mm) on Top Overlay And Text "C25"
Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Arc (4.65mm,13.45mm) on Top Overlay And Text "MC_CONTACTOR_GND"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (22.1mm,-17.55mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.165mm < 0.254mm) Between Text "1" (34.946mm,-17.69mm) on Top Overlay And Text "Q1_THERMISTOR"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (34.946mm,-17.69mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.052mm < 0.254mm) Between Text "1" (47.85mm,-17.799mm) on Top Overlay And Text "Q3_THERMISTOR"
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (47.85mm,-17.799mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (9.575mm,-17.259mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C15" (16.128mm,2.618mm) on Top Overlay And Text "R57"
Silk To Silk Clearance Constraint: (0.208mm < 0.254mm) Between Text "C25" (13.126mm,51.935mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.208mm < 0.254mm) Between Text "C25" (13.126mm,51.935mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.246mm < 0.254mm) Between Text "C38" (27.035mm,-6.017mm) on Top Overlay And Text "U12"
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "C40" (52.77mm,-6.17mm) on Top Overlay And Text "U11"
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "C7" (7.749mm,14.382mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D11" (1.667mm,70mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.222mm < 0.254mm) Between Text "D17" (10.339mm,-1.986mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D17" (10.339mm,-1.986mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.227mm < 0.254mm) Between Text "D2" (84.366mm,31.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.126mm < 0.254mm) Between Text "D4" (10.5mm,91.193mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "D7" (59.124mm,65.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "D8" (62.696mm,65.687mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.192mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.156mm < 0.254mm) Between Text "ISO_LAT CH_OUT" (25.475mm,63.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "ISO_ON" (25.18mm,16.712mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "LED1" (5.4mm,34.355mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.211mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.007mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.097mm < 0.254mm) Between Text "LED2" (15.825mm,10.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.095mm < 0.254mm) Between Text "LED4" (24.8mm,58.547mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.18mm < 0.254mm) Between Text "MC_CONTACTOR_GND" (5.005mm,19.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.136mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.117mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "P5" (96.83mm,6.152mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.177mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.173mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.217mm < 0.254mm) Between Text "Q5" (23.75mm,49.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "Q6" (18.356mm,7.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.242mm < 0.254mm) Between Text "R25" (23.342mm,10.85mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "R9" (49.363mm,75.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "U10" (38.288mm,-9.359mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.252mm < 0.254mm) Between Text "U10" (38.288mm,-9.359mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.103mm < 0.254mm) Between Text "U12" (25.349mm,-9.345mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.107mm < 0.254mm) Between Text "U12" (25.349mm,-9.345mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "U13" (12.725mm,-9.017mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "U13" (12.725mm,-9.017mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.232mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.147mm < 0.254mm) Between Text "U4" (57.2mm,56.82mm) on Top Overlay And Track

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "U6" (32.398mm,61.5mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.206mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "Q1_THERMISTOR" (30.2mm,-19.6mm) on Top
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Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "Q3_THERMISTOR" (42.6mm,-19.6mm) on Top
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Board Outline Clearance(Outline Edge): (0.117mm < 0.406mm) Between Board Edge And Text "R8_THERMISTOR" (17mm,-19.6mm) on Top
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