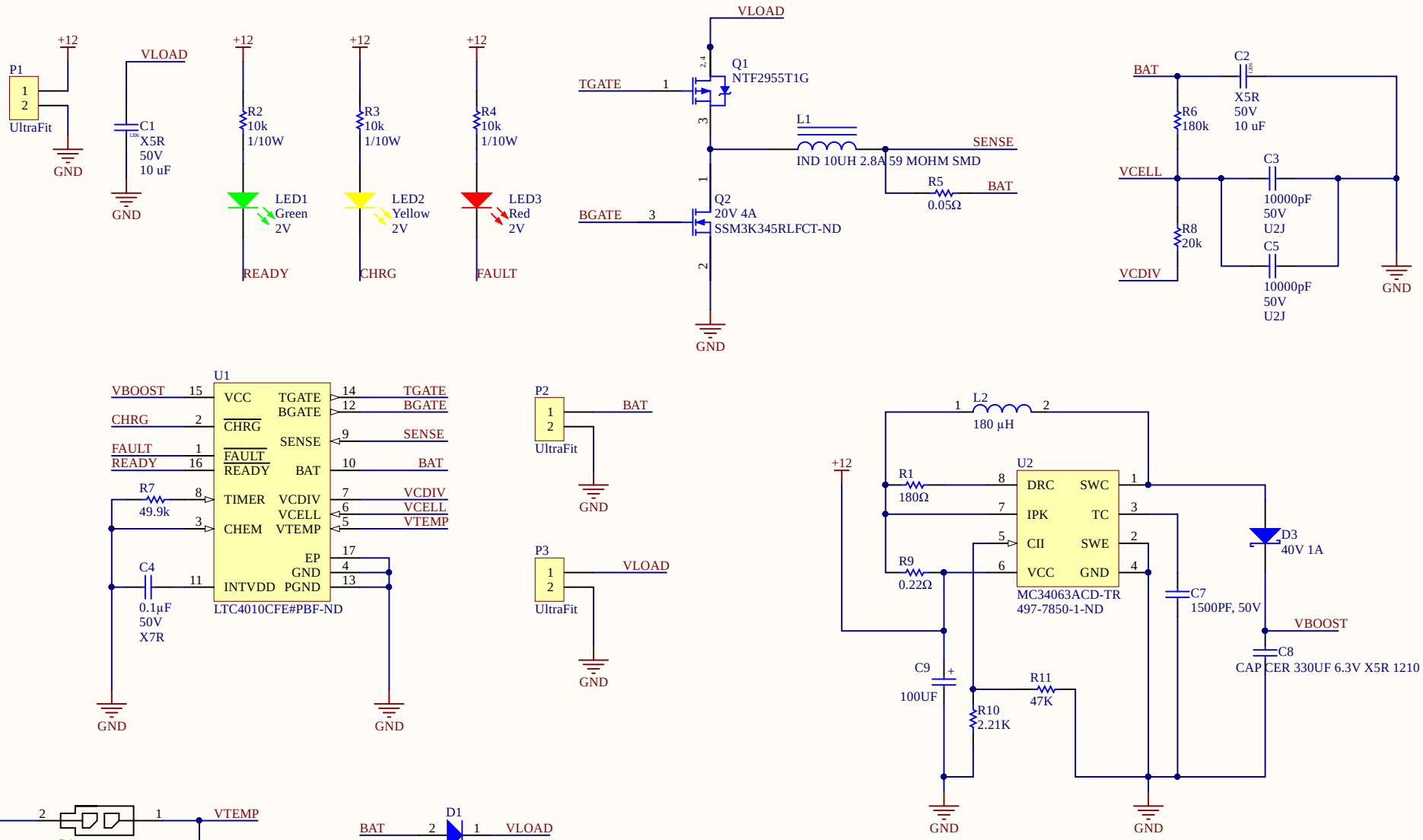
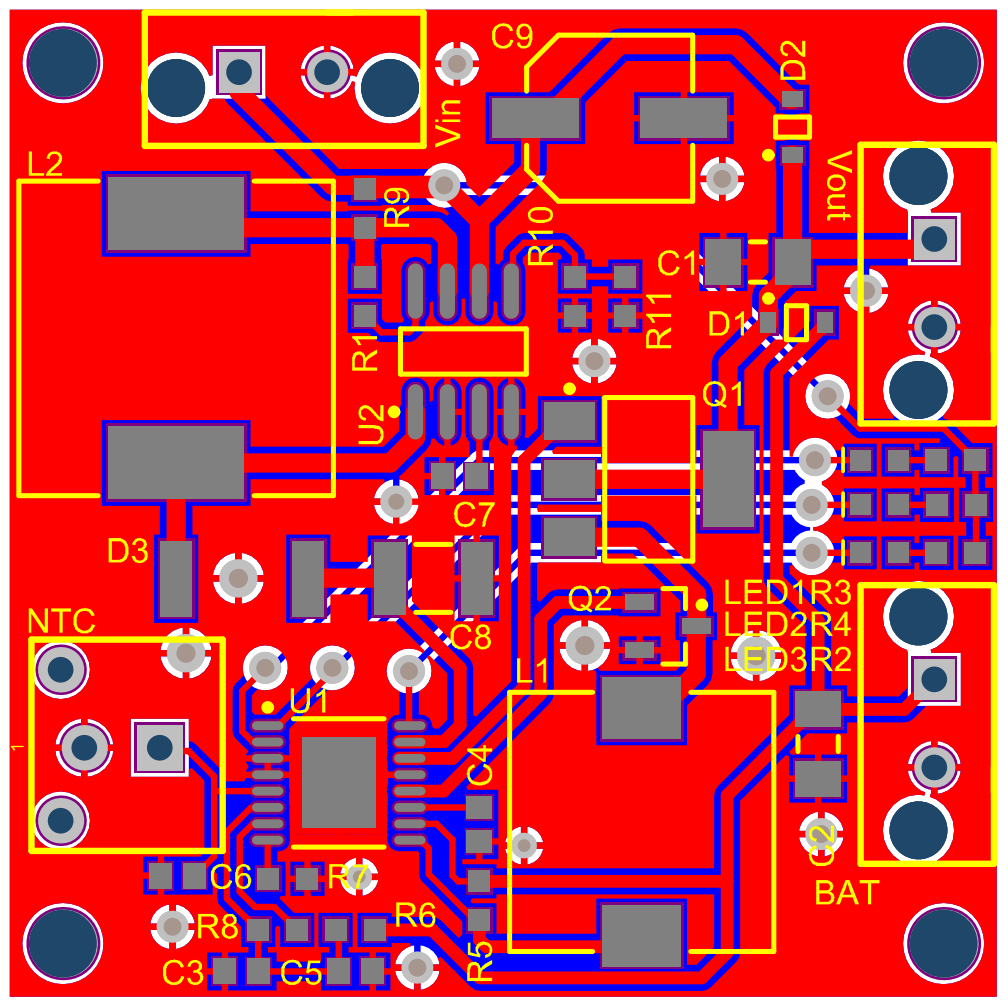


Title		
Size: A4	Number	Revision
Date: 2019/11/30	Sheet of	
File: C:\Users\..\NiMH Battery Charger.SchDoc	Drawn By:	

Bill of Materials

Project:	NiMH Battery Charger.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2019/11/30 13:18
Production Quantity:	1
Currency	CAD
Total Parts Count:	36

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Pric
CAP CER 10uF 50V 20% X5R 1206	C1, C2	Murata	GRT31CR61H106ME01L	Digi-Key	490-12457-1-ND	0.66411
CAP CER 10nF 50V 5% X7R 0603	C3, C5	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.43831
CAP CER 0.1UF 50V 10% X7R 0603	C4	Kyocera AVX	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.19923
CAP CER 0.068UF 10% 50V X7R 0603	C6	Murata	GCM188R71H683KA57D	Digi-Key	490-8027-1-ND	0.38518
CAP, 1500PF, 50V, 10%, X7R, 0603	C7	KEMET	C0603C152K5RACTU	Digi-Key		
CAP CER 330UF 6.3V X5R 1210	C8	Taiyo Yuden	JMK325ABJ337MM-P	Digi-Key	587-5449-1-ND	6.51
CAP ALUM 100UF 20% 35V SMD	C9	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951CT-ND	0.62426
DIODE Schottky Barrier	D1, D2			Digi-Key		
DIODE SCHOTTKY 40V 1A MELF	D3					
IND 10UH 2.8A 59 MOHM SMD	L1	Sumida	CDRH103RNP-100NC-B	Digi-Key	308-1910-1-ND	2.03
IND 180 µH Power Inductor	L2					
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18595
LED YELLOW CLEAR 2.1V 0603	LED2	Wurth Electronics	150060YS75000	Digi-Key	732-4981-1-ND	0.18595
LED RED CLEAR 2V 0603	LED3	Wurth Electronics	150060RS75000	Digi-Key	732-4978-1-ND	0.18595
CONN 2POS ULTRA-FIT 0.138"	P1, P2, P3	Molex	172287-1102	Digi-Key	WM11701-ND	1.04
CONN 2POS MICRO-FIT 3mm	P4	Molex	43045-0227	Digi-Key	WM10657-ND	1.12
ONSC-PMOS-G1D2S3D4-4	Q1					
MOSFET N-CHANNEL 20V 4A SOT23F	Q2	Toshiba	SSM3K345R,LF	Digi-Key	SSM3K345RLFCT-ND	0.55785
CMP-2002-08252-1	R1, R9	Vishay	CRCW0402180KFKED	Farnell	1571693	
RES 10K OHM 1% 1/10W 0603	R2, R3, R4	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13282
RES-2	R5					
RES	R6, R8					
CMP-2002-05244-1	R7					
RES 2.21K OHM 1% 1/10W 0603	R10	Yageo	AC0603FR-072K21L	Digi-Key	YAG3586CT-ND	0.13282
RES 47K OHM 1% 1/10W 0603	R11	Vishay	CRCW060347K0FKEA	Digi-Key		
IC Nickel Battery Charger	U1	Analog Devices / Linear	LTC4010CFE#PBF	Digi-Key	LTC4010CFE#PBF-ND	14.33


C9
D2
Vin
Vout
L2
R9
R10
C1
R11
D1
R1
U2
Q1
C7
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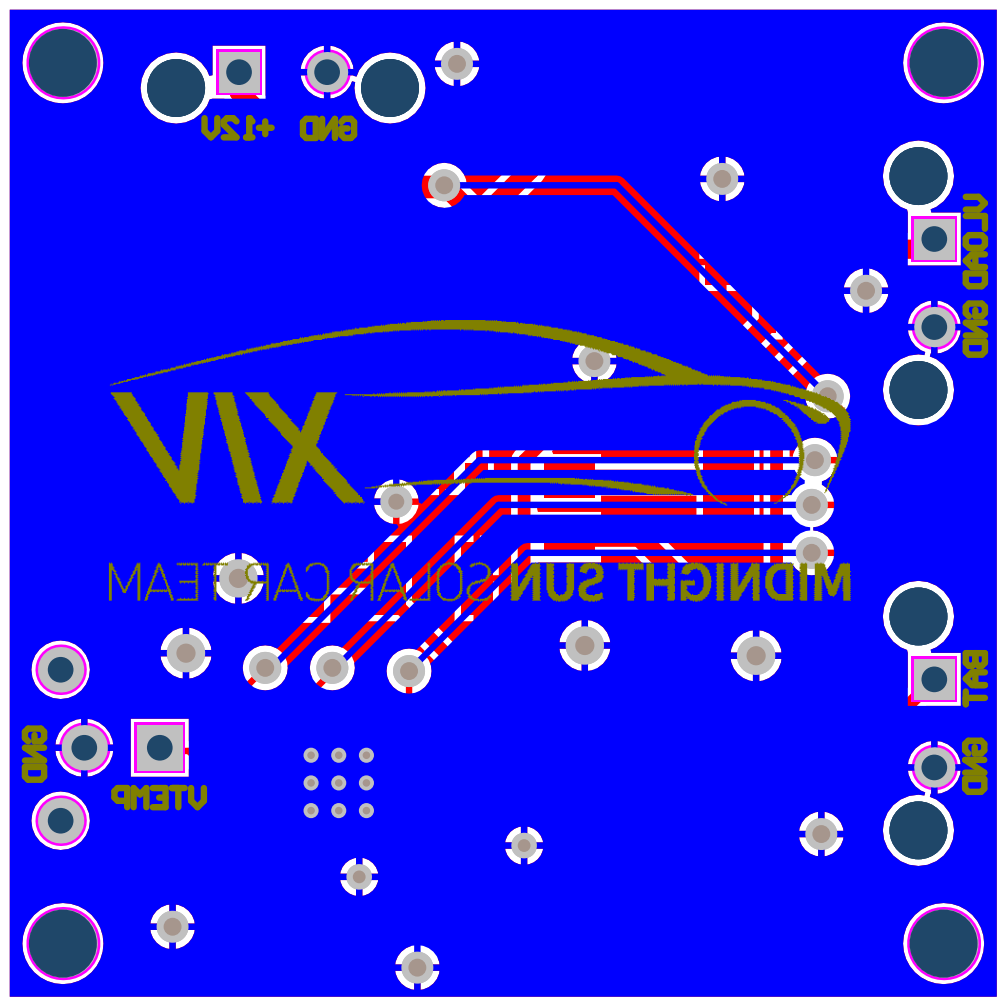
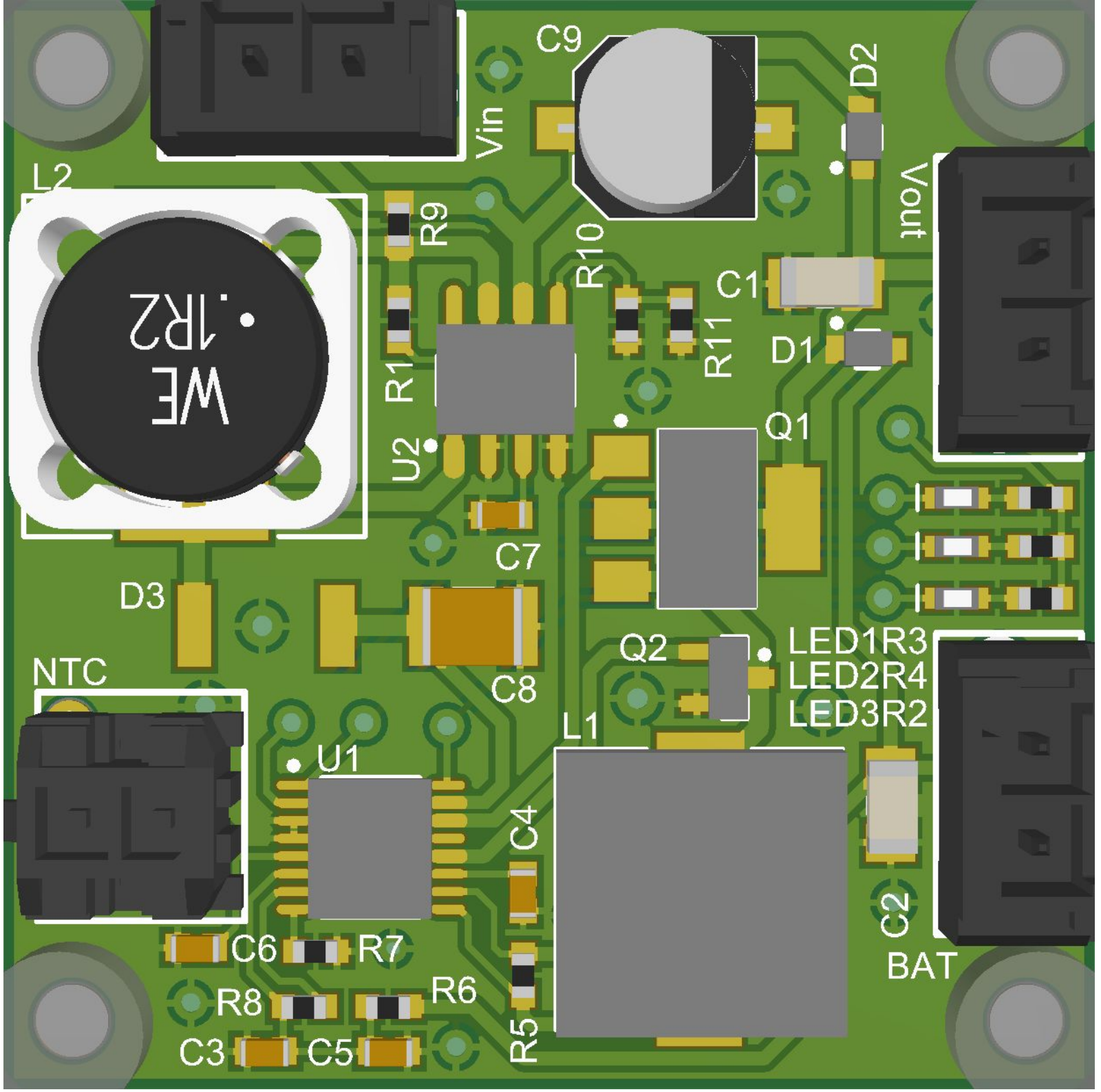
LED1R3
LED2R4
LED3R2
Q2
NTC
C8
L1
U1
C4
C6
R7
R8
R6
C3
C5
R5
BAT


+12V
GND
VLOAD
GND
BAT
GND
GND
VTEMP
MIDNIGHT SUN SOLAR CAR TEAM


C9
Vin
D2
Vout
L2
WE
.1R2
R9
R10
C1
R1
R11
D1
U2
Q1
C7
D3
C8
Q2
LED1R3
LED2R4
LED3R2
NTC
L1
U1
C4
C2
BAT
C6
R7
R8
R6
C3
C5
R5

Electrical Rules Check Report

Class	Document	Message
Warning	NiMH Battery Charger.SchDoc	Net NetR7_2 has no driving source (Pin R7-2,Pin U1-8)
Warning	NiMH Battery Charger.SchDoc	Net NetR10_1 has no driving source (Pin R10-1,Pin R11-1,Pin U2-5)
Warning	NiMH Battery Charger.SchDoc	Net SENSE has no driving source (Pin L1-2,Pin R5-1,Pin U1-9)
Warning	NiMH Battery Charger.SchDoc	Net VCELL has no driving source (Pin C3-1,Pin C5-1,Pin R6-1,Pin R8-2,Pin U1-6)
Warning	NiMH Battery Charger.SchDoc	Net VTEMP has no driving source (Pin C6-1,Pin P4-1,Pin U1-5)
Warning	NiMH Battery Charger.SchDoc	Off grid Net Label VLOAD at 4187.276mil,1000mil
Warning	NiMH Battery Charger.SchDoc	Off grid Net Label VLOAD at 5787.276mil,7200mil

Design Rules Verification Report

Filename : C:\Users\YCA42\hardware\MSXIV_AuxBatteryCharger\NiMH Battery Charger Rev

Warnings 0
Rule Violations 44

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	14
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	14
Silk to Silk (Clearance=10mil) (All),(All)	12
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	44

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1476.378mil,-1476.378mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1476.378mil,-98.425mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(98.425mil,-1476.378mil) on Multi-Layer Actual Hole Size = 106.299mil
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(98.425mil,-98.425mil) on Multi-Layer Actual Hole Size = 106.299mil

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-1(418.779mil,-1135.433mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-10(641.22mil,-1288.976mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-10(641.22mil,-1288.976mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-11(641.22mil,-1263.386mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-12(641.22mil,-1237.795mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-13(641.22mil,-1212.205mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-14(641.22mil,-1186.614mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-15(641.22mil,-1161.024mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-2(418.779mil,-1161.024mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-3(418.779mil,-1186.614mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-4(418.779mil,-1212.205mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-5(418.779mil,-1237.795mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-6(418.779mil,-1263.386mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (3.811mil < 10mil) Between Pad U1-7(418.779mil,-1288.976mil) on Top Layer And Pad

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.791mil < 10mil) Between Pad C5-1(530mil,-1520mil) on Top Layer And Text "C5" (440mil,-1540mil) on Top
Silk To Solder Mask Clearance Constraint: (8.948mil < 10mil) Between Pad C6-1(305mil,-1370mil) on Top Layer And Text "C6" (330mil,-1390mil) on Top
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C9-1(837.716mil,-185mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C9-1(837.716mil,-185mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C9-2(1070mil,-185mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C9-2(1070mil,-185mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED1-2(1345.945mil,-865mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED2-2(1345.945mil,-720mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(1345.945mil,-790mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.918mil < 10mil) Between Pad NTC-0(94.882mil,-1047.953mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad NTC-0(94.882mil,-1047.953mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.376mil < 10mil) Between Pad NTC-0(94.882mil,-1284.173mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad NTC-0(94.882mil,-1284.173mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.831mil < 10mil) Between Pad R7-2(420mil,-1375mil) on Top Layer And Text "C6" (330mil,-1390mil) on Top

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (8.324mil < 10mil) Between Arc (616.535mil,-644.488mil) on Top Overlay And Text "U2" (600mil,-695mil) on Top Overlay
Silk To Silk Clearance Constraint: (6.811mil < 10mil) Between Text "1" (37.402mil,-1173.937mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.079mil < 10mil) Between Text "L2" (45mil,-275mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.516mil < 10mil) Between Text "LED2" (1135mil,-995mil) on Top Overlay And Text "R4" (1270mil,-995mil) on Top
Silk To Silk Clearance Constraint: (8.349mil < 10mil) Between Text "LED3" (1135mil,-1050mil) on Top Overlay And Text "R2" (1270mil,-1050mil) on Top
Silk To Silk Clearance Constraint: (5.709mil < 10mil) Between Text "NTC" (45mil,-990mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (5.73mil < 10mil) Between Text "NTC" (45mil,-990mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.907mil < 10mil) Between Text "R2" (1270mil,-1050mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.963mil < 10mil) Between Text "R3" (1270mil,-945mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.685mil < 10mil) Between Text "R4" (1270mil,-995mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (5.225mil < 10mil) Between Text "U1" (455mil,-1115mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.051mil < 10mil) Between Text "Vout" (1295mil,-235mil) on Top Overlay And Track