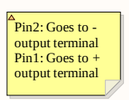
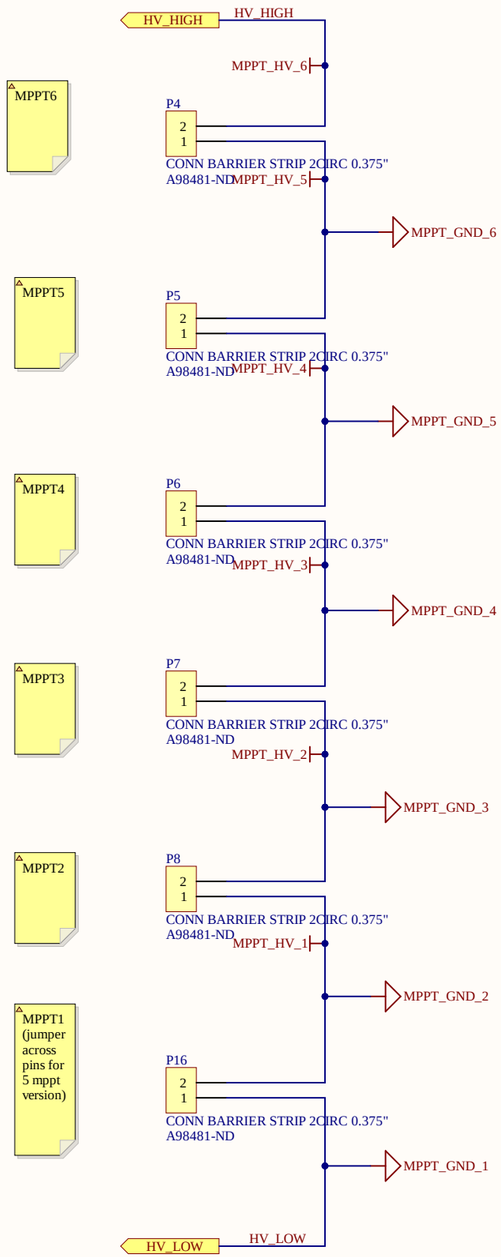
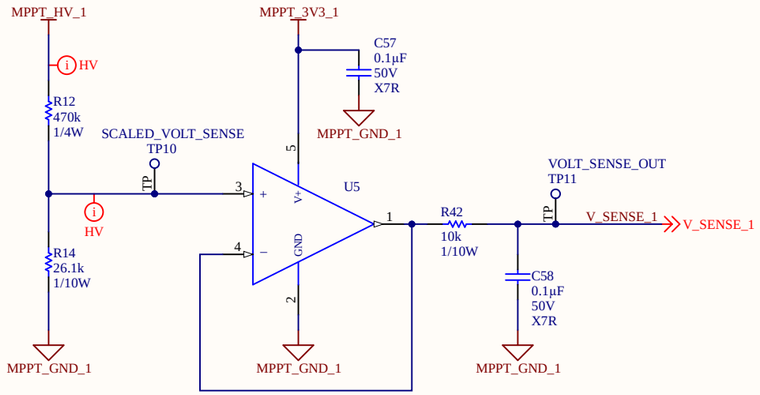
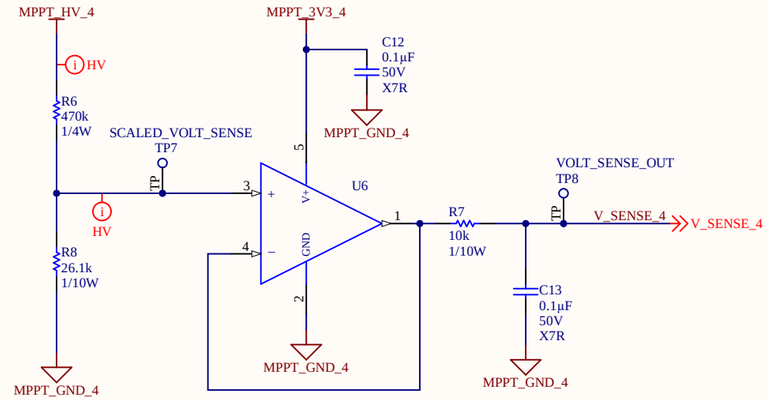
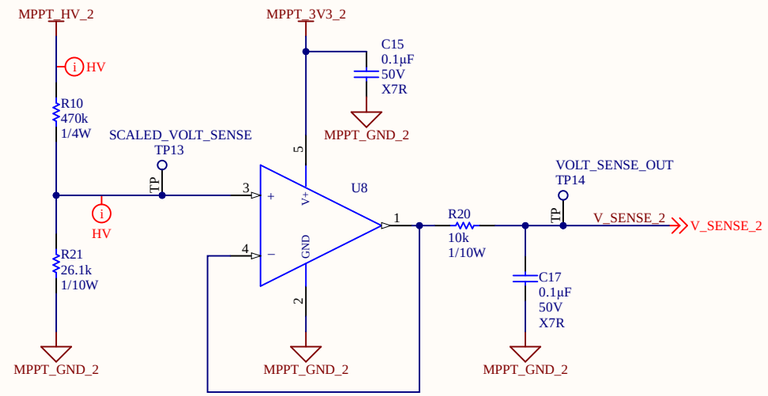
Voltage Sense

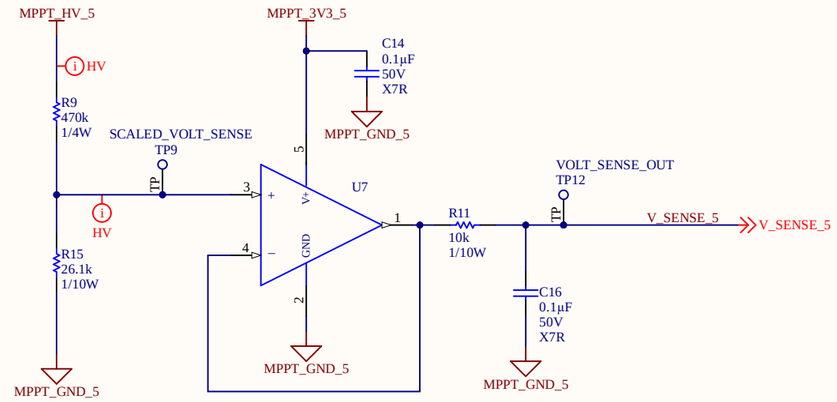


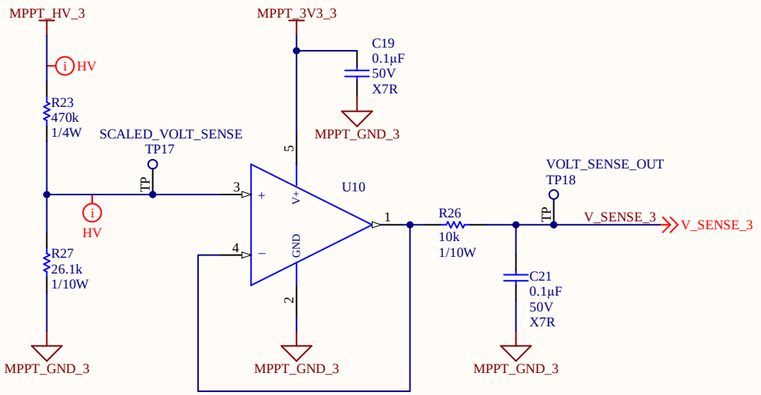


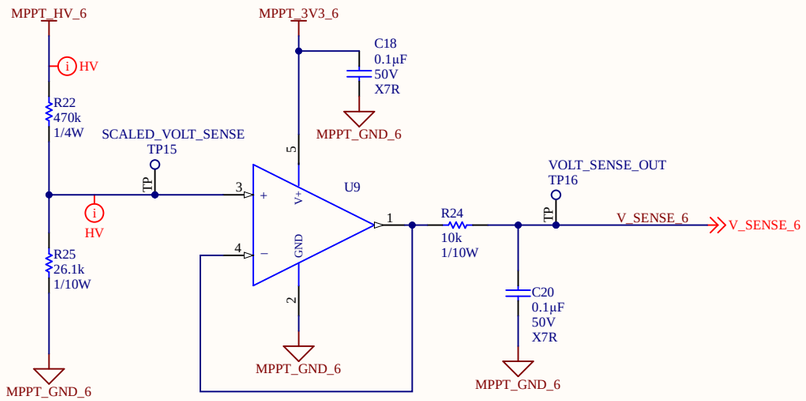




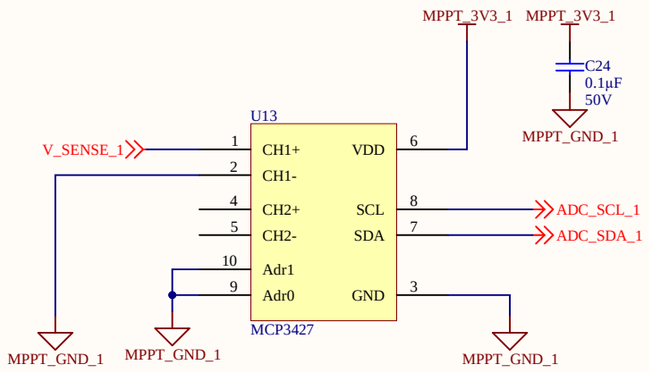


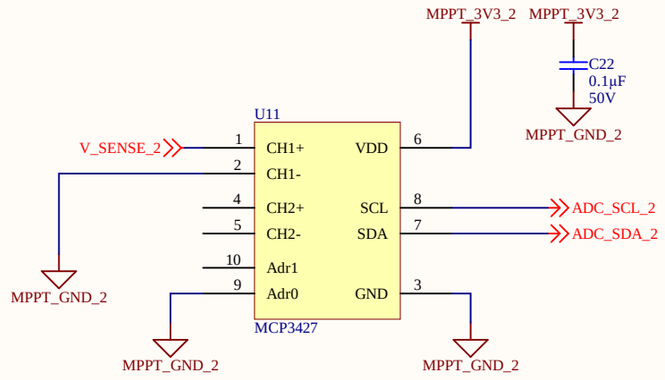


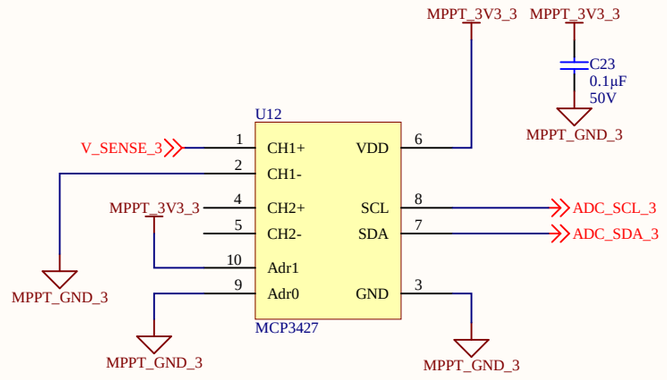




Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: **Solar Sense Slave**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Lead: *		
Size: Letter	Revision: *	
Date: 2020-02-11	Sheet 3 of 4	Website: www.uwmidsun.com

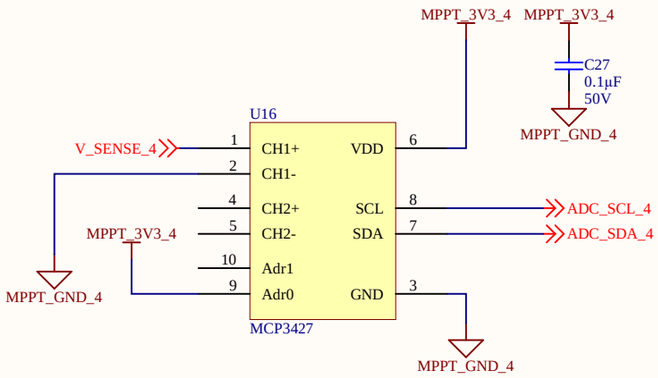


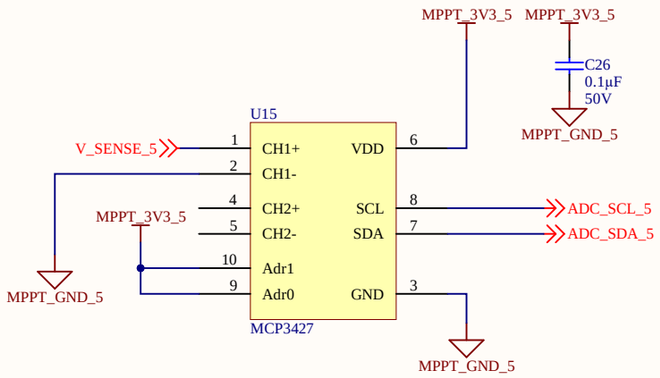


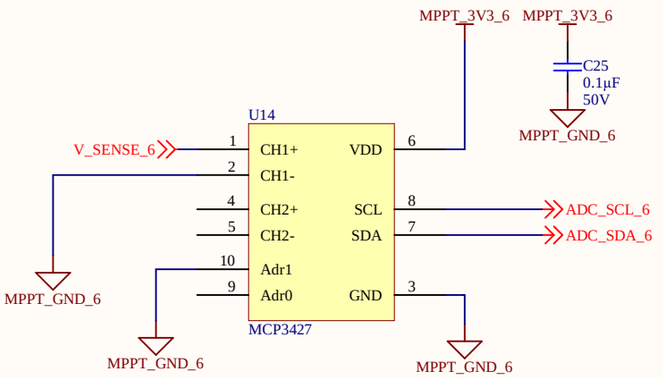


ADCs

I²C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float







Make combination of pulled high, low and floating (for address pins)

PROJECT	MSXIV_SolarSense.PrjPcb
DOCUMENT	*
PART NUMBER	
VARIANT	[No Variations]
DRAWN BY	Aashmika Mali
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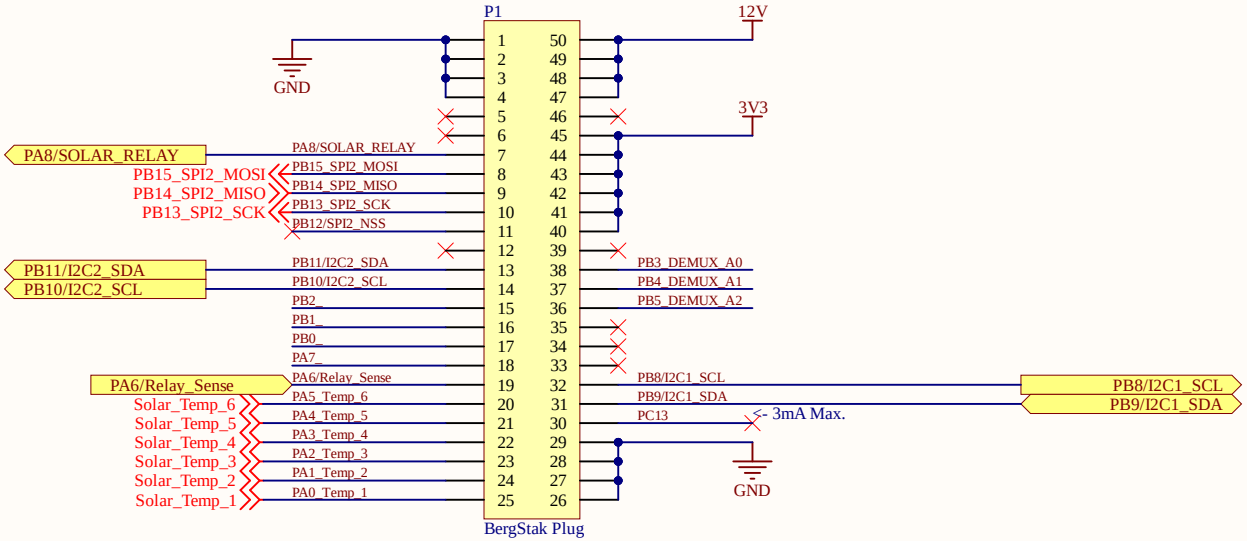
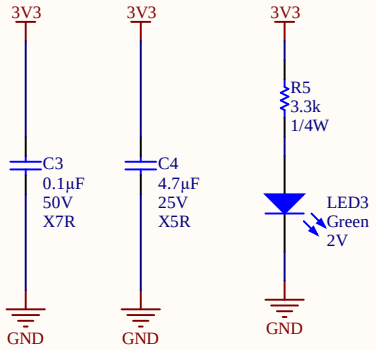
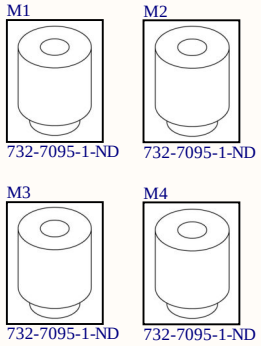
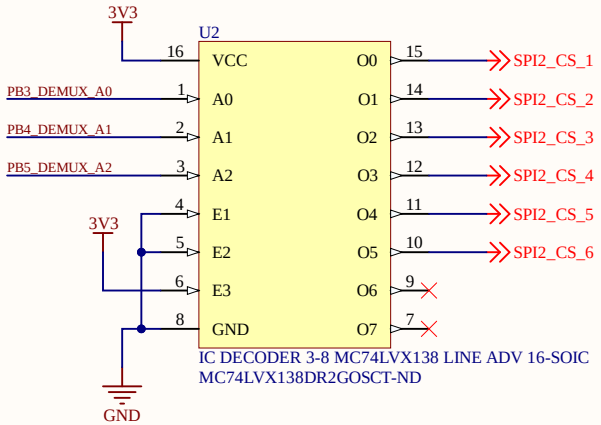
Add 6 gpio pins for slave select on spi, and 6 gpios for temperature sensing

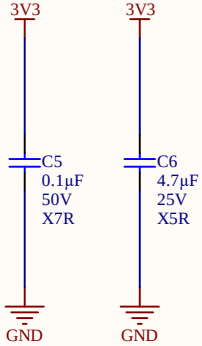




Standoffs







Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Aashmika Mali		
Size: Letter	Revision: 1.0	
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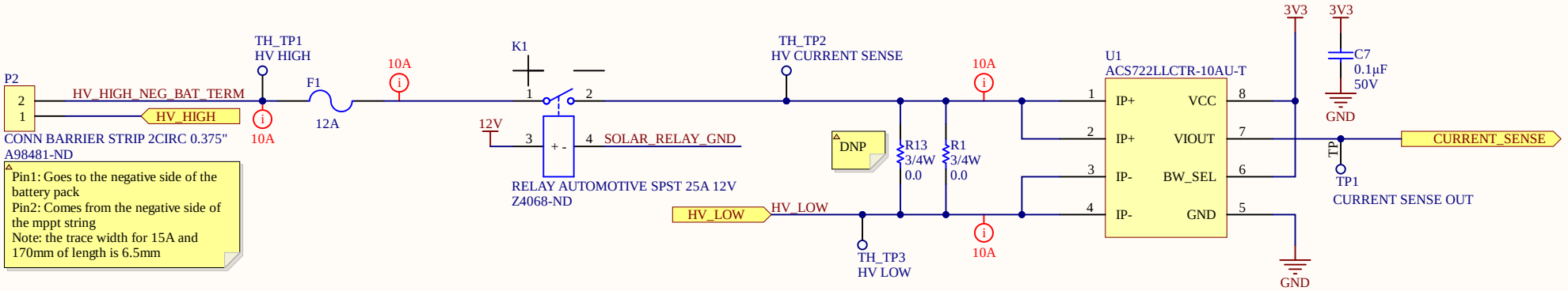
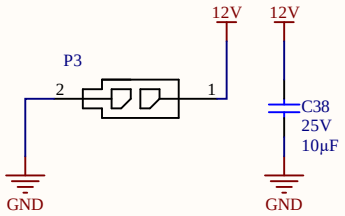
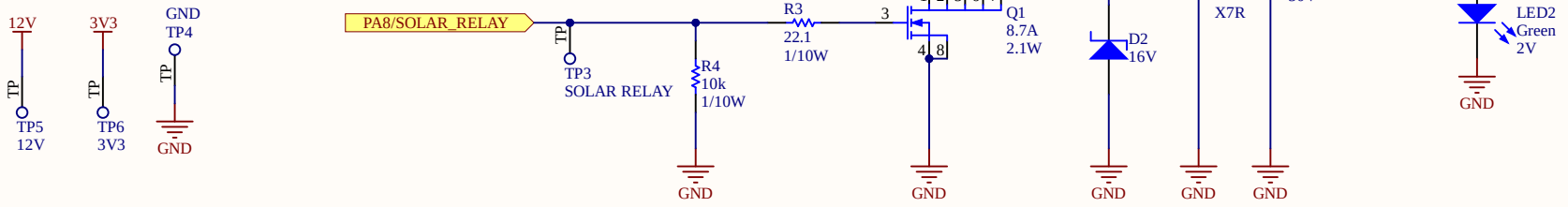
Passthrough - Current Sense, Fuse, and Relay







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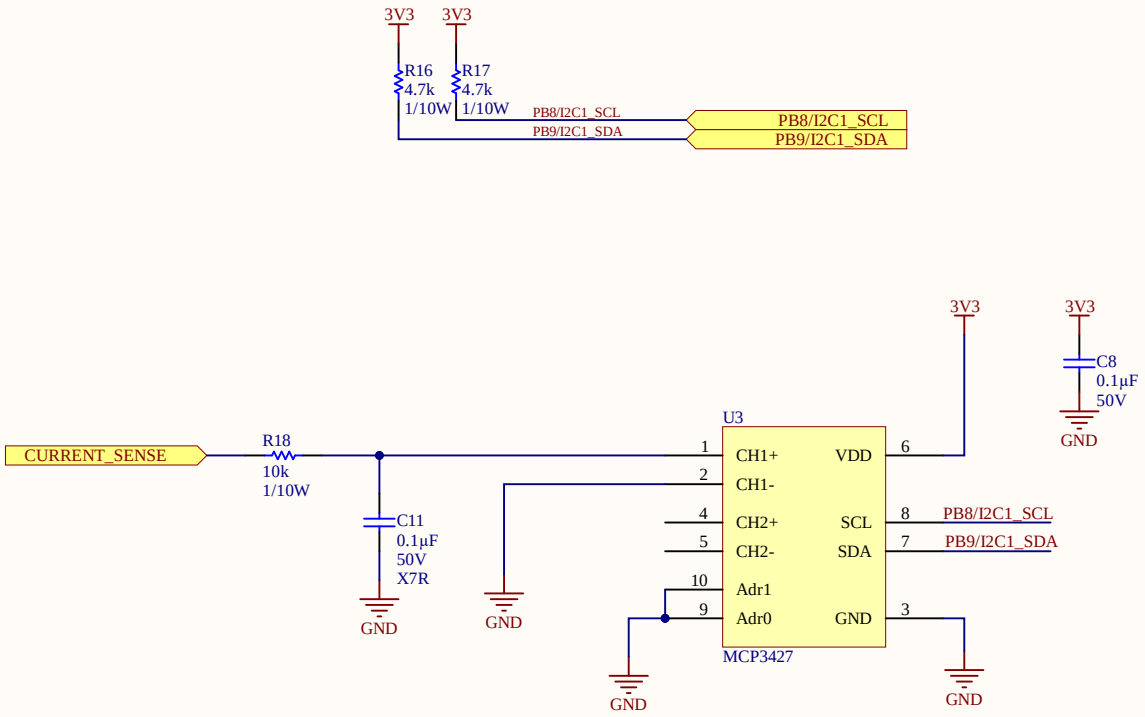
I2C Interface (for Current Sense)



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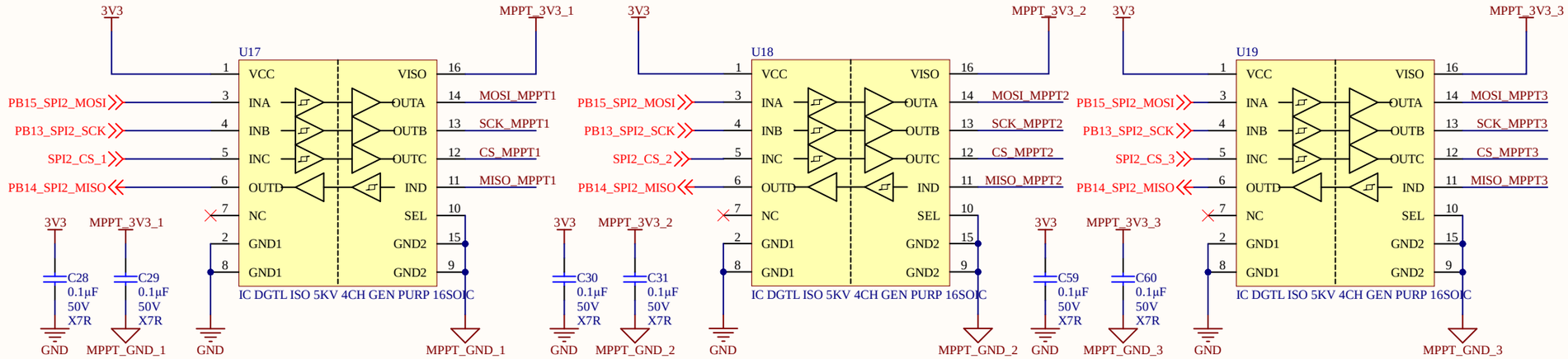
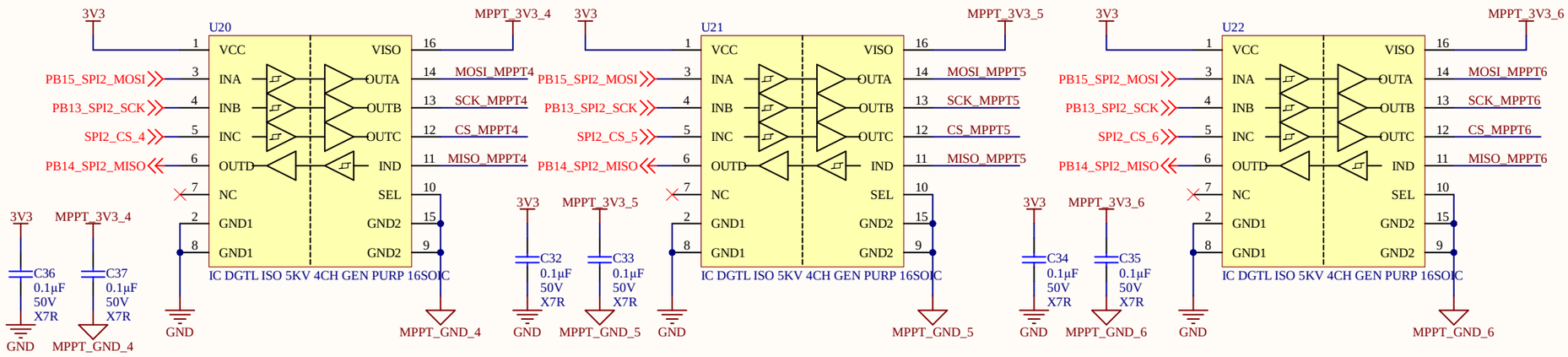
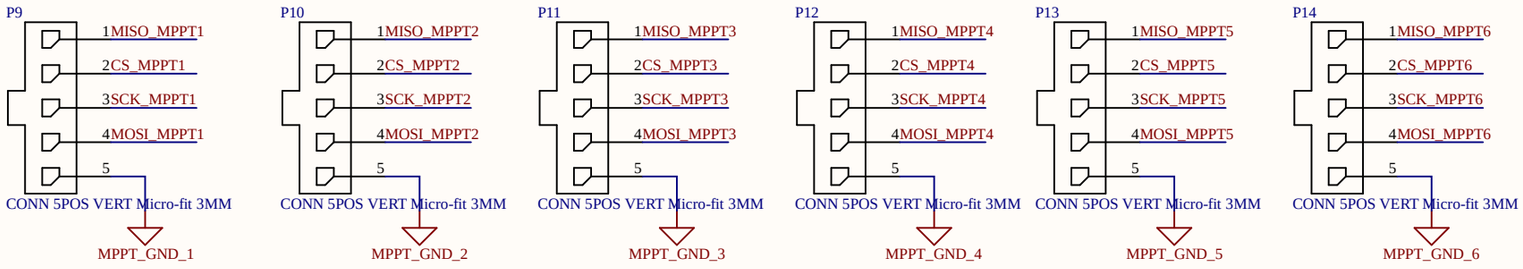
SPI Isolators







PROJECT MSXIV_SolarSense.PrjPcb	MIDNIGHT SUN
DOCUMENT *	
PART NUMBER	VARIANT [No Variations]
DRAWN BY Aashmika Mali	REVISION 1.0
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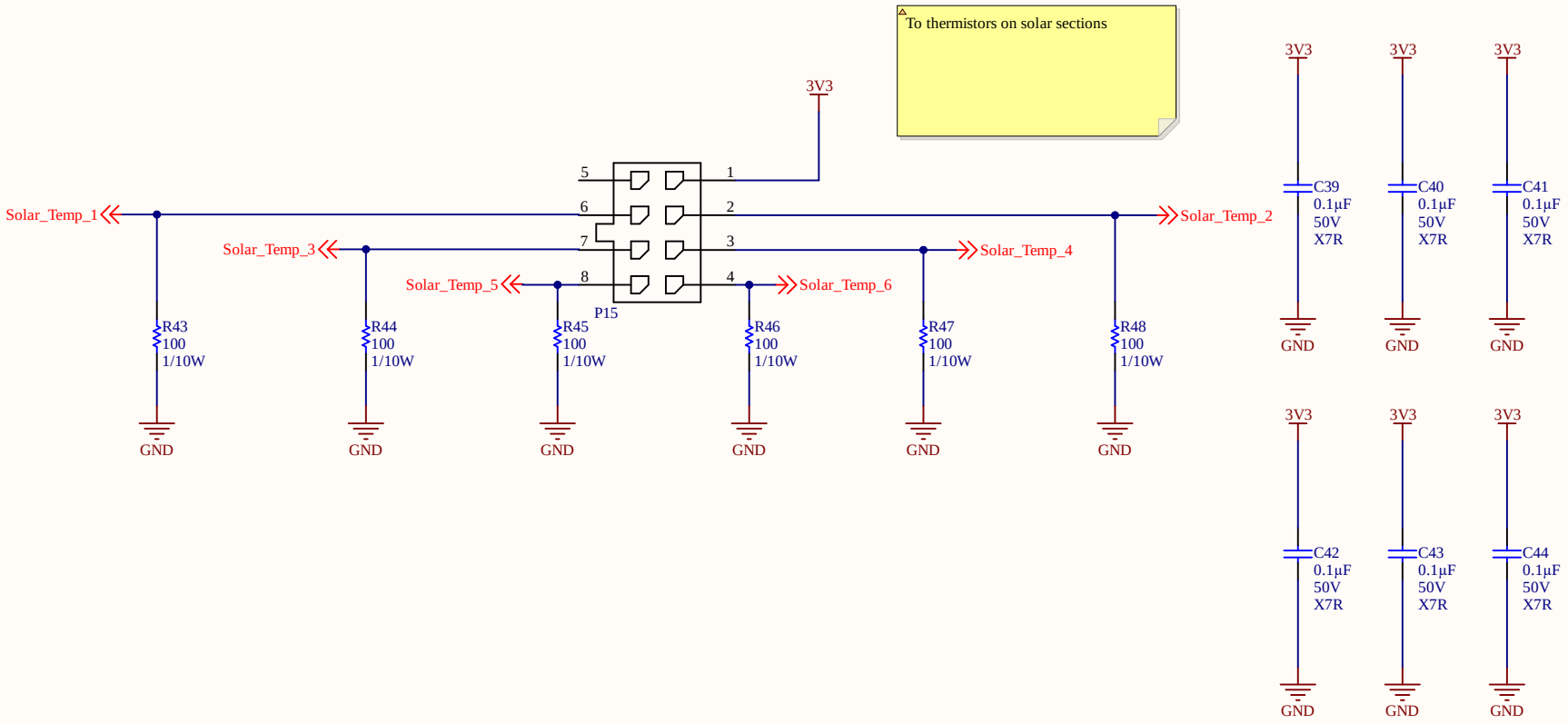
Temperature Sense for Array Sections



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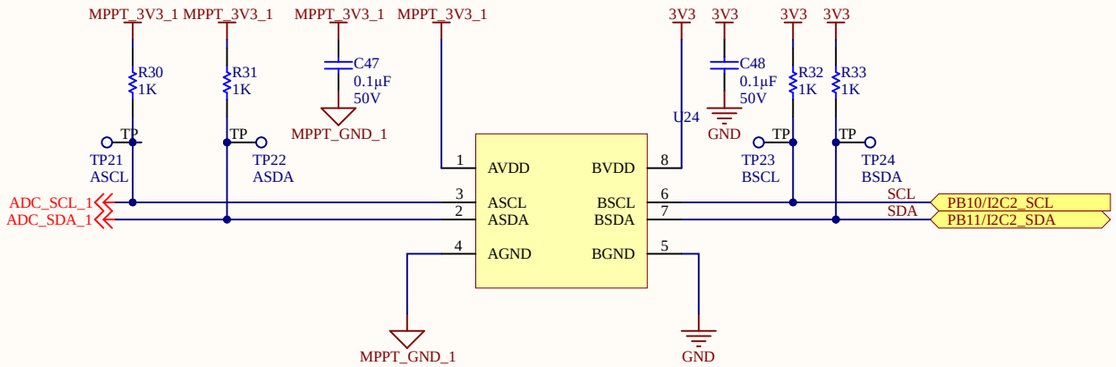
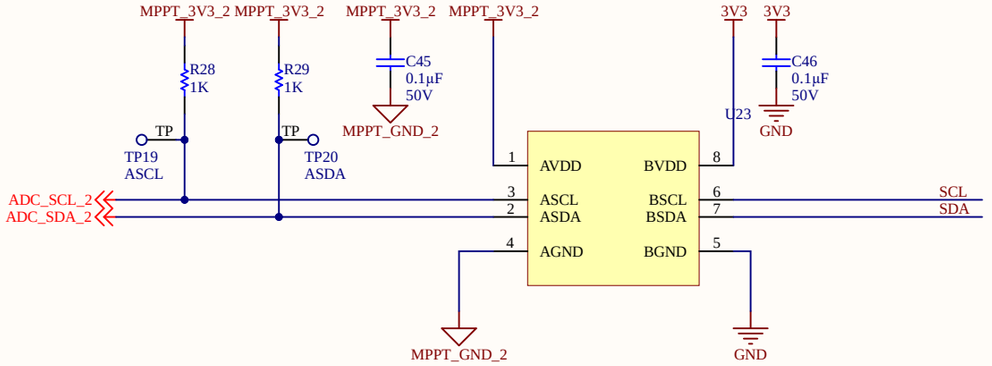
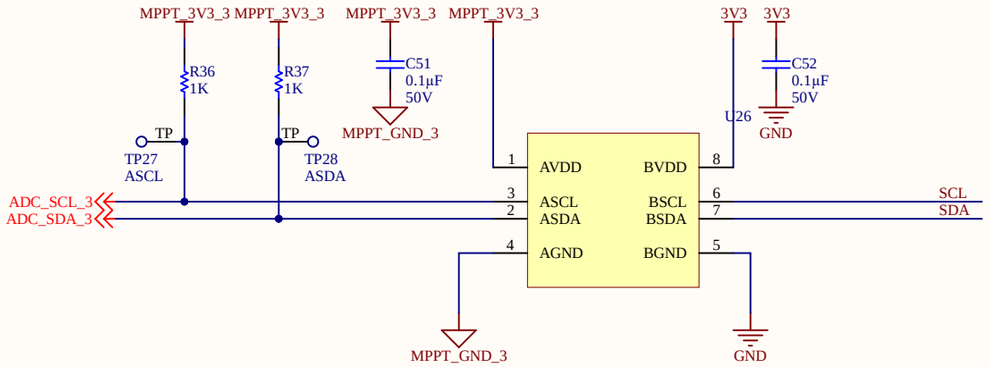
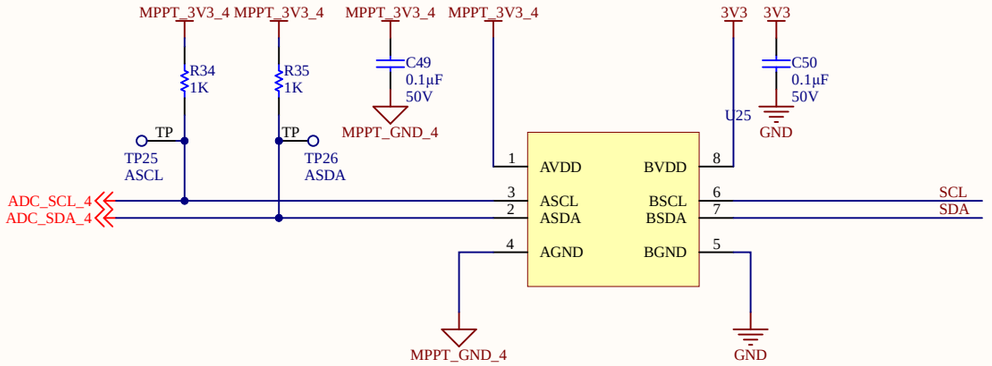
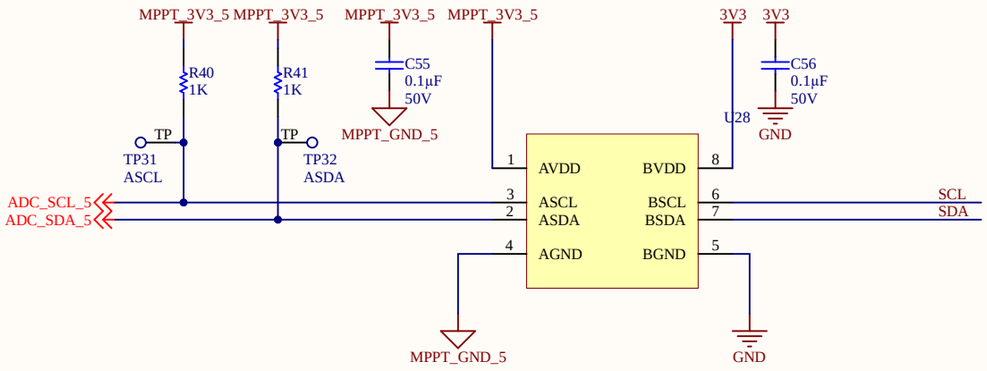
I2C Isolators for V-Sense

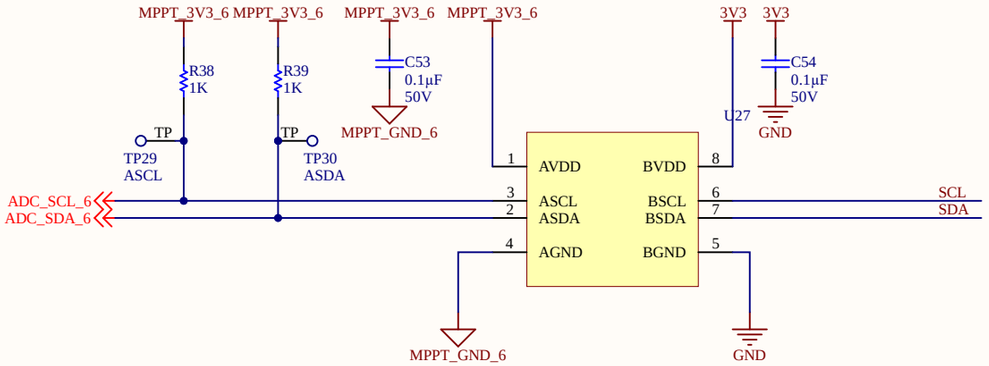












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DOCUMENT	*		
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DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-11	SHEET	* OF *

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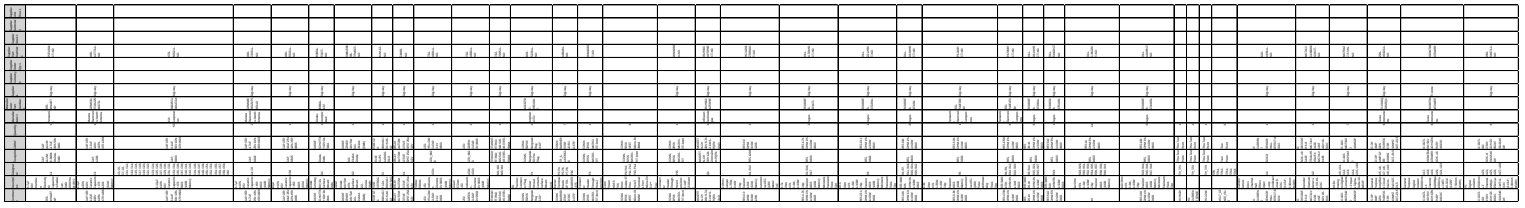
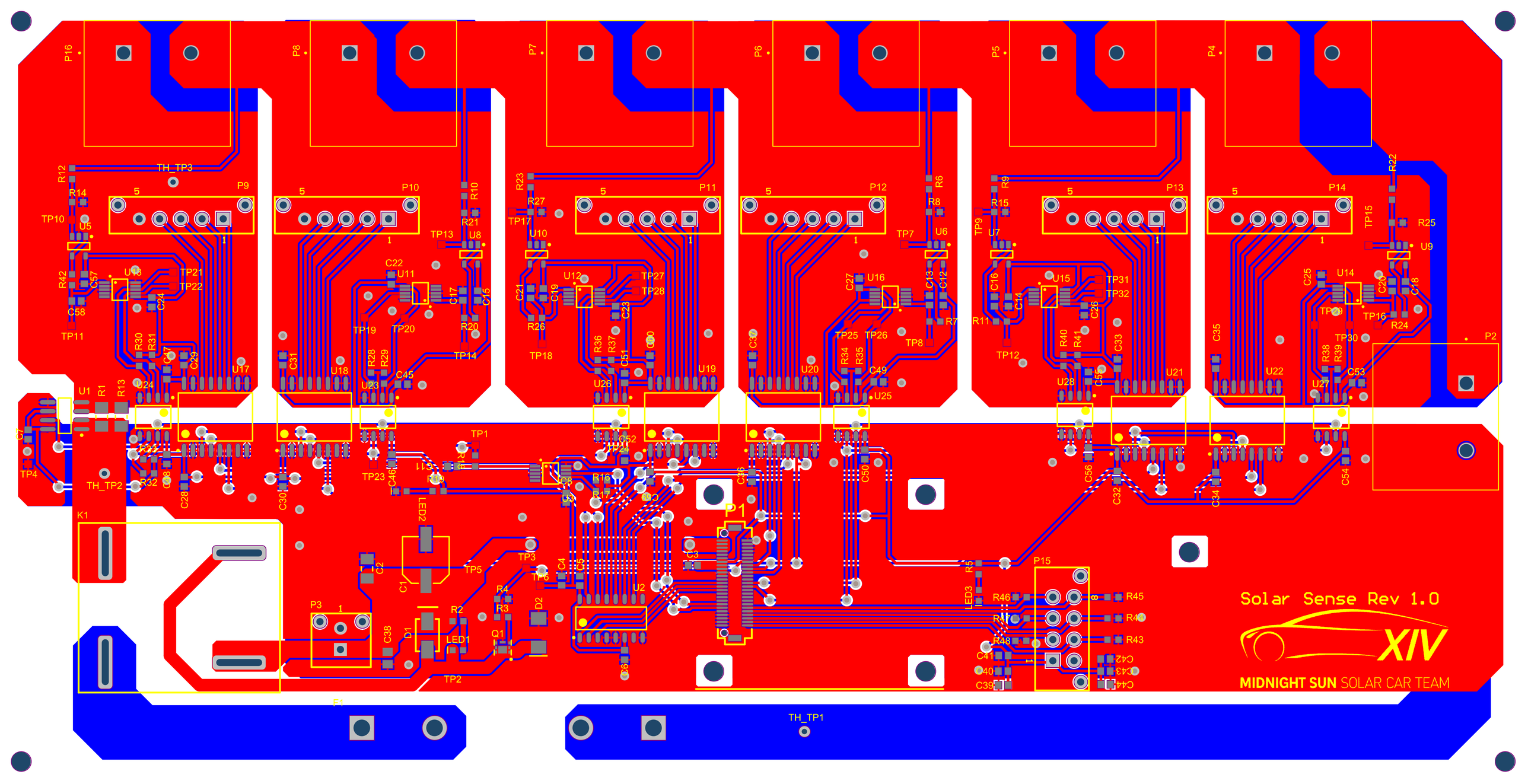
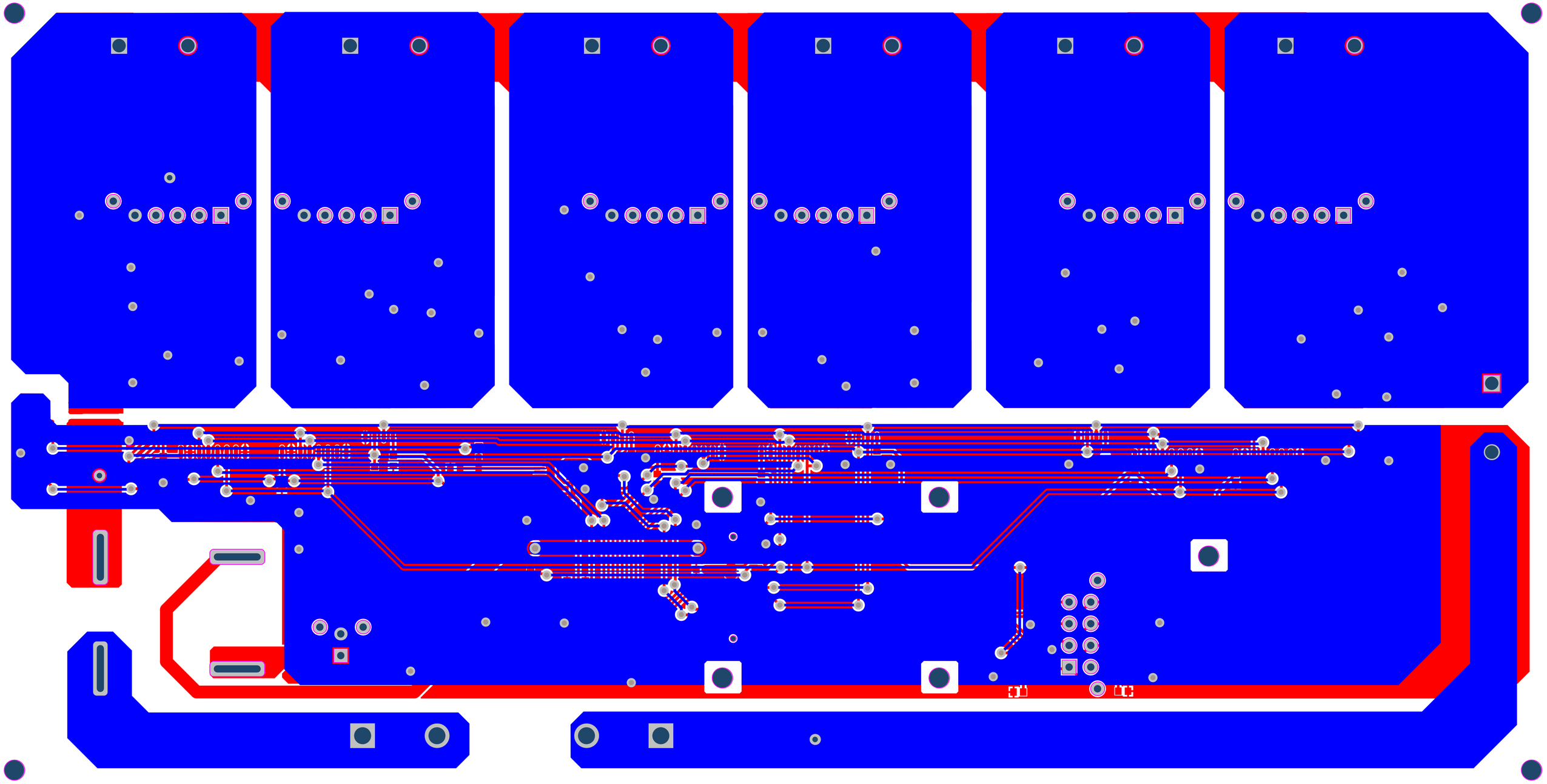
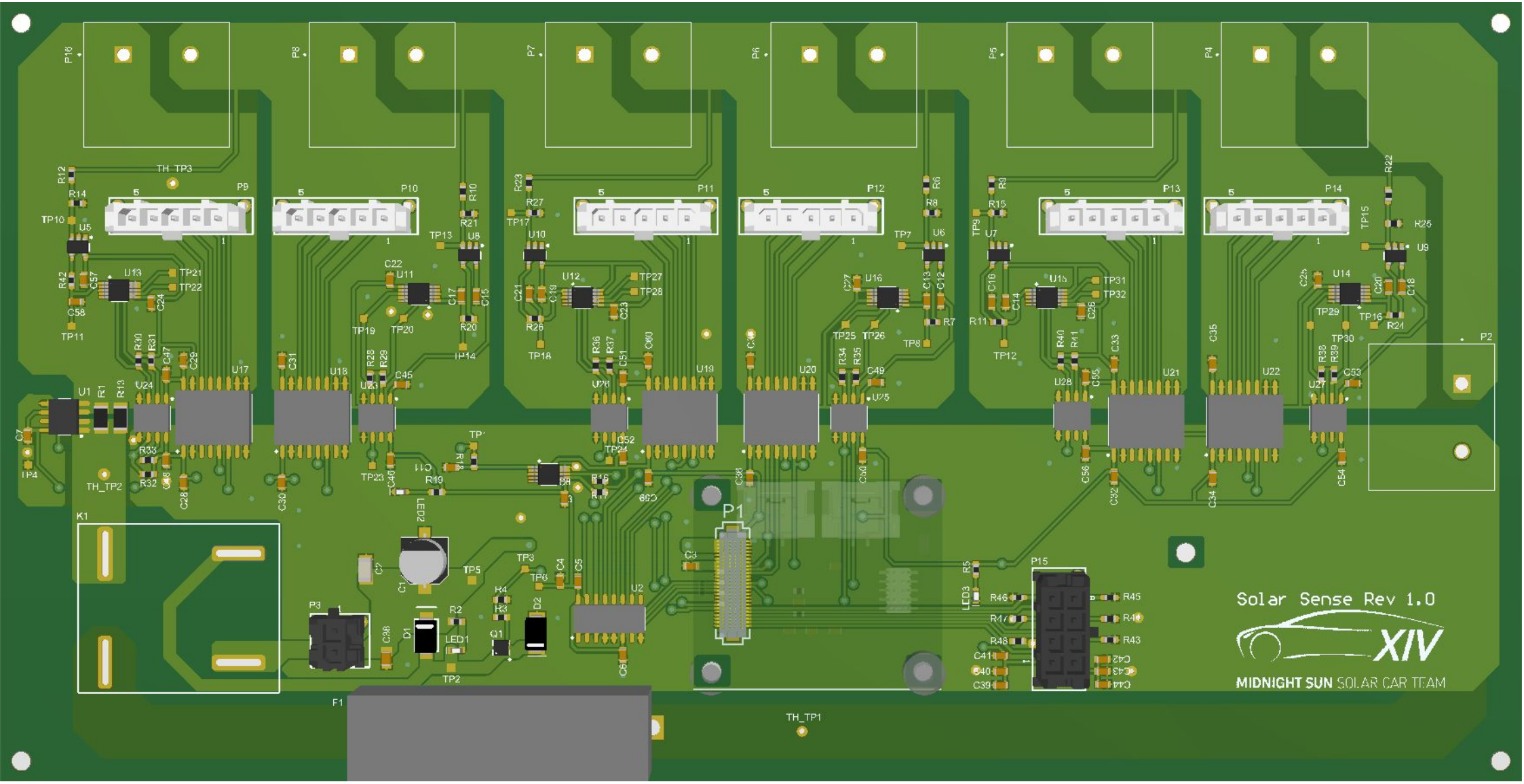



Solar Sense Rev 1.0
XIV
MIDNIGHT SUN SOLAR CAR TEAM

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MIDNIGHT SUN SOLAR CAR TEAM

Electrical Rules Check Report

Class	Document	Message
Error	Voltage_Sense.SchDoc	HV_LOW contains Power Pin and Output Port objects (Pin U5-2, Port HV_LOW).
Error	Controller_Board_Interface.SchDoc	Net PA6/Relay_Sense has only one pin (Pin P1-19)
Error	Controller_Board_Interface.SchDoc	Net PA7_ has only one pin (Pin P1-18)
Error	Controller_Board_Interface.SchDoc	Net PB0_ has only one pin (Pin P1-17)
Error	Controller_Board_Interface.SchDoc	Net PB1_ has only one pin (Pin P1-16)
Error	Controller_Board_Interface.SchDoc	Net PB2_ has only one pin (Pin P1-15)
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_GND_1 at 3650mil,1830mil has been reduced to local level by presence of port at 2000mil,1300mil
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_HV_6 at 3350mil,9100mil has been reduced to local level by presence of port at 2000mil,9400mil
Warning	Voltage_Sense.SchDoc	Net NetR6_2 has no driving source (Pin R6-2, Pin R8-1, Pin TP7-TP, Pin U6-3)
Warning	Voltage_Sense.SchDoc	Net NetR9_2 has no driving source (Pin R9-2, Pin R15-1, Pin TP9-TP, Pin U7-3)
Warning	Voltage_Sense.SchDoc	Net NetR10_2 has no driving source (Pin R10-2, Pin R21-1, Pin TP13-TP, Pin U8-3)
Warning	Voltage_Sense.SchDoc	Net NetR12_2 has no driving source (Pin R12-2, Pin R14-1, Pin TP10-TP, Pin U5-3)
Warning	Voltage_Sense.SchDoc	Net NetR22_2 has no driving source (Pin R22-2, Pin R25-1, Pin TP15-TP, Pin U9-3)
Warning	Voltage_Sense.SchDoc	Net NetR23_2 has no driving source (Pin R23-2, Pin R27-1, Pin TP17-TP, Pin U10-3)
Warning	Controller_Board_Interface.SchDoc	Net PB3_DEMUX_A0 has no driving source (Pin P1-38, Pin U2-1)
Warning	Controller_Board_Interface.SchDoc	Net PB4_DEMUX_A1 has no driving source (Pin P1-37, Pin U2-2)
Warning	Controller_Board_Interface.SchDoc	Net PB5_DEMUX_A2 has no driving source (Pin P1-36, Pin U2-3)
Warning	Current_and_Relay_Sense.SchDoc	Nets Wire HV_HIGH has multiple names (Net Label HV_HIGH, Power Object MPPT_HV_6, Power Object MPPT_HV_6)
Warning	ADCs.SchDoc	Nets Wire HV_LOW has multiple names (Net Label HV_LOW, Net Label HV_LOW, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_2 has multiple names (Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_HV_1, Power Object MPPT_HV_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_3 has multiple names (Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_HV_2, Power Object MPPT_HV_2)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_4 has multiple names (Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_HV_3, Power Object MPPT_HV_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_5 has multiple names (Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_HV_4, Power Object MPPT_HV_4)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_6 has multiple names (Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_HV_5, Power Object MPPT_HV_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA0_Temp_1 has multiple names (Cross-Sheet Connector Solar_Temp_1, Cross-Sheet Connector Solar_Temp_1, Net Label PA0_Temp_1)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA1_Temp_2 has multiple names (Cross-Sheet Connector Solar_Temp_2, Cross-Sheet Connector Solar_Temp_2, Net Label PA1_Temp_2)

Class	Document	Message
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA2_Temp_3 has multiple names (Cross-Sheet Connector Solar_Temp_3, Cross-Sheet Connector Solar_Temp_3, Net Label PA2_Temp_3)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA3_Temp_4 has multiple names (Cross-Sheet Connector Solar_Temp_4, Cross-Sheet Connector Solar_Temp_4, Net Label PA3_Temp_4)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA4_Temp_5 has multiple names (Cross-Sheet Connector Solar_Temp_5, Cross-Sheet Connector Solar_Temp_5, Net Label PA4_Temp_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA5_Temp_6 has multiple names (Cross-Sheet Connector Solar_Temp_6, Cross-Sheet Connector Solar_Temp_6, Net Label PA5_Temp_6)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB10/I2C2_SCL has multiple names (Net Label PB10/I2C2_SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB11/I2C2_SDA has multiple names (Net Label PB11/I2C2_SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA)
Warning	ADCs.SchDoc	Off grid C24 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SCL_1 at 3600mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SDA_1 at 3600mil,7544.41mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB13_SPI2_SCK at 6574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB14_SPI2_MISO at 6574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB15_SPI2_MOSI at 6574.41mil,6851.811mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_2 at 7837.008mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_4 at 6687.008mil,4596.063mil
Warning	Controller_Board_Interface.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 2247.008mil,4300mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 5650mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_1 at 1350mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_2 at 6281.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_3 at 11381.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_4 at 1631.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_5 at 6531.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_6 at 11231.89mil,3400mil
Warning	Controller_Board_Interface.SchDoc	Off grid M1 at 1693.983mil,2899.713mil
Warning	Controller_Board_Interface.SchDoc	Off grid M2 at 2406.601mil,2898.306mil
Warning	Controller_Board_Interface.SchDoc	Off grid M3 at 1693.983mil,1949.714mil
Warning	Controller_Board_Interface.SchDoc	Off grid M4 at 2406.601mil,1948.306mil
Warning	SPI_Interface.SchDoc	Off grid Net Label CS_MPPT2 at 8674.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT2 at 8624.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT3 at 12055.512mil,6250mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT2 at 8674.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT3 at 12055.512mil,6850mil
Warning	SPI_Interface.SchDoc	Off grid Net Label SCK_MPPT2 at 8674.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid No ERC at 6774.41mil,6051.811mil
Warning	TemperatureSense.SchDoc	Off grid P15 at 4521.654mil,5096.063mil
Warning	ADCs.SchDoc	Off grid Pin C24-1 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Pin C24-2 at 3818.11mil,8374.41mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-1 at 5421.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-2 at 5421.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-3 at 5421.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-4 at 5421.654mil,4396.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-5 at 4521.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-6 at 4521.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-7 at 4521.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-8 at 4521.654mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Pin U13-1 at 1658.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-2 at 1658.11mil,7894.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-3 at 3108.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil

Class	Document	Message
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-8 at 6774.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-9 at 8574.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-10 at 8574.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_

Warnings 0
Rule Violations 127

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=1.778mm) (Preferred=0.381mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	13
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	26
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	77
Silk to Silk (Clearance=0.254mm) (All),(All)	11
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	127

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-115mm,15.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-115mm,40.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-213mm,107.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-213mm,2.996mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-3mm,107.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-3mm,3mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-47.701mm,32.614mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-85mm,15.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(-85mm,40.754mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (6.5mm > 2.54mm) Pad K1-1(-201.091mm,17.054mm) on Multi-Layer Actual Slot Hole Height = 6.5mm
Hole Size Constraint: (6.5mm > 2.54mm) Pad K1-2(-201.091mm,32.454mm) on Multi-Layer Actual Slot Hole Height = 6.5mm
Hole Size Constraint: (6.5mm > 2.54mm) Pad K1-3(-182.141mm,17.004mm) on Multi-Layer Actual Slot Hole Height = 6.5mm
Hole Size Constraint: (6.5mm > 2.54mm) Pad K1-4(-182.141mm,32.504mm) on Multi-Layer Actual Slot Hole Height = 6.5mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(-112mm,20.454mm) on Top Layer And Pad P1-(-113.5mm,21.204mm)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(-112mm,36.054mm) on Top Layer And Pad P1-(-113.5mm,35.304mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-1(-143.921mm,18.472mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-2(-143.921mm,19.122mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-3(-143.921mm,19.772mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q1-3(-143.921mm,19.772mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-4(-145.771mm,19.772mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-4(-145.771mm,19.772mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q1-4(-145.771mm,19.772mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-5(-145.771mm,19.122mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q1-7(-144.846mm,18.822mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.116mm < 0.254mm) Between Pad R48-1(-70.754mm,20.079mm) on Top Layer And Via (69.375mm,19.678mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U10-1(-139.1mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U10-2(-140.05mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.254mm) Between Pad U3-10(-135.871mm,44.754mm) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (0.151mm < 0.254mm) Between Pad U3-9(-135.871mm,44.254mm) on Top Layer And Via
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(-203.885mm,77.285mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(-204.835mm,77.285mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-1(-82.55mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-2(-83.5mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-1(-73.275mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-2(-74.225mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-1(-148.395mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-2(-149.345mm,76.129mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-1(-17.1mm,76.004mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U9-2(-18.05mm,76.004mm) on Top Layer And Pad U9-3(-19mm,76.004mm)

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(-155.726mm,28.556mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-1(-155.726mm,28.556mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C11-1(-151.291mm,44.754mm) on Top Layer And Text "R18'
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-2(-155.726mm,34.456mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C1-2(-155.726mm,34.456mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.228mm < 0.254mm) Between Pad C15-1(-148.395mm,69.589mm) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (0.202mm < 0.254mm) Between Pad C15-2(-148.395mm,68.239mm) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C52-1(-127.595mm,46.929mm) on Top Layer And Text "TP24'
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad C6-2(-127.595mm,17.404mm) on Top Layer And Text "C6'
Silk To Solder Mask Clearance Constraint: (0.245mm < 0.254mm) Between Pad C7-1(-212mm,49.929mm) on Top Layer And Text "C7'
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad C7-2(-212mm,48.579mm) on Top Layer And Text "C7'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C8-1(-135.871mm,40.995mm) on Top Layer And Text "U3'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad C8-2(-135.871mm,39.645mm) on Top Layer And Text "U3'
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D1-1(-155.5mm,18.847mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D1-1(-155.5mm,18.847mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D1-2(-155.5mm,22.847mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D1-2(-155.5mm,22.847mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D2-2(-139.771mm,19.177mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(-151.95mm,18.754mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED2-2(-159.935mm,41.254mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED3-2(-77.5mm,25.754mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P10-0(-157.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P10-0(-157.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P10-0(-175.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P10-0(-175.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(-110.2mm,34.254mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P11-0(-115.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P11-0(-115.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P11-0(-133.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P11-0(-133.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P12-0(-109.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P12-0(-109.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P12-0(-91.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P12-0(-91.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(-110.2mm,22.254mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(-113.8mm,22.254mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P13-0(-49.225mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(-49.225mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P13-0(-67.225mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P13-0(-67.225mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P14-0(-25.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(-25.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P14-0(-43.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P14-0(-43.9mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(-113.8mm,34.254mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P15-0(-63.06mm,14.254mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.187mm < 0.254mm) Between Pad P15-0(-63.06mm,14.254mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P15-0(-63.06mm,29.254mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P15-0(-63.06mm,29.254mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P3-0(-164.715mm,22.787mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-0(-164.715mm,22.787mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P3-0(-170.715mm,22.787mm) on Multi-Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-0(-170.715mm,22.787mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.213mm < 0.254mm) Between Pad P9-0(-181.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P9-0(-181.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad P9-0(-199.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P9-0(-199.3mm,81.734mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.254mm) Between Pad Q1-1(-143.921mm,18.472mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.254mm) Between Pad Q1-2(-143.921mm,19.122mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.254mm) Between Pad Q1-2(-143.921mm,19.122mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.254mm) Between Pad Q1-3(-143.921mm,19.772mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.254mm) Between Pad Q1-4(-145.771mm,19.772mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.254mm) Between Pad Q1-5(-145.771mm,19.122mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.254mm) Between Pad Q1-5(-145.771mm,19.122mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.254mm) Between Pad Q1-6(-145.771mm,18.472mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.195mm < 0.254mm) Between Pad R16-1(-130.09mm,41.254mm) on Top Layer And Text "R17'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R16-2(-131.64mm,41.254mm) on Top Layer And Text "R17'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R17-1(-130.09mm,42.754mm) on Top Layer And Text "R16'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad R17-2(-131.64mm,42.754mm) on Top Layer And Text "R16'
Silk To Solder Mask Clearance Constraint: (0.064mm < 0.254mm) Between Pad R28-2(-163.5mm,56.479mm) on Top Layer And Text "U23'
Silk To Solder Mask Clearance Constraint: (0.243mm < 0.254mm) Between Pad R38-2(-28.5mm,56.979mm) on Top Layer And Text "U27'
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U13-1(-201.222mm,70.754mm) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad U13-2(-201.222mm,70.254mm) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad U26-7(-128.865mm,49.029mm) on Top Layer And Text "C52'
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad U26-8(-127.595mm,49.029mm) on Top Layer And Text "C52'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad U3-6(-135.871mm,42.754mm) on Top Layer And Text "C8'
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Pad U3-7(-135.871mm,43.254mm) on Top Layer And Text "C8'

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (-167.915mm,24.247mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (-70.7mm,17.354mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-107.5mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-130.9mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-173.5mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-196.9mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-41.5mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "5" (-64.825mm,83.294mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "8" (-61.5mm,26.454mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.163mm < 0.254mm) Between Text "C46" (-160.012mm,41.927mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "C8" (-136.64mm,42.215mm) on Top Overlay And Track