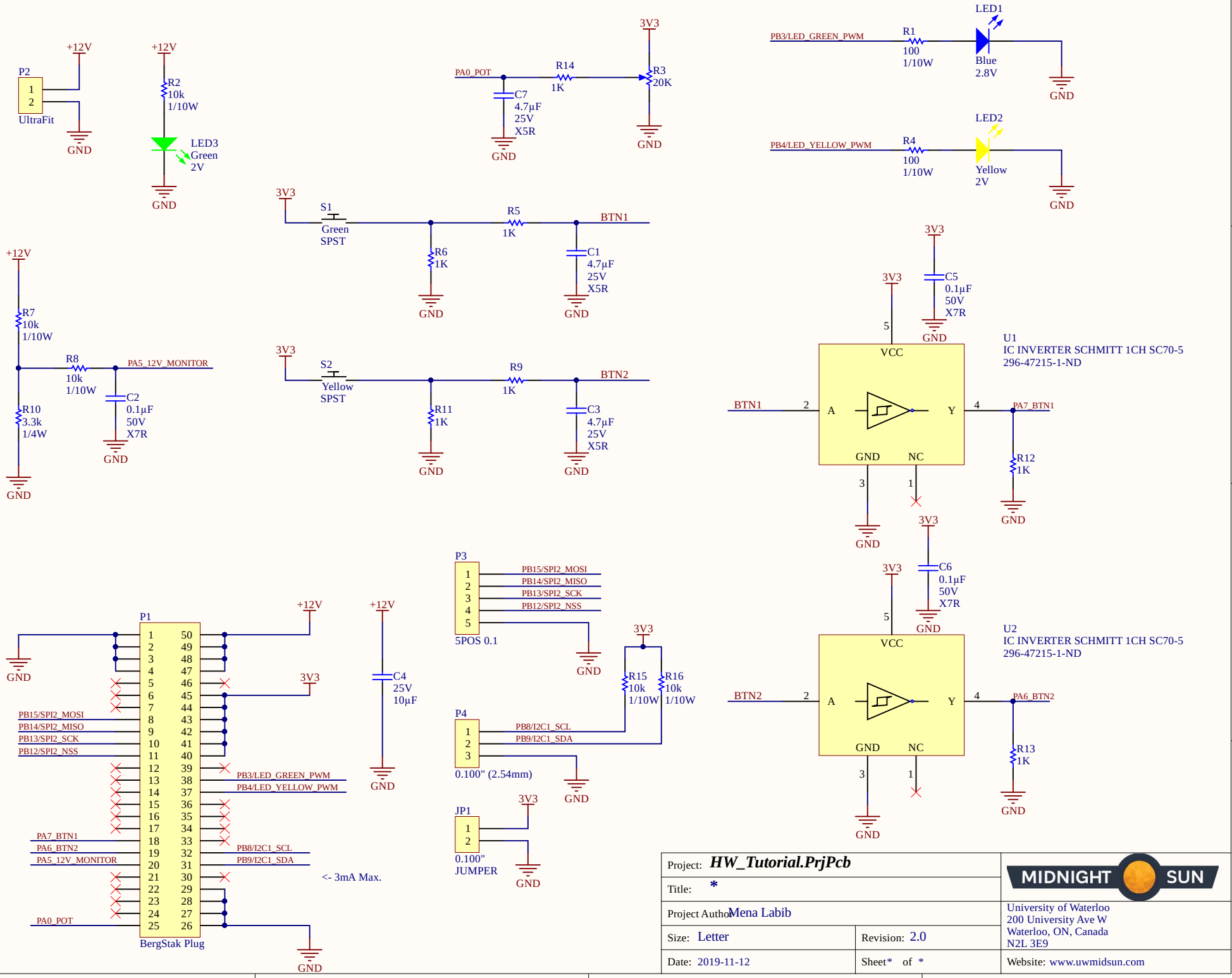
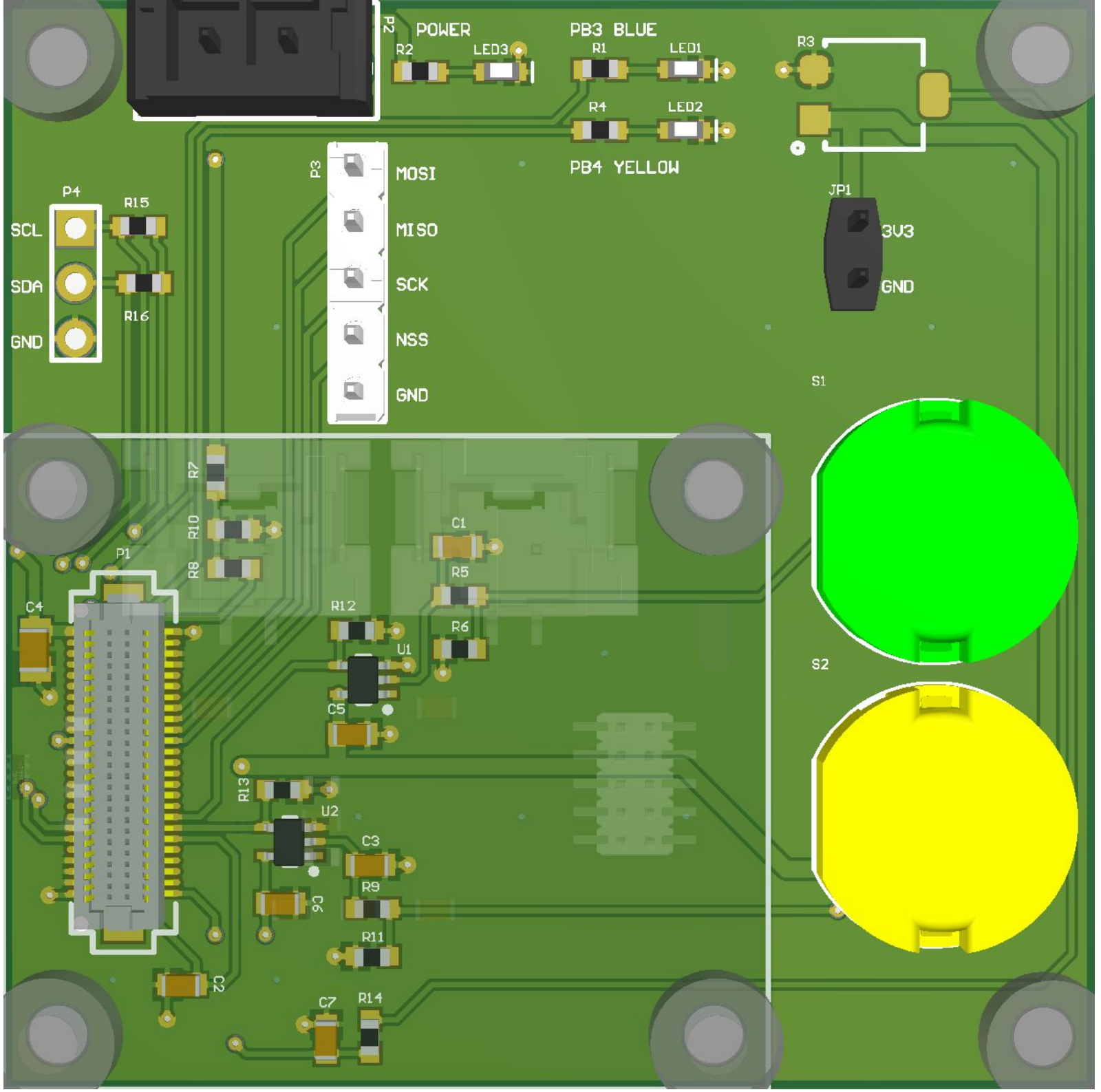
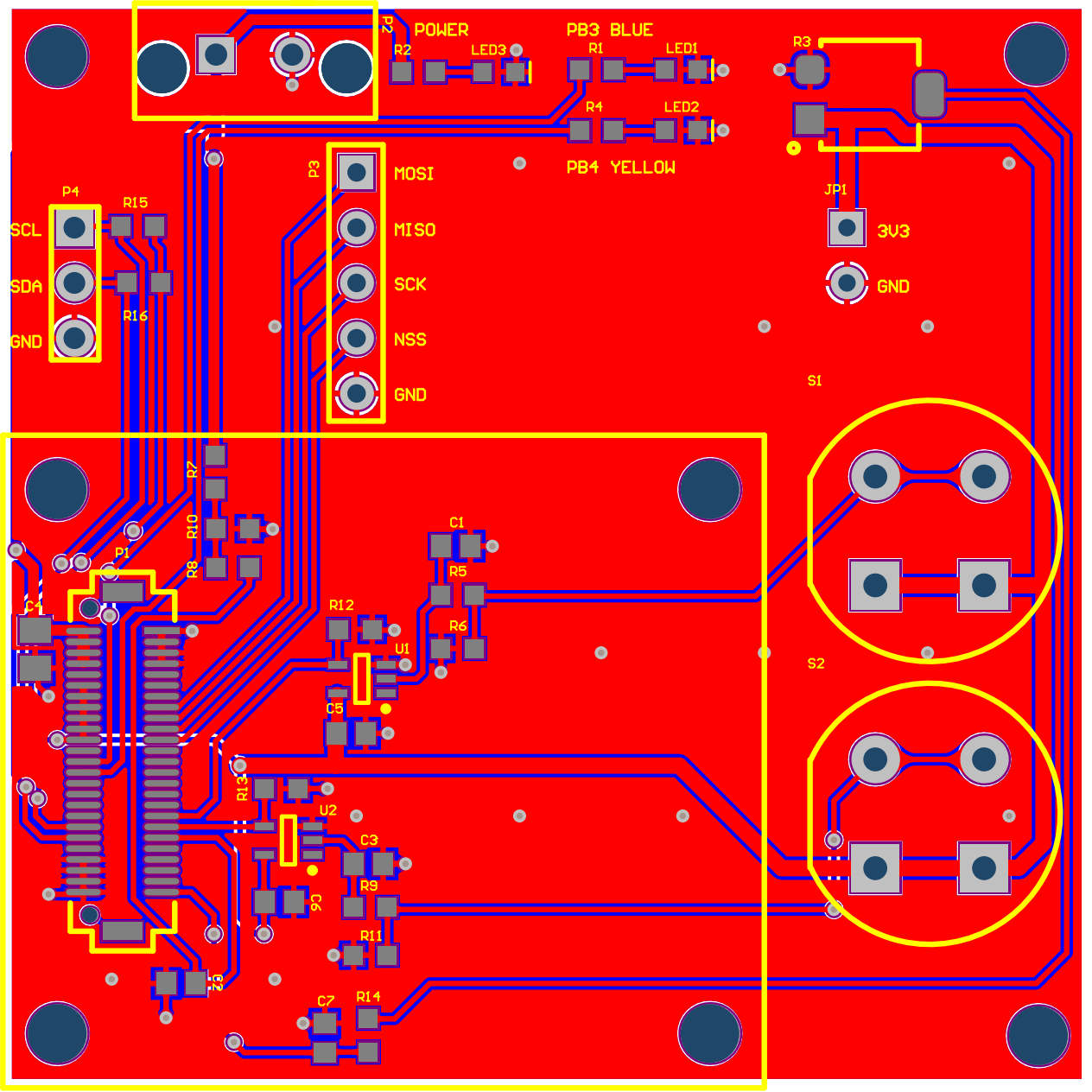

P2
1
2
UltraFit
+12V
GND
+12V
R2
10k
1/10W
LED3
Green
2V
GND
3V3
PA0_POT
R14
1K
R3
20K
C7
4.7µF
25V
X5R
GND
GND
LED1
PB3/LED_GREEN_PWM
R1
100
1/10W
Blue
2.8V
GND
LED2
PB4/LED_YELLOW_PWM
R4
100
1/10W
Yellow
2V
GND
3V3
S1
Green
SPST
R5
1K
BTN1
R6
1K
C1
4.7µF
25V
X5R
GND
GND
+12V
R7
10k
1/10W
R8
10k
1/10W
PA5_12V_MONITOR
C2
0.1µF
50V
X7R
R10
3.3k
1/4W
GND
GND
3V3
S2
Yellow
SPST
R9
1K
BTN2
R11
1K
C3
4.7µF
25V
X5R
GND
GND
3V3
C5
0.1µF
50V
X7R
GND
5
VCC
U1
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
BTN1
2
A
Y
4
PA7_BTN1
GND
NC
3
1
R12
1K
GND
GND
3V3
C6
0.1µF
50V
X7R
GND
5
VCC
U2
IC INVERTER SCHMITT 1CH SC70-5
296-47215-1-ND
BTN2
2
A
Y
4
PA6_BTN2
GND
NC
3
1
R13
1K
GND
GND
P1
BergStak Plug
+12V
3V3
GND
PB15/SPI2_MOSI
PB14/SPI2_MISO
PB13/SPI2_SCK
PB12/SPI2_NSS
PB3/LED_GREEN_PWM
PB4/LED_YELLOW_PWM
PB8/I2C1_SCL
PB9/I2C1_SDA
PA7_BTN1
PA6_BTN2
PA5_12V_MONITOR
PA0_POT
<- 3mA Max.
+12V
C4
25V
10µF
GND
P3
5POS 0.1
PB15/SPI2_MOSI
PB14/SPI2_MISO
PB13/SPI2_SCK
PB12/SPI2_NSS
GND
3V3
R15
10k
1/10W
R16
10k
1/10W
P4
PB8/I2C1_SCL
PB9/I2C1_SDA
0.100" (2.54mm)
GND
JP1
0.100"
JUMPER
3V3
GND
Project: HW_Tutorial.PrjPcb
Title: *
Project Author: Mena Labib
Size: Letter
Revision: 2.0
Date: 2019-11-12
Sheet* of *
MIDNIGHT SUN
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9
Website: www.uwmidsun.com

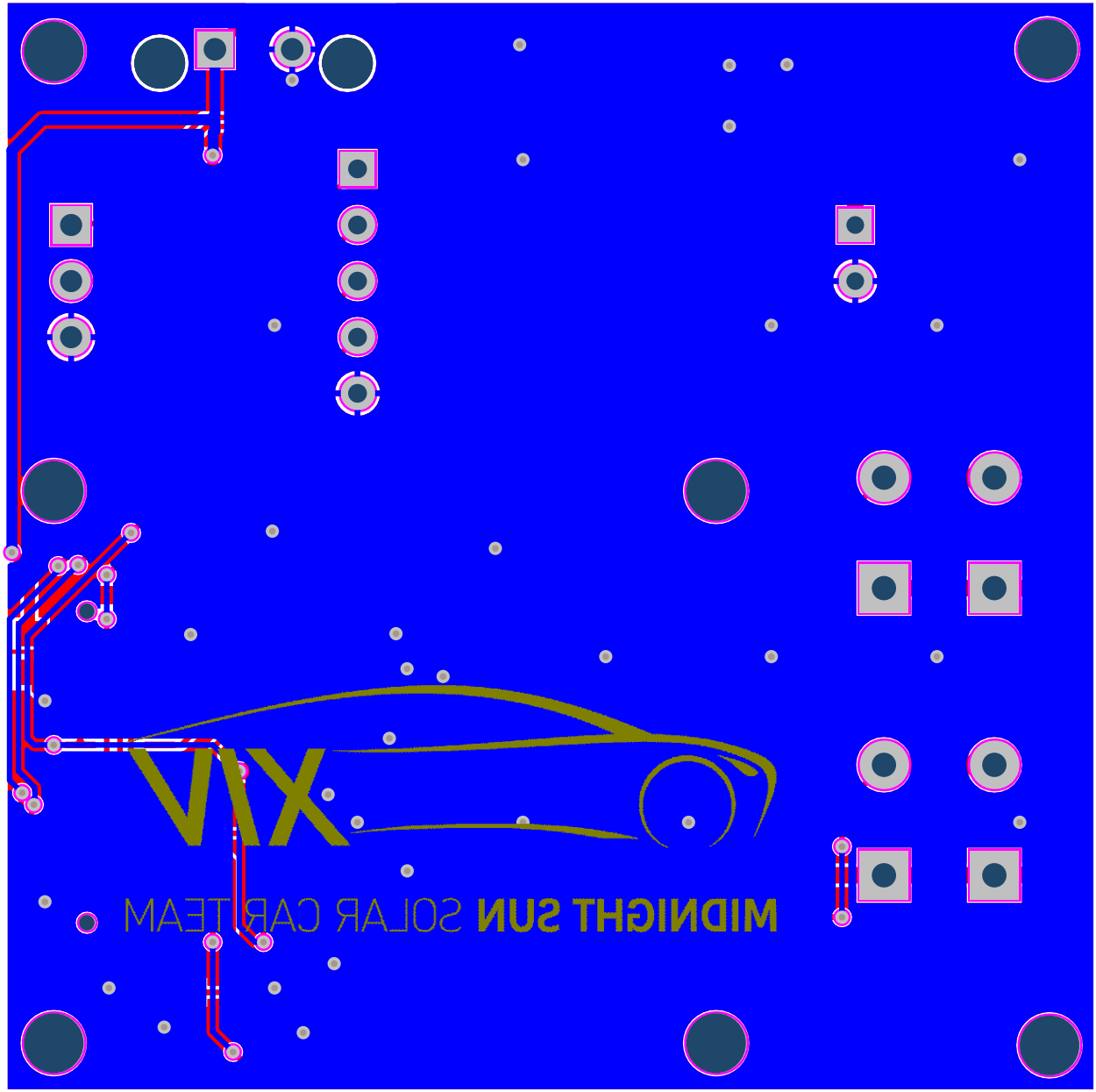
Bill of Materials

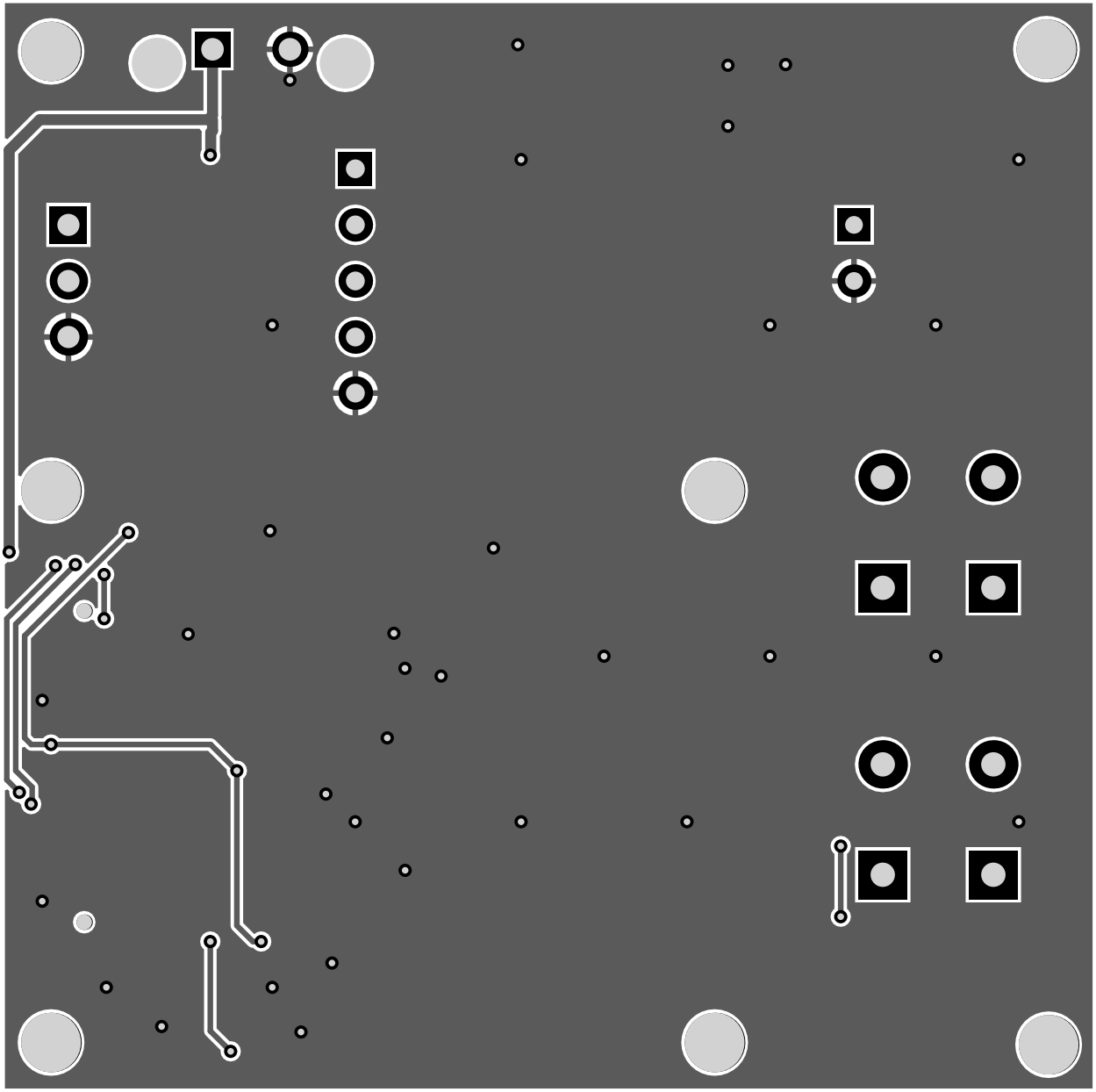
Project:	HW_Tutorial.PrjPcb
Revision:	2.0
Project Lead:	Mena Labib
Generated On:	2019-11-12 1:06 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	35

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Pric
CAP CER 4.7UF 25V 10% X5R 0603	C1, C3, C7	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.48942
CAP CER 0.1UF 50V 10% X7R 0603	C2, C5, C6	Kyocera AVX	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.19841
CAP CER 10uF 25V 10% X5R 0805	C4	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.56878
CONN 2POS JUMPER 0.1"	JP1	Omron	XG8T-0231	Digi-Key	XG8T-0231-ND	0.25132
LED BLUE CLEAR 2.8V 0603	LED1	Vishay Lite-On	LTST-C193TBKT-5A	Digi-Key	160-1827-1-ND	0.59524
LED YELLOW CLEAR 2.1V 0603	LED2	Wurth Electronics	150060YS75000	Digi-Key	732-4981-1-ND	0.18518
LED GREEN CLEAR 2V 0603	LED3	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18518
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.9
CONN 2POS ULTRA-FIT 0.138"	P2	Molex	1722861302	Digi-Key	WM11673-ND	1.93
CONN 5POS HEADR MALE 0.1in	P3	Molex	22-28-4050	Digi-Key	WM50014-05-ND	0.31746
CONN 3POS HEADR MALE 0.1"	P4	Wurth Electronics	61300311121	Digi-Key	732-5316-ND	0.17196
RES 100 OHM 1% 1/10W 0603	R1, R4	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13227
RES 10K OHM 1% 1/10W 0603	R2, R7, R8, R15, R16	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13227
POT 20k OHM 20% 1/4W	R3	TT BI	23BR20KLFTR	Digi-Key	987-1016-1-ND	1.68
RES 1K OHM 5% 1/10W 0603	R5, R6, R9, R11, R12, R13, R14	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.13227
RES 3.3K OHM 1% 1/4W 0603	R10	Panasonic	ERJ-PA3F3301V	Digi-Key	P3.3KBYCT-ND	0.21164
SW SPST-NO 0.1A 32V D6 Series Green	S1	ITT C&K	D6R50F1LFS	Digi-Key	401-1976-ND	1.59
SW SPST-NO 0.1A 32V D6 Series Yellow	S2	ITT C&K	D6R30F1LFS	Digi-Key	401-1974-ND	1.59
IC INVERTER SCHMITT 1CH SC70-5	U1, U2	Texas Instruments	SN74LVC1G14QDCKRQ1	Digi-Key	296-47215-1-ND	0.47619


P2
POWER
R2
LED3
PB3 BLUE
R1
LED1
R4
LED2
PB4 YELLOW
R3
P3
MOSI
MISO
SCK
NSS
GND
P4
SCL
SDA
GND
R15
R16
JP1
3V3
GND
S1
S2
P1
C4
R7
R10
R8
C1
R5
R12
R6
U1
C5
R13
U2
C3
R9
C6
R11
C2
C7
R14


P2
POWER
R2
LED3
PB3 BLUE
R1
LED1
R4
LED2
PB4 YELLOW
R3
P3
MOSI
MISO
SCK
NSS
GND
P4
SCL
SDA
GND
R15
R16
JP1
3V3
GND
S1
S2
P1
C1
R5
R6
R12
U1
C5
R13
U2
C3
R9
C6
R11
C7
R14
R7
R10
R8
C4
C2


MIDNIGHT SUN SOLAR CAR TEAM



Electrical Rules Check Report

Class	Document	Message
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 (Inferred) in Alternate 1 of part R3
Warning	hw_tutorial.SchDoc	Extra Pin R3-2 in Normal of part R3
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 (Inferred) in Alternate 1 of part R3
Warning	hw_tutorial.SchDoc	Extra Pin R3-3 in Normal of part R3

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXII_

Warnings 0
Rule Violations 111

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.152mm) (All)	49
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	35
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	8
Silk to Silk (Clearance=0.254mm) (All),(All)	1
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	18
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	111

Minimum Annular Ring (Minimum=0.152mm) (All)
Minimum Annular Ring: (0.15mm < 0.152mm) Via (0.606mm,24.719mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.068mm,13.832mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (1.6mm,13.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (10.621mm,2.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (10.9mm,14.814mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.4mm,25.68mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12.5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (12mm,7.075mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.3mm,46.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (13.8mm,2.975mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.925mm,13.754mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (15.2mm,6.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (16.25mm,12.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (17.7mm,16.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.508mm,10.3mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.5mm,19.45mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18mm,21.037mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.101mm,8.9mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.1mm,18mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.5mm,16mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.7mm,24.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (20.133mm,19.1mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (22.5mm,24.9mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.6mm,47.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,12.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.75mm,42.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (3.6mm,24.15mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.25mm,12.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,44.012mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.1mm,46.77mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35.708mm,46.802mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (35mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.2mm,11.4mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (38.2mm,8.2mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (4.9mm,21.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (4.9mm,23.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,20mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.5mm,35mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,12.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (46.25mm,42.5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (5mm,5mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (6mm,25.6mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (7.5mm,3.225mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (8.7mm,21mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.7mm,42.7mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.7mm,7.075mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top Layer,

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(20.133mm,24.9mm) on Top Layer And Pad C1-2(21.483mm,24.9mm)
Minimum Solder Mask Sliver Constraint: (0.089mm < 0.3mm) Between Pad C1-2(21.483mm,24.9mm) on Top Layer And Via (22.5mm,24.9mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(8.85mm,4.8mm) on Top Layer And Pad C2-2(7.5mm,4.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(16.125mm,10.3mm) on Top Layer And Pad C3-2(17.475mm,10.3mm)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad C3-2(17.475mm,10.3mm) on Top Layer And Via (18.508mm,10.3mm) from
Minimum Solder Mask Sliver Constraint: (0.217mm < 0.3mm) Between Pad C4-2(1.476mm,19.295mm) on Top Layer And Via (2.1mm,18mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(15.325mm,16.3mm) on Top Layer And Pad C5-2(16.675mm,16.3mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad C5-2(16.675mm,16.3mm) on Top Layer And Via (17.7mm,16.3mm) from Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(12.025mm,8.546mm) on Top Layer And Pad C6-2(13.375mm,8.546mm)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(14.8mm,1.625mm) on Top Layer And Pad C7-2(14.8mm,2.975mm) or
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.3mm) Between Pad C7-2(14.8mm,2.975mm) on Top Layer And Via (13.8mm,2.975mm) from Top
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED1-2(31.939mm,46.805mm) on Top Layer And Via (33.1mm,46.77mm)
Minimum Solder Mask Sliver Constraint: (0.258mm < 0.3mm) Between Pad LED2-2(31.939mm,44.012mm) on Top Layer And Via (33.1mm,44.012mm)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad LED3-2(23.55mm,46.7mm) on Top Layer And Via (23.6mm,47.7mm) from
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And Pad P1-(5.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.112mm < 0.3mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And Via (4.9mm,21.7mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And Pad P1-(5.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.3mm) Between Pad P1-(5.5mm,22.8mm) on Top Layer And Via (4.9mm,21.7mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad P1-1(7.3mm,21mm) on Top Layer And Via (8.7mm,21mm) from Top Layer to
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad P1-2(7.3mm,20.5mm) on Top Layer And Via (8.7mm,21mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-39(3.7mm,15.5mm) on Top Layer And Via (2.5mm,16mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.09mm < 0.3mm) Between Pad P1-41(3.7mm,16.5mm) on Top Layer And Via (2.5mm,16mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.297mm < 0.3mm) Between Pad P1-44(3.7mm,18mm) on Top Layer And Via (2.1mm,18mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.237mm < 0.3mm) Between Pad P1-50(3.7mm,21mm) on Top Layer And Via (4.9mm,21.7mm) from Top Layer
Minimum Solder Mask Sliver Constraint: (0.092mm < 0.3mm) Between Pad P2-2(13.3mm,47.495mm) on Multi-Layer And Via (13.3mm,46.1mm) from Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.3mm) Between Pad R10-2(11.325mm,25.7mm) on Top Layer And Via (12.4mm,25.68mm) from
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad R12-1(16.975mm,21.075mm) on Top Layer And Via (18mm,21.037mm) from
Minimum Solder Mask Sliver Constraint: (0.239mm < 0.3mm) Between Pad R3-3(37.1mm,46.8mm) on Top Layer And Via (35.708mm,46.802mm) from
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.3mm) Between Pad R6-1(20.133mm,20.2mm) on Top Layer And Via (20.133mm,19.1mm) from
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-1(17.6mm,18.15mm) on Top Layer And Pad U1-2(17.6mm,18.8mm) or
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U1-2(17.6mm,18.8mm) on Top Layer And Pad U1-3(17.6mm,19.45mm) or
Minimum Solder Mask Sliver Constraint: (0.126mm < 0.3mm) Between Pad U1-2(17.6mm,18.8mm) on Top Layer And Via (18.5mm,19.45mm) from Top
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-1(14.225mm,10.725mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.3mm) Between Pad U2-2(14.225mm,11.375mm) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.3mm) Between Via (2.7mm,24.1mm) from Top Layer to Bottom Layer And Via (3.6mm,24.15mm)

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.082mm < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.144mm < 0.178mm) Between Pad P4-1(3.286mm,39.54mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P4-2(3.286mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P4-2(3.286mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.088mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.169mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad P4-3(3.286mm,34.46mm) on Multi-Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.183mm < 0.254mm) Between Text "P2" (17.477mm,49.2mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "GND" (0.4mm,34.06mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "SCL" (0.4mm,39.2mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.3mm < 0.406mm) Between Board Edge And Text "SDA" (0.4mm,36.6mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (0.5mm,14.4mm)(0.5mm,21.7mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (0.5mm,14.4mm)(1.068mm,13.832mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (0.5mm,21.7mm)(2.633mm,23.833mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Track (0.606mm,24.719mm)(0.606mm,42.918mm) on Bottom
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Track (0.606mm,24.719mm)(1.4mm,23.926mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.356mm < 0.406mm) Between Board Edge And Track (0.606mm,42.918mm)(1.993mm,44.305mm) on Bottom
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(0mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,0mm)(35mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (0mm,30mm)(35mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (13.3mm,49.865mm)(17.13mm,49.865mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (17.13mm,44.565mm)(17.13mm,49.865mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (35mm,0mm)(35mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (6.055mm,44.565mm)(6.055mm,49.865mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (6.055mm,49.865mm)(14.3mm,49.865mm) on Top
Board Outline Clearance(Outline Edge): (0.306mm < 0.406mm) Between Board Edge And Via (0.606mm,24.719mm) from Top Layer to Bottom Layer