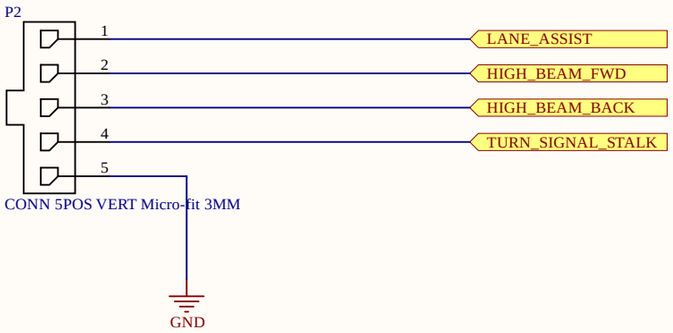
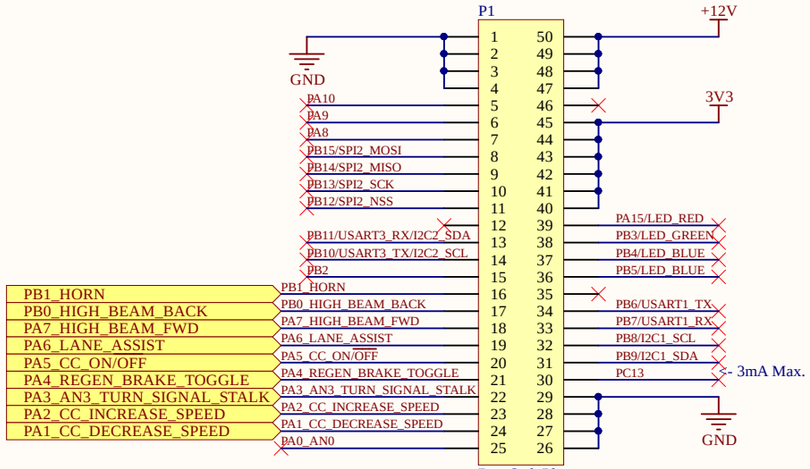
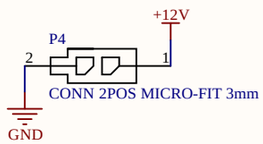
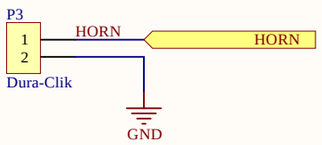
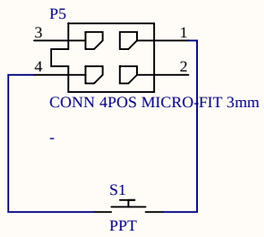










Button for Push-to-Talk (PPT)

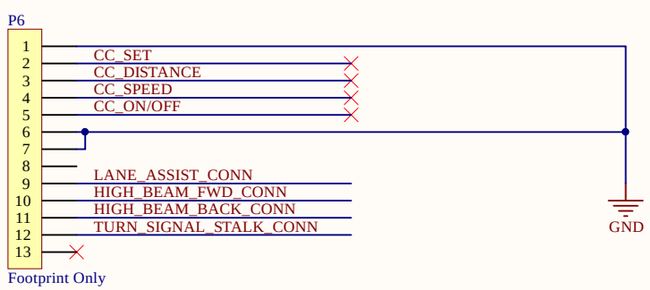
Standoffs

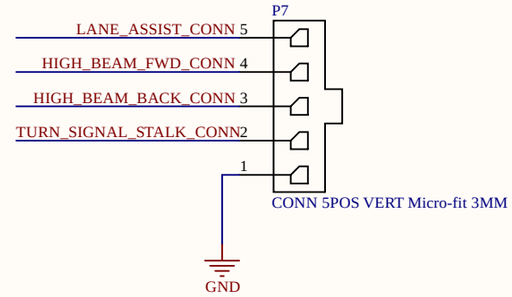
PROJECT	MSXIV_SteeringWheelInterfaceBoard.PrjPcb		
DOCUMENT	Steering Wheel Interface - Mezzanine		
PART NUMBER	MS-ELE0008	VARIANT	[No Variations]
DRAWN BY	Jenny Xia	REVISION	4.0
LAST MODIFIED	2020-05-28	SHEET	1 OF 5

MIDNIGHT SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

Steering Stalk Connector





PROJECT	MSXIV_SteeringWheelInterfaceBoard.PrjPcb		
DOCUMENT	Steering Wheel - Steering Stalk Connector		
PART NUMBER	MS-ELE0008	VARIANT	[No Variations]
DRAWN BY	Jenny Xia	REVISION	4.0
LAST MODIFIED	2020-05-28	SHEET	2 OF 5

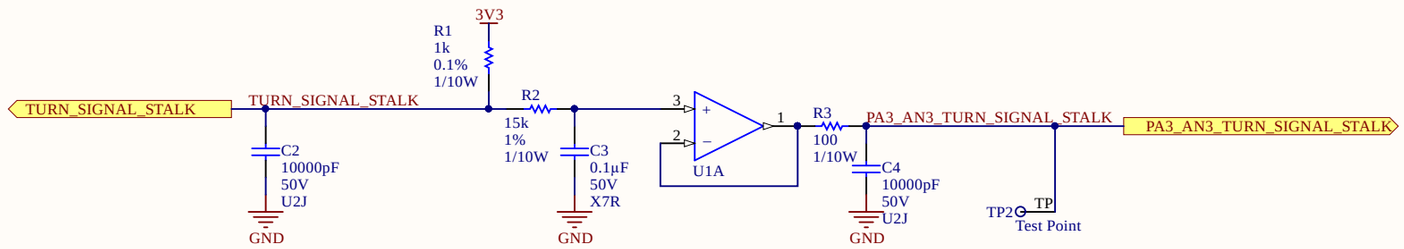
MIDNIGHT SUN

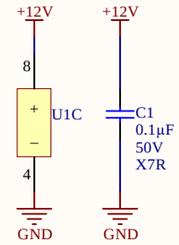
Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

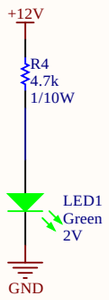
fc = 116.17[Hz]

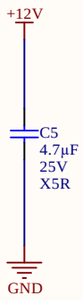
fc = 159154.94[Hz]

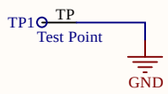
RC Low Pass Filter

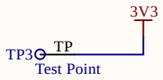


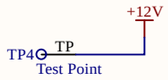










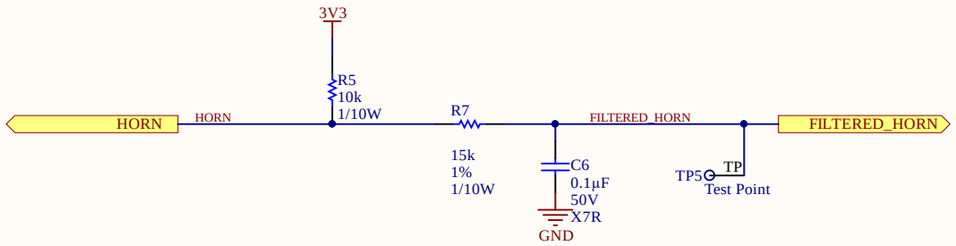


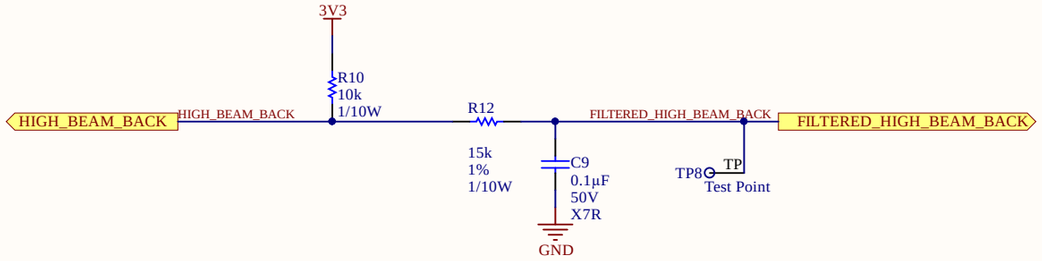
PROJECT	MSXIV_SteeringWheelInterfaceBoard.PrjPcb		
DOCUMENT	Steering Wheel Interface - Analog Inputs		
PART NUMBER	MS-ELE0008	VARIANT	[No Variations]
DRAWN BY	Jenny Xia	REVISION	4.0
LAST MODIFIED	2020-05-28	SHEET	3 OF 5

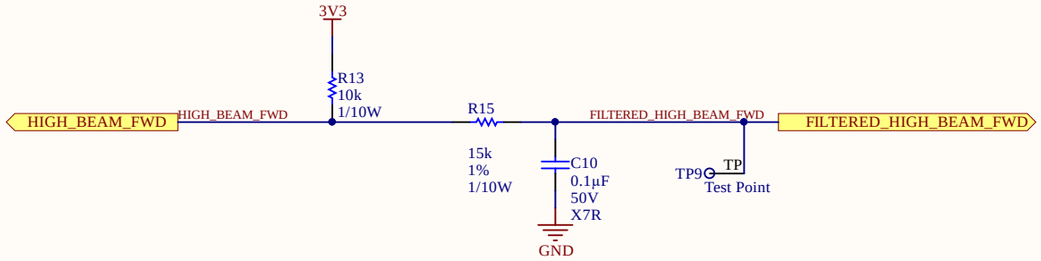
MIDNIGHT SUN

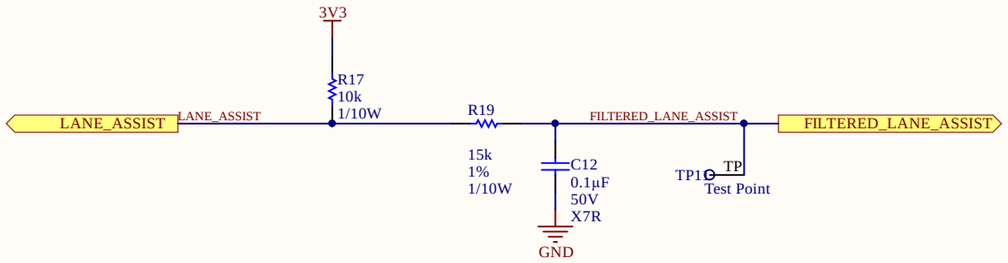
Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

Horn and Steering Stalk Inputs

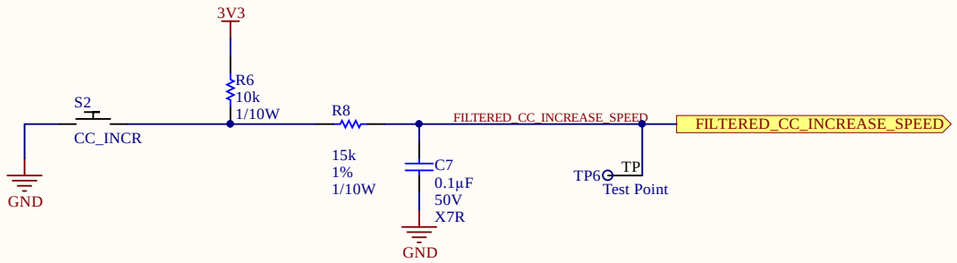


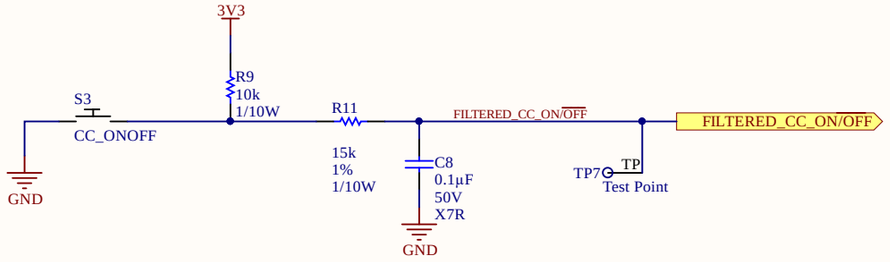


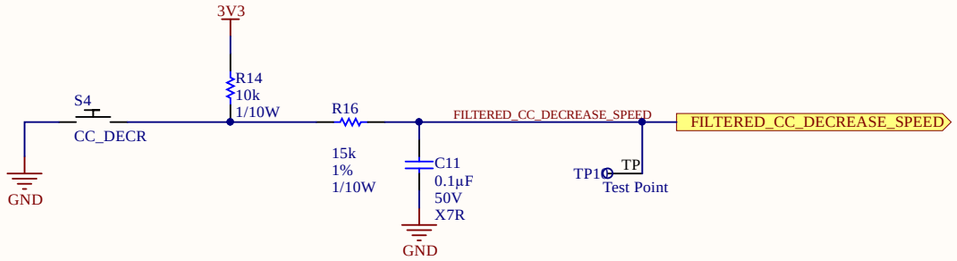


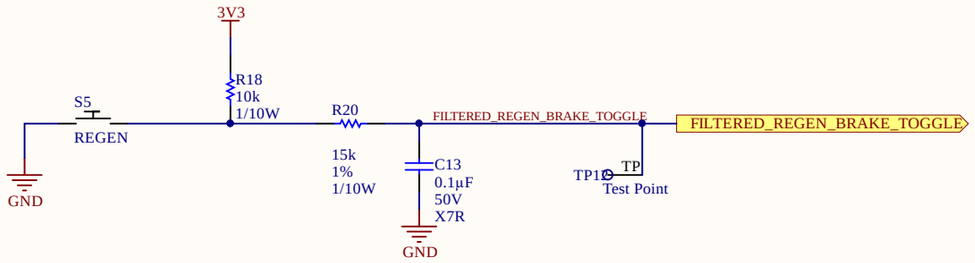


Steering Wheel Button Inputs







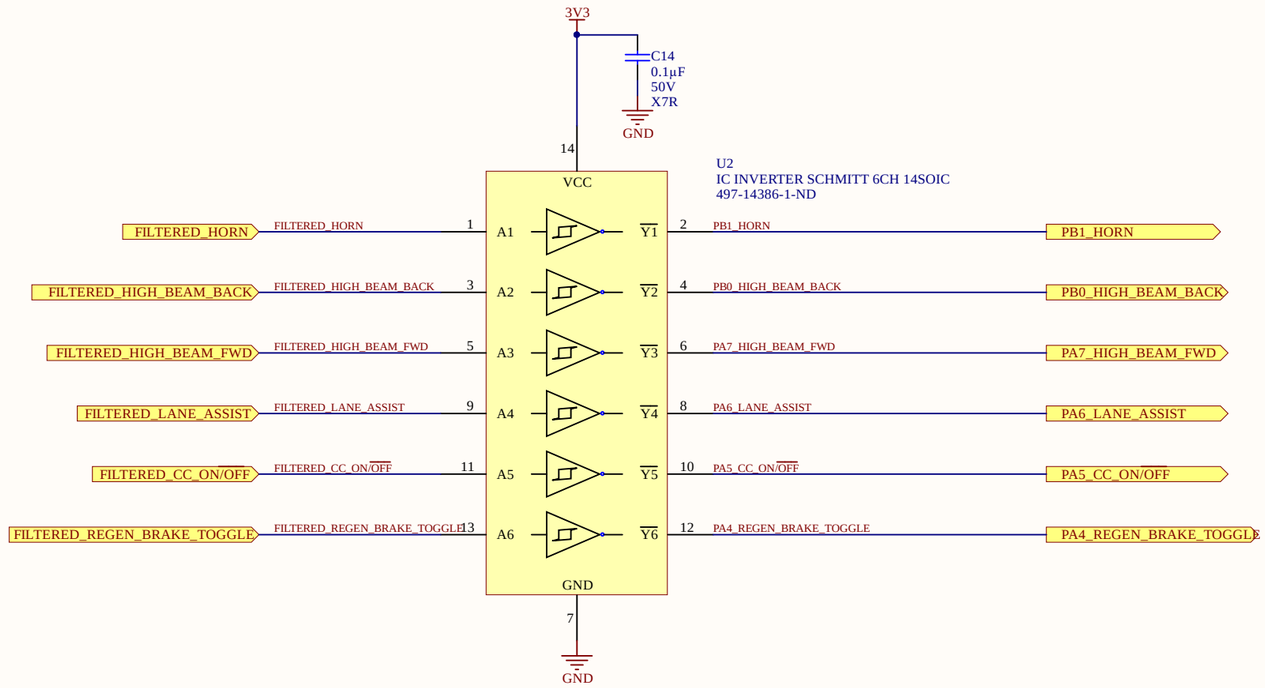


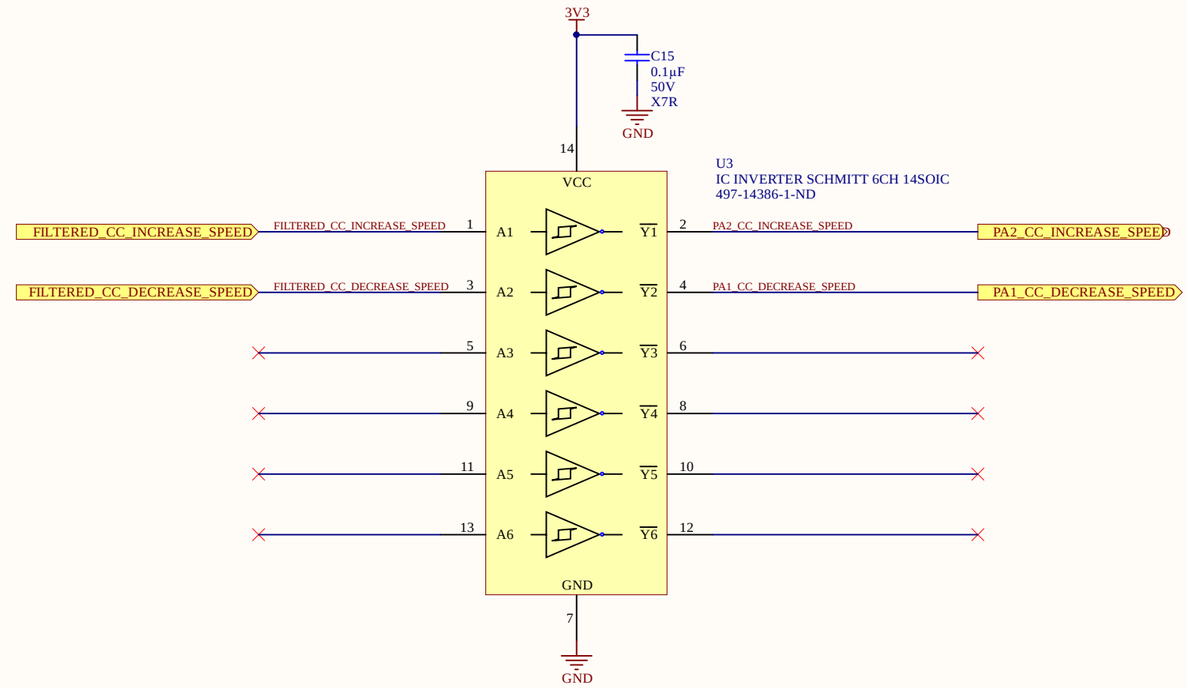
fc = 116.17[Hz]

PROJECT	MSXIV_SteeringWheelInterfaceBoard.PrjPcb		
DOCUMENT	Steering Wheel Interface - Digital Inputs		
PART NUMBER	MS-ELE0008	VARIANT	[No Variations]
DRAWN BY	Jenny Xia	REVISION	4.0
LAST MODIFIED	2020-05-28	SHEET	4 OF 5

MIDNIGHT SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com





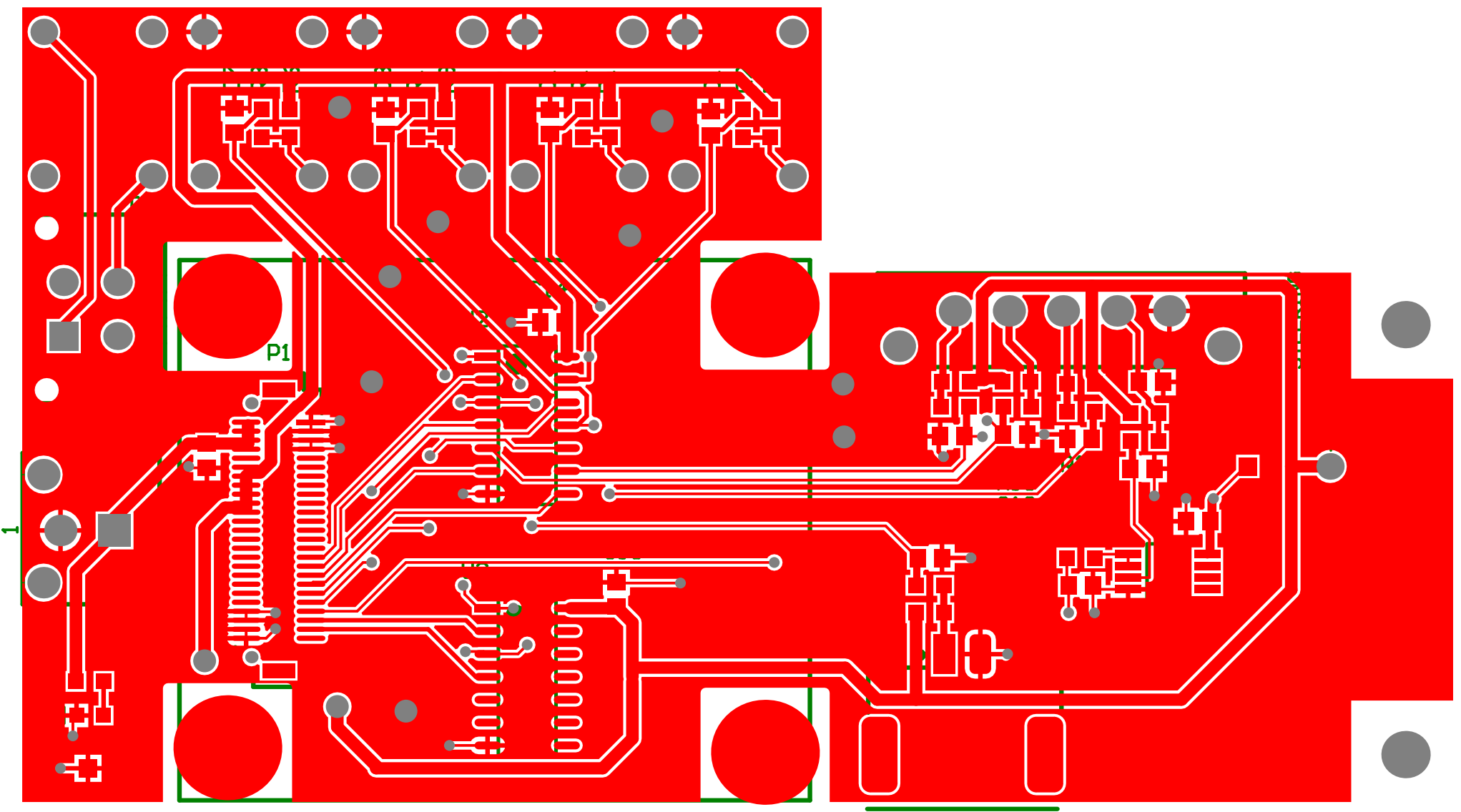
PROJECT	MSXIV_SteeringWheelInterfaceBoard.PrjPcb		MIDNIGHT SUN
DOCUMENT	Steering Wheel Interface - Schmitt Inverters		
PART NUMBER	MS-ELE0008	VARIANT	[No Variations]
DRAWN BY	Jenny Xia	REVISION	4.0
LAST MODIFIED	2020-05-28	SHEET 5 OF 5	

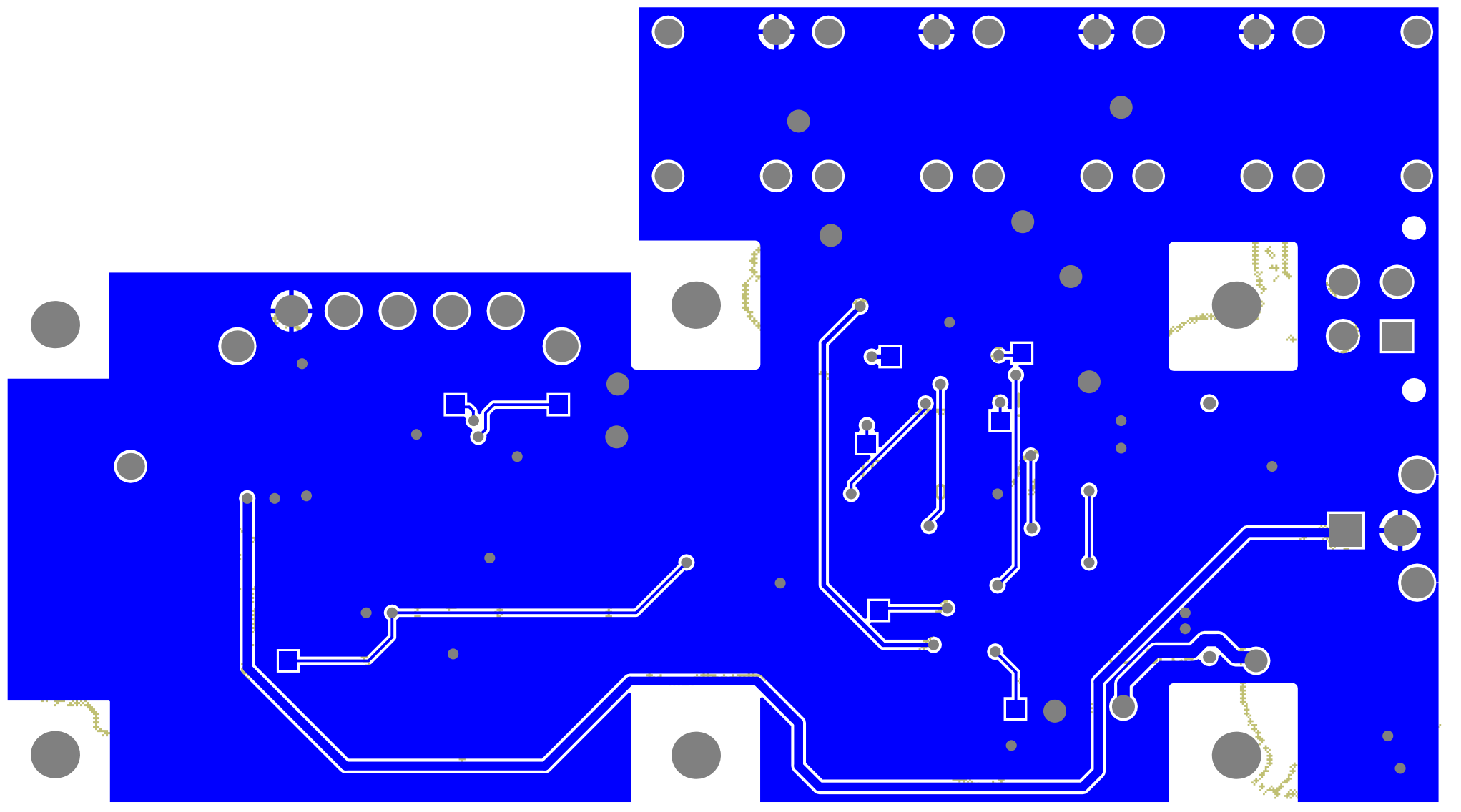
Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

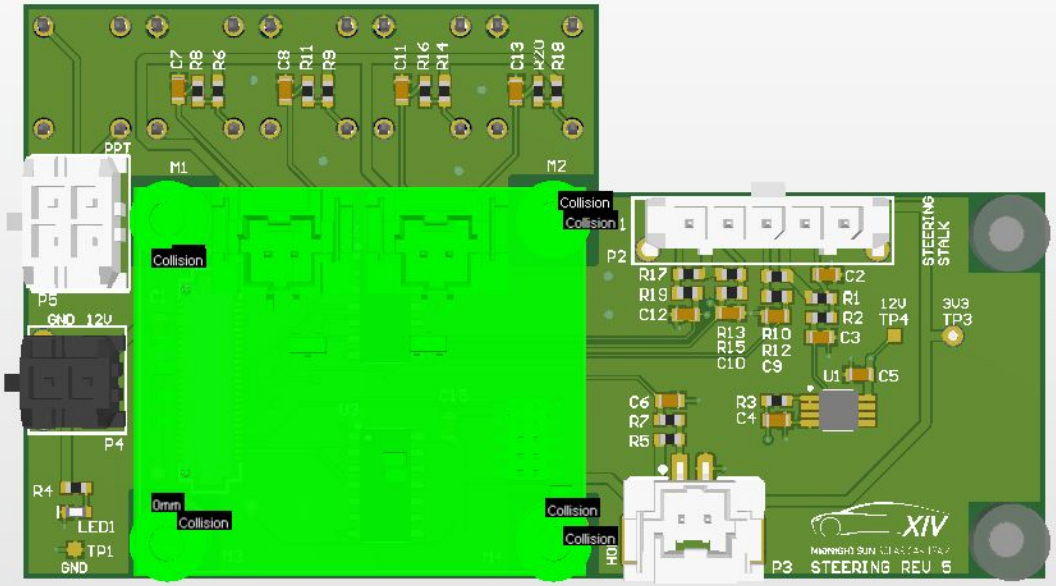
Bill of Materials

Project:	XIV_SteeringWheelInterfaceBoard.PrjPcb
Revision:	4.0
Project Lead:	Jenny Xia
Generated On:	2020-05-28 10:07 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	53

LibRef	Designator	Manufacturer 1	M
CAP CER 0.1UF 50V 10% X7R 0603	C3, C6, C7, C8, C9, C10, C11, C12, C13, C14	AVX Corporation	
CAP CER 10nF 50V 5% X7R 0603	C2, C4	KEMET	
CAP CER 4.7UF 25V 10% X5R 0603	C5	Murata Electronics North America	
LED GREEN CLEAR 2V 0603	LED1		


P1
1




C7
R8
R6
C8
R11
R9
C11
R16
R14
C13
R20
R18
PPT
M1
M2
Collision
Collision
Collision
P5
GND
12V
P4
R4
LED1
TP1
GND
0mm
Collision
Collision
Collision
HD
P2
R17
R19
C12
C2
R1
R2
C3
12V
TP4
3V3
TP3
R13
R15
C10
R10
R12
C9
U1
C5
C6
R7
R5
R3
C4
STEERING
STALK
P3
STEERING REV 5

Electrical Rules Check Repor

Class	Document	Message
Warning	Steering Wheel Carrier Boar Mezzanine.SchDoc	Component U1 IC OP AMP DUAL GP RR 10MHZ 8-VSSOP has unus sub-part (2)
Warning	Steering Wheel Interface Analog Inputs.SchDoc	Net NetC3_1 has no driving source (Pin C3-1,Pin R2-1,Pin U1-
Warning	Steering Wheel Interface Digital Inputs.SchDoc	Off grid Net Label FILTERED_REGEN_BRAKE_TOGGLE 10879.956mil,2300mil

Design Rules Verification Repor

Filename : Z:\hardware\MSXIV_SteeringWheelInterfaceBoard\SteeringWheelBoard.PcbD

Warnings 0
Rule Violations 196

Warnings	
Tota	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(Al	1
Short-Circuit Constraint (Allowed=No) (All),(Al	0
Un-Routed Net Constraint ((All)	6
Modified Polygon (Allow modified: No), (Allow shelved: N	0
Width Constraint (Min=0.154mm) (Max=2.54mm) (Preferred=0.2mm) (A	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254m	0
Minimum Annular Ring (Minimum=0.152mm) (Al	42
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (Al	0
Hole To Hole Clearance (Gap=0.254mm) (All),(A	4
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(Al	17
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(A	97
Silk to Silk (Clearance=0.254mm) (All),(Al	11
Net Antennae (Tolerance=0mm) (Al	0
Board Clearance Constraint (Gap=0mm) (Al	18
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (A	0
Tota	196

Clearance Constraint (Gap=0.152mm) (All),(Al
Clearance Constraint: (0.048mm < 0.152mm) Between Pad M4-(41.656mm,3.175mm) on Top Layer And Track (0mm,0mm)(80.168mm,0mm) on Keep-Out L

Un-Routed Net Constraint ((All)
Un-Routed Net Constraint: Net NetR14_2 Between Pad S4-2(28.29mm,35.18mm) on Multi-Layer And Pad R16-2(31.524mm,37.338mm) on Top La
Un-Routed Net Constraint: Net NetR6_2 Between Pad S2-2(10.51mm,35.18mm) on Multi-Layer And Pad R8-2(13.728mm,37.338mm) on Top La
Un-Routed Net Constraint: Net NetP5_4 Between Pad S1-1(1.62mm,43.18mm) on Multi-Layer And Pad S1-1(7.62mm,43.18mm) on Multi-La
Un-Routed Net Constraint: Net NetP5_1 Between Pad S1-2(1.62mm,35.18mm) on Multi-Layer And Pad S1-2(7.62mm,35.18mm) on Multi-La
Un-Routed Net Constraint: Net NetR9_2 Between Pad S3-2(19.4mm,35.18mm) on Multi-Layer And Track (22.352mm,37.338mm)(22.378mm,37.312mm) on Top L
Un-Routed Net Constraint: Net NetR18_2 Between Pad S5-2(37.18mm,35.18mm) on Multi-Layer And Pad S5-2(43.18mm,35.18mm) on Multi-La

Minimum Annular Ring (Minimum=0.152mm) (Al
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.478mm,10.033mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (14.478mm,10.922mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.034mm,20.066mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (18.034mm,21.59mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (19.812mm,13.716mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (19.812mm,17.688mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (2.54mm,2.286mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (22.987mm,15.621mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.049mm,19.646mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (23.876mm,24.13mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (24.13mm,3.556mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (24.748mm,22.606mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (24.825mm,25.224mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (24.892mm,12.446mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (24.892mm,17.526mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (25.019mm,8.763mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.559mm,27.051mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (27.686mm,11.176mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.067mm,23.622mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.448mm,9.144mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.702mm,15.748mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (28.892mm,22.543mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (3.228mm,4.086mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (31.877mm,25.146mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (32.148mm,21.336mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (32.512mm,27.94mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (33.02mm,17.526mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (36.957mm,12.573mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (42.164mm,13.716mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (51.562mm,19.596mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (53.086mm,13.97mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (53.721mm,20.701mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (53.975mm,21.59mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (55.118mm,8.636mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (57.15mm,20.828mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (58.507mm,10.922mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La

Minimum Annular Ring (Minimum=0.152mm) (Al
Minimum Annular Ring: (0.15mm < 0.152mm) Via (59.944mm,10.922mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (63.262mm,17.415mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (63.5mm,24.756mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (65.024mm,17.272mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (66.548mm,17.272mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La
Minimum Annular Ring: (0.15mm < 0.152mm) Via (9.652mm,19.05mm) from Top Layer to Bottom Layer (Annular Ring=0.15mm) On (Top La

Hole To Hole Clearance (Gap=0.254mm) (All),(Al
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(11.644mm,28.008mm) on Multi-Layer And Pad M1-(11.811mm,27.94mm) on Multi-Layer Pa
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(11.644mm,3.008mm) on Multi-Layer And Pad M3-(11.811mm,3.429mm) on Multi-Layer Pa
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(41.644mm,28.008mm) on Multi-Layer And Pad M2-(41.644mm,28.008mm) on Multi-Layer Pa
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-(41.644mm,3.008mm) on Multi-Layer And Pad M4-(41.656mm,3.175mm) on Multi-Layer Pa

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(Al
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(54.864mm,20.828mm) on Top Layer And Pad C10-2(56.214mm,20.828mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(10.668mm,20.32mm) on Top Layer And Pad C1-2(10.668mm,18.97mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(29.718mm,37.512mm) on Top Layer And Pad C11-2(29.718mm,38.862mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(52.724mm,20.72mm) on Top Layer And Pad C12-2(51.374mm,20.72mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(38.636mm,37.425mm) on Top Layer And Pad C13-2(38.636mm,38.775mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(30.52mm,27.051mm) on Top Layer And Pad C14-2(29.17mm,27.051mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C15-1(33.401mm,11.263mm) on Top Layer And Pad C15-2(33.401mm,12.613mm) on Top Laye
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(62.406mm,23.744mm) on Top Layer And Pad C2-2(63.756mm,23.744mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(61.912mm,18.926mm) on Top Layer And Pad C3-2(63.262mm,18.926mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(58.507mm,12.446mm) on Top Layer And Pad C4-2(59.857mm,12.446mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(66.374mm,16.002mm) on Top Layer And Pad C5-2(65.024mm,16.002mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(50.125mm,13.97mm) on Top Layer And Pad C6-2(51.475mm,13.97mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(12.192mm,37.592mm) on Top Layer And Pad C7-2(12.192mm,38.942mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(20.574mm,37.512mm) on Top Layer And Pad C8-2(20.574mm,38.862mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(59.77mm,20.574mm) on Top Layer And Pad C9-2(58.42mm,20.574mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(13.144mm,22.558mm) on Multi-Layer And Pad P1-(14.644mm,23.308mm) on Top Layer [Top S
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P1-(13.144mm,8.458mm) on Multi-Layer And Pad P1-(14.644mm,7.708mm) on Top Layer [Top S

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(A
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.178mm) Between Pad M1-(11.811mm,27.94mm) on Top Layer And Text "P1" (14.116mm,24.987mm) on Top Overl
Silk To Solder Mask Clearance Constraint: (0.12mm < 0.178mm) Between Pad M1-(11.811mm,27.94mm) on Top Layer And Track (9.144mm,0.508mm)(9.144mm,30.508mm) c
Silk To Solder Mask Clearance Constraint: (0.078mm < 0.178mm) Between Pad M1-(11.811mm,27.94mm) on Top Layer And Track (9.144mm,30.508mm)(44.144mm,30.508m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad M2-(41.644mm,28.008mm) on Top Layer And Track (44.144mm,0.508mm)(44.144mm,30.508m
Silk To Solder Mask Clearance Constraint: (0.01mm < 0.178mm) Between Pad M2-(41.644mm,28.008mm) on Top Layer And Track (9.144mm,30.508mm)(44.144mm,30.508m
Silk To Solder Mask Clearance Constraint: (0.136mm < 0.178mm) Between Pad M3-(11.811mm,3.429mm) on Top Layer And Track (9.144mm,0.508mm)(44.144mm,0.508mm) c
Silk To Solder Mask Clearance Constraint: (0.12mm < 0.178mm) Between Pad M3-(11.811mm,3.429mm) on Top Layer And Track (9.144mm,0.508mm)(9.144mm,30.508mm) c
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad M4-(41.656mm,3.175mm) on Top Layer And Track (44.144mm,0.508mm)(44.144mm,30.508m
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad M4-(41.656mm,3.175mm) on Top Layer And Track (9.144mm,0.508mm)(44.144mm,0.508mm) c
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P2-0(49.097mm,25.726mm) on Multi-Layer And Track (47.897mm,24.566mm)(47.897mm,29.76
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P2-0(49.097mm,25.726mm) on Multi-Layer And Track (47.897mm,24.566mm)(68.297mm,24.56
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P2-0(67.097mm,25.726mm) on Multi-Layer And Track (47.897mm,24.566mm)(68.297mm,24.56
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P2-0(67.097mm,25.726mm) on Multi-Layer And Track (68.297mm,24.566mm)(68.297mm,29.76
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad P2-5(64.097mm,27.686mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.009mm < 0.178mm) Between Pad P2-5(64.097mm,27.686mm) on Multi-Layer And Region (1 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.163mm < 0.178mm) Between Pad P3-3(48.006mm,3.048mm) on Top Layer And Track (47.381mm,5.378mm)(47.381mm,7.503m
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad P4-0(1.6mm,12.594mm) on Multi-Layer And Track (0.44mm,11.394mm)(0.44mm,19.794mm) o
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P4-0(1.6mm,12.594mm) on Multi-Layer And Track (0.44mm,11.394mm)(8.04mm,11.394mm) c
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad P4-0(1.6mm,18.594mm) on Multi-Layer And Track (0.44mm,11.394mm)(0.44mm,19.794mm) o
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P4-0(1.6mm,18.594mm) on Multi-Layer And Track (0.44mm,19.794mm)(8.04mm,19.794mm) o
Silk To Solder Mask Clearance Constraint: (0.085mm < 0.178mm) Between Pad P4-1(5.54mm,15.494mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P4-1(5.54mm,15.494mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.02mm < 0.178mm) Between Pad P4-1(5.54mm,15.494mm) on Multi-Layer And Region (3 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.072mm < 0.178mm) Between Pad P4-1(5.54mm,15.494mm) on Multi-Layer And Region (5 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.135mm < 0.178mm) Between Pad P5-1(5.715mm,29.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.13mm < 0.178mm) Between Pad P5-1(5.715mm,29.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.178mm) Between Pad P5-1(5.715mm,29.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P5-1(5.715mm,29.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.178mm) Between Pad P5-1(5.715mm,29.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.116mm < 0.178mm) Between Pad P5-2(5.715mm,26.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad P5-2(5.715mm,26.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad P5-2(5.715mm,26.289mm) on Multi-Layer And Region (0 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P5-2(5.715mm,26.289mm) on Multi-Layer And Region (2 hole(s)) Bottom Overlay [Bottom Overl
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-1(1.62mm,43.18mm) on Multi-Layer And Track (1.62mm,36.18mm)(1.62mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S1-1(7.62mm,43.18mm) on Multi-Layer And Track (2.72mm,43.18mm)(6.57mm,43.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-1(7.62mm,43.18mm) on Multi-Layer And Track (7.62mm,36.18mm)(7.62mm,42.18mm) on B

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(A
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-2(1.62mm,35.18mm) on Multi-Layer And Track (1.62mm,36.18mm)(1.62mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S1-2(1.62mm,35.18mm) on Multi-Layer And Track (2.62mm,35.18mm)(6.57mm,35.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S1-2(7.62mm,35.18mm) on Multi-Layer And Track (2.62mm,35.18mm)(6.57mm,35.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S1-2(7.62mm,35.18mm) on Multi-Layer And Track (7.62mm,36.18mm)(7.62mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-1(10.51mm,43.18mm) on Multi-Layer And Track (10.51mm,36.18mm)(10.51mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S2-1(16.51mm,43.18mm) on Multi-Layer And Track (11.61mm,43.18mm)(15.46mm,43.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-1(16.51mm,43.18mm) on Multi-Layer And Track (16.51mm,36.18mm)(16.51mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-2(10.51mm,35.18mm) on Multi-Layer And Track (10.51mm,36.18mm)(10.51mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S2-2(10.51mm,35.18mm) on Multi-Layer And Track (11.51mm,35.18mm)(15.46mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S2-2(16.51mm,35.18mm) on Multi-Layer And Track (11.51mm,35.18mm)(15.46mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S2-2(16.51mm,35.18mm) on Multi-Layer And Track (16.51mm,36.18mm)(16.51mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-1(19.4mm,43.18mm) on Multi-Layer And Track (19.4mm,36.18mm)(19.4mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S3-1(25.4mm,43.18mm) on Multi-Layer And Track (20.5mm,43.18mm)(24.35mm,43.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-1(25.4mm,43.18mm) on Multi-Layer And Track (25.4mm,36.18mm)(25.4mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-2(19.4mm,35.18mm) on Multi-Layer And Track (19.4mm,36.18mm)(19.4mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S3-2(19.4mm,35.18mm) on Multi-Layer And Track (20.4mm,35.18mm)(24.35mm,35.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S3-2(25.4mm,35.18mm) on Multi-Layer And Track (20.4mm,35.18mm)(24.35mm,35.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S3-2(25.4mm,35.18mm) on Multi-Layer And Track (25.4mm,36.18mm)(25.4mm,42.18mm) on B
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-1(28.29mm,43.18mm) on Multi-Layer And Track (28.29mm,36.18mm)(28.29mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S4-1(34.29mm,43.18mm) on Multi-Layer And Track (29.39mm,43.18mm)(33.24mm,43.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-1(34.29mm,43.18mm) on Multi-Layer And Track (34.29mm,36.18mm)(34.29mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-2(28.29mm,35.18mm) on Multi-Layer And Track (28.29mm,36.18mm)(28.29mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S4-2(28.29mm,35.18mm) on Multi-Layer And Track (29.29mm,35.18mm)(33.24mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S4-2(34.29mm,35.18mm) on Multi-Layer And Track (29.29mm,35.18mm)(33.24mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S4-2(34.29mm,35.18mm) on Multi-Layer And Track (34.29mm,36.18mm)(34.29mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S5-1(37.18mm,43.18mm) on Multi-Layer And Track (37.18mm,36.18mm)(37.18mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S5-1(43.18mm,43.18mm) on Multi-Layer And Track (38.28mm,43.18mm)(42.13mm,43.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S5-1(43.18mm,43.18mm) on Multi-Layer And Track (43.18mm,36.18mm)(43.18mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S5-2(37.18mm,35.18mm) on Multi-Layer And Track (37.18mm,36.18mm)(37.18mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.157mm < 0.178mm) Between Pad S5-2(37.18mm,35.18mm) on Multi-Layer And Track (38.18mm,35.18mm)(42.13mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad S5-2(43.18mm,35.18mm) on Multi-Layer And Track (38.18mm,35.18mm)(42.13mm,35.18m
Silk To Solder Mask Clearance Constraint: (0.168mm < 0.178mm) Between Pad S5-2(43.18mm,35.18mm) on Multi-Layer And Track (43.18mm,36.18mm)(43.18mm,42.18m
Silk To Solder Mask Clearance Constraint: (0.11mm < 0.178mm) Between Pad TP3-TP(73.025mm,19.05mm) on Multi-Layer And Text "TP3" (72.263mm,19.939mm) on Top O
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-1(26.248mm,25.146mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-10(30.648mm,20.066mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.73
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-11(30.648mm,21.336mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.73

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(A
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-12(30.648mm,22.606mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.73
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-13(30.648mm,23.876mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.73
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-14(30.648mm,25.146mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.73
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-2(26.248mm,23.876mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-3(26.248mm,22.606mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-4(26.248mm,21.336mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-5(26.248mm,20.066mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-6(26.248mm,18.796mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-7(26.248mm,17.526mm) on Top Layer And Track (26.848mm,16.936mm)(26.848mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-8(30.648mm,17.526mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U2-9(30.648mm,18.796mm) on Top Layer And Track (30.048mm,16.936mm)(30.048mm,25.736m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-1(26.248mm,11.176mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-10(30.648mm,6.096mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-11(30.648mm,7.366mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-12(30.648mm,8.636mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-13(30.648mm,9.906mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-14(30.648mm,11.176mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-2(26.248mm,9.906mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-3(26.248mm,8.636mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-4(26.248mm,7.366mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-5(26.248mm,6.096mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-6(26.248mm,4.826mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-7(26.248mm,3.556mm) on Top Layer And Track (26.848mm,2.966mm)(26.848mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-8(30.648mm,3.556mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U3-9(30.648mm,4.826mm) on Top Layer And Track (30.048mm,2.966mm)(30.048mm,11.766m

Silk to Silk (Clearance=0.254mm) (All),(Al
Silk To Silk Clearance Constraint: (0.154mm < 0.254mm) Between Region (1 hole(s)) Bottom Overlay And Text "S1" (8.128mm,33.274mm) on Bottom Overlay Silk Text I
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (0.14mm,15.394mm) on Top Overlay And Track (0.44mm,11.394mm)(0.44mm,19.794mm) on Top C
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "12V" (4.953mm,19.812mm) on Top Overlay And Track (0.44mm,19.794mm)(8.04mm,19.794mm) c
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "GND" (1.905mm,19.812mm) on Top Overlay And Track (0.44mm,19.794mm)(8.04mm,19.794mm) c
Silk To Silk Clearance Constraint: (0.23mm < 0.254mm) Between Text "P4" (6.477mm,10.16mm) on Top Overlay And Track (0.44mm,11.394mm)(8.04mm,11.394mm) on Top C
Silk To Silk Clearance Constraint: (0.089mm < 0.254mm) Between Text "P5" (1.27mm,21.463mm) on Top Overlay And Track (0.655mm,22.554mm)(8.34mm,22.554mm) c
Silk To Silk Clearance Constraint: (0.061mm < 0.254mm) Between Text "PPT" (6.35mm,33.147mm) on Top Overlay And Track (0.655mm,33.034mm)(8.34mm,33.034mm) c
Silk To Silk Clearance Constraint: (0.133mm < 0.254mm) Between Text "PPT" (6.35mm,33.147mm) on Top Overlay And Track (8.34mm,29.663mm)(8.34mm,33.034mm) c
Silk To Silk Clearance Constraint: (0.193mm < 0.254mm) Between Text "R13" (54.597mm,18.923mm) on Top Overlay And Text "R15" (54.61mm,17.78mm) on Top Overlay Silk
Silk To Silk Clearance Constraint: (0.196mm < 0.254mm) Between Text "R17" (48.514mm,23.368mm) on Top Overlay And Track (47.897mm,24.566mm)(68.297mm,24.566m
Silk To Silk Clearance Constraint: (0.216mm < 0.254mm) Between Text "REGEN" (31.75mm,27.051mm) on Bottom Overlay And Text "TP12" (31.623mm,26.035mm) on B

Board Clearance Constraint (Gap=0mm) (Al
Board Outline Clearance(Outline Edge): (0.175mm < 0.406mm) Between Board Edge And Pad M4-(41.656mm,3.175mm) on Top La
Board Outline Clearance(Outline Edge): (0.378mm < 0.406mm) Between Board Edge And Region (0 hole(s)) Bottom Over
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Text "1" (0.14mm,15.394mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.381mm < 0.406mm) Between Board Edge And Text "GND" (2.921mm,0.381mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.358mm < 0.406mm) Between Board Edge And Text "P3" (58.928mm,0.508mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.052mm < 0.406mm) Between Board Edge And Text "PPT" (6.35mm,33.147mm) on Bottom Ove
Board Outline Clearance(Outline Edge): (0.358mm < 0.406mm) Between Board Edge And Text "STEERING REV 5" (61.976mm,0.508mm) on Top Ove
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Text "STEERI

STALK" (72.771mm,24.384mm) on Top Overla

Board Clearance Constraint (Gap=0mm) (Al
Board Outline Clearance(Outline Edge): (0.313mm < 0.406mm) Between Board Edge And Track (0.44mm,11.394mm)(0.44mm,19.794mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.313mm < 0.406mm) Between Board Edge And Track (0.44mm,11.394mm)(8.04mm,11.394mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.313mm < 0.406mm) Between Board Edge And Track (0.44mm,19.794mm)(8.04mm,19.794mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.381mm < 0.406mm) Between Board Edge And Track (44.144mm,0.508mm)(44.144mm,30.508mm) on Top Ove
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (47.331mm,0.028mm)(57.881mm,0.028mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.333mm < 0.406mm) Between Board Edge And Track (47.897mm,24.566mm)(47.897mm,29.766mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.333mm < 0.406mm) Between Board Edge And Track (47.897mm,29.766mm)(68.297mm,29.766mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.333mm < 0.406mm) Between Board Edge And Track (68.297mm,24.566mm)(68.297mm,29.766mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.381mm < 0.406mm) Between Board Edge And Track (9.144mm,0.508mm)(44.144mm,0.508mm) on Top Ove
Board Outline Clearance(Outline Edge): (0.381mm < 0.406mm) Between Board Edge And Track (9.144mm,0.508mm)(9.144mm,30.508mm) on Top Ove