P1

Thermistor 1+	7		1	Voltage Tap 2
Thermistor 2+	8		2	Balance Tap 1
Thermistor 3+	9		3	Voltage Tap 1
Thermistor 4+	10		4	Balance Tap 3
Thermistor 5	11		5	Voltage Tap 3
	12		6	Balance Tap 2

CONN 12POS HEADER R/A MICROFIT 3MM
WM1818-ND

RT1
10K NTC
490-8601-ND

GND   GND

P2

Voltage Tap 2 — R3 1 Ohm 1/4W 5% — F3 500mA 250V JFC2410-0500FS	7		14	Thermistor 1+
Balance Tap 1 — R2 2 Ohm 1/4W 1% C269587 — F2 500mA 250V JFC2410-0500FS	6		13	Thermistor 2+
Voltage Tap 1 — R1 2 Ohm 1/4W 1% C269587 — F1 500mA 250V	5		12	Thermistor 3+
RES 2 OHM 1% 1/4W 1206 JFC2410-0500FS	4		11	Thermistor 4+
Balance Tap 3 — R6 2 Ohm 1/4W 1% RES 2 OHM 1% 1/4W 1206 — F6 500mA 250V JFC2410-0500FS	3		10	
Voltage Tap 3 — R5 1 Ohm 1/4W 5% 2 Ohm 1/4W 1% C269587 — F5 RES 2 OHM 1% 1/4W 1206	2		9	
Balance Tap 2 — R4 — F4 JFC2410-0500FS 500mA 250V	1		8	

CONN 14POS HEADER R/A MICROFIT 3MM
WM4723-ND

GND

GND

Bill of Materials

Project:	XIV_BatteryModuleConnectorBoard.PrjPcb
Revision:	2.0
Project Lead:	Aashmika Mali
Generated On:	2020-03-30 12:20 AM
Production Quantity:	1
Currency:	USD
Total Parts Count:	15

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
FUSE 500MA LCSC	F1, F2, F3, F4, F5, F6	Shenzen JDT Fuse	JFC2410-0500FS	LCSC	C136360		6	
CONN 12POS HEADER R/A MICROFIT 3MM	P1	Molex	0430451200	Digi-Key	WM1818-ND		1	
CONN 14POS HEADER R/A MICROFIT 3MM	P2	Molex	0430451400	Digi-Key	WM4723-ND		1	
RES 2 OHM 1% 1/4W 1206	R1, R2, R5, R6	TyoHM	RMC120621%N	LCSC	C269587		4	
RES 1 OHM 5% 1/4W 1206	R3, R4	TyoHM	RMC120615%N	LCSC	C325901		2	
NTC THERMISTOR 10K 1% BEAD	RT1			Digi-Key	490-8601-ND		1	
						Total:		$ -
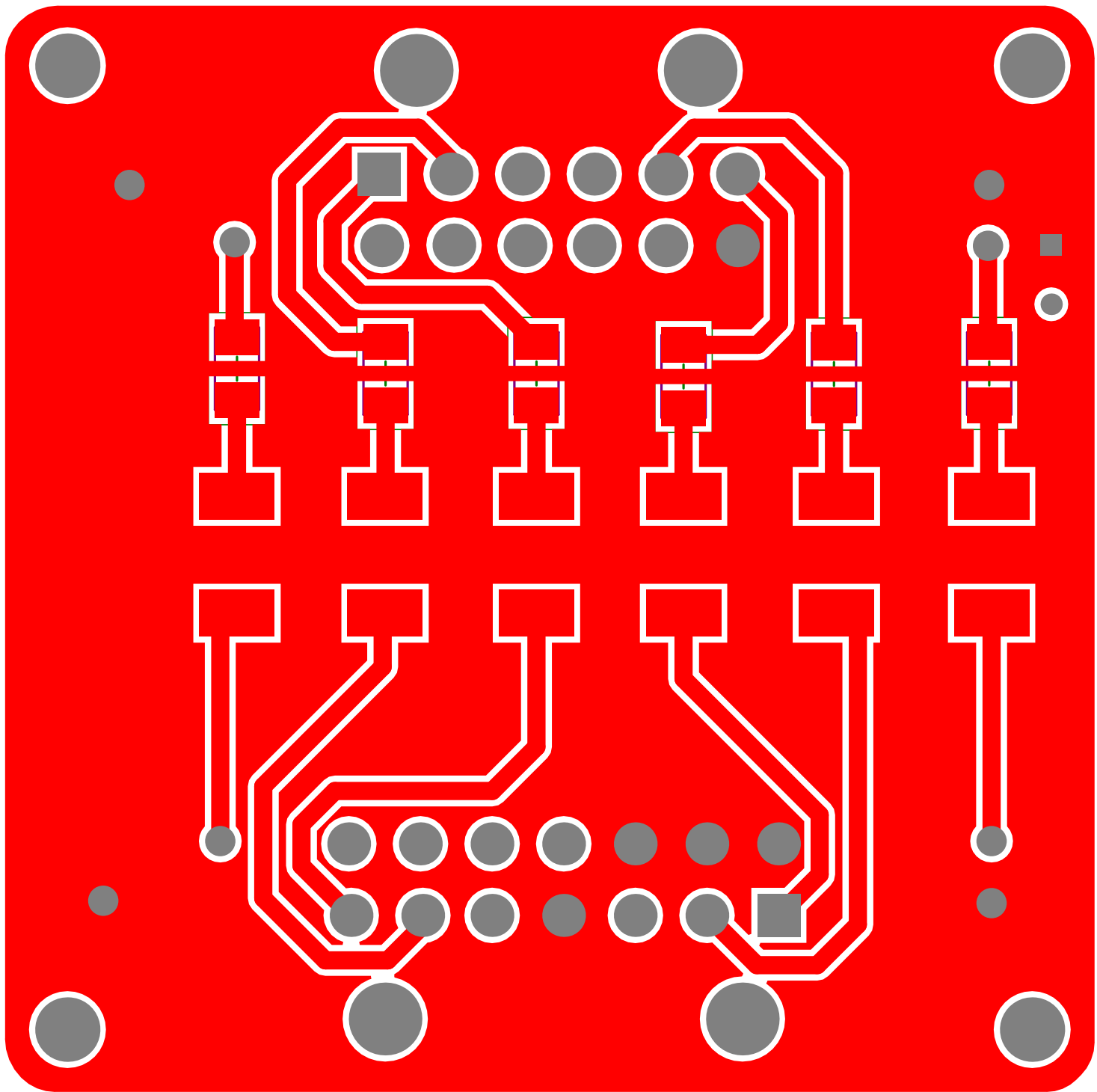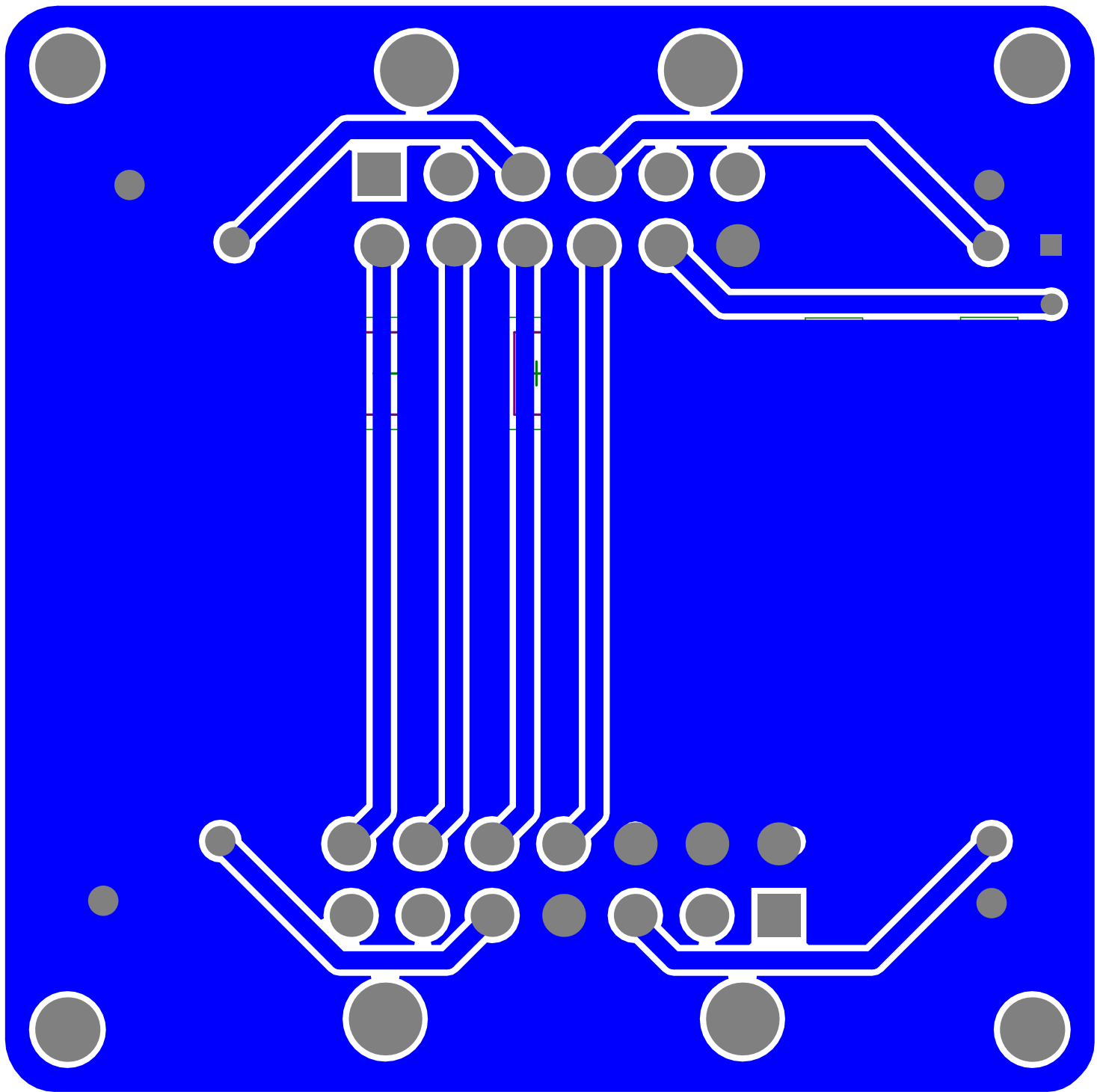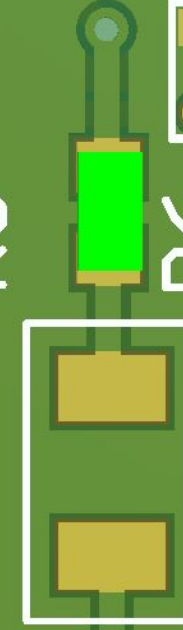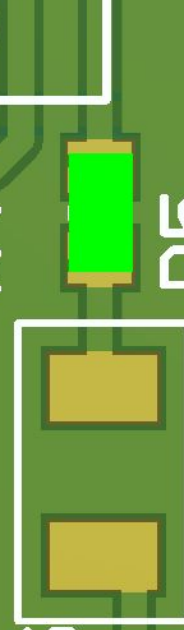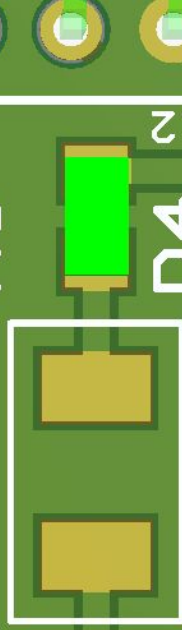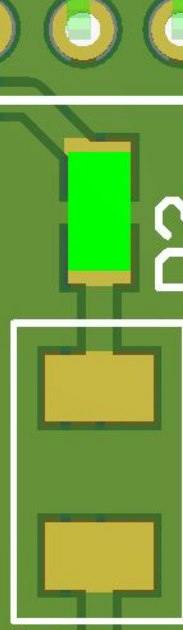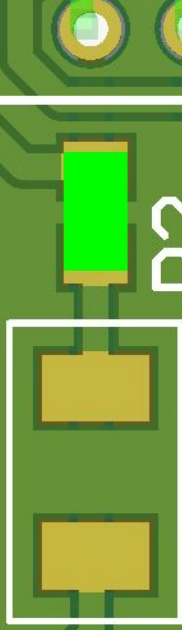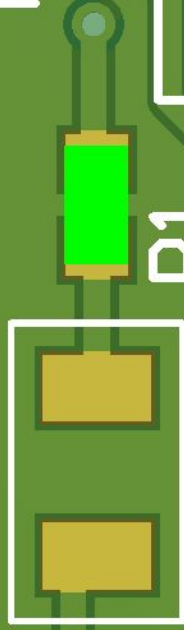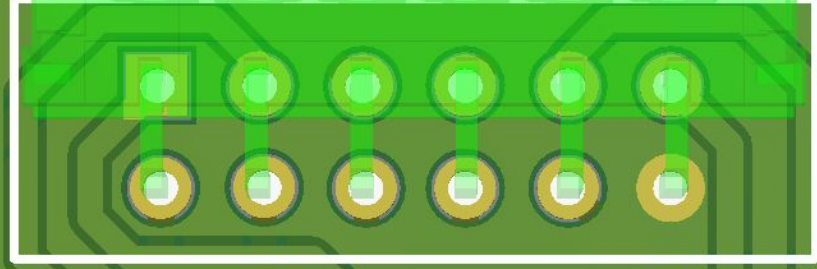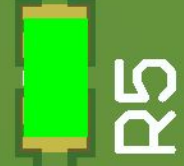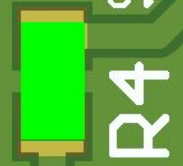
Design Rules Verification Report

Filename : C:\Users\ricky\Downloads\Projects\Midnight Sun\Midnight Sun Hardware\Wint
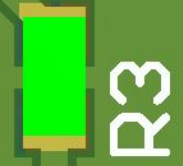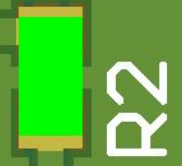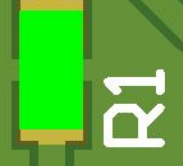
Warnings

Total	0

Rule Violations

Clearance Constraint (Gap=10mil) (All),(All)	15
Short-Circuit Constraint (Allowed=No) (All),(All)	15
Un-Routed Net Constraint ((All))	8
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=30mil) (Preferred=20mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	4
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	0
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	9
Silk to Silk (Clearance=10mil) (All),(All)	9
Net Antennae (Tolerance=0mil) (All)	12
Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)	15
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	87

Clearance Constraint (Gap=10mil) (All),(All)

Clearance Constraint: (Collision < 10mil) Between Pad F4-2(1133.858mil,998.032mil) on Top Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad F5-1(1385.827mil,998.032mil) on Top Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P1-12(1222.968mil,1411.677mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P1-5(1104.858mil,1529.787mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-1(1291.008mil,306.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-2(1172.559mil,306.496mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-8(1290.669mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad P2-8(1290.669mil,424.606mil) on Multi-Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad R4-1(1133.858mil,1143.701mil) on Top Layer And Track

Clearance Constraint: (Collision < 10mil) Between Pad R5-2(1381.89mil,1147.638mil) on Top Layer And Track

Clearance Constraint: (Collision < 10mil) Between Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil) on Top Layer And Track

Short-Circuit Constraint (Allowed=No) (All),(All)

Short-Circuit Constraint: Between Pad F4-2(1133.858mil,998.032mil) on Top Layer And Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil)

Short-Circuit Constraint: Between Pad F5-1(1385.827mil,998.032mil) on Top Layer And Track (1381.89mil,1001.968mil)(1381.89mil,1144.685mil) on

Short-Circuit Constraint: Between Pad P1-12(1222.968mil,1411.677mil) on Multi-Layer And Track

Short-Circuit Constraint: Between Pad P1-5(1104.858mil,1529.787mil) on Multi-Layer And Track

Short-Circuit Constraint: Between Pad P2-1(1291.008mil,306.606mil) on Multi-Layer And Track (1291.008mil,306.606mil)(1307.236mil,322.835mil)

Short-Circuit Constraint: Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track (1054.449mil,424.606mil)(1054.449mil,428.464mil)

Short-Circuit Constraint: Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track (1054.449mil,424.606mil)(1054.449mil,432.401mil)

Short-Circuit Constraint: Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track (1054.449mil,428.504mil)(1054.449mil,436.339mil)

Short-Circuit Constraint: Between Pad P2-10(1054.449mil,424.606mil) on Multi-Layer And Track (1054.449mil,432.401mil)(1058.386mil,432.401mil)

Short-Circuit Constraint: Between Pad P2-2(1172.559mil,306.496mil) on Multi-Layer And Track (1172.559mil,299.882mil)(1172.559mil,306.496mil)

Short-Circuit Constraint: Between Pad P2-8(1290.669mil,424.606mil) on Multi-Layer And Track (1290.669mil,424.606mil)(1290.669mil,428.465mil)

Short-Circuit Constraint: Between Pad P2-8(1290.669mil,424.606mil) on Multi-Layer And Track (1290.669mil,428.465mil)(1310.354mil,428.465mil)

Short-Circuit Constraint: Between Pad R4-1(1133.858mil,1143.701mil) on Top Layer And Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil)

Short-Circuit Constraint: Between Pad R5-2(1381.89mil,1147.638mil) on Top Layer And Track (1381.89mil,1001.968mil)(1381.89mil,1144.685mil)

Short-Circuit Constraint: Between Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil) on Top Layer And Track

Un-Routed Net Constraint ((All))

Un-Routed Net Constraint: Net NetF4_2 Between Pad F4-2(1133.858mil,998.032mil) on Top Layer And Pad R4-1(1133.858mil,1143.701mil) on Top

Un-Routed Net Constraint: Net NetF5_1 Between Pad R5-2(1381.89mil,1147.638mil) on Top Layer And Pad F5-1(1385.827mil,998.032mil) on Top

Un-Routed Net Constraint: Net Thermistor 5 Between Pad P1-11(1104.858mil,1411.677mil) on Multi-Layer And Track

Un-Routed Net Constraint: Net Balance Tap 2 Between Track (1104.858mil,1529.787mil)(1112.465mil,1529.787mil) on Top Layer And Pad

Un-Routed Net Constraint: Net Thermistor 4+ Between Pad P2-11(936.339mil,424.606mil) on Multi-Layer And Track

Un-Routed Net Constraint: Net Thermistor 1+ Between Pad P2-14(582.008mil,424.606mil) on Multi-Layer And Track

Un-Routed Net Constraint: Net NetF5_1 Between Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil) on Top Layer And Pad

Un-Routed Net Constraint: Net NetF4_2 Between Track (1133.858mil,998.032mil)(1157.441mil,1021.614mil) on Top Layer And Track

Hole Size Constraint (Min=1mil) (Max=100mil) (All)

Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil

Hole Size Constraint: (106.299mil > 100mil) Pad Free-(118.11mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mil

Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil

Hole Size Constraint: (106.299mil > 100mil) Pad Free-(1708.661mil,1708.661mil) on Multi-Layer Actual Hole Size = 106.299mil

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(1161.417mil,1700.787mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad P1-0(693.417mil,1700.787mil) on Multi-Layer And Text "1"

Silk To Solder Mask Clearance Constraint: (7.531mil < 10mil) Between Pad P1-0(693.417mil,1700.787mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT1-1(1740.158mil,1413.386mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (8.833mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track

Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT1-2(1740.158mil,1314.961mil) on Multi-Layer And Track

Silk to Silk (Clearance=10mil) (All),(All)

Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "1" (1314.291mil,208.071mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (637.354mil,1676.457mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "12" (1247.59mil,1314.252mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "14" (585.945mil,570.276mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.432mil < 10mil) Between Text "F3" (846.457mil,614.173mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.04mil < 10mil) Between Text "F3" (846.457mil,614.173mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (9.009mil < 10mil) Between Text "F4" (1094.488mil,612.205mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (7.294mil < 10mil) Between Text "F5" (1358.268mil,618.11mil) on Top Overlay And Track

Silk To Silk Clearance Constraint: (3.103mil < 10mil) Between Text "F5" (1358.268mil,618.11mil) on Top Overlay And Track

Net Antennae (Tolerance=0mil) (All)

Net Antennae: Track (1104.858mil,1529.787mil)(1112.465mil,1529.787mil) on Top Layer

Net Antennae: Track (1104.858mil,1529.787mil)(1112.465mil,1529.787mil) on Top Layer

Net Antennae: Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil) on Top Layer

Net Antennae: Track (1133.858mil,998.032mil)(1133.858mil,1144.685mil) on Top Layer

Net Antennae: Track (1172.559mil,299.882mil)(1172.559mil,306.496mil) on Bottom Layer

Net Antennae: Track (1172.559mil,299.882mil)(1172.559mil,306.496mil) on Bottom Layer

Net Antennae: Track (1222.968mil,1411.677mil)(1224.434mil,1411.677mil) on Bottom Layer

Net Antennae: Track (1222.968mil,1411.677mil)(1224.434mil,1411.677mil) on Bottom Layer

Net Antennae: Track (1291.008mil,306.606mil)(1307.236mil,322.835mil) on Bottom Layer

Net Antennae: Track (1291.008mil,306.606mil)(1307.236mil,322.835mil) on Bottom Layer

Net Antennae: Track (1381.89mil,1001.968mil)(1381.89mil,1144.685mil) on Top Layer

Net Antennae: Track (1381.89mil,1001.968mil)(1381.89mil,1144.685mil) on Top Layer

Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil) (InComponentClas
Room Definition: Between Component P1-CONN 12POS HEADER R/A MICROFIT 3MM (875.417mil,2026.787mil) on Top Layer And Room
Room Definition: Between Component P2-CONN 14POS HEADER R/A MICROFIT 3MM (937.008mil,149.606mil) on Top Layer And Room
Room Definition: Between Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)
Room Definition: Between Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)
Room Definition: Between Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)
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Room Definition: Between Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)
Room Definition: Between Room MSXIV_BatteryModuleConnectorBoard (Bounding Region = (0mil, 0mil, 2000mil, 1000mil)