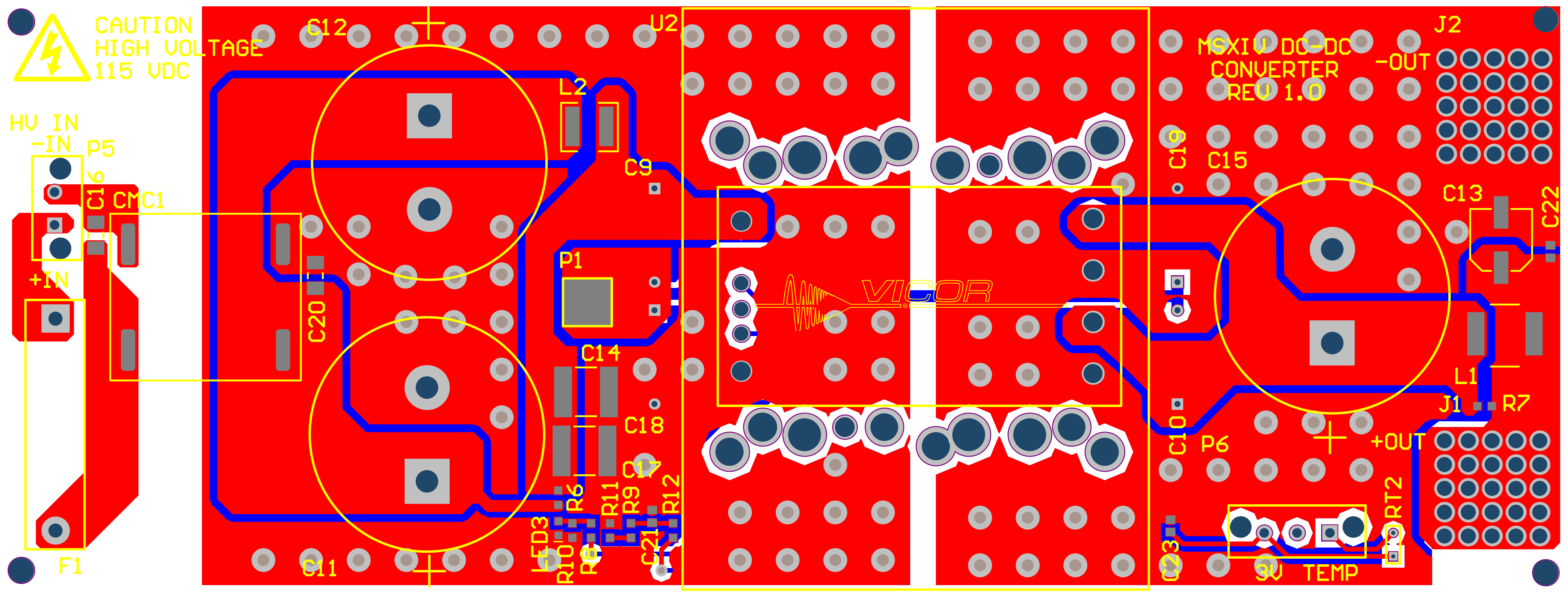
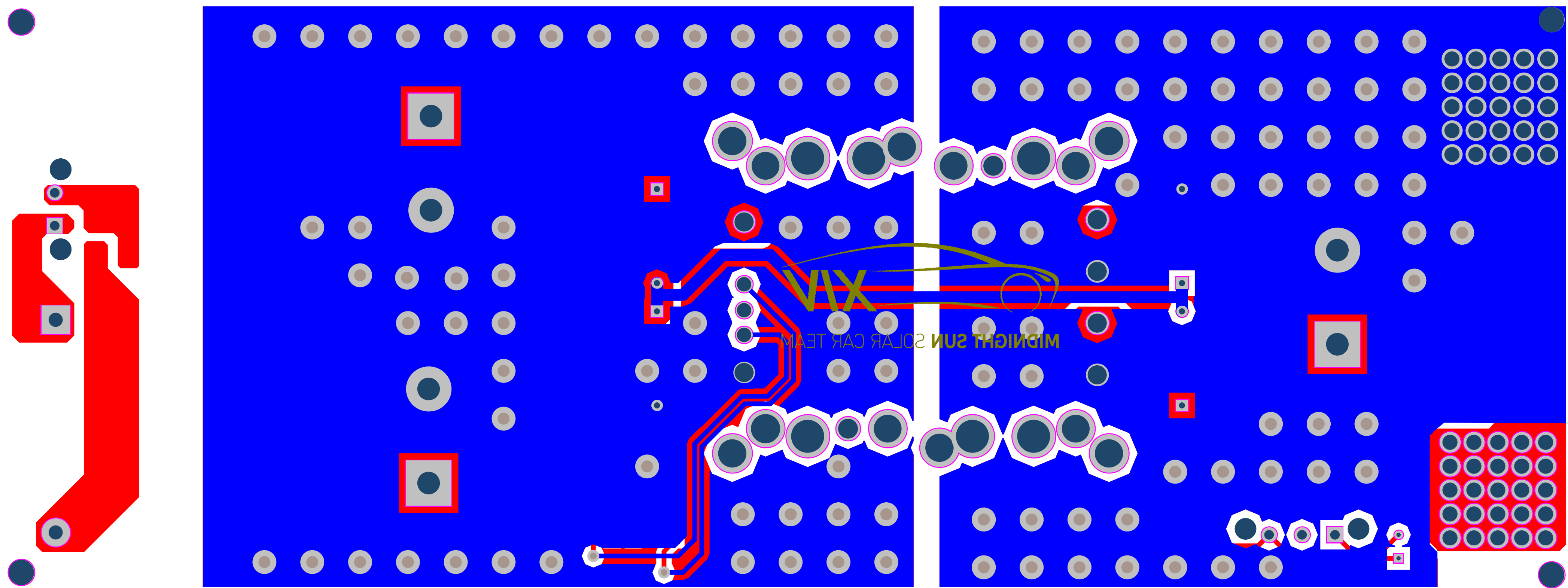


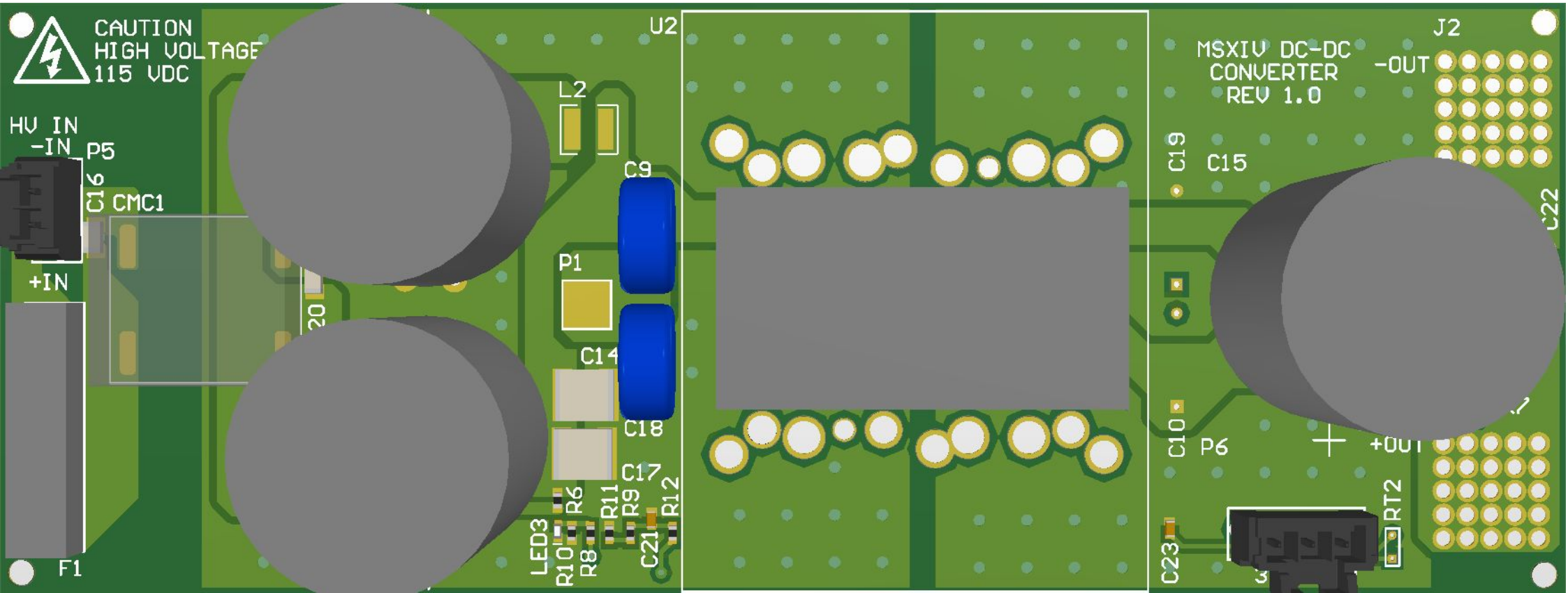
MIDNIGHT SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
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Commer	Descripti	Designat	Footprint	LibRef	Quantity	Manufact	Manufact	Supplier	Supplier	Supplier	Supplier	Supplier	Supplier	Supplier
CAP CER	4700pF ±	C9, C18	CAP 470	CAP CER	2			Digi-Key				399-9517-1-ND		
CAP ALU	CAP RAD	C11, C12	CAP ALU	CAP ALU	2	Cornell D	SLPX102	Digi-Key				338-1557-ND		
EEE-1HA	4.7µF 50V	C13	CAP ALU	CAP ALU	1	Panasoni	EEE-1HA	Digi-Key				PCE4304CT-ND		
CAP CER	1µF ±10%	C14, C17	CAP, 222	CAP CER	2		GRM55D	Digi-Key				490-14683-1-ND		
CAP ALU	15000µF	C15	CAP ALU	CAP ALU	1			Digi-Key				338-1470-ND		
CAP CER	CAP CER	C16, C20	CAP, 120	CAP CER	2	Manufact	8853422	Digi-Key				732-12081-1-ND		
CAP CER	0.10µF ±	C21, C23	CAP, 060	CAP CER	2	AVX Corp	06035C1	Digi-Key				478-5052-1-ND		
CAP CER	10µF ±2%	C22	CAP, 060	CAP CER	1	Murata E	GRM188	Digi-Key				490-7202-1-ND		
CM Chok	2 Line Co	CMC1	LCCI 50	(COMMON	1	Pulse Ele	P0353NL	Digi-Key				553-1764-1-ND		
FUSE 420	8A 420V	F1	FUSE 420	FUSE 420	1			Digi-Key				F6659-ND		
TERM PV	25 Pin Str	J1, J2	TERM PV	TERM PV	2	Wurth El	7460719	Digi-Key				732-3219-ND		
IND 820	820nH S	L1	IND 820	IND 820	1			Digi-Key				XC2399CT-ND		
IND 1UH	1µH Sem	L2	IND 1UH	IND 1uH	1	Bourns I	SRN5040	Digi-Key				SRN5040TA-1ROMCT-ND		
LED GRE	Green 57	LED3	LED_060	LED GRE	1			Digi-Key				732-4980-1-ND		
5mm PA	5x5mm	P1	5mm PA	5mm PA	1									
CONN 2P	2 Positio	P5	CONN, 2	CONN 2P	1	Molex, LL	1722861	Digi-Key				WM11673-ND		
CONN 3P	3 Positio	P6	CONN, 3	CONN 3P	1	Molex, LL	1722871	Digi-Key				WM11702-ND		
RES 1 OH	RES SMD	R6, R7	RES, 060	RES 1 OH	2	Rohm Se	KTR03EZ	Digi-Key				RHM1.0AZCT-ND		
RES 330	330 Ohm	R8	RES, 060	RES 330	1			Digi-Key				A129682TR-ND		
RES 10K	RES SMD	R9	RES, 060	RES 10K	1	Yageo	RC0603F	Digi-Key				311-10.0KHRCT-ND		
RES 54.9	54.9k OH	R10	RES, 060	RES 54.9	1			Digi-Key				P54.9KHCT-ND		
RES 15.6	5.6 kOhm	R11	RES, 060	RES 5.6K	1	Yageo	RC0603J	Digi-Key				311-5.6KGRCT-ND		
RES 0.0	RES SMD	R12	RES, 060	RES 0.0	1	Vishay D	CRCW06	Digi-Key				541-0.0SBCT-ND		
10K NTC	NTC Ther	RT2	NTC THE	NTC THE	1			Digi-Key				490-8601-ND		







Electrical Rules Check Report

Class	Document	Message
Warning	MSXIV_DC-DC_Converter.SchDoc	Off grid NetParameter at 9444.489mil,5600mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXII_

Warnings 0
Rule Violations 194

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	2
Clearance Constraint (Gap=5mil) (IsStitchingVia and InNet('HV_GND')),(IsVia and (Not IsStitchingVia)) Or IsPad	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	24
Hole To Hole Clearance (Gap=10mil) (All),(All)	55
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	89
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	22
Silk to Silk (Clearance=10mil) (All),(All)	2
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1968.504mil) (Preferred=500mil) (All)	0
Total	194

Clearance Constraint (Gap=10mil) (All),(All)	
Clearance Constraint: (24.922mil < 30mil) Between Pad P5-(253.15mil,1440.945mil) on Multi-Layer And Region (0 hole(s)) Top Layer	
Clearance Constraint: (20.315mil < 30mil) Between Pad P5-(253.15mil,1775.591mil) on Multi-Layer And Region (0 hole(s)) Top Layer	

Hole Size Constraint (Min=1mil) (Max=100mil) (All)	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(6486.221mil,2401.575mil) on Multi-Layer Actual Hole Size = 106.299mi	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(6486.221mil,78.74mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(88.583mil,2391.732mil) on Multi-Layer Actual Hole Size = 106.299mi	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(88.583mil,88.583mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(3061.024mil,1893.701mil) on Multi-Layer Actual Hole Size = 118.11mi	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(3061.024mil,586.614mil) on Multi-Layer Actual Hole Size = 118.11mil	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(3200mil,1790.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(3200mil,690.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (122.047mil > 100mil) Pad U2-(3200mil,690.158mil) on Multi-Layer Actual Hole Size = 122.047mil	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(3375.984mil,1822.047mil) on Multi-Layer Actual Hole Size = 137.795mil	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(3375.984mil,1822.047mil) on Multi-Layer Actual Hole Size = 137.795mil	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(3375.984mil,658.268mil) on Multi-Layer Actual Hole Size = 137.795mi	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(3631.89mil,1822.047mil) on Multi-Layer Actual Hole Size = 137.795mi	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(3710.63mil,690.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(3769.685mil,1870.079mil) on Multi-Layer Actual Hole Size = 118.11mi	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(3927.165mil,610.236mil) on Multi-Layer Actual Hole Size = 118.11mi	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(3986.22mil,1790.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(4064.961mil,658.268mil) on Multi-Layer Actual Hole Size = 137.795mi	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(4320.866mil,1822.047mil) on Multi-Layer Actual Hole Size = 137.795mil	
Hole Size Constraint: (137.795mil > 100mil) Pad U2-(4320.866mil,658.268mil) on Multi-Layer Actual Hole Size = 137.795mi	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(4496.85mil,1790.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (116.142mil > 100mil) Pad U2-(4496.85mil,690.158mil) on Multi-Layer Actual Hole Size = 116.142mi	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(4635.827mil,1893.701mil) on Multi-Layer Actual Hole Size = 118.11mi	
Hole Size Constraint: (118.11mil > 100mil) Pad U2-(4635.827mil,586.614mil) on Multi-Layer Actual Hole Size = 118.11mi	

Hole To Hole Clearance (Gap=10mil) (All),(All)

[illegible]

Hole To Hole Clearance (Gap=10mil) (All), (All)
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Via (5912.5mil,2110mil) from Top Layer to Bottom Layer And Via (5912.5mil,2110mil)
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Via (5912.5mil,2310mil) from Top Layer to Bottom Layer And Via (5912.5mil,2310mil)
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Via (6112.5mil,1510mil) from Top Layer to Bottom Layer And Via (6112.5mil,1510mil)

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)

[illegible]

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C13-1(6299.213mil,1360.236mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C13-1(6299.213mil,1360.236mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C13-2(6299.213mil,1592.52mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C13-2(6299.213mil,1592.52mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.604mil < 10mil) Between Pad C21-1(2736.22mil,288.386mil) on Top Layer And Text "C21"
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(2342.52mil,236.22mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad P1-1(2464.567mil,1212.598mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad P1-1(2464.567mil,1212.598mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad P1-1(2464.567mil,1212.598mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad P1-1(2464.567mil,1212.598mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT2-1(5846.457mil,147.638mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT2-1(5846.457mil,147.638mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (6.811mil < 10mil) Between Pad RT2-1(5846.457mil,147.638mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT2-2(5846.457mil,246.063mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.359mil < 10mil) Between Pad RT2-2(5846.457mil,246.063mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.941mil < 10mil) Between Pad RT2-2(5846.457mil,246.063mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.655mil < 10mil) Between Pad U2-(3200mil,1790.158mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.646mil < 10mil) Between Pad U2-(3200mil,690.158mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.646mil < 10mil) Between Pad U2-(3710.63mil,690.158mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.655mil < 10mil) Between Pad U2-(3986.22mil,1790.158mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.655mil < 10mil) Between Pad U2-(4496.85mil,1790.158mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.646mil < 10mil) Between Pad U2-(4496.85mil,690.158mil) on Multi-Layer And Track

Silk to Silk (Clearance=10mil) (All),(All)

Silk To Silk Clearance Constraint: (6.385mil < 10mil) Between Arc (1791.339mil,659.449mil) on Top Overlay And Text "+" (1899.606mil,9.842mil) on Top
Silk To Silk Clearance Constraint: (9.685mil < 10mil) Between Text "R12" (2844.488mil,334.646mil) on Top Overlay And Track