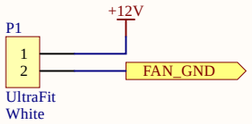
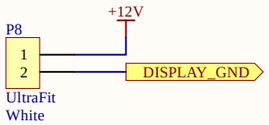
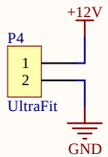
Fan Power



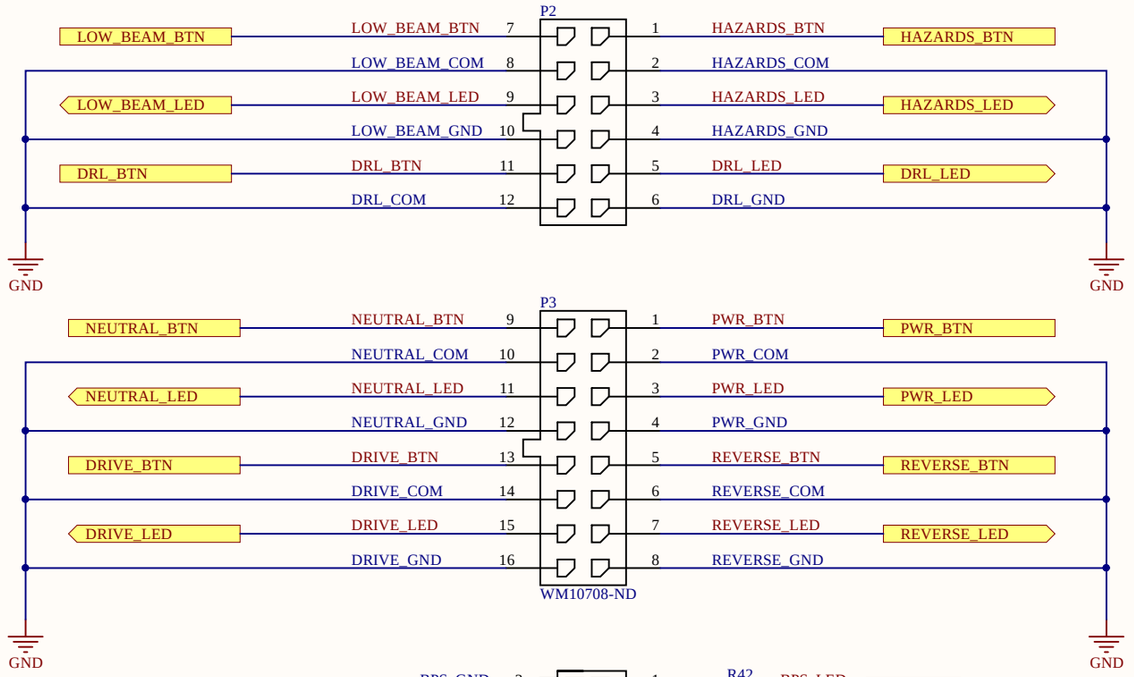
Display Power

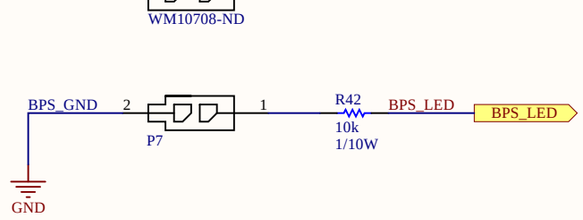


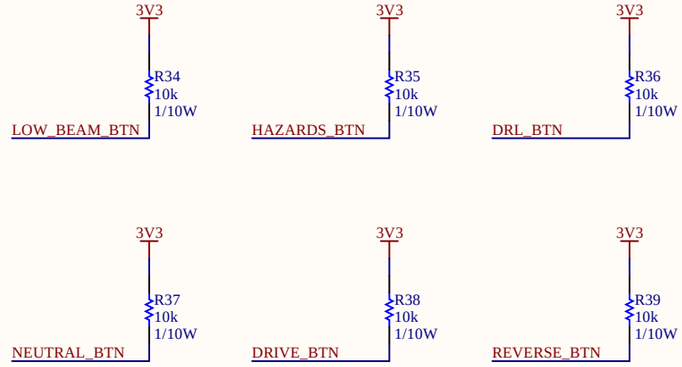
Carrier Board Power

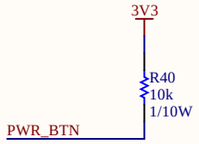


Buttons & LEDs



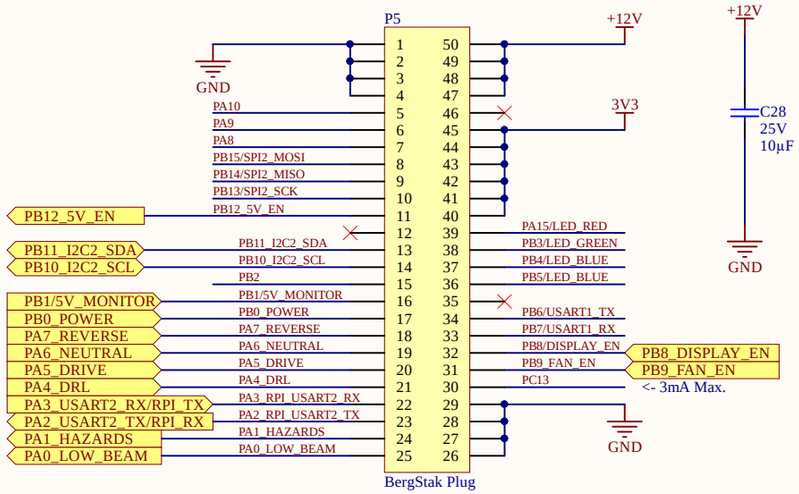




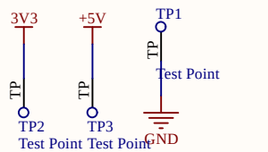


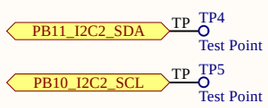
Standoffs

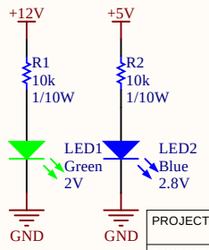
CB Conn



Test Points







PROJECT	Center Console.PrjPcb		
DOCUMENT	Center Console - Connectors		
PART NUMBER	MS-ELE0007	VARIANT	01 - Standard
DRAWN BY	Mena Labib	REVISION	3.0
LAST MODIFIED	2019-03-18	SHEET	1 OF 4

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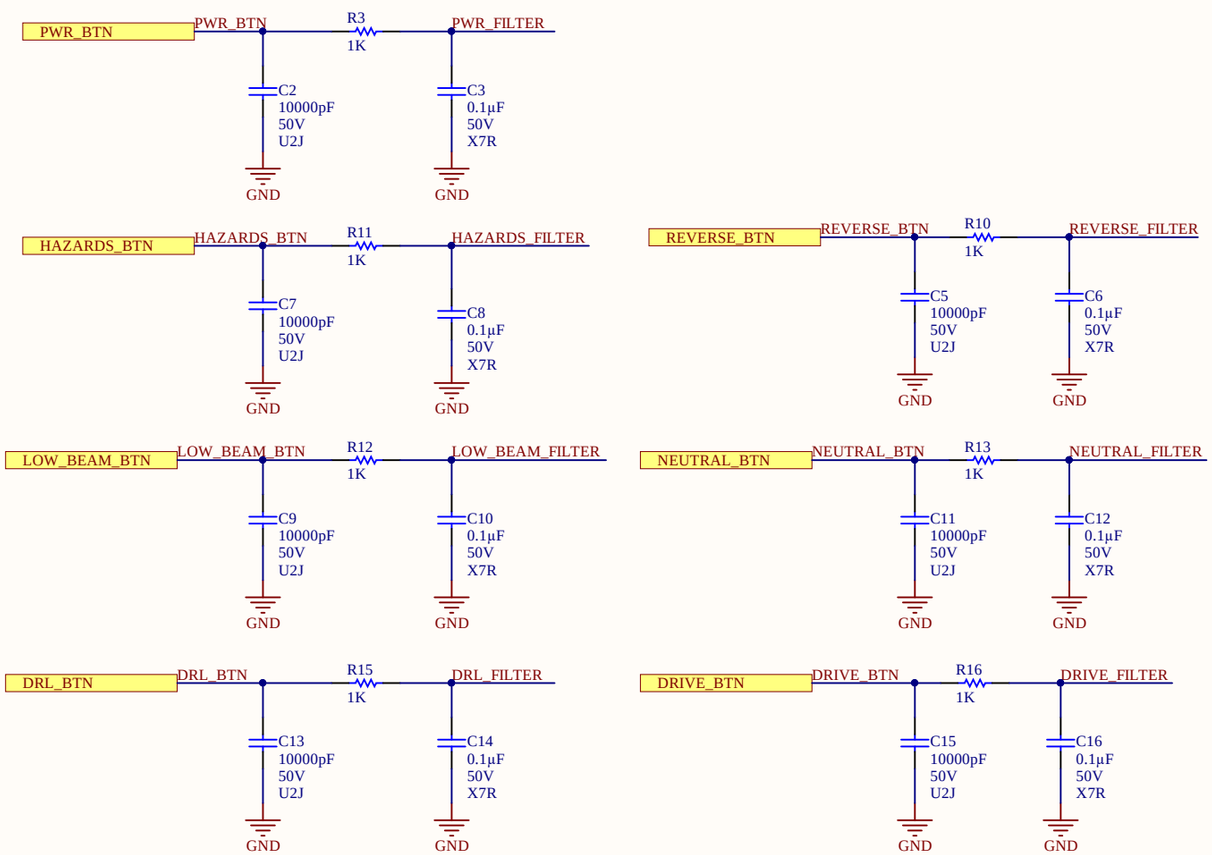
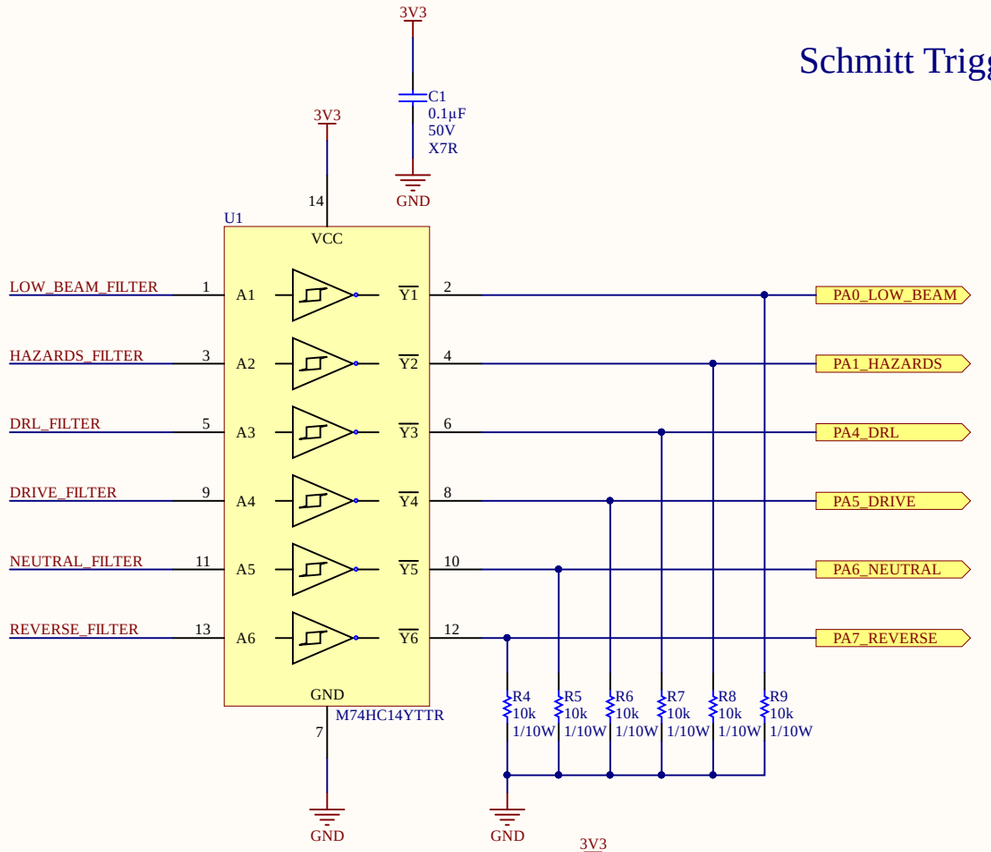
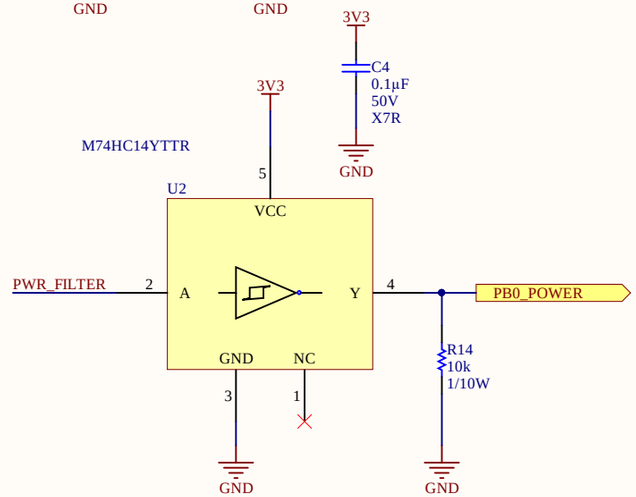
RC-Filters



Schmitt Triggers





PROJECT	Center Console.PrjPcb		
DOCUMENT	Center Console - Buttons Interface		
PART NUMBER	MS-ELE0007	VARIANT	01 - Standard
DRAWN BY	Mena Labib	REVISION	3.0
LAST MODIFIED	2019-03-18	SHEET	2 OF 4

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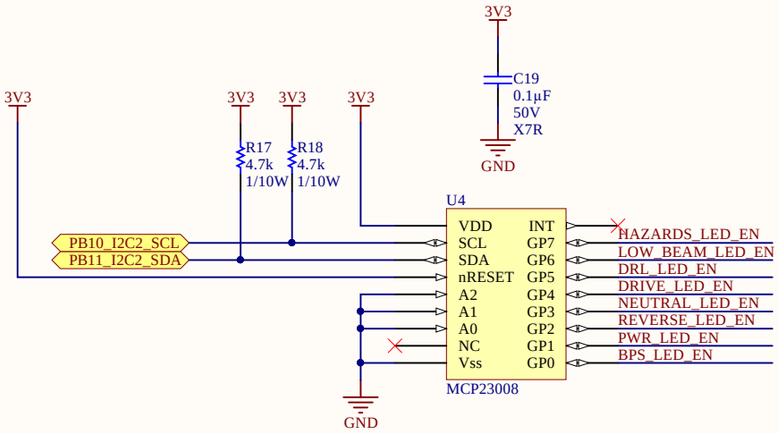
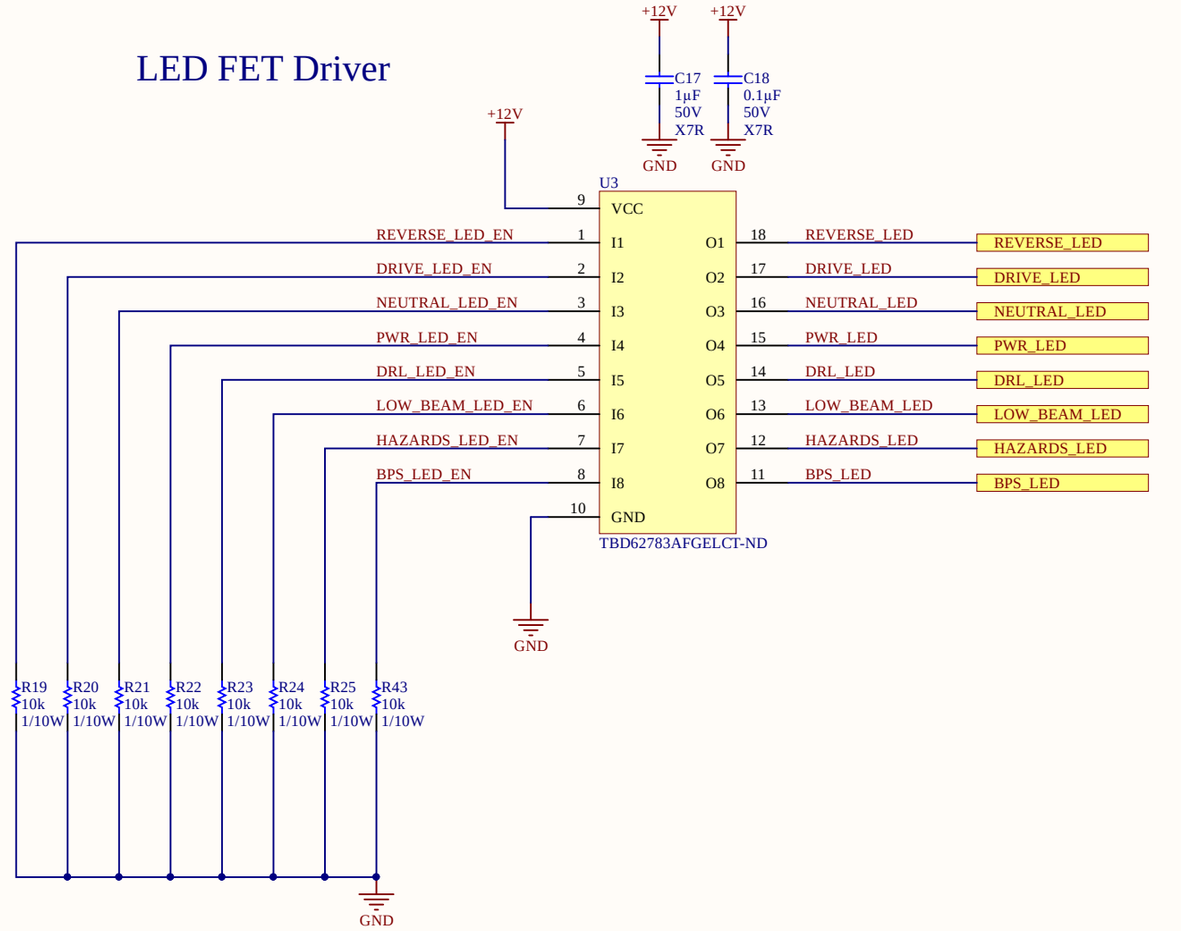
LED IO-Expander



LED FET Driver



PROJECT	Center Console.PrjPcb		MIDNIGHT SUN
DOCUMENT	Center Console - LED Interface		
PART NUMBER	MS-ELE0007	VARIANT	01 - Standard
DRAWN BY	Mena Labib	REVISION	3.0
LAST MODIFIED	2019-03-18	SHEET	3 OF 4

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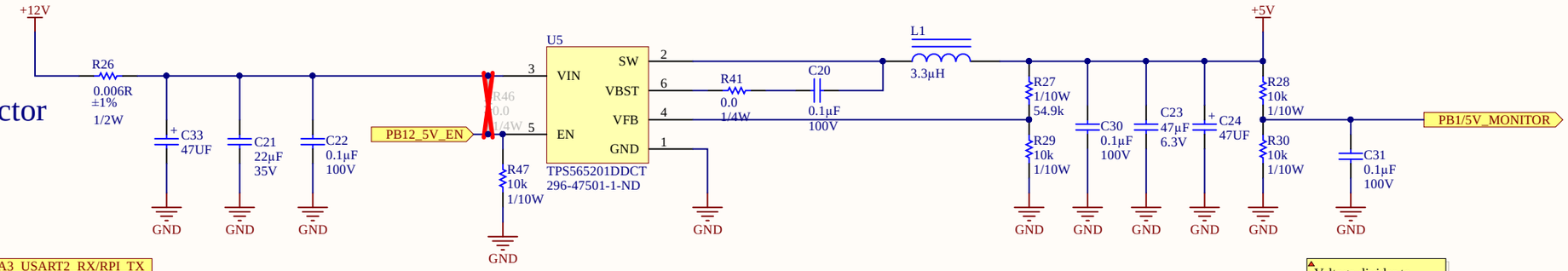
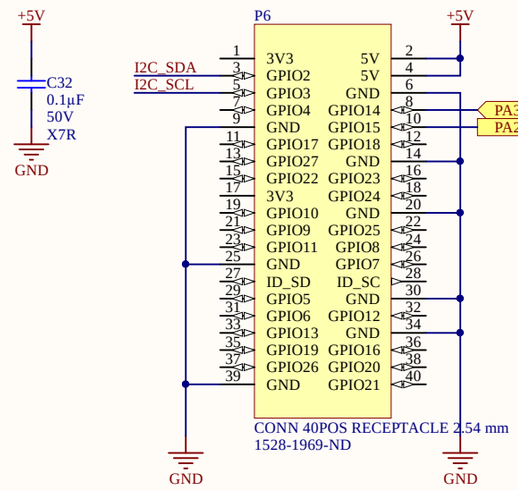
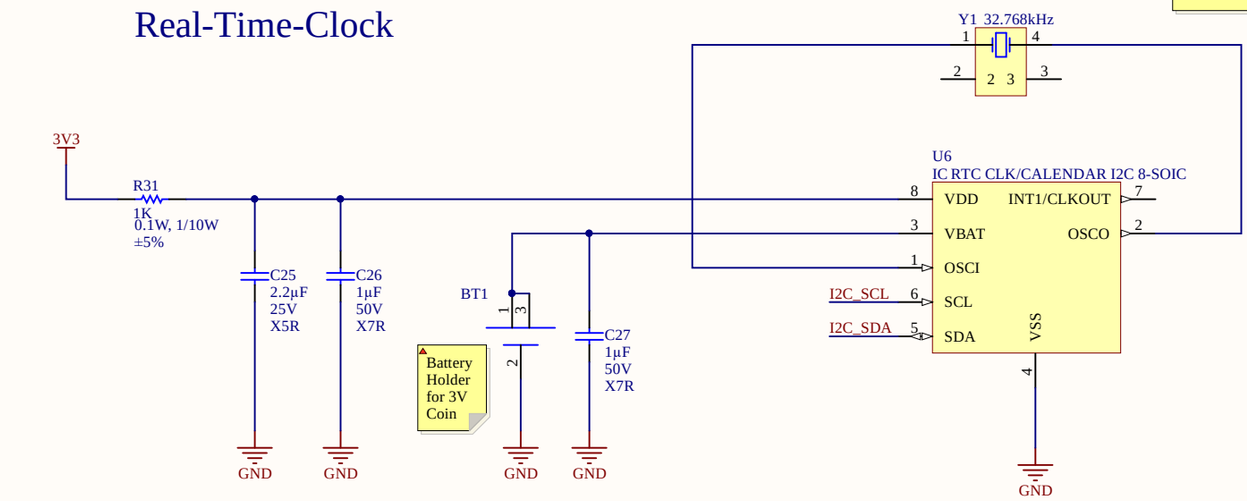
Regulator



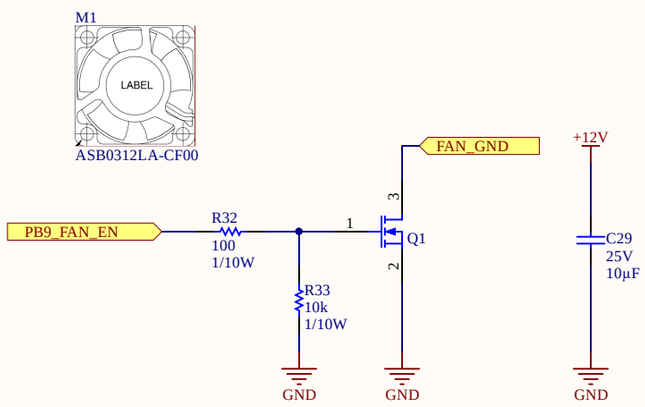
Rasberry Pi Connector

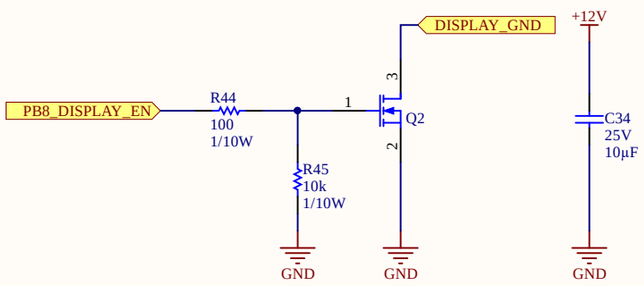


Real-Time-Clock



30mm Fan





PROJECT	Center Console.PrjPcb		
DOCUMENT	Center Console - Raspberry Pi Interface		
PART NUMBER	MS-ELE0007	VARIANT	01 - Standard
DRAWN BY	Mena Labib	REVISION	3.0
LAST MODIFIED	2019-03-18	SHEET	4 OF 4

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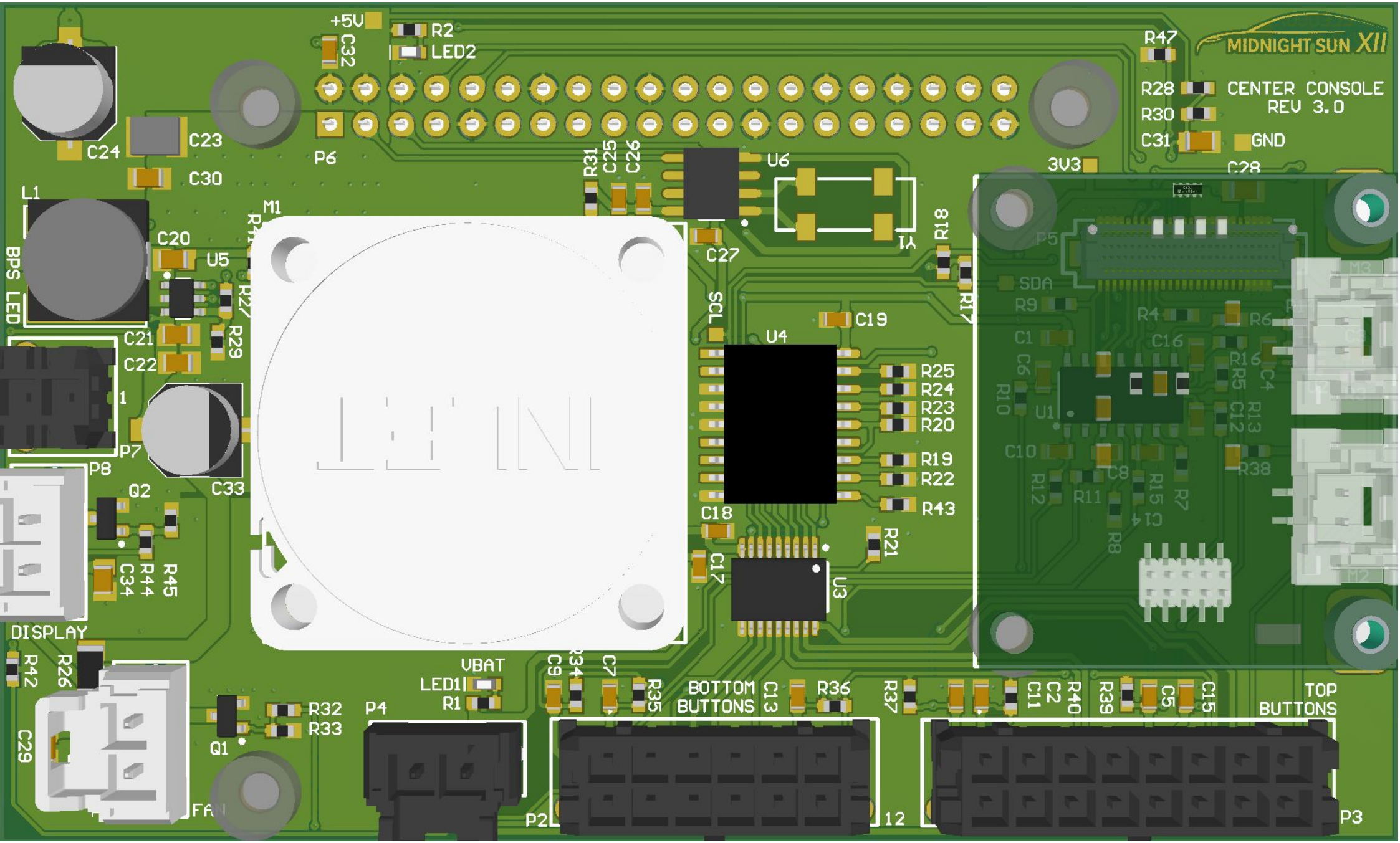
Bill of Materials

Project:	Center Console.PrjPcb
Revision:	3
Project Lead:	Mena Labib
Generated On:	2019-03-18 22:39
Production Quantity:	1
Currency	CAD
Total Parts Count:	104

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
HOLDER BATTERY COIN 12MM DIA	BT1	Keystone Electronics	3000	Digi-Key	36-3000-ND	0.69471	1	$ 0.69
CAP CER 0.1UF 50V 10% X7R 0603	C3, C4, C6, C8, C10, C12, C14, C16, C18, C19	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.15364	12	$ 1.84
CAP CER 10nF 50V 5% X7R 0603	C2, C5, C7, C9, C11, C13, C15	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.48096	7	$ 3.37
CAP CER 1UF 50V 10% X7R 0603	C17, C26, C27	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.37408	3	$ 1.12
CAP CER 0.1UF 100V 10% X7R 0805	C20, C22, C30, C31	Murata	GCM21BR72A104KA37L	Digi-Key	490-4789-1-ND	0.54776	4	$ 2.19
CAP CER 22UF 35V X5R 0805	C21	TDK	C2012X5R1V226M125AC	Digi-Key	445-14428-1-ND	1.66	1	$ 1.66
CAP CER 47UF 6.3V X7R 1210	C23	Murata	GCJ32ER70J476KE01L	Digi-Key	490-10559-1-ND	1.96	1	$ 1.96
CAP ALUM 47UF 20% 35V SMD	C24, C33	Panasonic	EEE1VA470WP	Digi-Key	PCE3961CT-ND	0.54776	2	$ 1.10
CAP CER 2.2UF 25V 10% X5R 0603	C25	Murata	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.22712	1	$ 0.23
CAP CER 10uF 25V 10% X5R 0805	C28, C29, C34	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.57448	3	$ 1.72
IND 3.3uH 5.2A 20MOHM SMD	L1	TDK	VLP8040T-3R3N	Digi-Key	445-6581-1-ND	0.80159	1	$ 0.80
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18704	1	$ 0.19
LED BLUE CLEAR 2.8V 0603	LED2	Vishay Lite-On	LTST-C193TBKT-5A	Digi-Key	160-1827-1-ND	0.62791	1	$ 0.63
FAN AXIAL 30x10MM 12VDC	M1	Delta Design	ASB0312LA-CF00	Digi-Key	603-1728-ND			
STANDOFF RND M2.5X0.45 STEEL 5MM	M2, M3	Wurth Electronics	9774050151R	Digi-Key	732-7095-1-ND	1.46	2	$ 2.91
CONN 2POS ULTRA-FIT NATURAL COLOR 0.138	P1, P8	Molex	1722872102	Digi-Key	WM11722-ND	1.15	2	$ 2.30
CONN 12POS MICRO-FIT 3mm	P2	Molex	43045-1227	Digi-Key	WM10697-ND	3.45	1	$ 3.45
CONN 16POS MICRO-FIT 3mm	P3	Molex	430451627	Digi-Key	WM10708-ND	4.36	1	$ 4.36
CONN 2POS ULTRA-FIT 0.138"	P4	Molex	1722861302	Digi-Key	WM11673-ND	1.95	1	$ 1.95
CONN 50POS Bergstak Plug 0.02"	P5	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.87	1	$ 1.87
CONN 40POS RECEPTACLE 2.54 mm	P6	Adafruit Industries	1992	Digi-Key	1528-1969-ND	3.94	1	$ 3.94
CONN 2POS MICRO-FIT 3mm	P7	Molex	43045-0227	Digi-Key	WM10657-ND	1.12	1	$ 1.12
MOSFET N-CH 30V 6.2A 0.9W SOT-23	Q1, Q2	Diodes	DMN3023L-7	Digi-Key	DMN3023L-7DICT-ND	0.6012	2	$ 1.20
RES 10K OHM 1% 1/10W 0603	R22, R23, R24, R25, R28, R29, R30, R33, R34	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.03206	31	$ 0.99
RES 1K OHM 5% 1/10W 0603	R3, R10, R11, R12, R13, R15, R16, R31	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.1336	8	$ 1.07
RES 4.7K OHM 1% 1/10W 0603	R17, R18	Yageo Phycomp	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.1336	2	$ 0.27
RES 0.006 OHM 1% 1/2W 1206	R26	Panasonic	ERJMP2KF6M0U	Digi-Key	P19333CT-ND	0.56112	1	$ 0.56
RES 54.9K OHM 1% 1/10W 0603	R27	Panasonic	ERJ3EKF5492V	Digi-Key	P54.9KHCT-ND	0.1336	1	$ 0.13
RES 100 OHM 1% 1/10W 0603	R32, R44	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.1336	2	$ 0.27
RES 0.0 OHM 1/4W 0603	R41	Vishay Dale	CRCW06030000Z0EAHP	Digi-Key	541-0.0SBCT-ND	0.22712	1	$ 0.23
IC INVERTER SCHMITT 6CH 14TSSOP	U1	STMicroelectronics	M74HC14YTTR	Digi-Key	497-14387-1-ND	0.58784	1	$ 0.59
IC INVERTER SCHMITT 1CH SC70-5	U2	Texas Instruments	SN74LVC1G14QDCKRQ1	Digi-Key	296-47215-1-ND	0.48096	1	$ 0.48
IC LOAD SWITCH 8CH 0.5A 18SOP	U3	Toshiba	TBD62783AFG,EL	Digi-Key	TBD62783AFGELCT-ND	1.54	1	$ 1.54
IC I/O EXPANDER I2C 8B 18SOIC	U4	Microchip	MCP23008T-E/SO	Digi-Key	MCP23008T-E/SOCT-ND	1.4	1	$ 1.40
REG BUCK 4.5V TO 17V, 5A, SYNCHRONOUS S	U5	Texas Instruments	TPS565201DDCT	Digi-Key	296-47501-1-ND	3.29	1	$ 3.29
IC RTC CLK/CALENDAR I2C 8-SOIC	U6	NXP Semiconductors	PCF8523T/1,118	Digi-Key	568-5306-1-ND			
CRYSTAL 32.7680KHZ 12.5PF SMD	Y1	ECS International	ECS-.327-12.5-17X-TR	Digi-Key	XC1195CT-ND	0.74815	1	$ 0.75
							Total:	$ 52.17


MIDNIGHT SUN XII
CENTER CONSOLE
REV 3.0
+5V
R2
LED2
C32
R47
R28
R30
C31
GND
3V3
C28
C24
C23
C30
P6
R31
C25
C26
U6
Y1
R18
C27
L1
BPS LED
C20
U5
R27
R29
C21
C22
P7
P8
C33
Q2
R44
R45
C34
DISPLAY
R42
R26
C29
Q1
R32
R33
VBAT
LED1
R1
P4
C9
R34
C7
R35
BOTTOM
BUTTONS
C13
R36
R37
C11
C2
R40
R39
C5
C15
TOP
BUTTONS
P2
12
P3
M1
SCL
SDA
U4
C19
R25
R24
R23
R20
R19
R22
R43
C18
C17
U3
R21
P5
R9
R4
R6
C1
C16
C6
R10
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R11
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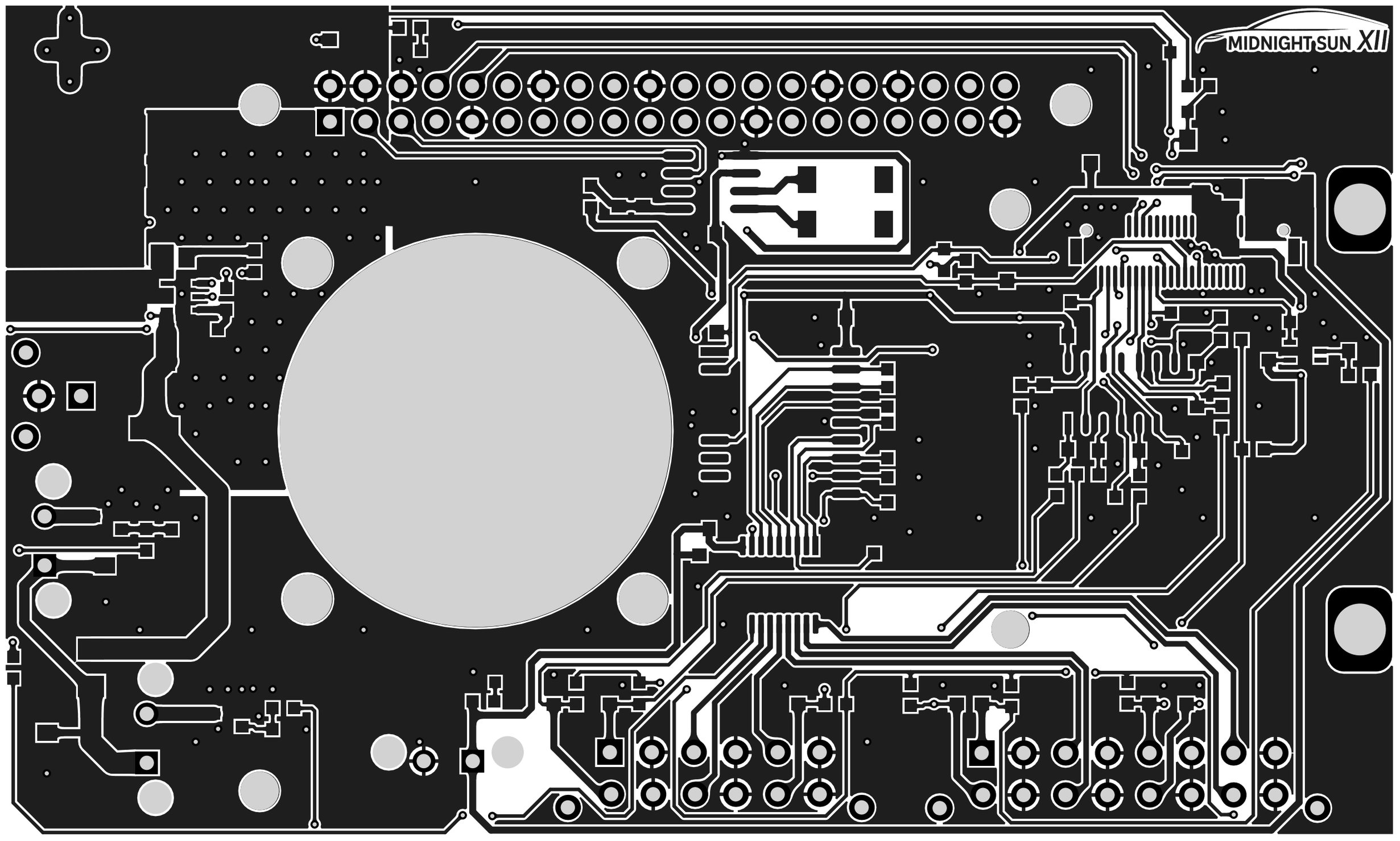
C14
R7
R8
R38


MIDNIGHT SUN XII

19/03
MS-ELE0007
REV 3.0

Electrical Rules Check Report

Class	Document	Message
Warning	Center Console - Connectors.SchDoc	BPS_LED contains Output Port and Unspecified Port objects (Port BPS_LED,Port BPS_LED)
Warning	Center Console - Connectors.SchDoc	DRIVE_LED contains Output Port and Unspecified Port objects (Port DRIVE_LED,Port DRIVE_LED)
Warning	Center Console - Connectors.SchDoc	DRL_LED contains Output Port and Unspecified Port objects (Port DRL_LED,Port DRL_LED)
Warning	Center Console - Connectors.SchDoc	HAZARDS_LED contains Output Port and Unspecified Port objects (Port HAZARDS_LED,Port HAZARDS_LED)
Warning	Center Console - Connectors.SchDoc	LOW_BEAM_LED contains Output Port and Unspecified Port objects (Port LOW_BEAM_LED,Port LOW_BEAM_LED)
Warning	Center Console - Connectors.SchDoc	Net BPS_LED has no driving source (Pin R42-2,Pin U3-11)
Warning	Center Console - Connectors.SchDoc	Net DRIVE_LED has no driving source (Pin P3-15,Pin U3-17)
Warning	Center Console - Connectors.SchDoc	Net DRL_LED has no driving source (Pin P2-5,Pin U3-14)
Warning	Center Console - Connectors.SchDoc	Net HAZARDS_LED has no driving source (Pin P2-3,Pin U3-12)
Warning	Center Console - Connectors.SchDoc	Net LOW_BEAM_LED has no driving source (Pin P2-9,Pin U3-13)
Warning	Center Console - Raspberry Pi Interface.SchDoc	Net NetU6_1 has no driving source (Pin U6-1,Pin Y1-1)
Warning	Center Console - Connectors.SchDoc	Net NEUTRAL_LED has no driving source (Pin P3-11,Pin U3-16)
Warning	Center Console - Buttons Interface.SchDoc	Net PA0_LOW_BEAM has no driving source (Pin P5-25,Pin R9-1,Pin U1-2)
Warning	Center Console - Buttons Interface.SchDoc	Net PA1_HAZARDS has no driving source (Pin P5-24,Pin R8-1,Pin U1-4)
Error	Center Console - Raspberry Pi Interface.SchDoc	Net PA3_RPI_USART2_RX contains multiple Input Ports (Port PA3_USART2_RX/RPI_TX,Port PA3_USART2_RX/RPI_TX)
Error	Center Console - Buttons Interface.SchDoc	Net PA8_1 has only one pin (Pin P5-7)
Error	Center Console - Buttons Interface.SchDoc	Net PA9_1 has only one pin (Pin P5-6)
Error	Center Console - Buttons Interface.SchDoc	Net PA10_1 has only one pin (Pin P5-5)
Error	Center Console - Buttons Interface.SchDoc	Net PA15/LED_RED_1 has only one pin (Pin P5-39)
Error	Center Console - Buttons Interface.SchDoc	Net PB2_1 has only one pin (Pin P5-15)
Error	Center Console - Buttons Interface.SchDoc	Net PB3/LED_GREEN_1 has only one pin (Pin P5-38)
Error	Center Console - Buttons Interface.SchDoc	Net PB4/LED_BLUE_1 has only one pin (Pin P5-37)
Error	Center Console - Buttons Interface.SchDoc	Net PB5/LED_BLUE_1 has only one pin (Pin P5-36)
Error	Center Console - Buttons Interface.SchDoc	Net PB6/USART1_TX_1 has only one pin (Pin P5-34)
Error	Center Console - Buttons Interface.SchDoc	Net PB7/USART1_RX_1 has only one pin (Pin P5-33)
Error	Center Console - Raspberry Pi Interface.SchDoc	Net PB8/DISPLAY_EN contains multiple Input Ports (Port PB8_DISPLAY_EN,Port PB8_DISPLAY_EN)
Error	Center Console - Raspberry Pi Interface.SchDoc	Net PB9_FAN_EN contains multiple Input Ports (Port PB9_FAN_EN,Port PB9_FAN_EN)
Error	Center Console - Buttons Interface.SchDoc	Net PB13/SPI2_SCK_1 has only one pin (Pin P5-10)
Error	Center Console - Buttons Interface.SchDoc	Net PB14/SPI2_MISO_1 has only one pin (Pin P5-9)
Error	Center Console - Buttons Interface.SchDoc	Net PB15/SPI2_MOSI_1 has only one pin (Pin P5-8)
Error	Center Console - Buttons Interface.SchDoc	Net PC13_1 has only one pin (Pin P5-30)
Warning	Center Console - Connectors.SchDoc	Net PWR_LED has no driving source (Pin P3-3,Pin U3-15)
Warning	Center Console - Connectors.SchDoc	Net REVERSE_LED has no driving source (Pin P3-7,Pin U3-18)
Warning	Center Console - Connectors.SchDoc	Nets Wire PA2_RPI_USART2_TX has multiple names (Net Label PA2_RPI_USART2_TX,Port PA2_USART2_TX/RPI_RX)
Warning	Center Console - Buttons Interface.SchDoc	Nets Wire PA2_RPI_USART2_TX has multiple names (Net Label PA2_RPI_USART2_TX,Port PA2_USART2_TX/RPI_RX,Port PA2_USART2_TX/RPI_RX)
Warning	Center Console - Connectors.SchDoc	Nets Wire PA3_RPI_USART2_RX has multiple names (Net Label

Class	Document	Message
		PA3_RPI_USART2_RX,Port PA3_USART2_RX/RPI_TX)
Warning	Center Console - Buttons Interface.SchDoc	Nets Wire PA3_RPI_USART2_RX has multiple names (Net Label PA3_RPI_USART2_RX,Port PA3_USART2_RX/RPI_TX,Port PA3_USART2_RX/RPI_TX)
Warning	Center Console - Connectors.SchDoc	Nets Wire PB8/DISPLAY_EN has multiple names (Net Label PB8/DISPLAY_EN,Port PB8_DISPLAY_EN)
Warning	Center Console - Buttons Interface.SchDoc	Nets Wire PB8/DISPLAY_EN has multiple names (Net Label PB8/DISPLAY_EN,Port PB8_DISPLAY_EN,Port PB8_DISPLAY_EN)
Warning	Center Console - Connectors.SchDoc	NEUTRAL_LED contains Output Port and Unspecified Port objects (Port NEUTRAL_LED,Port NEUTRAL_LED)
Warning	Center Console - Raspberry Pi Interface.SchDoc	Off grid at 1995.469mil,2798.267mil
Warning	Center Console - Connectors.SchDoc	Off grid at 11293.983mil,4199.713mil
Warning	Center Console - Connectors.SchDoc	Off grid at 12006.601mil,4198.306mil
Warning	Center Console - Raspberry Pi Interface.SchDoc	PA2_USART2_TX/RPI_RX contains IO Pin and Output Port objects (Port PA2_USART2_TX/RPI_RX)
Warning	Center Console - Raspberry Pi Interface.SchDoc	PA3_USART2_RX/RPI_TX contains IO Pin and Input Port objects (Port PA3_USART2_RX/RPI_TX)
Warning	Center Console - Connectors.SchDoc	PWR_LED contains Output Port and Unspecified Port objects (Port PWR_LED,Port PWR_LED)
Warning	Center Console - Connectors.SchDoc	REVERSE_LED contains Output Port and Unspecified Port objects (Port REVERSE_LED,Port REVERSE_LED)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\Midnight Sun\hardware\MSXII_Center_Console\Center Console.PcbDoc

Warnings 0
Rule Violations 106

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.25mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=100mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	67
Silk to Silk (Clearance=0.254mm) (All),(All)	27
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	12
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	106

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.178mm) Between Arc (11.95mm,40.475mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad 3V3-TP(77.98mm,48.326mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C2-1(70.2mm,9.7mm) on Top Layer And Text "1" (70.18mm,9.955mm) on
Silk To Solder Mask Clearance Constraint: (0.167mm < 0.178mm) Between Pad C22-1(11.95mm,34.2mm) on Top Layer And Text "C22" (9mm,33.7mm) on
Silk To Solder Mask Clearance Constraint: (0.099mm < 0.178mm) Between Pad C33-2(16.95mm,29.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C4-1(90.725mm,34.25mm) on Top Layer And Text "C4"
Silk To Solder Mask Clearance Constraint: (0.064mm < 0.178mm) Between Pad C4-1(90.725mm,34.25mm) on Top Layer And Text "R16"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C7-1(43.6mm,9.7mm) on Top Layer And Text "1" (43.7mm,9.955mm) on
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad GND-TP(88.925mm,50mm) on Top Layer And Text "GND"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad L1-1(6.15mm,38.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad L1-1(6.15mm,38.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad L1-2(6.15mm,43.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad L1-2(6.15mm,43.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad L1-2(6.15mm,43.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad M2-1(97.225mm,15.025mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad M2-1(97.225mm,15.025mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad M3-1(97.225mm,45.025mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad M3-1(97.225mm,45.025mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P2-0(40.6mm,2.315mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P2-0(40.6mm,2.315mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P2-0(61.6mm,2.315mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P2-0(61.6mm,2.315mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.178mm) Between Pad P3-0(67.18mm,2.265mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P3-0(67.18mm,2.265mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.147mm < 0.178mm) Between Pad P3-0(94.18mm,2.265mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad P7-0(1.86mm,28.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P7-0(1.86mm,28.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad P7-0(1.86mm,34.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.174mm < 0.178mm) Between Pad P7-0(1.86mm,34.8mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-1(17.3mm,8.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-2(17.3mm,9.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q2-1(8.7mm,22.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q2-2(8.7mm,24mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Q2-3(6.7mm,23.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.143mm < 0.178mm) Between Pad R17-1(69.055mm,41.418mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.143mm < 0.178mm) Between Pad R17-2(69.055mm,39.868mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.085mm < 0.178mm) Between Pad R26-1(6.525mm,10.975mm) on Top Layer And Text "FAN

GND" (4.8mm,7.796mm) on Top Overlay [Top Overlay] to [Top Solder] clearance [0.085mm]

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.111mm < 0.178mm) Between Pad R26-2(6.525mm,13.625mm) on Top Layer And Text "DISPLAY"
Silk To Solder Mask Clearance Constraint: (0.138mm < 0.178mm) Between Pad R34-1(41.2mm,11.225mm) on Top Layer And Text "R34"
Silk To Solder Mask Clearance Constraint: (0.149mm < 0.178mm) Between Pad R41-1(18.2mm,40.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.149mm < 0.178mm) Between Pad R41-2(18.2mm,42.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-1(76.355mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-10(81.435mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-11(80.165mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-12(78.895mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-13(77.625mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-14(76.355mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-2(77.625mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-3(78.895mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-4(80.165mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-5(81.435mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-6(82.705mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-7(83.975mm,29.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-8(83.975mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U1-9(82.705mm,34.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-1(11.95mm,39.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-2(11.95mm,38.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-3(11.95mm,37.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-4(14.2mm,37.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-5(14.2mm,38.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.1mm < 0.178mm) Between Pad U5-6(14.2mm,39.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Y1-1(57.7mm,43.957mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Y1-1(57.7mm,43.957mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.178mm) Between Pad Y1-2(63.2mm,43.957mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.178mm) Between Pad Y1-3(63.2mm,47.158mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Y1-4(57.7mm,47.158mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Y1-4(57.7mm,47.158mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (43.7mm,9.955mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "1" (70.18mm,9.955mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "1" (8.7mm,31.346mm) on Top Overlay And Track (8.3mm,27.6mm)(8.3mm,36mm)
Silk To Silk Clearance Constraint: (0.236mm < 0.254mm) Between Text "BPS LED" (0.414mm,42.552mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.015mm < 0.254mm) Between Text "C28" (87.902mm,47.742mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "FAN" (13.886mm,1.843mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.228mm < 0.254mm) Between Text "LED1" (30.173mm,10.84mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.251mm < 0.254mm) Between Text "M1" (18.931mm,44.977mm) on Top Overlay And Text "R41" (17.8mm,44.75mm)
Silk To Silk Clearance Constraint: (0.243mm < 0.254mm) Between Text "P1" (6.621mm,1.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "P1" (6.621mm,1.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.155mm < 0.254mm) Between Text "P2" (37.71mm,1.126mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.156mm < 0.254mm) Between Text "P2" (37.71mm,1.126mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "P5" (74.25mm,42.72mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "P5" (74.25mm,42.72mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "P7" (8.7mm,27.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "P7" (8.7mm,27.5mm) on Top Overlay And Track (8.3mm,27.6mm)(8.3mm,36mm)
Silk To Silk Clearance Constraint: (0.172mm < 0.254mm) Between Text "P8" (6.504mm,26.257mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.172mm < 0.254mm) Between Text "P8" (6.504mm,26.257mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "R16" (88.087mm,34.129mm) on Top Overlay And Text "R5" (88.233mm,33.75mm)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R17" (68.75mm,39.1mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.002mm < 0.254mm) Between Text "R34" (40.8mm,13.996mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.099mm < 0.254mm) Between Text "R41" (17.8mm,44.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.134mm < 0.254mm) Between Text "R41" (17.8mm,44.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.193mm < 0.254mm) Between Text "TOP

BUTTONS" (90.061mm,8.95mm) on Top Overlay And Track (65.98mm,8.705mm)(95.43mm,8.705mm) on Top Overlay Silk T

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "TOP

BUTTONS" (90.061mm,8.95mm) on Top Overlay And Track (95.43mm,1.105mm)(95.43mm,8.705mm) on Top Overlay Silk T

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "U4" (54.95mm,35.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.046mm < 0.254mm) Between Text "VBAT" (4.95mm,5.35mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.383mm < 0.406mm) Between Board Edge And Track (0.583mm,17.608mm)(0.583mm,20.72mm) on Bottom
Board Outline Clearance(Outline Edge): (0.383mm < 0.406mm) Between Board Edge And Track (0.583mm,17.608mm)(0.925mm,17.266mm) on Bottom
Board Outline Clearance(Outline Edge): (0.383mm < 0.406mm) Between Board Edge And Track (0.583mm,20.72mm)(0.608mm,20.745mm) on Bottom
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (0.75mm,59mm)(1.25mm,59.5mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.4mm < 0.406mm) Between Board Edge And Track (0.95mm,2.65mm)(3.075mm,0.525mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (1.25mm,59.5mm)(31.5mm,59.5mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.4mm < 0.406mm) Between Board Edge And Track (3.075mm,0.525mm)(31.825mm,0.525mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (31.5mm,59.5mm)(32.75mm,58.25mm) on Bottom Layer
Board Outline Clearance(Outline Edge): (0.4mm < 0.406mm) Between Board Edge And Track (31.825mm,0.525mm)(33.055mm,1.755mm) on Top Layer
Board Outline Clearance(Outline Edge): (0.148mm < 0.406mm) Between Board Edge And Track (69.75mm,12.5mm)(99.725mm,12.5mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.148mm < 0.406mm) Between Board Edge And Track (69.75mm,47.525mm)(99.725mm,47.525mm) on Top
Board Outline Clearance(Outline Edge): (0.148mm < 0.406mm) Between Board Edge And Track (99.725mm,12.5mm)(99.725mm,47.525mm) on Top