
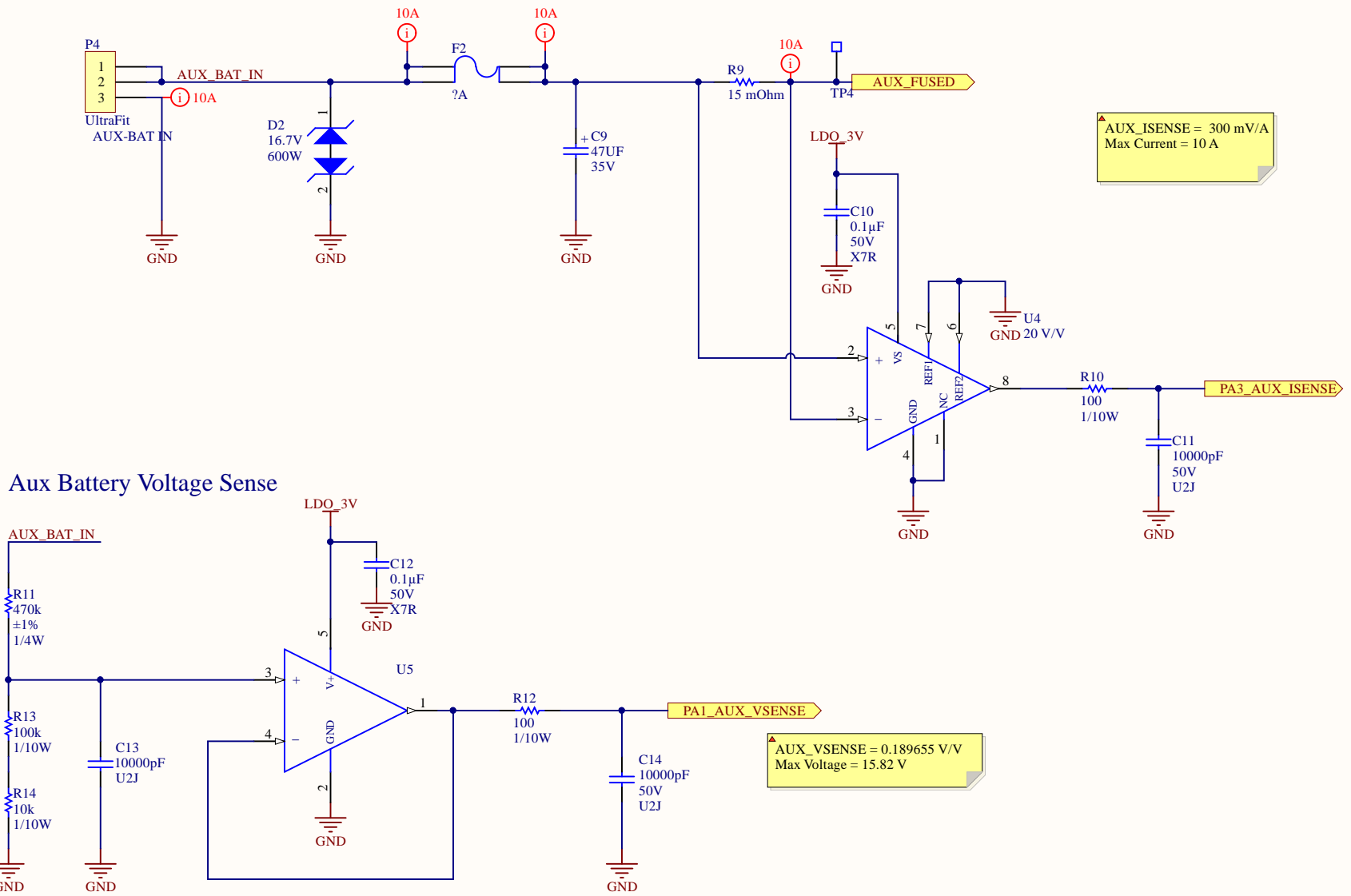
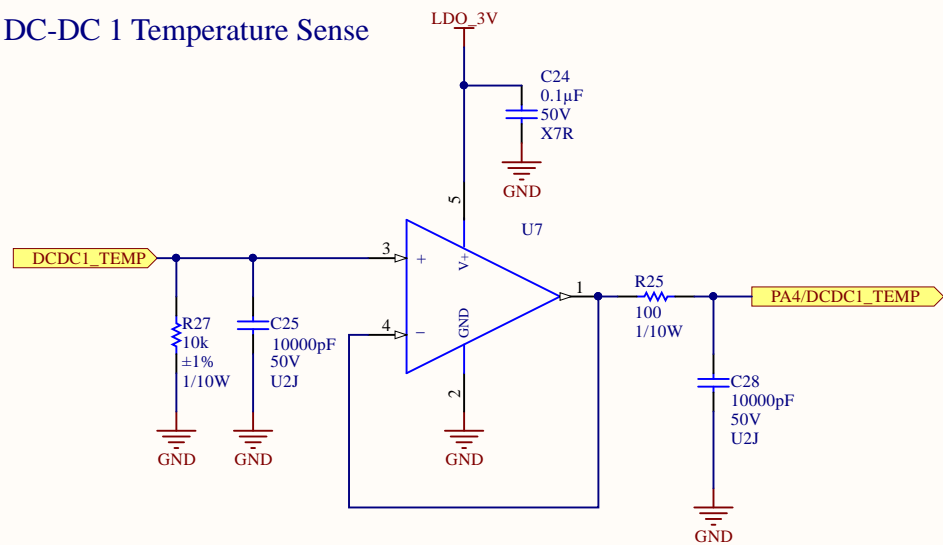


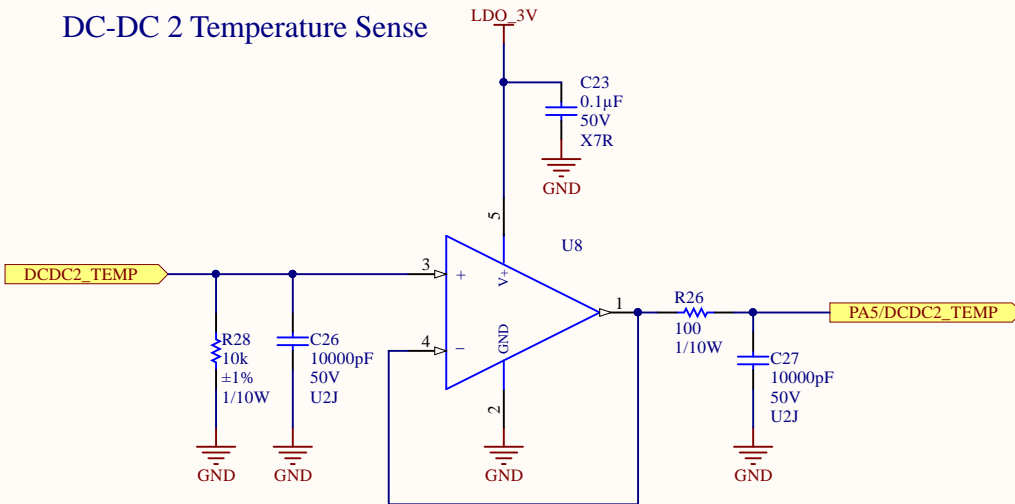
Project: PowerDistribution.PrjPcb		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: Controller Board Interface & Power		
Project Author: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet1 of 10	
		Website: www.uwmidsun.com




DC-DC 1 Temperature Sense

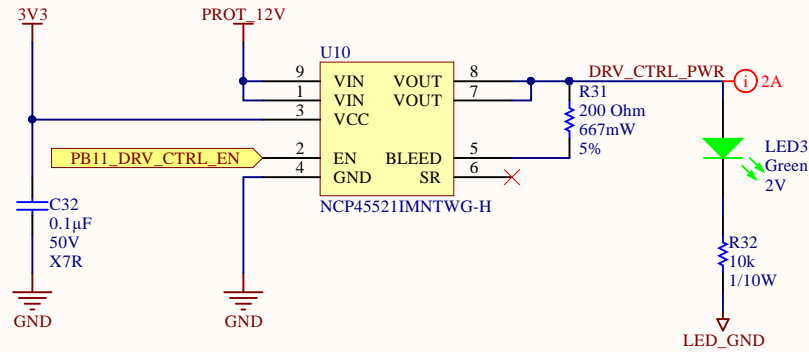


DC-DC 2 Temperature Sense

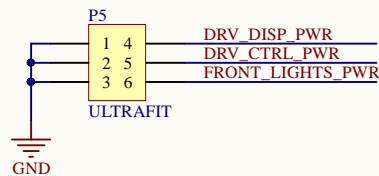
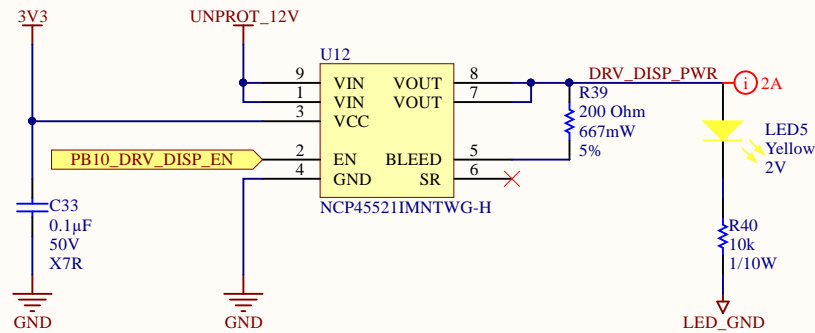


Project: PowerDistribution.PrjPcb		<div>MIDNIGHTSUN</div>
Title: Temperature Sense		
Project Author Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet 5 of 10	

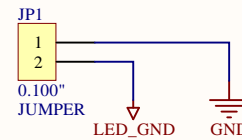
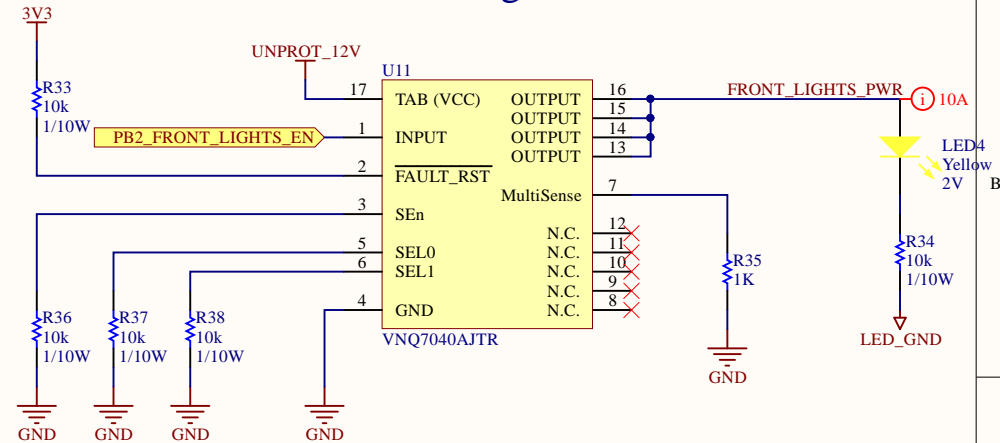
Driver Controls




Driver Display



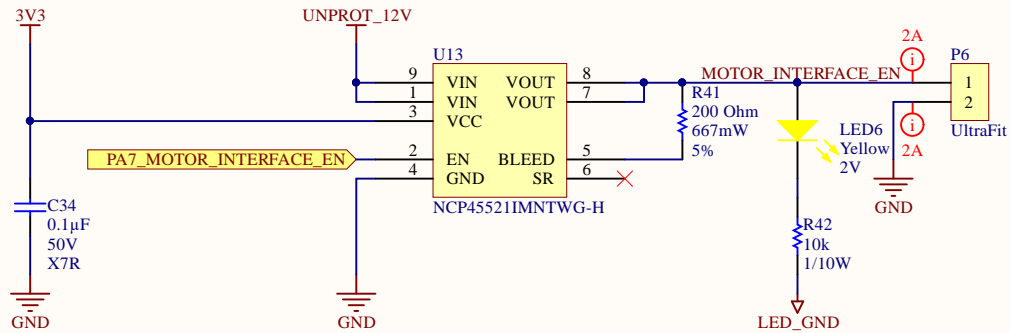
Front Lights



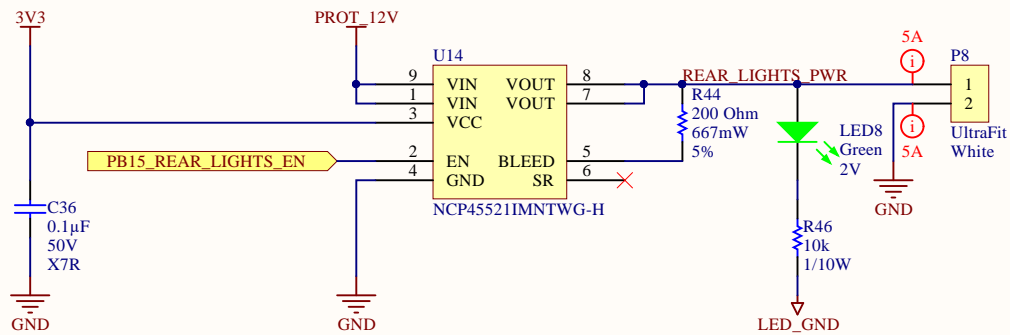
Connect jumper to turn enable all LEDs

Project: PowerDistribution.PrjPcb		<div>MIDNIGHTSUN</div>
Title: Outputs to Front Enclosure		
Project Author: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet 6 of 10	
		Website: www.uwmidsun.com

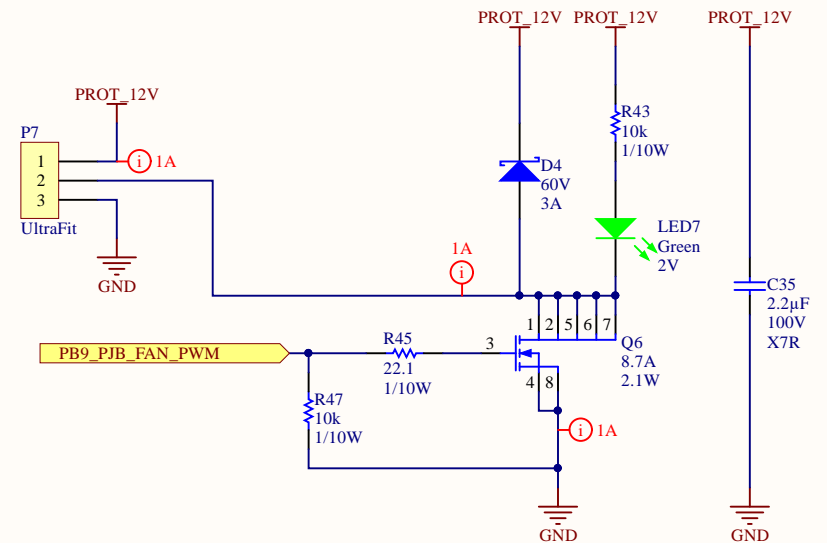
Motor Interface Board




Rear Lights

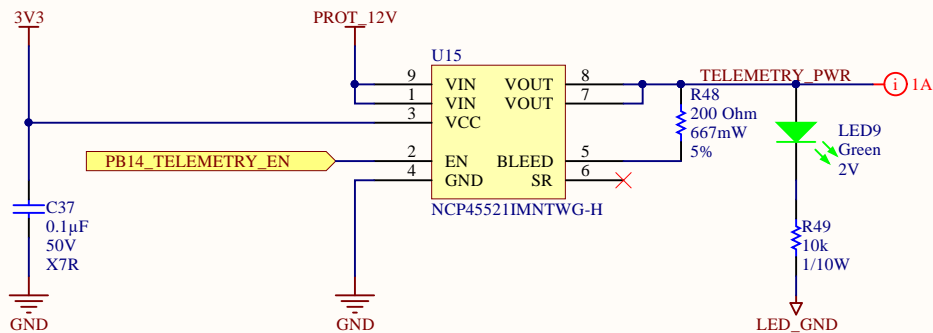


PJB Fan

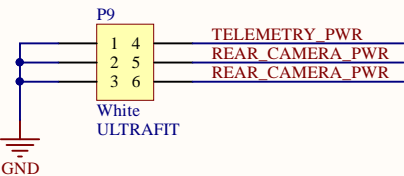
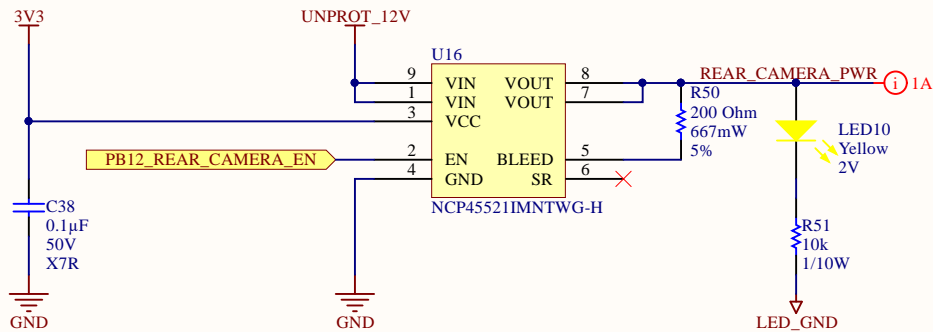



Project: PowerDistribution.PrjPcb		
Title: Outputs to PJB		
Project Author: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet 7 of 10	

Telemetry

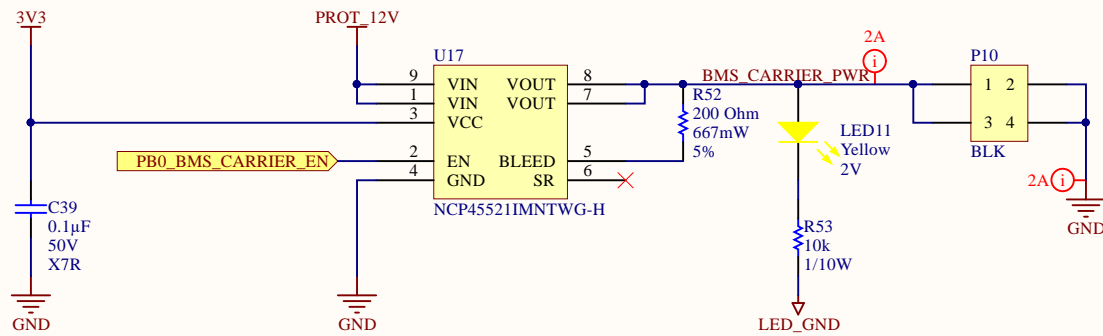


Rear Camera

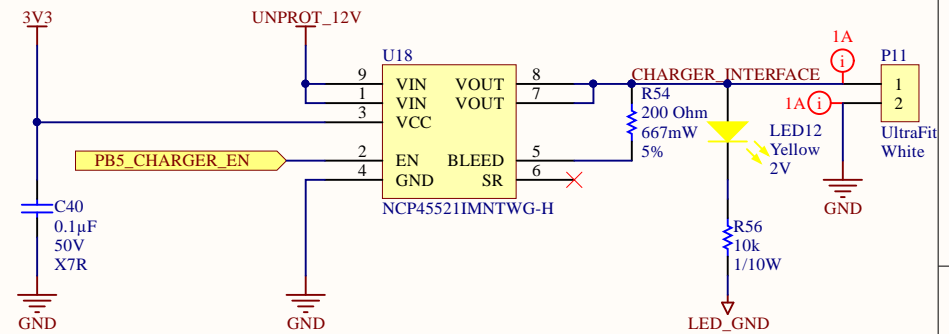


Project: PowerDistribution.PrjPcb		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: Outputs to Roof Enclosure		
Project Author: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet 8 of 10	Website: www.uwmidsun.com

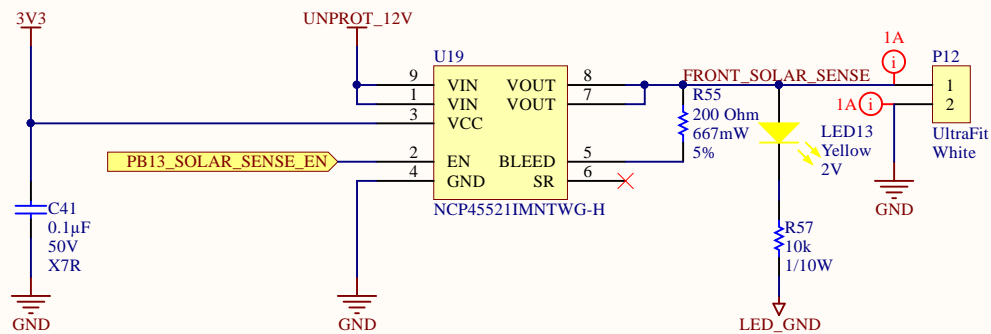
BMS Carrier (Master and Slave)



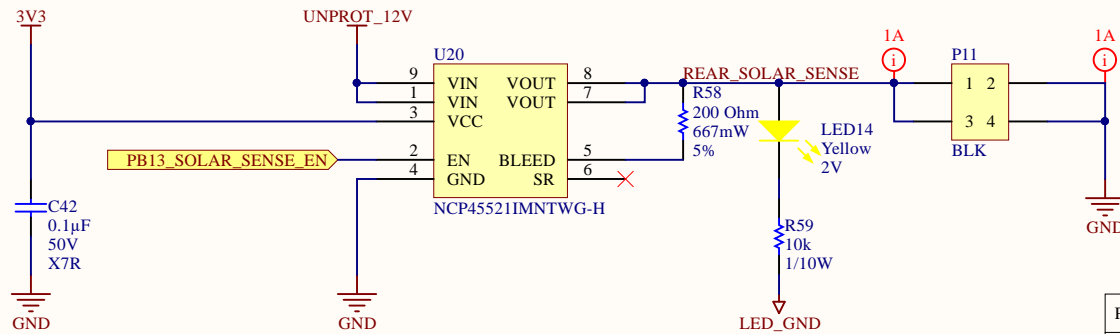
Charger Interface



Front Solar Sense



Rear Solar Sense



Project: **PowerDistribution.PrjPcb**

Title: **Misc Outputs**

Project AuthoTaiping Li

Size: **Letter**

Date: 2018-06-22

Revision: 3.0

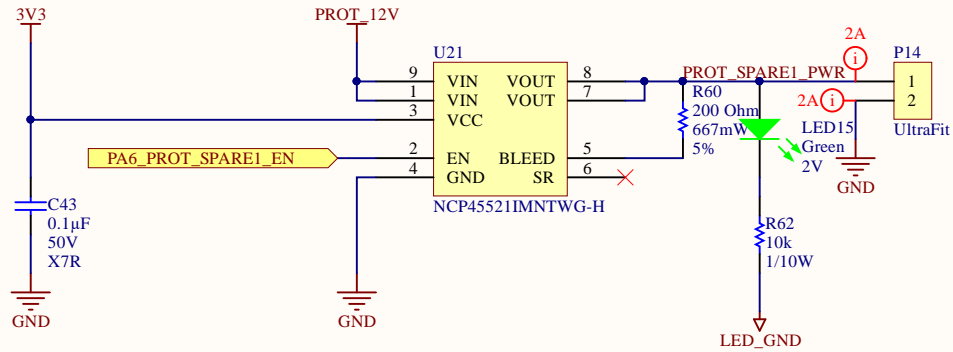
Sheet9 of 10



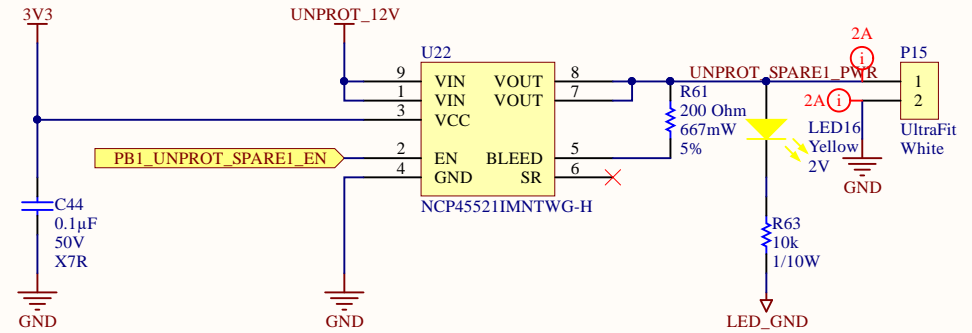
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9

Website: www.uwmidsun.com

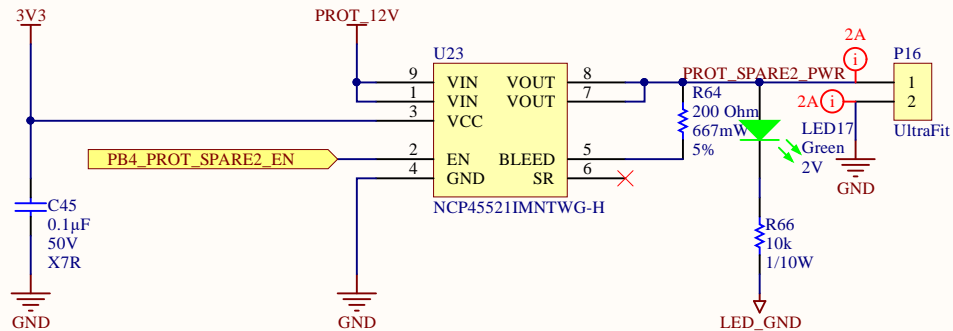
Protected Spare 1



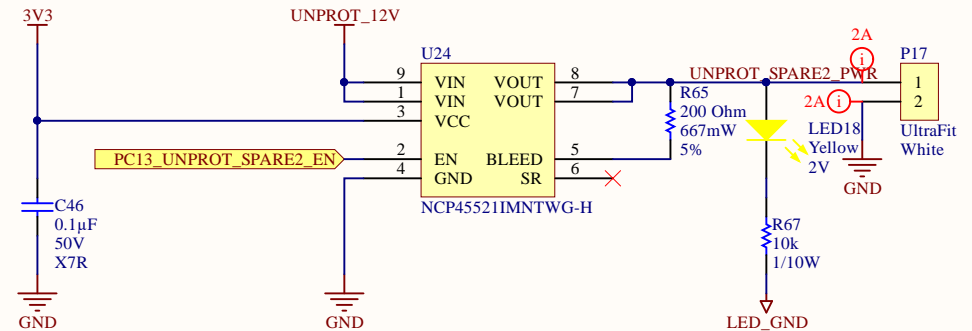
Unprotected Spare 1




Protected Spare 2



Unprotected Spare 2

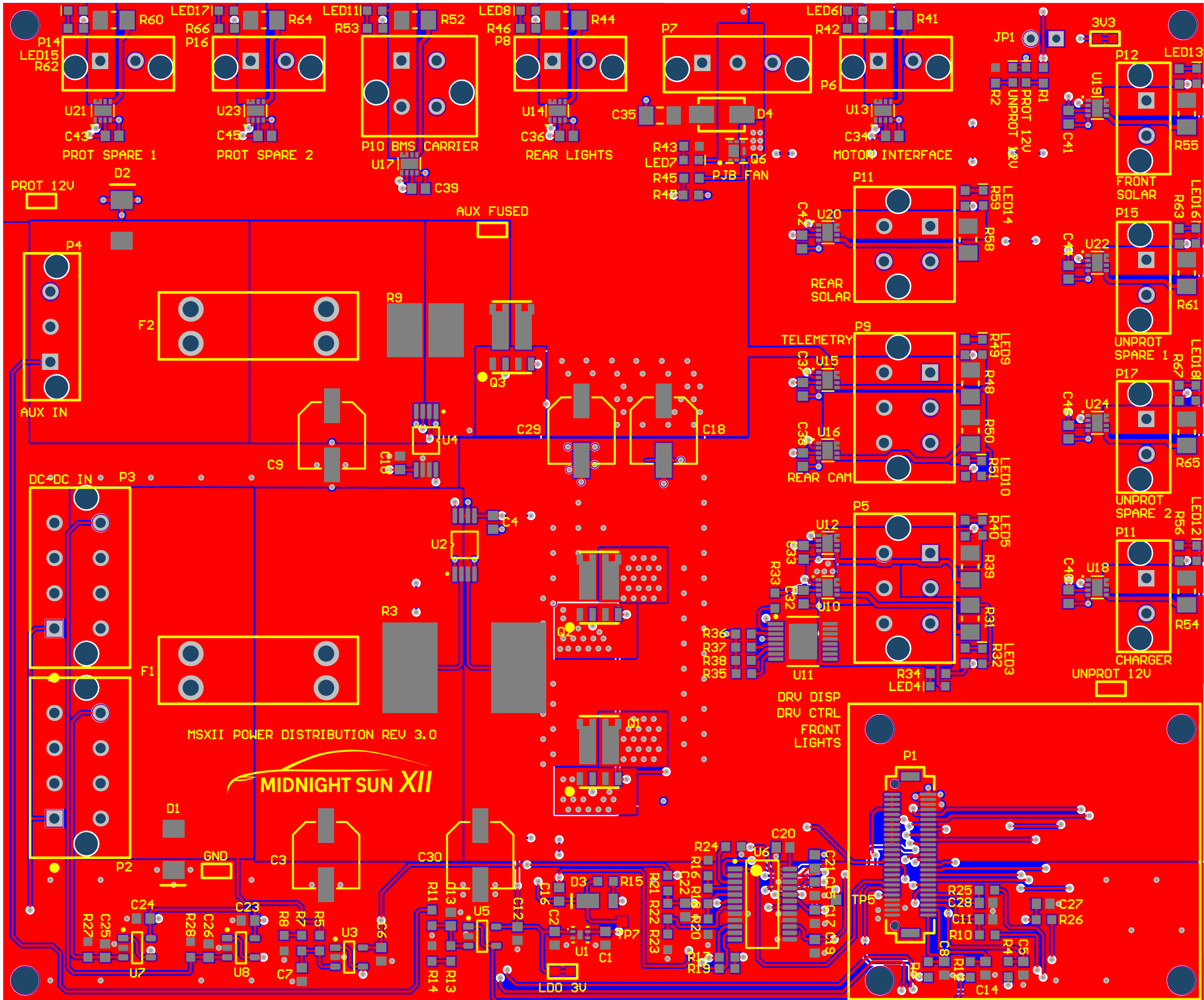


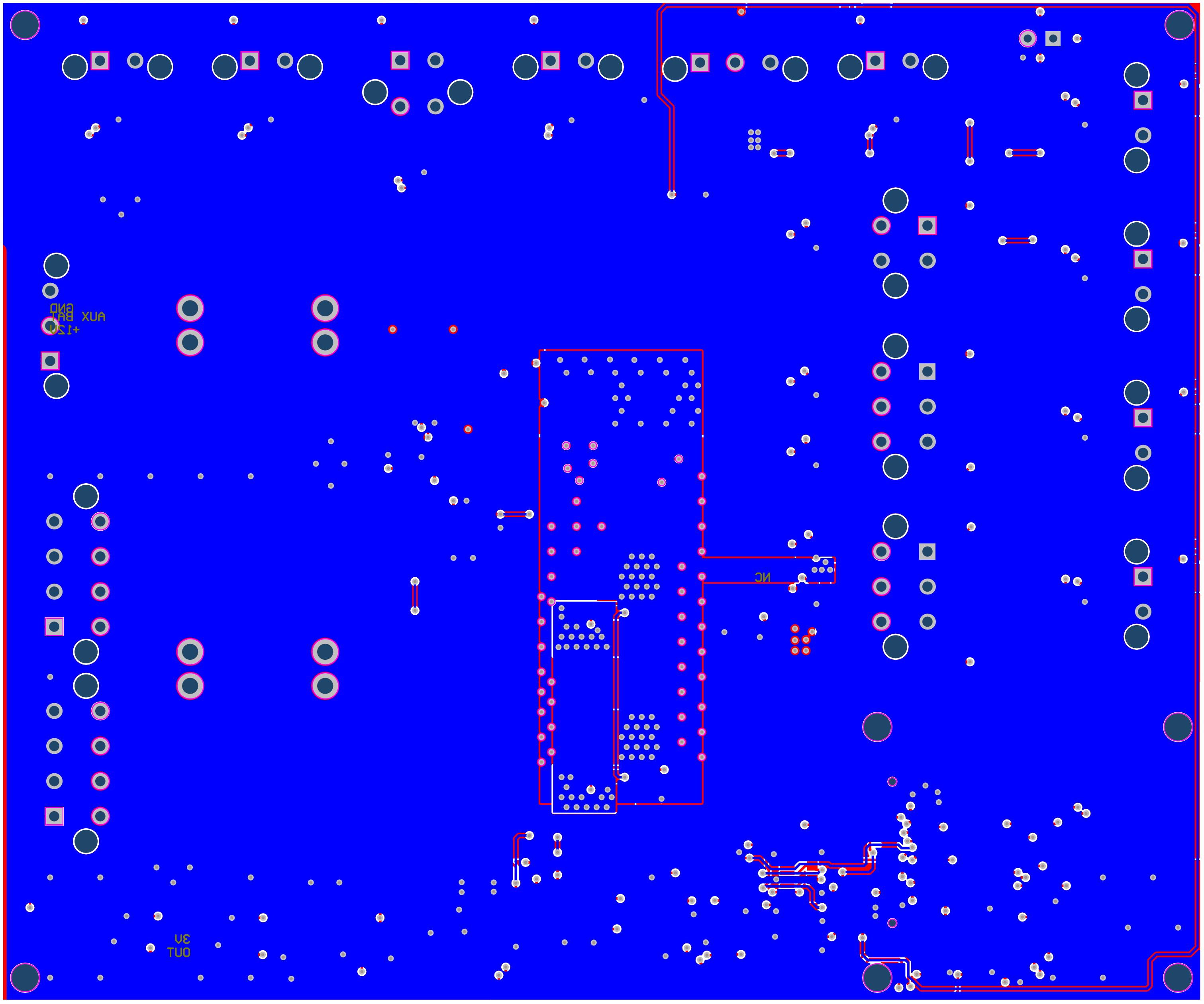
Project: PowerDistribution.PrjPcb		
Title: Spare Outputs		
Project Author: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 3.0	
Date: 2018-06-22	Sheet 10 of 10	

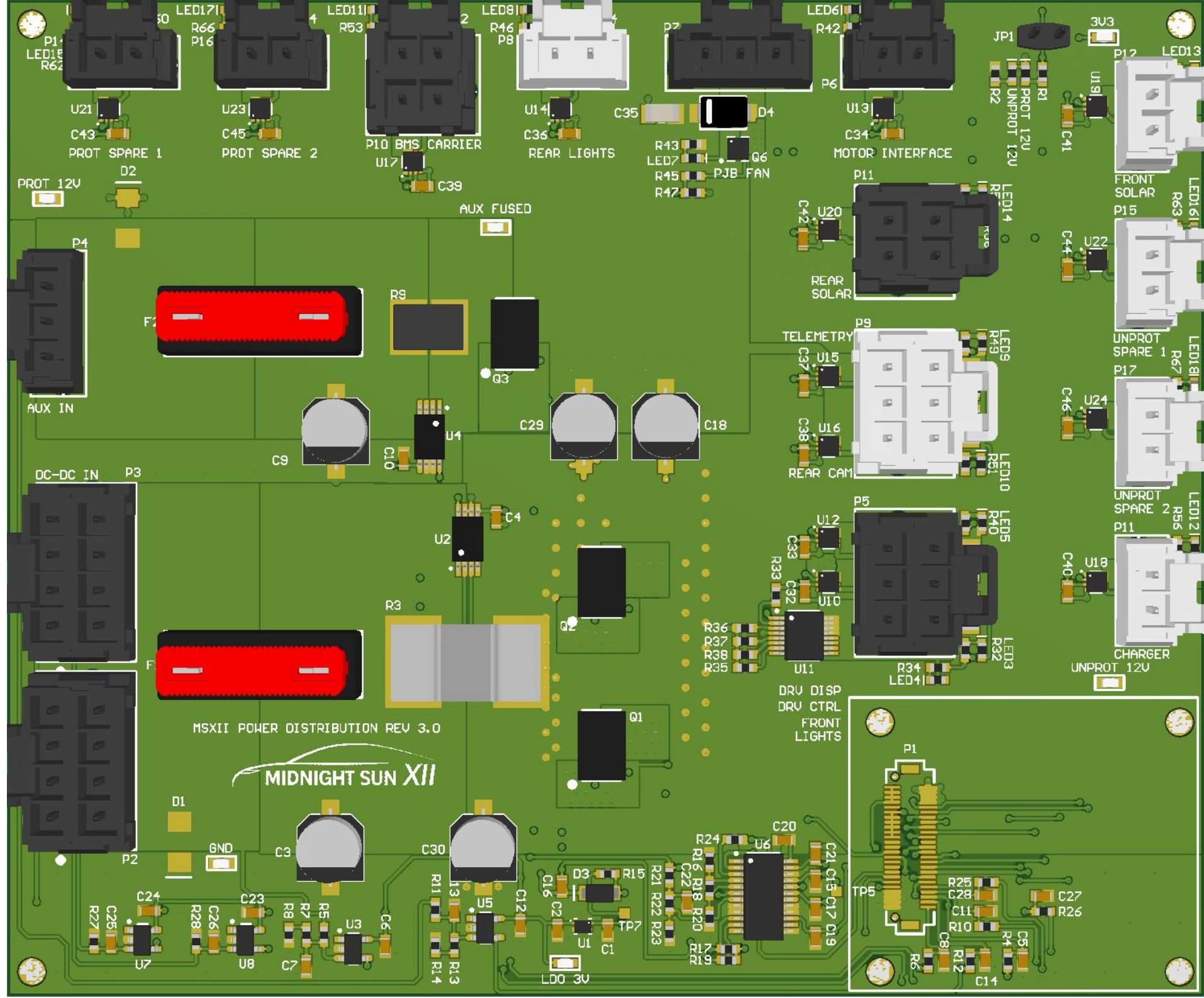
Bill of Materials	
Project:	PowerDistribution.PrjPcb
Revision:	3.0
Project Lead:	Taiping Li
Generated On:	2018-06-22 3:19:53 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	183



LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
Test Point 0603 SMD	TP1, TP2, TP3, TP4, TP6, TP8	TE Connectivity AMP	RCUOC	Digi-Key	A106145CT-ND	0.29	6	\$ 1.76
RES 470K OHM 1% 1/4W 0603	R5, R11	Panasonic	ERJPA3F4703V	Digi-Key	P470KBYCT-ND	0.21	2	\$ 0.43
RES 255K OHM 1% 1/10W 0603	R24	Yageo	RC0603FR-07255KL	Digi-Key	311-255KHRCT-ND	0.13	1	\$ 0.13
RES 200 OHM 5% 2/3W 1206	R31, R39, R41, R44, R48, R50, R52, R54, R55, R58, R60, R61, R64, R65	Panasonic	ERJ-P08J201V	Digi-Key	P200ALCT-ND	0.18	14	\$ 2.55
RES 100K OHM 5% 1/8W 0603	R7, R13	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCT-ND	0.13	2	\$ 0.27
RES 100 OHM 1% 1/10W 0603	R4, R6, R10, R12, R25, R26	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.03	10	\$ 0.32
RES 86.6K OHM 1% 1/10W 0603	R20	Panasonic	ERJ-3EKF8662V	Digi-Key	P86.6KHCT-ND	0.13	1	\$ 0.13
RES 78.7K OHM 1% 1/10W 0603	R23	Panasonic	ERJ-3EKF7872V	Digi-Key	P78.7KHCT-ND	0.13	1	\$ 0.13
RES 54.9K OHM 1% 1/10W 0603	R22	Panasonic	ERJ-3EKF5492V	Digi-Key	P54.9KHCT-ND	0.13	1	\$ 0.13
RES 22.1 OHM 1% 1/10W 0603	R45	Yageo	RC0603FR-0722R1L	Digi-Key	311-22.1HRCT-ND	0.13	1	\$ 0.13
RES 11.8K OHM 1% 1/10W 0603	R18	Yageo	RC0603FR-0711K8L	Digi-Key	311-11.8KHRCT-ND	0.13	1	\$ 0.13
RES 10K OHM 1% 1/10W 0603	R8, R14, R17, R19, R27, R28, R32, R33, R34, R36, R37, R38, R40, R42, R43, R46, R47, R49, R51, R53, R56, R57, R59, R62, R63, R66, R67	Yageo	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.03	27	\$ 0.86
RES 4.7K OHM 1% 1/10W 0603	R1, R2	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13	2	\$ 0.27
RES 2.21K OHM 1% 1/10W 0603	R15	Yageo	AC0603FR-072K21L	Digi-Key	YAG3586CT-ND	0.13	1	\$ 0.13
RES 1M OHM 1% 1/10W 0603	R16, R21	Yageo	RC0603FR-071ML	Digi-Key	311-1.00MHRCT-ND	0.13	2	\$ 0.27
RES 1K OHM 5% 1/10W 0603	R35	Yageo	RC0603JR-071KL	Digi-Key	311-1.0KGRCT-ND	0.13	1	\$ 0.13
RES 0.015 OHM 1% 7W 2818	R9							
RES 0.004 OHM 1% 7W 5931	R3	Yageo	PU5931FKMP70R004L	Digi-Key	YAG4096CT-ND	2.74	1	\$ 2.74
MOSFET P-CH DUAL 30V 60A PPAK SO-8	Q1, Q2, Q3	Vishay Siliconix	SI7997DP-T1-GE3	Digi-Key	SI7997DP-T1-GE3CT-ND	3.31	3	\$ 9.94
MOSFET N-CH 30V 8.7A 2.1W 6-PQFN (2x2)	Q6	Infineon	IRLHS6342TRPBF	Digi-Key	IRLHS6342TRPBFCT-ND	0.93	1	\$ 0.93
LED YELLOW CLEAR 2.1V 0603	LED2, LED4, LED5, LED6, LED10, LED11, LED12, LED13, LED14, LED16, LED18	Würth Electronics	150060YS75000	Digi-Key	732-4981-1-ND	0.19	11	\$ 2.05
LED GREEN CLEAR 2V 0603	LED1, LED3, LED7, LED8, LED9, LED15, LED17	Würth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.19	7	\$ 1.30
IC REG LDO 3V 0.2A 4-TDFN	U1	Microchip	MIC94310-PYMT-TR	Digi-Key	576-4761-1-ND	0.39	1	\$ 0.39
IC OR CONTROLLER SOURCE SELECT 24SSOP	U6	Analog Devices / Linear Technology	LTC4417CGN#PBF	Digi-Key	LTC4417CGN#PBF-ND	9.14	1	\$ 9.14
IC OP AMP GEN PURPOSE RR 10MHZ SOT-23-5	U3, U5, U7, U8	Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND	1.13	4	\$ 4.52
IC LOAD SWITCH ACT-HI 10.5A 8DFN	U10, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24	ON Semiconductor	NCP45521IMNTWG-H	Digi-Key	NCP45521IMNTWG-HOSDKR-ND	1.29	14	\$ 17.99
IC DVR HIGH-SIDE 1CH POWERSSO-16	U11	STMicroelectronics	VN7040AJTR	Digi-Key	497-15853-1-ND	2.42	1	\$ 2.42
IC CURRENT AMPLIFIER INA240A1 20V/V 8-TSSOP	U4	Texas Instruments	INA240A1PWR	Digi-Key	296-45088-1-ND	3.53	1	\$ 3.53
IC CURRENT AMPLIFIER INA240 8-TSSOP	U2	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.53	1	\$ 3.53
FUSE ATO FUSE HOLDER	F1, F2	Keystone Electronics	3557-2	Digi-Key	36-3557-2-ND	1.3	2	\$ 2.61
DIODE TVS 15VWM 24.4VC D0-214AA (SMB)	D1, D2	ON Semiconductor / Fairchild	SMBJ15CA	Digi-Key	SMBJ15CAFSCT-ND	0.68	2	\$ 1.36
DIODE SCHOTTKY 60V 3A SMA	D4	Diodes	B360A-13-F	Digi-Key	B360A-FDICT-ND	0.64	1	\$ 0.64
DIODE SCHOTTKY 30V 1A POWERD123	D3	Diodes	DFLS130L-7	Digi-Key	DFLS130LDICT-ND	0.67	1	\$ 0.67
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.86	1	\$ 1.86
CONN 8POS ULTRA-FIT 0.138"	P2, P3	Molex	1722991108	Digi-Key	WM11779-ND	1.92	2	\$ 3.83
CONN 6POS ULTRA-FIT NATURAL COLOR 0.138"	P9	Molex	1722992106	Digi-Key	WM11799-ND	1.69	1	\$ 1.69
CONN 6POS ULTRA-FIT 0.138"	P5	Molex	1722991106	Digi-Key	WM11778-ND	1.5	1	\$ 1.50
CONN 4POS 2 ROW ULTRA-FIT 0.138"	P10, P11	Molex	1722991104	Digi-Key	WM11777-ND	1.14	2	\$ 2.29
CONN 3POS ULTRA-FIT 0.138"	P4, P7	Molex	1722871103	Digi-Key	WM11702-ND	1.09	2	\$ 2.18
CONN 2POS ULTRA-FIT NATURAL COLOR 0.138"	P8, P11, P12, P15, P17	Molex	1722872102	Digi-Key	WM11722-ND	1.09	5	\$ 5.45
CONN 2POS ULTRA-FIT 0.138"	P6, P14, P16	Molex	1722861302	Digi-Key	WM11673-ND	1.84	3	\$ 5.51
CONN 2POS JUMPER 0.1"	JP1	Omron	XG8T-0231	Digi-Key	XG8T-0231-ND	0.25	1	\$ 0.25
CAP CER 6800pF 50V 10% X7R 0603	C16	Samsung	CL10B682KB85FNC	Digi-Key	1276-2103-1-ND	0.13	1	\$ 0.13
CAP CER 10nF 50V 5% X7R 0603	C5, C7, C8, C11, C13, C14, C25, C26, C27, C28	KEMET	C0603C103J5JAC7867	Digi-Key	399-13384-1-ND	0.27	10	\$ 2.71
CAP CER 2.2UF 100V ±20% X7R 1206	C35	Murata	GRM31CR72A225MA73L	Digi-Key	490-12773-1-ND	0.93	1	\$ 0.93
CAP CER 1UF 50V 10% X7R 0603	C1, C2	Taivo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.39	2	\$ 0.77
CAP CER 0.1UF 50V 10% X7R 0603	C4, C6, C10, C12, C15, C19, C20, C21, C23, C24, C32, C33, C34, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.15	24	\$ 3.64
CAP CER 0.068UF 10% 50V X7R 0603	C17	Murata	GCM188R71H683KA57D	Digi-Key	490-8027-1-ND	0.21	1	\$ 0.21
CAP CER 0.022UF 50V 10% X7R 0603	C22	Murata	GRM188R71H223KA01D	Digi-Key	490-1517-1-ND	0.17	1	\$ 0.17
CAP ALUM 100UF 20% 35V SMD	C18	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951CT-ND	0.59	1	\$ 0.59
CAP ALUM 47UF 20% 35V SMD	C3, C9	Panasonic	EEE-1VA470WP	Digi-Key	PCE3961CT-ND	0.51	2	\$ 1.01
							Total:	\$ 106.28







Electrical Rules Check Report

Class	Document	Message
Error	Power Distribution - Misc Boards.SchDoc	Duplicate Component Designators P11 at 5450mil,2200mil and 10490mil,5150mil
Error	Power Distribution - Misc Boards.SchDoc	Duplicate Component Designators P11 at 10490mil,5150mil and 5450mil,2200mil
Warning	Power Distribution - DC-DC.SchDoc	Net NetC3_1 has no driving source (Pin C3-1,Pin F1-2,Pin F1-4,Pin R3-1,Pin U2-2)
Warning	Power Distribution - DC-DC.SchDoc	Net NetC7_1 has no driving source (Pin C7-1,Pin R5-2,Pin R7-1,Pin U3-3)
Warning	Power Distribution - Aux Battery.SchDoc	Net NetC9_1 has no driving source (Pin C9-1,Pin F2-2,Pin F2-4,Pin R9-1,Pin U4-2)
Warning	Power Distribution - Aux Battery.SchDoc	Net NetC13_1 has no driving source (Pin C13-1,Pin R11-2,Pin R13-1,Pin U5-3)
Error	Power Distribution - Misc Boards.SchDoc	Net NetU19_2 contains multiple Input Ports (Port PB13_SOLAR_SENSE_EN,Port PB13_SOLAR_SENSE_EN)
Warning	Controller_Board_Interface.SchDoc	Net PA15/LED_RED has only one pin (Pin P1-39)
Warning	Controller_Board_Interface.SchDoc	Net PB3/LED_GREEN has only one pin (Pin P1-38)
Warning	Power Distribution - Power Path.SchDoc	Net PB8/EN has no driving source (Pin P1-32,Pin U6-1)
Error	Power Distribution - PJB.SchDoc	Net PB9_PJB_FAN_PWM contains multiple Input Ports (Port PB9_PJB_FAN_PWM,Port PB9_PJB_FAN_PWM)
Error	Power Distribution - Misc Boards.SchDoc	Net PB13_SOLAR_SENSE_EN contains multiple Input Ports (Port PB13_SOLAR_SENSE_EN,Port PB13_SOLAR_SENSE_EN)
Error	Power Distribution - Spare Outputs.SchDoc	Net PC13_UNPROT_SPARE2_EN contains multiple Input Ports (Port PC13_UNPROT_SPARE2_EN,Port PC13_UNPROT_SPARE2_EN)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA8/SHHDIN\ has multiple names (Net Label PA8/SHHDIN,Net Label PA8_SHHDIN)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB8/EN has multiple names (Net Label PB8/EN,Net Label PB8_EN)
Warning	Power Distribution - Spare Outputs.SchDoc	Net UNPROT_12V has no driving source (Pin C20-1,Pin C30-1,Pin Q1-7,Pin Q1-8,Pin Q2-7,Pin Q2-8,Pin R2-1,Pin R3-2,Pin R16-1,Pin TP3-1,Pin U2-3,Pin U6-24,Pin U11-17,Pin U12-1,Pin U12-9,Pin U13-1,Pin U13-9,Pin U16-1,Pin U16-9,Pin U18-1,Pin U18-9,Pin U19-1,Pin U19-9,Pin U20-1,Pin U20-9,Pin U22-1,Pin U22-9,Pin U24-1,Pin U24-9)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_PowerDistribution\F

Warnings 0
Rule Violations 420

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.127mm) (IsStitchingVia and InNet('UNPROT_12V')),(IsVia and (Not IsStitchingVia)) Or	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	1
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=1.27mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	81
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	264
Silk to Silk (Clearance=0.254mm) (All),(All)	64
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	3
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	420

Un-Routed Net Constraint ((All))	
Isolated copper: Split Plane (GND) on Ground. Dead copper detected. Copper area is : 0.416 sq. mm	

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(117.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(117.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(117.65mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,97.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(87.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(87.5mm,27.5mm) on Multi-Layer Actual Hole Size = 2.7mm	

Minimum Solder Mask Sliver (Gap=0.254mm) (All), (All)
Minimum Solder Mask Sliver Constraint: (0.097mm < 0.254mm) Between Pad C18-2(66mm,54.225mm) on Component Side And Via (66mm,51.9mm) from
Minimum Solder Mask Sliver Constraint: (0.186mm < 0.254mm) Between Pad C28-1(97.375mm,10.211mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.186mm < 0.254mm) Between Pad C28-2(98.725mm,10.211mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.075mm < 0.254mm) Between Pad C29-2(57.826mm,54.225mm) on Component Side And Via
Minimum Solder Mask Sliver Constraint: (0.034mm < 0.254mm) Between Pad C29-2(57.826mm,54.225mm) on Component Side And Via
Minimum Solder Mask Sliver Constraint: (0.052mm < 0.254mm) Between Pad C29-2(57.826mm,54.225mm) on Component Side And Via
Minimum Solder Mask Sliver Constraint: (0.208mm < 0.254mm) Between Pad C30-2(47.749mm,12mm) on Component Side And Via
Minimum Solder Mask Sliver Constraint: (0.208mm < 0.254mm) Between Pad C30-2(47.749mm,12mm) on Component Side And Via (49.235mm,12mm)
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad LED4-1(93.98mm,31.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad LED4-2(92.48mm,31.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.201mm < 0.254mm) Between Pad LED6-1(85.75mm,98.952mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad LED9-1(97.7mm,64.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(89mm,22.05mm) on Multi-Layer And Pad P1-(90.5mm,22.8mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(89mm,7.95mm) on Multi-Layer And Pad P1-(90.5mm,7.2mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-1(72.6mm,84.061mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-2(73.25mm,84.061mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-3(73.9mm,84.061mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q6-3(73.9mm,84.061mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-4(73.9mm,85.911mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-4(73.9mm,85.911mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-4(73.9mm,85.911mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q6-4(73.9mm,85.911mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q6-5(73.25mm,85.911mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q6-7(72.95mm,84.986mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.191mm < 0.254mm) Between Pad R16-2(70.39mm,12.915mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.254mm) Between Pad R17-1(73.065mm,4.825mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.072mm < 0.254mm) Between Pad R17-2(71.515mm,4.825mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad R21-2(66.377mm,11.404mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.231mm < 0.254mm) Between Pad R31-2(96.474mm,37.155mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.214mm < 0.254mm) Between Pad R3-2(51.557mm,33.59mm) on Component Side And Via (55mm,30mm) from
Minimum Solder Mask Sliver Constraint: (0.214mm < 0.254mm) Between Pad R3-2(51.557mm,33.59mm) on Component Side And Via (55mm,32mm) from
Minimum Solder Mask Sliver Constraint: (0.253mm < 0.254mm) Between Pad R35-1(74.74mm,33mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.253mm < 0.254mm) Between Pad R35-2(73.19mm,33mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.126mm < 0.254mm) Between Pad R41-1(87.304mm,98mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.122mm < 0.254mm) Between Pad R48-1(96.5mm,63.2mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.242mm < 0.254mm) Between Pad R55-1(118mm,90mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.18mm < 0.254mm) Between Pad R61-1(118mm,74.167mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad R64-1(24.89mm,98mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U10-6(83.206mm,41.33mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U10-8(83.056mm,42.08mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(56.974mm,7.35mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-1(56.974mm,7.35mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-2(56.974mm,6.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U12-6(83.206mm,45.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U12-8(83.056mm,46.5mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-3(58.414mm,6.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-3(58.414mm,6.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U13-6(88.054mm,89.87mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U13-8(87.304mm,89.72mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-4(58.414mm,7.35mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U14-6(55.664mm,89.87mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U14-8(54.914mm,89.72mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U15-6(83.206mm,61.95mm) on Component Side And Pad

Minimum Solder Mask Sliver (Gap=0.254mm) (All), (All)
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U15-8(83.056mm,62.7mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U16-6(83.206mm,54.95mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U16-8(83.056mm,55.7mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U17-6(40.946mm,84.607mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U17-8(40.196mm,84.457mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U18-6(110mm,41.33mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U18-8(109.85mm,42.08mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U19-6(110mm,89mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U19-8(109.85mm,89.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U20-6(83.206mm,76.625mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U20-8(83.056mm,77.375mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U21-6(10.464mm,89.87mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U21-8(9.714mm,89.72mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U22-6(110mm,73.605mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U22-8(109.85mm,74.355mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U23-6(25.664mm,89.87mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U23-8(24.914mm,89.72mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.098mm < 0.254mm) Between Pad U24-6(110mm,57.688mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.048mm < 0.254mm) Between Pad U24-8(109.85mm,58.438mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U3-1(33.339mm,5.775mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U3-2(33.339mm,4.825mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(46.575mm,7.85mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(46.575mm,6.9mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-1(12.25mm,6.7mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U7-2(12.25mm,5.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-1(22.582mm,6.7mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U8-2(22.582mm,5.75mm) on Component Side And Pad
Minimum Solder Mask Sliver Constraint: (0.188mm < 0.254mm) Between Via (46.04mm,11.03mm) from Component Side to Solder Side And Via
Minimum Solder Mask Sliver Constraint: (0.12mm < 0.254mm) Between Via (49.235mm,11.076mm) from Component Side to Solder Side And Via

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (107.65mm,42.68mm) on Top Overlay And Pad U18-1(108.2mm,42.33mm)
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (107.65mm,59.038mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (107.65mm,74.955mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (107.65mm,90.35mm) on Top Overlay And Pad U19-1(108.2mm,90mm) on
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (24.314mm,87.52mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (39.596mm,82.257mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (54.314mm,87.52mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.188mm < 0.254mm) Between Arc (56.466mm,7.604mm) on Top Overlay And Pad U1-1(56.974mm,7.35mm)
Silk To Solder Mask Clearance Constraint: (0.141mm < 0.254mm) Between Arc (77.139mm,38.684mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (80.856mm,42.68mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (80.856mm,47.1mm) on Top Overlay And Pad U12-1(81.406mm,46.75mm)
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (80.856mm,56.3mm) on Top Overlay And Pad U16-1(81.406mm,55.95mm)
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (80.856mm,63.3mm) on Top Overlay And Pad U15-1(81.406mm,62.95mm)
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (80.856mm,77.975mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (86.704mm,87.52mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Arc (9.114mm,87.52mm) on Top Overlay And Pad U21-1(9.464mm,88.07mm)
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad 3V3-1(109.1mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad 3V3-1(109.1mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad 3V3-1(109.1mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad 3V3-1(110.65mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad 3V3-1(110.65mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad 3V3-1(110.65mm,96.151mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad AUX FUSED-1(48.185mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad AUX FUSED-1(48.185mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad AUX FUSED-1(48.185mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad AUX FUSED-1(49.735mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad AUX FUSED-1(49.735mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad AUX FUSED-1(49.735mm,77.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C18-1(66mm,60.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C18-1(66mm,60.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C18-2(66mm,54.225mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C18-2(66mm,54.225mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad C20-2(77.175mm,15.75mm) on Component Side And Text "U6"
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad C2-1(55.164mm,7.35mm) on Component Side And Text "C2"
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.254mm) Between Pad C22-1(68.137mm,10.173mm) on Component Side And Text "R18"
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.254mm) Between Pad C22-2(68.137mm,8.823mm) on Component Side And Text "R20"
Silk To Solder Mask Clearance Constraint: (0.217mm < 0.254mm) Between Pad C25-2(10.464mm,6.15mm) on Component Side And Text "C25"
Silk To Solder Mask Clearance Constraint: (0.208mm < 0.254mm) Between Pad C26-2(20.75mm,6.15mm) on Component Side And Text "C26"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C29-1(57.826mm,60.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C29-1(57.826mm,60.125mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C29-2(57.826mm,54.225mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C29-2(57.826mm,54.225mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C30-1(47.749mm,17.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C30-1(47.749mm,17.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C30-2(47.749mm,12mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C30-2(47.749mm,12mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C3-1(32.427mm,17.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C3-1(32.427mm,17.9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C3-2(32.427mm,12mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C3-2(32.427mm,12mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad C33-1(79.902mm,45.75mm) on Component Side And Text "C33"
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad C33-2(79.902mm,44.4mm) on Component Side And Text "C33"

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad C38-2(79.839mm,53.6mm) on Component Side And Text "REAR CAM"
Silk To Solder Mask Clearance Constraint: (0.118mm < 0.254mm) Between Pad C8-1(93.894mm,4.375mm) on Component Side And Text "C8"
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C9-1(33mm,59.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C9-1(33mm,59.65mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C9-2(33mm,53.75mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C9-2(33mm,53.75mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D4-1(73.773mm,88.595mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D4-1(73.773mm,88.595mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D4-2(69.773mm,88.595mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.254mm) Between Pad D4-2(69.773mm,88.595mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-3(18.957mm,31.6mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-4(32.427mm,31.6mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-3(18.957mm,65.849mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-4(32.427mm,65.849mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad GND-1(20.75mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad GND-1(20.75mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad GND-1(20.75mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad GND-1(22.3mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad GND-1(22.3mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad GND-1(22.3mm,13.391mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad LDO 3V-1(55.164mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad LDO 3V-1(55.164mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad LDO 3V-1(55.164mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad LDO 3V-1(56.714mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad LDO 3V-1(56.714mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad LDO 3V-1(56.714mm,3.397mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED10-2(97.597mm,54.15mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED11-2(36.5mm,98.952mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED1-2(102.026mm,93.28mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED12-2(119mm,45.75mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED13-2(119mm,93.17mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED14-2(97.75mm,81.05mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED15-2(6.768mm,98.925mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED16-2(118.925mm,77.275mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED17-2(21.75mm,98.925mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED18-2(118.925mm,61.675mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED2-2(100.7mm,93.28mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED3-2(97.674mm,35.5mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED4-2(92.48mm,31.75mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED5-2(97.7mm,48.25mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED6-2(84.25mm,98.952mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED7-2(69.473mm,84.061mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED8-2(51.75mm,98.952mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.254mm) Between Pad LED9-2(97.7mm,66.25mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(92.3mm,21mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(92.3mm,9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(88.7mm,9mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(88.7mm,21mm) on Component Side And Track
Silk To Solder Mask Clearance Constraint: (0.051mm < 0.254mm) Between Pad P4-2(5mm,67.5mm) on Multi-Layer And Text "AUX BAT"

+12V" (10.598mm,64.651mm) on Bottom Overlay [Bottom Overlay] to [Bottom Solder] clearance [0.051mm]

[illegible][illegible]

[illegible][illegible]

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad U24-9(109.1mm,57.938mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad UNPROT 12V-1(109.7mm,31.5mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad UNPROT 12V-1(109.7mm,31.5mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad UNPROT 12V-1(109.7mm,31.5mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad UNPROT 12V-1(111.25mm,31.5mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.148mm < 0.254mm) Between Pad UNPROT 12V-1(111.25mm,31.5mm) on Component Side And Track

Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad UNPROT 12V-1(111.25mm,31.5mm) on Component Side And Track

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (56.648mm,37.62mm) on Top Overlay And Text "Q2" (55.526mm,36.787mm) on Top

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "AUX BAT

+12V" (10.598mm,64.651mm) on Bottom Overlay And Text "GND" (7.378mm,68.715mm) on Bottom Overlay Silk Text to :

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C13" (44.425mm,12.179mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C13" (44.425mm,12.179mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.156mm < 0.254mm) Between Text "C22" (67.684mm,13.281mm) on Top Overlay And Text "R16"

Silk To Silk Clearance Constraint: (0.16mm < 0.254mm) Between Text "C22" (67.684mm,13.281mm) on Top Overlay And Text "R18" (68.79mm,11.762mm)

Silk To Silk Clearance Constraint: (0.211mm < 0.254mm) Between Text "CHARGER" (110.913mm,33.827mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.191mm < 0.254mm) Between Text "CHARGER" (110.913mm,33.827mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.206mm < 0.254mm) Between Text "CHARGER" (110.913mm,33.827mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.242mm < 0.254mm) Between Text "DC-DC IN" (3.02mm,51.942mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.24mm < 0.254mm) Between Text "DC-DC IN" (3.02mm,51.942mm) on Top Overlay And Track

Silk To Silk Clearance Constraint: (0.107mm < 0.254mm) Between Text "FRONT

SOLAR" (111mm,80.102mm) on Top Overlay And Track (111.07mm,82.67mm)(111.07mm,93.745mm) on Top Overlay Silk

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.097mm < 0.254mm) Between Text "FRONT

SOLAR" (111mm,80.102mm) on Top Overlay And Track (111.07mm,82.67mm)(116.37mm,82.67mm) on Top Overlay Silk

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.207mm < 0.254mm) Between Text "GND" (20.371mm,14.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.23mm < 0.254mm) Between Text "LED10" (99.577mm,54.379mm) on Top Overlay And Text "R51"
Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "LED11" (32.227mm,98.552mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.157mm < 0.254mm) Between Text "LED15" (2.108mm,94.119mm) on Top Overlay And Text "R62"
Silk To Silk Clearance Constraint: (0.216mm < 0.254mm) Between Text "LED17" (17.101mm,98.552mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.034mm < 0.254mm) Between Text "LED18" (118.541mm,66.141mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "LED3" (99.961mm,35.922mm) on Top Overlay And Text "R32"
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "LED4" (88.52mm,31.35mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.166mm < 0.254mm) Between Text "LED5" (99.577mm,48.638mm) on Top Overlay And Text "R40"
Silk To Silk Clearance Constraint: (0.191mm < 0.254mm) Between Text "LED6" (80.336mm,98.552mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.118mm < 0.254mm) Between Text "LED9" (99.577mm,66.764mm) on Top Overlay And Text "R49"
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "P11" (111.07mm,46.697mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "P11" (111.07mm,46.697mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.199mm < 0.254mm) Between Text "P12" (111.07mm,94.146mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.199mm < 0.254mm) Between Text "P12" (111.07mm,94.146mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.123mm < 0.254mm) Between Text "P14" (3.895mm,95.405mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.17mm < 0.254mm) Between Text "P17" (111.07mm,62.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.17mm < 0.254mm) Between Text "P17" (111.07mm,62.45mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P4" (6.706mm,75.17mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "P4" (6.706mm,75.17mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "P5" (84.97mm,49.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "P5" (84.97mm,49.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.214mm < 0.254mm) Between Text "P7" (65.925mm,96.775mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.203mm < 0.254mm) Between Text "P7" (65.925mm,96.775mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "P9" (85.144mm,67.144mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.092mm < 0.254mm) Between Text "P9" (85.144mm,67.144mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.247mm < 0.254mm) Between Text "PROT 12V" (1.25mm,81.141mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.239mm < 0.254mm) Between Text "PROT 12V" (1.25mm,81.141mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.242mm < 0.254mm) Between Text "PROT 12V" (1.25mm,81.141mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.226mm < 0.254mm) Between Text "R17" (68.51mm,4.471mm) on Top Overlay And Text "R19" (68.51mm,3.295mm)
Silk To Silk Clearance Constraint: (0.216mm < 0.254mm) Between Text "R42" (81.223mm,96.675mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.216mm < 0.254mm) Between Text "R42" (81.223mm,96.675mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.198mm < 0.254mm) Between Text "REAR CAM" (78.289mm,51.975mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "REAR CAM" (78.289mm,51.975mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.073mm < 0.254mm) Between Text "TELEMETRY" (77.614mm,65.665mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.16mm < 0.254mm) Between Text "TELEMETRY" (77.614mm,65.665mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.173mm < 0.254mm) Between Text "TP5" (84.764mm,10.148mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.233mm < 0.254mm) Between Text "U10" (81.423mm,39.298mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "U12" (81.283mm,47.444mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.092mm < 0.254mm) Between Text "U14" (52.047mm,88.531mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.189mm < 0.254mm) Between Text "U16" (81.423mm,56.664mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.178mm < 0.254mm) Between Text "U19" (108.661mm,92.703mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.164mm < 0.254mm) Between Text "U20" (81.391mm,78.314mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "U22" (108.055mm,75.353mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U24" (108.06mm,59.433mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.236mm < 0.254mm) Between Text "UNPROT 12V" (106.73mm,32.625mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.223mm < 0.254mm) Between Text "UNPROT 12V" (106.73mm,32.625mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.233mm < 0.254mm) Between Text "UNPROT
SPARE 1" (110.791mm,64.152mm) on Top Overlay And Track (111.07mm,66.837mm)(111.07mm,77.911mm) on Top Over

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.213mm < 0.254mm) Between Text "UNPROT

SPARE 1" (110.791mm,64.152mm) on Top Overlay And Track (111.07mm,66.837mm)(116.37mm,66.837mm) on Top Over

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.117mm < 0.254mm) Between Text "UNPROT

SPARE 2" (110.913mm,48.415mm) on Top Overlay And Track (111.07mm,51.004mm)(111.07mm,62.078mm) on Top Over

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.117mm < 0.254mm) Between Text "UNPROT

SPARE 2" (110.913mm,48.415mm) on Top Overlay And Track (111.07mm,51.004mm)(116.37mm,51.004mm) on Top Over

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (0.256mm < 0.3mm) Between Board Edge And Text "CHARGER" (110.913mm,33.827mm) on Top Overlay

Board Outline Clearance(Outline Edge): (0.169mm < 0.3mm) Between Board Edge And Text "FRONT

SOLAR" (111mm,80.102mm) on Top Overlay

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (0.256mm < 0.3mm) Between Board Edge And Text "UNPROT

SPARE 2" (110.913mm,48.415mm) on Top Overlay