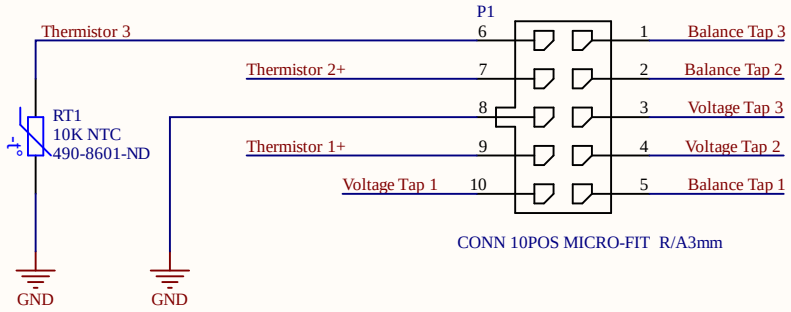
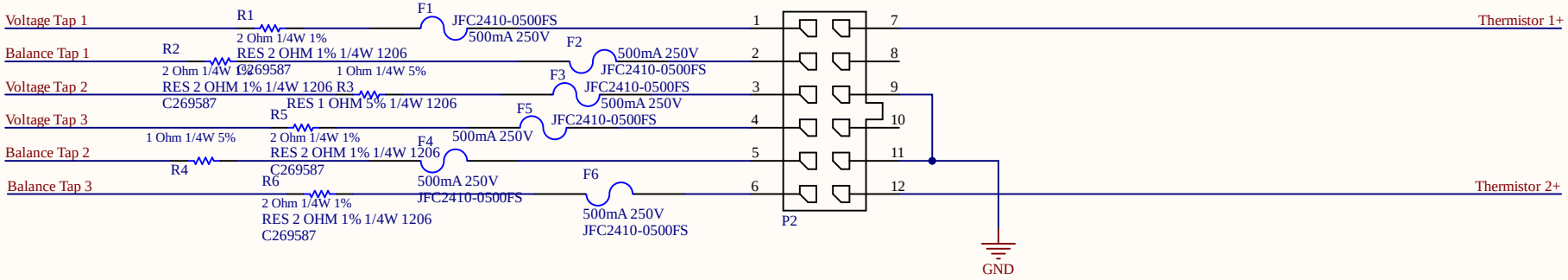


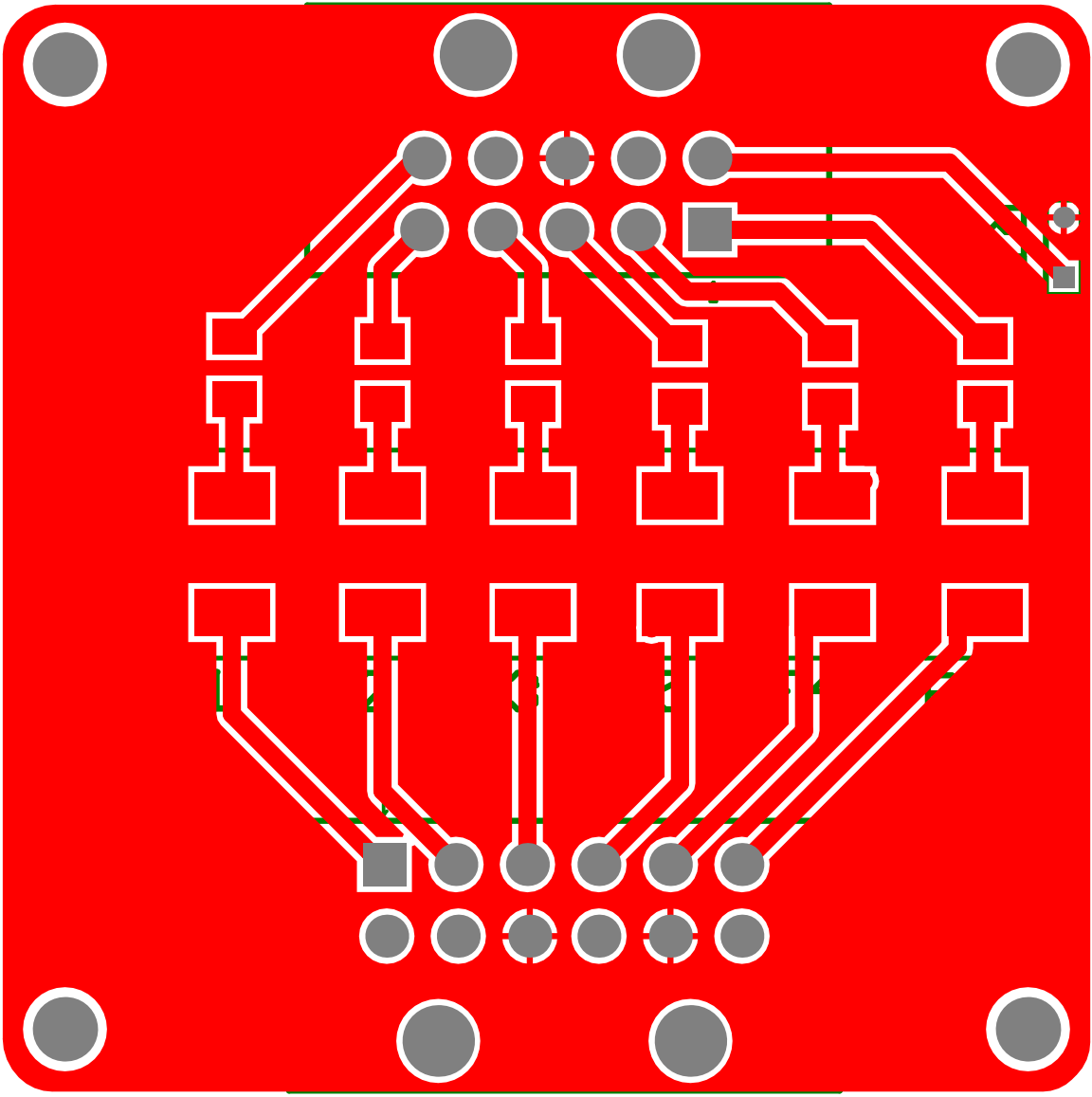


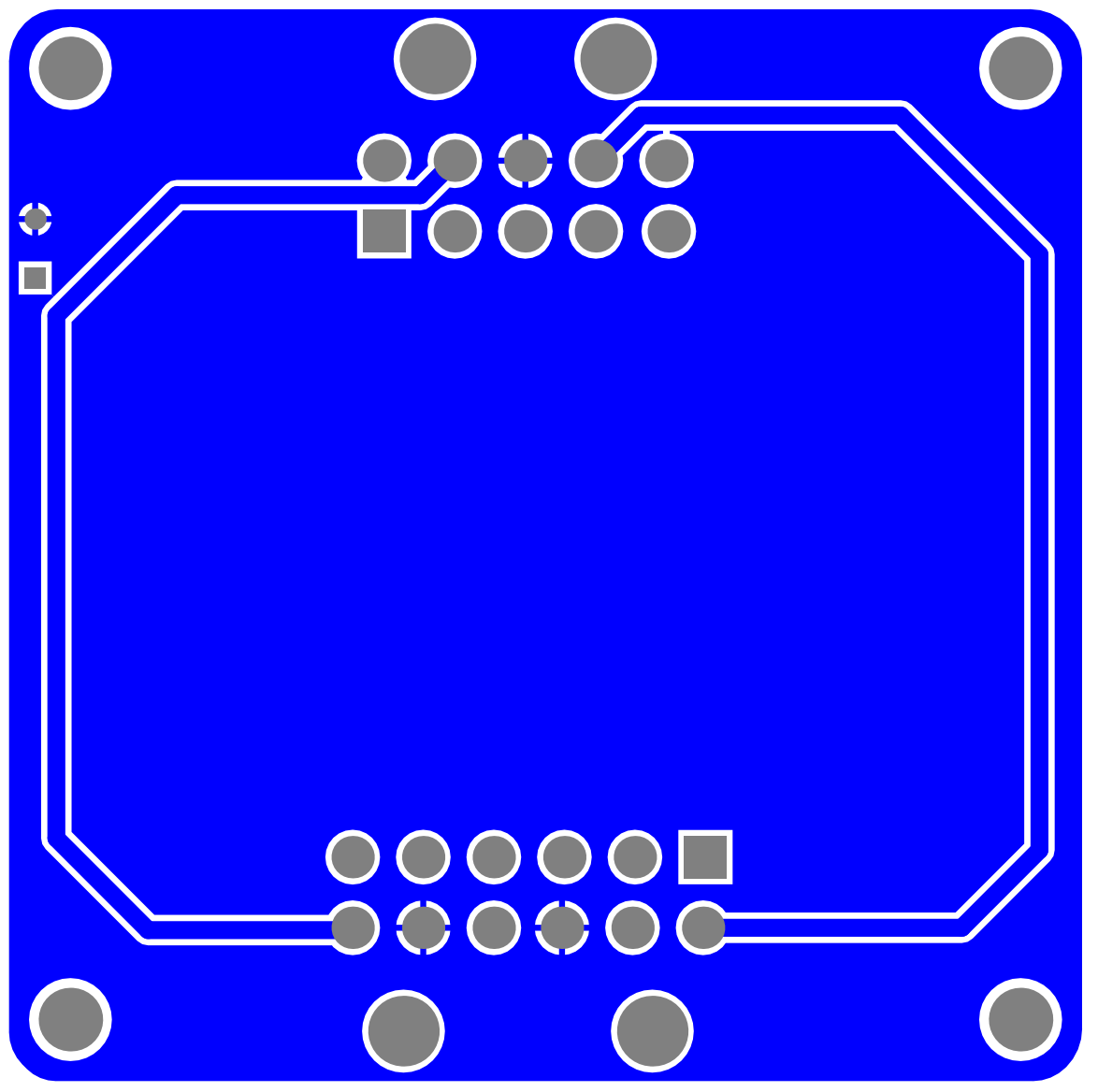
Project: *MSXIV_BatteryModuleConnectorBoard.Pr*		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Aashmika Mali		
Size: Letter	Revision: 2.0	
Date: 2019-12-01	Sheet * of *	Website: uwmidsun.com

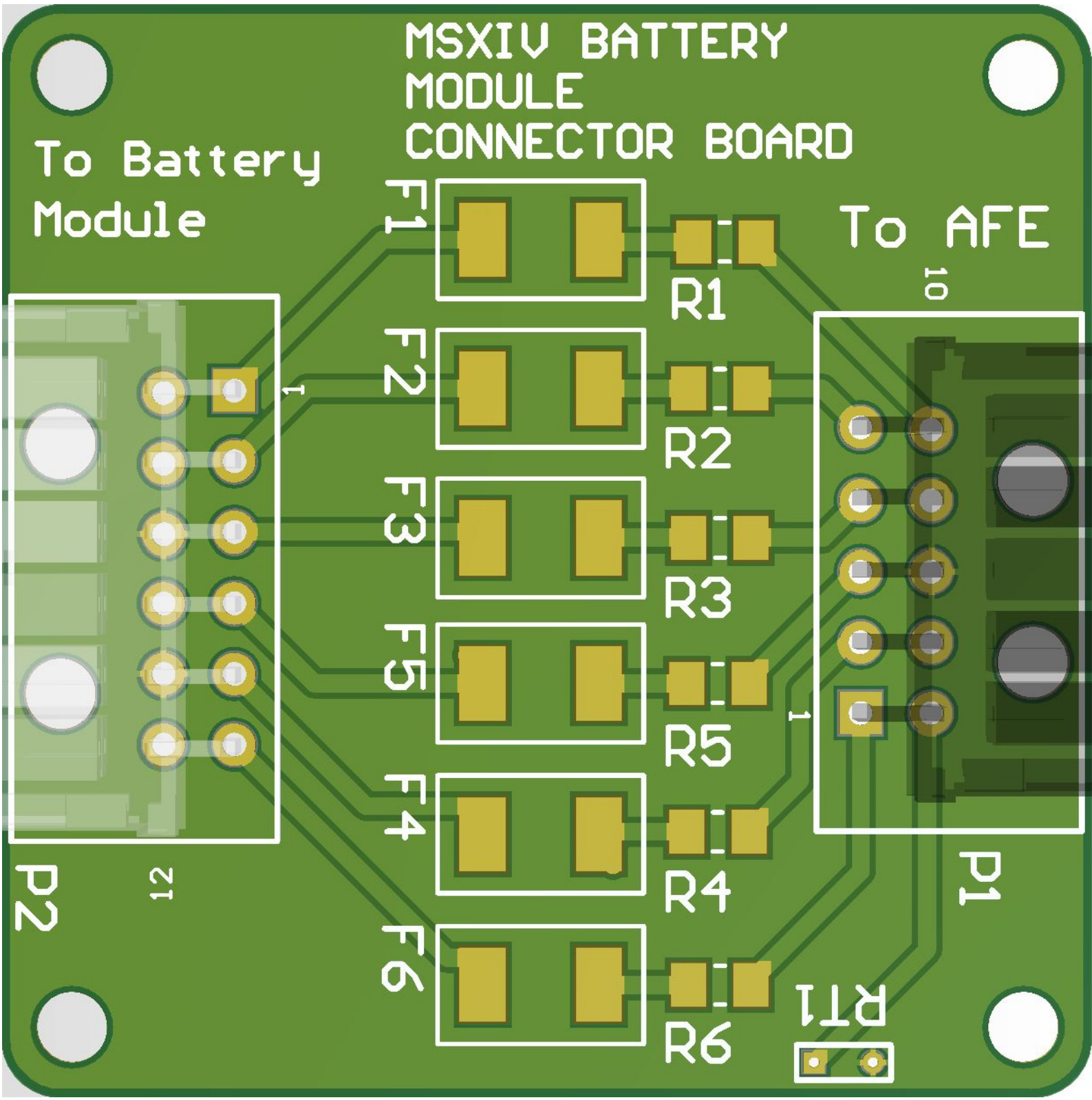
Bill of Materials

Project:	KIV_BatteryModuleConnectorBoard.PrjPcb
Revision:	2.0
Project Lead:	Aashmika Mali
Generated On:	2019-12-01 10:27 PM
Production Quantity:	1
Currency	USD
Total Parts Count:	15

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
FUSE 500MA LCSC	F1, F2, F3, F4, F5, F6	Shenzen JDT Fuse	JFC2410-0500FS	LCSC	C136360		6	
CONN 10POS MICRO-FIT R/A3mm	P1	Molex	430451000	Digi-Key	WM1817-ND		1	
CONN 12POS HEADER R/A 3MM	P2	Molex	430451200	Digi-Key	WM1818-ND		1	
RES 2 OHM 1% 1/4W 1206	R1, R2, R5, R6	TyoHM	RMC120621%N	LCSC	C269587		4	
RES 1 OHM 5% 1/4W 1206	R3, R4	TyoHM	RMC120615%N	LCSC	C325901		2	
NTC THERMISTOR 10K 1% BEAD	RT1			Digi-Key	490-8601-ND		1	
							Total:	$ -






MSXIV BATTERY
MODULE
CONNECTOR BOARD
To Battery
Module
To AFE
F1
F2
F3
F5
F4
F6
R1
R2
R3
R5
R4
R6
RT1
P1
P2
1
10
1
12

Design Rules Verification Report

Filename : C:\Users\Midnight Sun\Documents\Midnight Sun\hardware\MSXIV_BatteryM

Warnings 0
Rule Violations 17

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.762mm) (Preferred=0.508mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	8
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	6
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	17

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.184mm < 0.254mm) Between Pad P1-6(30.06mm,39.48mm) on Multi-Layer And Track

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(3mm,3mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(3mm,43.4mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(43.4mm,3mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad Free-(43.4mm,43.4mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P1-(20.22mm,43.8mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P1-(27.9mm,43.8mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P2-(18.66mm,2.51mm) on Multi-Layer Actual Hole Size = 3mm
Hole Size Constraint: (3mm > 2.54mm) Pad P2-(29.24mm,2.51mm) on Multi-Layer Actual Hole Size = 3mm

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Pad RT1-1(44.9mm,34.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad RT1-2(44.9mm,37mm) on Multi-Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.068mm < 0.254mm) Between Text "1" (16.5mm,12.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "1" (30.06mm,33.48mm) on Top Overlay And Track