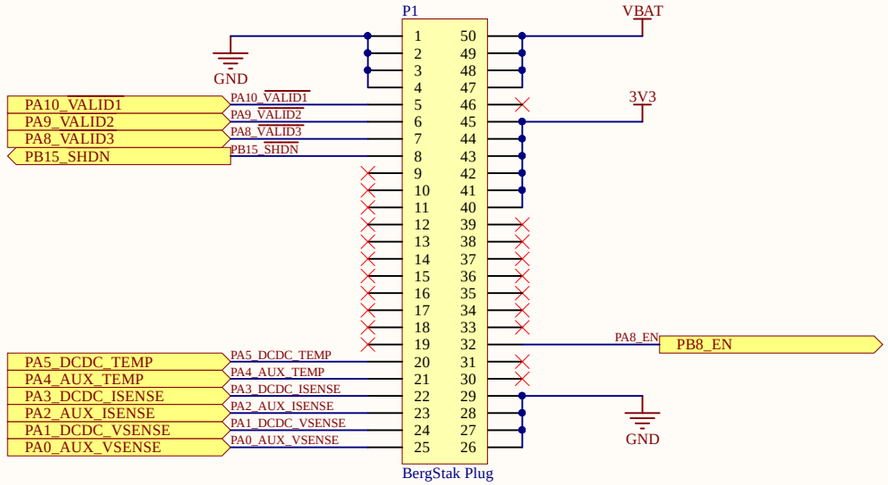
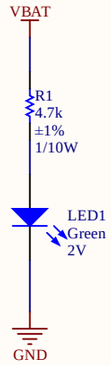
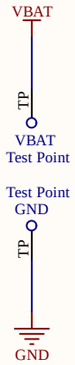
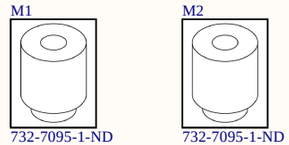
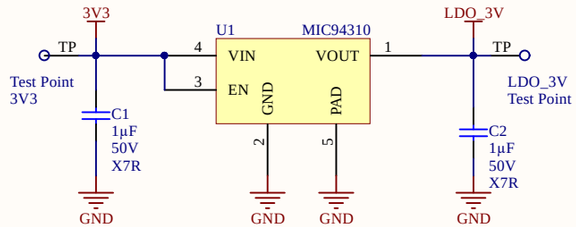


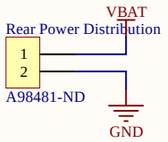
<- 3mA Max.

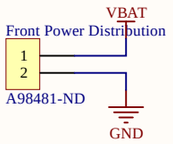




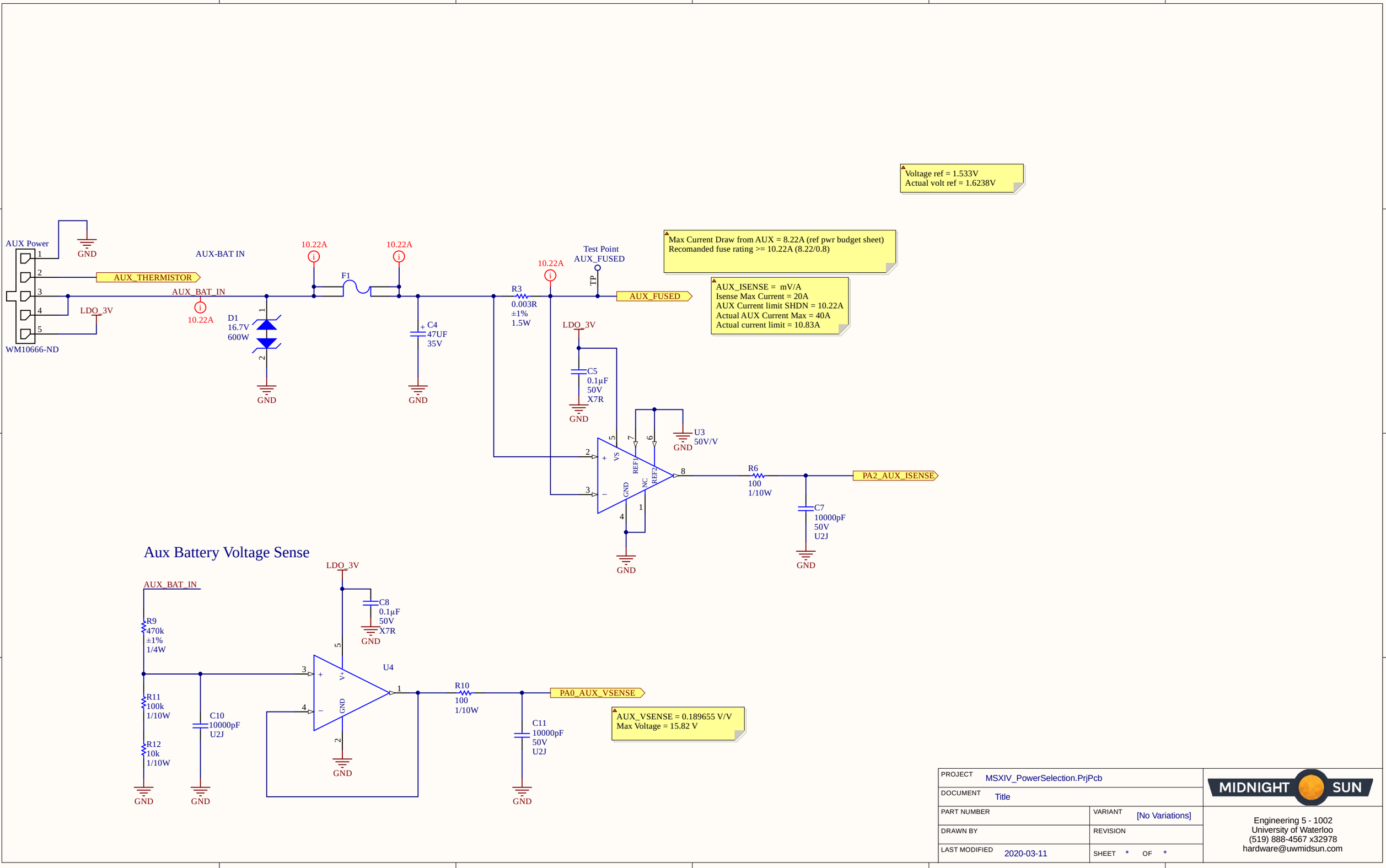








PROJECT	MSXIV_PowerSelection.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
PART NUMBER	VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
DRAWN BY	REVISION	
LAST MODIFIED 2020-03-11	SHEET * OF *	



PROJECT	MSXIV_PowerSelection.PrjPcb
DOCUMENT	Title
PART NUMBER	VARIANT [No Variations]
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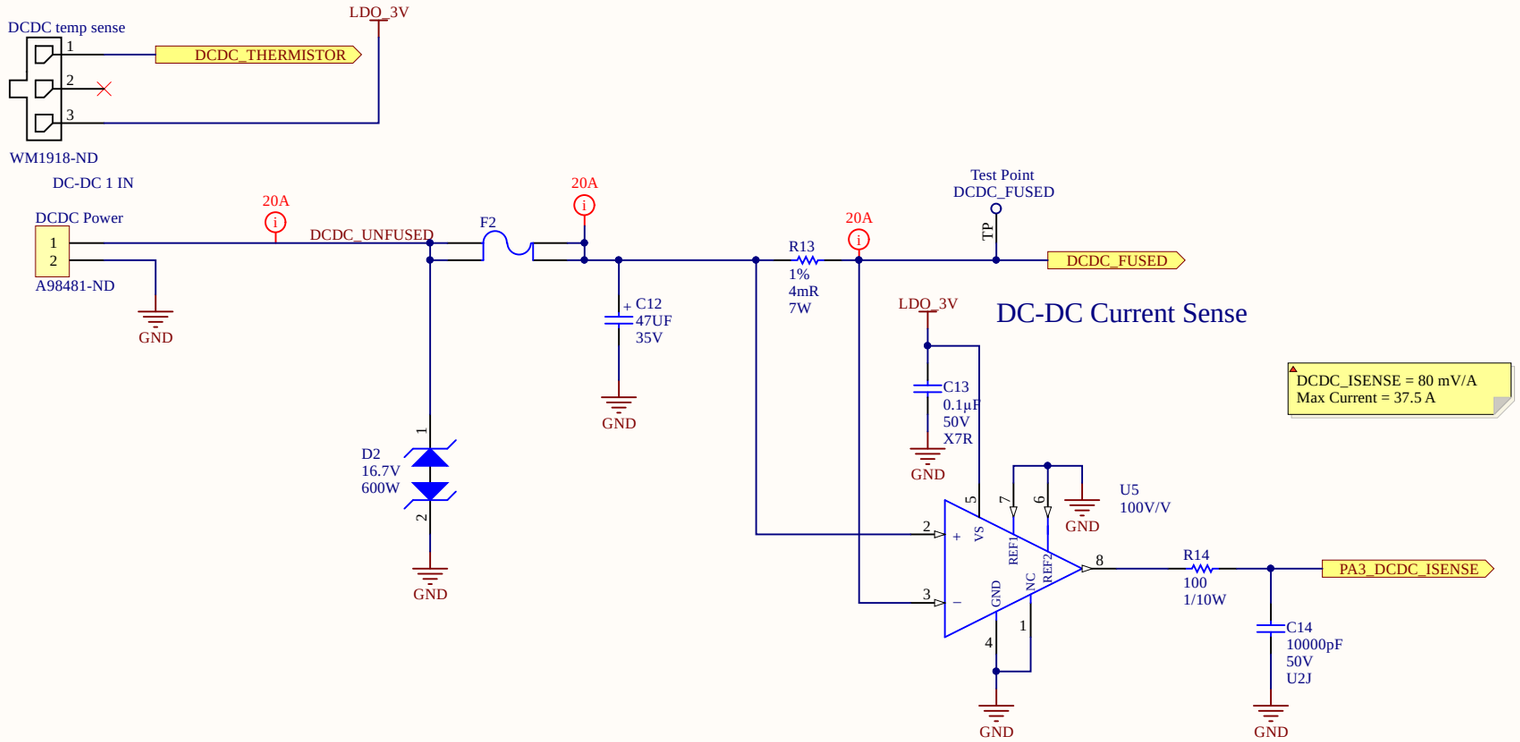
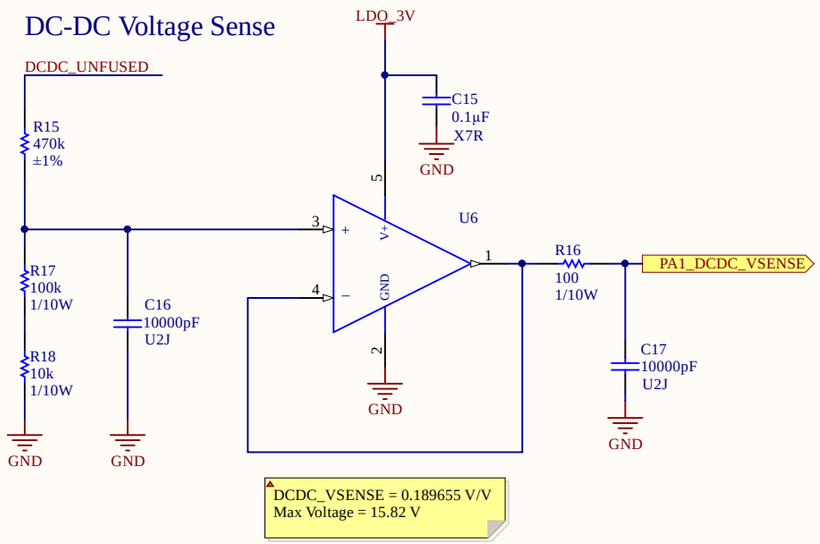
MIDNIGHT SUN

Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com





PROJECT	MSXIV_PowerSelection.PrjPcb		MIDNIGHT SUN
DOCUMENT	Title		
PART NUMBER		VARIANT [No Variations]	Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com
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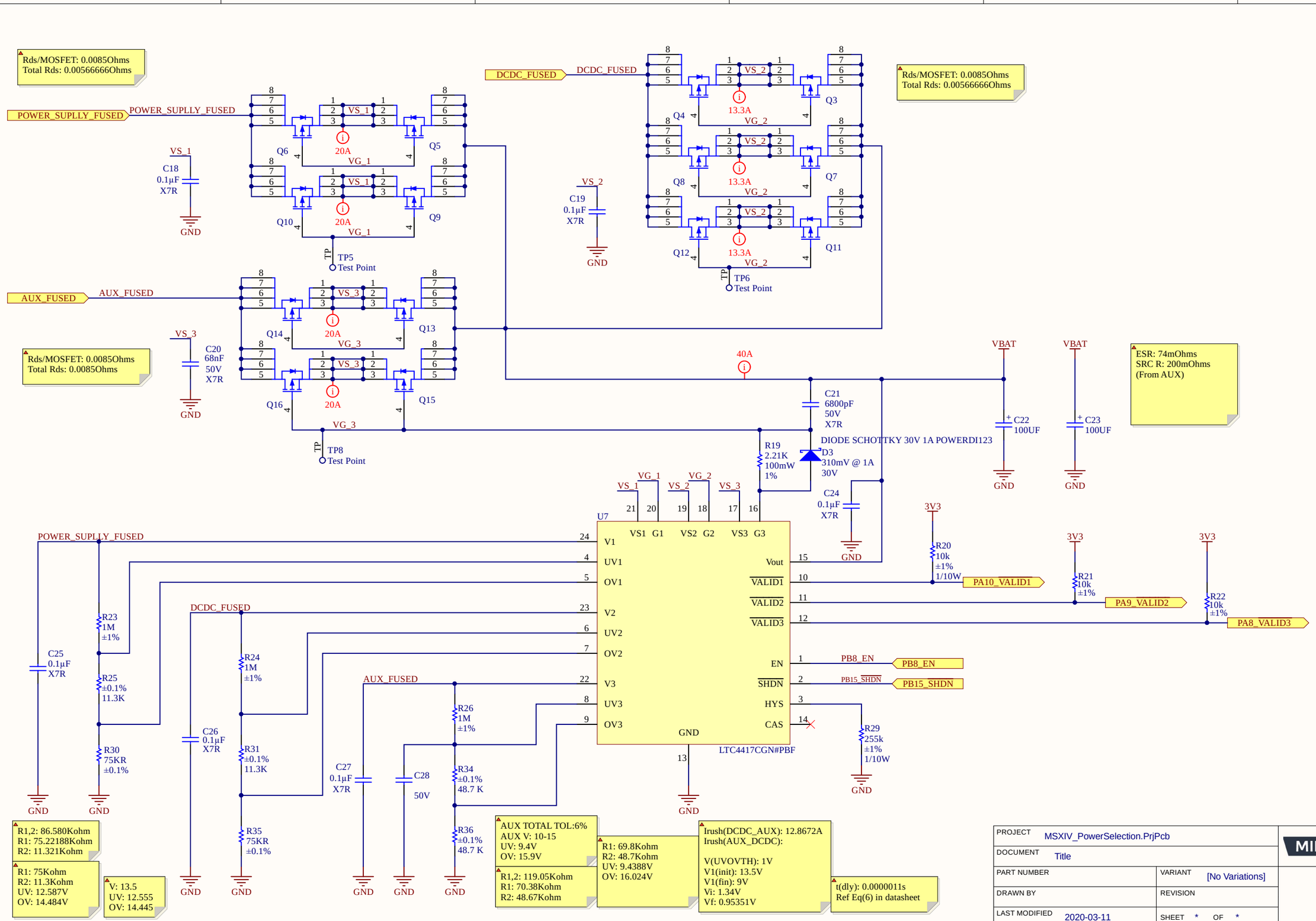
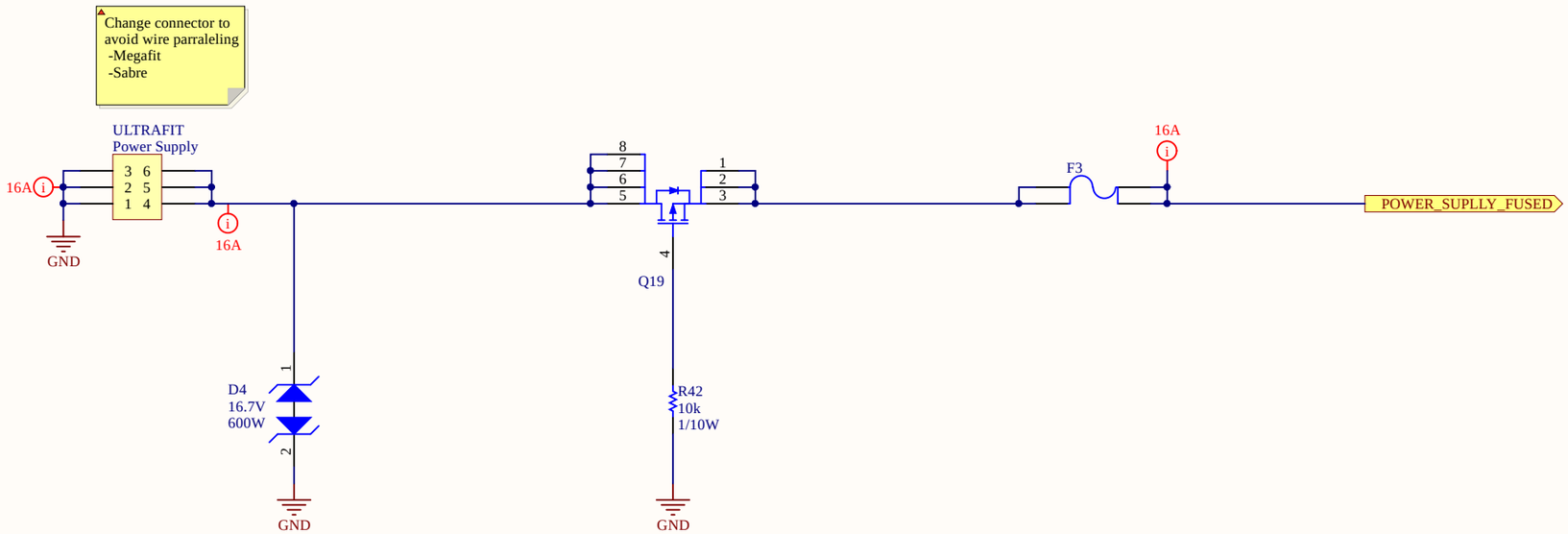
LAST MODIFIED	2020-03-11	SHEET * OF *	


Rds/MOSFET: 0.0085Ohms
Total Rds: 0.00566666Ohms
POWER_SUPLLY_FUSED
POWER_SUPLLY_FUSED
VS_1
C18
0.1µF
X7R
GND
Q6
Q5
Q10
Q9
VS_1
VG_1
20A
TP5
Test Point
DCDC_FUSED
DCDC_FUSED
Rds/MOSFET: 0.0085Ohms
Total Rds: 0.00566666Ohms
VS_2
C19
0.1µF
X7R
GND
Q3
Q4
Q7
Q8
Q11
Q12
VS_2
VG_2
13.3A
TP6
Test Point
AUX_FUSED
AUX_FUSED
Rds/MOSFET: 0.0085Ohms
Total Rds: 0.0085Ohms
VS_3
C20
68nF
50V
X7R
GND
Q14
Q13
Q16
Q15
VS_3
VG_3
20A
TP8
Test Point
40A
C21
6800pF
50V
X7R
R19
2.21K
100mW
1%
DIODE SCHOTTKY 30V 1A POWERDI123
D3
310mV @ 1A
30V
C24
0.1µF
X7R
GND
VBAT
C22
100UF
GND
VBAT
C23
100UF
GND
ESR: 74mOhms
SRC R: 200mOhms
(From AUX)
U7
VS1 G1
VS2 G2
VS3 G3
V1
UV1
OV1
V2
UV2
OV2
V3
UV3
OV3
GND
Vout
VALID1
VALID2
VALID3
EN
SHDN
HYS
CAS
LTC4417CGN#PBF
3V3
R20
10k
±1%
1/10W
PA10_VALID1
3V3
R21
10k
±1%
PA9_VALID2
3V3
R22
10k
±1%
PA8_VALID3
PB8_EN
PB8_EN
PB15_SHDN
PB15_SHDN
R29
255k
±1%
1/10W
GND
POWER_SUPLLY_FUSED
R23
1M
±1%
R25
±0.1%
11.3K
R30
75KR
±0.1%
GND
GND
C25
0.1µF
X7R
DCDC_FUSED
C26
0.1µF
X7R
R24
1M
±1%
R31
±0.1%
11.3K
R35
75KR
±0.1%
GND
GND
AUX_FUSED
C27
0.1µF
X7R
C28
50V
R26
1M
±1%
R34
±0.1%
48.7 K
R36
±0.1%
48.7 K
GND
GND
GND
R1,2: 86.580Kohm
R1: 75.22188Kohm
R2: 11.321Kohm
R1: 75Kohm
R2: 11.3Kohm
UV: 12.587V
OV: 14.484V
V: 13.5
UV: 12.555
OV: 14.445
AUX TOTAL TOL:6%
AUX V: 10-15
UV: 9.4V
OV: 15.9V
R1,2: 119.05Kohm
R1: 70.38Kohm
R2: 48.67Kohm
R1: 69.8Kohm
R2: 48.7Kohm
UV: 9.4388V
OV: 16.024V
Irush(DCDC_AUX): 12.8672A
Irush(AUX_DCDC):
V(UVOVTH): 1V
V1(init): 13.5V
V1(fin): 9V
Vi: 1.34V
Vf: 0.95351V
t(dly): 0.0000011s
Ref Eq(6) in datasheet
PROJECT MSXIV_PowerSelection.PrjPcb
DOCUMENT Title
PART NUMBER
VARIANT [No Variations]
DRAWN BY
REVISION
LAST MODIFIED 2020-03-11
SHEET * OF *
MIDNIGHT SUN
Engineering 5 - 1002
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com



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DOCUMENT	Title		
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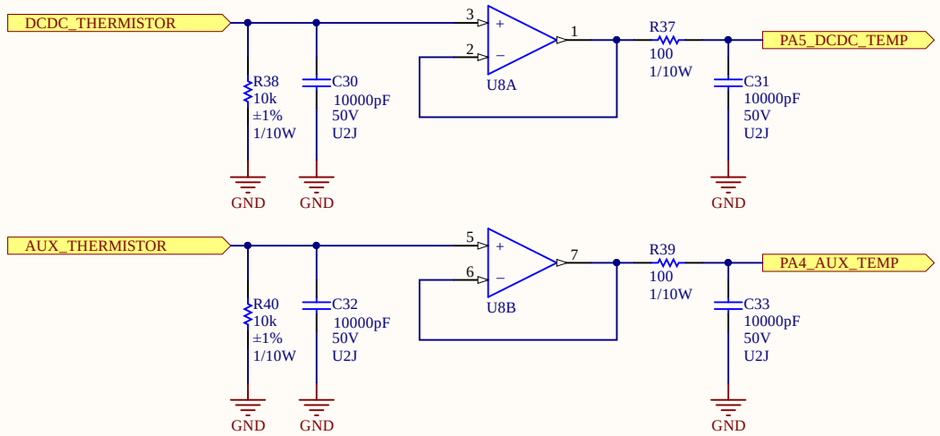
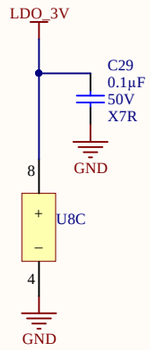
LAST MODIFIED	2020-03-11	SHEET * OF *	

Temperature Sense





Beaware that there will be two general purpose amp as dcdc and aux both uses this design, please make sure does this part belong in main schematic or stays here.

PROJECT	MSXIV_PowerSelection.PrjPcb	MIDNIGHT SUN
DOCUMENT	Title	
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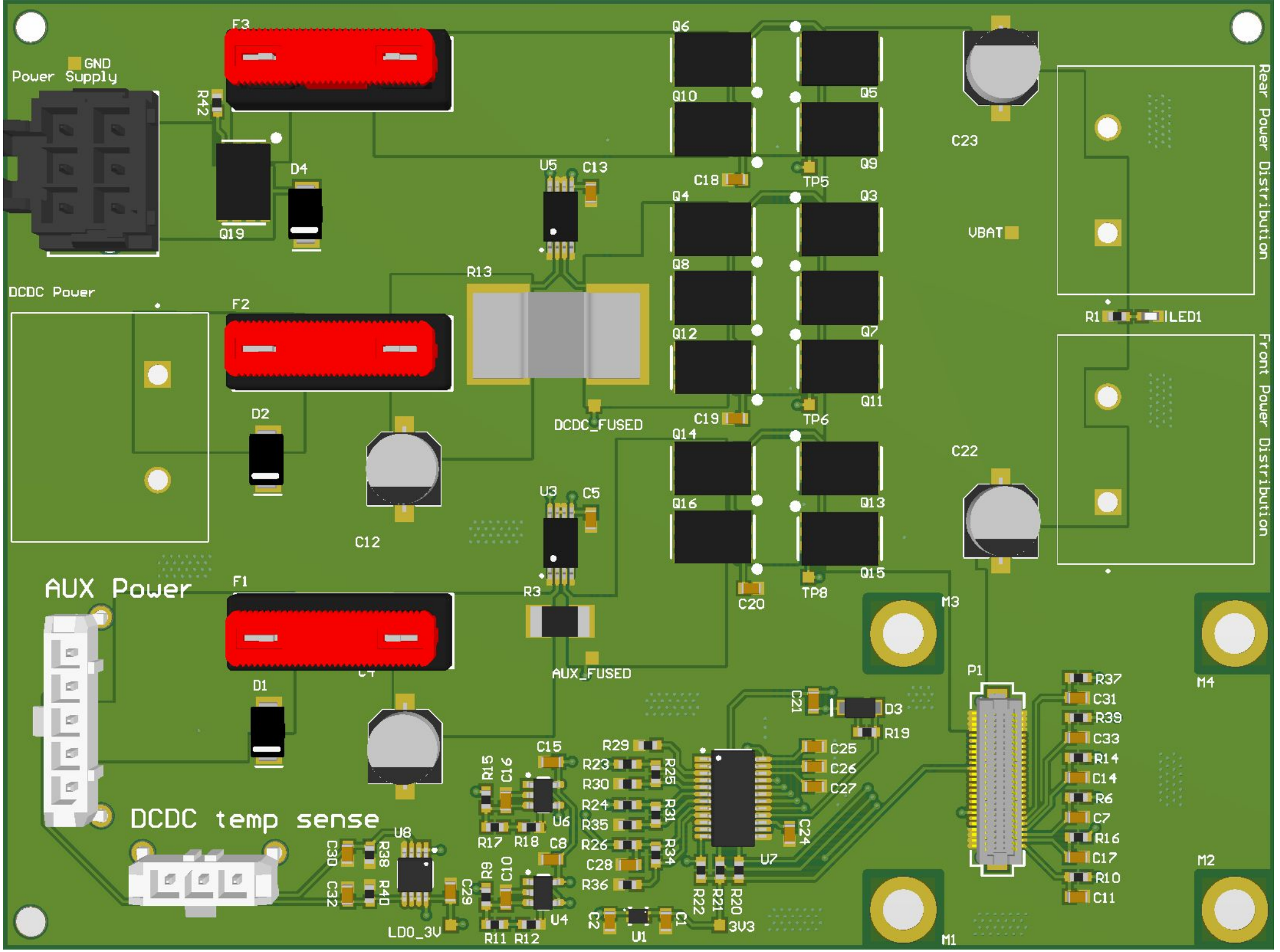
DRAWN BY	REVISION	
LAST MODIFIED 2020-03-11	SHEET * OF *	

Bill of Materials

Project:	MSXIV_PowerSelection.PrjPcb
Revision:	<Parameter ProjectRevision not found>
Project Lead:	<Parameter ProjectAuthor not found>
Generated On:	2020-03-11 12:38 AM
Production Quantity:	1
Currency	CAD
Total Parts Count:	102

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CONN 5POS MICROFIT SINGAL ROW	AUX Power	Molex	0436500527	Digi-Key	WM10666-ND	1.8	1	$ 1.80
CAP CER 1UF 50V 10% X7R 0603	C1, C2	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.34433	2	$ 0.69
CAP ALUM 47UF 20% 35V SMD	C4, C12	Panasonic	EEE-1VA470WP	Digi-Key	PCE3961CT-ND	0.5647	2	$ 1.13
CAP CER 0.1UF 50V 10% X7R 0603	C8, C13, C15, C18, C19, C24, C25, C26, C27	Kyocera AVX	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.09641	11	$ 1.06
CAP CER 10nF 50V 5% X7R 0603	, C10, C11, C14, C16, C17, C30, C31, C32, C3	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.30852	10	$ 3.09
CAP CER 0.068UF 10% 50V X7R 0603	C20	Murata	GCM188R71H683KA57D	Digi-Key	490-8027-1-ND	0.24792	1	$ 0.25
CAP CER 6800pF 50V 10% X7R 0603	C21	Samsung	CL10B682KB8SFNC	Digi-Key	1276-2103-1-ND		1	
CAP ALUM 100UF 20% 35V SMD	C22	Panasonic	EEE-1VA101XP	Digi-Key	PCE3951CT-ND	0.64734	1	$ 0.65
CAP CER 0.022UF 50V 10% X7R 0603	C28	Murata	GRM188R71H223KA01D	Digi-Key	490-1517-1-ND		1	
DIODE TVS 15VWM 24.4VC DO-214AA (SMB)	D1, D2, D4	Taiwan Semiconductor	SMBJ15CA	Digi-Key	SMBJ15CAFSCT-ND	0.67489	3	$ 2.02
DIODE SCHOTTKY 30V 1A POWERDI123	D3	Diodes	DFLS130L-7	Digi-Key	DFLS130LDICT-ND	0.60602	1	$ 0.61
CONN BARRIER STRIP 2CIRC 0.375"	ower, Front Power Distribution, Rear Power Di	BUCHANAN - TE CONNECTIVITY	6PCV-02-006	Digi-Key	A98481-ND	2.25	3	$ 6.74
CONN 3POS MICROFIT	DCDC temp sense	Molex	43650-0315	Digi-Key	WM1918-ND	1.42	1	$ 1.42
FUSE ATO FUSE HOLDER	F1, F2, F3	Keystone Electronics	3557-2	Digi-Key	36-3557-2-ND	1.42	3	$ 4.26
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.19282	1	$ 0.19
STANDOFF RND M2.5X0.45 STEEL 5MM	M1, M2, M3, M4	Wurth Electronics	9774050151R	Digi-Key	732-7095-1-ND	1.5	4	$ 6.01
CONN 50POS Bergstak Plug 0.02"	P1	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.98	1	$ 1.98
CONN 6POS ULTRA-FIT 0.138"	Power Supply	Molex	1722991106	Digi-Key	WM11778-ND	1.64	1	$ 1.64
MOSFET P-CH PWR56 40V 4.9MOHM	Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q1	ON Semiconductor	FDWS9508L_F085	Digi-Key	DWS9508L-F085OSCT-ND		15	
RES 4.7K OHM 1% 1/10W 0603	R1	Yageo Phycomp	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.13773	1	$ 0.14
RES 0.003 OHM 1% 1.5W 2010	R3	Stackpole Electronics	CSNL2010FT3L00	Digi-Key	CSNL2010FT3L00CT-ND	0.89526	1	$ 0.90
RES 100 OHM 1% 1/10W 0603	R6, R10, R14, R16, R37, R39	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13773	6	$ 0.83
RES 470K OHM 1% 1/4W 0603	R9, R15	Panasonic	ERJ-PA3F4703V	Digi-Key	P470KBYCT-ND	0.19282	2	$ 0.39
RES 100K OHM 5% 1/8W 0603	R11, R17	Yageo	RC0603JR-07100KL	Digi-Key	311-100KGRCT-ND	0.13773	2	$ 0.28
RES 10K OHM 1% 1/10W 0603	R12, R18, R20, R21, R22, R38, R40, R42	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13773	8	$ 1.10
RES 0.004 OHM 1% 7W 5931	R13	Yageo	PU5931FKMP70R004L	Digi-Key	YAG4096CT-ND	2.77	1	$ 2.77
RES 2.21K OHM 1% 1/10W 0603	R19	Yageo	AC0603FR-072K21L	Digi-Key	YAG3586CT-ND	0.13773	1	$ 0.14
RES 1M OHM 1% 1/10W 0603	R23, R24, R26	Yageo	RC0603FR-071ML	Digi-Key	311-1.00MHRCT-ND	0.13773	3	$ 0.41
RES SMD 11.3KOHM 0.1% 1/10W 0603	R25, R31	Panasonic	ERA-3AEB1132V	Digi-Key	P11.3KDBCT-ND	0.46829	2	$ 0.94
RES 255K OHM 1% 1/10W 0603	R29	Yageo	RC0603FR-07255KL	Digi-Key	311-255KHRCT-ND	0.13773	1	$ 0.14
RES SMD 75K OHM 0.1% 1/10W 0603	R30, R35	Panasonic	ERA-3AEB753V	Digi-Key	P75KDBCT-ND	0.48206	2	$ 0.96
RES SMD 48.7KOHM 0.1% 1/10W 0603	R34, R36	Panasonic	ERA-3AEB4871V	Digi-Key	P4.87KDBCT-ND	0.46829	2	$ 0.94
IC REG LDO 3V 0.2A 4-TDFN	U1	Microchip	MIC94310-PYMT-TR	Digi-Key	576-4761-1-ND	0.38565	1	$ 0.39
IC CURRENT AMPLIFIER INA240 8-TSSOP	U3	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.83	1	$ 3.83
COP AMP GEN PURPOSE RR 10MHZ SOT-23-5	U4, U6	Texas Instruments	TLV316QDBVRQ1	Digi-Key	296-45323-1-ND	1.28	2	$ 2.56
IC CURRENT AMPLIFIER INA240 8-TSSOP	U5	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.83	1	$ 3.83
COR CONTROLLER SOURCE SELECT 24SSO	U7	Analog Devices / Linear	LTC4417CGN#PBF	Digi-Key	LTC4417CGN#PBF-ND	10.8	1	$ 10.80
IC OP AMP DUAL GP RR 10MHZ 8-VSSOP	U8	Texas Instruments	OPA2197IDGKR	Digi-Key	296-47349-1-ND	3.22	1	$ 3.22
							Total:	$ 68.07


Power Supply
GND
F3
R42
Q19
D4
U5
C13
C18
Q6
Q10
Q5
Q9
TP5
C23
VBAT
Rear Power Distribution
R1
LED1
Front Power Distribution
DCDC Power
F2
R13
Q4
Q3
Q8
Q7
Q12
Q11
TP6
C19
D2
C12
DCDC_FUSED
C22
U3
C5
Q14
Q13
Q16
Q15
C20
TP8
R3
AUX Power
F1
AUX_FUSED
M3
M4
P1
D1
C21
D3
R19
C25
C26
C27
C24
U7
R37
C31
R39
C33
R14
C14
R6
C7
R16
C17
R10
C11
M2
DCDC temp sense
U8
C30
C32
R38
R40
C29
LDO_3V
C15
R15
C16
U6
R17
R18
C8
R29
R23
R30
R24
R35
R26
C28
R36
R25
R31
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U1
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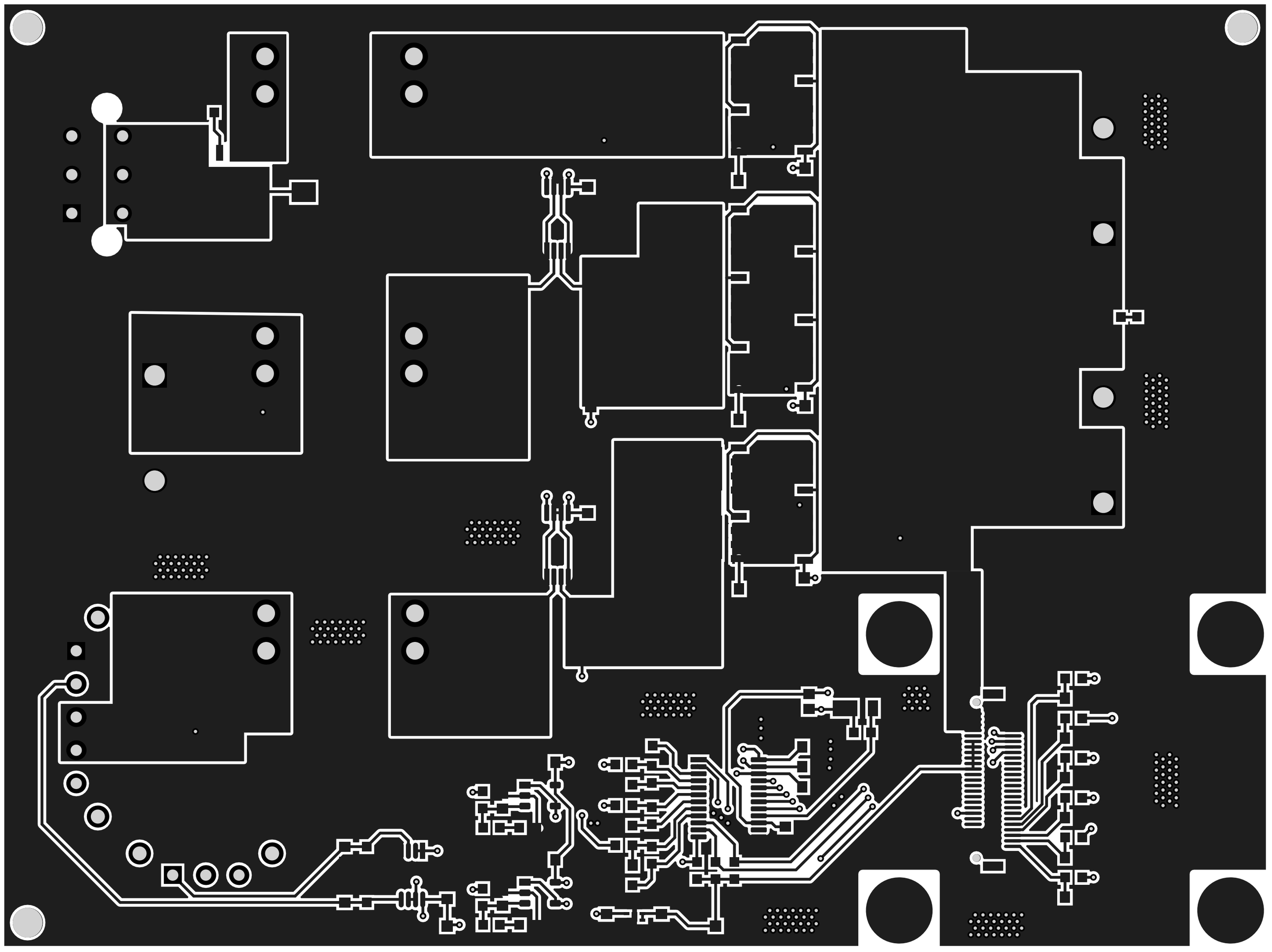
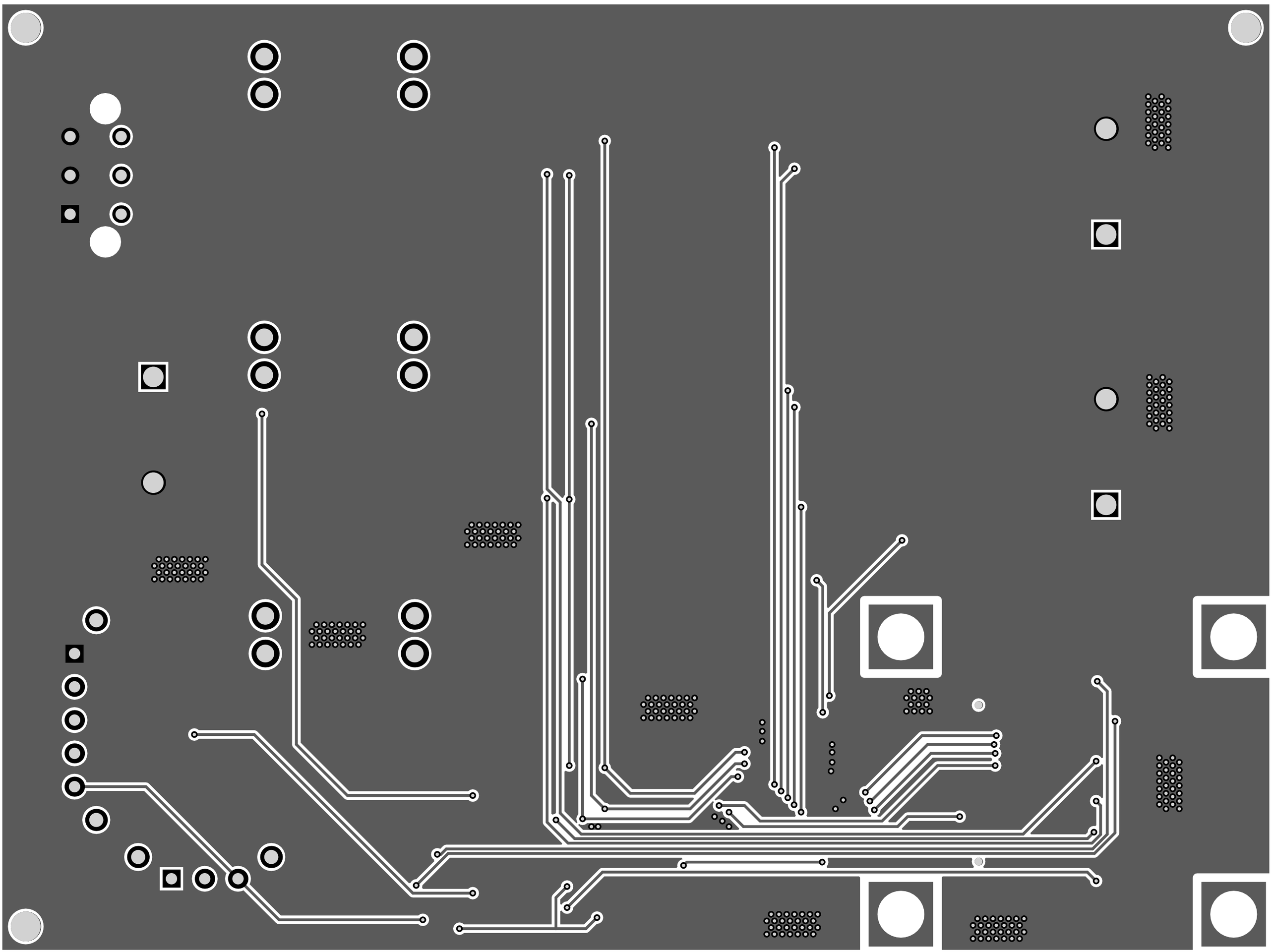
3V3
R9
C10
U4
R11
R12
M1





Design Rules Verification Report

Filename : D:\Josh9\Documents\Midnight Sun\hardware\MSXIV_PowerSelection\Power Sel

Warnings 0
Rule Violations 185

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.254mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	7
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	12
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	164
Silk to Silk (Clearance=0.254mm) (All),(All)	2
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	185

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(112.5mm,83.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,83.5mm) on Multi-Layer Actual Hole Size = 2.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M1-(81.4mm,3.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M2-(111.4mm,3.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M3-(81.4mm,28.6mm) on Multi-Layer Actual Hole Size = 3.7mm
Hole Size Constraint: (3.7mm > 2.54mm) Pad M4-(111.4mm,28.6mm) on Multi-Layer Actual Hole Size = 3.7mm

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(88.4mm,22.45mm) on Multi-Layer And Pad P1-(89.9mm,23.2mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(88.4mm,8.35mm) on Multi-Layer And Pad P1-(89.9mm,7.6mm) on Top
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-1(56.735mm,3.325mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-1(56.735mm,3.325mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.012mm < 0.254mm) Between Pad U1-2(56.735mm,2.725mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-4(58.175mm,3.325mm) on Top Layer And Pad U1-5(57.45mm,3.025mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-1(47.525mm,6.15mm) on Top Layer And Pad U4-2(47.525mm,5.2mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U4-2(47.525mm,5.2mm) on Top Layer And Pad U4-3(47.525mm,4.25mm) or
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-1(47.525mm,14.95mm) on Top Layer And Pad U6-2(47.525mm,14mm)
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U6-2(47.525mm,14mm) on Top Layer And Pad U6-3(47.525mm,13.05mm)

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.188mm < 0.254mm) Between Arc (56.227mm,3.579mm) on Top Overlay And Pad U1-1(56.735mm,3.325mm)
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-1(36.3mm,46.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-1(36.3mm,46.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-2(36.3mm,40.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C12-2(36.3mm,40.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(90.2mm,41.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-1(90.2mm,41.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(90.2mm,35.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C22-2(90.2mm,35.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-1(90.2mm,76.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-1(90.2mm,76.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-2(90.2mm,82.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C23-2(90.2mm,82.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(36.4mm,21.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-1(36.4mm,21.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(36.4mm,15.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad C4-2(36.4mm,15.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D1-2(24.1mm,17.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D2-2(24mm,42.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Pad D4-2(27.5mm,64.536mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-3(24.1mm,27.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F1-4(37.57mm,27.1mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-3(24mm,52.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F2-4(37.47mm,52.2mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F3-3(24mm,77.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad F3-4(37.47mm,77.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.161mm < 0.254mm) Between Pad GND-TP(6.5mm,80.2mm) on Top Layer And Text "Power Supply"
Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(104.45mm,57.31mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-1(91.7mm,21.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.223mm < 0.254mm) Between Pad P1-25(91.7mm,9.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-26(88.1mm,9.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.239mm < 0.254mm) Between Pad P1-50(88.1mm,21.4mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-1(66.895mm,72.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-2(66.895mm,73.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-3(66.895mm,74.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-4(66.895mm,76.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-5(61.405mm,76.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-6(61.405mm,74.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-7(61.405mm,73.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q10-8(61.405mm,72.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-1(72.895mm,54.665mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-2(72.895mm,53.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-3(72.895mm,52.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-4(72.895mm,50.855mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-5(78.385mm,50.855mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-6(78.385mm,52.125mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-7(78.385mm,53.395mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q11-8(78.385mm,54.665mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-1(66.9mm,50.765mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-2(66.9mm,52.035mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-3(66.9mm,53.305mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-4(66.9mm,54.575mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-5(61.41mm,54.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-6(61.41mm,53.305mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-7(61.41mm,52.035mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q12-8(61.41mm,50.765mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-1(72.895mm,45.465mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-2(72.895mm,44.195mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-3(72.895mm,42.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-4(72.895mm,41.655mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-5(78.385mm,41.655mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-6(78.385mm,42.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-7(78.385mm,44.195mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q13-8(78.385mm,45.465mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-1(66.895mm,41.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-2(66.895mm,42.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-3(66.895mm,44.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-4(66.895mm,45.47mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-5(61.405mm,45.47mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-6(61.405mm,44.2mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-7(61.405mm,42.93mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q14-8(61.405mm,41.66mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-1(72.895mm,39.105mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-2(72.895mm,37.835mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-3(72.895mm,36.565mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-4(72.895mm,35.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-5(78.385mm,35.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-6(78.385mm,36.565mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-7(78.385mm,37.835mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q15-8(78.385mm,39.105mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-1(66.895mm,35.455mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-2(66.895mm,36.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-3(66.895mm,37.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-4(66.895mm,39.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-5(61.405mm,39.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-6(61.405mm,37.995mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-7(61.405mm,36.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q16-8(61.405mm,35.455mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-1(23.7mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-2(22.43mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-3(21.16mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-4(19.89mm,72.19mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-5(19.89mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-6(21.16mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-7(22.43mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q19-8(23.7mm,66.7mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-1(72.895mm,67.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-2(72.895mm,65.795mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-3(72.895mm,64.525mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-4(72.895mm,63.255mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-5(78.385mm,63.255mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-6(78.385mm,64.525mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-7(78.385mm,65.795mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q3-8(78.385mm,67.065mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-1(66.895mm,63.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-2(66.895mm,64.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-3(66.895mm,65.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-4(66.895mm,67.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-5(61.405mm,67.075mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-6(61.405mm,65.805mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-7(61.405mm,64.535mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q4-8(61.405mm,63.265mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-1(72.895mm,82.505mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-2(72.895mm,81.235mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-3(72.895mm,79.965mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-4(72.895mm,78.695mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-5(78.385mm,78.695mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-6(78.385mm,79.965mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-7(78.385mm,81.235mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q5-8(78.385mm,82.505mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-1(66.895mm,78.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-2(66.895mm,79.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-3(66.895mm,81.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-4(66.895mm,82.405mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-5(61.405mm,82.405mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-6(61.405mm,81.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-7(61.405mm,79.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q6-8(61.405mm,78.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-1(72.895mm,60.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-2(72.895mm,59.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-3(72.895mm,58.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-4(72.895mm,57.055mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-5(78.385mm,57.055mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-6(78.385mm,58.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-7(78.385mm,59.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q7-8(78.385mm,60.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-1(66.895mm,57.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-2(66.895mm,58.335mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-3(66.895mm,59.605mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-4(66.895mm,60.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-5(61.405mm,60.875mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-6(61.405mm,59.605mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-7(61.405mm,58.335mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q8-8(61.405mm,57.065mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-1(72.895mm,76.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-2(72.895mm,74.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-3(72.895mm,73.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-4(72.895mm,72.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-5(78.385mm,72.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-6(78.385mm,73.595mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-7(78.385mm,74.865mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.179mm < 0.254mm) Between Pad Q9-8(78.385mm,76.135mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-1(56.735mm,3.325mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-2(56.735mm,2.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-3(58.175mm,2.725mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U1-4(58.175mm,3.325mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad U8-1(38.275mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-2(37.625mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-3(36.975mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-4(36.325mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-5(36.325mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-6(36.975mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-7(37.625mm,4.6mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad U8-8(38.275mm,4.6mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "C4" (32.233mm,24.79mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.186mm < 0.254mm) Between Text "GND" (7.5mm,79.8mm) on Top Overlay And Text "Power Supply"