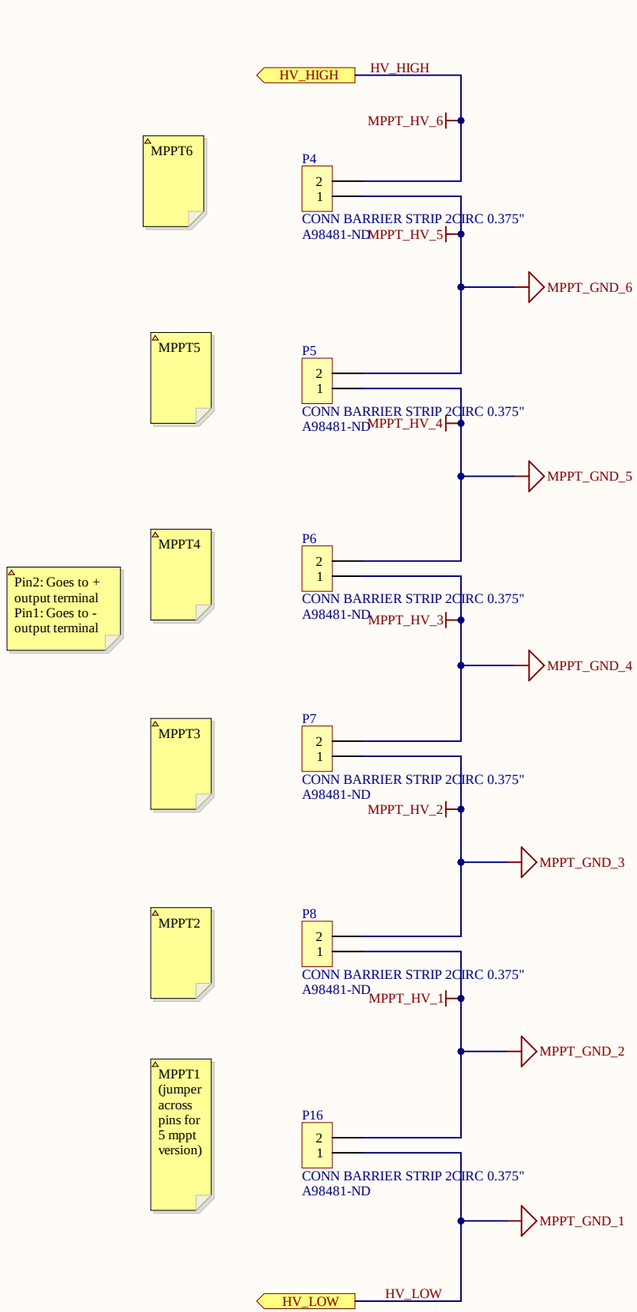
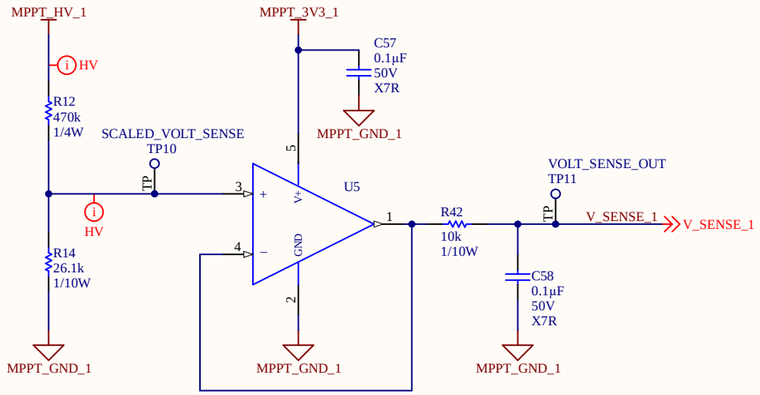
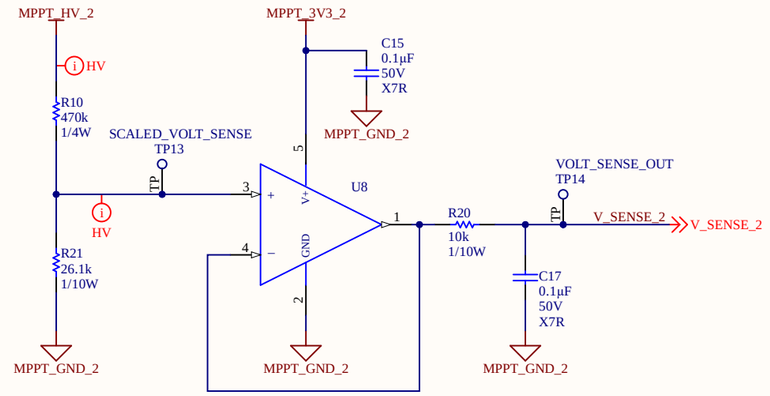
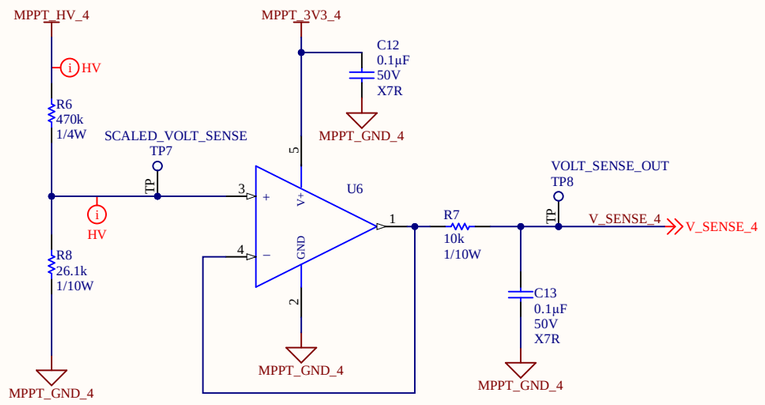
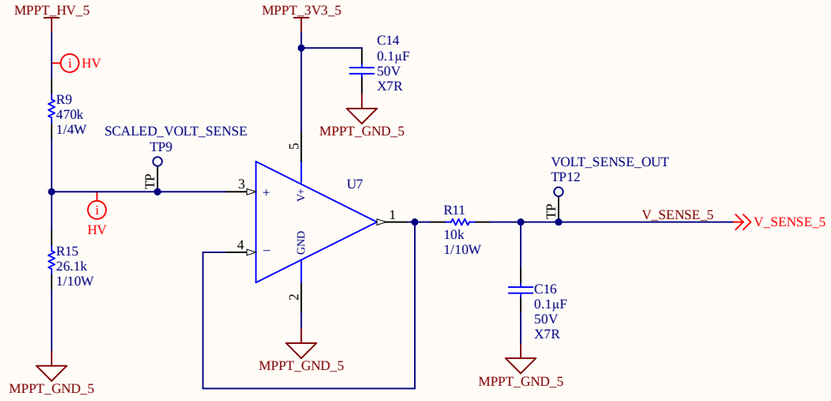
Voltage Sense

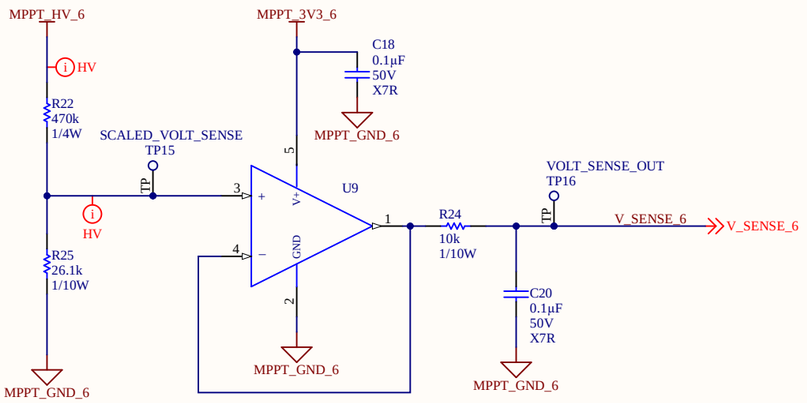




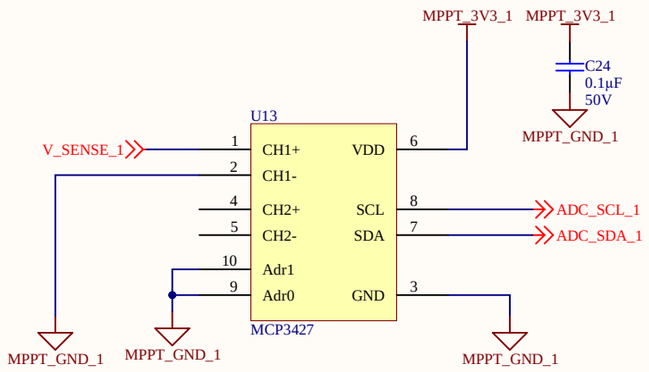


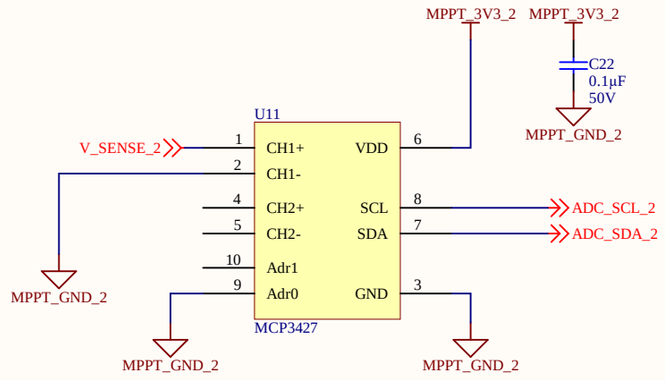


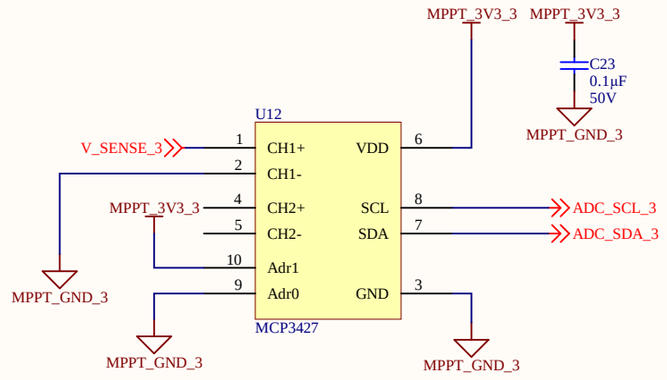




Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: **Solar Sense Slave**		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Lead: *		
Size: Letter	Revision: *	
Date: 2020-02-23	Sheet 3 of 4	Website: www.uwmidsun.com

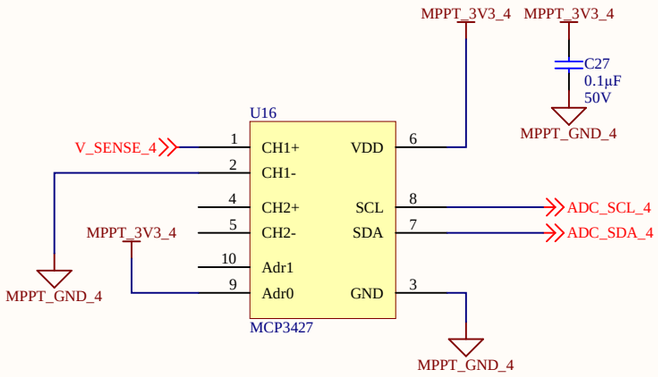


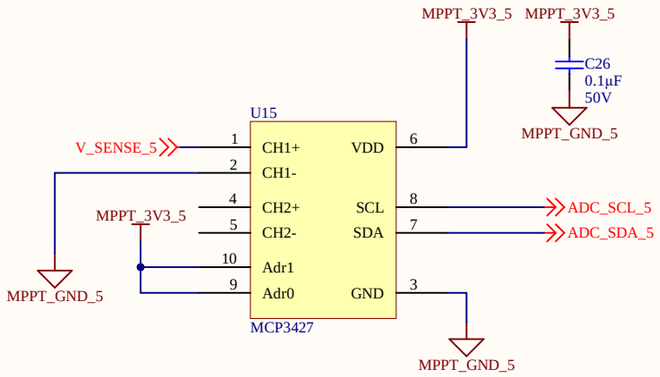


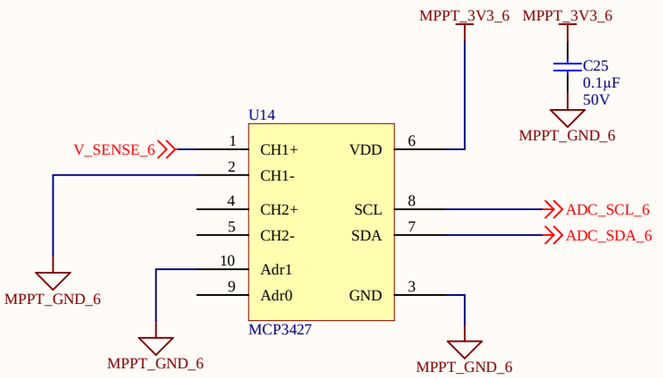


ADCs

I²C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float







Make combination of pulled high, low and floating (for address pins)

PROJECT	MSXIV_SolarSense.PrjPcb
DOCUMENT	*
PART NUMBER	
VARIANT	[No Variations]
DRAWN BY	Aashmika Mali
REVISION	1.0
LAST MODIFIED	2020-02-23
SHEET	* OF *

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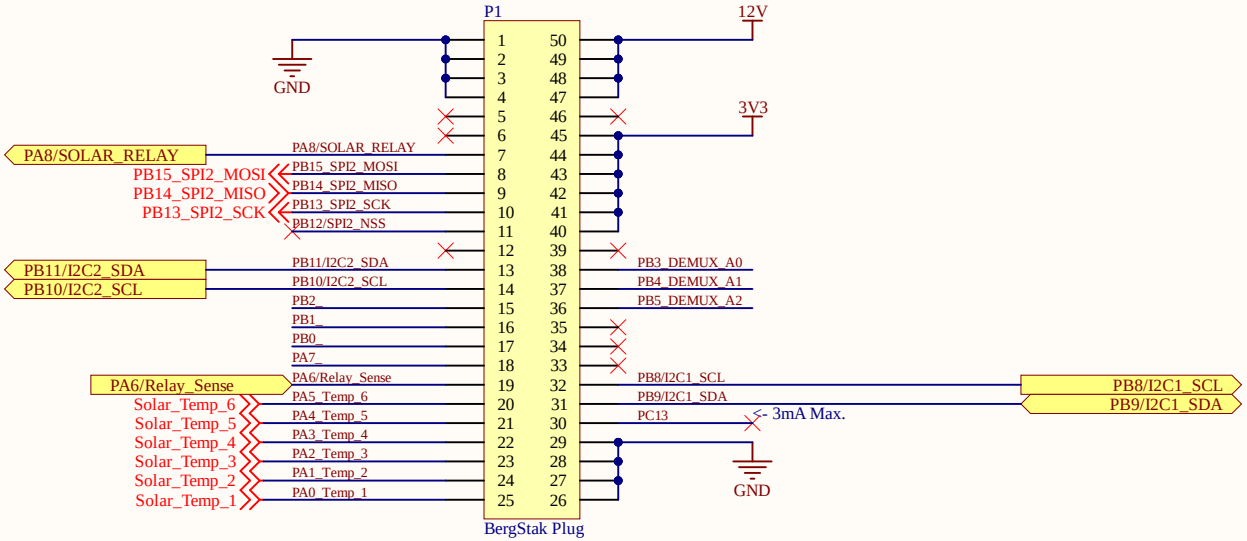
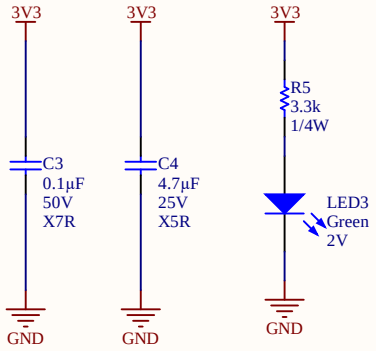
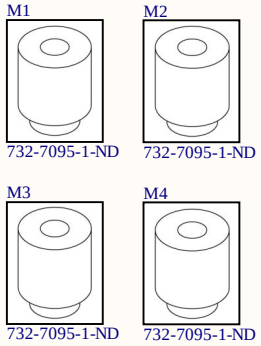
Controller Board

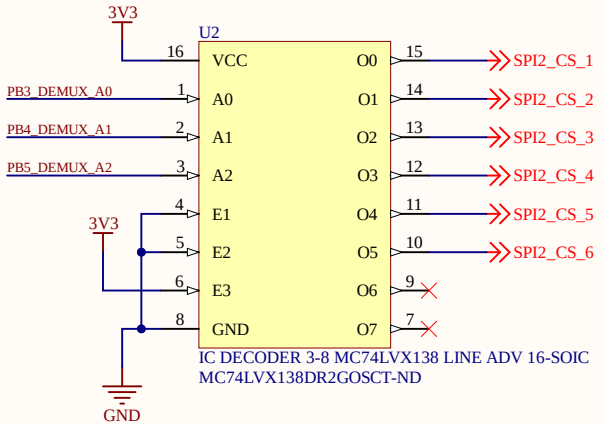


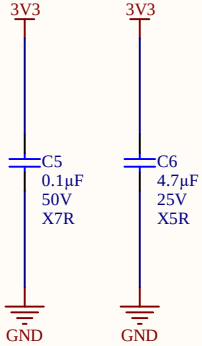


Standoffs



Solar Sense Rev 1.0
MSXIV LOGO
MSXIV_LOGO





Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: *		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Project Author: Aashmika Mali		
Size: Letter	Revision: 1.0	
Date: 2020-02-23	Sheet * of *	Website: www.uwmidsun.com

Passthrough - Current Sense, Fuse, and Relay

CONN BARRIER STRIP 2CIRC 0.375"
P2
2
1
HV_HIGH_NEG_BAT_TERM
HV_HIGH_POS_BAT_TERM
HV_LOW
A98481-ND

Pin2: Goes to the negative side of the battery pack
Pin1: Goes to the positive terminal of the battery pack
Note: the trace width for 15A and 170mm of length is 6.5mm

Power Path:
MPPT OUT -> CURRENT SNS -> FUSE -> RELAY -> IDEAL DIODE (this component last so that there is no current from battery to mppts because in this position the ideal diode cannot be forward biased unless the relay is closed and the fuse is intact) -> BATT TERMS

TH_TP2
HV CURRENT SENSE
HV_HIGH
10A
U1
ACS722LLCTR-10AU-T
IP+ VCC
IP+ VIOUT
IP- BW_SEL
IP- GND
3V3
3V3
C7
0.1µF
50V
GND
CURRENT_SENSE
TP
TP1
CURRENT SENSE OUT
DNP
R13
3/4W
0.0
R1
3/4W
0.0
TH_TP1
HV HIGH
TH_TP3
HV LOW
10A
10A
10A
HV_HIGH_IDEAL_DIODE
K1
F1
12A
SOLAR_RELAY_POS
RELAY AUTOMOTIVE SPST 25A 12V
Z4068-ND
D3
60V
3A
GND

Ideal Diode

1/10W good enough?
R19
1K
MPPT_GND_1
D4
ES1DFSCT-ND
200V
C9
720-1168-1-ND
470nF
200V
2220
Q2
Q3
IPB200N25N3GATMA1CT-ND
BSS126H6327XTSA2CT-ND
D5
DIODE ZENER 12V 500MW SOD123
8222413
R51
1M
1/10W
HV_HIGH_IDEAL_DIODE
HV_HIGH_POS_BAT_TERM
C1
C2
CAP ALUM 10UF 20% 200V SMD
MPPT_GND_1
Bulk cap for output of power supply created from 6 mppt sources
LTC4359IMS8#PBF-ND
U29
IN
SOURCE
GATE
OUT
NC
NC
SHDN
VSS
C66
10000pF
50V
U2J
D6
DIODE ZENER 12V 500MW SOD123
8222413
D7
DIODE ZENER 15V 150MW SOD523
R54
RES 200K OHM 0.5% 1/4W 0805
P21279CT-ND
MPPT_GND_1

P3
12V
12V
C38
25V
10µF
GND
GND

12V
TP
TP5
12V
3V3
TP
TP6
3V3
GND
TP4
TP
GND

Relay coil low current driver

SOLAR ENABLE
TP33
PA8/SOLAR_RELAY
DRV120PWR
U4
EN
HOLD
KEEP
OSC
PEAK
VIN
OUT STATUS
NC
NC
NC
NC
NC
GND
SOLAR_RELAY_POS
R49
RES 200K
C64
1µF 50V
R52
RES 200K
R53
X7R 1/10W78.7k
12V
C65
4.7uF
50V
R50
4.7k
1/10W
LED2
Yellow
2V
GND
GND
GND

PROJECT	MSXIV_SolarSense.PrjPcb		MIDNIGHT SUN
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-23	SHEET * OF *	

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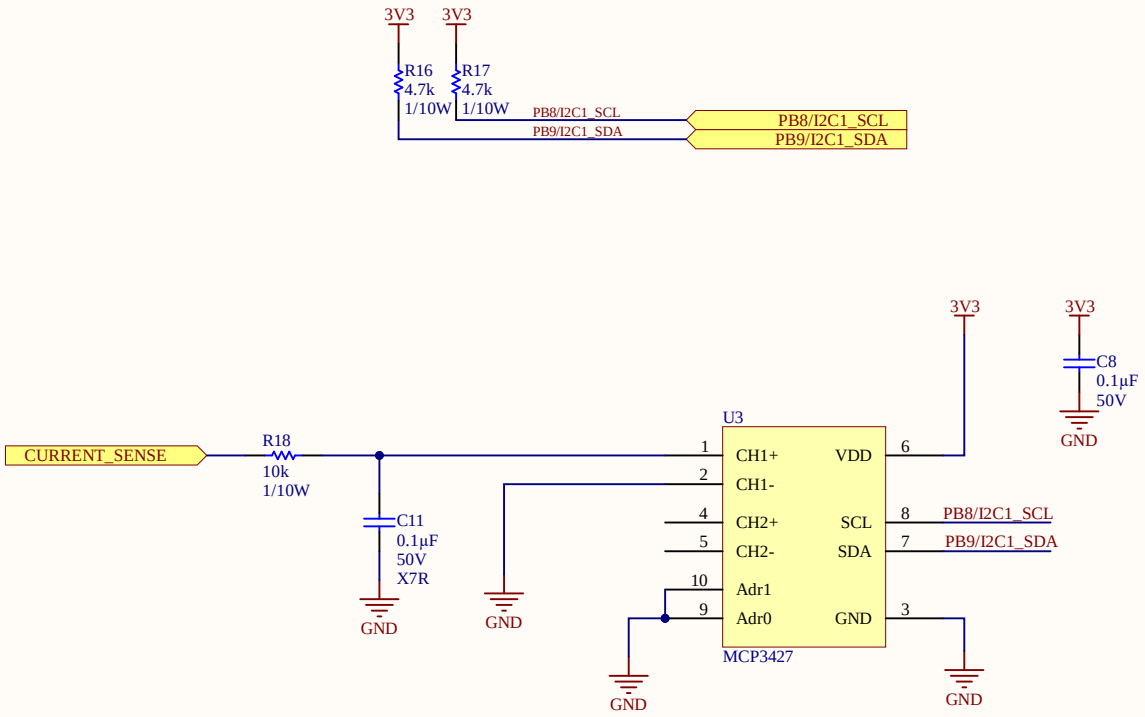
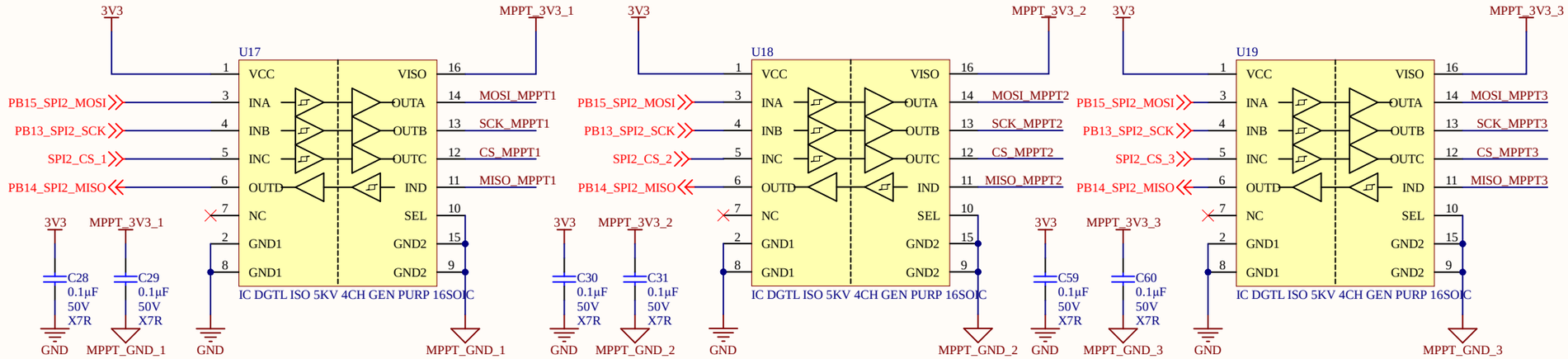
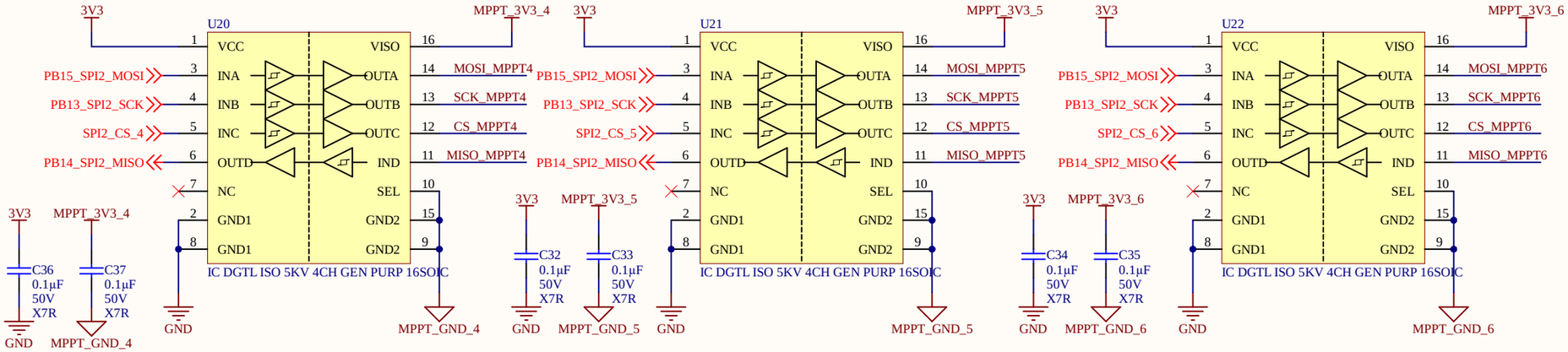
I2C Interface (for Current Sense)

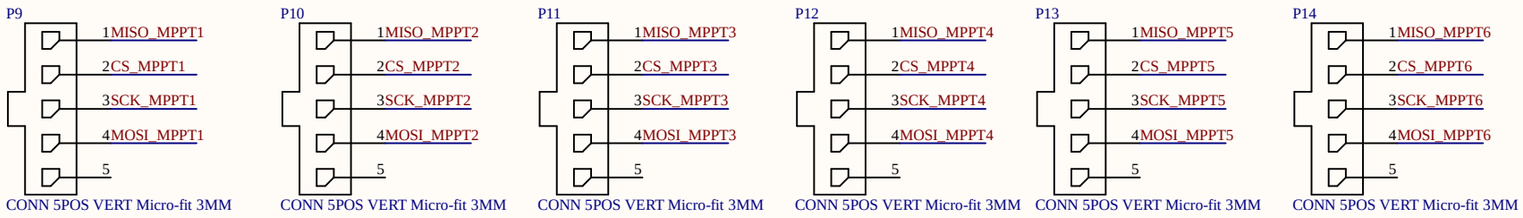


Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
Title: *		
Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2020-02-23	Sheet * of *	Website: www.uwmidsun.com

SPI Isolators







PROJECT	MSXIV_SolarSense.PrjPcb		
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-23	SHEET	* OF *

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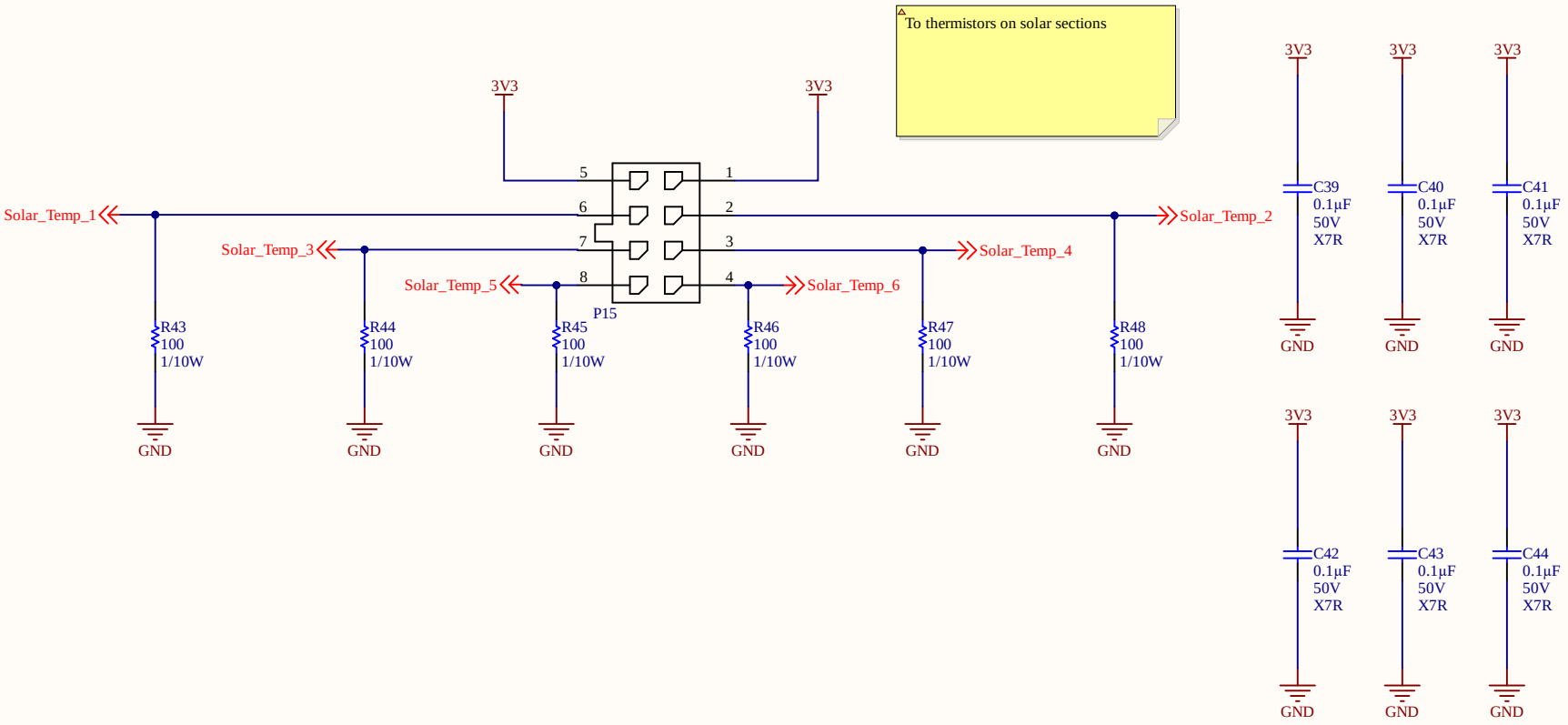
Temperature Sense for Array Sections



Project: ***MSXIV_SolarSense.PrjPcb***		MIDNIGHT SUN
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Project Author: Aashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
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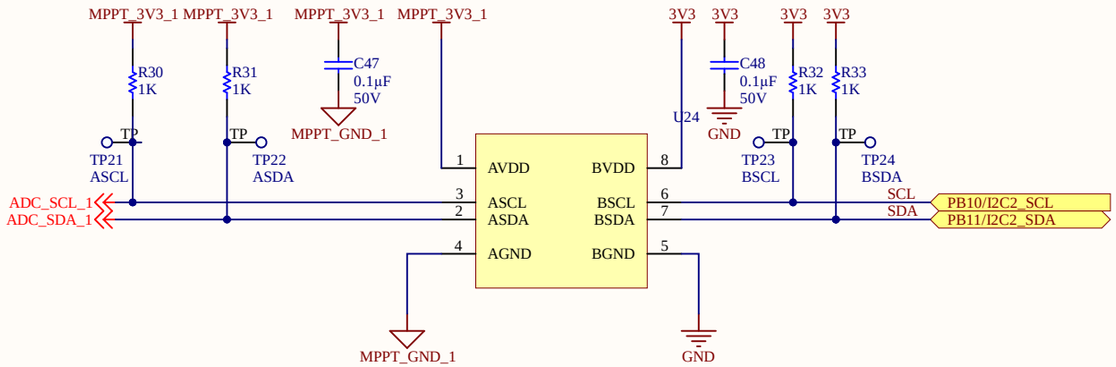
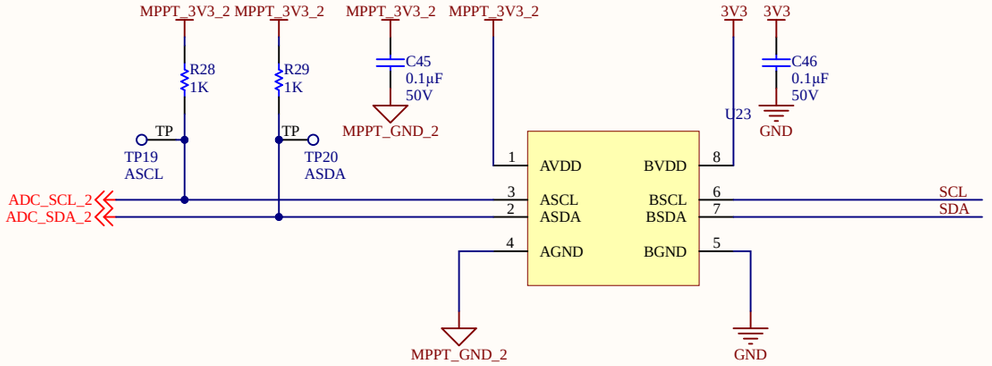
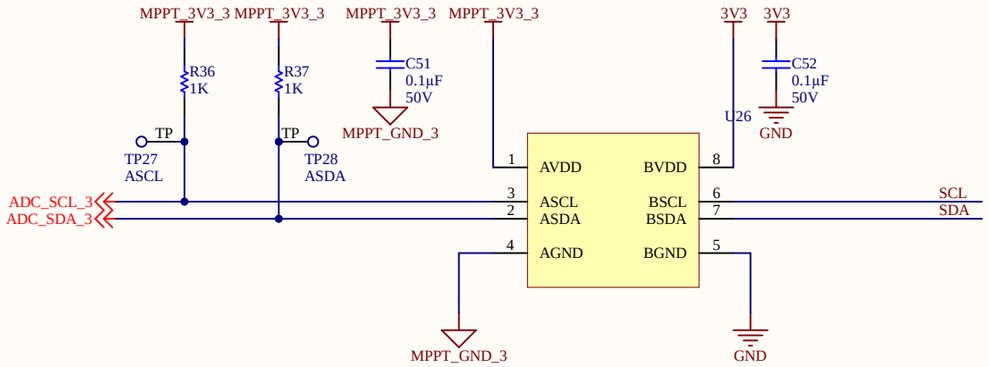
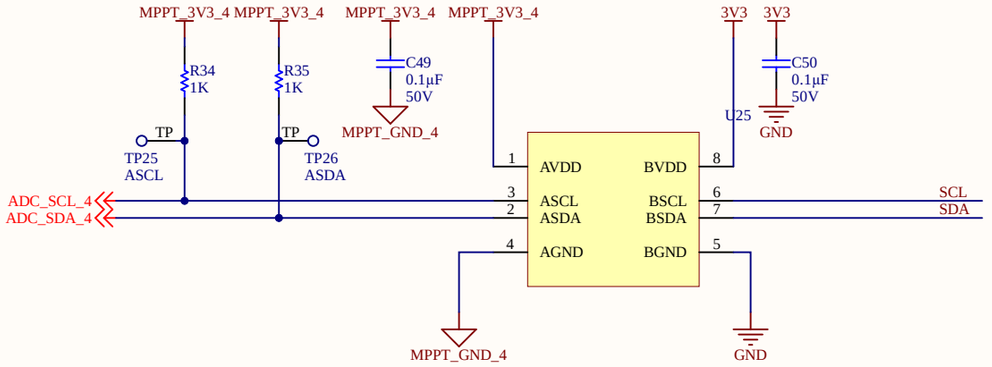
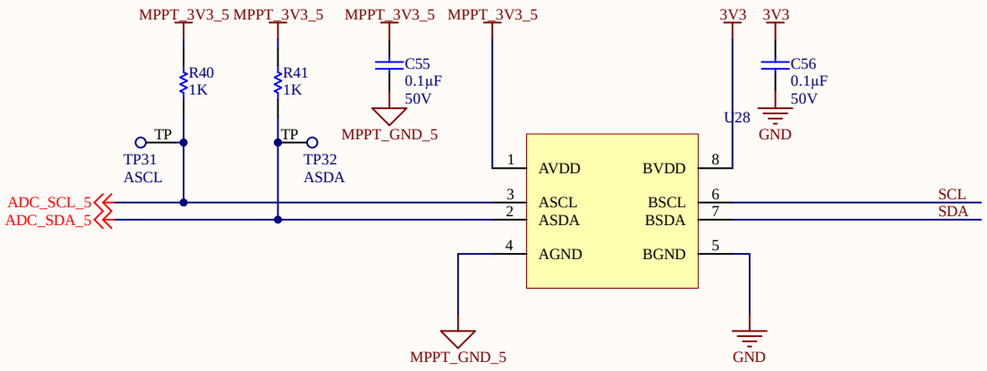
I2C Isolators for V-Sense

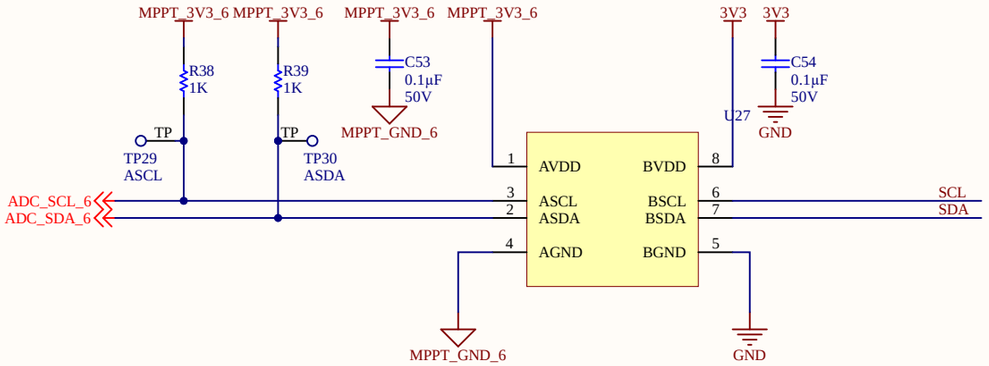












PROJECT	MSXIV_SolarSense.PrjPcb		MIDNIGHT SUN
DOCUMENT	*		
PART NUMBER		VARIANT	[No Variations]
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-23	SHEET	* OF *

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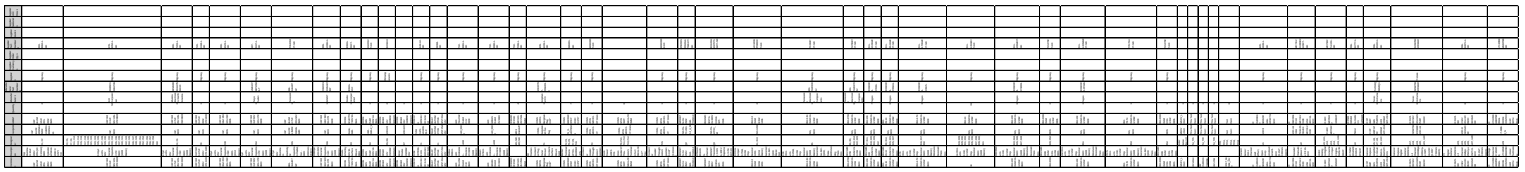
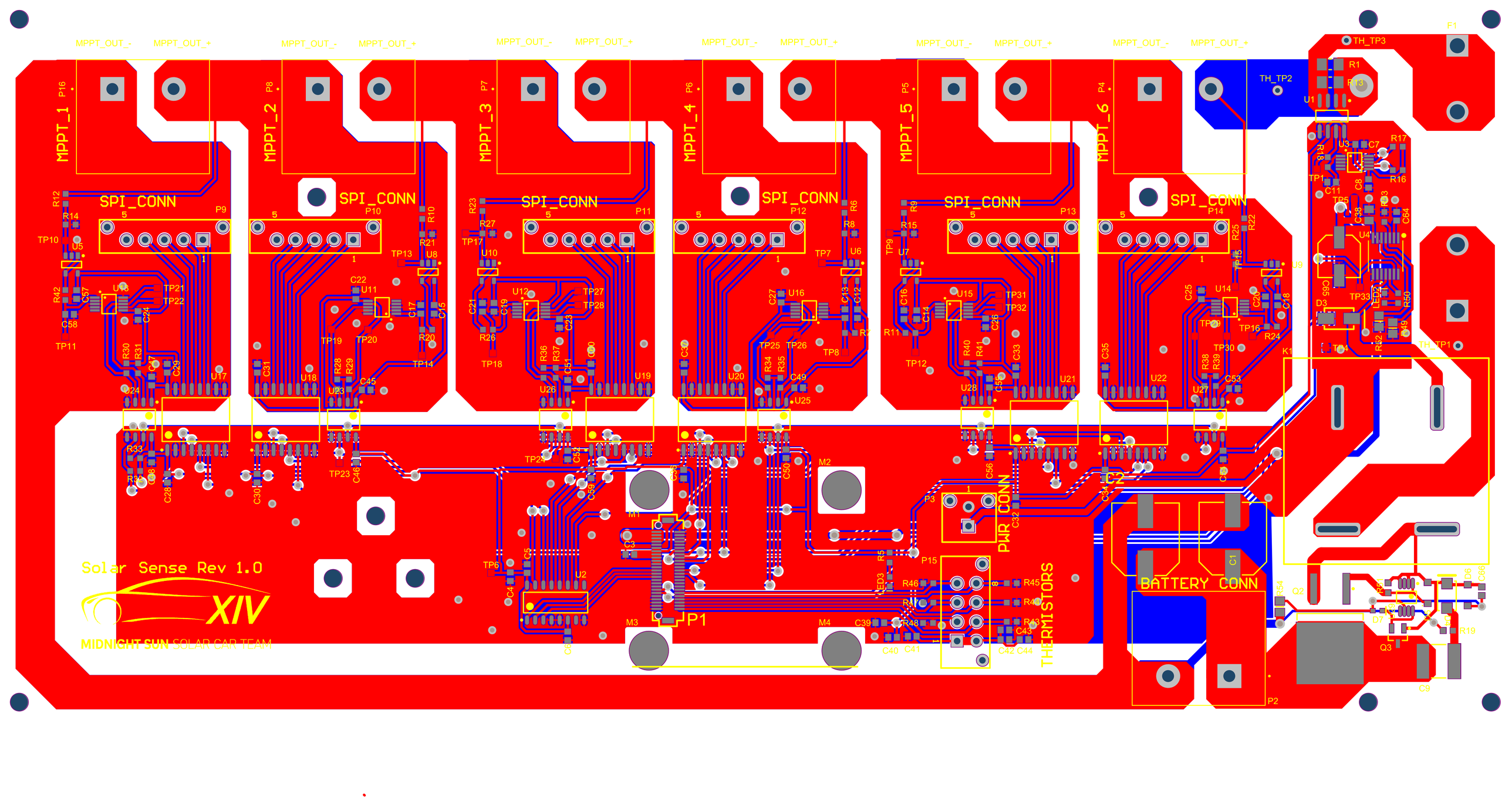
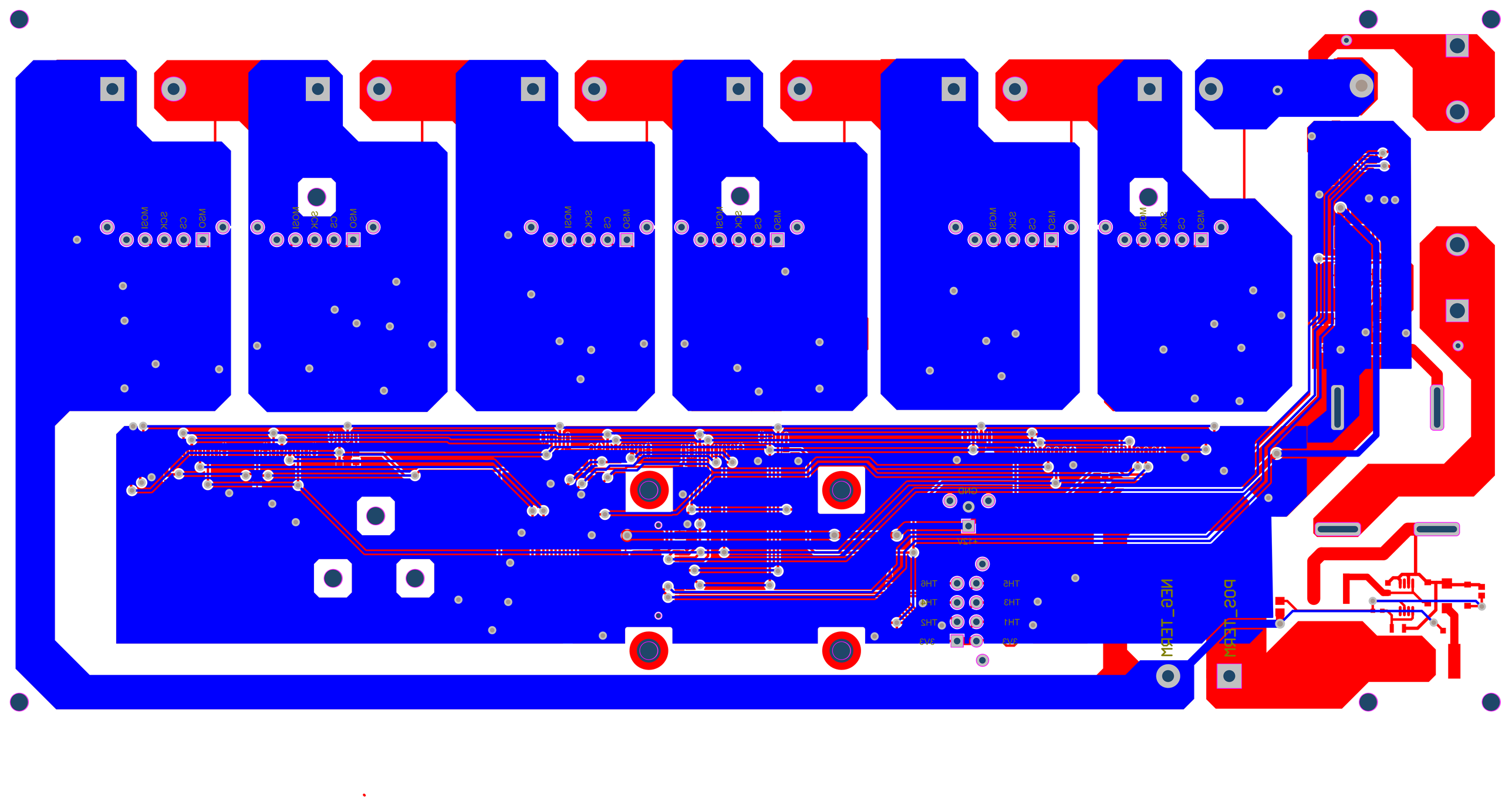



MPPT_1
MPPT_2
MPPT_3
MPPT_4
MPPT_5
MPPT_6
SPI_CONN
PWR CONN
BATTERY CONN
THERMISTORS
Solar Sense Rev 1.0
XIV
MIDNIGHT SUN SOLAR CAR TEAM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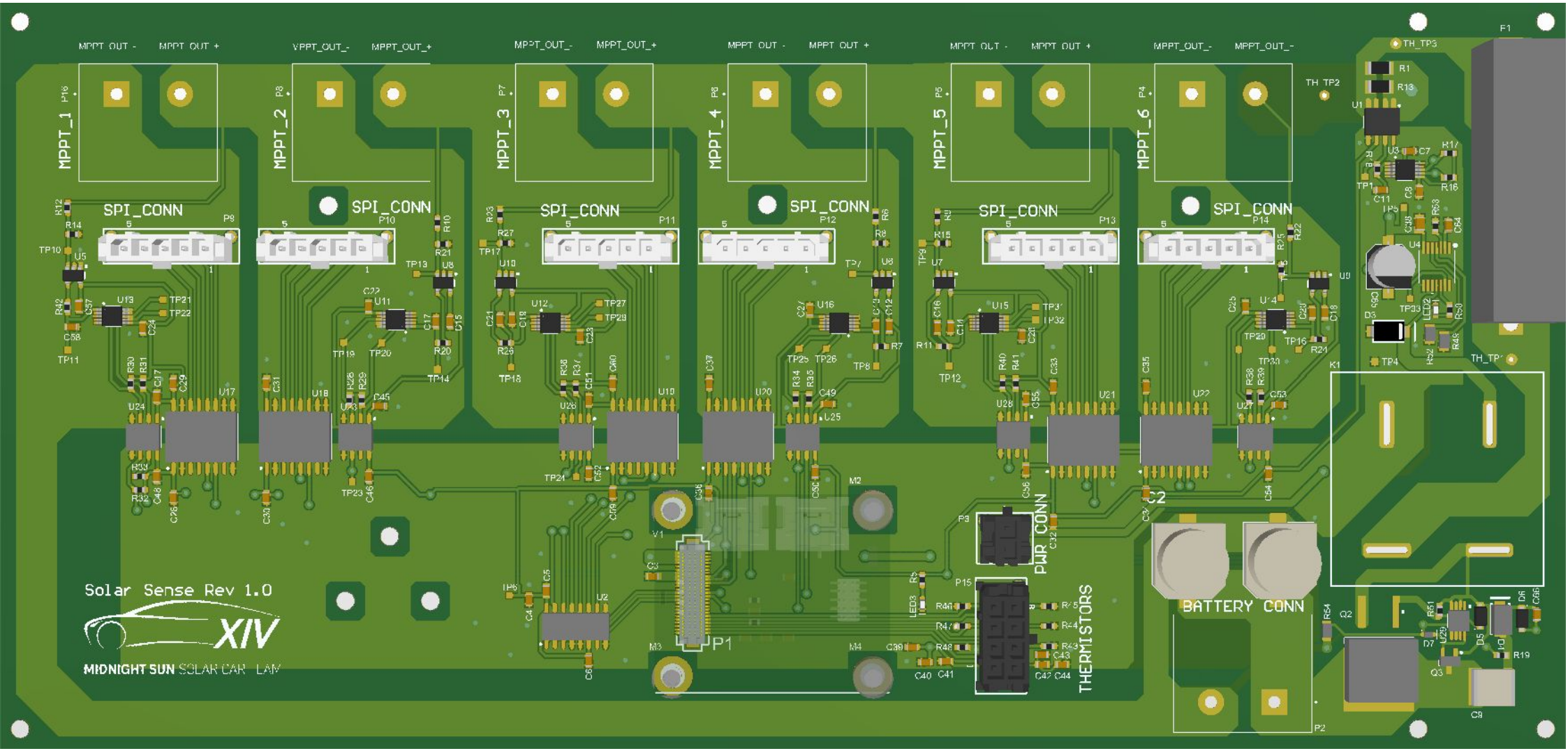
SCK
CS
MISO
MOSI_3V3
MISO_3V3


MPPT_1
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MPPT_3
MPPT_4
MPPT_5
MPPT_6
SPI_CONN
PWR_CONN
THERMISTORS
BATTERY CONN
Solar Sense Rev 1.0
XIV
MIDNIGHT SUN SOLAR CAR LAM

Electrical Rules Check Report

Class	Document	Message
Error	Voltage_Sense.SchDoc	HV_LOW contains Power Pin and Output Port objects (Pin U5-2, Port HV_LOW).
Error	Controller_Board_Interface.SchDoc	Net PA6/Relay_Sense has only one pin (Pin P1-19)
Error	Controller_Board_Interface.SchDoc	Net PA7_ has only one pin (Pin P1-18)
Error	Controller_Board_Interface.SchDoc	Net PB0_ has only one pin (Pin P1-17)
Error	Controller_Board_Interface.SchDoc	Net PB1_ has only one pin (Pin P1-16)
Error	Controller_Board_Interface.SchDoc	Net PB2_ has only one pin (Pin P1-15)
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_GND_1 at 3650mil,1830mil has been reduced to local level by presence of port at 2000mil,1300mil
Warning	Voltage_Sense.SchDoc	Global Power-Object MPPT_HV_6 at 3350mil,9100mil has been reduced to local level by presence of port at 2000mil,9400mil
Warning	Controller_Board_Interface.SchDoc	Net 12V has no driving source (Pin C38-1, Pin C65-1, Pin P1-47, Pin P1-48, Pin P1-49, Pin P1-50, Pin P3-1, Pin TP5-TP, Pin U4-7)
Warning	Current_and_Relay_Sense.SchDoc	Net NetC64_2 has no driving source (Pin C64-2, Pin U4-2)
Warning	Current_and_Relay_Sense.SchDoc	Net NetD7_2 has no driving source (Pin D7-2, Pin Q3-2, Pin U29-8)
Warning	Voltage_Sense.SchDoc	Net NetR6_2 has no driving source (Pin R6-2, Pin R8-1, Pin TP7-TP, Pin U6-3)
Warning	Voltage_Sense.SchDoc	Net NetR9_2 has no driving source (Pin R9-2, Pin R15-1, Pin TP9-TP, Pin U7-3)
Warning	Voltage_Sense.SchDoc	Net NetR10_2 has no driving source (Pin R10-2, Pin R21-1, Pin TP13-TP, Pin U8-3)
Warning	Voltage_Sense.SchDoc	Net NetR12_2 has no driving source (Pin R12-2, Pin R14-1, Pin TP10-TP, Pin U5-3)
Warning	Voltage_Sense.SchDoc	Net NetR22_2 has no driving source (Pin R22-2, Pin R25-1, Pin TP15-TP, Pin U9-3)
Warning	Voltage_Sense.SchDoc	Net NetR23_2 has no driving source (Pin R23-2, Pin R27-1, Pin TP17-TP, Pin U10-3)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR49_2 has no driving source (Pin R49-2, Pin U4-4)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR52_2 has no driving source (Pin R52-2, Pin U4-5)
Warning	Current_and_Relay_Sense.SchDoc	Net NetR53_2 has no driving source (Pin R53-2, Pin U4-3)
Warning	Controller_Board_Interface.SchDoc	Net PB3_DEMUX_A0 has no driving source (Pin P1-38, Pin U2-1)
Warning	Controller_Board_Interface.SchDoc	Net PB4_DEMUX_A1 has no driving source (Pin P1-37, Pin U2-2)
Warning	Controller_Board_Interface.SchDoc	Net PB5_DEMUX_A2 has no driving source (Pin P1-36, Pin U2-3)
Warning	Current_and_Relay_Sense.SchDoc	Nets Wire HV_HIGH has multiple names (Net Label HV_HIGH, Power Object MPPT_HV_6, Power Object MPPT_HV_6)
Warning	ADCs.SchDoc	Nets Wire HV_HIGH_NEG_BAT_TERM has multiple names (Net Label HV_HIGH_NEG_BAT_TERM, Net Label HV_LOW, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Powe Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Powe Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Powe Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1, Powe Object MPPT_GND_1, Power Object MPPT_GND_1, Power Object MPPT_GND_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_2 has multiple names (Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Objec MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Objec MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Objec MPPT_GND_2, Power Object MPPT_GND_2, Power Object MPPT_GND_2, Power Objec MPPT_HV_1, Power Object MPPT_HV_1)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_3 has multiple names (Power Object MPPT_GND_3, Power Objec MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Objec MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Objec MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Objec MPPT_GND_3, Power Object MPPT_GND_3, Power Object MPPT_GND_3, Power Objec MPPT_HV_2, Power Object MPPT_HV_2)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_4 has multiple names (Power Object MPPT_GND_4, Power Objec MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Objec MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Objec MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_GND_4, Power Objec MPPT_GND_4, Power Object MPPT_GND_4, Power Object MPPT_HV_3, Power Object MPPT_HV_3)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_5 has multiple names (Power Object MPPT_GND_5, Power Objec MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Objec MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Objec MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_GND_5, Power Objec MPPT_GND_5, Power Object MPPT_GND_5, Power Object MPPT_HV_4, Power Object MPPT_HV_4)
Warning	ADCs.SchDoc	Nets Wire MPPT_GND_6 has multiple names (Power Object MPPT_GND_6, Power Objec MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Objec

Class	Document	Message
		MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_GND_6, Power Object MPPT_HV_5, Power Object MPPT_HV_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA0_Temp_1 has multiple names (Cross-Sheet Connector Solar_Temp_1, Cross-Sheet Connector Solar_Temp_1, Net Label PA0_Temp_1)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA1_Temp_2 has multiple names (Cross-Sheet Connector Solar_Temp_2, Cross-Sheet Connector Solar_Temp_2, Net Label PA1_Temp_2)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA2_Temp_3 has multiple names (Cross-Sheet Connector Solar_Temp_3, Cross-Sheet Connector Solar_Temp_3, Net Label PA2_Temp_3)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA3_Temp_4 has multiple names (Cross-Sheet Connector Solar_Temp_4, Cross-Sheet Connector Solar_Temp_4, Net Label PA3_Temp_4)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA4_Temp_5 has multiple names (Cross-Sheet Connector Solar_Temp_5, Cross-Sheet Connector Solar_Temp_5, Net Label PA4_Temp_5)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PA5_Temp_6 has multiple names (Cross-Sheet Connector Solar_Temp_6, Cross-Sheet Connector Solar_Temp_6, Net Label PA5_Temp_6)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB10/I2C2_SCL has multiple names (Net Label PB10/I2C2_SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL, Net Label SCL)
Warning	Controller_Board_Interface.SchDoc	Nets Wire PB11/I2C2_SDA has multiple names (Net Label PB11/I2C2_SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA, Net Label SDA)
Warning	ADCs.SchDoc	Off grid C24 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SCL_1 at 3600mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector ADC_SDA_1 at 3600mil,7544.41mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB13_SPI2_SCK at 6574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB14_SPI2_MISO at 6574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Cross-Sheet Connector PB15_SPI2_MOSI at 6574.41mil,6851.811mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_2 at 7837.008mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_4 at 6687.008mil,4596.063mil
Warning	Controller_Board_Interface.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 2247.008mil,4300mil
Warning	TemperatureSense.SchDoc	Off grid Cross-Sheet Connector Solar_Temp_6 at 5700mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_1 at 1350mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_2 at 6281.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_3 at 11381.89mil,8100mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_4 at 1631.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_5 at 6531.89mil,3500mil
Warning	ADCs.SchDoc	Off grid Cross-Sheet Connector V_SENSE_6 at 11231.89mil,3400mil
Warning	Controller_Board_Interface.SchDoc	Off grid M1 at 1693.983mil,2899.713mil
Warning	Controller_Board_Interface.SchDoc	Off grid M2 at 2406.601mil,2898.306mil
Warning	Controller_Board_Interface.SchDoc	Off grid M3 at 1693.983mil,1949.714mil
Warning	Controller_Board_Interface.SchDoc	Off grid M4 at 2406.601mil,1948.306mil
Warning	SPI_Interface.SchDoc	Off grid Net Label CS_MPPT2 at 8674.41mil,6451.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label HV_HIGH_NEG_BAT_TERM at 998.148mil,7600mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT2 at 8624.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MISO_MPPT3 at 12055.512mil,6250mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT2 at 8674.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Net Label MOSI_MPPT3 at 12055.512mil,6850mil
Warning	SPI_Interface.SchDoc	Off grid Net Label SCK_MPPT2 at 8674.41mil,6651.811mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid Net Label SOLAR_RELAY_POS at 11601.896mil,3900mil
Warning	Current_and_Relay_Sense.SchDoc	Off grid NetParameter at 6495.503mil,7000mil
Warning	SPI_Interface.SchDoc	Off grid No ERC at 6774.41mil,6051.811mil
Warning	TemperatureSense.SchDoc	Off grid P15 at 4521.654mil,5096.063mil
Warning	ADCs.SchDoc	Off grid Pin C24-1 at 3818.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Pin C24-2 at 3818.11mil,8374.41mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-1 at 5421.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-2 at 5421.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-3 at 5421.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-4 at 5421.654mil,4396.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-5 at 4521.654mil,4996.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-6 at 4521.654mil,4796.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-7 at 4521.654mil,4596.063mil
Warning	TemperatureSense.SchDoc	Off grid Pin P15-8 at 4521.654mil,4396.063mil
Warning	ADCs.SchDoc	Off grid Pin U13-1 at 1658.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-2 at 1658.11mil,7894.41mil

Class	Document	Message
Warning	ADCs.SchDoc	Off grid Pin U13-3 at 3108.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-8 at 6774.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-9 at 8574.41mil,5651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-10 at 8574.41mil,6051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 4099.606mil,5389.764mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	Controller_Board_Interface.SchDoc	Off grid Solar Sense Rev 1.0 at 4505.679mil,2561.84mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_

Warnings 0
Rule Violations 159

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=80mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	24
Hole To Hole Clearance (Gap=10mil) (All),(All)	4
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	29
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	85
Silk to Silk (Clearance=10mil) (All),(All)	17
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	159

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-2218.858mil,3215.5mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4099.52mil,1418.004mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4099.52mil,433.752mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4720.984mil,3221.5mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5280.622mil,1418.004mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5280.622mil,433.752mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-6713.063mil,877.5mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-6954.677mil,1260.104mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-7215.393mil,877.5mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-7316.102mil,3215.5mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-871.173mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-871.173mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9138.89mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9138.89mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mi
Hole Size Constraint: (248.031mil > 100mil) Pad K1-1(-451mil,1179mil) on Multi-Layer Actual Slot Hole Height = 248.031mi
Hole Size Constraint: (248.031mil > 100mil) Pad K1-2(-1057.299mil,1179mil) on Multi-Layer Actual Slot Hole Height = 248.031mi
Hole Size Constraint: (248.031mil > 100mil) Pad K1-3(-449.031mil,1925.063mil) on Multi-Layer Actual Slot Hole Height = 248.031mi
Hole Size Constraint: (248.031mil > 100mil) Pad K1-4(-1059.268mil,1925.063mil) on Multi-Layer Actual Slot Hole Height = 248.031mi
Hole Size Constraint: (145.669mil > 100mil) Pad M1-(-5277.468mil,1419.409mil) on Multi-Layer Actual Hole Size = 145.669mi
Hole Size Constraint: (145.669mil > 100mil) Pad M2-(-4099.52mil,1418.004mil) on Multi-Layer Actual Hole Size = 145.669mi
Hole Size Constraint: (145.669mil > 100mil) Pad M3-(-5280.622mil,433.752mil) on Multi-Layer Actual Hole Size = 145.669mi
Hole Size Constraint: (145.669mil > 100mil) Pad M4-(-4099.52mil,433.752mil) on Multi-Layer Actual Hole Size = 145.669mi

Hole To Hole Clearance (Gap=10mil) (All),(All)
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4099.52mil,1418.004mil) on Multi-Layer And Pad
M2-(-4099.52mil,1418.004mil) Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4099.52mil,433.752mil) on Multi-Layer And Pad M4-(-4099.52mil,433.752mil)
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5280.622mil,1418.004mil) on Multi-Layer And Pac
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5280.622mil,433.752mil) on Multi-Layer And Pad
M3-(-5280.622mil,433.752mil)

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (6.727mil < 10mil) Between Pad C43-1(-3124.984mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (6.727mil < 10mil) Between Pad C43-2(-3071.834mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (8.198mil < 10mil) Between Pad C43-2(-3071.834mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5162.512mil,1232.964mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5162.512mil,618.791mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U10-1(-6229.441mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U10-2(-6266.842mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-1(-687.728mil,2965.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-10(-790.09mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-10(-790.09mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-11(-764.5mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-12(-738.909mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-13(-713.319mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-2(-713.319mil,2965.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-3(-738.909mil,2965.255mil) on Top Layer And Pad
U4-4(-764.5mil,2965.255mil) Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-4(-764.5mil,2965.255mil) on Top Layer And Pad
U4-5(-790.09mil,2965.255mil) Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-5(-790.09mil,2965.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-6(-815.681mil,2965.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-8(-841.271mil,2743.255mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U5-1(-8780.031mil,2856.232mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U5-2(-8817.433mil,2856.232mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U6-1(-4003.063mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U6-2(-4040.464mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U7-1(-3637.905mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U7-2(-3675.307mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U8-1(-6595.386mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U8-2(-6632.787mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U9-1(-1426.291mil,2805.799mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U9-2(-1463.693mil,2805.799mil) on Top Layer And Pac

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-230.11mil,851.756mil) on Top Overlay And Pad D6-1(-262mil,838.37mil) or
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-538.89mil,710.244mil) on Top Overlay And Pad D5-1(-507mil,723.63mil) or
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-853.37mil,702.622mil) on Top Overlay And Pad D7-1(-843.528mil,679mil) or
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C1-1(-1701mil,947.772mil) on Top Layer And Text "BATTERY CONN'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C1-1(-1701mil,947.772mil) on Top Layer And Text "C1'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-1701mil,947.772mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-1(-1701mil,947.772mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.709mil < 10mil) Between Pad C11-2(-1121.575mil,3308mil) on Top Layer And Text "TP1'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-1701mil,1294.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C1-2(-1701mil,1294.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.995mil < 10mil) Between Pad C15-1(-6595.386mil,2553.24mil) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (7.941mil < 10mil) Between Pad C15-2(-6595.386mil,2500.09mil) on Top Layer And Text "C15'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C2-1(-2236mil,943.772mil) on Top Layer And Text "BATTERY CONN'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C2-1(-2236mil,943.772mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C2-1(-2236mil,943.772mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C2-2(-2236mil,1290.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C2-2(-2236mil,1290.228mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C34-1(-2483.181mil,1543.004mil) on Top Layer And Text "C2'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad C34-2(-2483.181mil,1489.854mil) on Top Layer And Text "C2'
Silk To Solder Mask Clearance Constraint: (9.475mil < 10mil) Between Pad C6-2(-5776.488mil,498.713mil) on Top Layer And Text "C6'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-1049.5mil,2968.334mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-1049.5mil,2968.334mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-1049.5mil,2736.05mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-1049.5mil,2736.05mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-1130.008mil,2470.294mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-1130.008mil,2470.294mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-972.527mil,2470.294mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-972.527mil,2470.294mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (2.839mil < 10mil) Between Pad D7-2(-784.472mil,679mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED2-2(-772.301mil,2626.291mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(-3804.244mil,827.453mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M3-(-5280.622mil,433.752mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M4-(-4099.52mil,433.752mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P10-0(-6969.598mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-6969.598mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P10-0(-7678.26mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-7678.26mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.78mil < 10mil) Between Pad P1-1(-5091.646mil,1162.097mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P11-0(-5292.433mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-5292.433mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P11-0(-6001.094mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-6001.094mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P12-0(-4371.173mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-4371.173mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P12-0(-5079.834mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-5079.834mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.767mil < 10mil) Between Pad P1-25(-5091.646mil,689.657mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.4mil < 10mil) Between Pad P1-26(-5233.378mil,689.657mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P13-0(-2691.055mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-2691.055mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P13-0(-3399.716mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-3399.716mil,3031.39mil) on Multi-Layer And Track

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P14-0(-1772.748mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-1772.748mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P14-0(-2481.409mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-2481.409mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3235.74mil,374.697mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.376mil < 10mil) Between Pad P15-0(-3235.74mil,374.697mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3235.74mil,965.248mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.918mil < 10mil) Between Pad P15-0(-3235.74mil,965.248mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.401mil < 10mil) Between Pad P1-50(-5233.378mil,1162.097mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P3-0(-3198.89mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3198.89mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P3-0(-3435.11mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3435.11mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P9-0(-7890.858mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-7890.858mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P9-0(-8599.519mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-8599.519mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.133mil < 10mil) Between Pad R18-1(-1119mil,3460.512mil) on Top Layer And Text "R18'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-1(-1684.549mil,2803.988mil) on Top Layer And Text "TP15'
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-2(-1684.549mil,2865.012mil) on Top Layer And Text "TP15'
Silk To Solder Mask Clearance Constraint: (2.51mil < 10mil) Between Pad R28-2(-7190.071mil,2037.098mil) on Top Layer And Text "U23'
Silk To Solder Mask Clearance Constraint: (9.584mil < 10mil) Between Pad R38-2(-1875.11mil,2056.783mil) on Top Layer And Text "U27'
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R49-1(-720.701mil,2376.449mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R49-2(-720.701mil,2447.315mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R52-1(-805.611mil,2419.175mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R52-2(-805.611mil,2490.041mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.806mil < 10mil) Between Pad R54-1(-1413.039mil,738.755mil) on Top Layer And Text "R54'
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R54-1(-1413.039mil,738.755mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R54-2(-1413.039mil,667.889mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.54mil < 10mil) Between Pad TP15-TP(-1687.063mil,2667.961mil) on Top Layer And Text "U14'
Silk To Solder Mask Clearance Constraint: (9.791mil < 10mil) Between Pad U13-1(-8675.173mil,2599.106mil) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (9.797mil < 10mil) Between Pad U13-2(-8675.173mil,2579.421mil) on Top Layer And Text "C57'
Silk To Solder Mask Clearance Constraint: (8.009mil < 10mil) Between Pad U4-(-654mil,2980.505mil) on Top Overlay And Polygon Region (42 hole(s)) Top

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (3.858mil < 10mil) Between Text "1" (-3324.874mil,1410.598mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (-3536.527mil,496.744mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-2386.921mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-3305.228mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-4985.346mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-5906.606mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-7583.771mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-8505.031mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (-3174.323mil,855.012mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.189mil < 10mil) Between Text "BATTERY CONN" (-2256.516mil,817.452mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.189mil < 10mil) Between Text "BATTERY CONN" (-2256.516mil,817.452mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.475mil < 10mil) Between Text "C66" (-156.797mil,861.324mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.598mil < 10mil) Between Text "D3" (-1186.989mil,2548.283mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.598mil < 10mil) Between Text "D3" (-1186.989mil,2548.283mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.775mil < 10mil) Between Text "PWR CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.737mil < 10mil) Between Text "PWR CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.966mil < 10mil) Between Text "PWR CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track