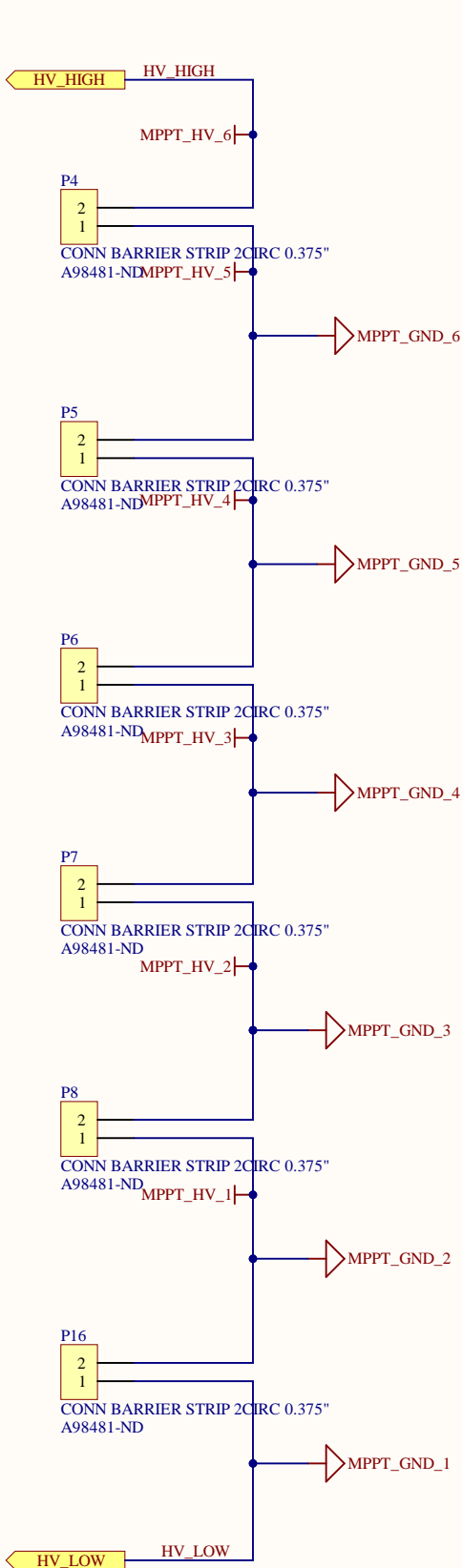
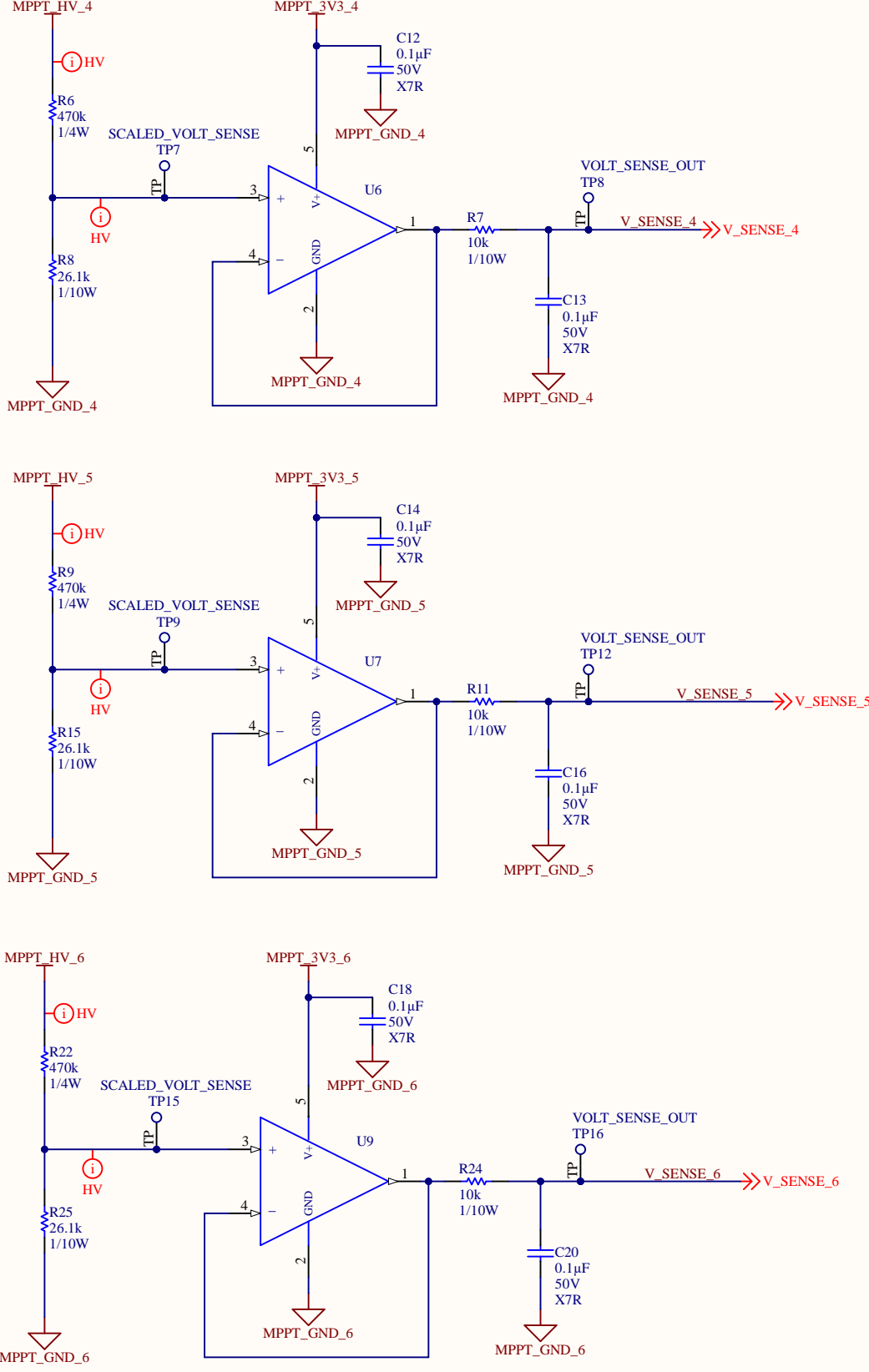
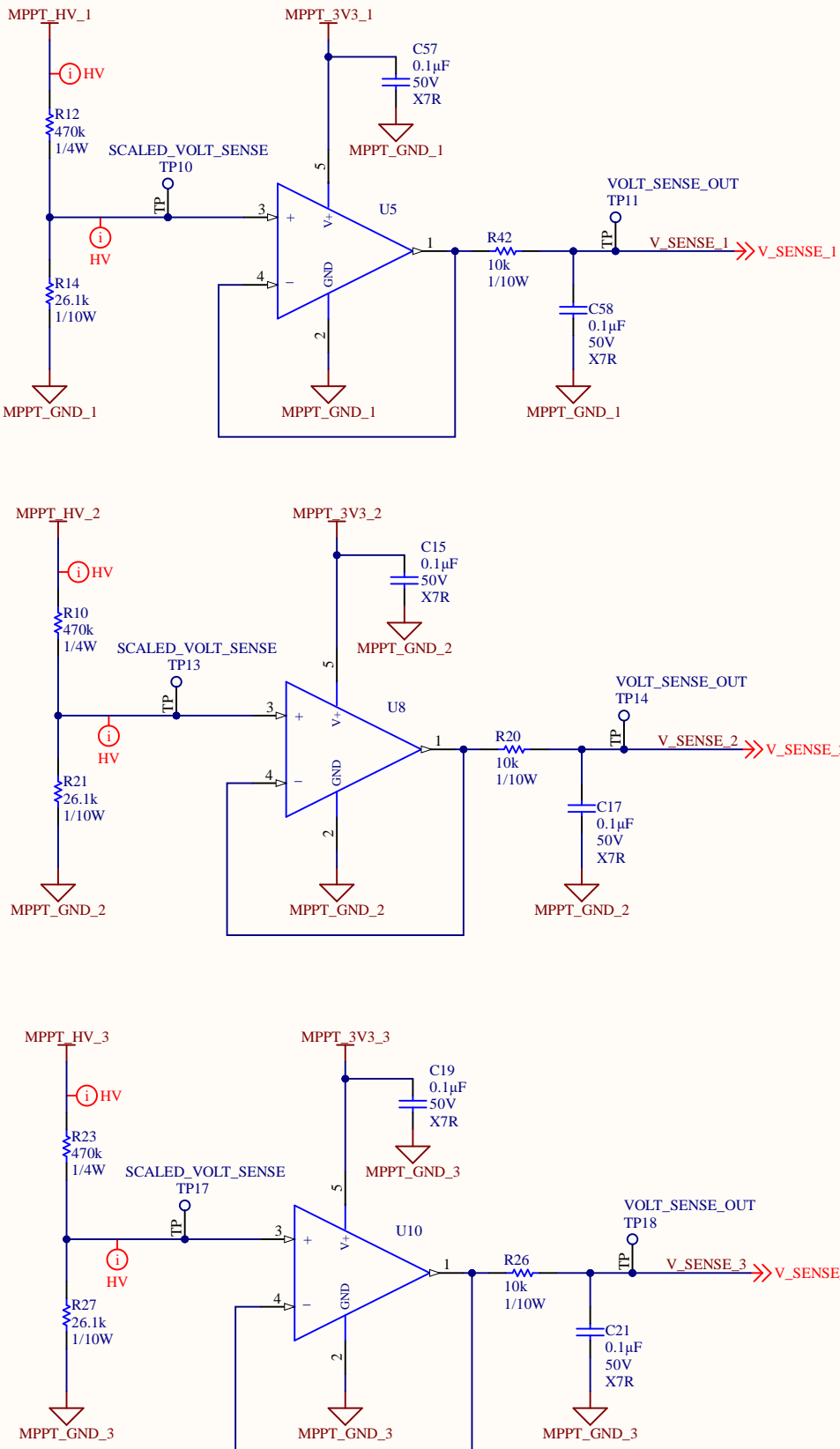
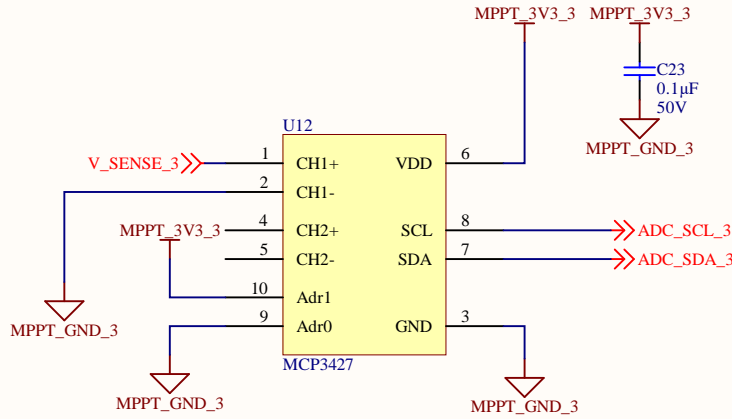
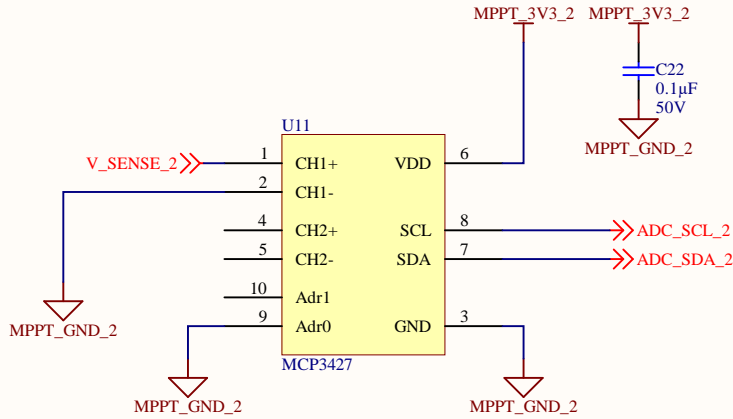
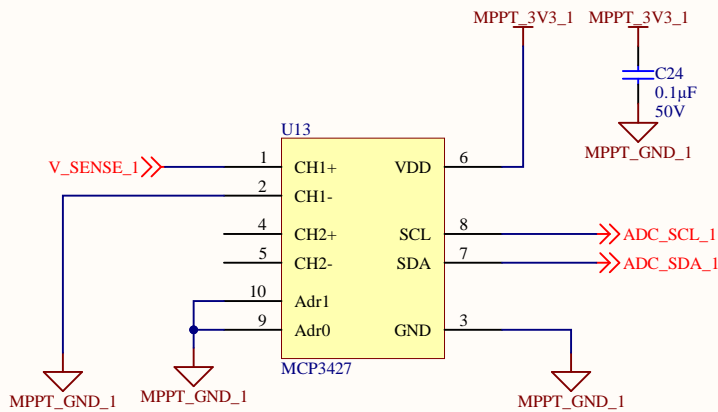


Voltage Sense



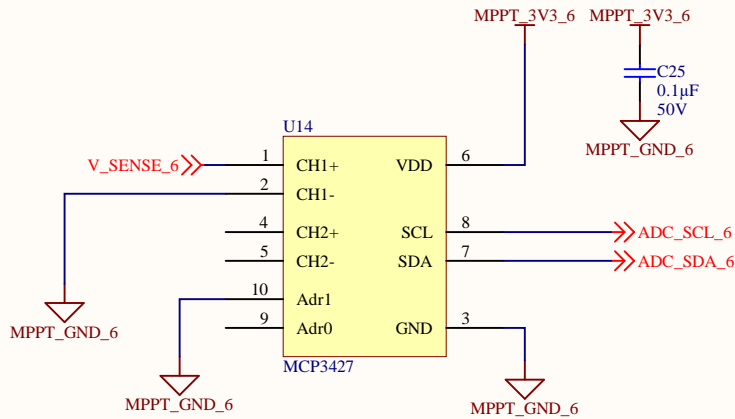
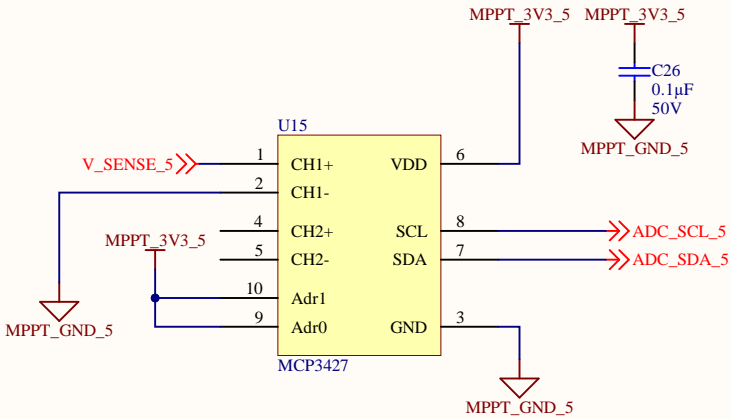
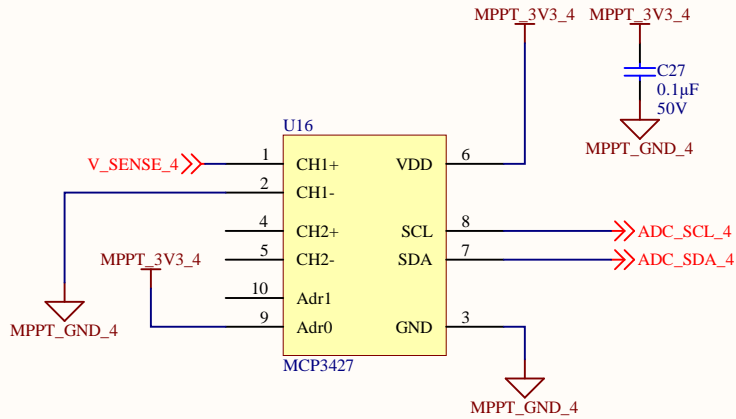
Pin2: Goes to + output terminal
Pin1: Goes to - output terminal





ADCs

I ² C Device Address Bits			Logic Status of Address Selection Pins	
A2	A1	A0	Adr0 Pin	Adr1 Pin
0	0	0	0 (Addr_Low)	0 (Addr_Low)
0	0	1	0 (Addr_Low)	Float
0	1	0	0 (Addr_Low)	1 (Addr_High)
1	0	0	1 (Addr_High)	0 (Addr_Low)
1	0	1	1 (Addr_High)	Float
1	1	0	1 (Addr_High)	1 (Addr_High)
0	1	1	Float	0 (Addr_Low)
1	1	1	Float	1 (Addr_High)
0	0	0	Float	Float



Make combination of pulled high, low and floating (for address pins)

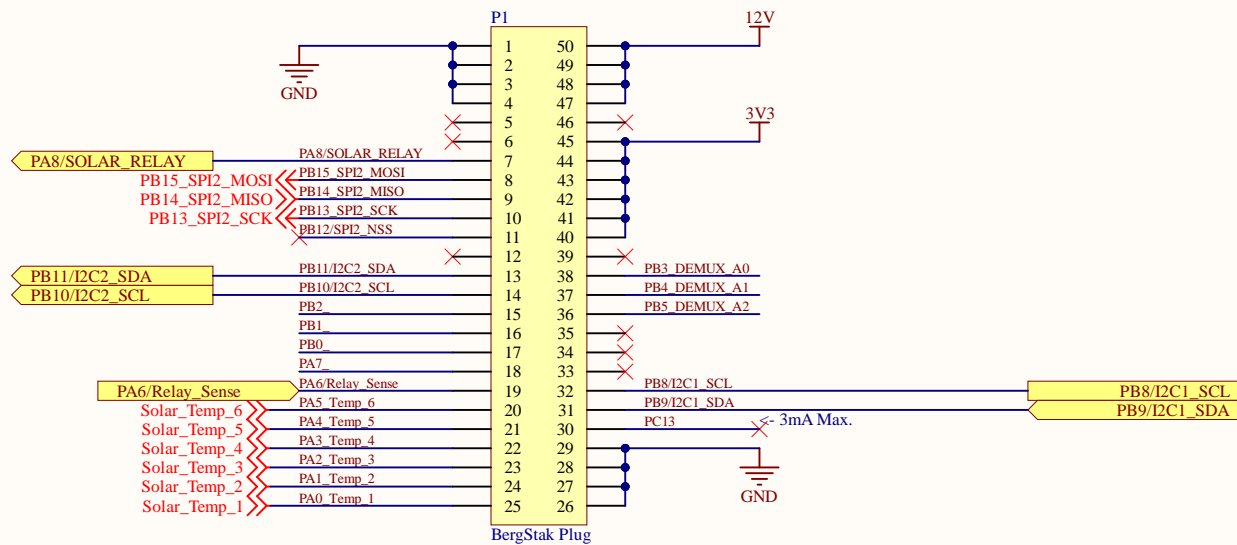
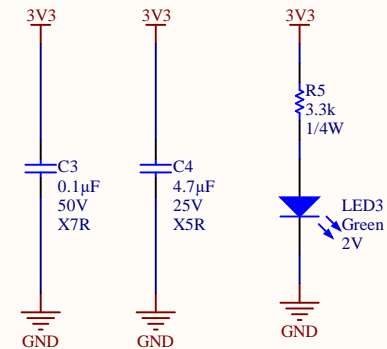
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DOCUMENT		*	
PART NUMBER		VARIANT	[No Variations]
DRAWN BY		REVISION	1.0
LAST MODIFIED		SHEET	* OF *

MIDNIGHT

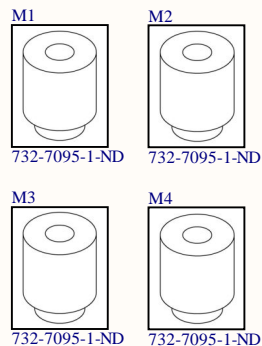
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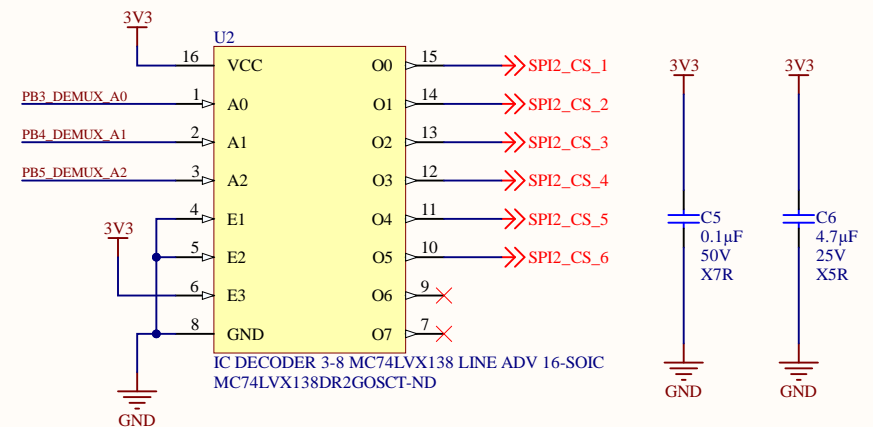
Add 6 gpio pins for slave select on spi, and 6 gpios for temperature sensing




Standoffs

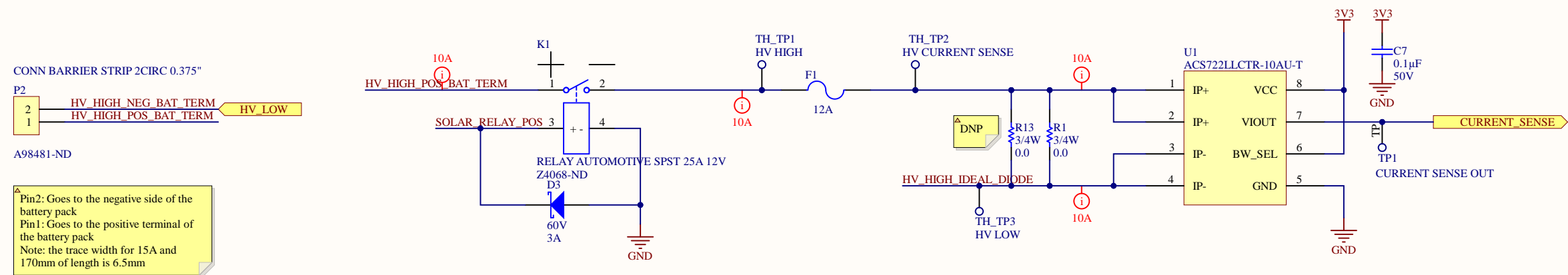


Solar Sense Rev 1.0
MSXIV LOGO
MSXIV LOGO

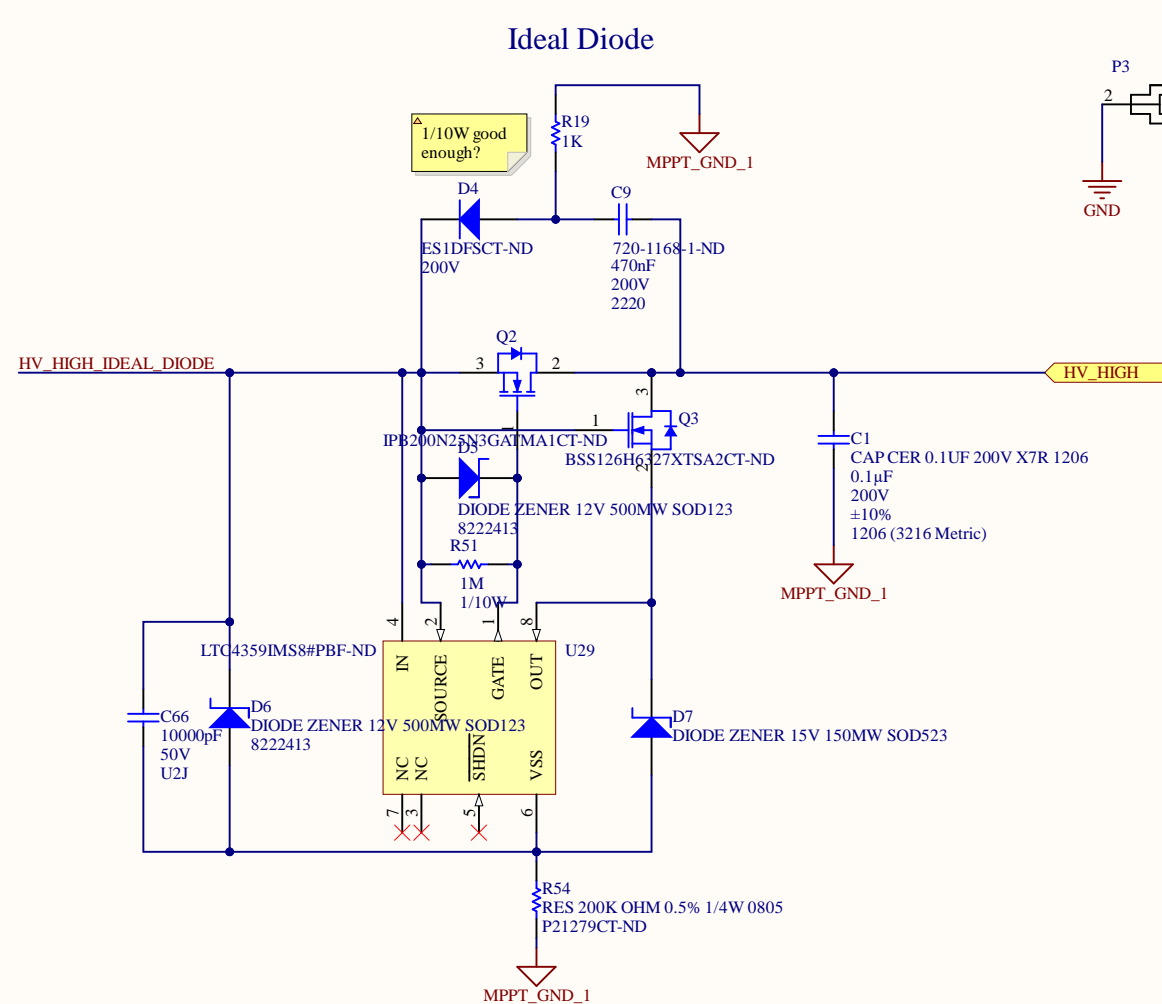


Project: <i>MSXIV_SolarSense.PrjPcb</i>		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: *		
Project AuthorAashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.0	
Date: 2020-02-23	Sheet * of *	
		Website: www.uwmidsun.com

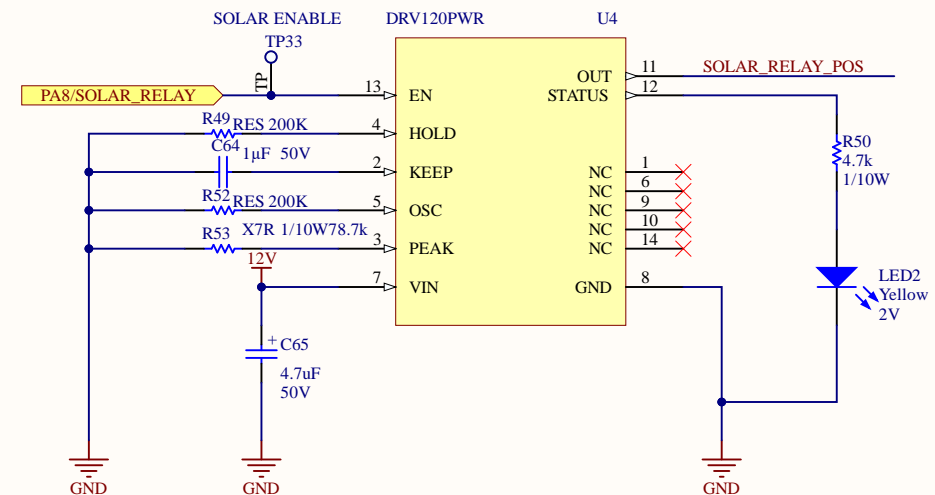
Passthrough - Current Sense, Fuse, and Relay



Ideal Diode

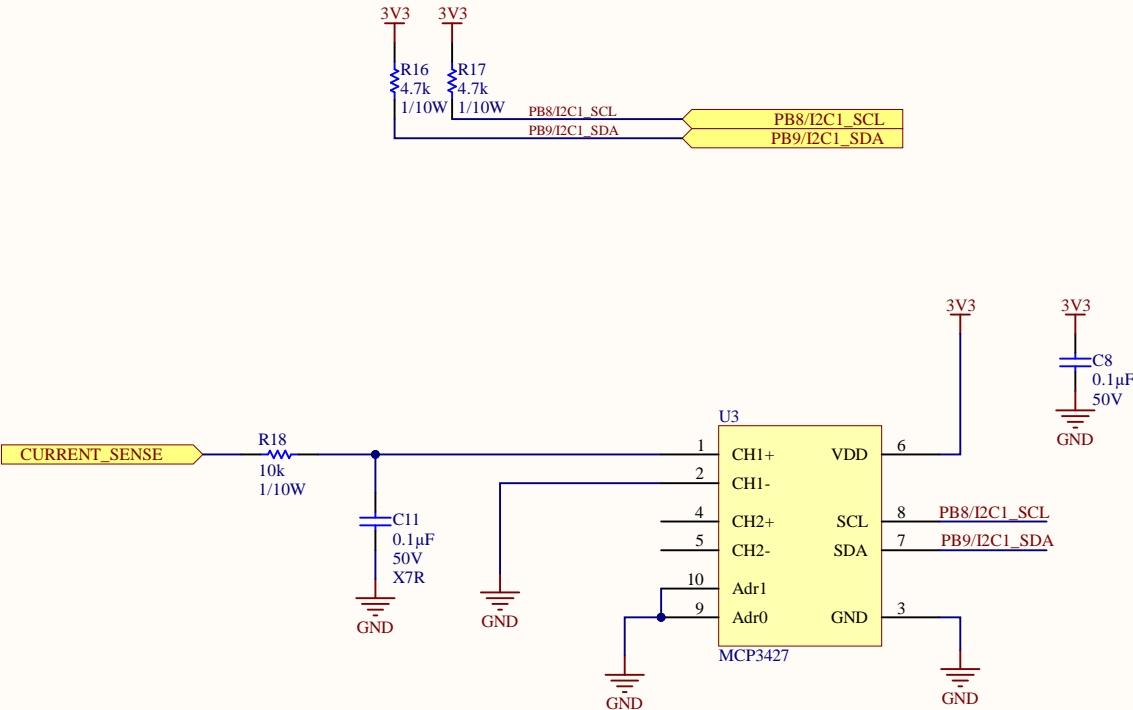


Relay coil low current driver

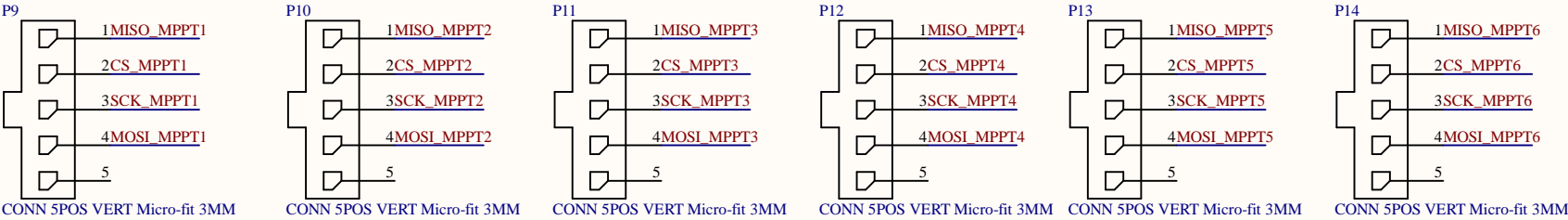
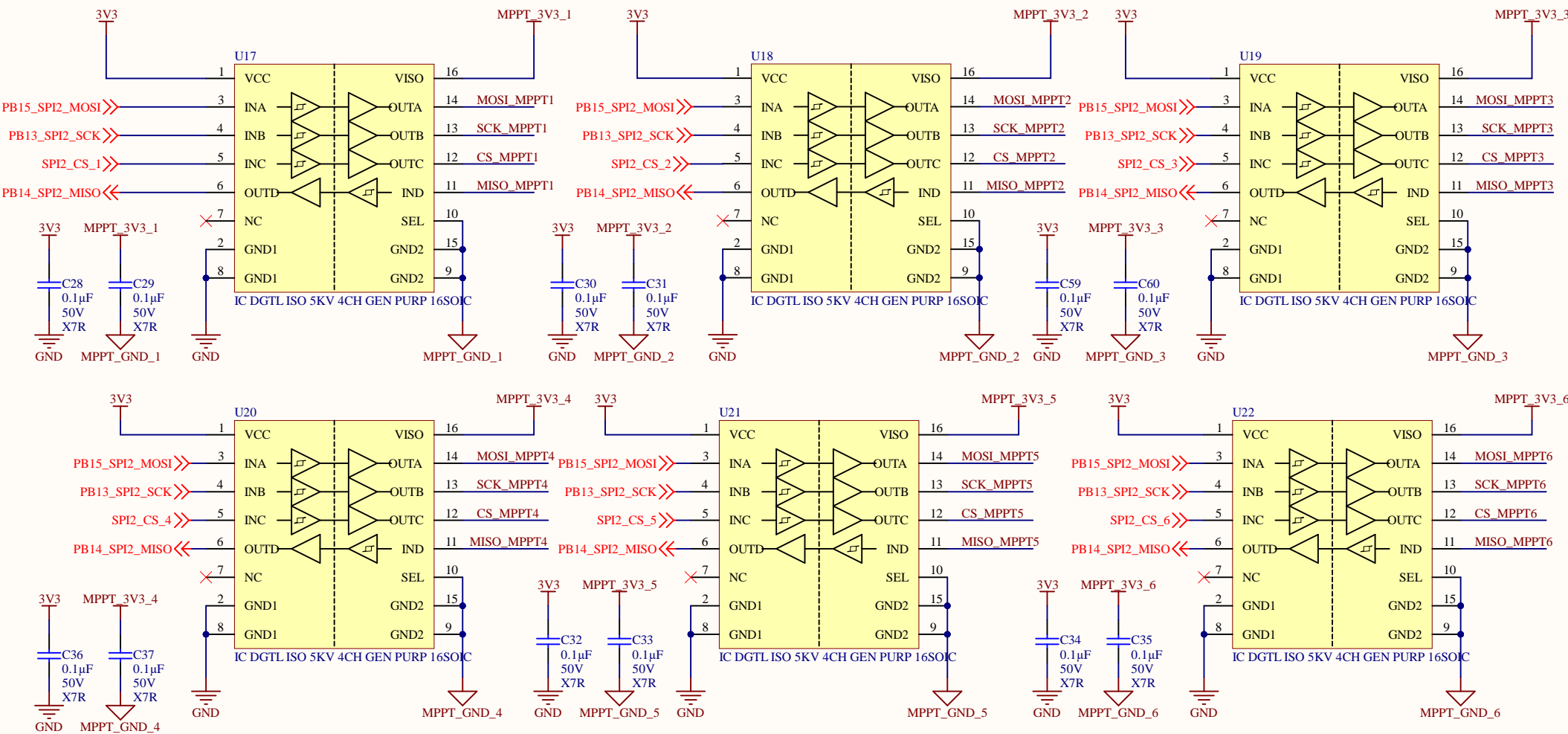


PROJECT		MSXIV_SolarSense.PrjPcb	
DOCUMENT *			
PART NUMBER		VARIANT	[No Variations]
DRAWN BY Aashmika Mali		REVISION	1.0
LAST MODIFIED 2020-02-23		SHEET *	OF *

I2C Interface (for Current Sense)



SPI Isolators



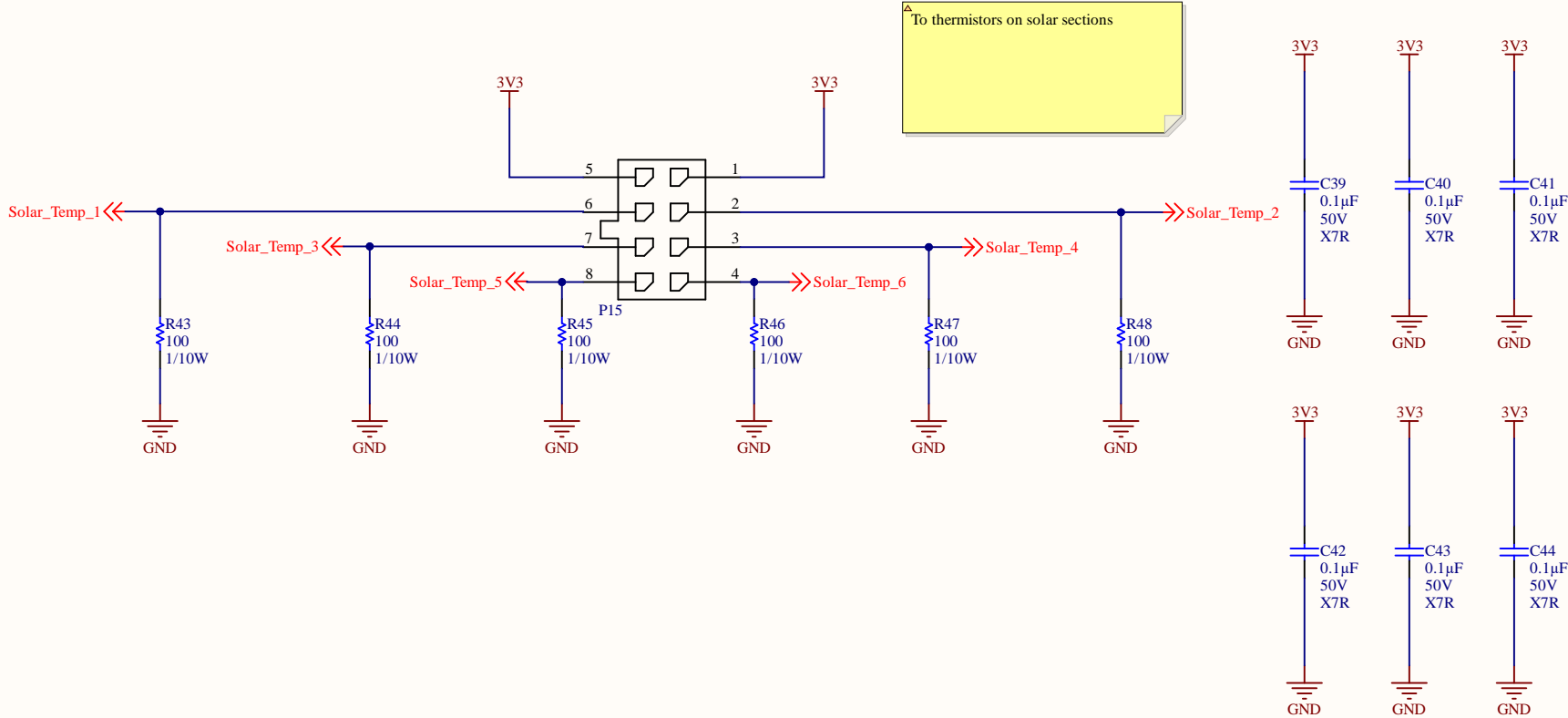
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DOCUMENT	*		
PART NUMBER	VARIANT	[No Variations]	
DRAWN BY	Aashmika Mali	REVISION	1.0
LAST MODIFIED	2020-02-23	SHEET	* OF *


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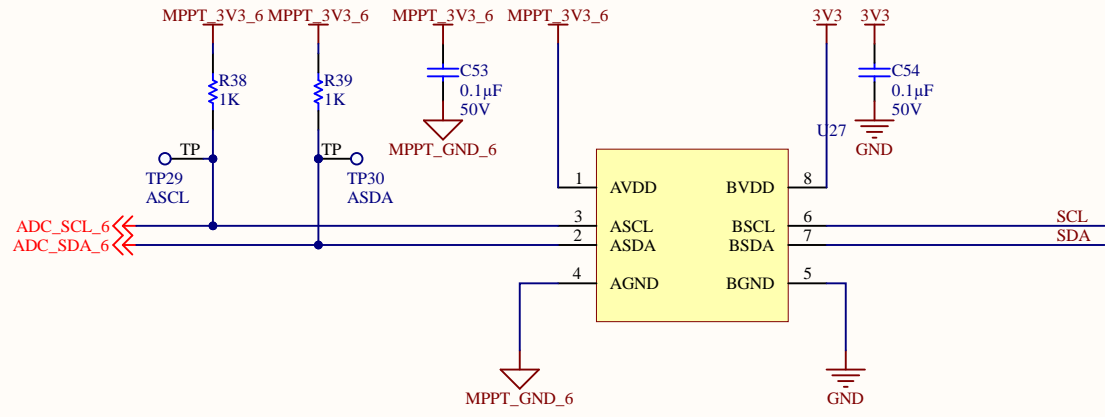
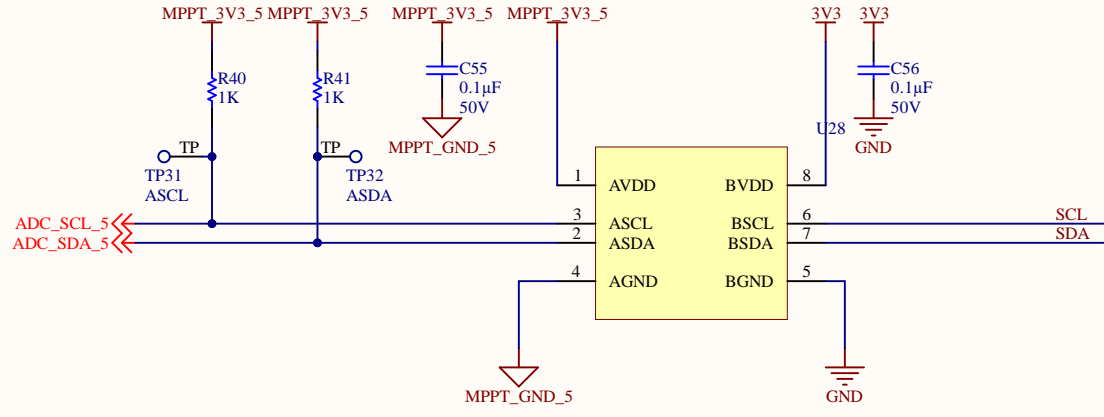
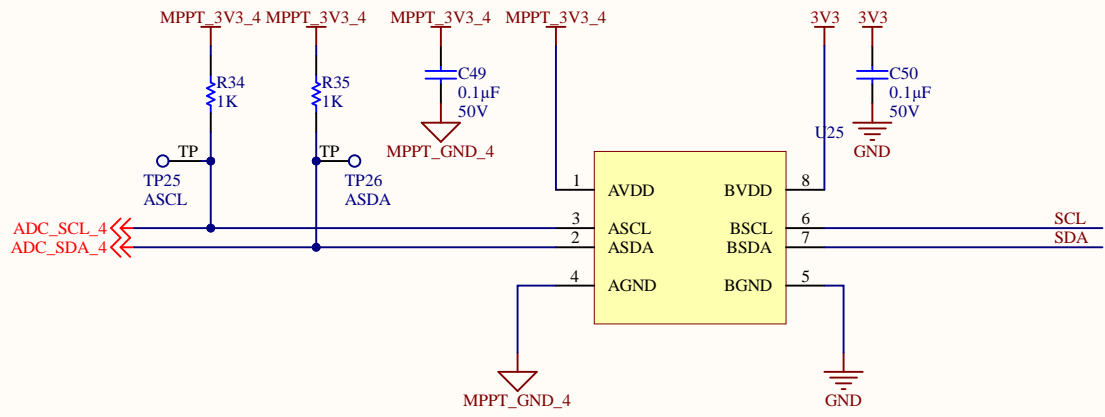
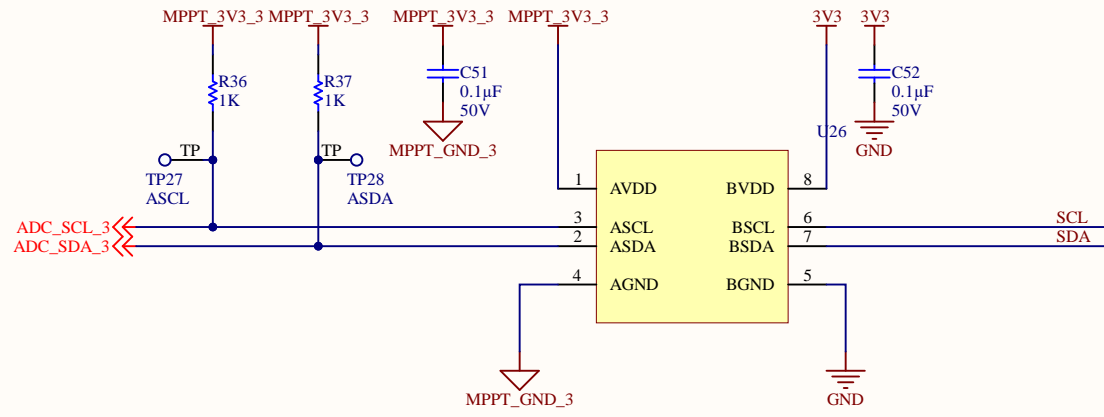
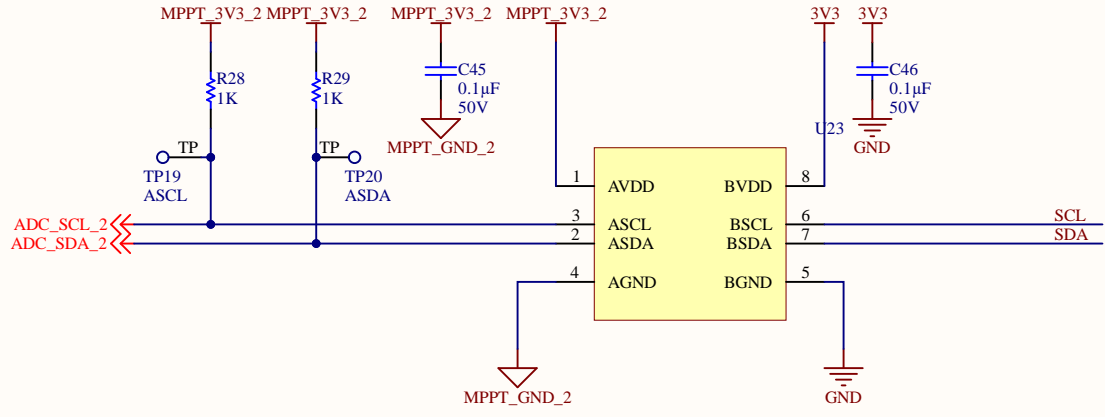
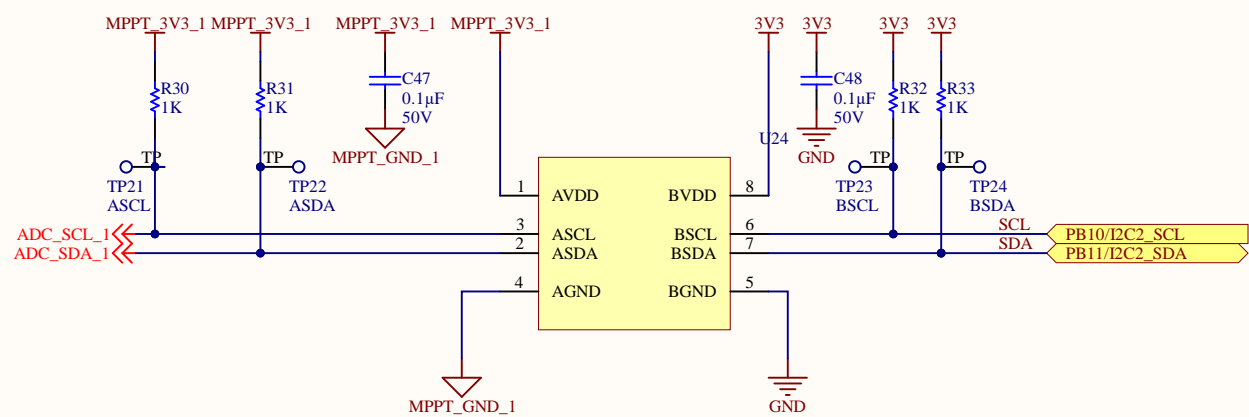
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hardware@uwmidsun.com

Temperature Sense for Array Sections



Project: <i>MSXIV_SolarSense.PrjPcb</i>		
Title: *		
Project AuthorAashmika Mali		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 1.0	
Date: 2020-02-23	Sheet* of *	

I2C Isolators for V-Sense



PROJECT		MSXIV_SolarSense.PrjPcb	
DOCUMENT		*	
PART NUMBER	VARIANT	[No Variations]	
DRAWN BY	REVISION	Aashmika Mali 1.0	
LAST MODIFIED	SHEET	2020-02-23 * OF *	

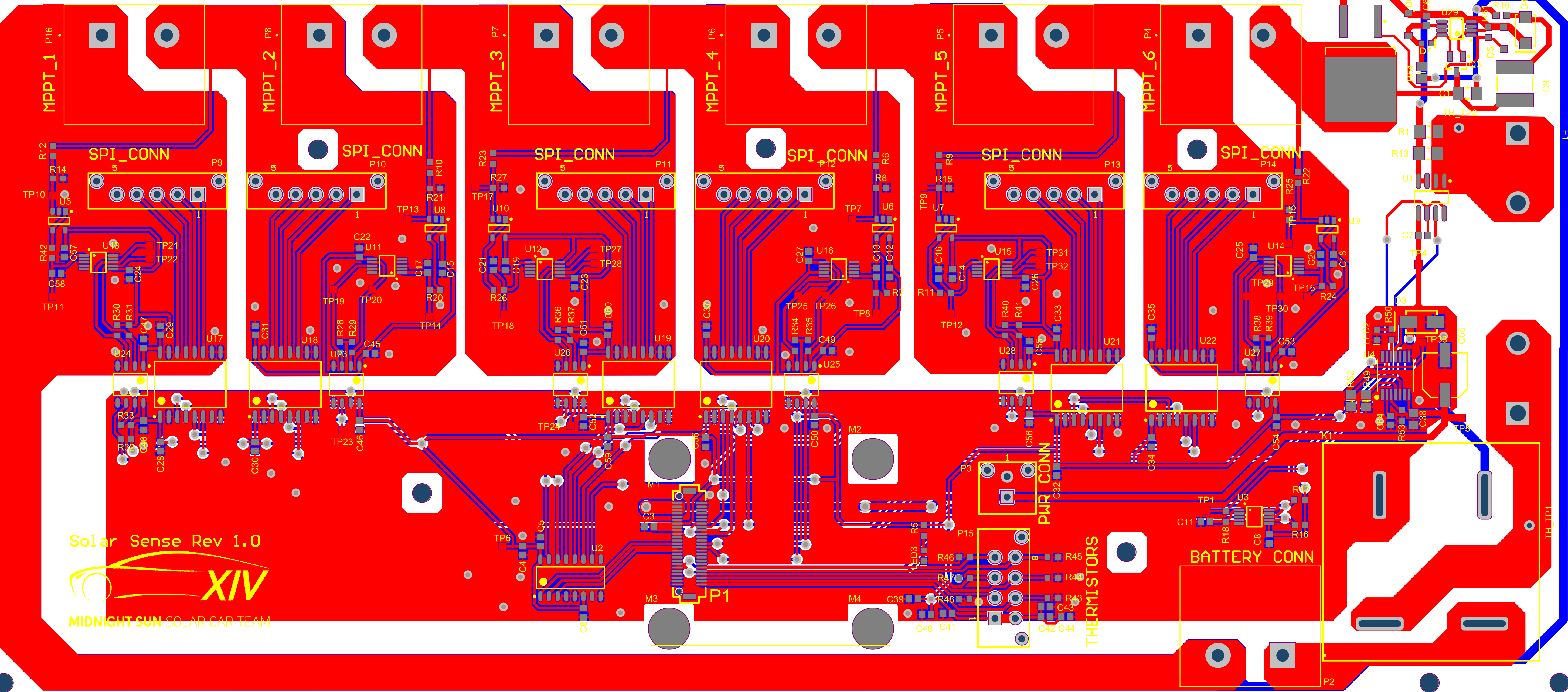
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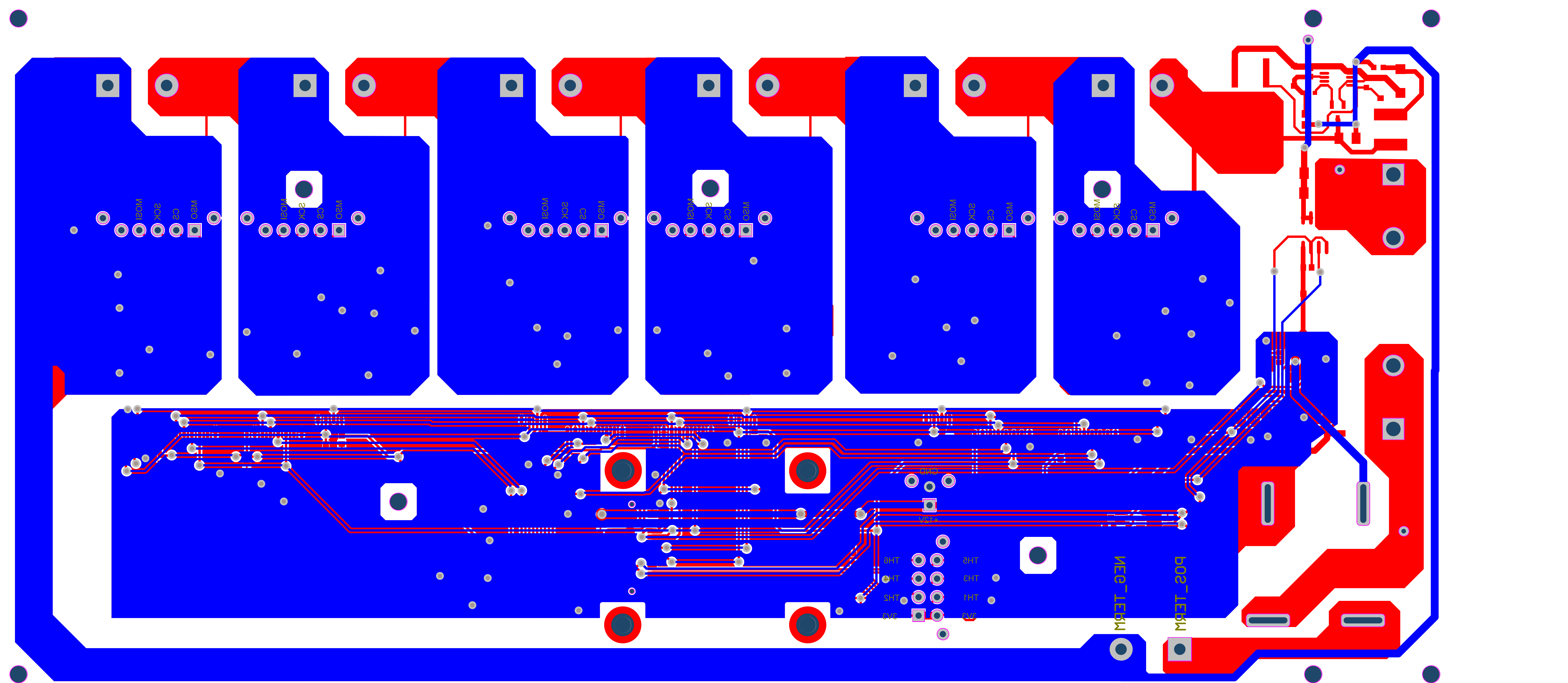
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Solar Sense Rev 1.0

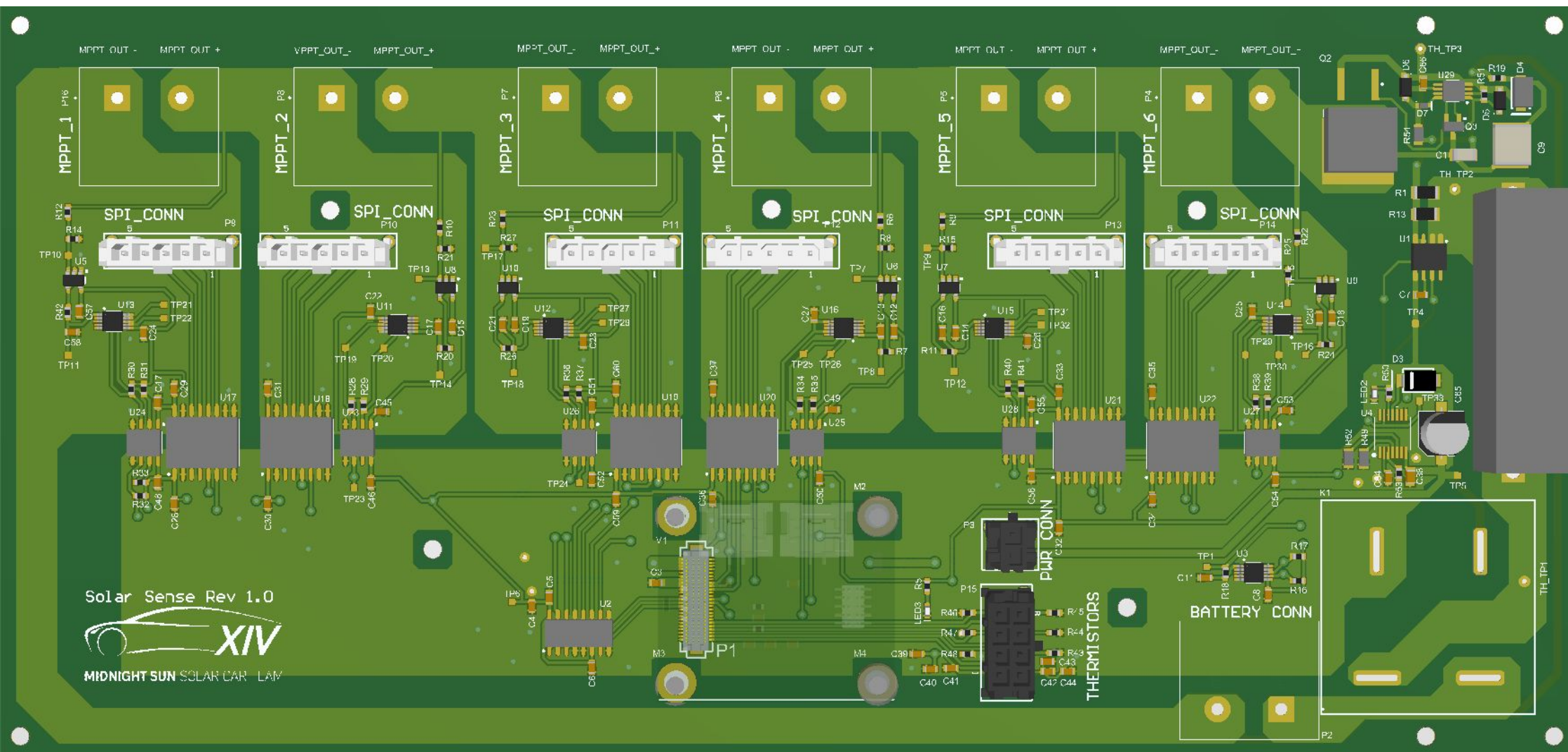




Solar Sense Rev 1.0



MIDNIGHT SUN SOLAR CAR LAM



Electrical Rules Check Report

[illegible]

Class	Document	Message
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Warning	ADCs.SchDoc	Off grid Pin U13-4 at 1658.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-5 at 1658.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-6 at 3108.11mil,8044.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-7 at 3108.11mil,7544.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-8 at 3108.11mil,7694.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-9 at 1658.11mil,7194.41mil
Warning	ADCs.SchDoc	Off grid Pin U13-10 at 1658.11mil,7344.41mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-1 at 6774.41mil,7051.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-2 at 6774.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-3 at 6774.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-4 at 6774.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-5 at 6774.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-6 at 6774.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-7 at 6774.41mil,6051.811mil
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Warning	SPI_Interface.SchDoc	Off grid Pin U18-11 at 8574.41mil,6251.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-12 at 8574.41mil,6451.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-13 at 8574.41mil,6651.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-14 at 8574.41mil,6851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-15 at 8574.41mil,5851.811mil
Warning	SPI_Interface.SchDoc	Off grid Pin U18-16 at 8574.41mil,7051.811mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 4099.606mil,5389.764mil
Warning	TemperatureSense.SchDoc	Off grid Power Object 3V3 at 5899.606mil,5389.764mil
Warning	SPI_Interface.SchDoc	Off grid Power Object 3V3 at 6174.41mil,7351.811mil
Warning	SPI_Interface.SchDoc	Off grid Power Object GND at 6774.41mil,5351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3218.11mil,8674.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_3V3_1 at 3818.11mil,8674.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_3V3_2 at 9074.41mil,7351.811mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 818.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3468.11mil,7074.41mil
Warning	ADCs.SchDoc	Off grid Power Object MPPT_GND_1 at 3818.11mil,8374.41mil
Warning	SPI_Interface.SchDoc	Off grid Power Object MPPT_GND_2 at 8574.41mil,5351.811mil
Warning	Controller_Board_Interface.SchDoc	Off grid Solar Sense Rev 1.0 at 4505.679mil,2561.84mil
Warning	ADCs.SchDoc	Off grid U13 at 1958.11mil,8194.41mil
Warning	SPI_Interface.SchDoc	Off grid U18 at 7474.41mil,6651.811mil

Design Rules Verification Report

Filename : C:\Users\Aashmika Mali\Documents\First Year\Midnight Sun\hardware\MSXIV_

Warnings 0
Rule Violations 146

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=70mil) (Preferred=15mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4,	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	23
Hole To Hole Clearance (Gap=10mil) (All),(All)	4
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	30
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	75
Silk to Silk (Clearance=10mil) (All),(All)	14
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Total	146

Hole Size Constraint (Min=1mil) (Max=100mil) (All)	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-118.111mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-2218.858mil,3215.5mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-2629.063mil,877.5mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4099.52mil,1418.004mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4099.52mil,433.752mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-4720.984mil,3221.5mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5280.622mil,1418.004mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-5280.622mil,433.752mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-6713.063mil,1220.5mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-7316.102mil,3215.5mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-871.173mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-871.173mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9138.89mil,118.11mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (106.299mil > 100mil) Pad Free-(-9138.89mil,4306.39mil) on Multi-Layer Actual Hole Size = 106.299mil	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-1(-552.85mil,462.583mil) on Multi-Layer Actual Slot Hole Height = 248.031mi	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-2(-1159.15mil,462.583mil) on Multi-Layer Actual Slot Hole Height = 248.031mi	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-3(-550.882mil,1208.646mil) on Multi-Layer Actual Slot Hole Height = 248.031mi	
Hole Size Constraint: (248.031mil > 100mil) Pad K1-4(-1161.118mil,1208.646mil) on Multi-Layer Actual Slot Hole Height = 248.031mi	
Hole Size Constraint: (145.669mil > 100mil) Pad M1-(-5277.468mil,1419.409mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M2-(-4099.52mil,1418.004mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M3-(-5280.622mil,433.752mil) on Multi-Layer Actual Hole Size = 145.669mil	
Hole Size Constraint: (145.669mil > 100mil) Pad M4-(-4099.52mil,433.752mil) on Multi-Layer Actual Hole Size = 145.669mil	

Hole To Hole Clearance (Gap=10mil) (All),(All)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4099.52mil,1418.004mil) on Multi-Layer And Pad M2-(-4099.52mil,1418.004mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-4099.52mil,433.752mil) on Multi-Layer And Pad M4-(-4099.52mil,433.752mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5280.622mil,1418.004mil) on Multi-Layer And Pad M3-(-5280.622mil,433.752mil)	
Hole To Hole Clearance Constraint: (Collision < 10mil) Between Pad Free-(-5280.622mil,433.752mil) on Multi-Layer And Pad M3-(-5280.622mil,433.752mil)	

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (9.709mil < 10mil) Between Pad C4-1(-6129mil,913.575mil) on Top Layer And Via (-6130mil,973mil) from Top
Minimum Solder Mask Sliver Constraint: (6.727mil < 10mil) Between Pad C43-1(-3124.984mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (6.727mil < 10mil) Between Pad C43-2(-3071.834mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (8.198mil < 10mil) Between Pad C43-2(-3071.834mil,560.773mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5162.512mil,1232.964mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (4.145mil < 10mil) Between Pad P1-(-5162.512mil,618.791mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U10-1(-6229.441mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U10-2(-6266.842mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-1(-1144.272mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-10(-1041.909mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-10(-1041.909mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-11(-1067.5mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-12(-1093.091mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-13(-1118.681mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-2(-1118.681mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-3(-1093.091mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-4(-1067.5mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-5(-1041.909mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.59mil < 10mil) Between Pad U4-6(-1016.319mil,1791.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (3.591mil < 10mil) Between Pad U4-8(-990.728mil,2013.937mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U5-1(-8780.031mil,2856.232mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U5-2(-8817.433mil,2856.232mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U6-1(-4003.063mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U6-2(-4040.464mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U7-1(-3637.905mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U7-2(-3675.307mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U8-1(-6595.386mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U8-2(-6632.787mil,2810.72mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U9-1(-1426.291mil,2805.799mil) on Top Layer And Pac
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U9-2(-1463.693mil,2805.799mil) on Top Layer And Pac

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-471.89mil,3784.744mil) on Top Overlay And Pad D5-1(-440mil,3798.13mil)
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-928.37mil,3855.343mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Arc (-961.11mil,4018.256mil) on Top Overlay And Pad D6-1(-993mil,4004.87mil)
Silk To Solder Mask Clearance Constraint: (8.995mil < 10mil) Between Pad C15-1(-6595.386mil,2553.24mil) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (7.941mil < 10mil) Between Pad C15-2(-6595.386mil,2500.09mil) on Top Layer And Text "C15"
Silk To Solder Mask Clearance Constraint: (8.548mil < 10mil) Between Pad C38-1(-965.421mil,1685.346mil) on Top Layer And Text "C38"
Silk To Solder Mask Clearance Constraint: (8.104mil < 10mil) Between Pad C38-2(-965.421mil,1616.449mil) on Top Layer And Text "C38"
Silk To Solder Mask Clearance Constraint: (9.475mil < 10mil) Between Pad C6-2(-5776.488mil,498.713mil) on Top Layer And Text "C6"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-782.5mil,1788.858mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-1(-782.5mil,1788.858mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.237mil < 10mil) Between Pad C65-2(-782.5mil,2021.142mil) on Top Layer And Text "TP33"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-782.5mil,2021.142mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad C65-2(-782.5mil,2021.142mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-837.5mil,2214mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-1(-837.5mil,2214mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-994.98mil,2214mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.535mil < 10mil) Between Pad D3-2(-994.98mil,2214mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (2.839mil < 10mil) Between Pad D7-2(-859.472mil,3831.721mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED2-2(-1176.106mil,2108.913mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.213mil < 10mil) Between Pad LED3-2(-3804.244mil,827.453mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M3-(-5280.622mil,433.752mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.408mil < 10mil) Between Pad M4-(-4099.52mil,433.752mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P10-0(-6969.598mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-6969.598mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P10-0(-7678.26mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P10-0(-7678.26mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.78mil < 10mil) Between Pad P1-1(-5091.646mil,1162.097mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P11-0(-5292.433mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-5292.433mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P11-0(-6001.094mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P11-0(-6001.094mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P12-0(-4371.173mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-4371.173mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P12-0(-5079.834mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P12-0(-5079.834mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.767mil < 10mil) Between Pad P1-25(-5091.646mil,689.657mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.4mil < 10mil) Between Pad P1-26(-5233.378mil,689.657mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P13-0(-2691.055mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-2691.055mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P13-0(-3399.716mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P13-0(-3399.716mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P14-0(-1772.748mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-1772.748mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P14-0(-2481.409mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P14-0(-2481.409mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3235.74mil,374.697mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.376mil < 10mil) Between Pad P15-0(-3235.74mil,374.697mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P15-0(-3235.74mil,965.248mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.918mil < 10mil) Between Pad P15-0(-3235.74mil,965.248mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.401mil < 10mil) Between Pad P1-50(-5233.378mil,1162.097mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P3-0(-3198.89mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3198.89mil,1353.118mil) on Multi-Layer And Track

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P3-0(-3435.11mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P3-0(-3435.11mil,1353.118mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (8.4mil < 10mil) Between Pad P9-0(-7890.858mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-7890.858mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (7.053mil < 10mil) Between Pad P9-0(-8599.519mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (9.281mil < 10mil) Between Pad P9-0(-8599.519mil,3031.39mil) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-1(-1684.549mil,2803.988mil) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R25-2(-1684.549mil,2865.012mil) on Top Layer And Text "TP15"
Silk To Solder Mask Clearance Constraint: (2.51mil < 10mil) Between Pad R28-2(-7190.071mil,2037.098mil) on Top Layer And Text "U23"
Silk To Solder Mask Clearance Constraint: (9.584mil < 10mil) Between Pad R38-2(-1875.11mil,2056.783mil) on Top Layer And Text "U27"
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R49-1(-1238.073mil,1720.915mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R49-2(-1238.073mil,1791.781mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 10mil) Between Pad R50-2(-1091.5mil,2171.943mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R52-1(-1328.461mil,1722.113mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R52-2(-1328.461mil,1792.979mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (9.653mil < 10mil) Between Pad R53-1(-1032.5mil,1639.937mil) on Top Layer And Text "R53"
Silk To Solder Mask Clearance Constraint: (8.513mil < 10mil) Between Pad R54-1(-917mil,3696.866mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (7.874mil < 10mil) Between Pad R54-2(-917mil,3626mil) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (6.54mil < 10mil) Between Pad TP15-TP(-1687.063mil,2667.961mil) on Top Layer And Text "U14"
Silk To Solder Mask Clearance Constraint: (8.169mil < 10mil) Between Pad TP33-TP(-910mil,2095mil) on Top Layer And Text "TP33"
Silk To Solder Mask Clearance Constraint: (9.791mil < 10mil) Between Pad U13-1(-8675.173mil,2599.106mil) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (9.797mil < 10mil) Between Pad U13-2(-8675.173mil,2579.421mil) on Top Layer And Text "C57"
Silk To Solder Mask Clearance Constraint: (8.009mil < 10mil) Between Pad U4-(-1178mil,1776.687mil) on Top Overlay And Polygon Region (83 hole(s))

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (3.858mil < 10mil) Between Text "1" (-3324.874mil,1410.598mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.806mil < 10mil) Between Text "1" (-3536.527mil,496.744mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-2386.921mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-3305.228mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-4985.346mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-5906.606mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-7583.771mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "5" (-8505.031mil,3092.807mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (7.795mil < 10mil) Between Text "8" (-3174.323mil,855.012mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (2.64mil < 10mil) Between Text "P12" (-4406.324mil,3113.214mil) on Top Overlay And Text "SPI_CONN"
Silk To Silk Clearance Constraint: (7.775mil < 10mil) Between Text "PWR_CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.737mil < 10mil) Between Text "PWR_CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (8.966mil < 10mil) Between Text "PWR_CONN" (-3073.89mil,1045.52mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.511mil < 10mil) Between Text "R53" (-1013.547mil,1526.306mil) on Top Overlay And Track