

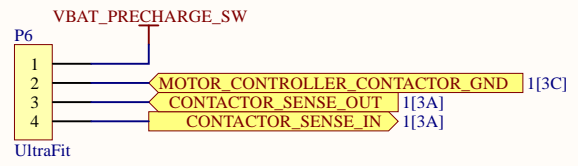
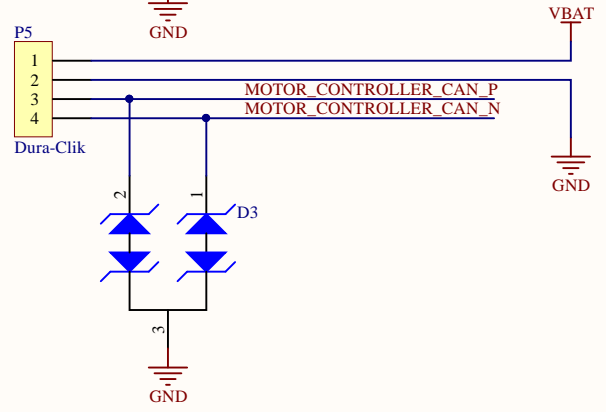
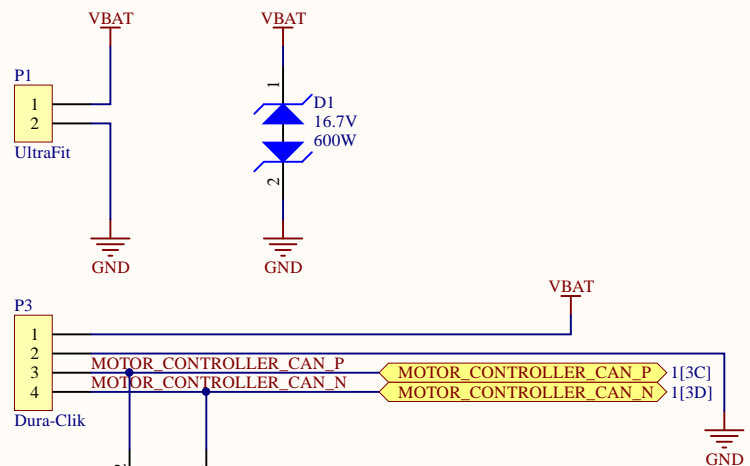
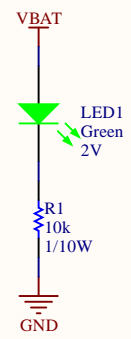
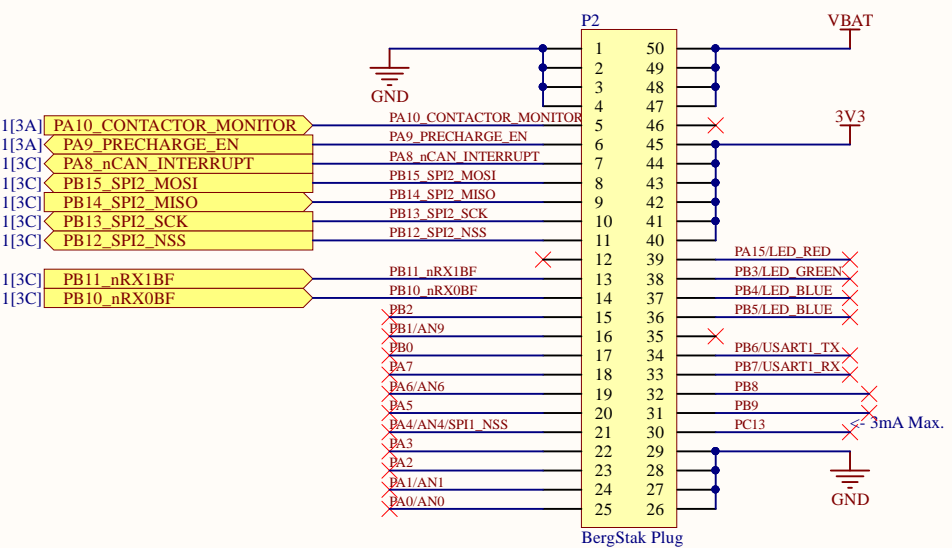
PROJECT	PreCharge.PrjPcb	
DOCUMENT	Title	
PART NUMBER	MS14004	VARIANT 01 - Standard
DRAWN BY	Taiping Li	REVISION 4.0
LAST MODIFIED	2019-01-18	SHEET 1 OF 6

MIDNIGHT

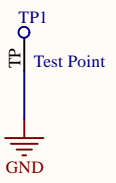
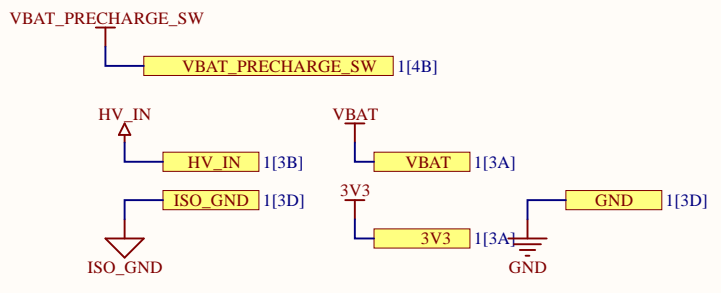
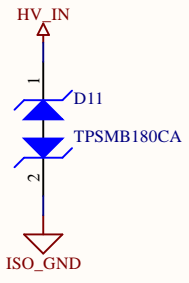
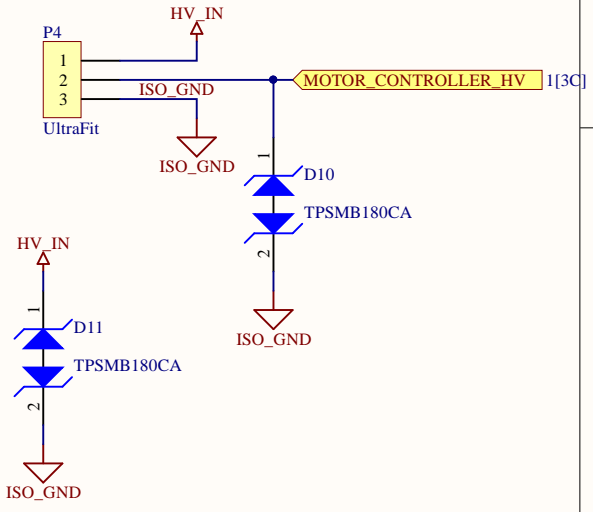
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Connectors



HV Connector



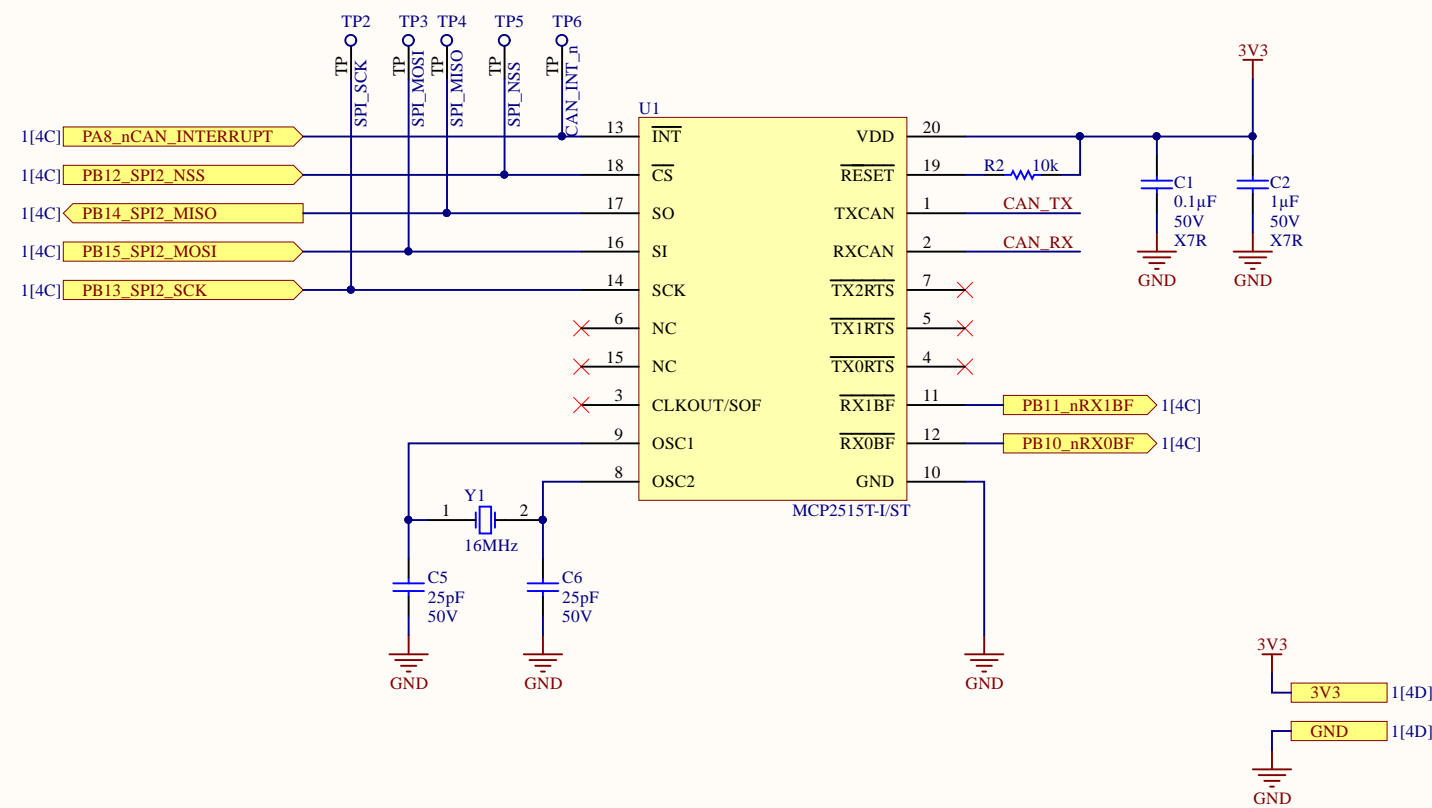
PROJECT	PreCharge.PrjPcb	
DOCUMENT	Motor Interface - Connectors	
PART NUMBER	MS14004	VARIANT 01 - Standard
DRAWN BY	Taiping Li	REVISION 4.0
LAST MODIFIED	2019-01-18	SHEET 2 OF 6

MIDNIGHT

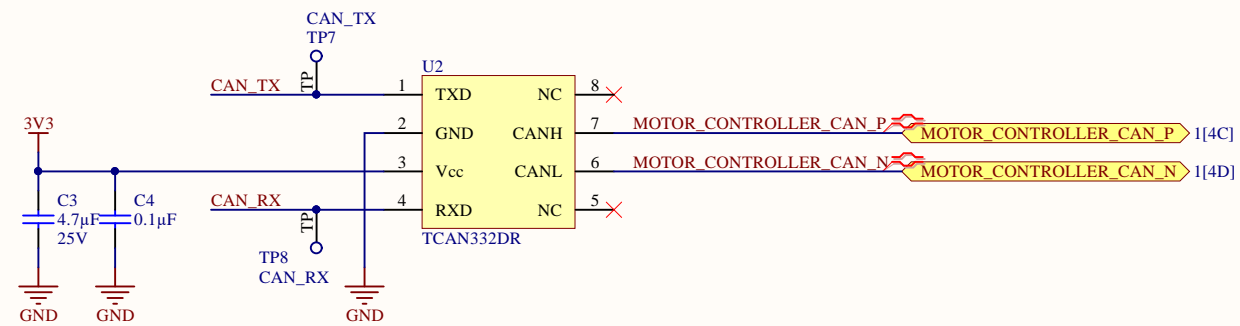
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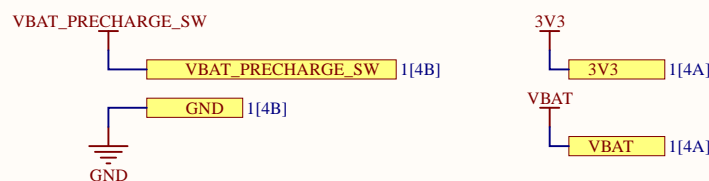
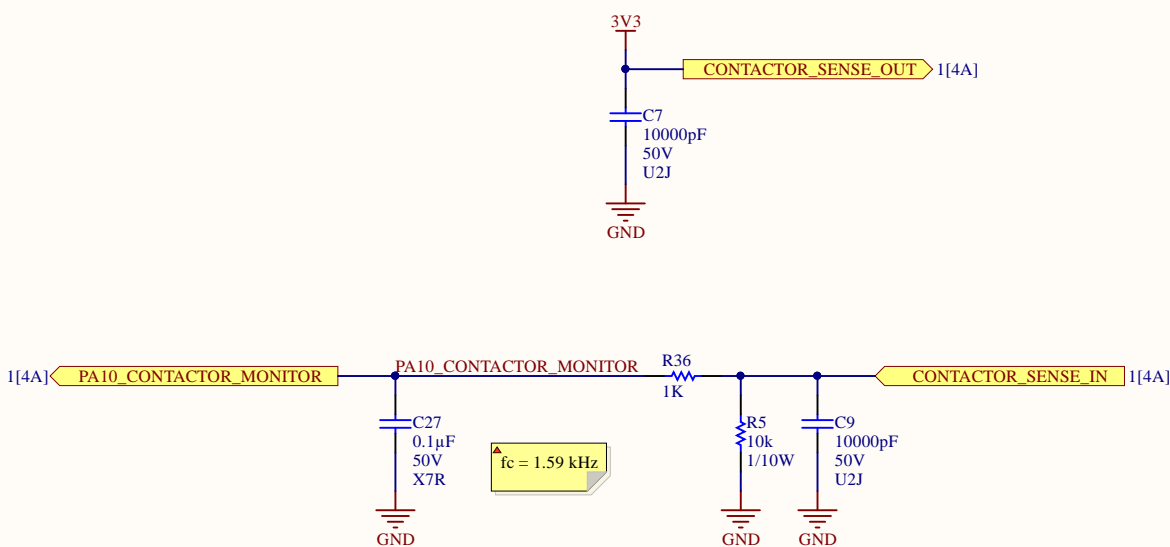
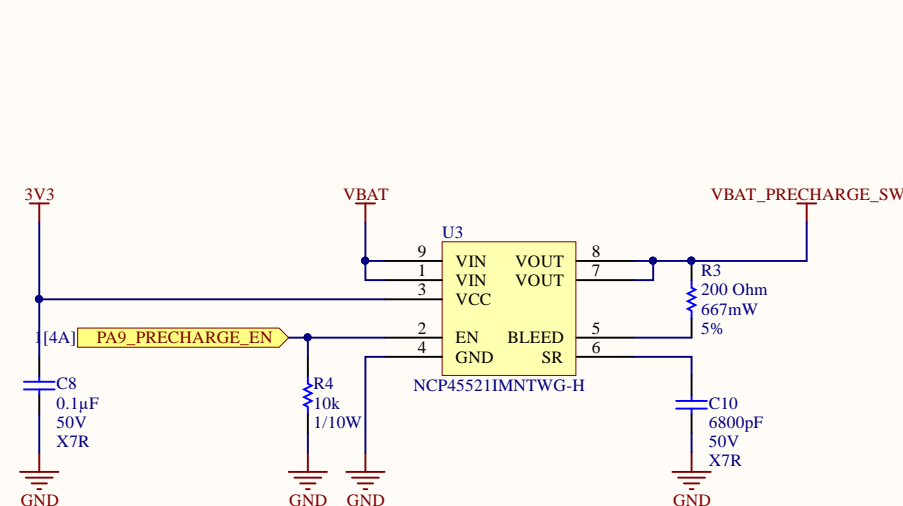
CAN Controller



CAN Transceiver



Precharge Control

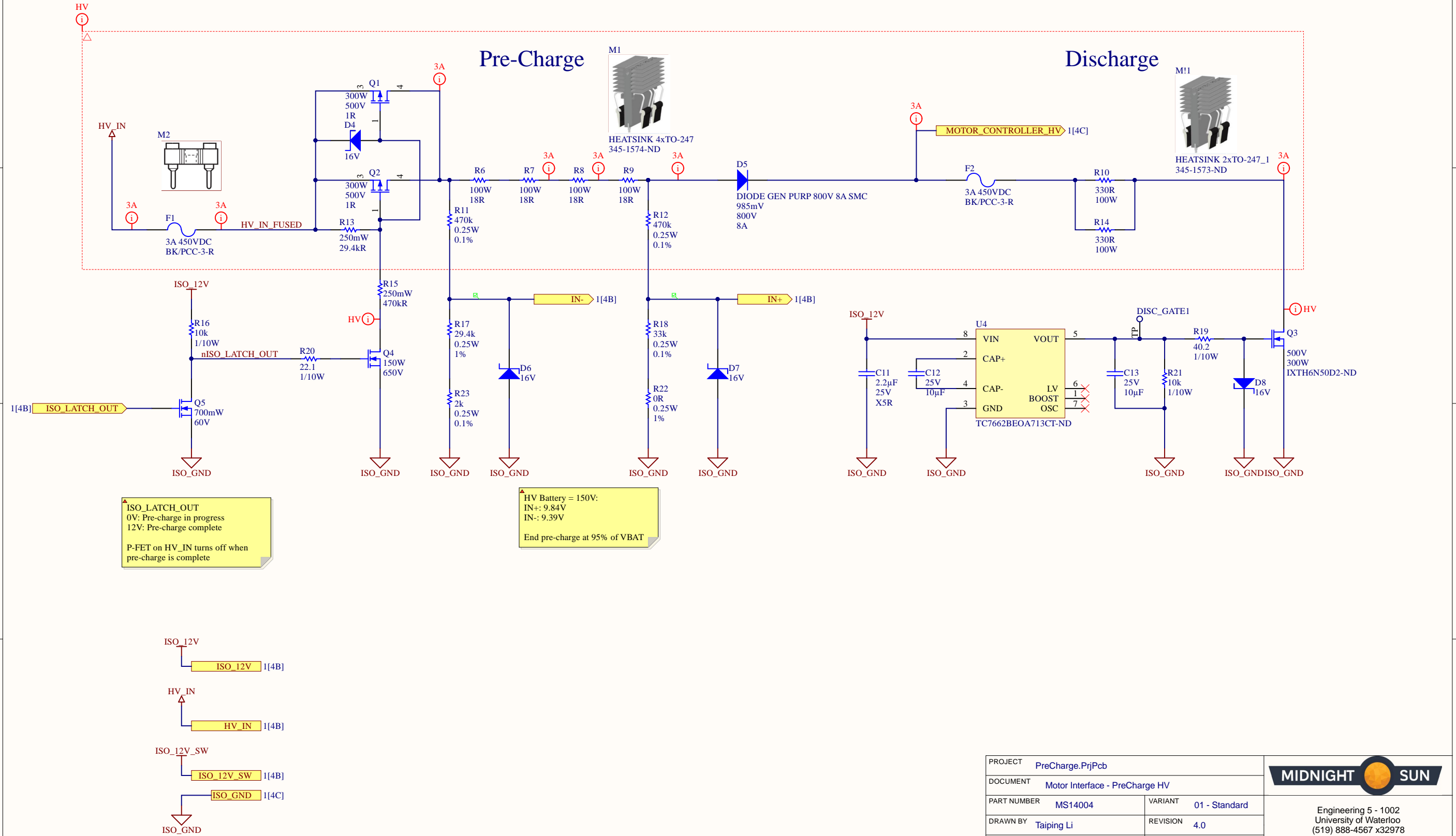


PROJECT	PreCharge.PrjPcb	
DOCUMENT	Motor Interface - PreCharge Interface	
PART NUMBER	MS14004	VARIANT 01 - Standard
DRAWN BY	Taiping Li	REVISION 4.0
LAST MODIFIED	2019-01-18	SHEET 4 OF 6

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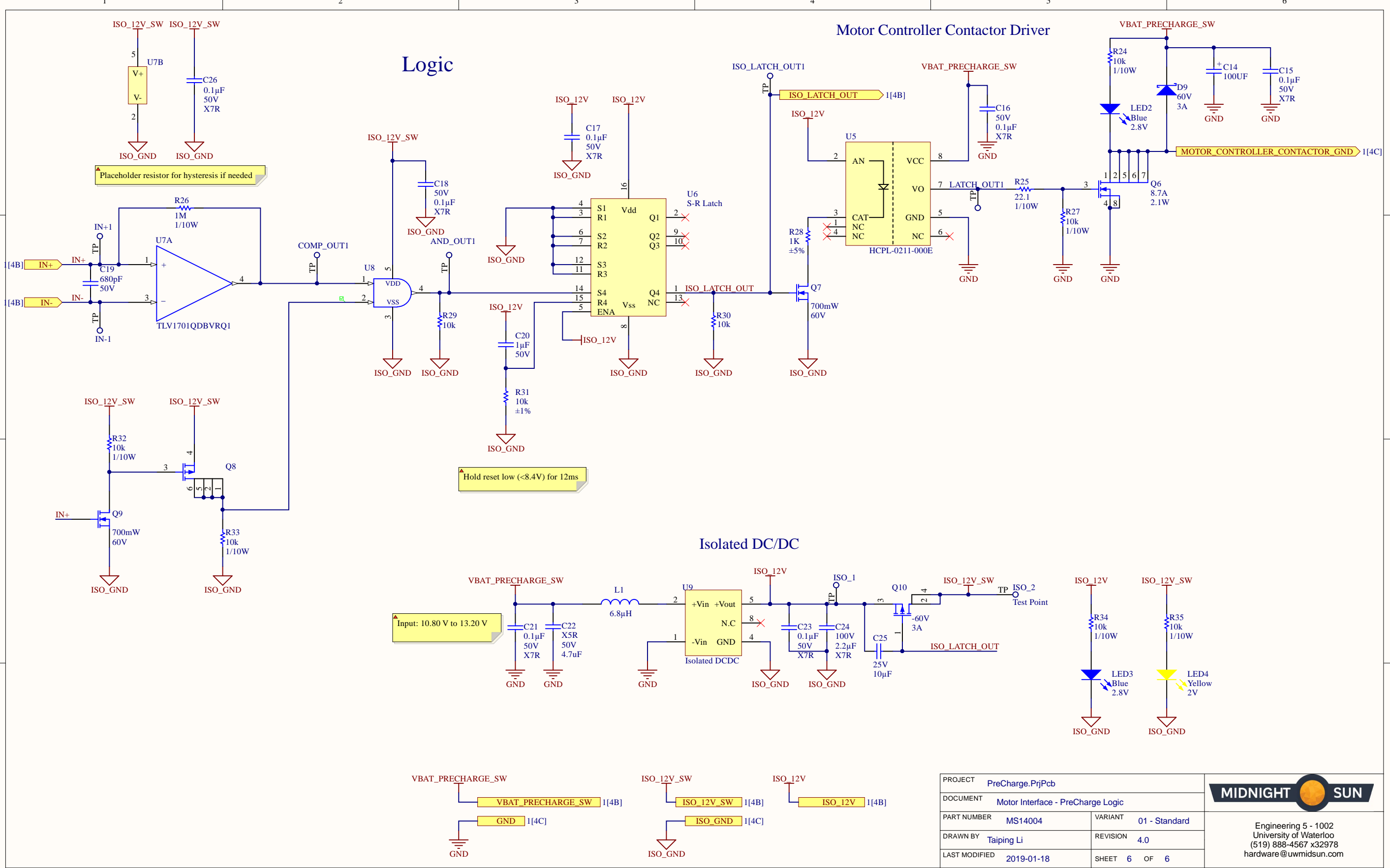


PROJECT		PreCharge.PrjPcb	
DOCUMENT		Motor Interface - PreCharge HV	
PART NUMBER	MS14004	VARIANT	01 - Standard
DRAWN BY	Taiping Li	REVISION	4.0
LAST MODIFIED	2019-01-18	SHEET	5 OF 6

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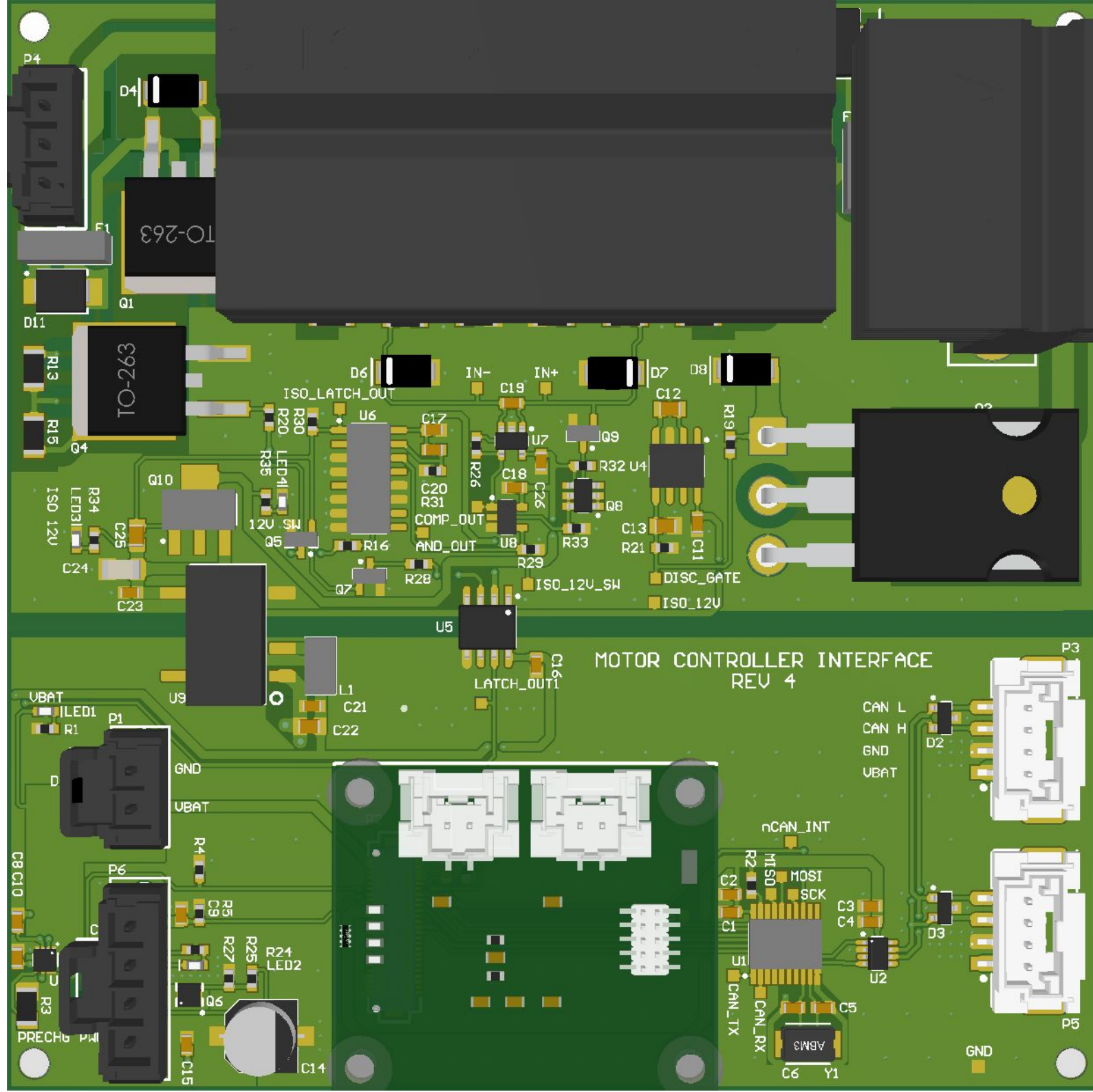


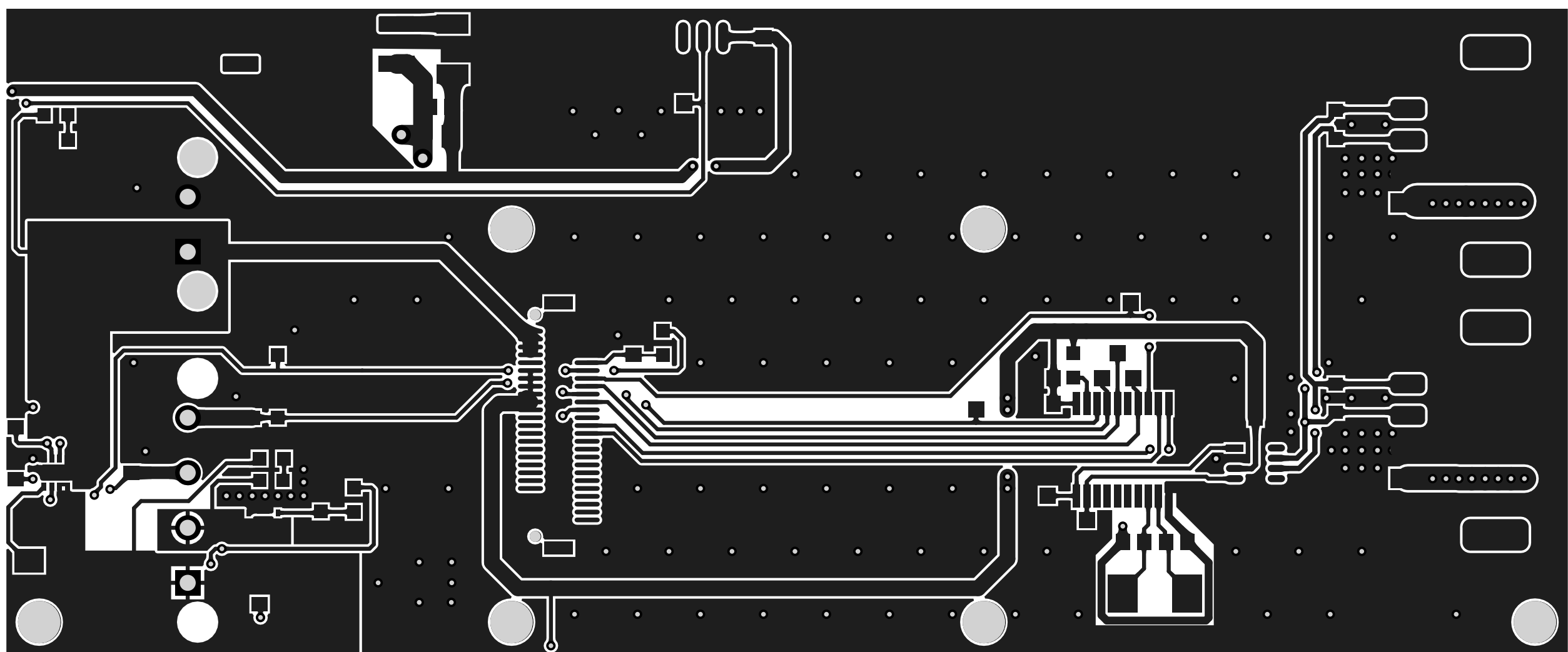
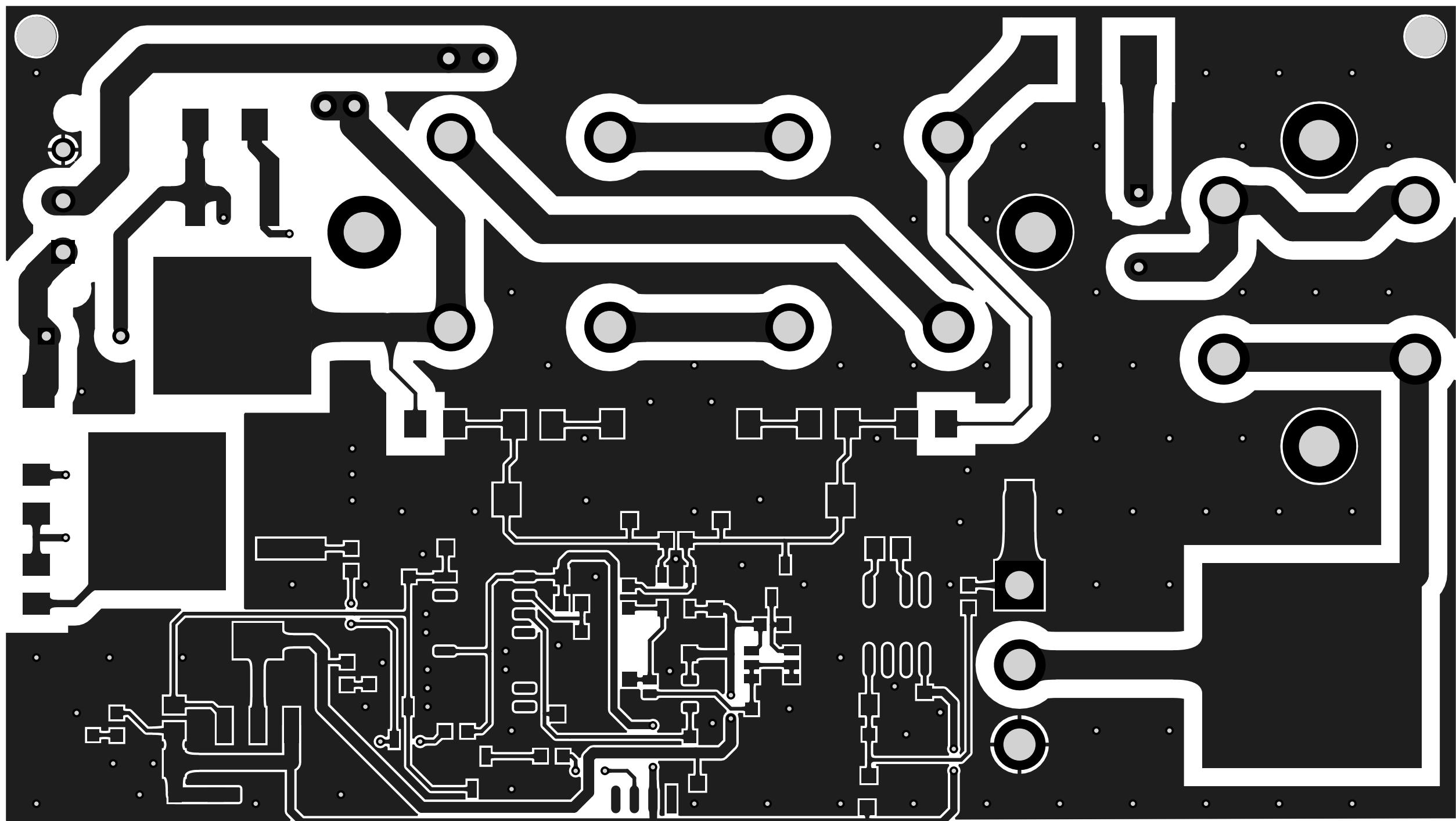
PROJECT		PreCharge.PrjPcb	
DOCUMENT		Motor Interface - PreCharge Logic	
PART NUMBER	MS14004	VARIANT	01 - Standard
DRAWN BY	Taiping Li	REVISION	4.0
LAST MODIFIED	2019-01-18	SHEET	6 OF 6

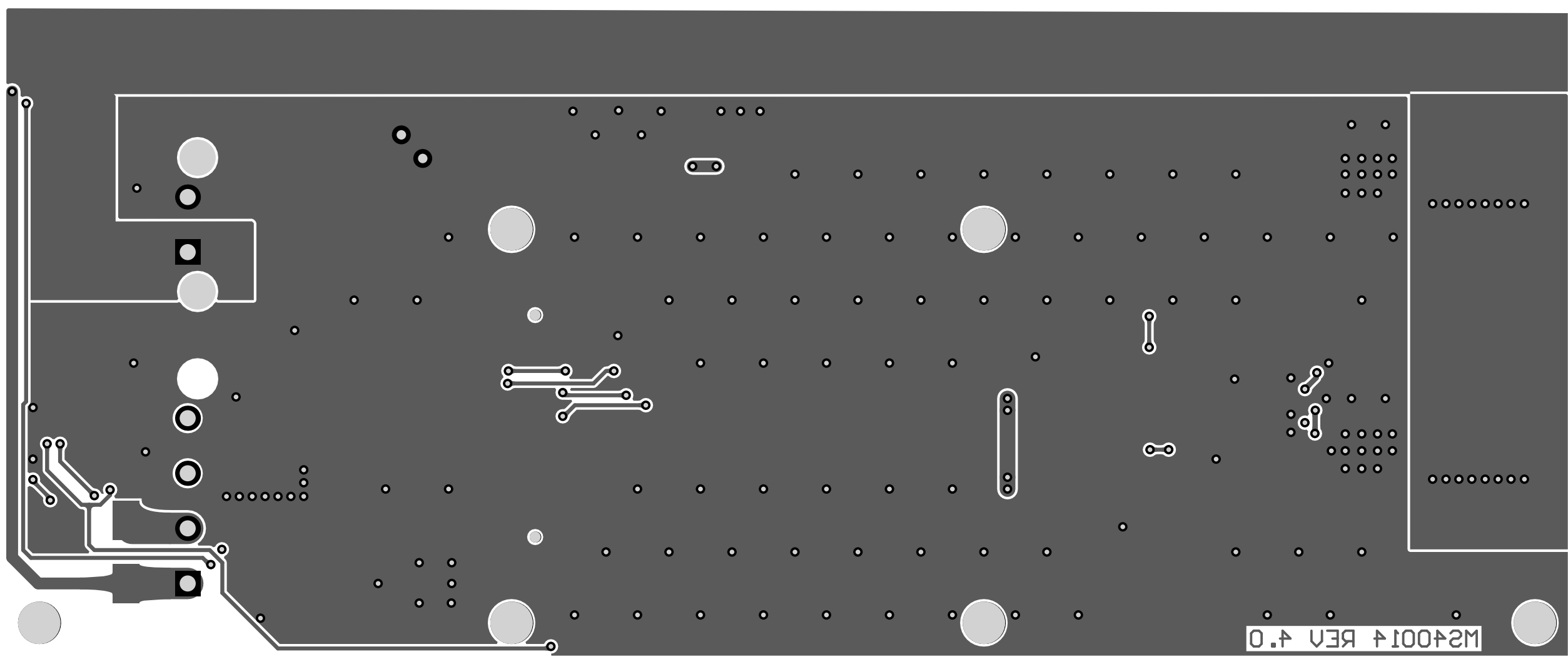
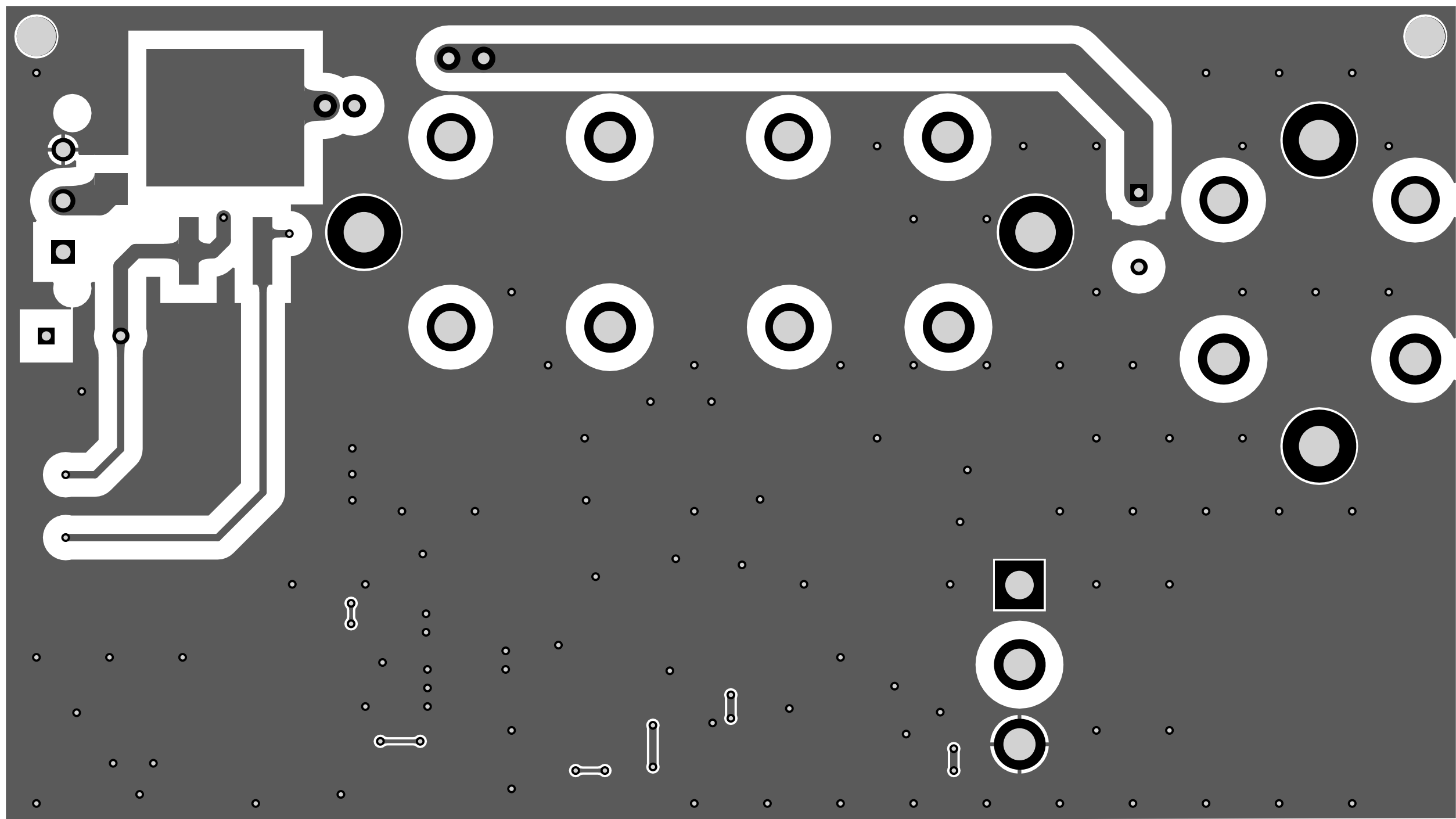
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Electrical Rules Check Report

Class	Document	Message
Warning	Motor Interface - Pre-Charge Interface.SchDoc	3V3 contains Output Port and Unspecified Port objects (Port 3V3,Port CONTACTOR_SENSE_OUT)
Warning	Motor Interface - Pre-Charge Interface.SchDoc	Nets Wire 3V3 has multiple names (Power Object 3V3,Power Object 3V3,Power Object 3V3,Port 3V3,Port CONTACTOR_SENSE_OUT)
Warning	Motor Interface - Top Sheet.SchDoc	Nets Wire 3V3 has multiple names (Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Power Object 3V3,Sheet Entry U_Motor Interface - CAN-3V3(Passive),Sheet Entry U_Motor Interface - Connectors-3V3(Passive),Sheet Entry U_Motor Interface - Connectors-CONTACTOR_SENSE_OUT(Input),Sheet Entry U_Motor Interface - Pre-Charge Interface-3V3(Passive),Sheet Entry U_Motor Interface - Pre-Charge Interface-CONTACTOR_SENSE_OUT(Output),Port 3V3,Port 3V3,Port 3V3,Port CONTACTOR_SENSE_OUT,Port CONTACTOR_SENSE_OUT)
Warning	Motor Interface - Pre-Charge HV.SchDoc	Off grid at 1800.611mil,7392.532mil
Warning	Motor Interface - Pre-Charge HV.SchDoc	Off grid at 6303.039mil,8262.396mil
Warning	Motor Interface - Pre-Charge HV.SchDoc	Off grid at 12010.97mil,8056.662mil

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_PreChargeControlle

Warnings 0

Rule Violations 104

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=1.25mm) (InNetClass('HV') and Not (InNet('IN+') or InNet('IN-'))),(InNet(''))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=10mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.05mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	65
Silk to Silk (Clearance=0.254mm) (All),(All)	37
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	2
Height Constraint (Min=0mm) (Max=200mm) (Preferred=12.7mm) (All)	0
Total	104

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (30.841mm,77.6mm) on Top Overlay And Pad R6-1(30.841mm,77.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (30.841mm,90.6mm) on Top Overlay And Pad R8-1(30.841mm,90.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (41.721mm,77.6mm) on Top Overlay And Pad R6-2(41.721mm,77.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (41.721mm,90.6mm) on Top Overlay And Pad R8-2(41.721mm,90.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (53.961mm,77.6mm) on Top Overlay And Pad R7-1(54mm,77.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (53.961mm,90.6mm) on Top Overlay And Pad R9-1(53.941mm,90.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (64.841mm,77.6mm) on Top Overlay And Pad R7-2(64.88mm,77.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (64.841mm,90.6mm) on Top Overlay And Pad R9-2(64.821mm,90.6mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (83.741mm,75.43mm) on Top Overlay And Pad R10-2(83.7mm,75.42mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (83.741mm,86.31mm) on Top Overlay And Pad R10-1(83.7mm,86.3mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (96.741mm,75.46mm) on Top Overlay And Pad R14-2(96.8mm,75.42mm)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Arc (96.741mm,86.34mm) on Top Overlay And Pad R14-1(96.8mm,86.3mm) on
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C1-2(65.557mm,16.374mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.134mm < 0.178mm) Between Pad C16-2(48.5mm,38.355mm) on Top Layer And Text "LATCH_OUT1"
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-1(39.779mm,60.525mm) on Top Layer And Text "C17"
Silk To Solder Mask Clearance Constraint: (0.077mm < 0.178mm) Between Pad C17-2(38.429mm,60.525mm) on Top Layer And Text "C17"
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C2-2(65.575mm,18mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad C7-2(8.333mm,13.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad COMP_OUT-TP(43.08mm,53.5mm) on Top Layer And Text "COMP_OUT"
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-1(8mm,9mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad D9-2(8mm,5mm) on Bottom Layer And Track
Silk To Solder Mask Clearance Constraint: (0.115mm < 0.178mm) Between Pad MOSI-TP(70.989mm,19.609mm) on Top Layer And Text "MISO"
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P3-7(95mm,25.55mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P3-7(95mm,38.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P5-7(95mm,21.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P5-7(95mm,8.05mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad Q5-2(26.025mm,51.635mm) on Top Layer And Text "12V SW"
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-1(17.656mm,8.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-2(17.656mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-3(17.656mm,9.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-4(15.806mm,9.45mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.112mm < 0.178mm) Between Pad Q6-5(15.806mm,8.8mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad Q6-6(15.806mm,8.15mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.067mm < 0.178mm) Between Pad R29-2(47.2mm,49.575mm) on Top Layer And Text "U8" (45.3mm,49.8mm)
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-1(78.425mm,13.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-2(78.425mm,12.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-3(78.425mm,12.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-4(78.425mm,11.625mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-5(81.075mm,11.625mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-6(81.075mm,12.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-7(81.075mm,12.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-8(81.075mm,13.575mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.162mm < 0.178mm) Between Pad U3-1(4.3mm,12.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.139mm < 0.178mm) Between Pad U3-4(2.8mm,12.9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.131mm < 0.178mm) Between Pad U3-5(2.8mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad U3-8(4.05mm,11.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.155mm < 0.178mm) Between Pad U3-8(4.3mm,11.1mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U3-9(3.55mm,12mm) on Top Layer And Track

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-1(45.939mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-2(44.669mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-3(43.399mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (Collision < 0.178mm) Between Pad U5-4(42.129mm,45.295mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-5(42.129mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-6(43.399mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-7(44.669mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0mm < 0.178mm) Between Pad U5-8(45.939mm,39.705mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-1(47.2mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-2(46.25mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-3(45.3mm,60.65mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-4(45.3mm,58.35mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad U7-5(47.2mm,58.35mm) on Top Layer And Track

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (0.075mm < 0.254mm) Between Text "C16" (49.984mm,39.905mm) on Top Overlay And Text "LATCH_OUT1"
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "C7" (7.749mm,14.382mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "D11" (1.667mm,70mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.227mm < 0.254mm) Between Text "D2" (84.366mm,31.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.126mm < 0.254mm) Between Text "D4" (10.5mm,91.193mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.221mm < 0.254mm) Between Text "D7" (59.124mm,65.4mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "D8" (62.696mm,65.687mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.192mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "F1" (8.261mm,78.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.144mm < 0.254mm) Between Text "ISO_LATCH_OUT" (25.475mm,63.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "L1" (30.57mm,36.327mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "LED1" (5.4mm,34.355mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.251mm < 0.254mm) Between Text "LED2" (23.951mm,11.099mm) on Top Overlay And Text "R24" (23.9mm,12.3mm)
Silk To Silk Clearance Constraint: (0.211mm < 0.254mm) Between Text "LED3" (5.93mm,55.177mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.095mm < 0.254mm) Between Text "LED4" (24.8mm,58.547mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.077mm < 0.254mm) Between Text "M!1" (93mm,93.739mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.077mm < 0.254mm) Between Text "M!1" (93mm,93.739mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.136mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.117mm < 0.254mm) Between Text "P1" (9.45mm,33.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.177mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.173mm < 0.254mm) Between Text "P6" (9.45mm,19.875mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.217mm < 0.254mm) Between Text "Q5" (23.75mm,49.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "Q6" (18.356mm,7.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.14mm < 0.254mm) Between Text "Q9" (54.6mm,59.525mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R14" (94.191mm,89.323mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "U1" (66.566mm,11.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.232mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "U2" (79.177mm,9.9mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.147mm < 0.254mm) Between Text "U4" (57.2mm,56.82mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.245mm < 0.254mm) Between Text "U6" (32.398mm,61.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.206mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.205mm < 0.254mm) Between Text "U8" (45.3mm,49.8mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (30mm,0mm)(30mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (65mm,0mm)(65mm,30mm) on Top Overlay