Song Hang **Chai**
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EDUCATION

The University of Texas at Austin, USA Aug 2024 – **Jun 2029 (Expected)**
- **Doctor of Philosophy (Electrical and Computer Engineering)**
- Supervisor: Dr. Sensen Li
- Research Direction: (1) *Radio Frequency Integrated Circuit Design (RFIC)* (2) *Design Automation of RFIC using AI/ML Techniques*

Nanyang Technological University, Singapore (NTU) Aug 2020 – Jun 2024
- **Bachelor of Engineering (Electrical and Electronic Engineering)**
- **Honours (Highest Distinction)** CGPA: 4.85 / 5.00
- Specialisation: **Integrated Circuit Design**
- Relevant Modules: (1) *Analog Electronics* (2) *Digital Electronics* (3) *Semiconductor Fundamentals* (4) *Control Engineering* (5) *Advanced Signal Processing* (6) *Analog and Mixed Signal IC Design* (7) *Radio Frequency Circuits* (8) *Radio Frequency Integrated System Design* (9) *Analysis and Design of Integrated Circuits*

Case Western Reserve University, USA (Overseas semester exchange programme) Jan 2023 – May 2023
- **Bachelor of Engineering (Electrical, Computer, and Systems Engineering)**
- **Honours (Highest Distinction)** CGPA: 4.00/4.00
- Modules taken: (1) *Electromagnetic Fields I (2) Signal Processing (3) Digital Systems Design (4) Control Engineering I With Lab (5) Engineering Projects I*

PUBLICATIONS

A D-band InP Power Amplifier Featuring Fully AI-Generated Passive Networks To be published
***Song Hang Chai**, Hyunsu Chae, Hao Yu, David Z. Pan, Sensen Li*
IEEE Microwave and Wireless Technology Letters

ML-Assisted RFIC Design Enhancement: The New Frontier of AI for EDA March 2025
*Hyunsu Chae, **Song Hang Chai**, Taiyun Chi, Sensen Li, David Z. Pan*
Proceddings of the 30th Asia and South Pacific Design Automation Conference

RESEARCH EXPERIENCE

PhD First Year Project Oct 2024 – Dec 2024
Project title*:* **A D-band InP Power Amplifier (PA) Featuring Fully AI-Generated Passive Networks**.
- Authored the part on AI-generated Passive Networks.
- Performed large-signal measurements on the PA.

Undergraduate Final Year Project (FYP) Jul 2023 – May 2024
Project title*:* **Fully Differential Controlled Gain Open-Loop Wideband Amplifier with common-mode feedback**.
- Designed a fully-differential wideband amplifier utilizing an recycling folded-cascode topology in Global Foundry 55nm CMOS technology.
- Achieved a compact layout with a final silicon area of $26.137\mu m \times 32.084\mu m$, maintaining the parasitic variation within $\pm 10\%$ post-layout.

Undergraduate Research Project Jul 2022 – Jul 2023
Project title*:* **Continuous-time Sigma-Delta Analog to Digital Converter**
- Developed an 8-bit Sigma-Delta ADC in TSMC 65nm technology node.
- Designed and integrated key building blocks including a high-gain operational amplifier, StrongARM latch comparator, D flip-flop-based clock divider and data sampler

Professional Internship Research Project Sep 2022 – Dec 2022
Project title: **Application of Principal Component Analysis (PCA) on Even-and-Odd Jitter (EOJ) in PAM4 Signalling**
- Implemented a PCA-based mathematical model that can accurately calculate the yield rate, significantly reduced the reliance on extensive Monte Carlo simulations.
- The yield rate calculation is accurate up to 99% with as few as 50 data points.

COURSEWORK PROJECT

Undergraduate Coursework Project (EE4304) Apr 2024 – May 2024
Project title: ***Source-degenerated Low Noise Amplifier***
- Designed two source-degenerated LNA with different topologies that meet the target specifications.

Undergraduate Coursework Project (EE4303) Oct 2023 – Nov 2023

Project title: ***Sample-Data System using Switched-Capacitor Amplifier (SC-Amplifier) for SoC application***

- Designed several analog blocks for this sample-data system. This includes RFC-OTA, current-mode voltage reference, and inverter-based ring oscillator.
- Final design achieves a worst-case accuracy of 99.53%, and a total current consumption of $201.3163\mu A$.

INTERNSHIP

Advanced Micro Devices (AMD)/Xilinx – *IC Design Intern* (SerDes Design Department) May 2022 – Dec 2022

- Offered the chance to rotate between different functional teams in design department.
- Permanently attached to Analog Design Team, spent one month each at Digital Design Team, Place and Route Team, Layout Team, and Verification Team.
- Completed several small projects in each team, and a two big projects at the Analog Design Team.

TEACHING EXPERIENCE

UT Austin Chandra School of Electrical and Computer Engineering Aug 2024 – Dec 2024

Role: ***Teaching Assistant***

- Teaching assistant for a sophomore module consists of 64 students: *ECE411 Circuit Theory*
- Collaborate with the course coordinator to enhance students' understanding of course materials.
- Conducted weekly office hours to support and enhance students' understanding of course materials.
- Evaluated and graded homework and exams to assess student performance.

NTU School of Electrical and Electronic Engineering Aug 2023 – May 2024

Role: ***Peer Tutor***

- Peer tutor for a sophomore module: *Analog Electronics*
- Focused on supporting students who are placed on academic warning/probation list.
- Worked alongside the course coordinator to facilitate student comprehension of the course materials.
- Conducted weekly tutorial class after working hours to enhance tutees' understanding on the course.

NTU School of Electrical and Electronic Engineering SEEENIOR Program Jan 2022 – Dec 2022

Role: ***SEEENIOR (Peer Tutor)***

- Strived to assist students with academic difficulties.
- Provided additional notes for tutees to enhance their understanding on a subject.
- Instructed the following modules: *(1) Analog Electronics, (2) Engineering Mathematics I, (3) Engineering Mathematics II, (4) Semiconductor Fundamentals.*

SCHOLARSHIPS/AWARDS

IMS/RFIC PhD Student Sponsorship

UT Austin Graduate School Fellowships

NTU Undergraduates Scholarship

- Awarded to students who demonstrate exceptional performance in both academic and co-curricular activities
- Scholarships awarded: (1) *Lam Research Scholarship* (2) *NTU Class of 1985 Scholarship*

NTU School of Electrical and Electronic Engineering Dean's List

- The Dean's List is awarded annually to the top 5% of the cohort for excellent academic performance
- Dean's List recipient for: (1) *AY2021-22* (2) *AY2023-24*

SKILLS

- **Languages**: Fluent in *English, Mandarin, Malay* ; Elementary proficiency in *German*
- **Software Programming**: MATLAB, Python, Basic Linux/Unix command, Bash Scripting, Basic vi/vim editor
- **EDA Tools**: Cadence, ADS, HFSS