CSED311 Homework 2

~~컴퓨터공학과~~

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2.39.1

Arithmetic instruction ⇒ 500 → ~~5%감소~~ 500 · 0.75 (분모 millions로 바꿀 계산기에게 생략)

하지만, Cycle time 10% 증가 ⇒ total × 1.1 = result

Initial ⇐ Condition = 500 · 1 + 300 · 10 + 3 · 100

= 3800 cycle.

After ⇒ 500 · 0.75 × 1 + 300 · 10 + 3 · 100

= 375 + 3000 + 300

= 3675

Result = 3675 × 1.1

= 4042.5 cycle

Speedup = $\frac{old}{new} = \frac{3800}{4042.5} \simeq 0.94$.

∴ 0.94 //

2.39.2 Arithmetic performance → ×2.

⇒ ~~1 cycle~~ CPI → 0.5 CPI.

500 · 0.5 + 300 · 10 + 3 · 100

= 250 + 300 + 3000 = 3550

Speedup = $\frac{3800}{3550} \simeq 1.07$ //

2.39.3 by 10 times ↑ ⇒ $\frac{old}{new} = 10 = \frac{1}{0.1}$ CPI //

500 · 0.1 + 300 · 10 + 100 · 3

= 50 + 3000 + 300 = 3350

Speedup = $\frac{3800}{3350} \simeq 1.13$ //

4.16.1

Pipelined clock cycle ⇒ longest stage latency.

: ID 350 ps

non- " = Σ each stage latency

= 250 + 350 + 150 + 300 + 200

= 1250 ps

4.16.2 lw instruction total latency

Pipelined ⇒ longest stage * 5

= 350 · 5 = 1750 ps

non-pipelined ⇒ Σ each stage latency

= 1250 ps.

4.16.3 ~~ff~~ ID stage ⇒ ID가 모든 stage 중에서 가장 길게 걸리는 이유는 두개로 나누면 175ps로 잘라지므로 longest stage latency는 300ps로 바꿀수 없게 된다

∴ ID. 300ps

4.16.4 With No data Hazard or stall

⇒ data memory를 쓰는 inst ⇒ STore/Load

= ⇒ 15% + 20% = 35%

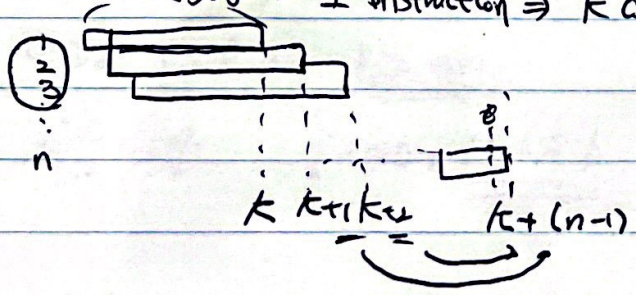
Write rejitta util.

⇒ Arithmetic, ~~Store~~ Load (Jump, branch x)

⇒ 45% + 20% = 65%

4.17 Minimum ※ cycles in k stage pipeline

k stage - 1 instruction ⇒ k cycle.



∴ ※cycle of Minimum

= k + (n-1) //

단, 1st half에 쓰고 2nd half에 read하므로 WB cycle에 사용가능.

4.26.4

No forwarding! → forwarding이 없으므로 write-back 될 때까지 기다려야 한다

① Ex to 1st only

add x3 x2
add x3

0 0 0 0 0
~~0 0 x x~~ < 2stall
0 x x 0 0 0

② MEM to 1st only

lw x2 x1
add x3, x2

0 0 0 0 0 < 2stall
0 x x 0 0

③ Ex to 2nd only

add x3 x2
~~add~~
add x3

0 0 0 0 0
0 0 0 0 0 < 1stall
0 x 0 0 0

④ MEM to 2nd only

lw x2 x1
~~add~~
add x2.

0 0 0 0 0
0 0 0 0 0 < 1stall
0 x 0 0 0

⑤ Ex to 1st & 2nd

add (x2) x1 x3
add x4 (x2) x1
add x4 (x2) x1

0 0 0 0 0
0 x x 0 < 2stall
0 x 0

$2 \cdot 0.05 = 0.1$
$\Rightarrow + 2 \cdot 0.2 = 0.4$
$+ 1 \cdot 0.05 = 0.05$
$+ 1 \cdot 0.1 = 0.1$
$2 \cdot 0.1 = 0.2$

0.85 stall

$\Rightarrow \therefore$ CPI = basic + stall = $1 + 0.85 =$ 1.85 CPI

$\frac{0.85}{1.85} \times 100 = 45.95\%$

4.26.5 with full forwarding

① 0 0 0 0 0
0 0 0 0 0 < 0 stall

② 0 0 0 0 0
0 0 x 0 0 < 1 stall

③ 0 0 0 0 0
~~0 0 0 0 0~~ < 0 stall
0 0 0 0 0

④ 0 0 0 0 0
0 0 0 0 0 < 0 stall
0 0 0 0 0

⑤ 0 0 0 0 0
0 0 0 0 0 0 stall
0 0 0 0 0

$\Rightarrow 1 \cdot 0.2 = 0.2$

$\therefore$ CPI $= 1 + 0.2 =$ 1.2 CPI

$\frac{0.2}{1.2} = \frac{1}{6}$ $\quad \frac{1}{6} \times 100 = 16.67\%$

4.26.6

Option 1. Only in Ex/MEM Register

①
00000
00000 < 0 stall

② 00000 → 여기서 value 나옴.
0 X X 0 0 < 2 stall

③ 1 00000
2 00000 < 1 stall
3 0 X 0 0 0

→ 2 line instruction으로 가면 EX/MEM Reg updated ⇒ 1사이클 WB에 되어 쓸수 있음.

④ 00000
00000 < 1 stall
0 X 0 0 0

⑤ ~~①∪②~~ ⇒ 1 stall
①∪③

⇒
2 · 0.2 = 0.4
1 · 0.05 = 0.05
1 · 0.1 = 0.2
1 · 0.1
0.65

$CPI = 1 + 0.65 = 1.65$ CPI

Option 2 Only in MEM/WB reg.

①
000000
0 X 0 0 0 < 1 stall

② 00000
00 X 0 < 1 stall

③ 00000
00000 0 stall
000

④ 00000
00000 0 stall
00000

⑤ ①∪③ → 1 stall

1 · 0.05 = 0.05
1 · 0.2 = 0.2
1 · 0.1 = 0.1
0.35

$CPI = 1 + 0.35 = 1.35$ CPI

4.26.7

CPI · t = 1 cycle time

No forwarding t = 120 ps ⇒ 1.85 · 120
Full forwarding t = 130 ps (longest) ⇒ 1.2 · 130
Only EXE/MEM t = 120 ps ⇒ 1.65 · 120
〃 MEM/WB t = 120 ps ⇒ 1.35 · 120.

speedup $\frac{t_{old}}{t_{new}}$

① EXE/MEM $\frac{1.85 \cdot 120}{1.65 \cdot 120} \approx 1.12$

② MEM/WB $\frac{1.85 \cdot 120}{1.35 \cdot 120} \approx 1.37$

③ Full forwarding $\frac{1.85 \cdot 120}{1.2 \cdot 130} = \frac{222}{156} \approx 1.42$