Date:

EXPERIMENT NO. 4

AIM: Implement arithmetic and logic unit circuits in Logisim.

OBJECTIVES:

i. Implement 1-bit, 2-bit, 4-bit and 8-bit arithmetic unit circuits

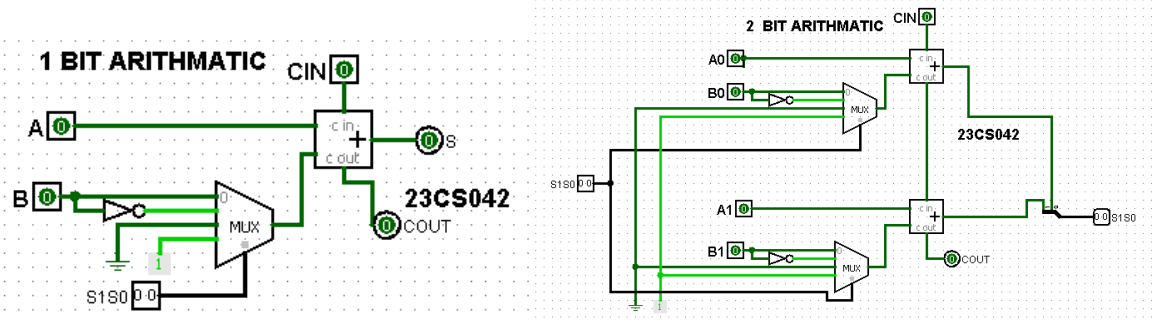
ii. Implement 1-bit, 2-bit, 4-bit and 8-bit logical unit circuits for four logical functions

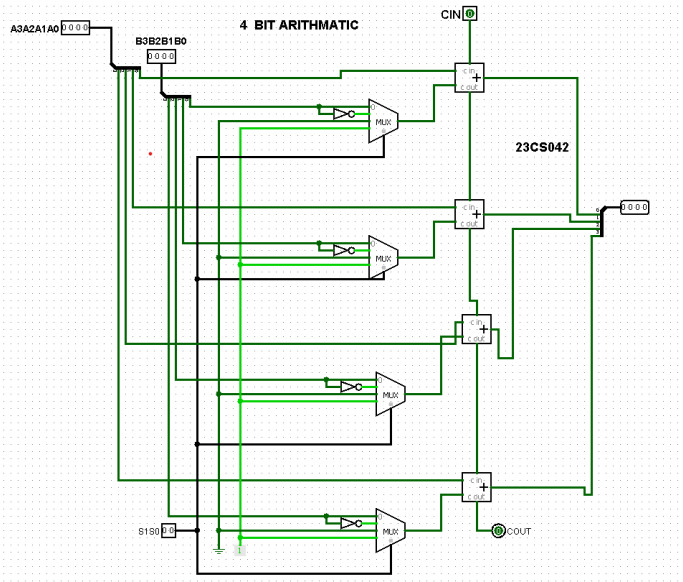
iii. Implement 1-bit and 2-bit logical unit circuits for sixteen logical functions

iv. Implement 2-bit, 4-bit and 8-bit bidirectional shifter

v. Implement 1-bit, 2-bit, 4-bit and 8-bit ALU

CIRCUITS:





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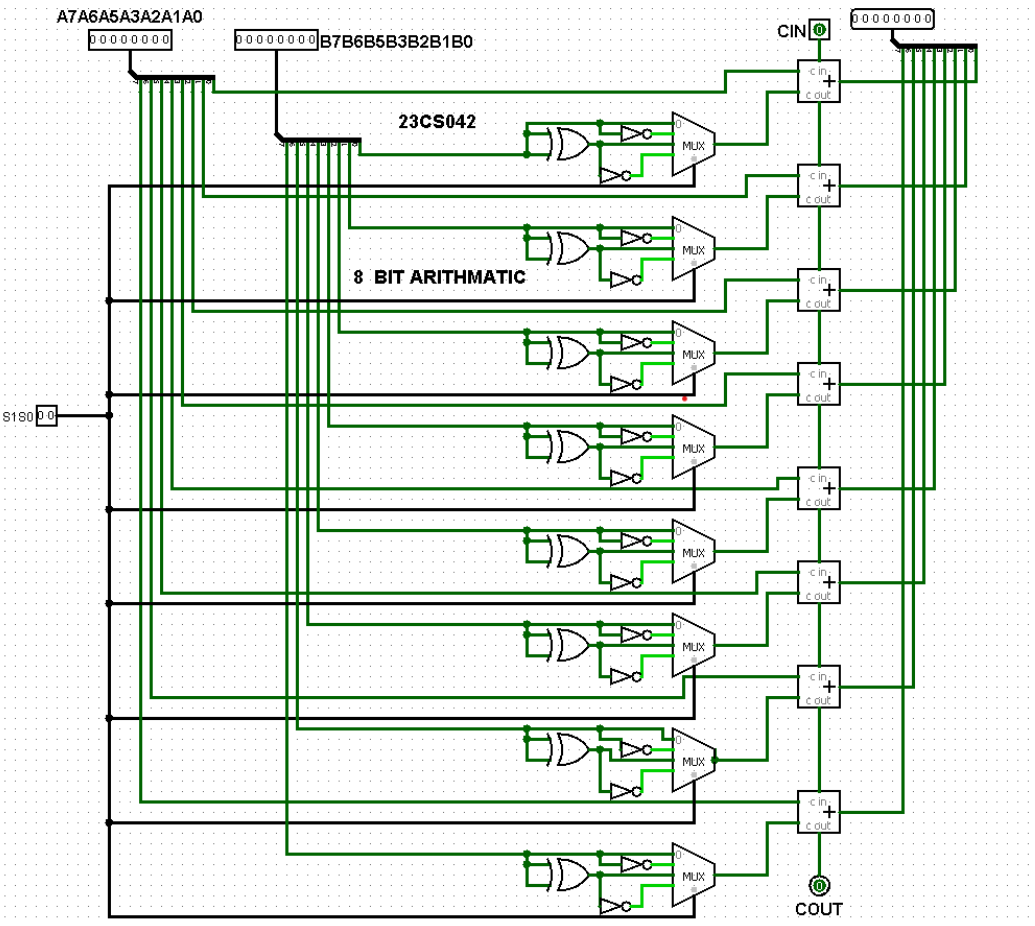
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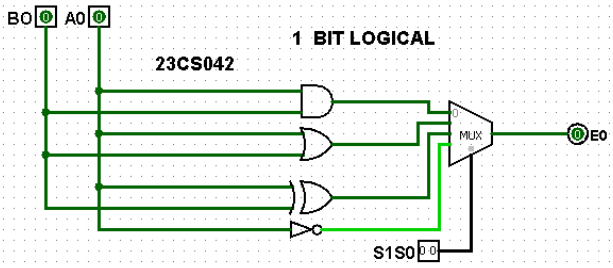
23CS042
8 BIT ARITHMATIC
MUX
S1S0
COUT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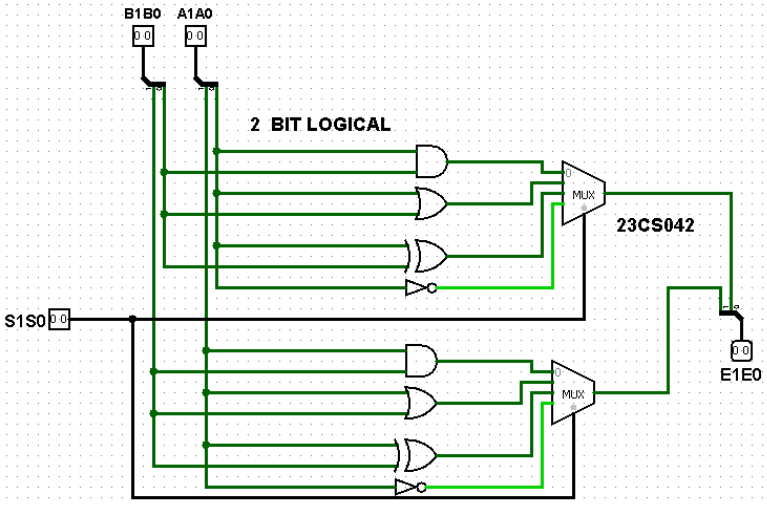
1 BIT LOGICAL
23CS042
MUX
E0
S1S0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A1A0
2 BIT LOGICAL
MUX
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S1S0
E1E0

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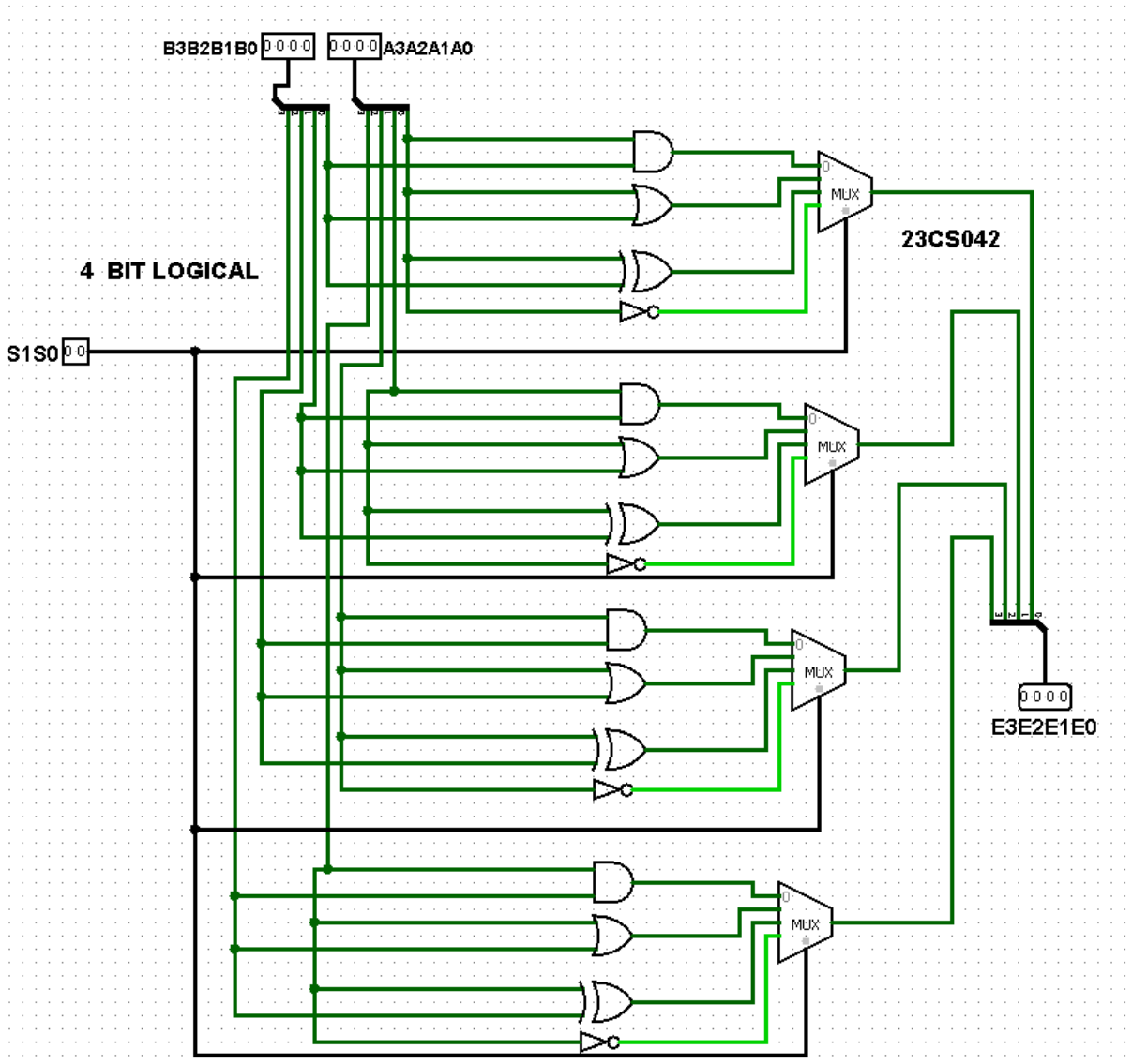
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S1S0
MUX
MUX
MUX
MUX
E3E2E1E0

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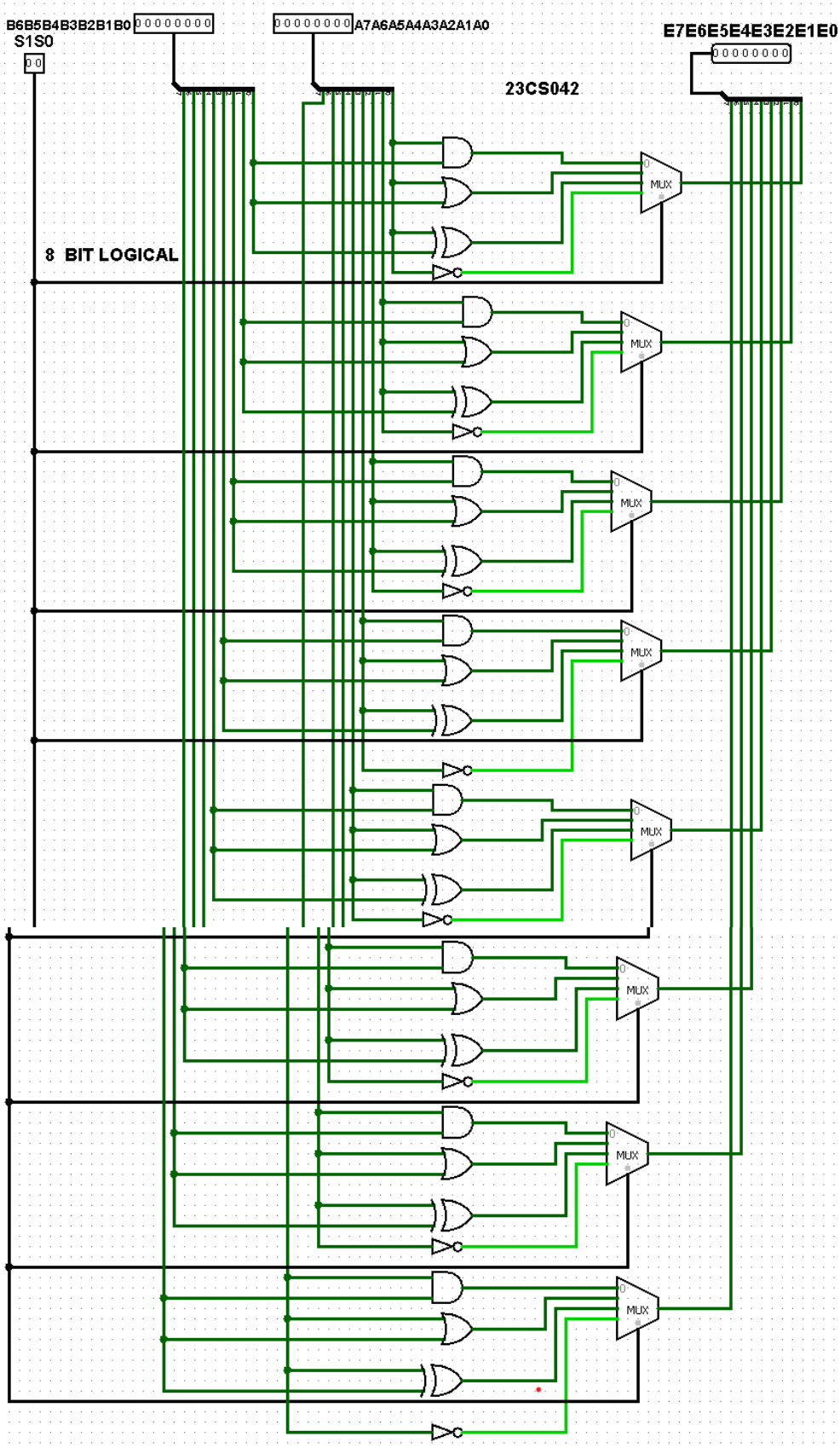
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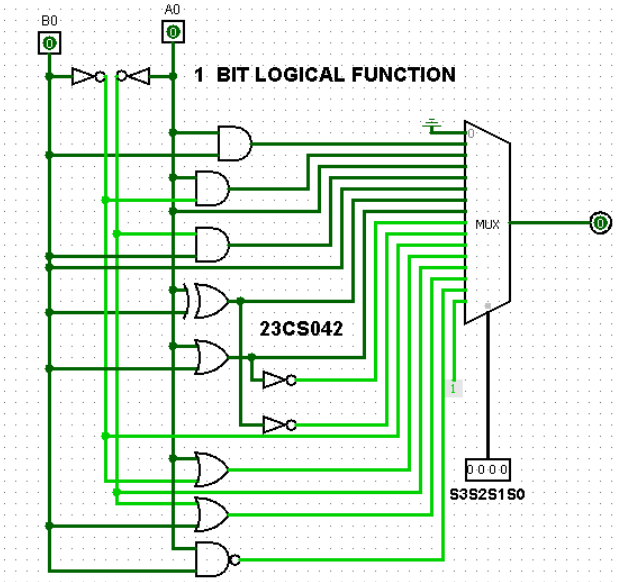
23CS042
8 BIT LOGICAL
MUX

PAGE NO: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MUX
23CS042
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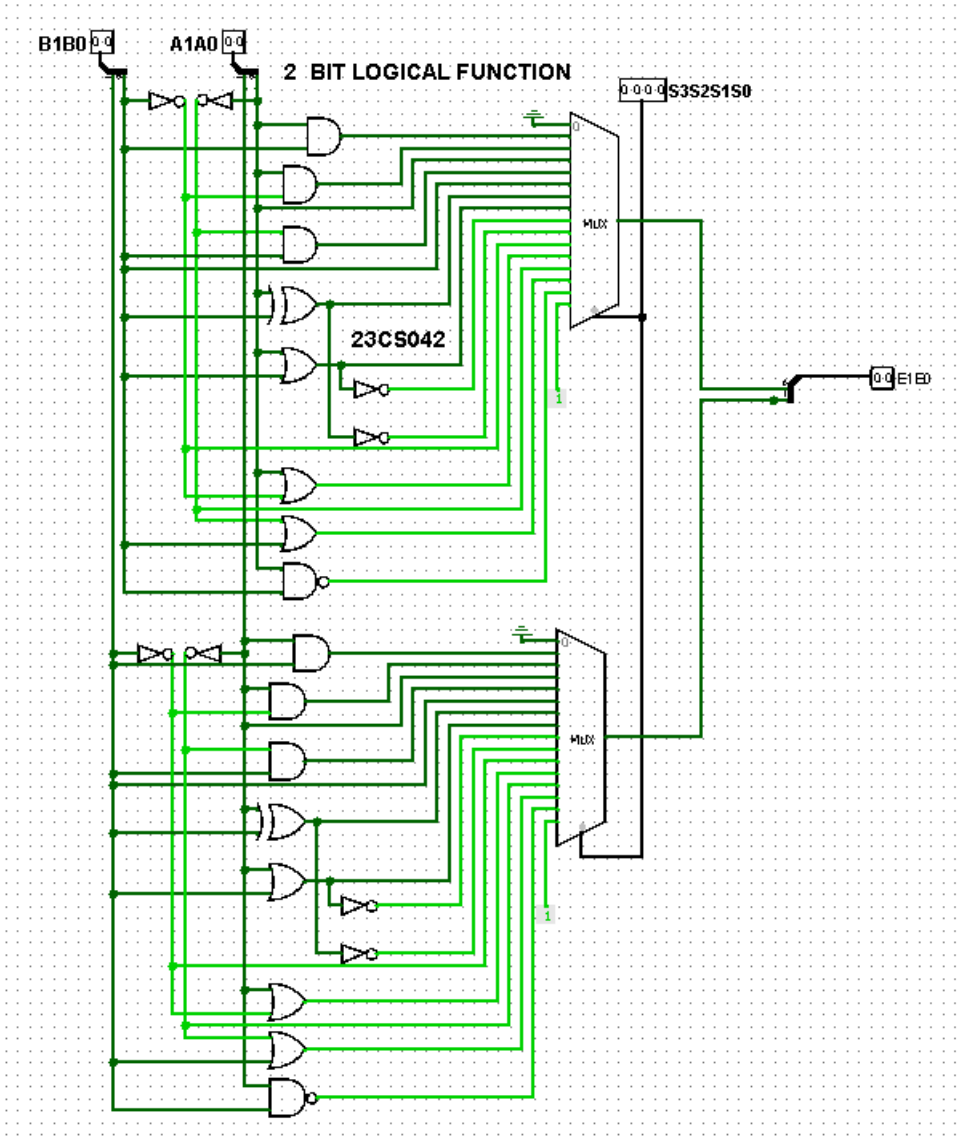
S3S2S1S0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A1A0
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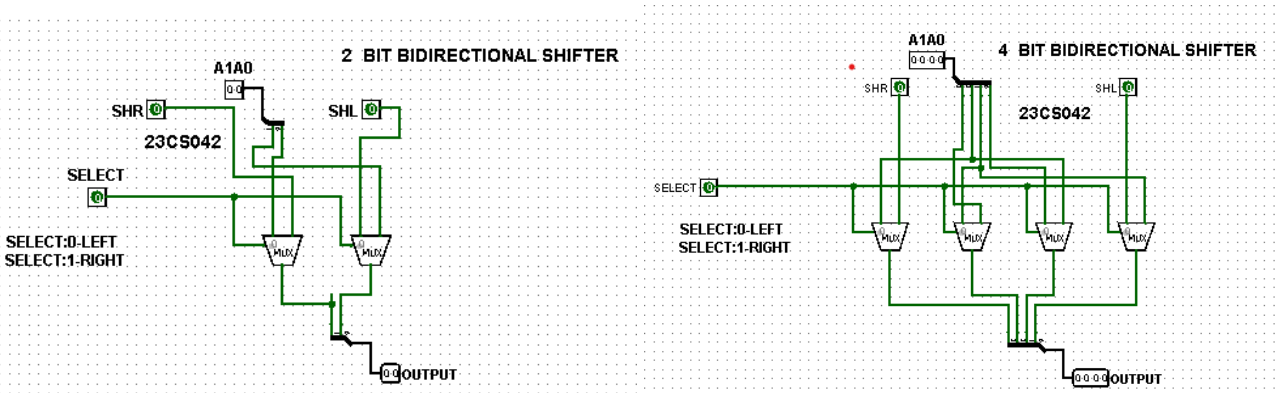
MUX
23CS042
E1E0
MUX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SHR
SHL
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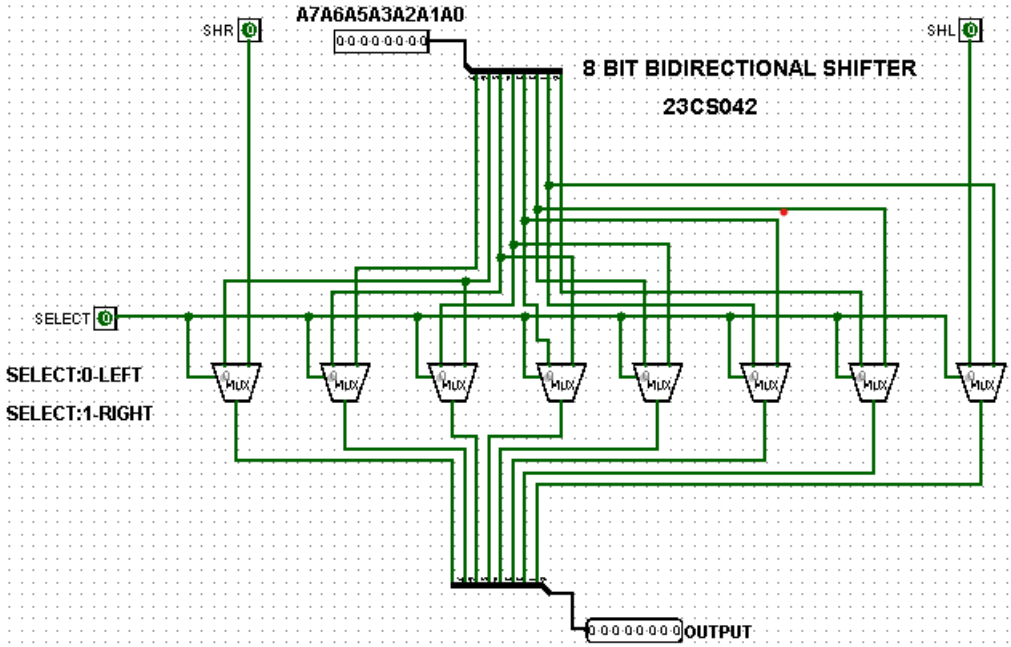
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
OUTPUT
4 BIT BIDIRECTIONAL SHIFTER
A1A0
SHR
SHL
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
OUTPUT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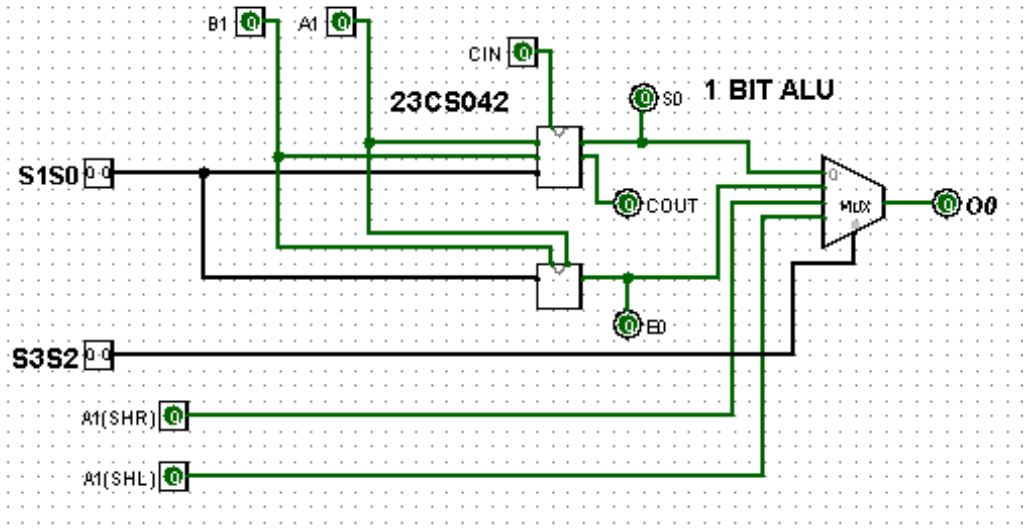
SHR
SHL
8 BIT BIDIRECTIONAL SHIFTER
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
OUTPUT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S0
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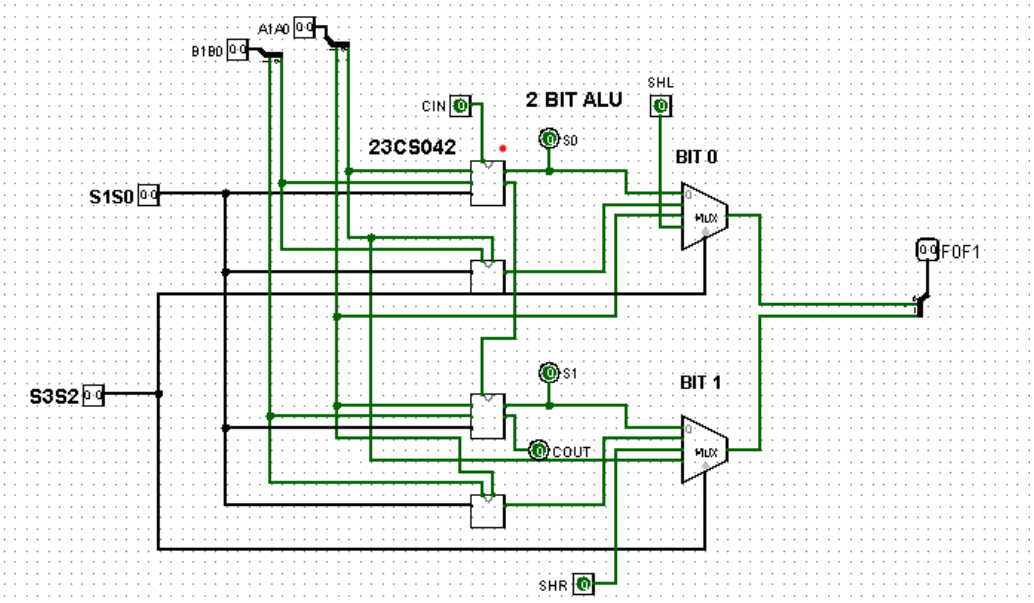
S1S0
COUT
O0
B0
S3S2
A1(SHR)
A1(SHL)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B1B0
CIN
2 BIT ALU
SHL
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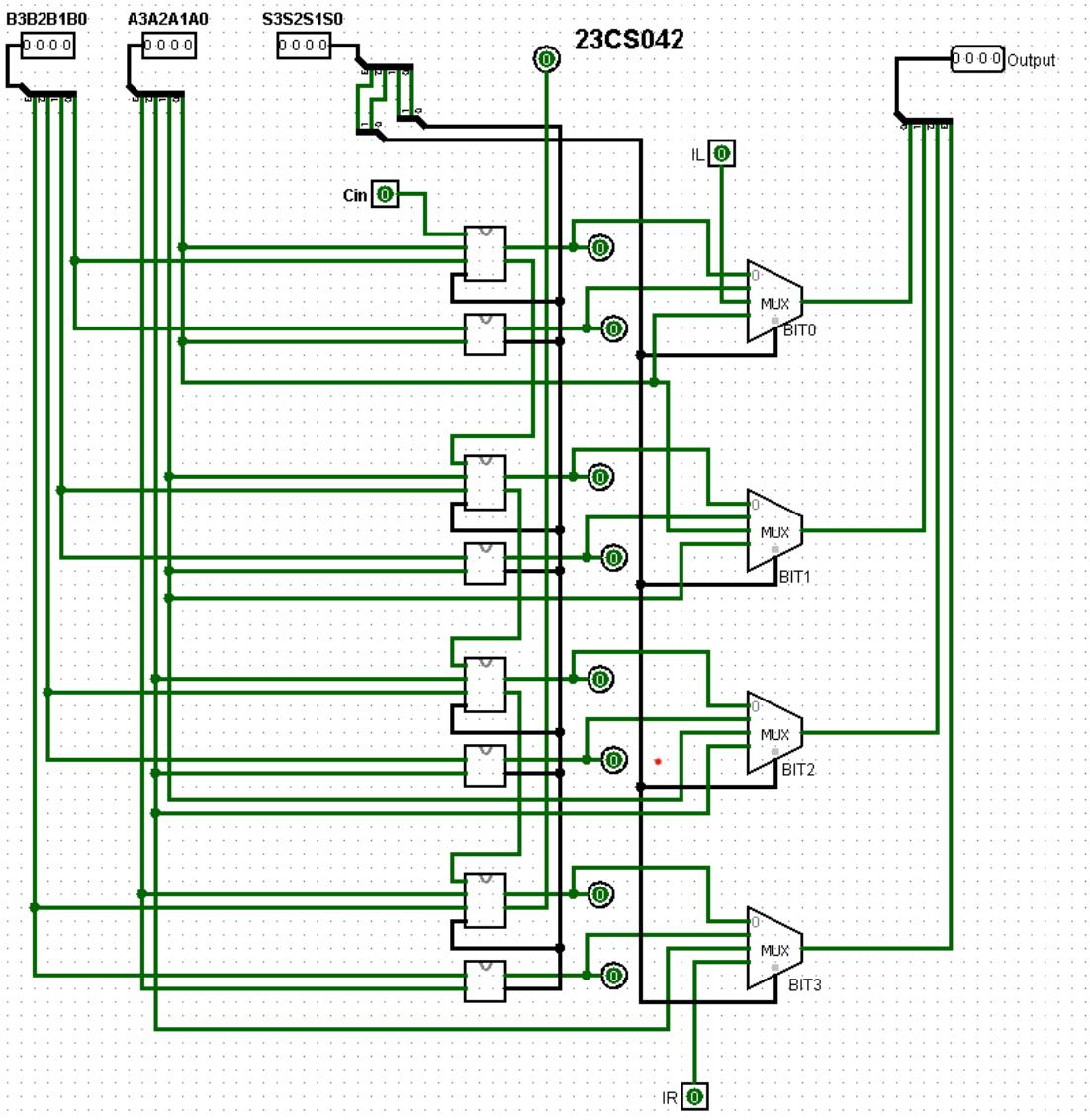
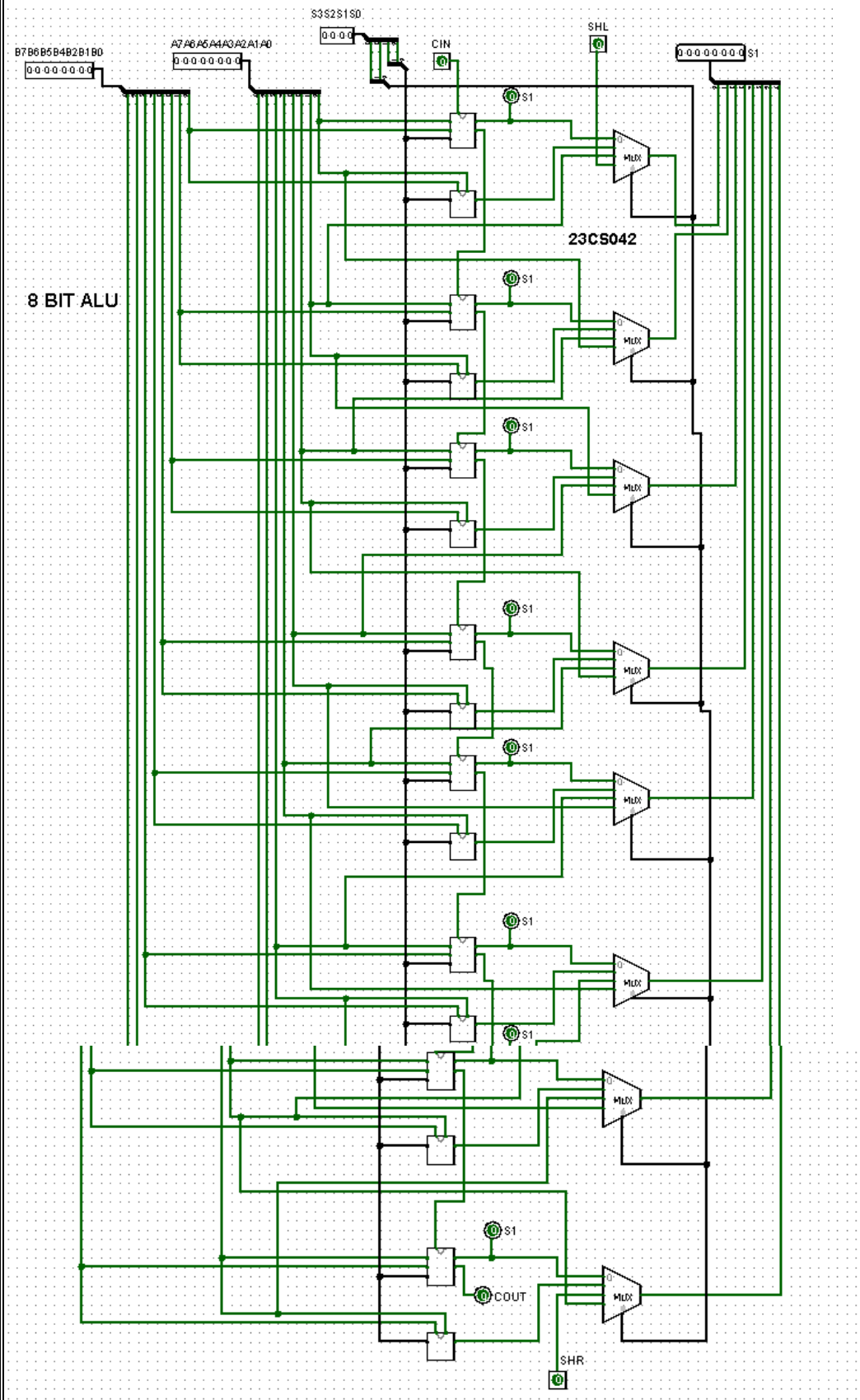
S0
BIT 0
S1S0
MUX
F0F1
S1
BIT 1
S3S2
COUT
MUX
SHR


B3B2B1B0
A3A2A1A0
S3S2S1S0
23CS042
Output
IL
Cin
MUX
BIT0
MUX
BIT1
MUX
BIT2
MUX
BIT3
IR

PAGE NO:


8 BIT ALU
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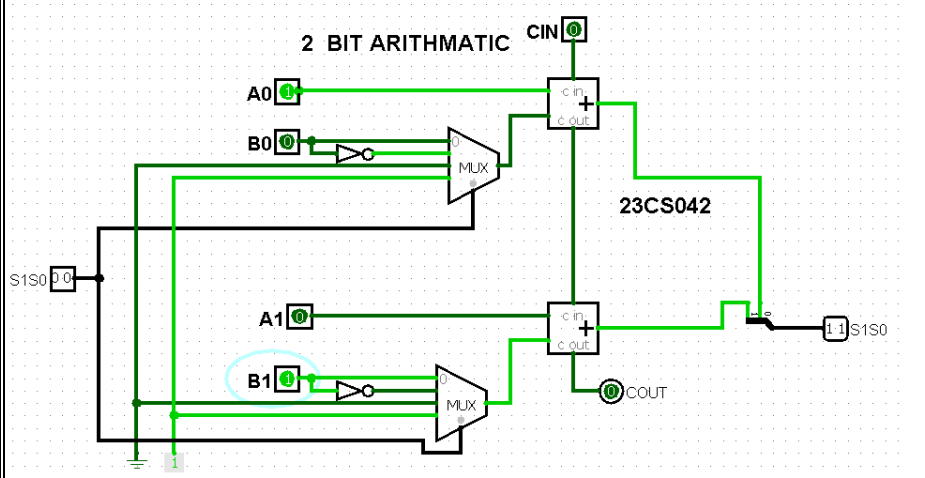
A7A6A5A4A3A2A1A0
S3S2S1S0
CIN
SHL
S1
MUX
COUT
SHR

PAGE NO:

OUTPUTS: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MUX
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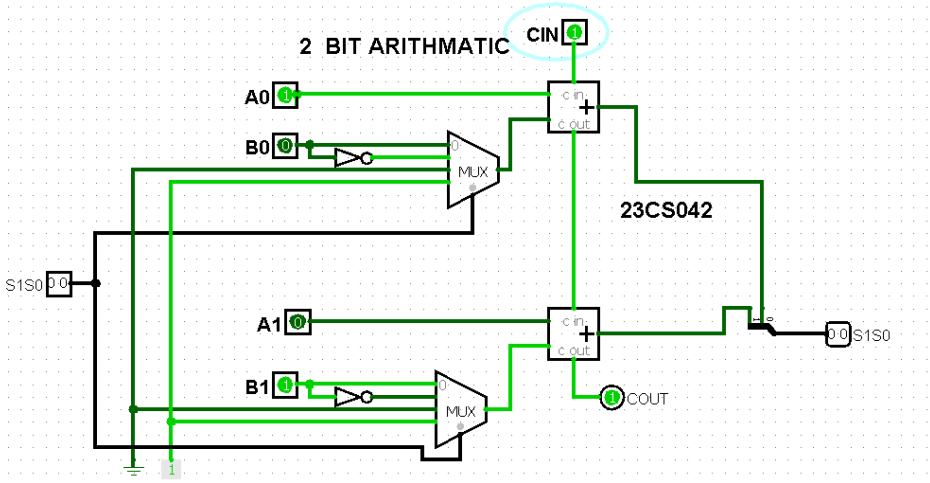
S1S0
A1
B1
MUX
COUT
S1S0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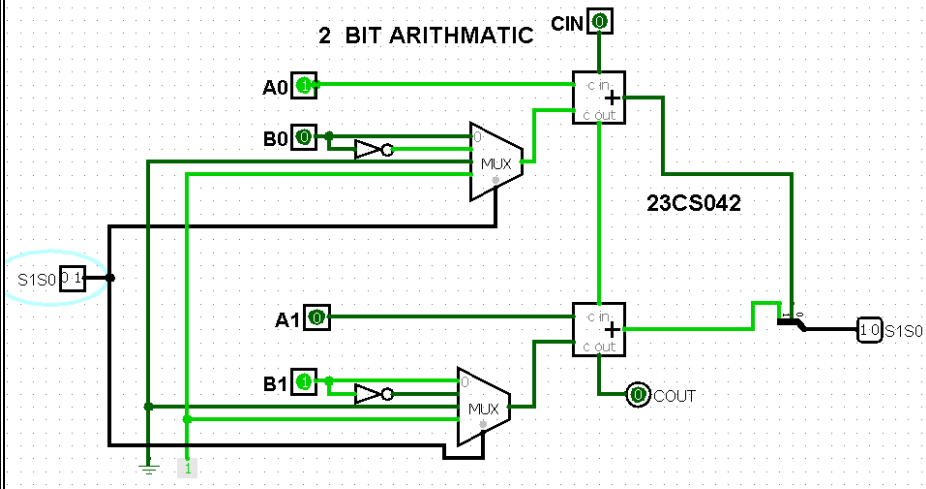
CIN
A0
B0
MUX
23CS042
S1S0
A1
B1
MUX
COUT
S1S0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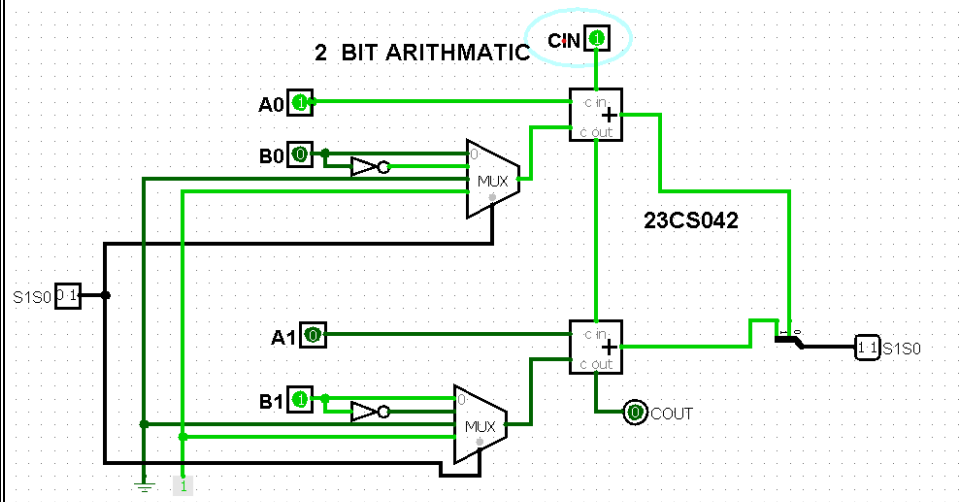
CIN
A0
B0
MUX
23CS042
S1S0
A1
B1
MUX
COUT
S1S0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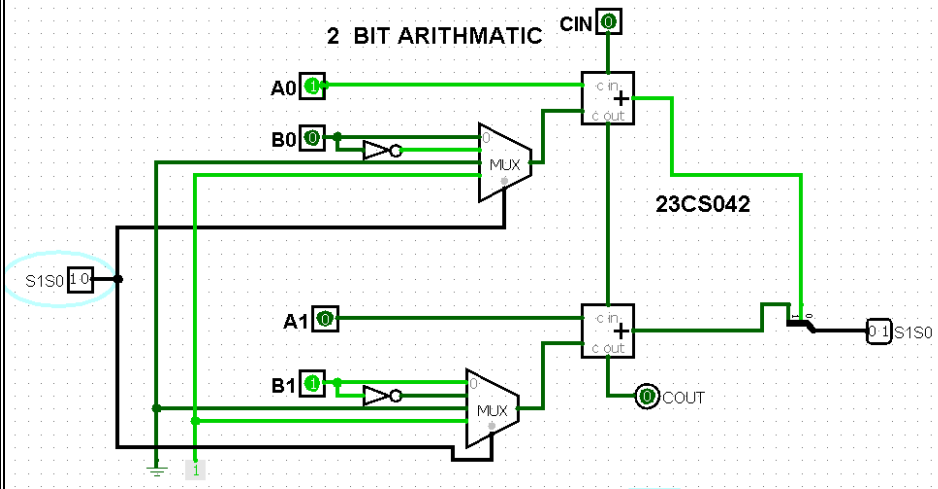
CIN
A0
B0
MUX
23CS042
S1S0
A1
B1
MUX
COUT
S1S0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B0
MUX
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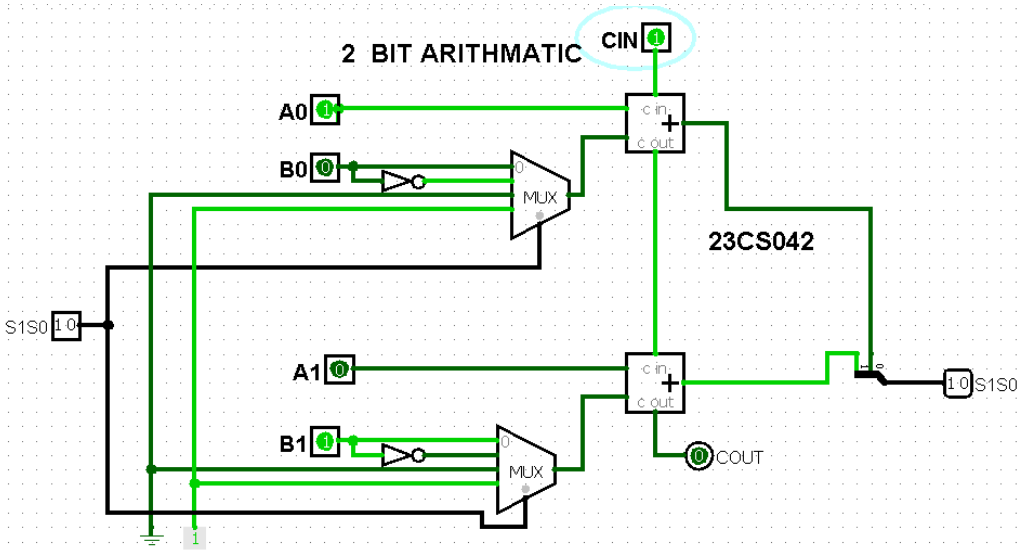
S1S0
A1
B1
MUX
COUT
S1S0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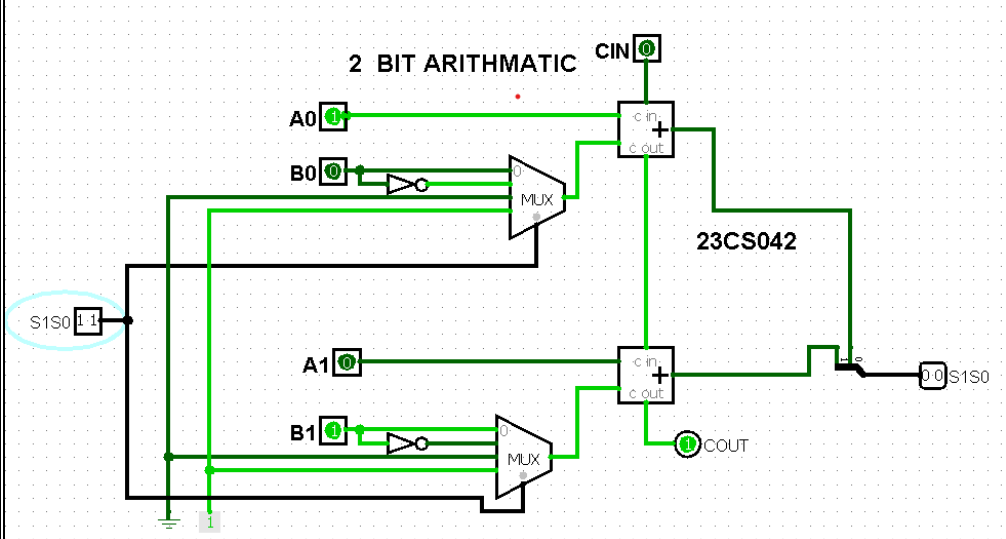
S1S0
A1
B1
MUX
COUT
S1S0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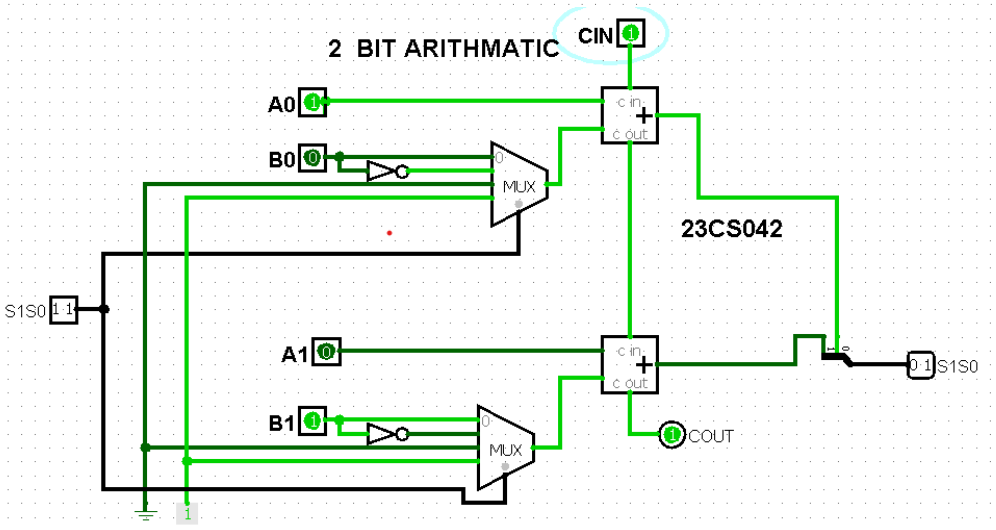
S1S0
A1
B1
COUT
S1S0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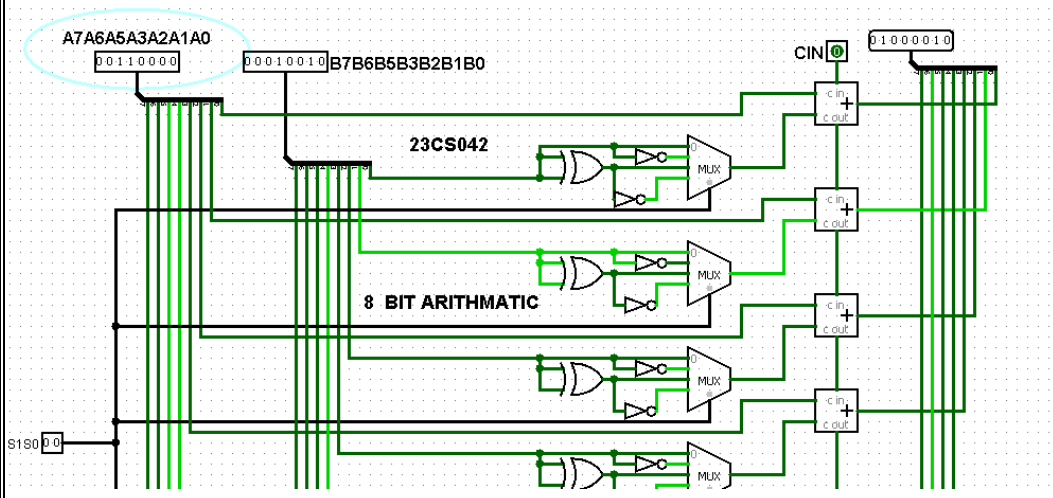
CIN
A0
B0
MUX
23CS042
S1S0
A1
B1
COUT
S1S0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CIN
23CS042
MUX
8 BIT ARITHMATIC
S1S0

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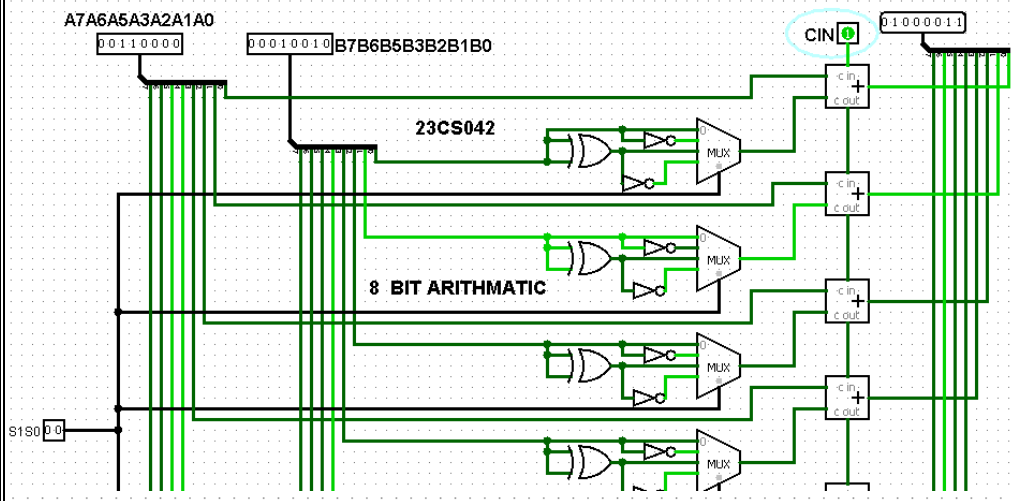
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MUX
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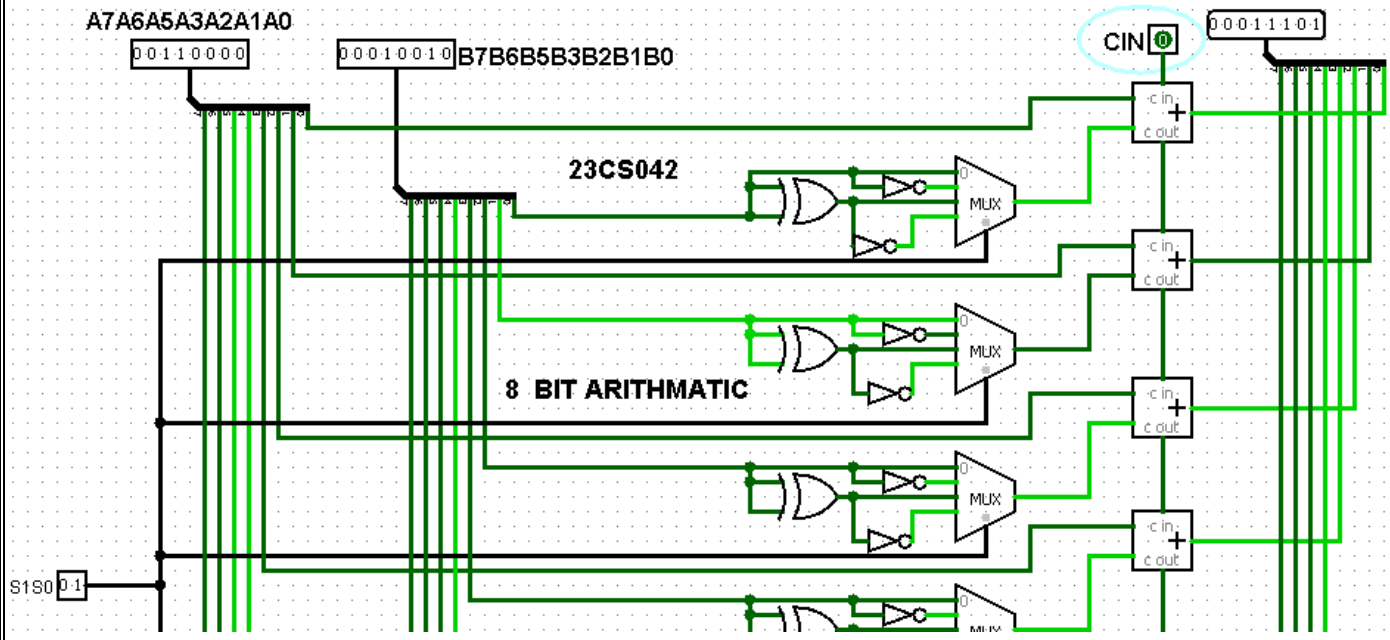
c in
c out
S1S0 00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c in
c out
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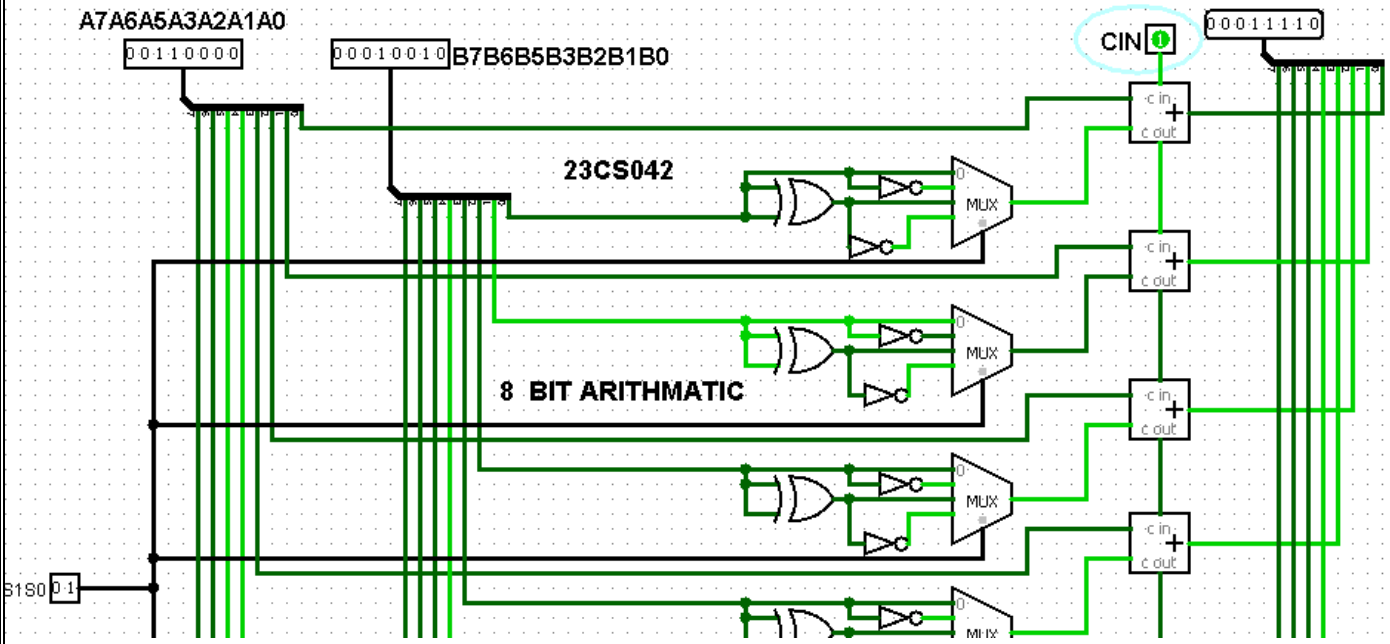
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MUX
8 BIT ARITHMATIC
c in
c out
S1S0 01

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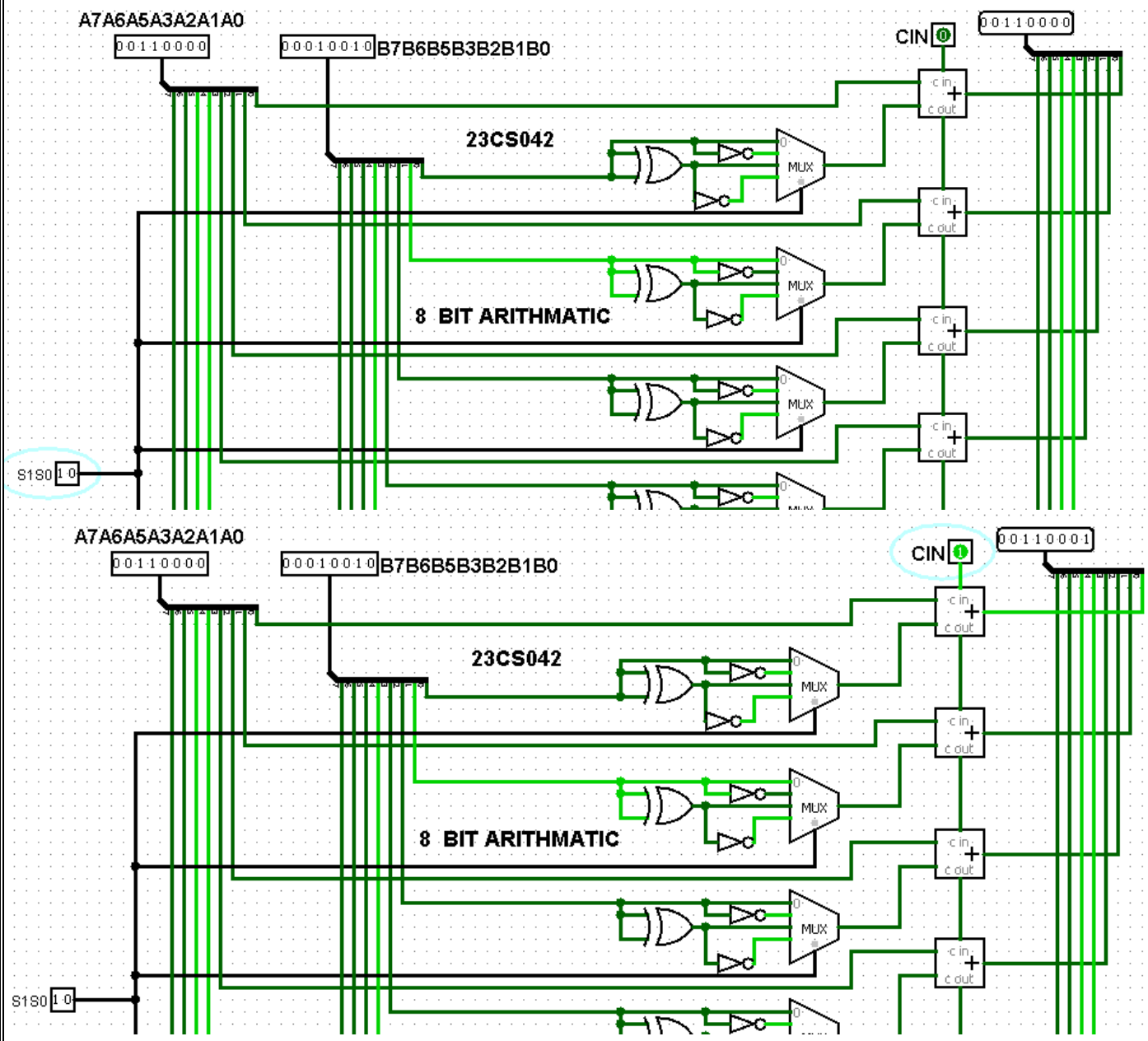
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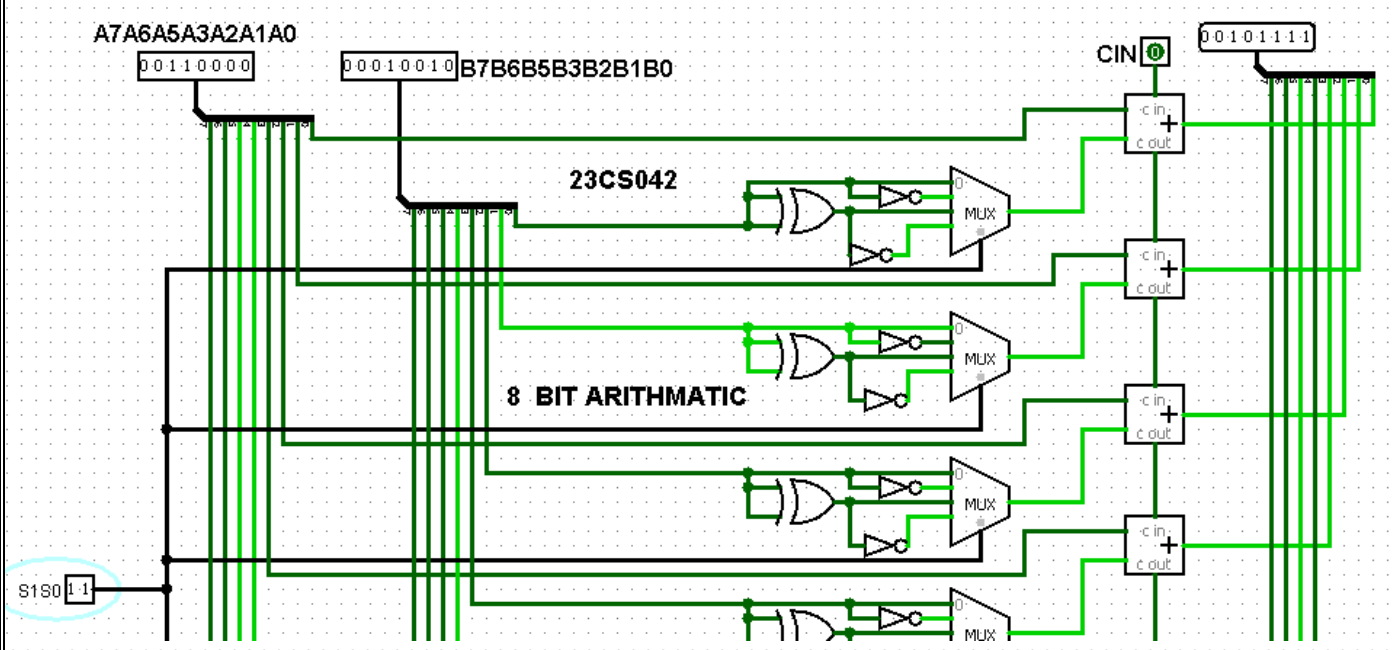
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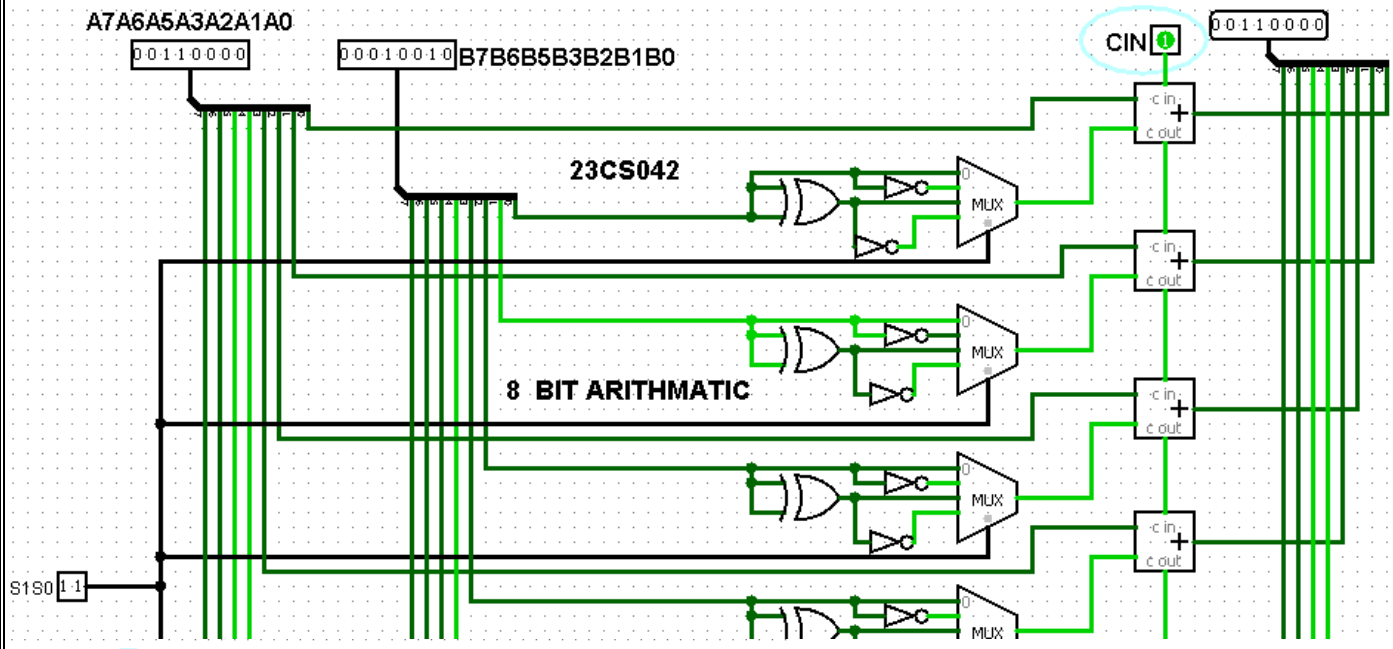
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MUX
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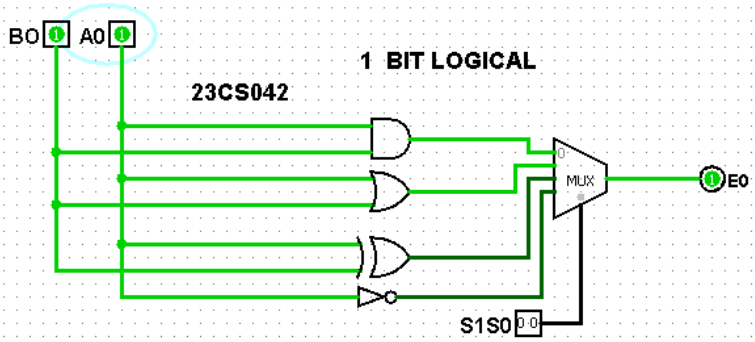
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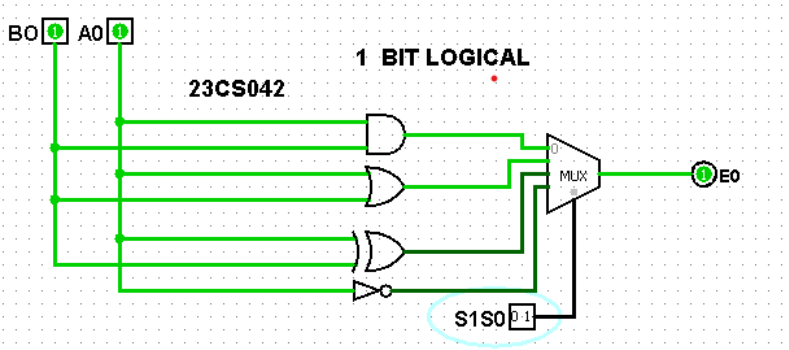
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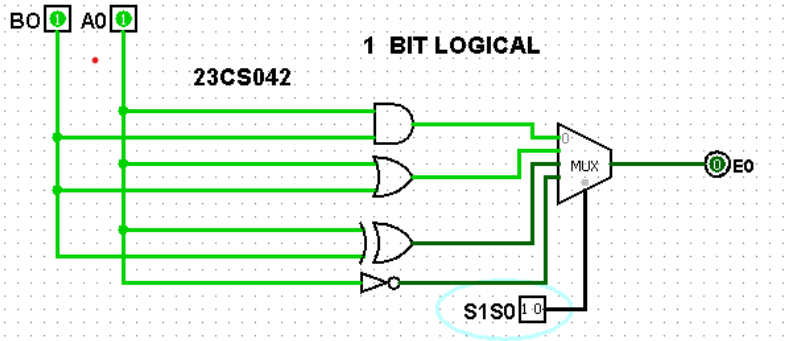
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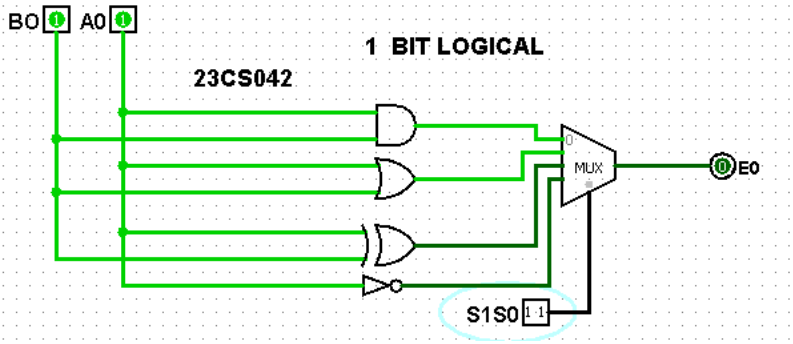
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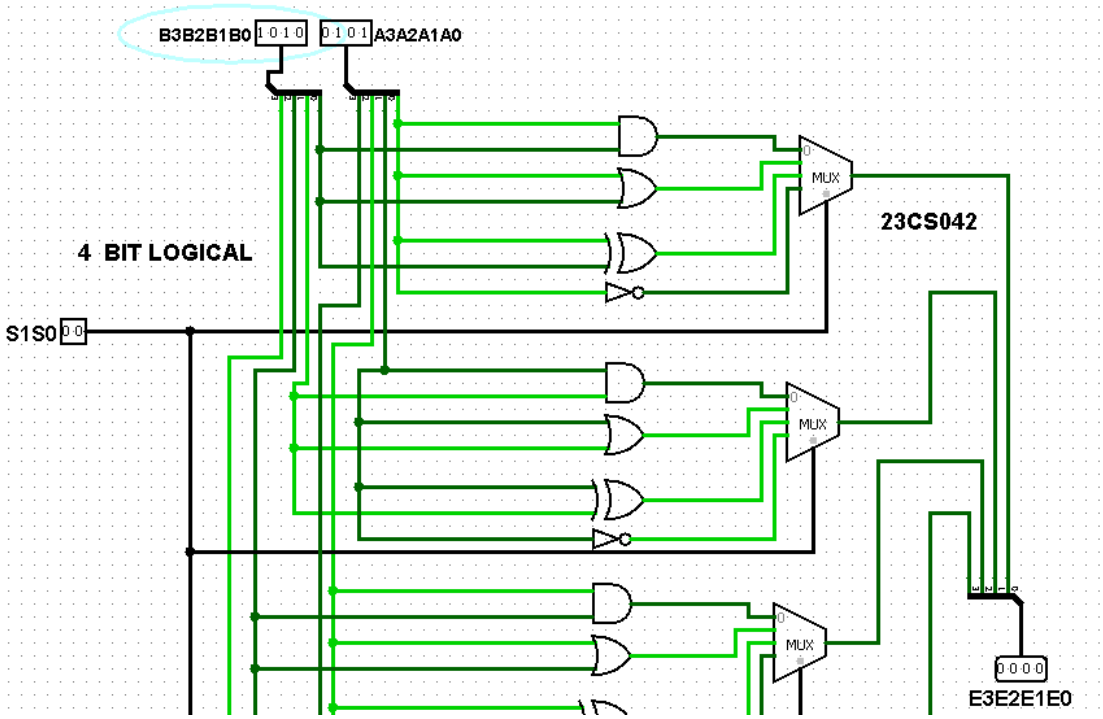
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MUX
MUX
MUX
0000
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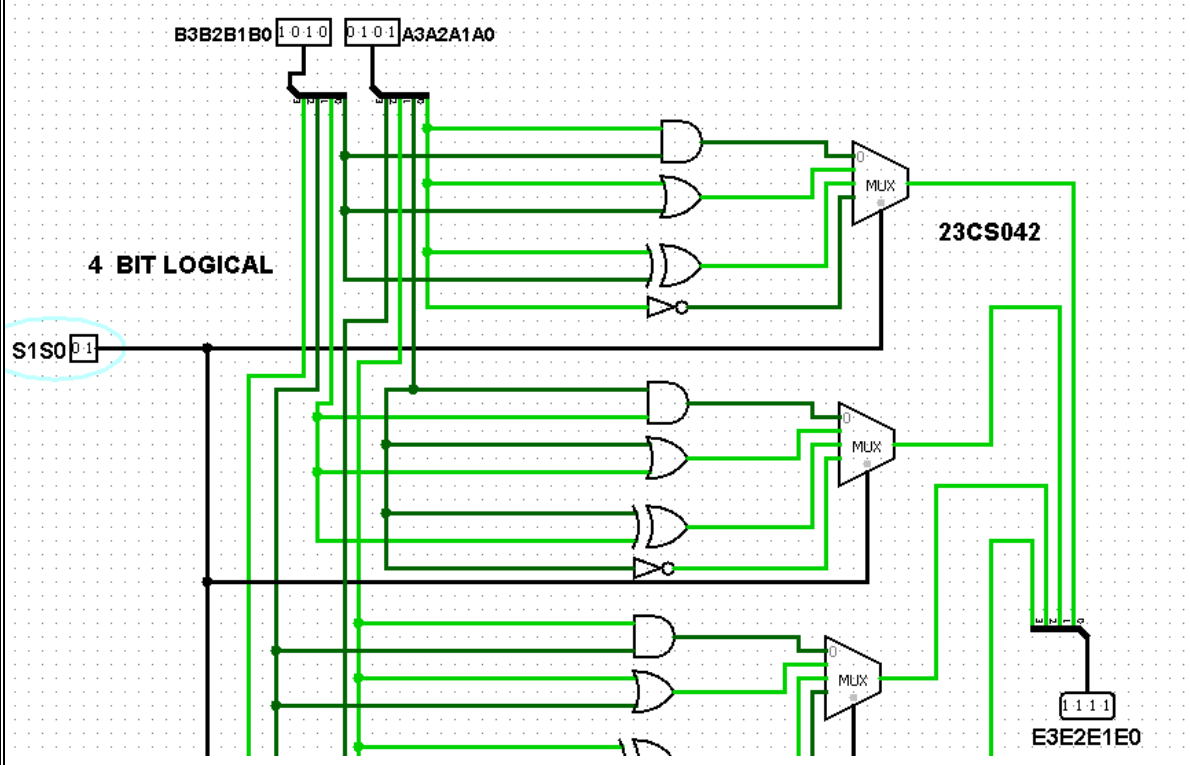
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MUX
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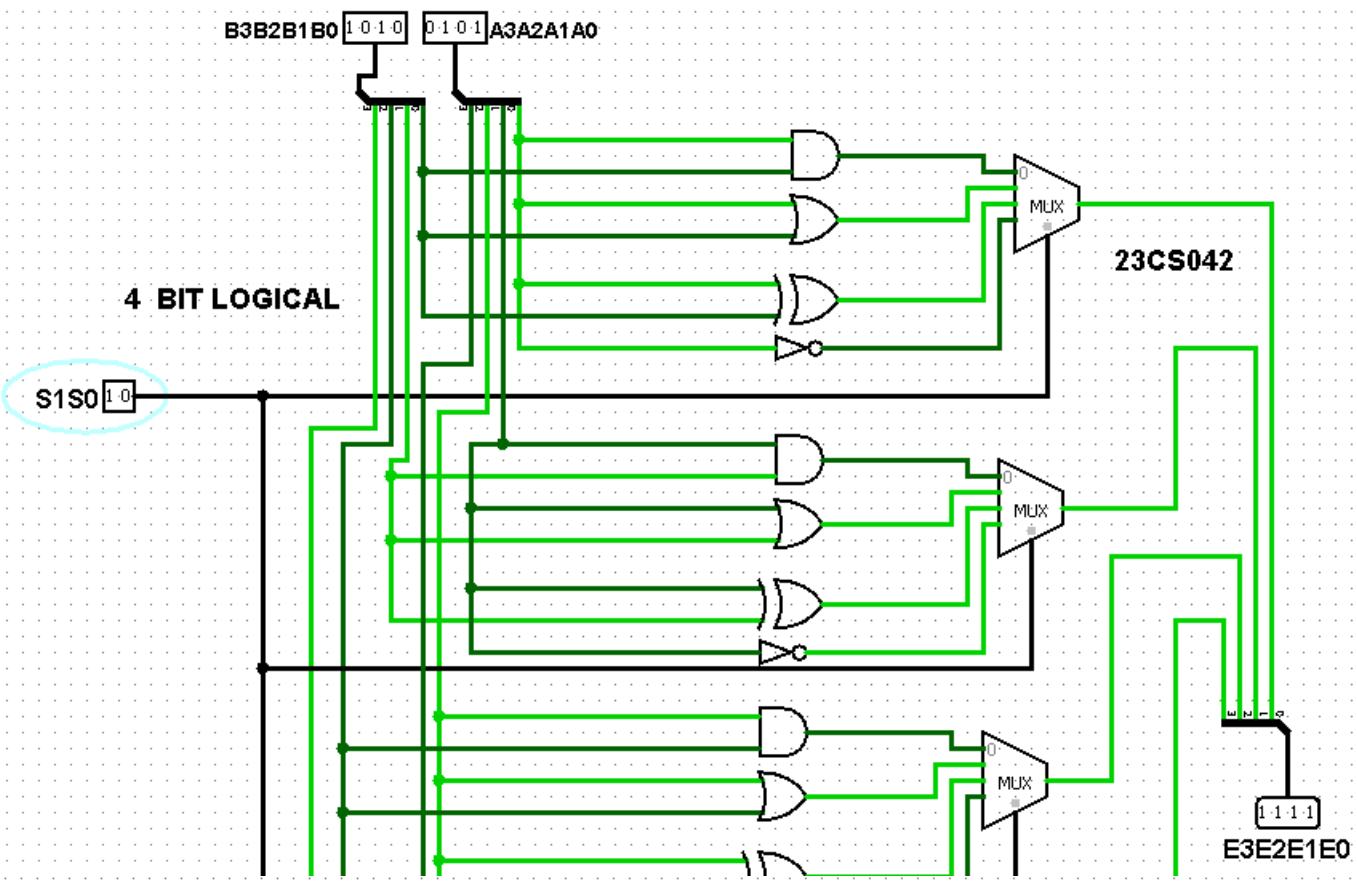
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4 BIT LOGICAL
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MUX
MUX
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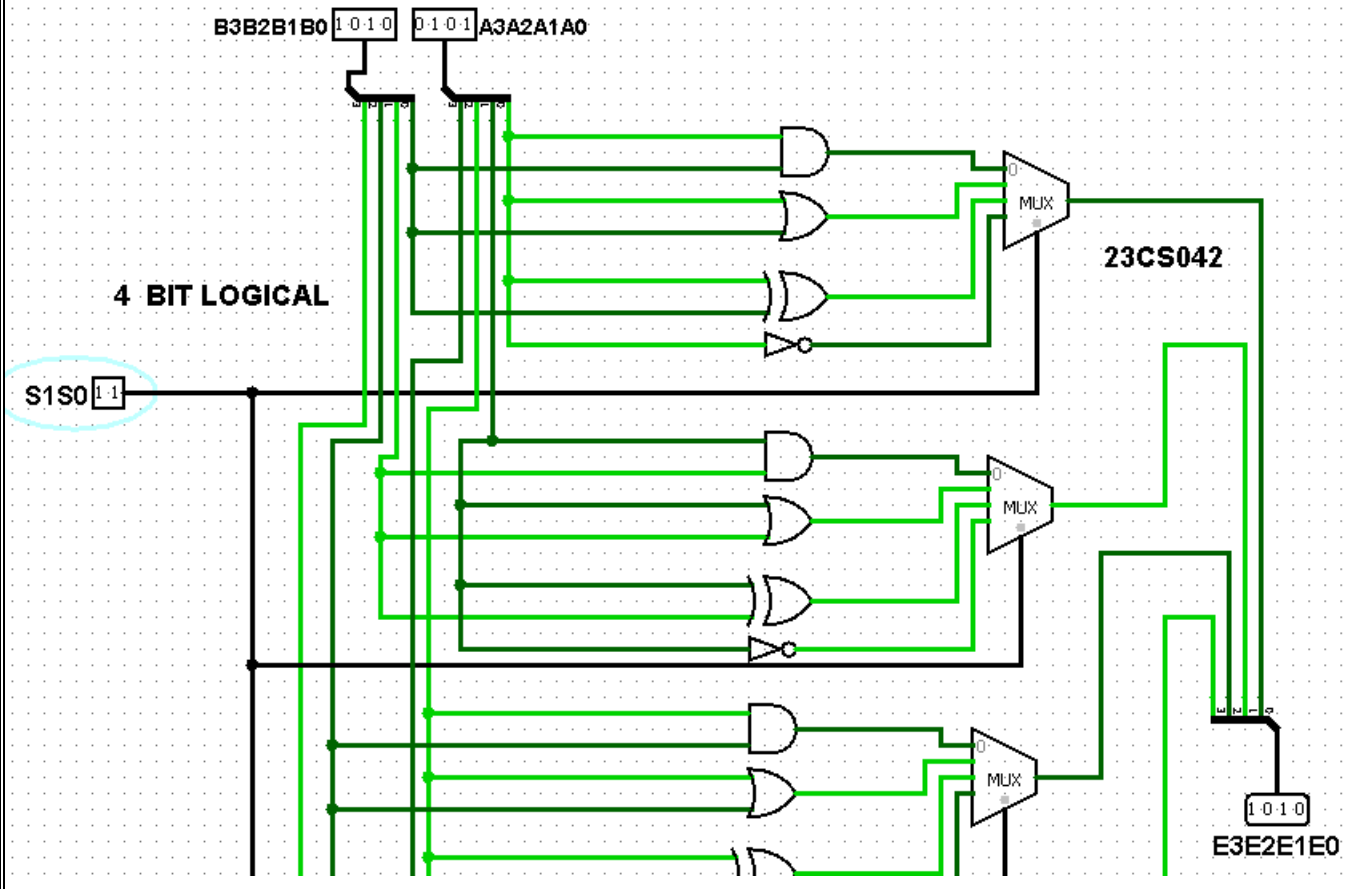
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4 BIT LOGICAL
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S1S0
1 1
MUX
MUX
MUX
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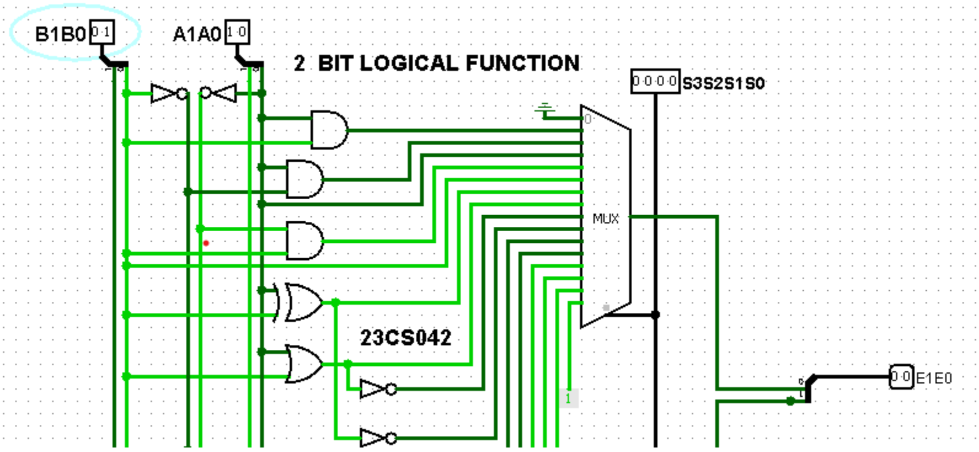
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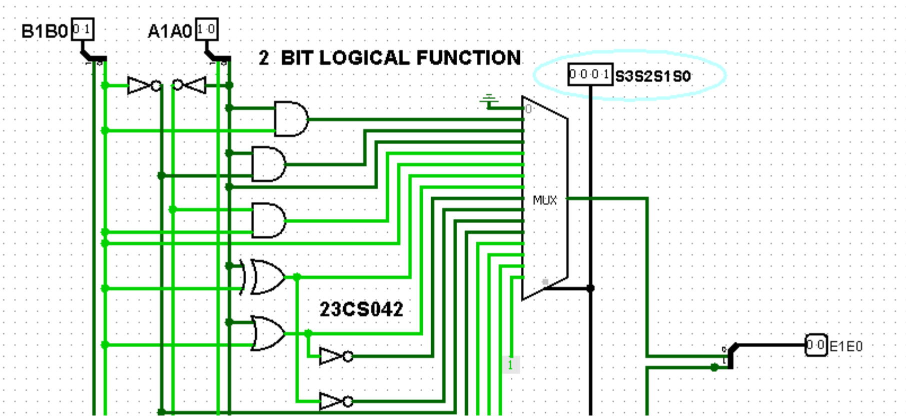
2 BIT LOGICAL FUNCTION
0 0 0 0 S3S2S1S0
MUX
23CS042
0 0 E1E0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0 0 0 1 S3S2S1S0
MUX
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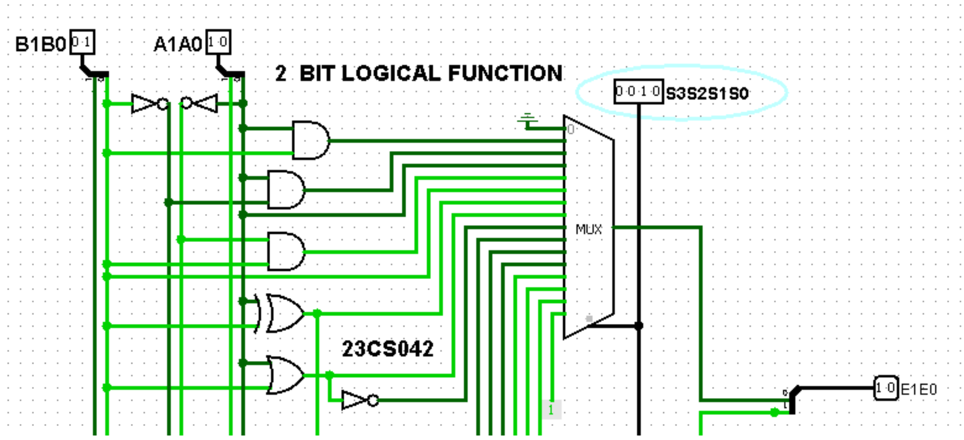
0 0 E1E0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A1A0 1 0
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MUX
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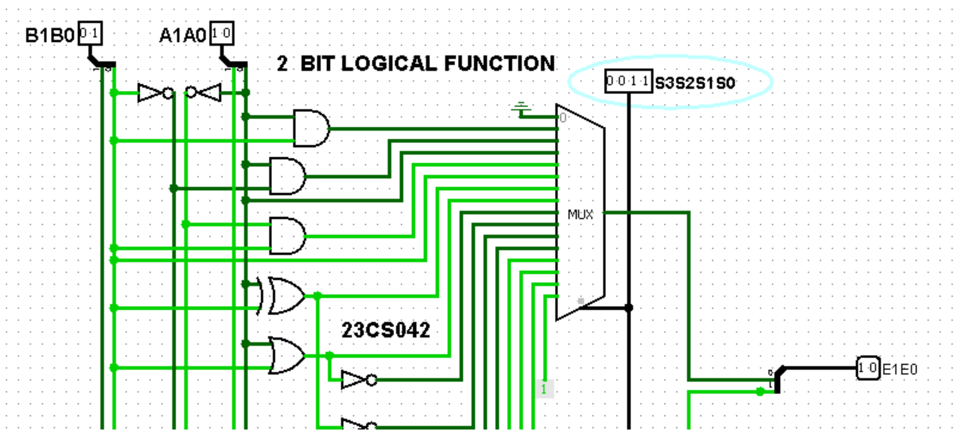
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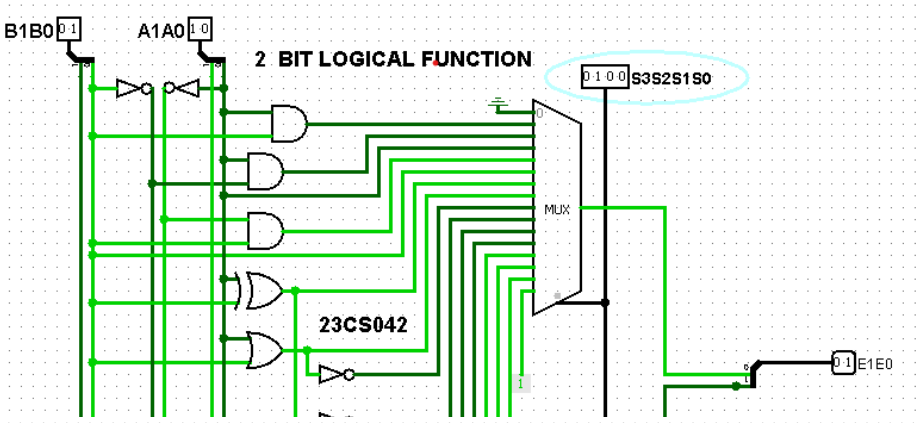
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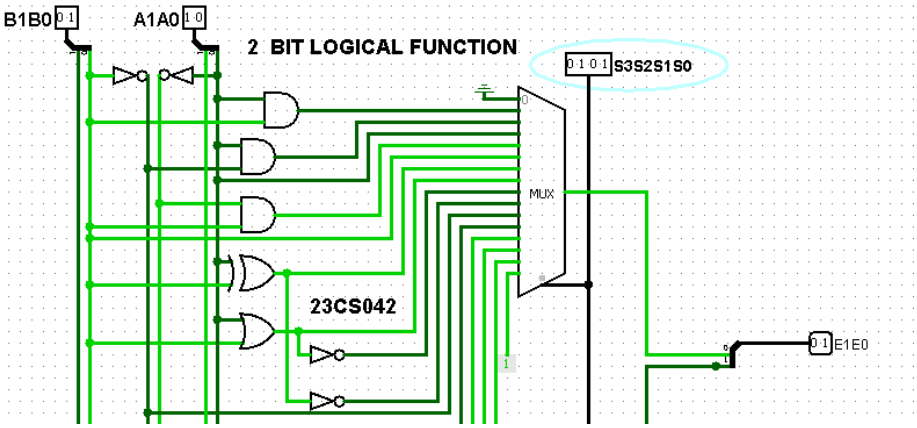
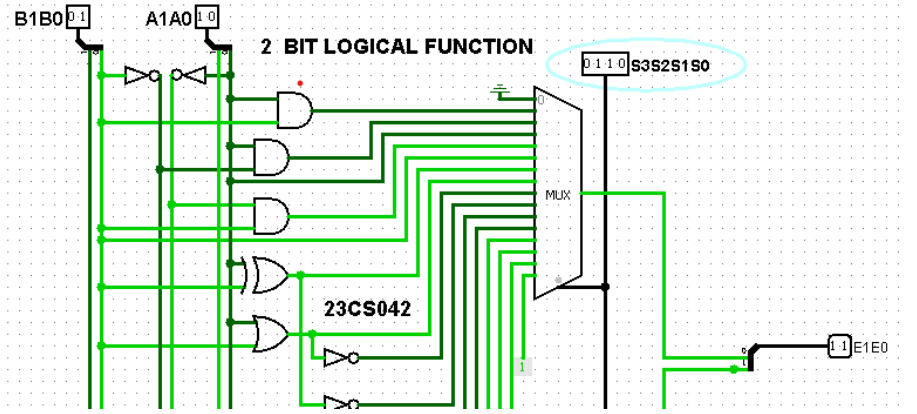
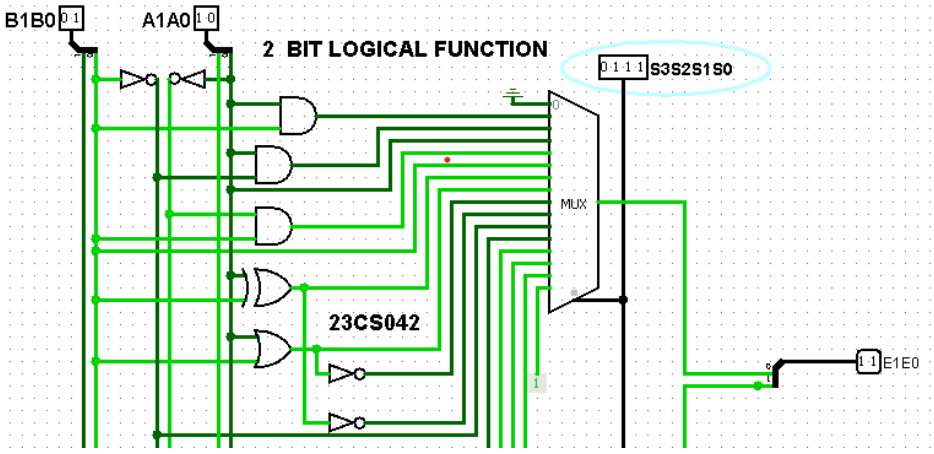
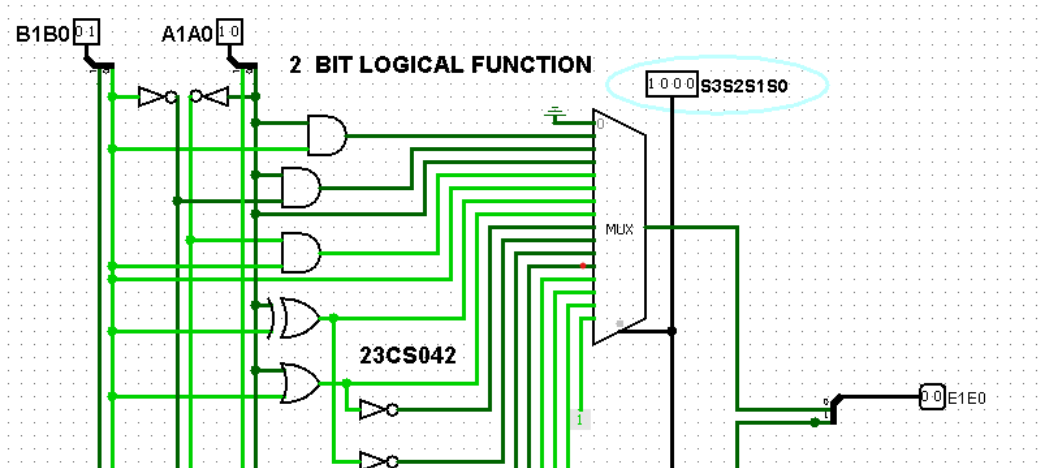
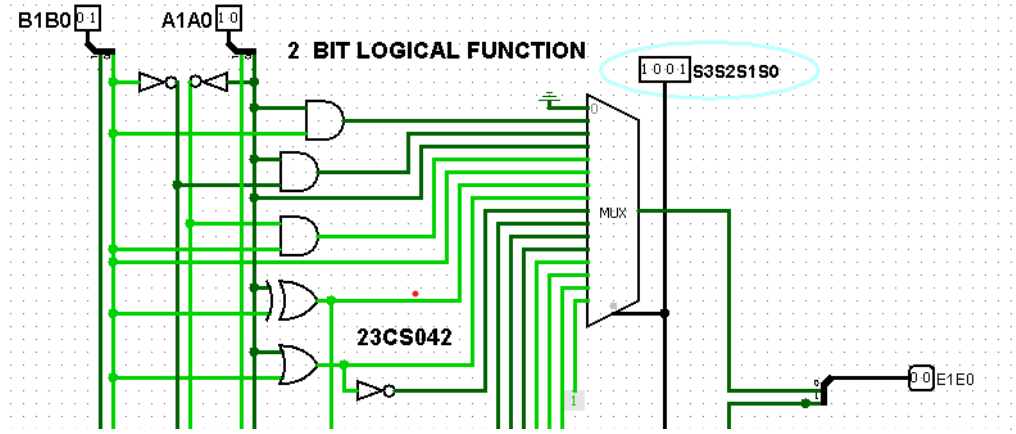
A1A0 1 0
2 BIT LOGICAL FUNCTION
0 1 0 0 S3S2S1S0
MUX
23CS042
0 1 E1E0

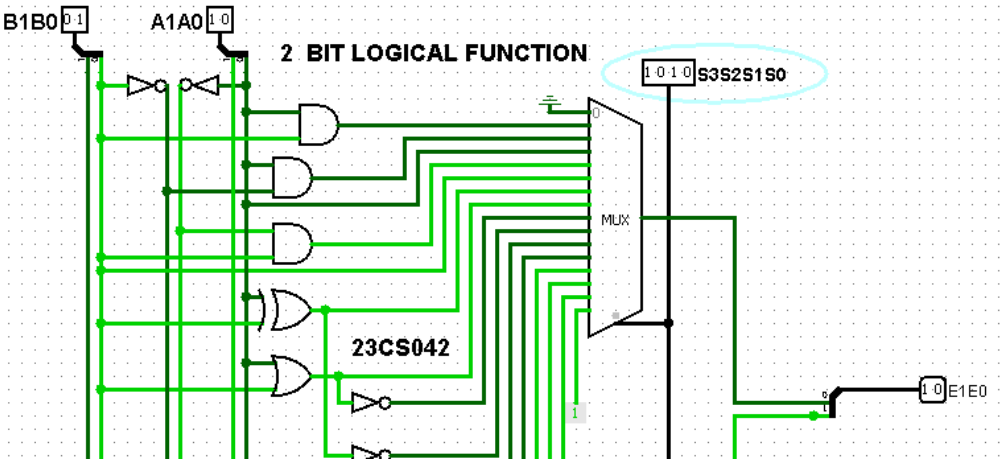

B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
0 1 0 1 S3S2S1S0
MUX
23CS042
0 1 E1E0


B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
0 1 1 0 S3S2S1S0
MUX
23CS042
1 1 E1E0

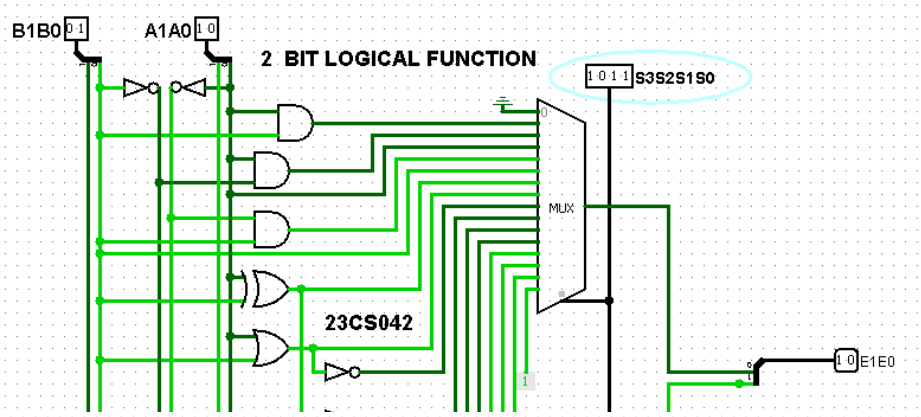

B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
0 1 1 1 S3S2S1S0
MUX
23CS042
1 1 E1E0

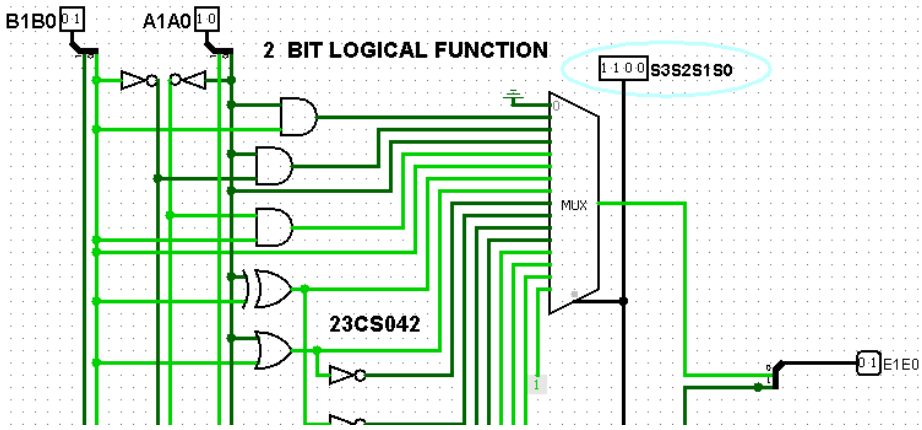

B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
1 0 0 0 S3S2S1S0
MUX
23CS042
0 0 E1E0

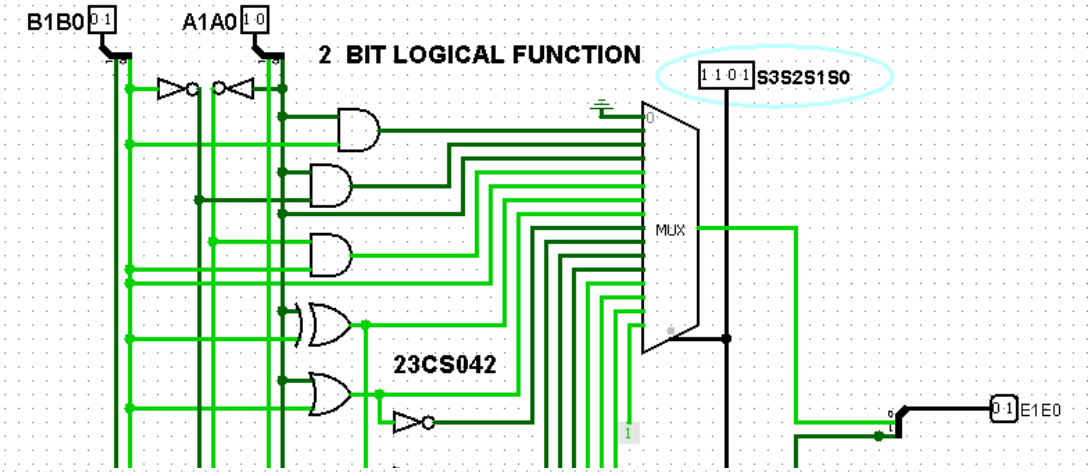

B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
1 0 0 1 S3S2S1S0
MUX
23CS042
0 0 E1E0

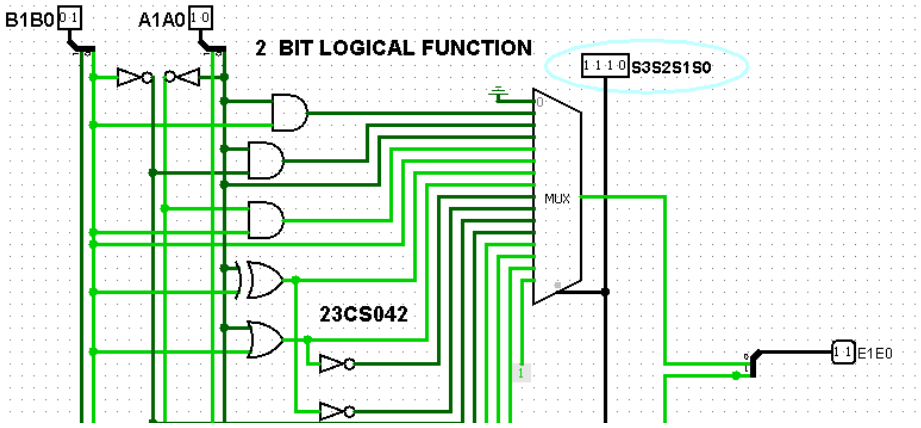

B1B0 0 1
A1A0 1 0
2 BIT LOGICAL FUNCTION
1 0 1 0 S3S2S1S0
MUX
23CS042
1 0 E1E0

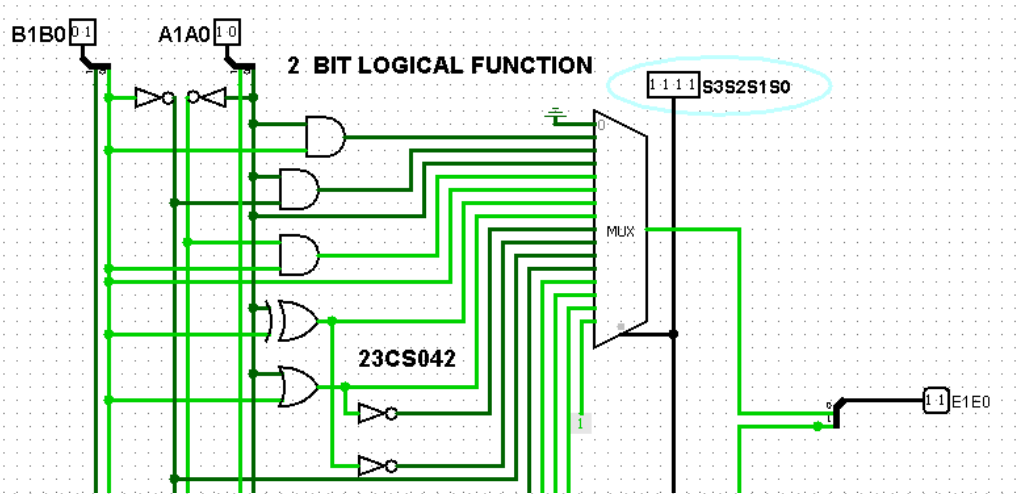
PAGE NO:


B1B0
A1A0
2 BIT LOGICAL FUNCTION
1011 S3S2S1S0
MUX
23CS042
E1E0

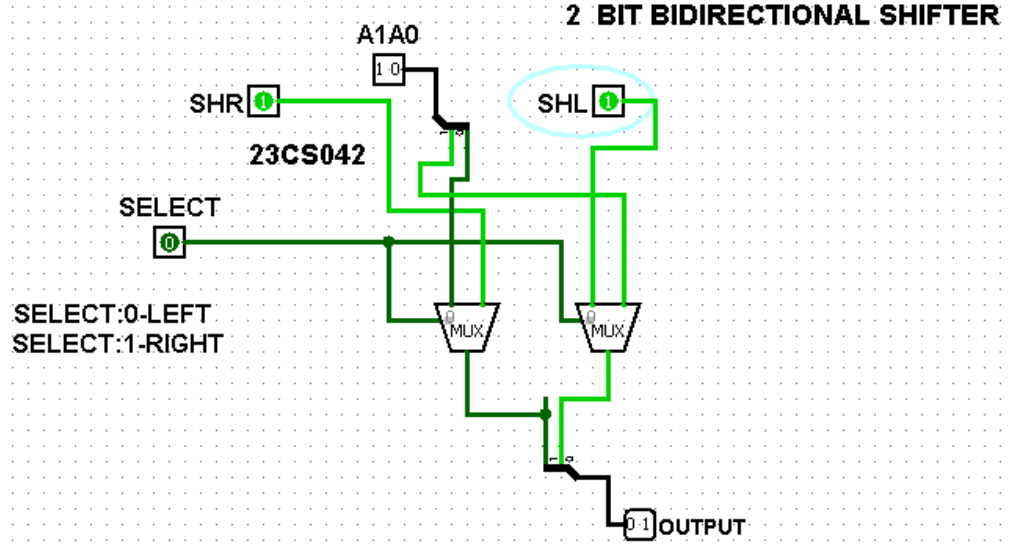

B1B0
A1A0
2 BIT LOGICAL FUNCTION
1100 S3S2S1S0
MUX
23CS042
E1E0


B1B0
A1A0
2 BIT LOGICAL FUNCTION
1101 S3S2S1S0
MUX
23CS042
E1E0

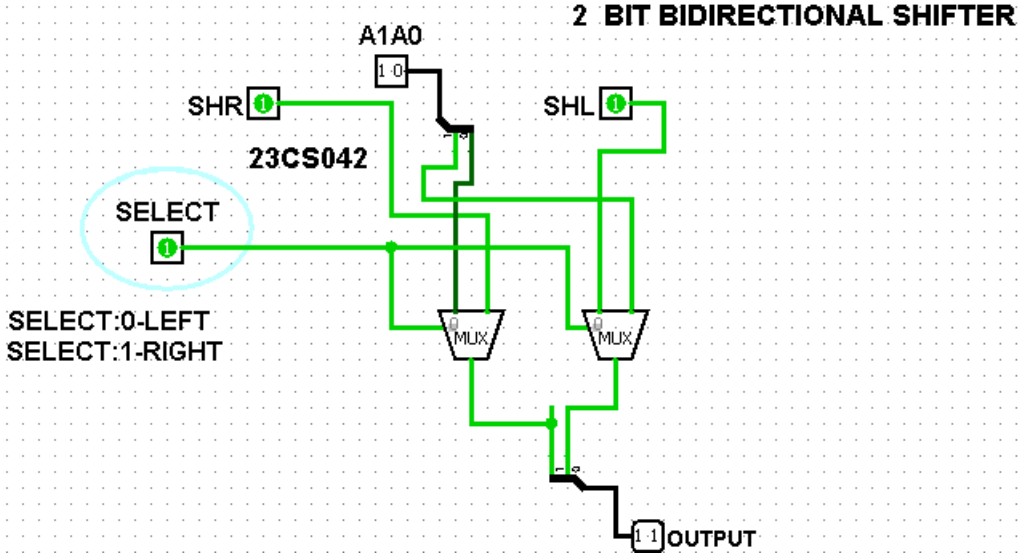

B1B0
A1A0
2 BIT LOGICAL FUNCTION
1110 S3S2S1S0
MUX
23CS042
E1E0

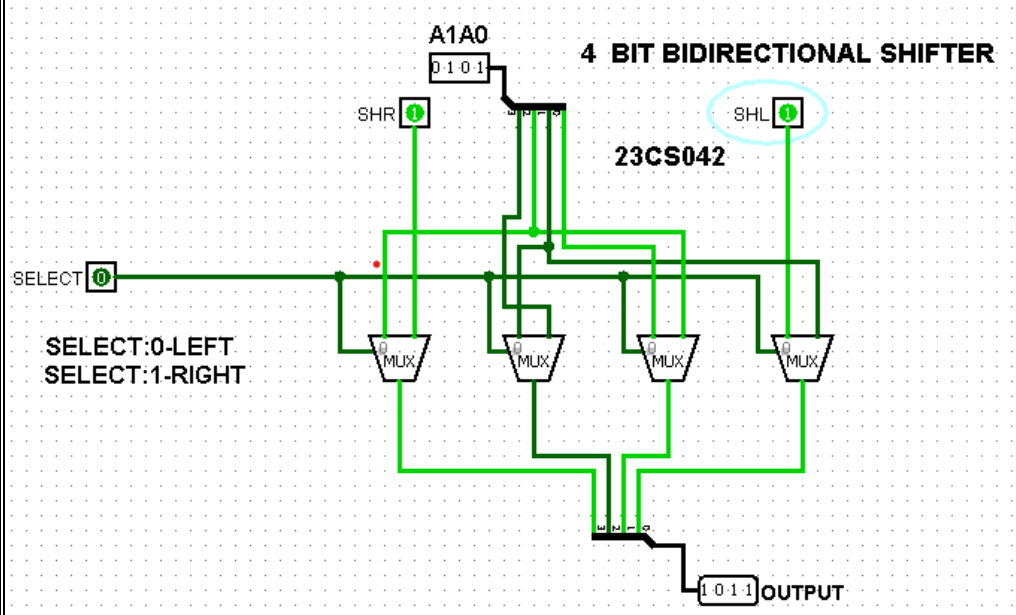


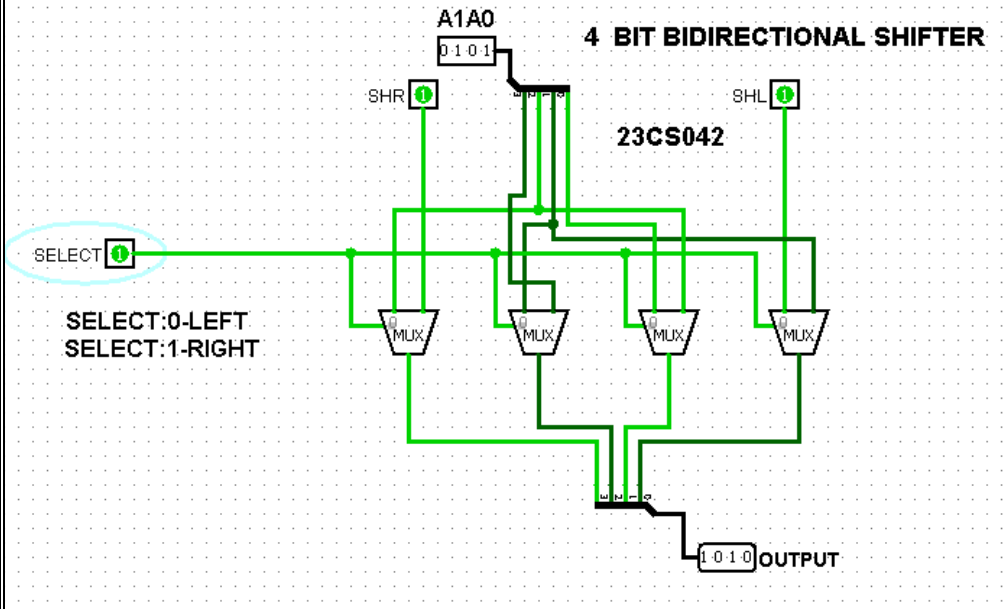
2 BIT BIDIRECTIONAL SHIFTER

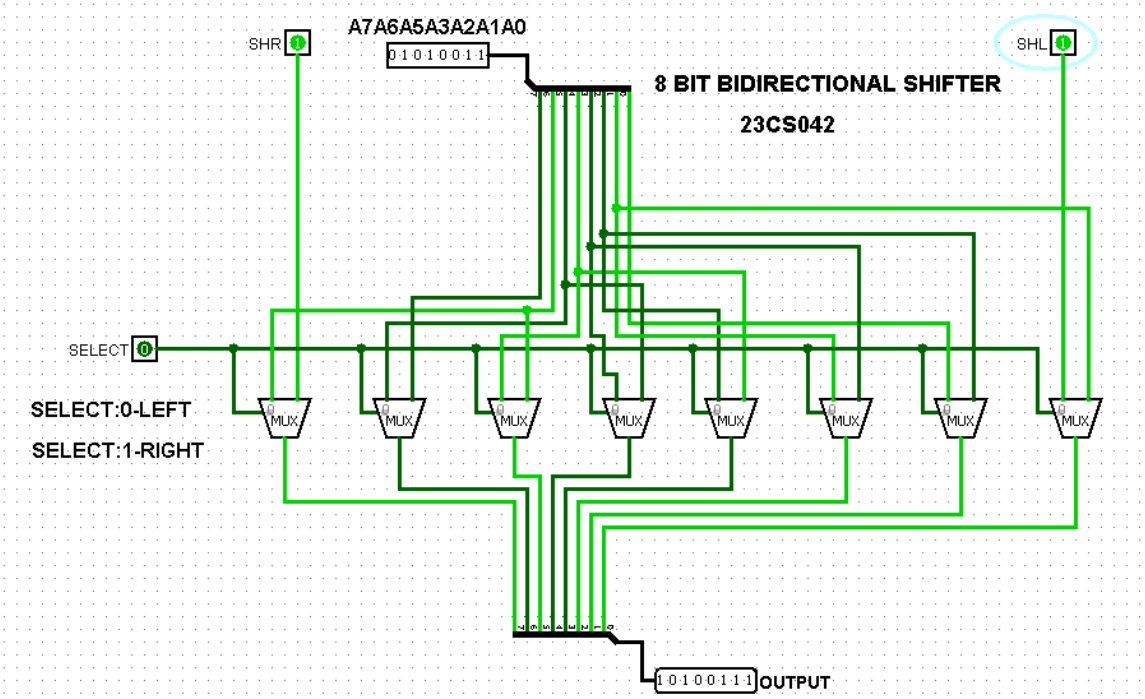


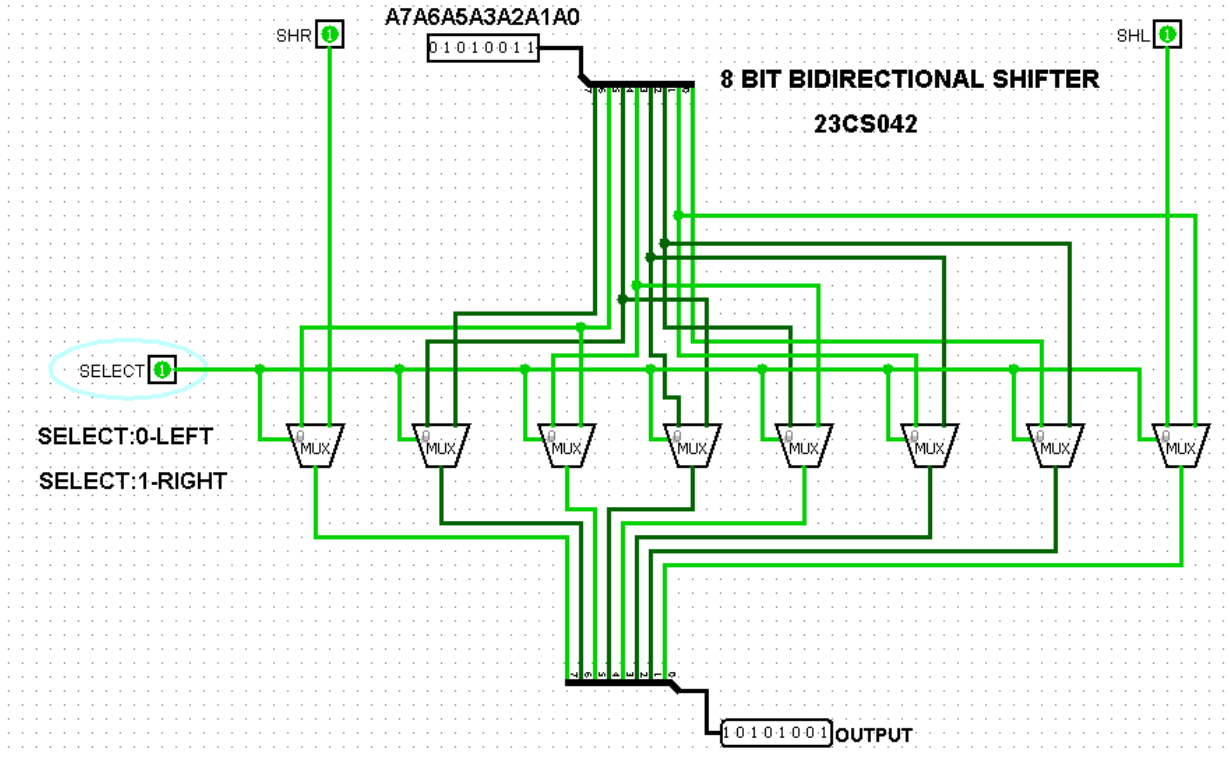
2 BIT BIDIRECTIONAL SHIFTER

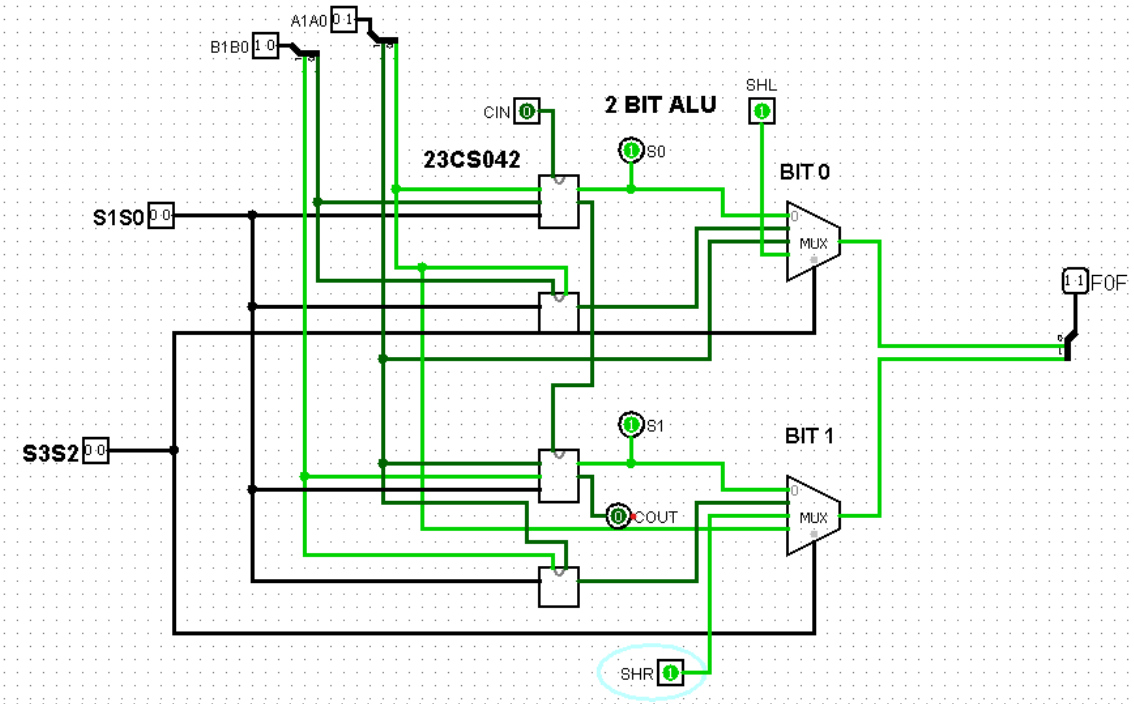


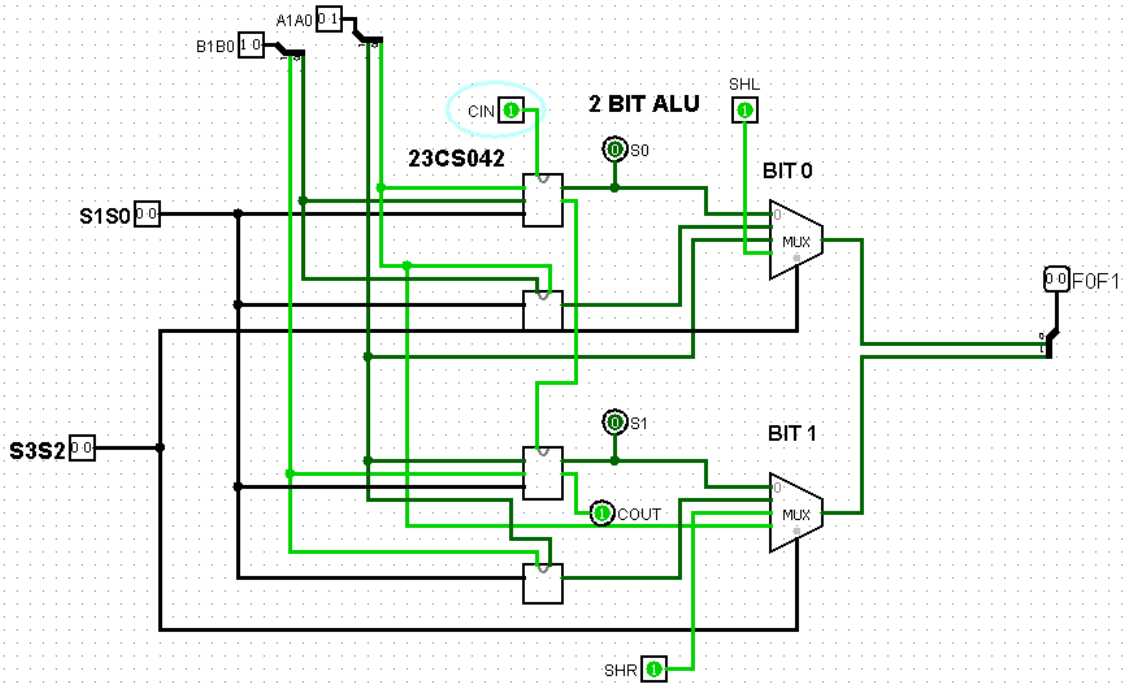

A1A0
0 1 0 1
4 BIT BIDIRECTIONAL SHIFTER
SHR
SHL
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
MUX
MUX
3 2 1 0
1 0 1 1
OUTPUT


A1A0
0 1 0 1
4 BIT BIDIRECTIONAL SHIFTER
SHR
SHL
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
MUX
MUX
MUX
3 2 1 0
1 0 1 0
OUTPUT

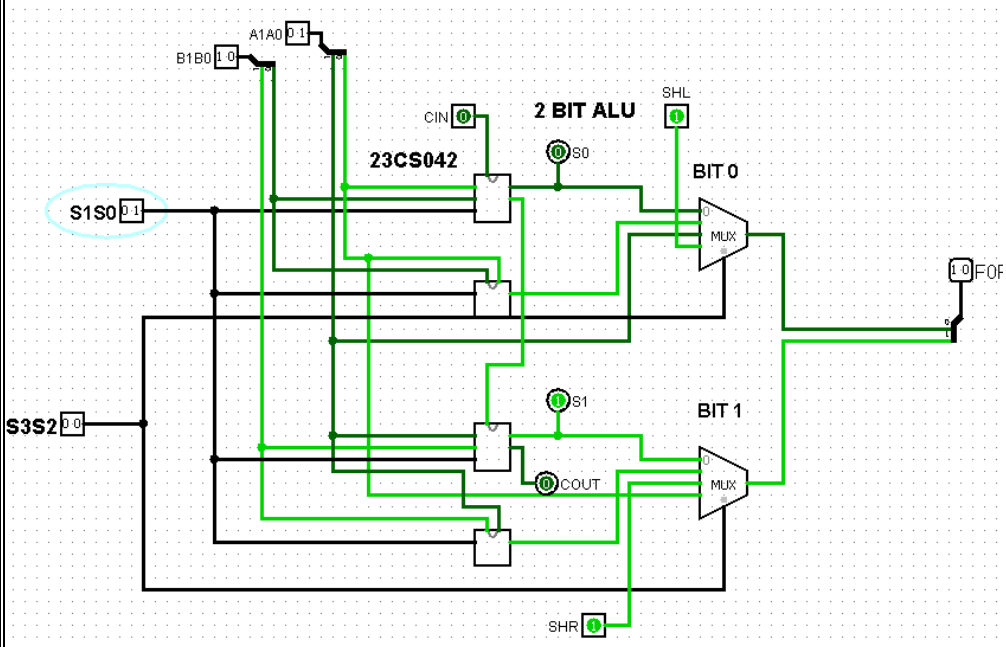

A7A6A5A3A2A1A0
01010011
SHR
SHL
8 BIT BIDIRECTIONAL SHIFTER
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
10100111
OUTPUT

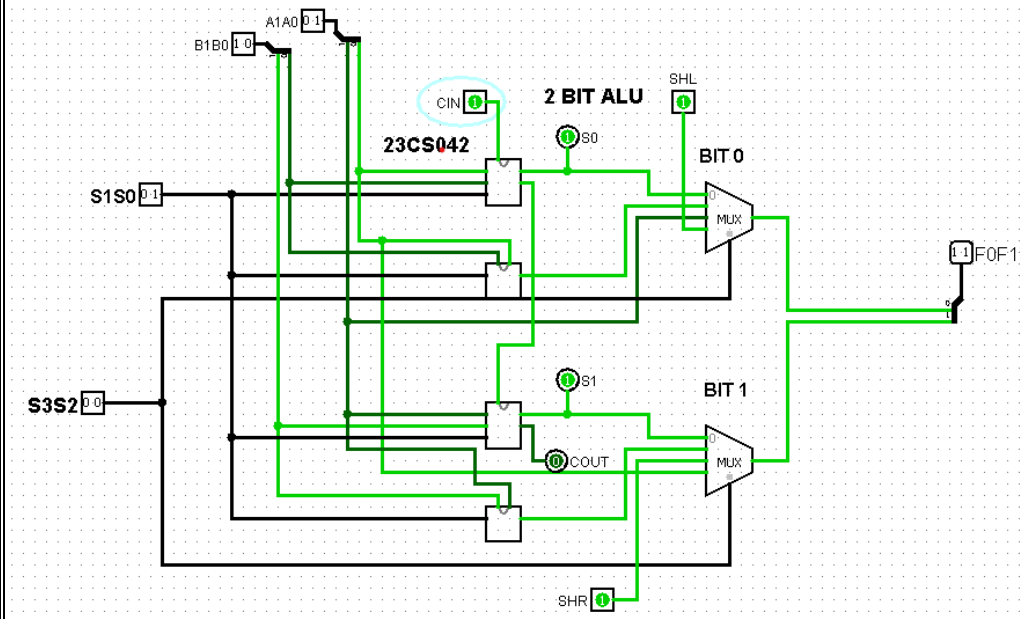

A7A6A5A3A2A1A0
01010011
SHR
SHL
8 BIT BIDIRECTIONAL SHIFTER
23CS042
SELECT
SELECT:0-LEFT
SELECT:1-RIGHT
MUX
10101001
OUTPUT

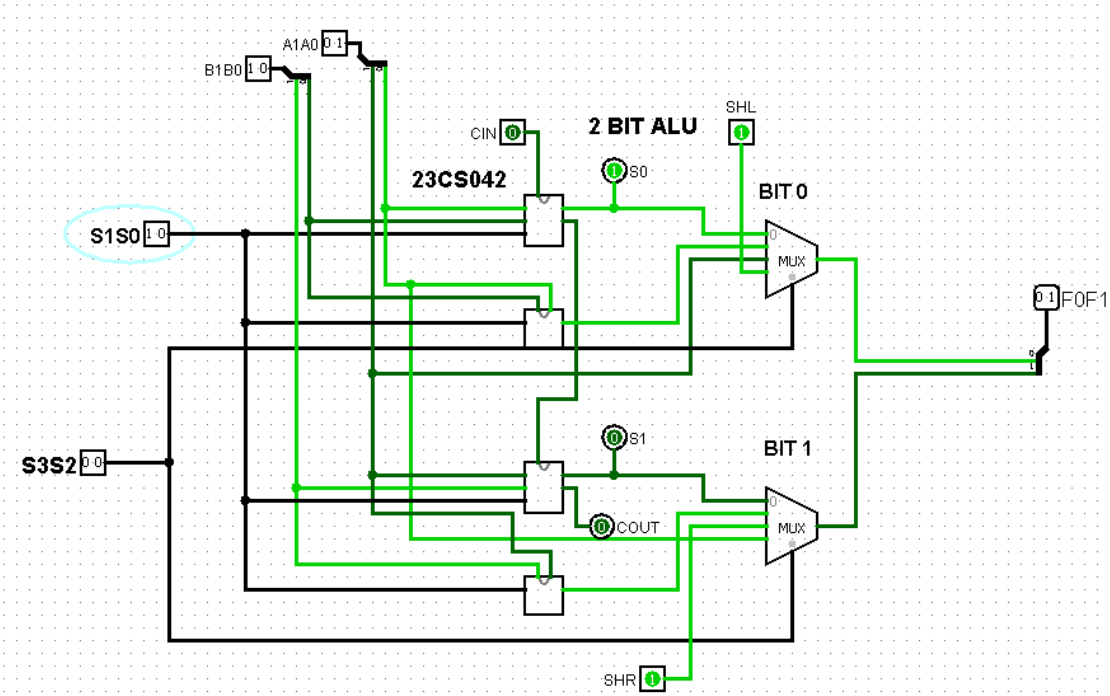

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F
S1
BIT 1
S3S2
COUT
MUX
SHR

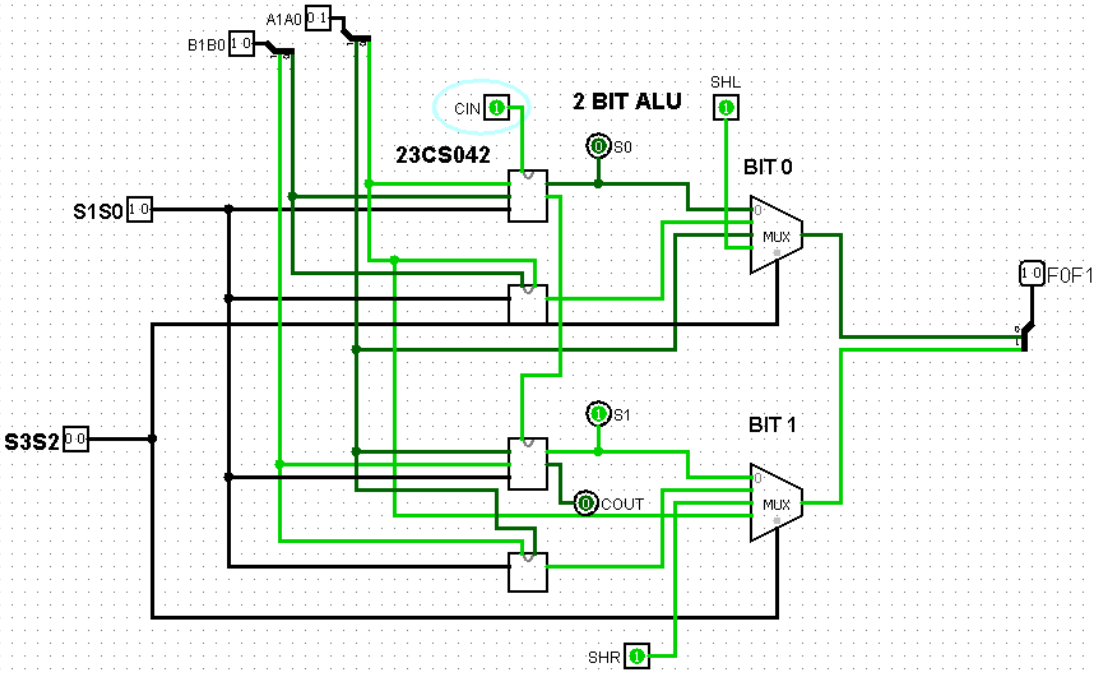

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S1
BIT 1
S3S2
COUT
MUX
SHR

PAGE NO:

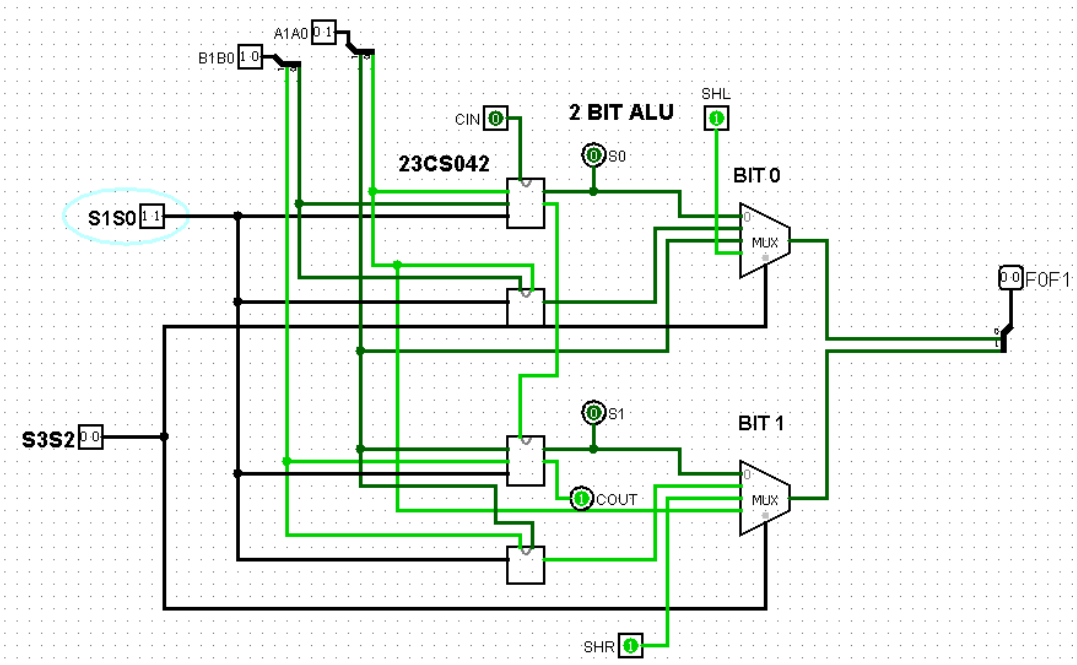

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F
S3S2
S1
BIT 1
COUT
MUX
SHR

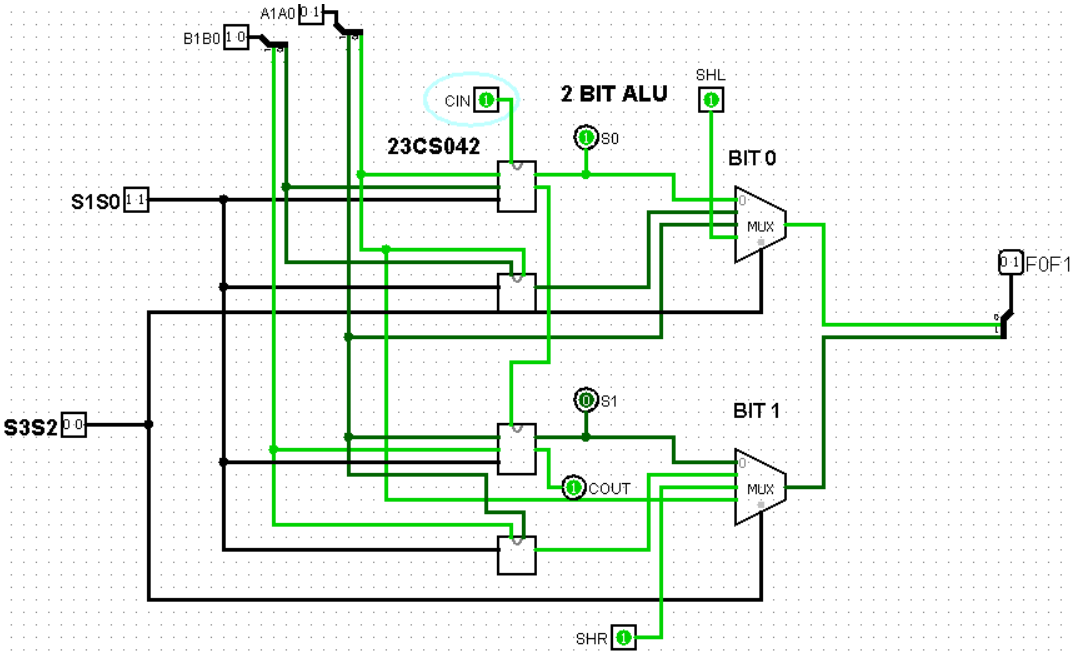

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

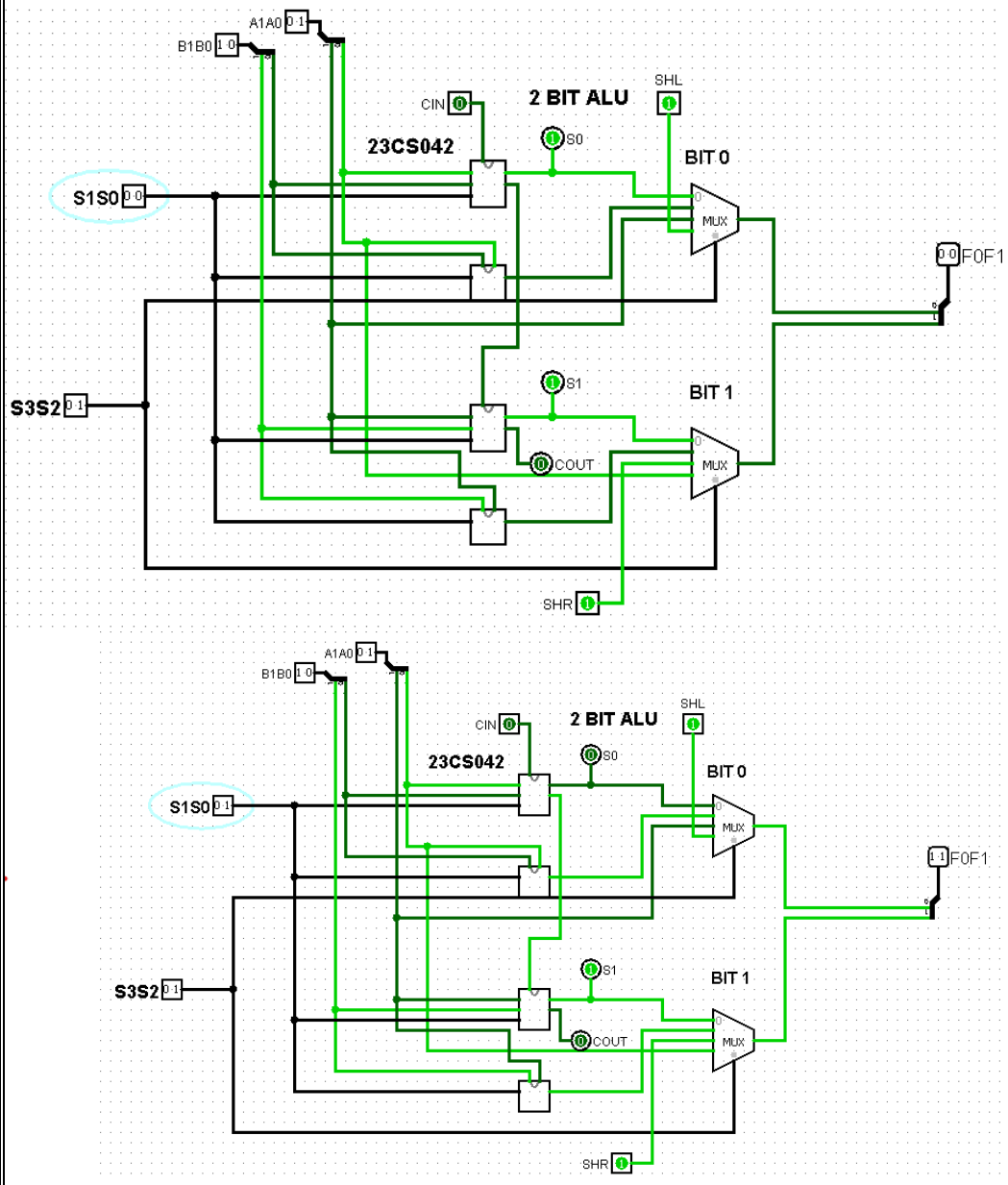

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR


A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

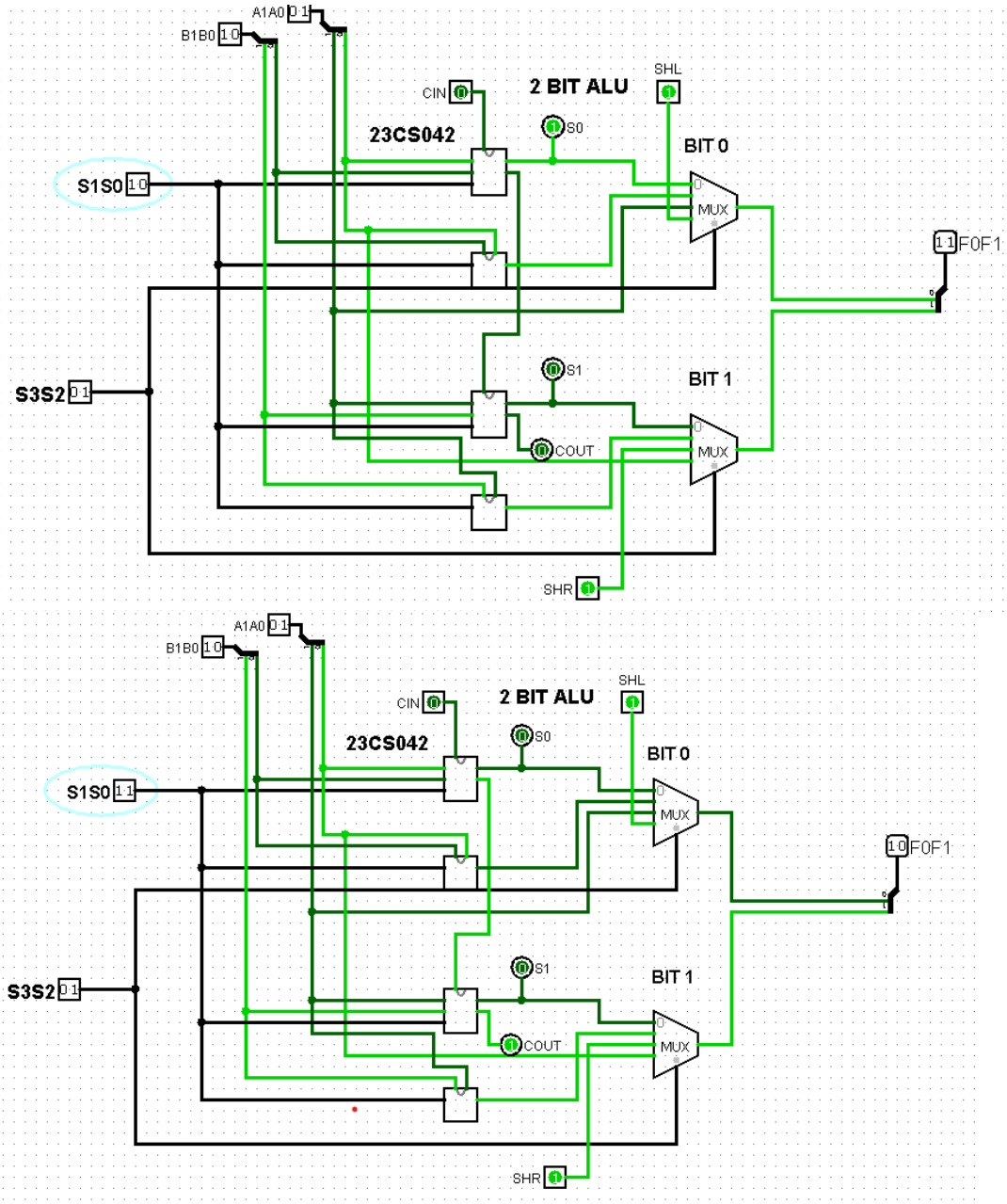
PAGE NO:


A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

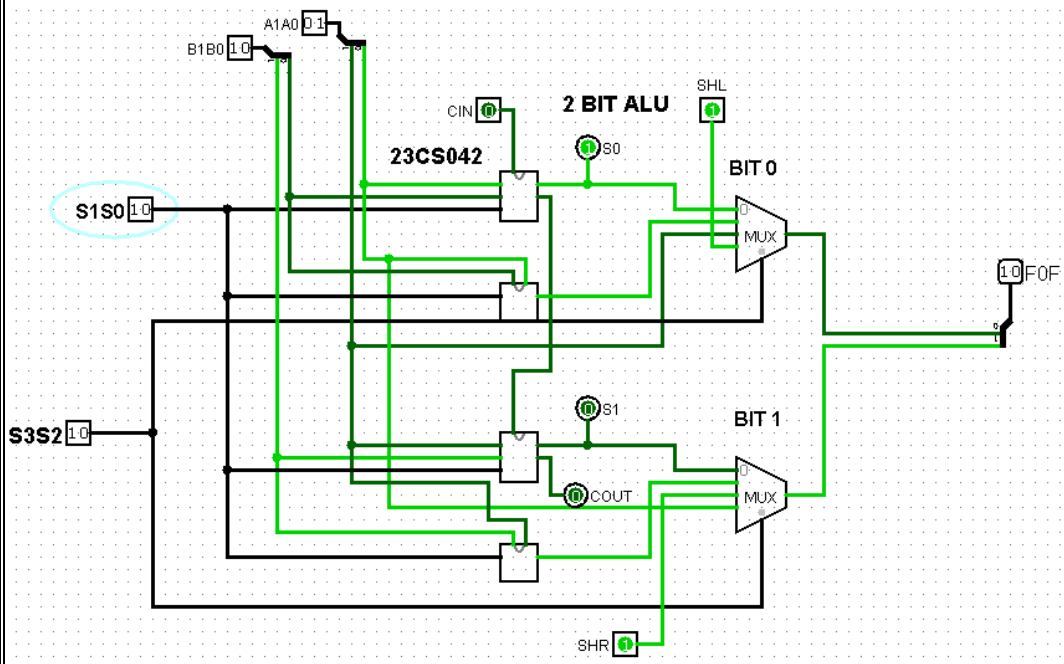

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

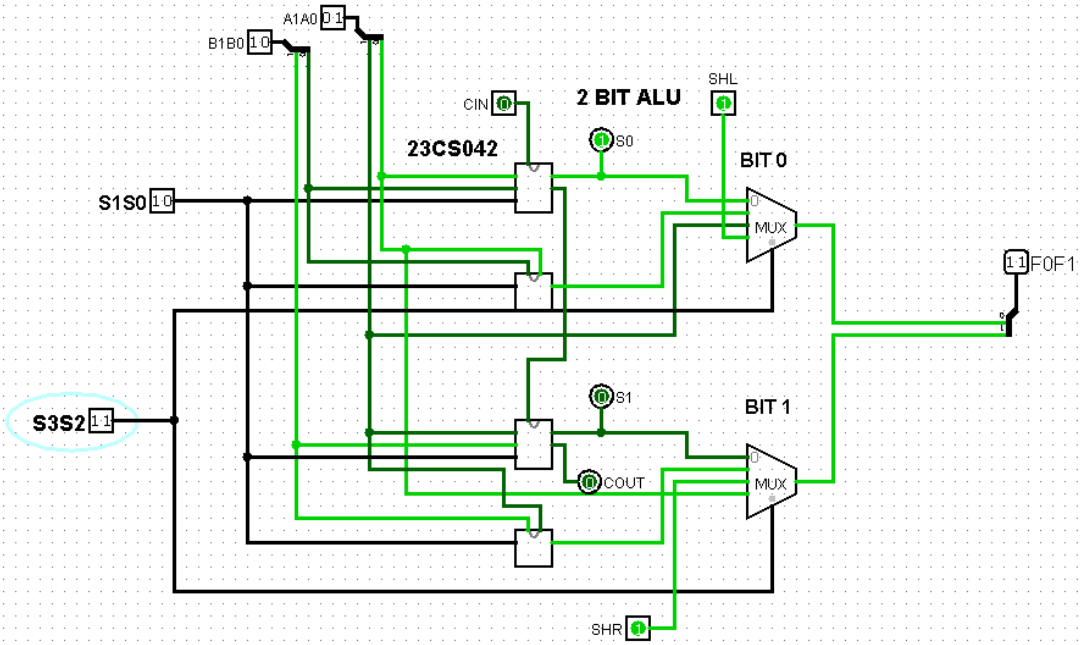

A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

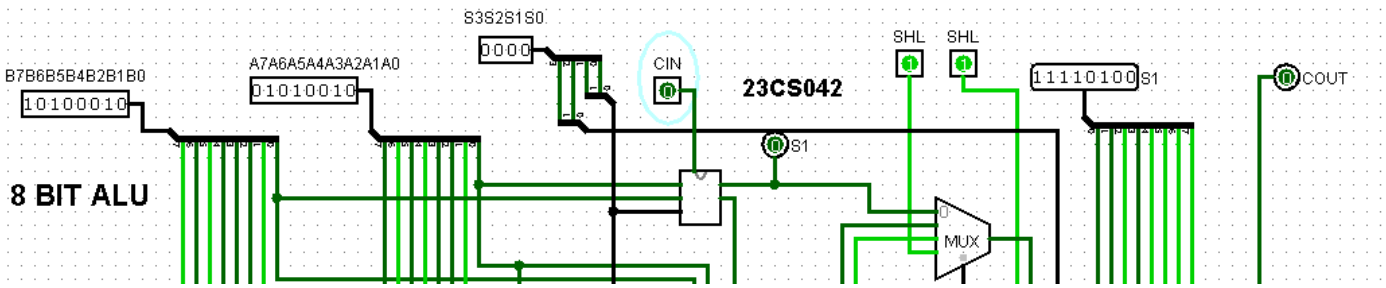
A1A0
B1B0
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0
MUX
F0F1
S3S2
S1
BIT 1
COUT
MUX
SHR

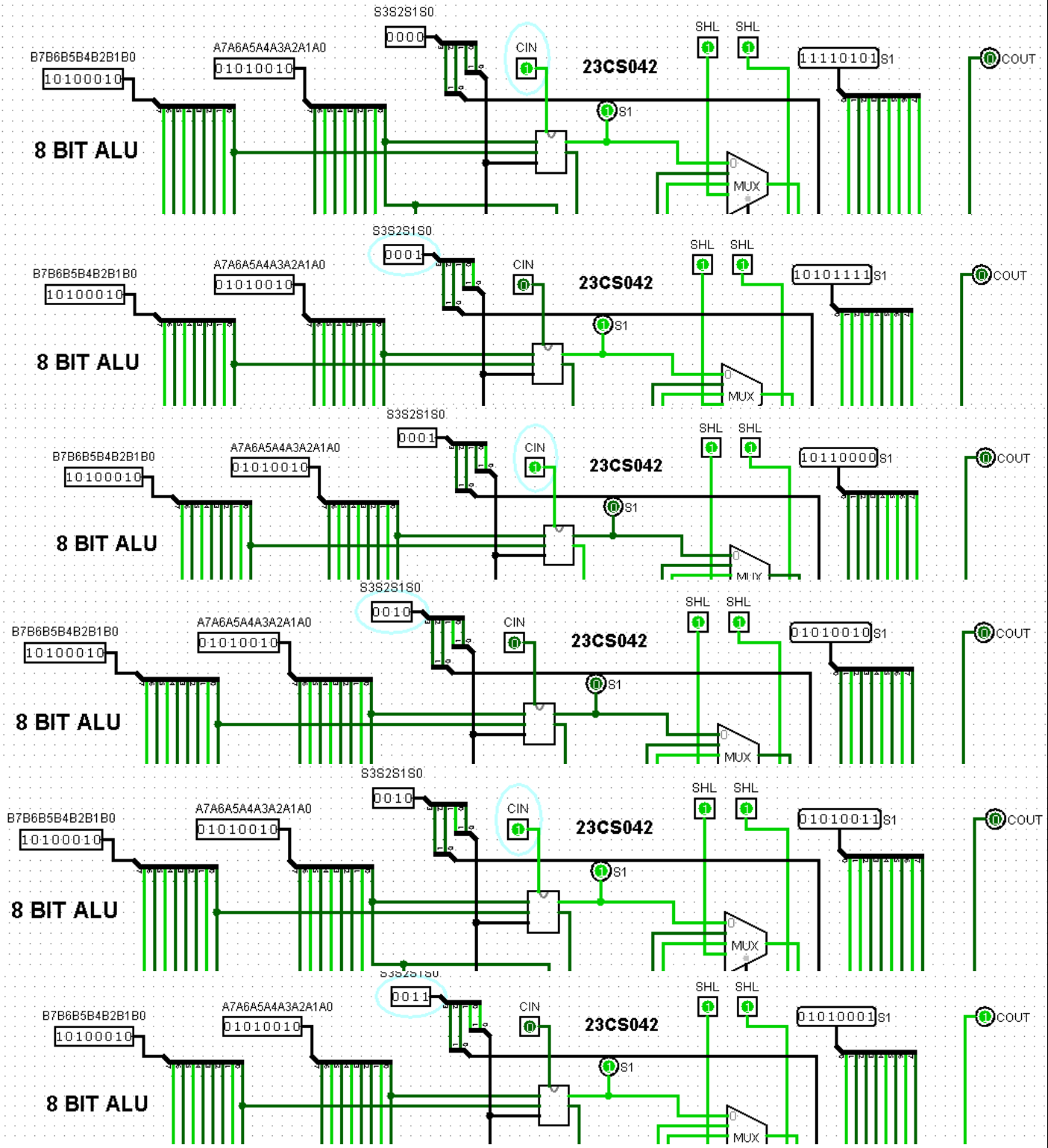

A1A0 0 1
B1B0 1 0
CIN 0
2 BIT ALU
23CS042
SHL 1
S0
BIT 0
S1S0 1 0
MUX
1 1 F0F1
S3S2 0 1
S1
BIT 1
COUT
MUX
SHR 1
A1A0 0 1
B1B0 1 0
CIN 0
2 BIT ALU
23CS042
SHL 1
S0
BIT 0
S1S0 1 1
MUX
1 0 F0F1
S3S2 0 1
S1
BIT 1
COUT
MUX
SHR 1

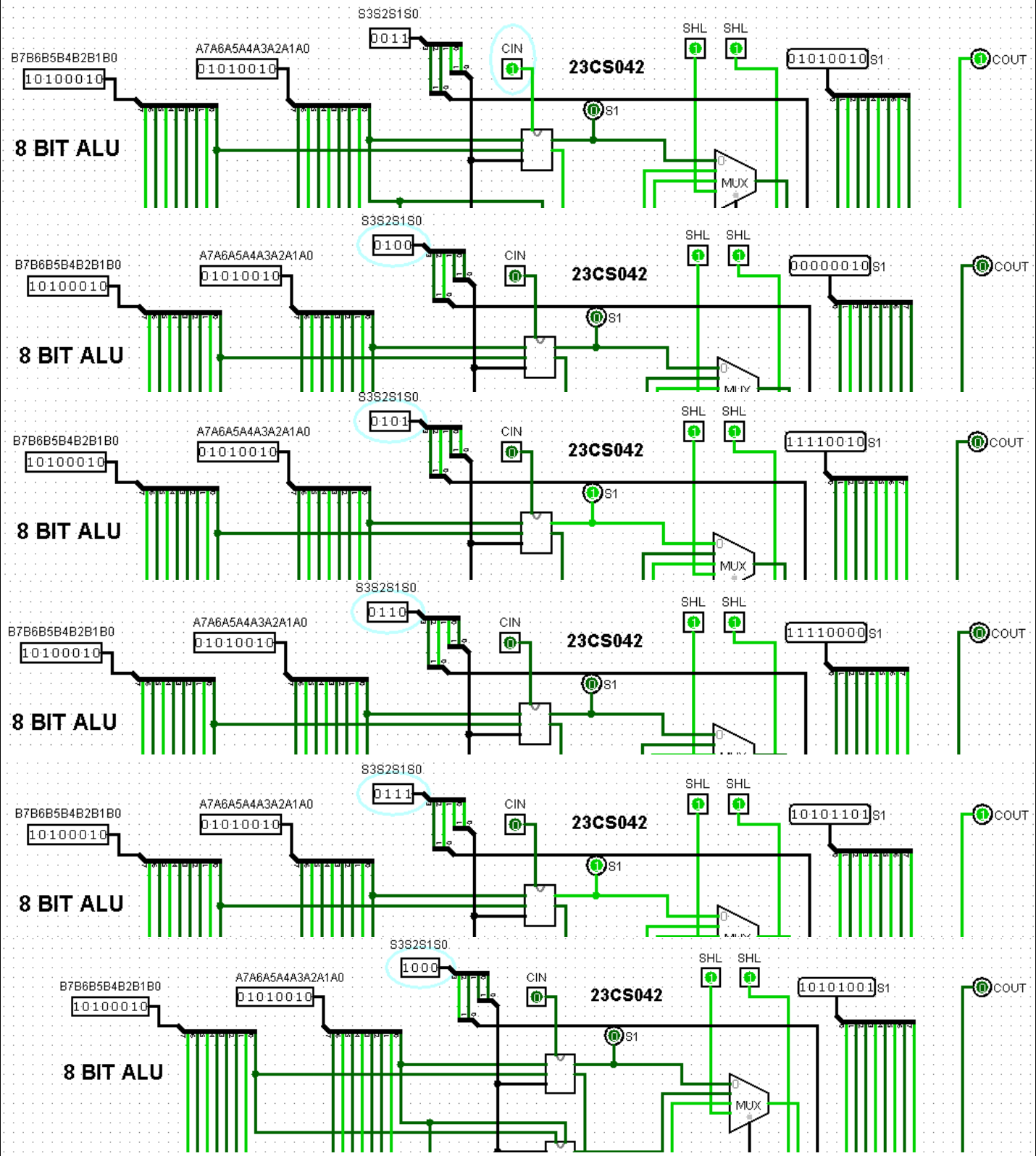
PAGE NO:

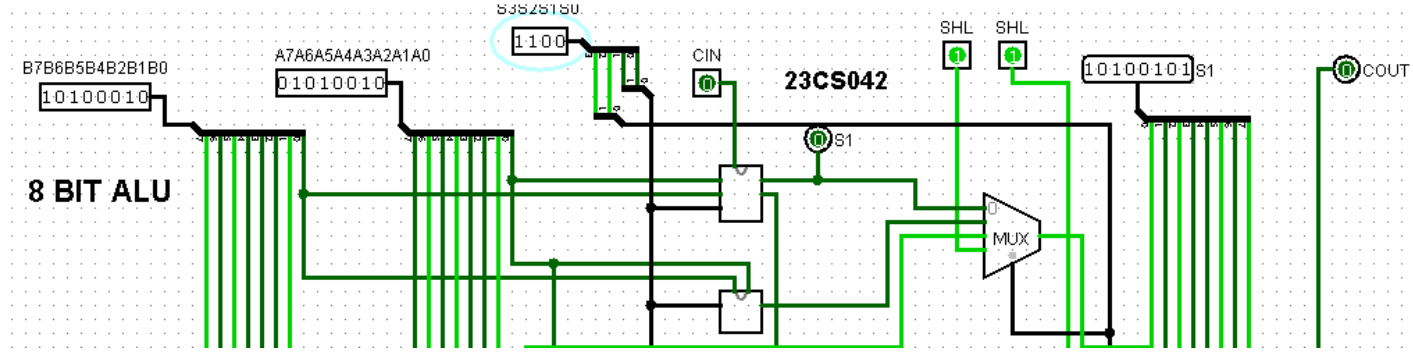

A1A0 01
B1B0 10
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0 10
MUX
10 F0F
S1
BIT 1
S3S2 10
COUT
MUX
SHR


A1A0 01
B1B0 10
CIN
2 BIT ALU
SHL
23CS042
S0
BIT 0
S1S0 10
MUX
11 F0F1
S1
BIT 1
S3S2 11
COUT
MUX
SHR


S3S2S1S0
0000
B7B6B5B4B2B1B0
10100010
A7A6A5A4A3A2A1A0
01010010
CIN
23CS042
SHL
SHL
11110100 S1
COUT
S1
8 BIT ALU
MUX


S3S2S1S0
0000
B7B6B5B4B2B1B0
10100010
A7A6A5A4A3A2A1A0
01010010
CIN
23CS042
SHL
SHL
11110101S1
COUT
S1
8 BIT ALU
MUX
S3S2S1S0
0001
10101111S1
S3S2S1S0
0001
10110000S1
S3S2S1S0
0010
01010010S1
S3S2S1S0
0010
01010011S1
S3S2S1S0
0011
01010001S1


S3S2S1S0
0011
B7B6B5B4B2B1B0
10100010
A7A6A5A4A3A2A1A0
01010010
CIN
23CS042
SHL
SHL
01010010 S1
COUT
S1
8 BIT ALU
MUX
S3S2S1S0
0100
00000010 S1
S3S2S1S0
0101
11110010 S1
S3S2S1S0
0110
11110000 S1
S3S2S1S0
0111
10101101 S1
S3S2S1S0
1000
10101001 S1


B7B6B5B4B2B1B0
10100010
A7A6A5A4A3A2A1A0
01010010
S3S2S1S0
1100
CIN
23CS042
SHL
SHL
10100101
S1
COUT
S1
8 BIT ALU
MUX

CONCLUSION: