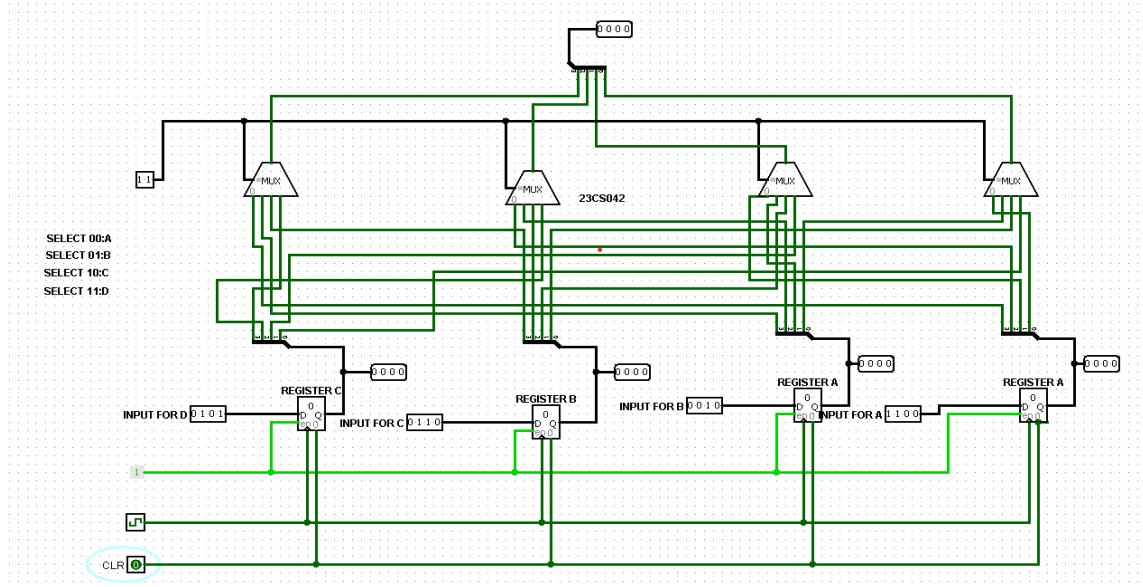
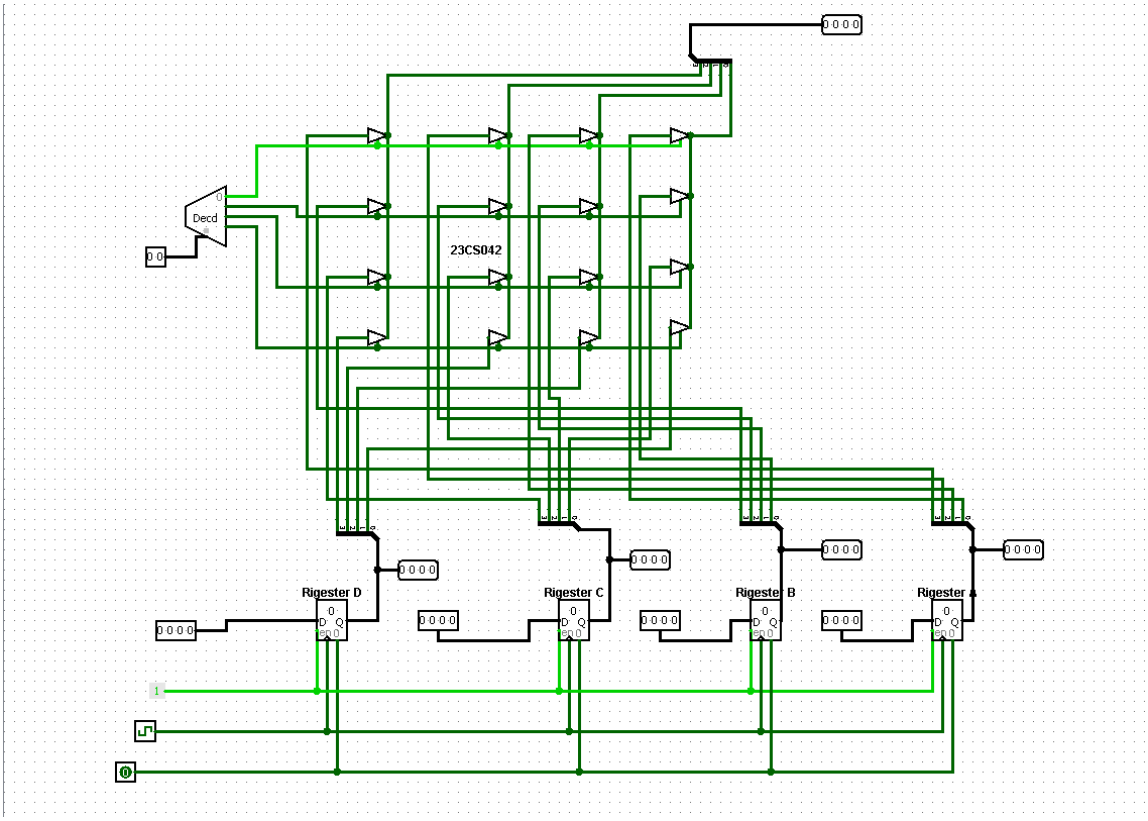
Date:

EXPERIMENT NO. 3

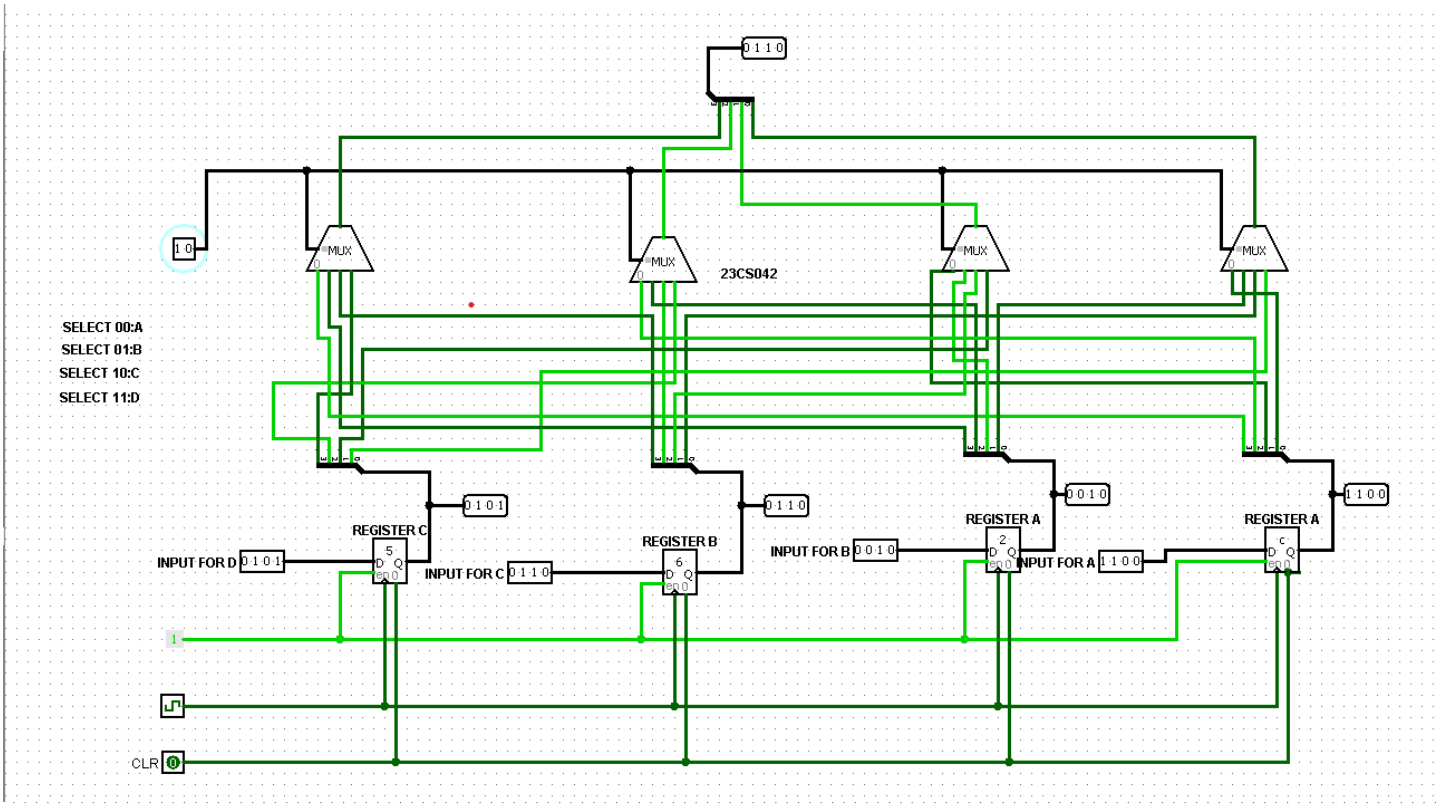
AIM: Implement a 4-bit common bus system to interface four 4-bit registers with a common bus using i. Multiplexer and ii. Decoder and tristate buffers.

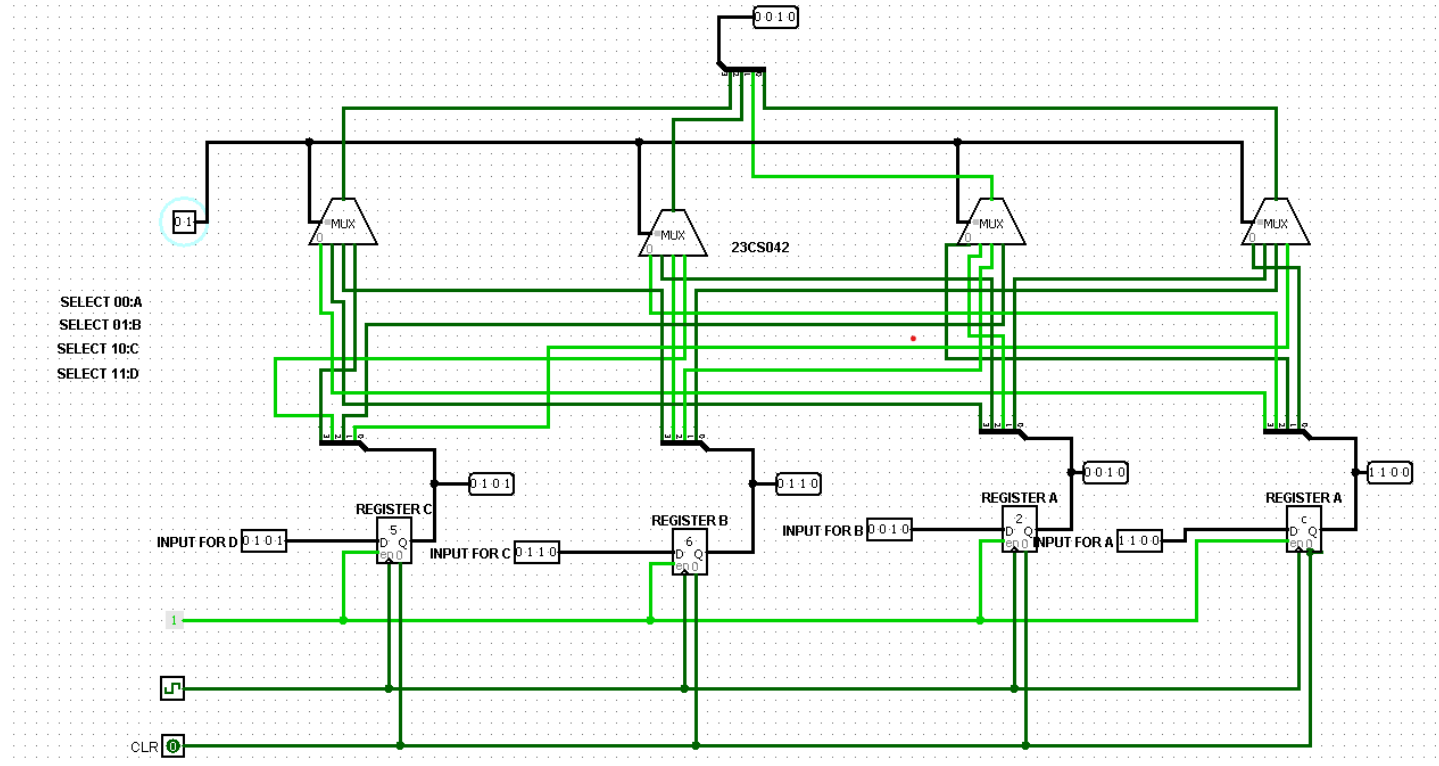
CIRCUITS:

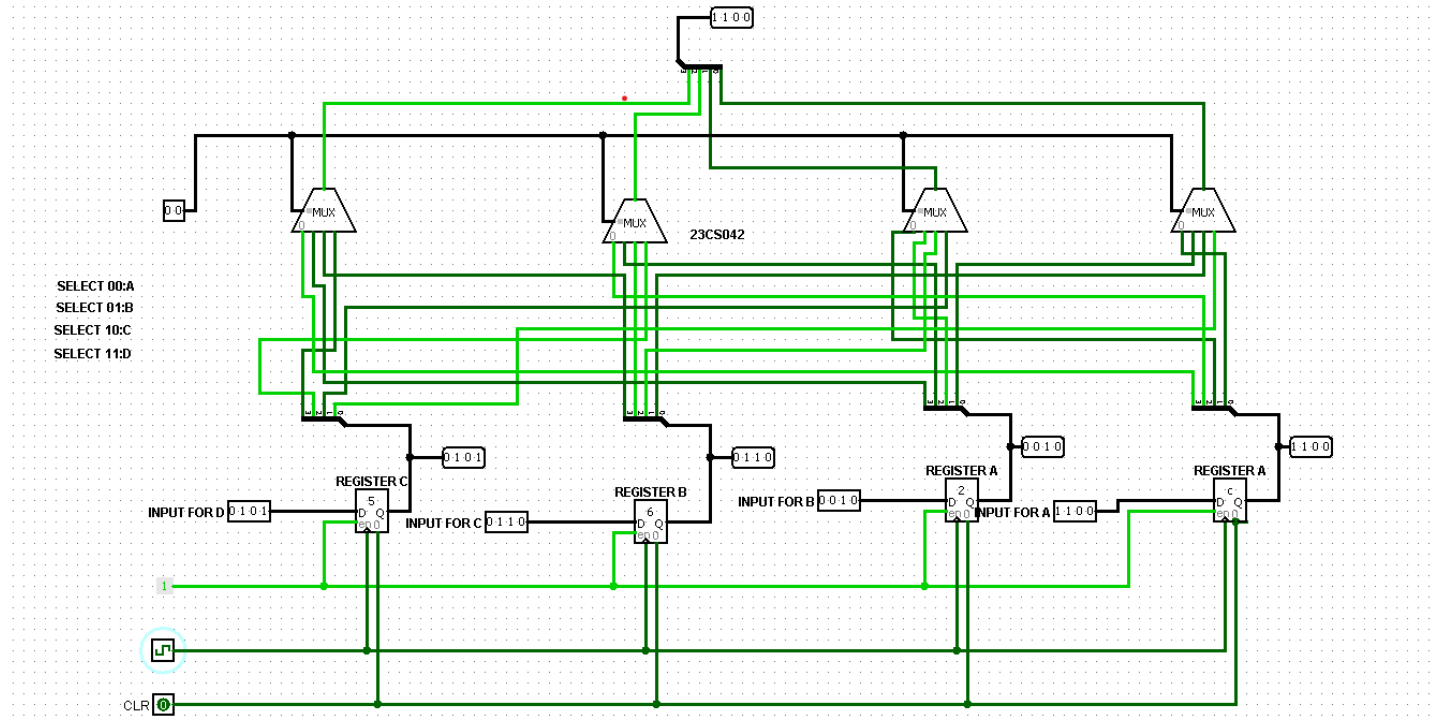


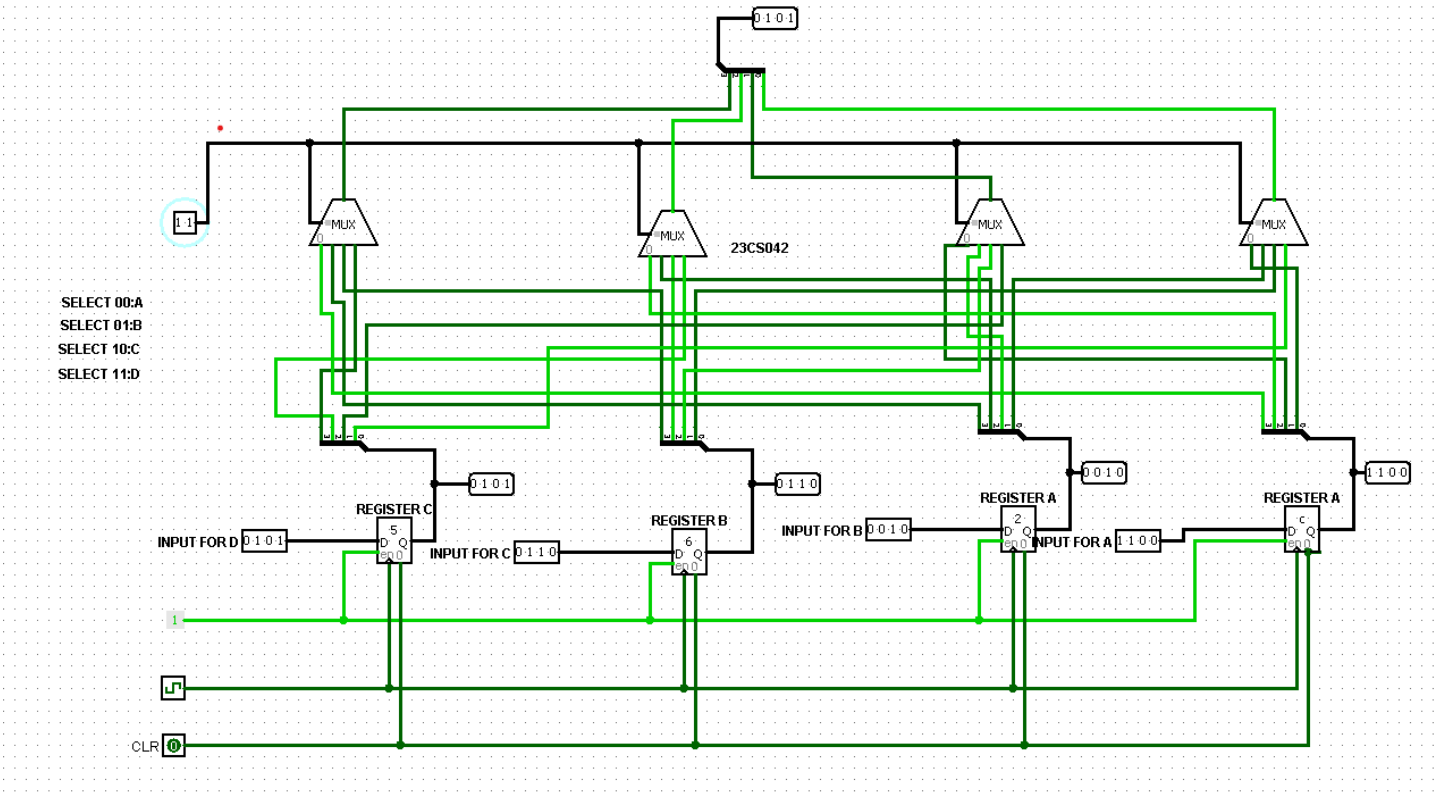


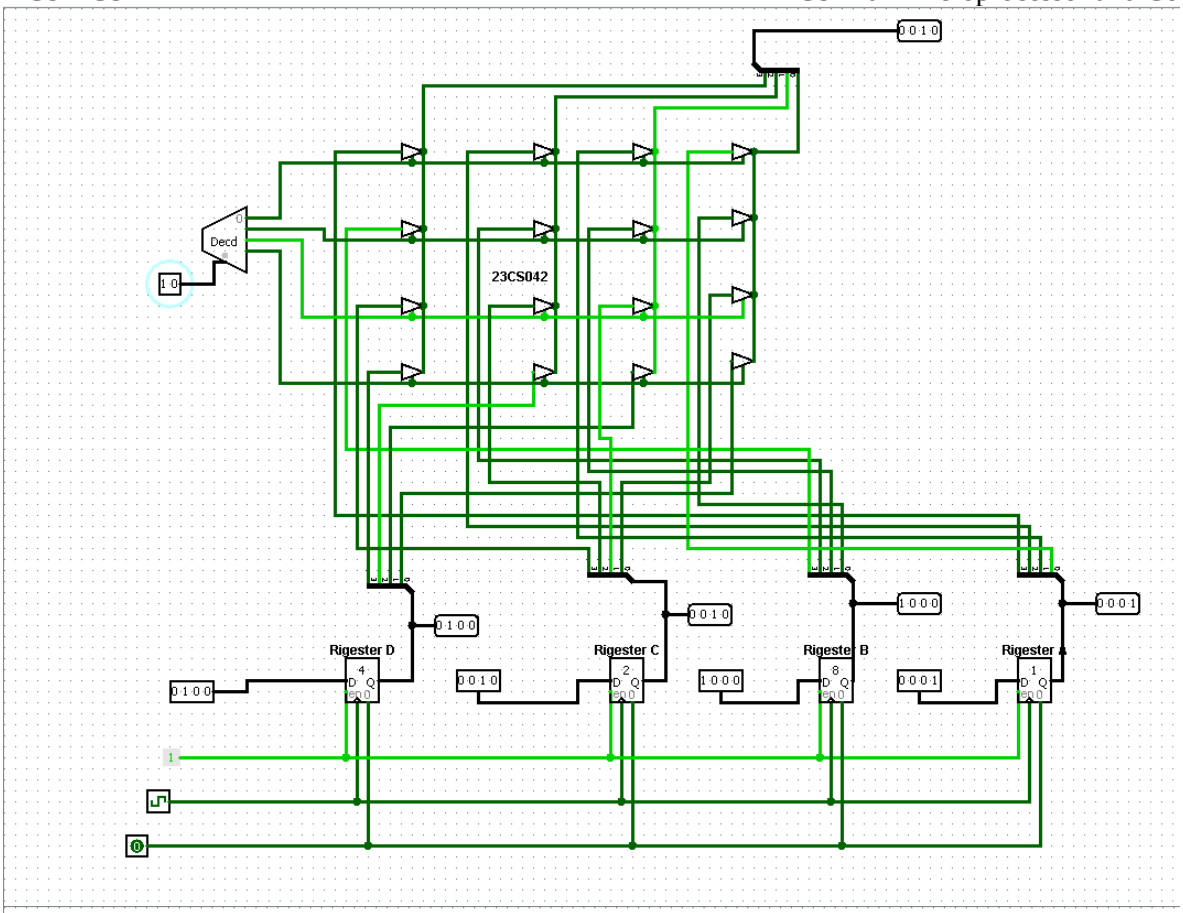
OUTPUTS:

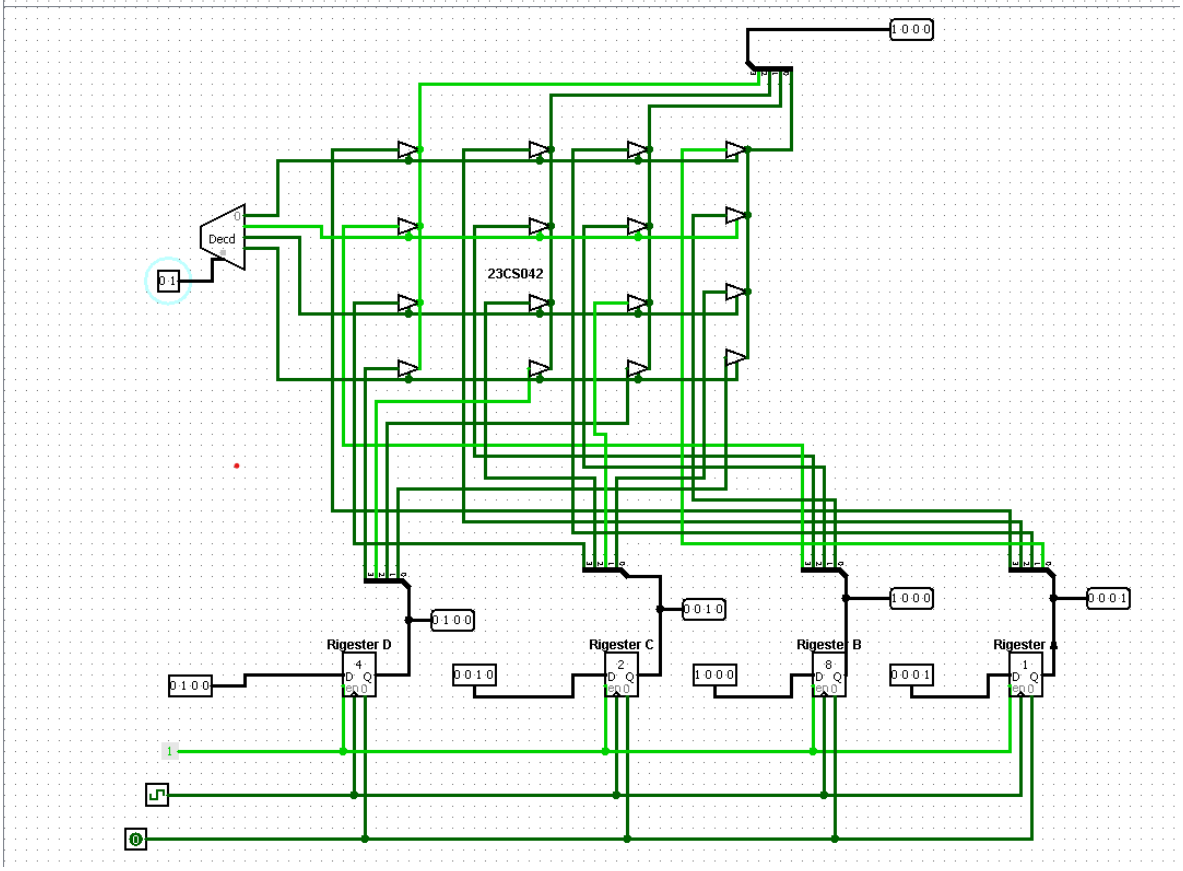

SELECT 00:A
SELECT 01:B
SELECT 10:C
SELECT 11:D
23CS042
MUX
REGISTER C
REGISTER B
REGISTER A
INPUT FOR D
INPUT FOR C
INPUT FOR B
INPUT FOR A
CLR

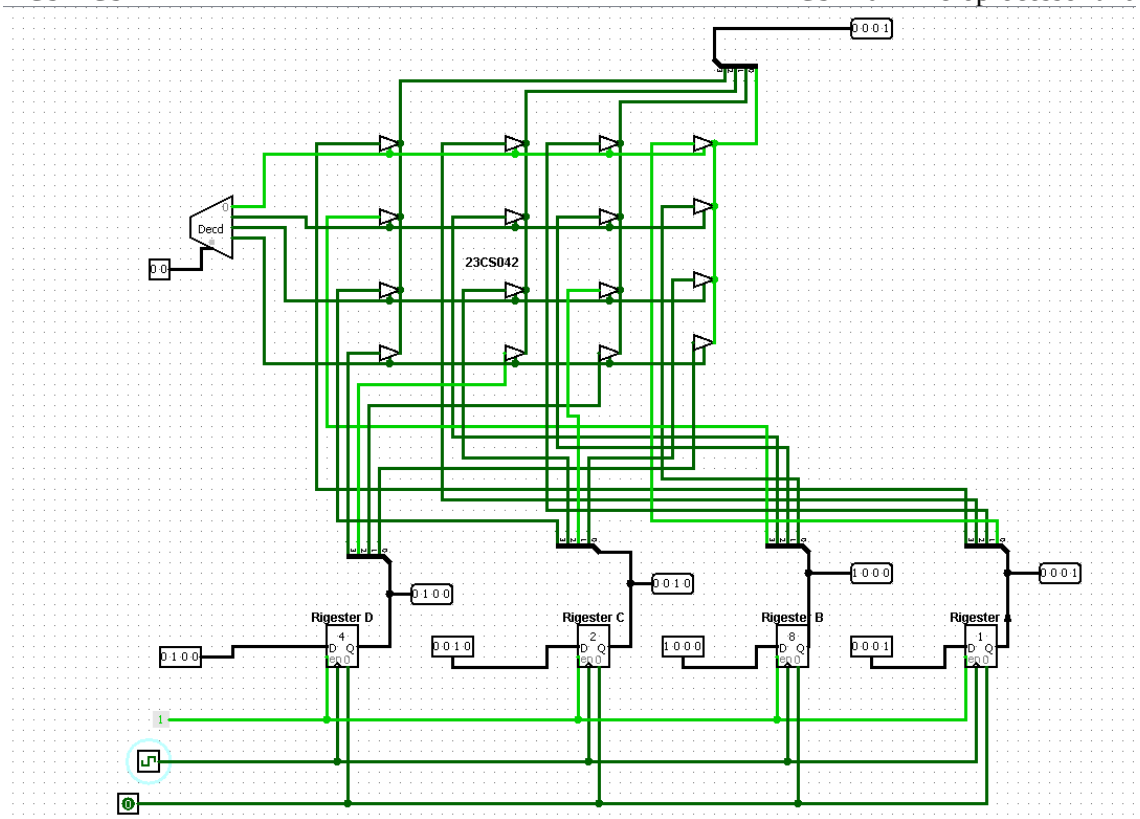

SELECT 00:A
SELECT 01:B
SELECT 10:C
SELECT 11:D
23CS042
MUX
REGISTER C
REGISTER B
REGISTER A
INPUT FOR D
INPUT FOR C
INPUT FOR B
INPUT FOR A
CLR

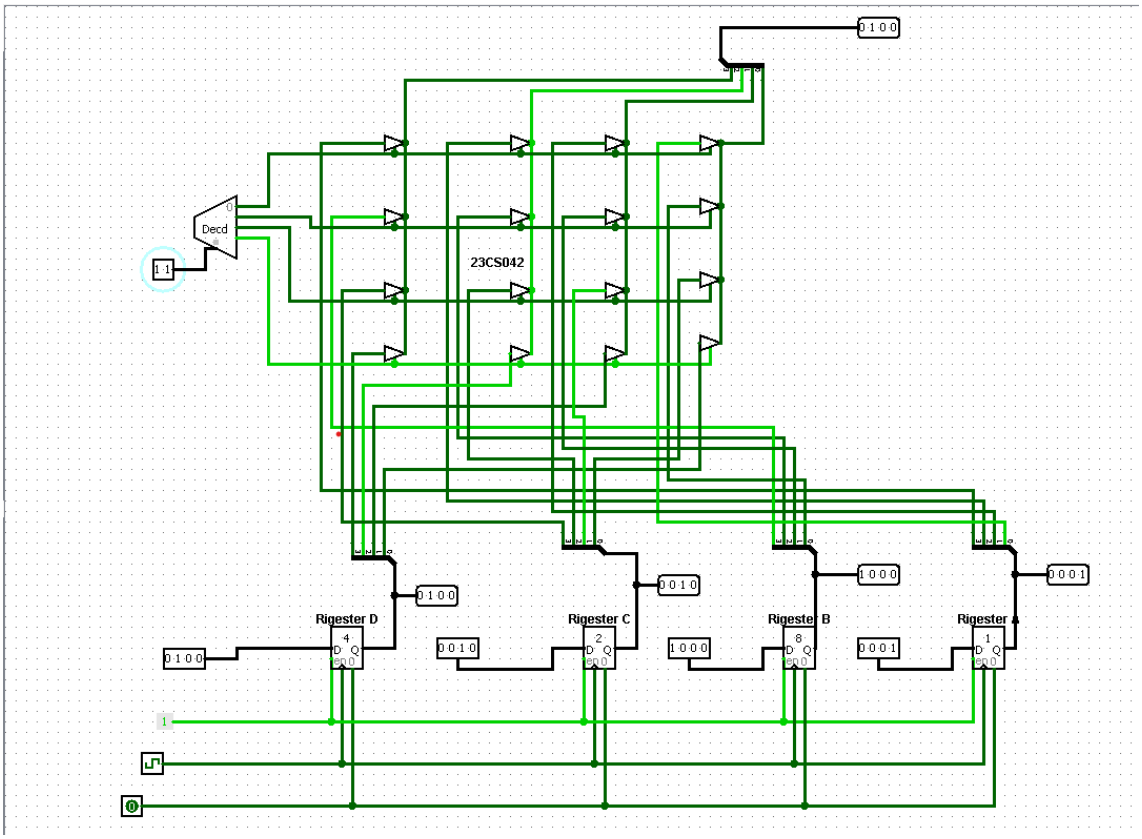

1 1 0 0
0 0
MUX
23CS042
SELECT 00:A
SELECT 01:B
SELECT 10:C
SELECT 11:D
0 1 0 1
0 1 1 0
0 0 1 0
1 1 0 0
REGISTER C
REGISTER B
REGISTER A
REGISTER A
INPUT FOR D 0 1 0 1
INPUT FOR C 0 1 1 0
INPUT FOR B 0 0 1 0
INPUT FOR A 1 1 0 0
1
CLR


0 1 0 1
1 1
MUX
23CS042
SELECT 00:A
SELECT 01:B
SELECT 10:C
SELECT 11:D
0 1 0 1
0 1 1 0
0 0 1 0
1 1 0 0
REGISTER C
REGISTER B
REGISTER A
REGISTER A
INPUT FOR D 0 1 0 1
INPUT FOR C 0 1 1 0
INPUT FOR B 0 0 1 0
INPUT FOR A 1 1 0 0
1
CLR


0 0 1 0
Decd
1 0
23CS042
0 1 0 0
0 0 1 0
1 0 0 0
0 0 0 1
Rigester D
Rigester C
Rigester B
Rigester A
4
2
8
1
D Q
PRO
0 1 0 0
0 0 1 0
1 0 0 0
0 0 0 1
1


1 0 0 0
Decd
0 1
23CS042
0 1 0 0
0 0 1 0
1 0 0 0
0 0 0 1
Rigester D
Rigester C
Rigester B
Rigester A
4
2
8
1
D Q
PRO
0 1 0 0
0 0 1 0
1 0 0 0
0 0 0 1
1


0001
Decd
00
23CS042
0100
0010
1000
0001
Rigester D
Rigester C
Rigester B
Rigester A
4
2
8
1
0100
0010
1000
0001
1
0


0100
Decd
11
23CS042
0100
0010
1000
0001
Rigester D
Rigester C
Rigester B
Rigester A
4
2
8
1
0100
0010
1000
0001
1
0

CONCLUSION:

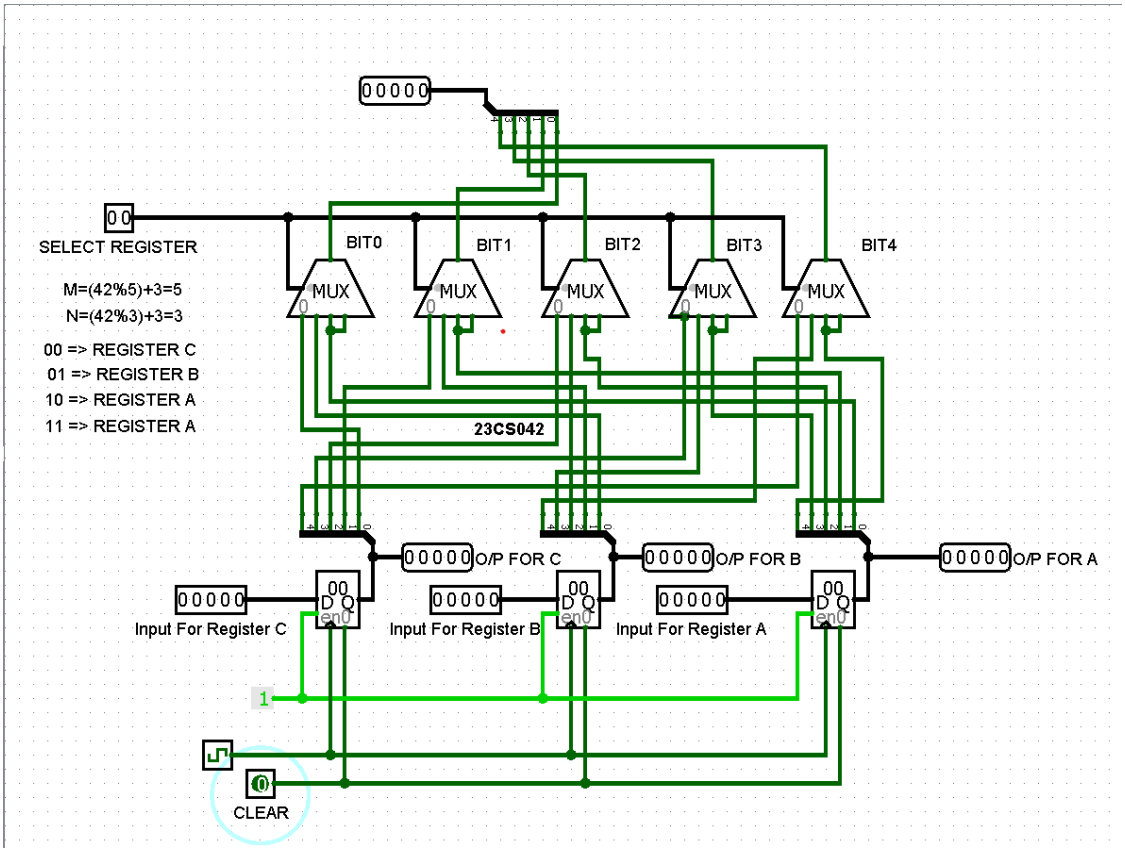
POST SESSION EXCERCISES:

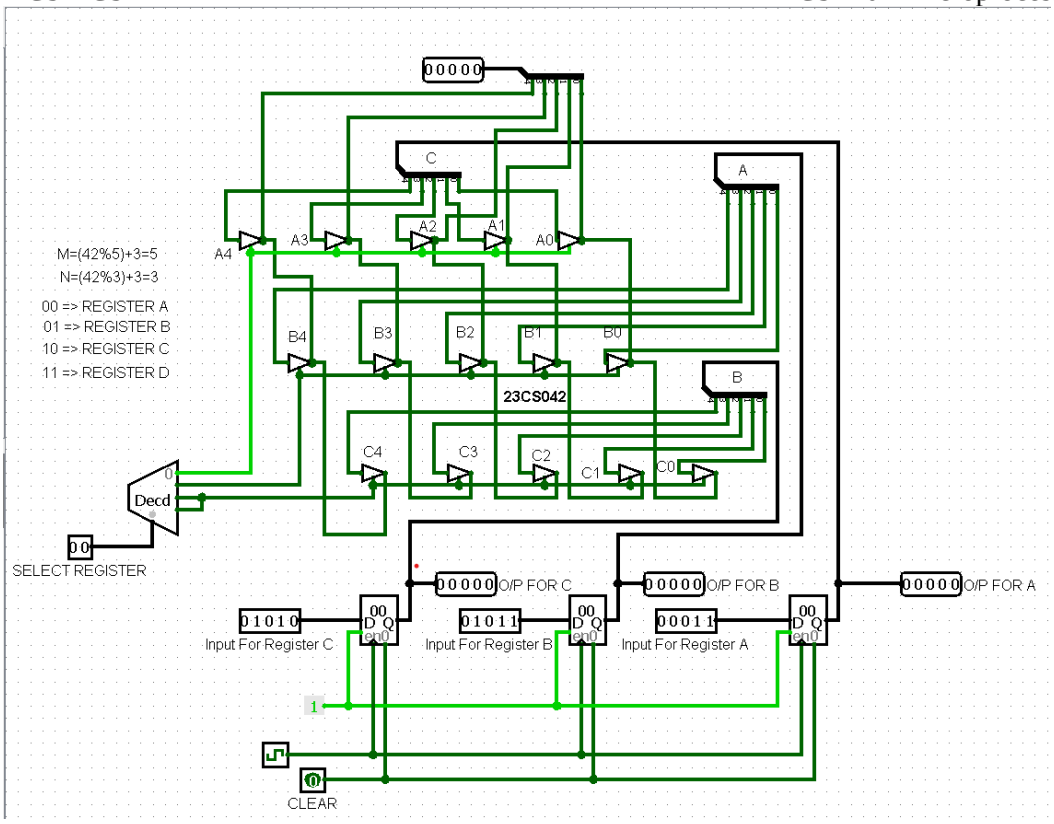
1. Find a number M=(MOD(Last Three Digits of your enrolment number, 5)+3) and find a number N=(MOD(Last Three Digits of your enrolment number, 3)+3). Implement a M-bit common bus system to interface N M-bit registers with a common bus using i. Multiplexer and ii. Decoder and tristate buffers.

M=(42%5)+3
M=(2+3)=5
N=(42%3)+3
N=(0+3)=3

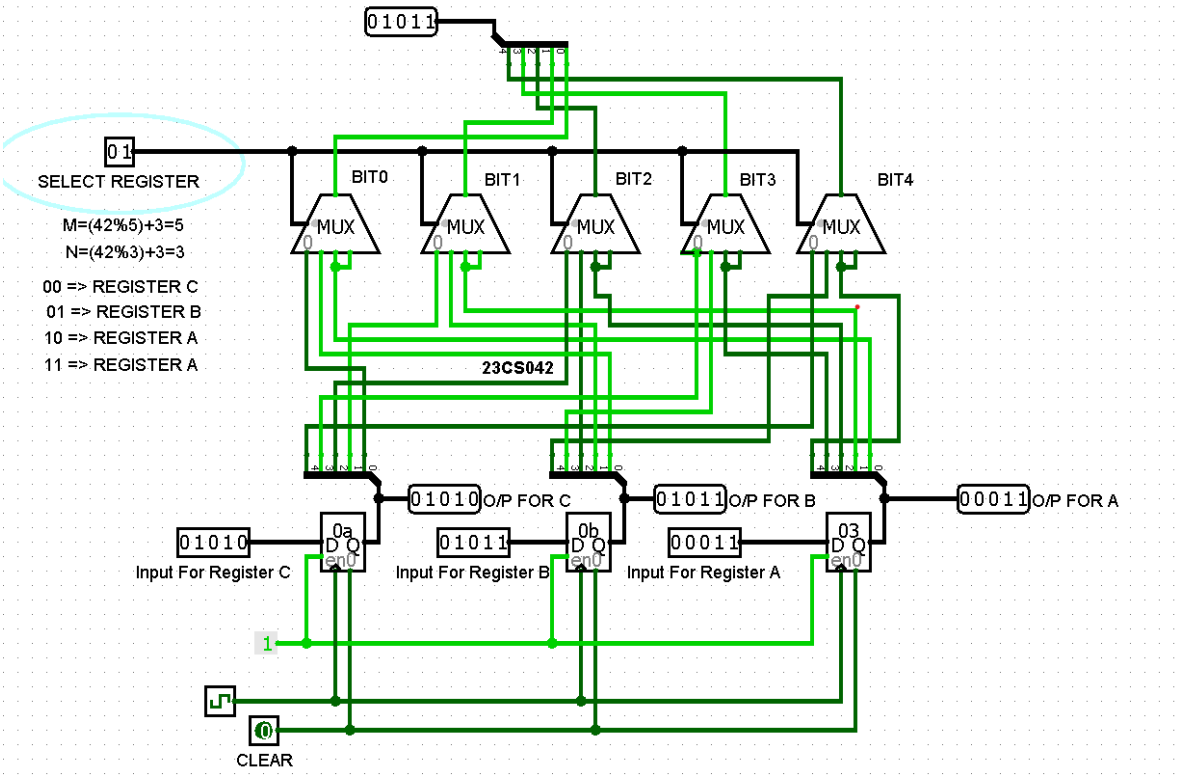
AIM: Implement a 5-bit common bus system to interface three 5-bit registers with a common bus using i. Multiplexer and ii. Decoder and tristate buffers.

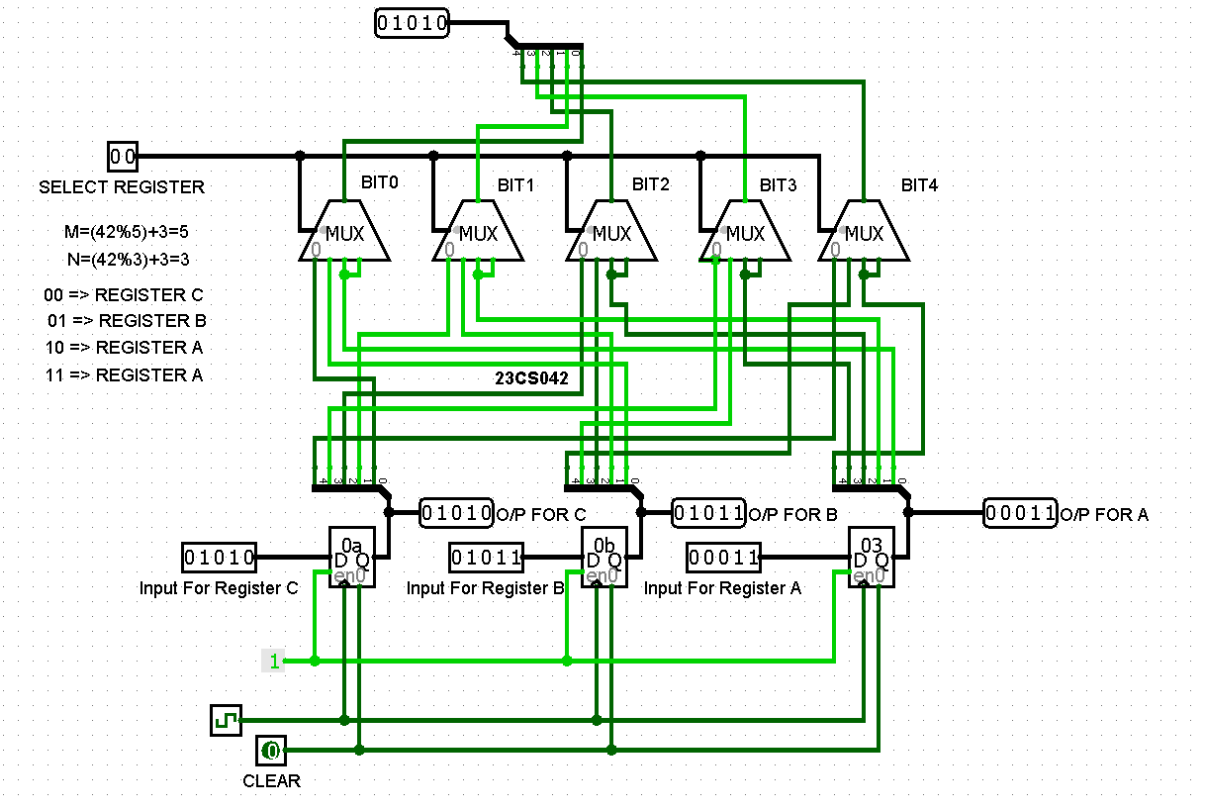
CIRCUITS:

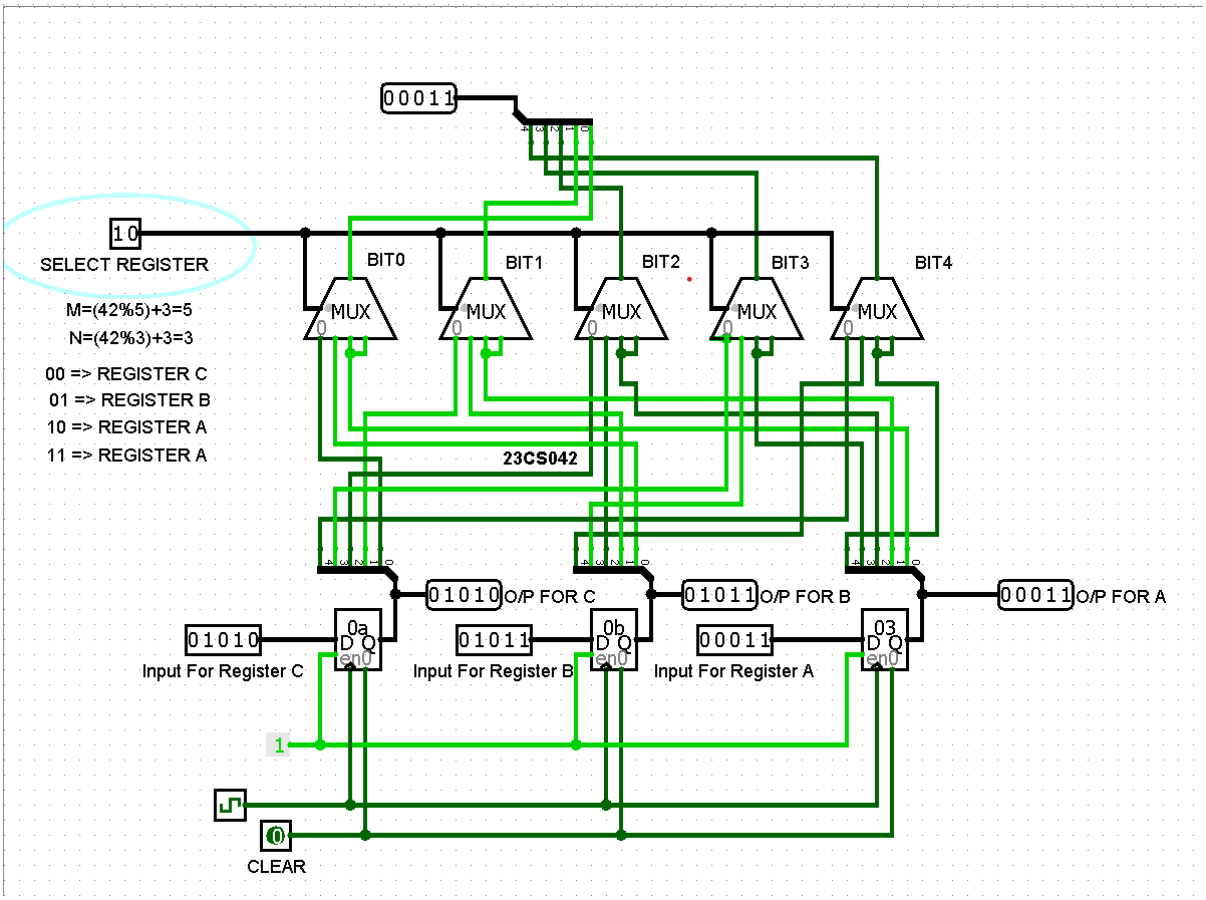


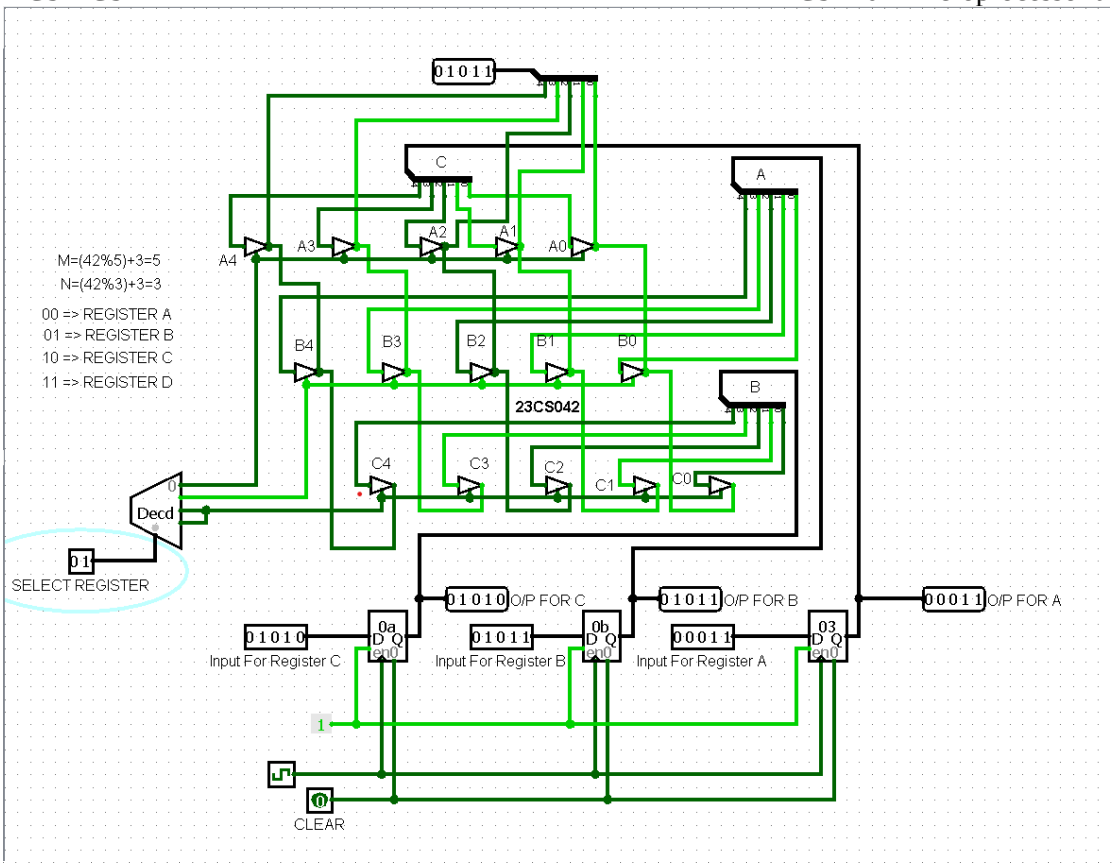

00000
C
A
A4
A3
A2
A1
A0
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER A
01 => REGISTER B
10 => REGISTER C
11 => REGISTER D
B4
B3
B2
B1
B0
B
23CS042
C4
C3
C2
C1
C0
Decd
00
SELECT REGISTER
00000 O/P FOR C
00000 O/P FOR B
00000 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
1
CLEAR

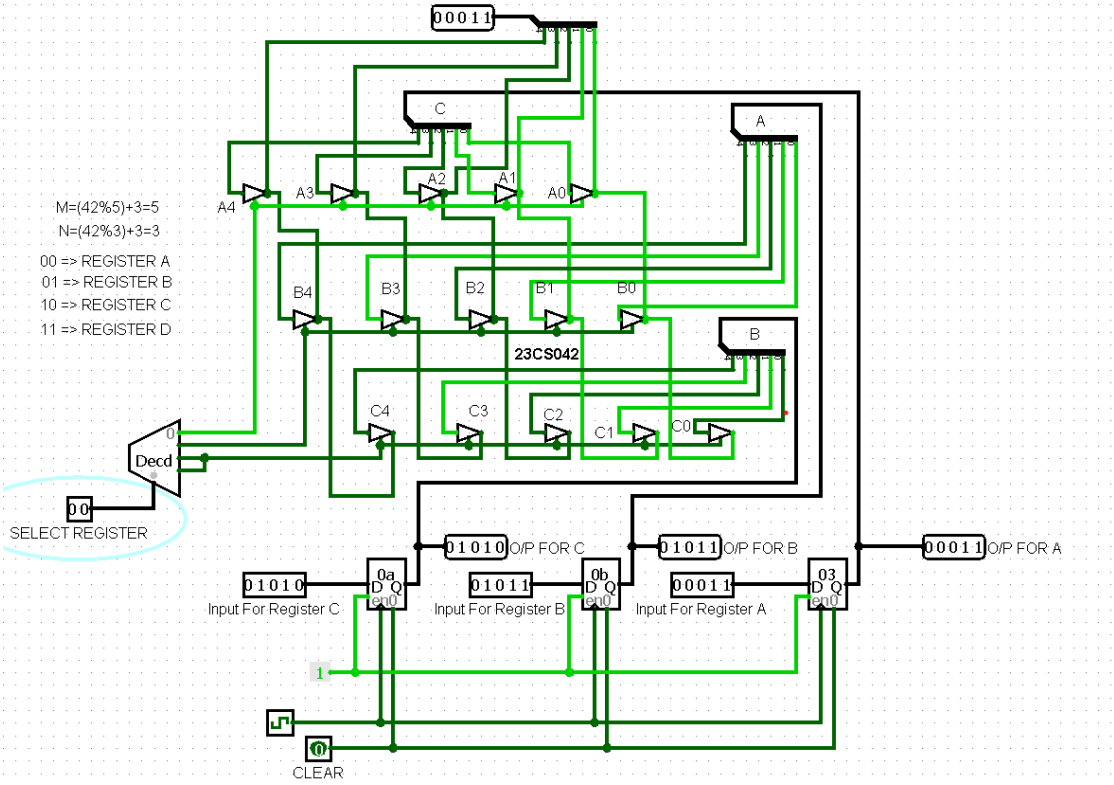
OUTPUTS:

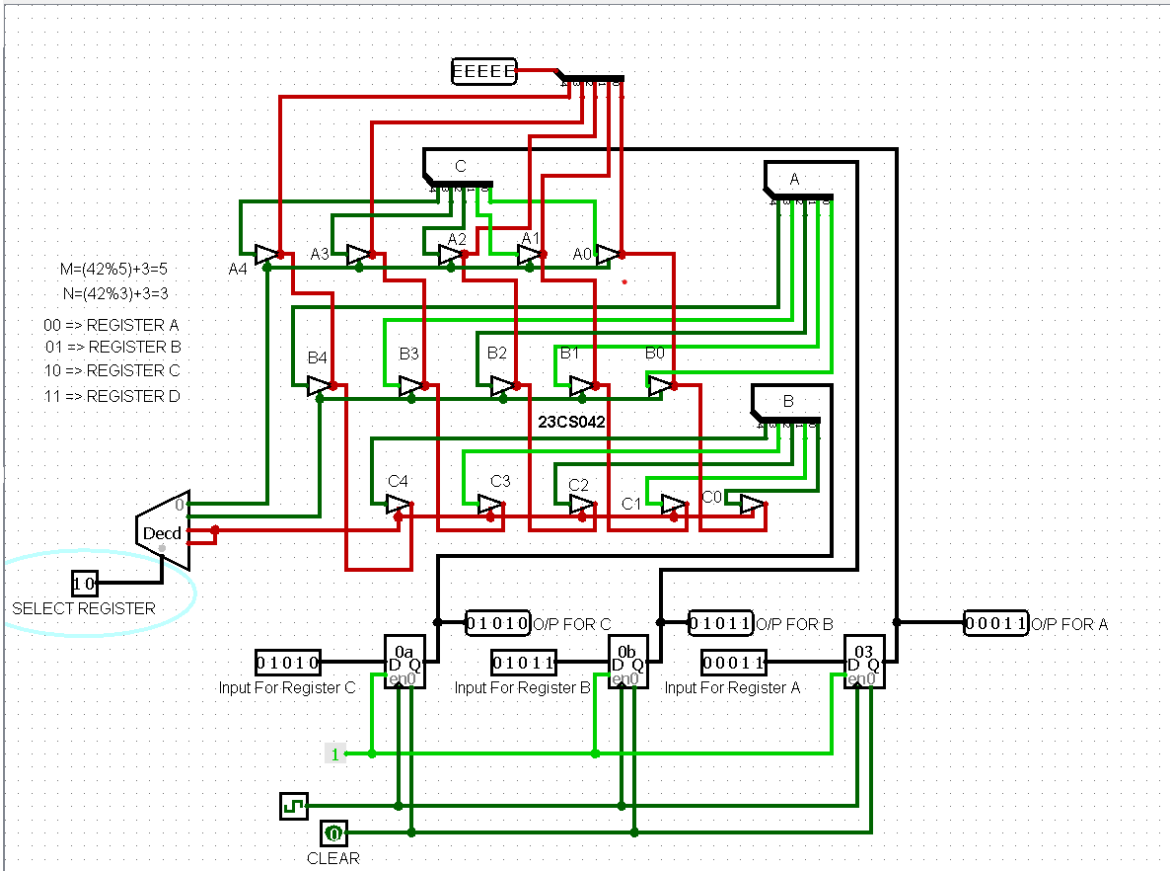

01011
01
SELECT REGISTER
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER C
01 => REGISTER B
10 => REGISTER A
11 => REGISTER A
BIT0
BIT1
BIT2
BIT3
BIT4
MUX
23CS042
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
1
CLEAR


01010
00
SELECT REGISTER
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER C
01 => REGISTER B
10 => REGISTER A
11 => REGISTER A
BIT0
BIT1
BIT2
BIT3
BIT4
MUX
23CS042
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
0a
0b
03
1
CLEAR


00011
10
SELECT REGISTER
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER C
01 => REGISTER B
10 => REGISTER A
11 => REGISTER A
BIT0
BIT1
BIT2
BIT3
BIT4
MUX
23CS042
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
0a
0b
03
1
CLEAR


01011
C
A
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER A
01 => REGISTER B
10 => REGISTER C
11 => REGISTER D
A4
A3
A2
A1
A0
B4
B3
B2
B1
B0
B
23CS042
C4
C3
C2
C1
C0
Decd
01
SELECT REGISTER
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
0a
0b
03
D Q
ext0
1
CLEAR


00011
C
A
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER A
01 => REGISTER B
10 => REGISTER C
11 => REGISTER D
A4
A3
A2
A1
A0
B4
B3
B2
B1
B0
B
23CS042
C4
C3
C2
C1
C0
Decd
00
SELECT REGISTER
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
0a
0b
03
D Q
ext0
1
CLEAR


EEEEE
C
A
A4
A3
A2
A1
A0
M=(42%5)+3=5
N=(42%3)+3=3
00 => REGISTER A
01 => REGISTER B
10 => REGISTER C
11 => REGISTER D
B4
B3
B2
B1
B0
B
23CS042
C4
C3
C2
C1
C0
Decd
10
SELECT REGISTER
01010 O/P FOR C
01011 O/P FOR B
00011 O/P FOR A
01010
Input For Register C
01011
Input For Register B
00011
Input For Register A
0a
0b
03
D Q
en0
1
CLEAR