Date:

EXPERIMENT NO. 5

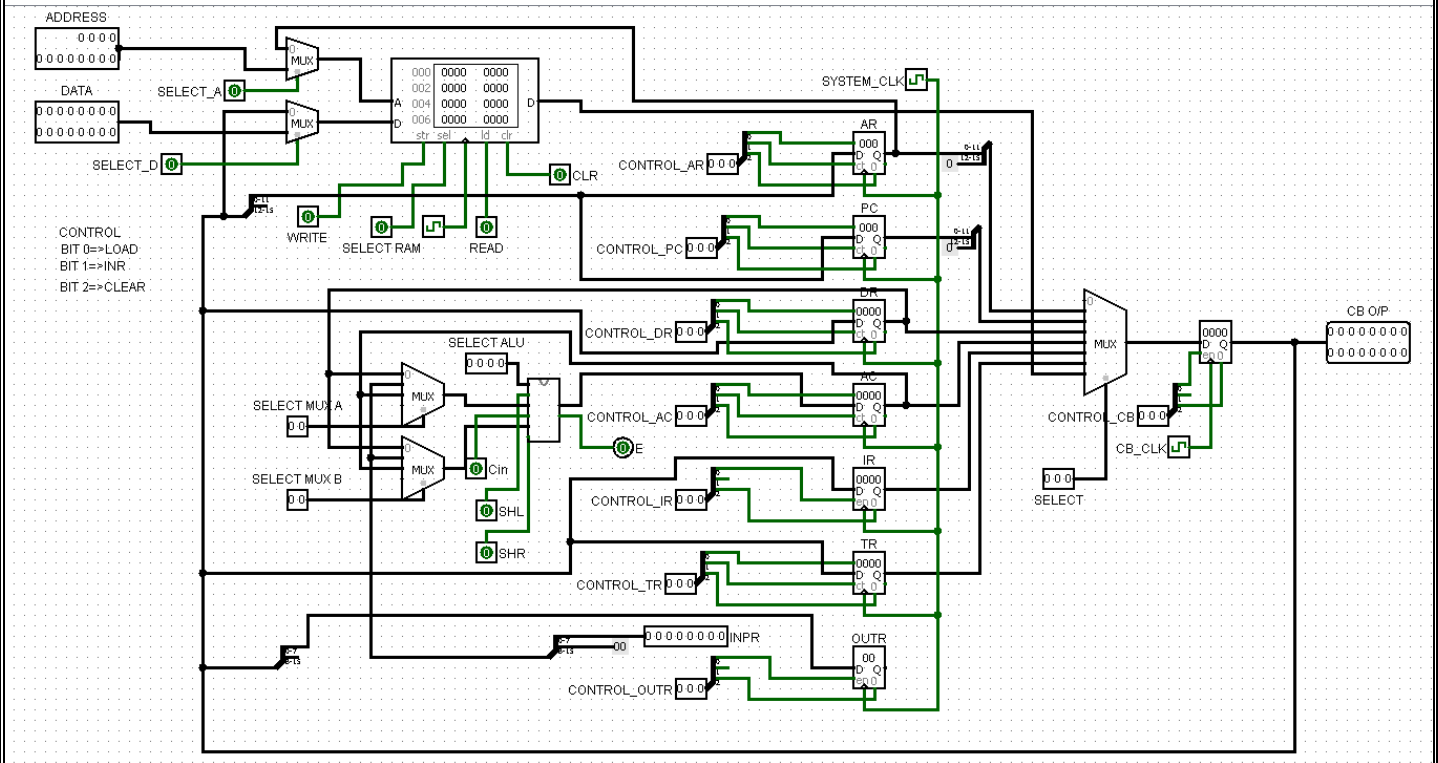
AIM: Implement a common bus system with ALU, 8 registers and 1 memory unit with necessary control signals.

OBJECTIVES:

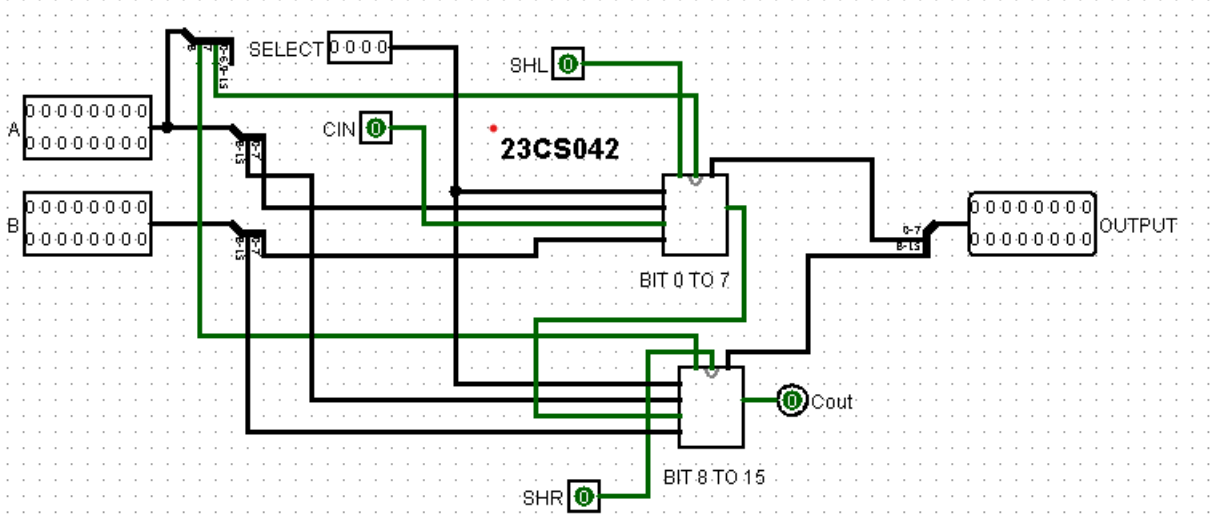
i. Implement 16-bit ALU that is suitable for common bus system

ii. Implement 16-bit common bus system with ALU, 8 registers and 1 memory unit

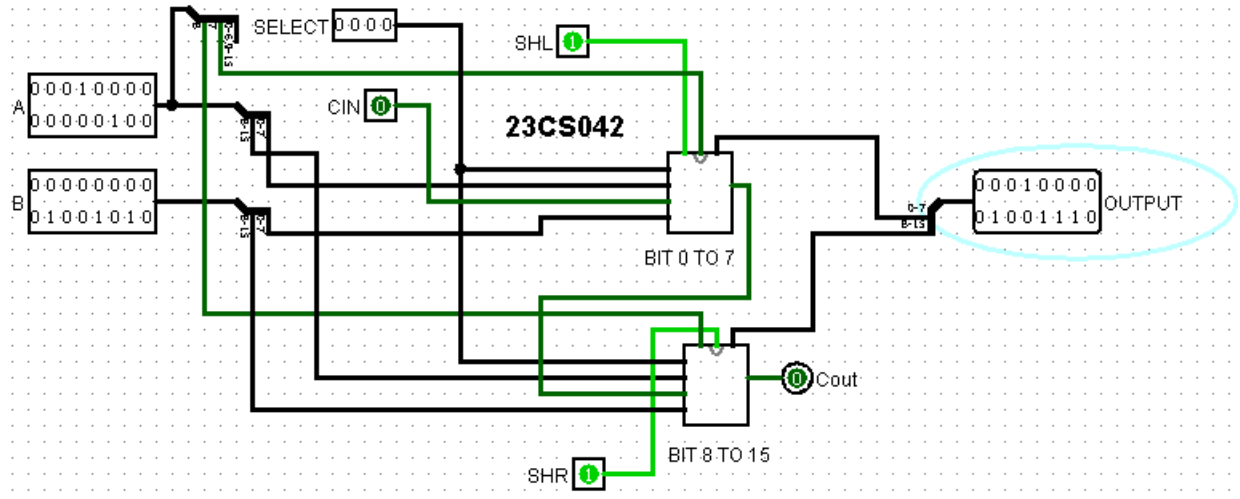
CIRCUITS:

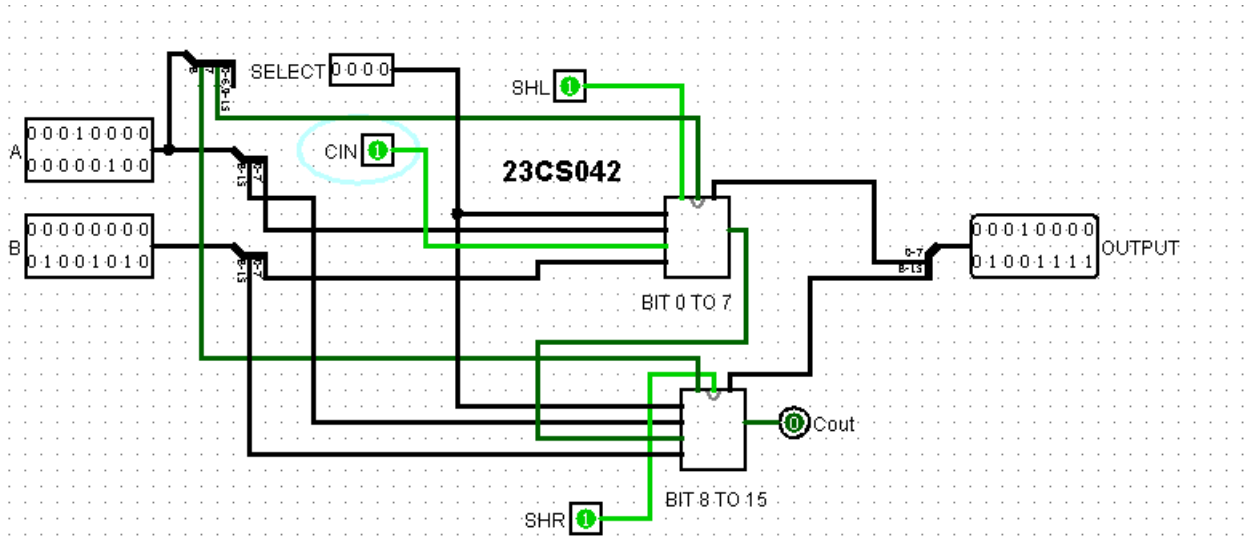


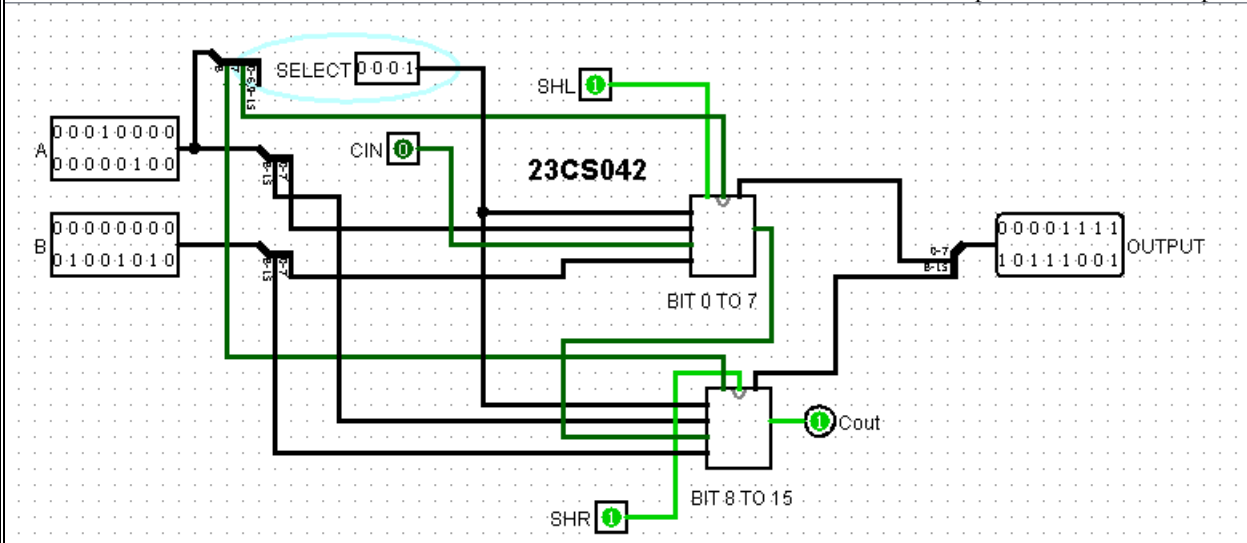
Page No:

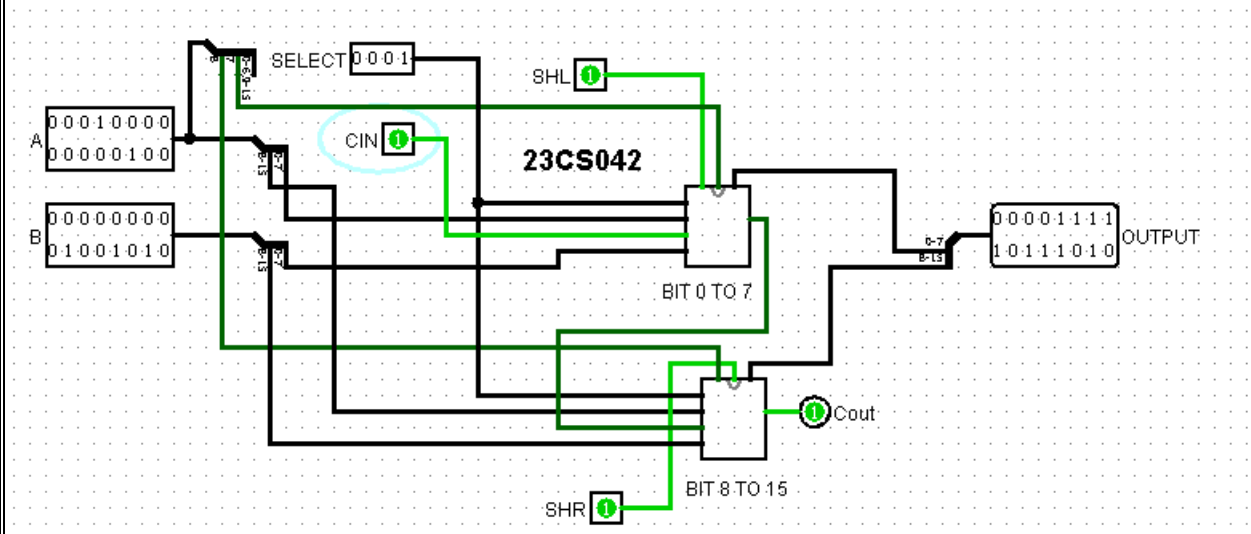

SELECT
0 0 0 0
SHL
CIN
23CS042
A
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
B
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

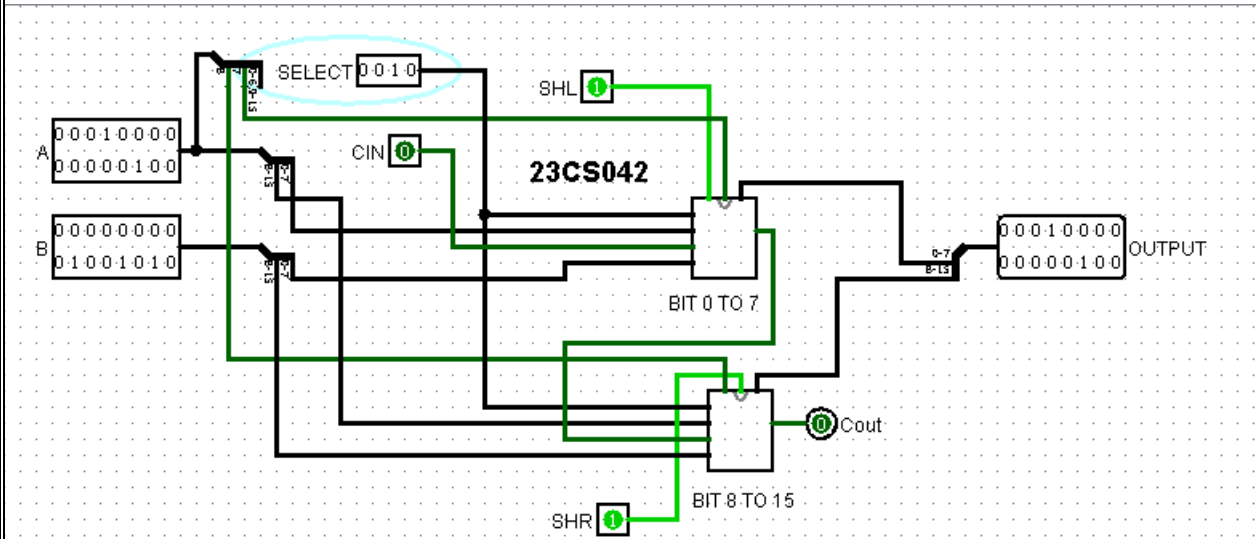
OUTPUTS:

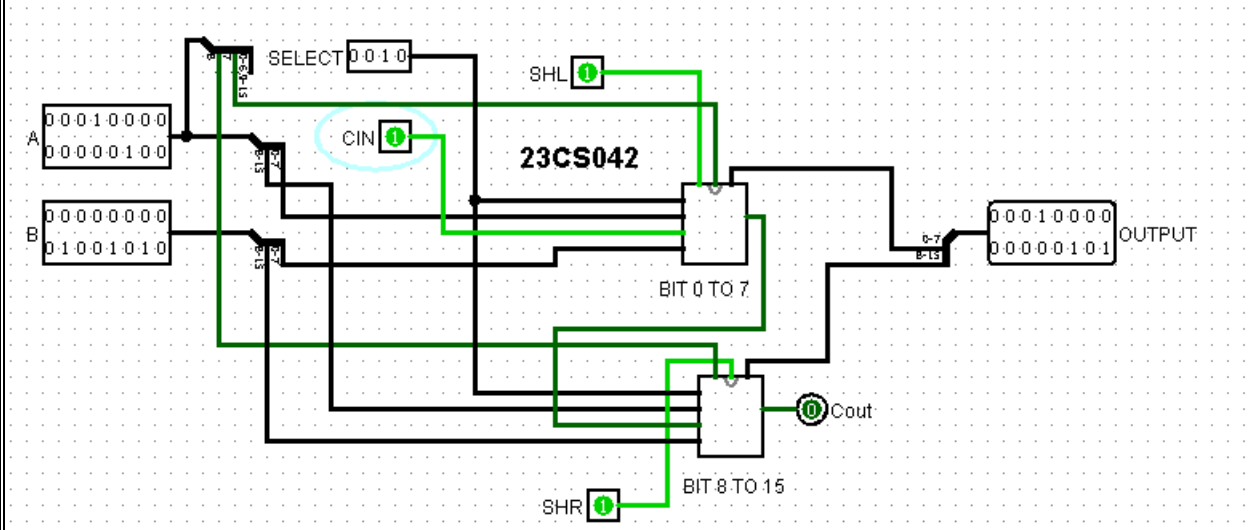

SELECT
0 0 0 0
SHL
CIN
23CS042
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 1 0 0 1 1 1 0
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

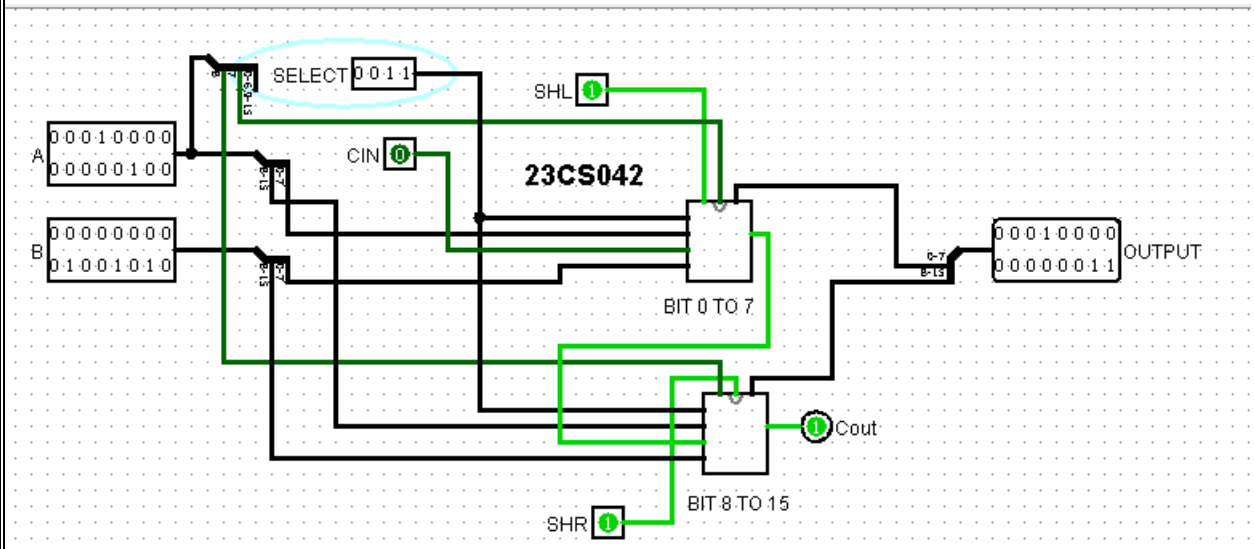

SELECT
0 0 0 0
SHL
CIN
23CS042
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 1 0 0 1 1 1 1
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

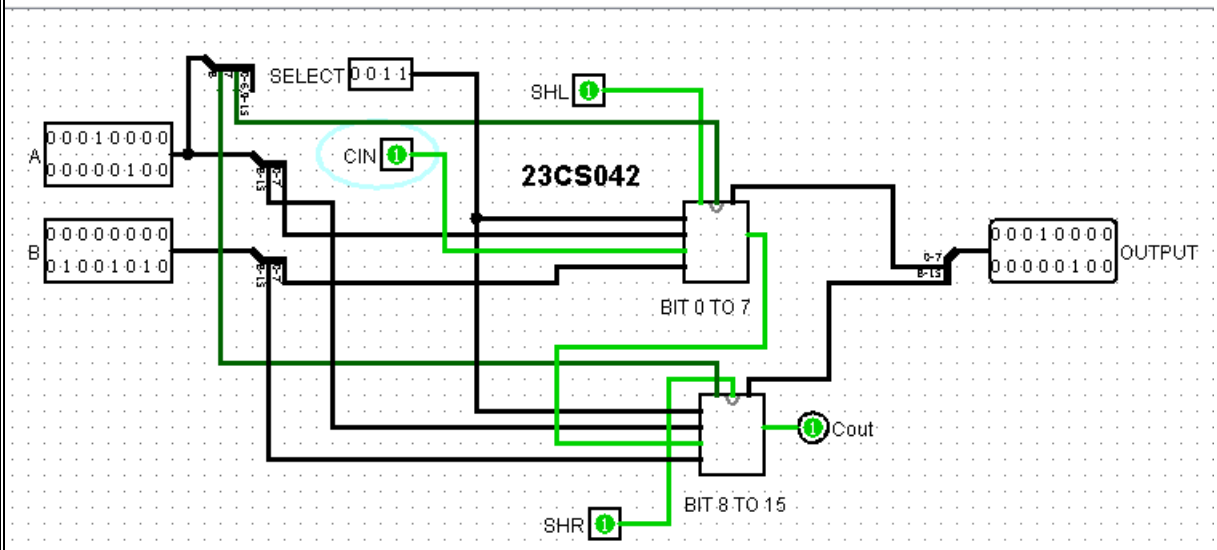

SELECT
0 0 0 1
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 0 1 1 1 1
1 0 1 1 1 0 0 1
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

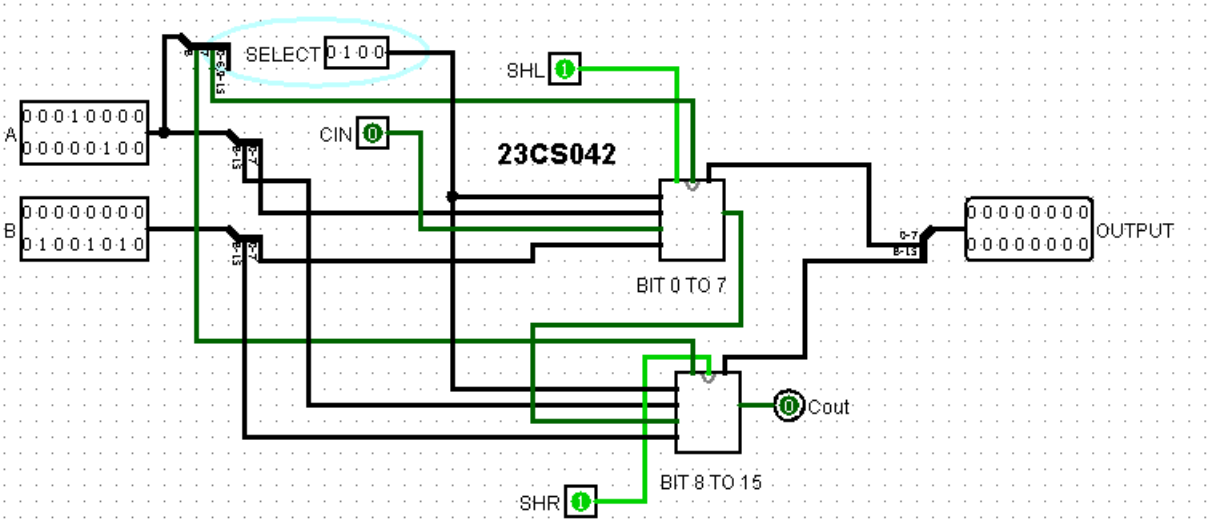

SELECT
0 0 0 1
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 0 1 1 1 1
1 0 1 1 1 0 1 0
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

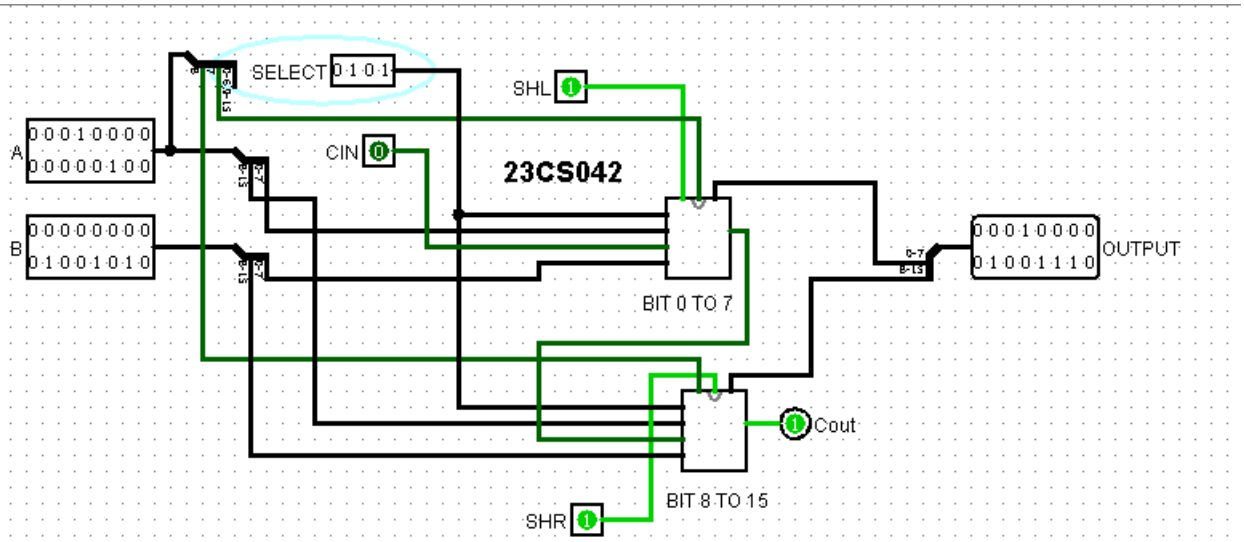

SELECT
0 0 1 0
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

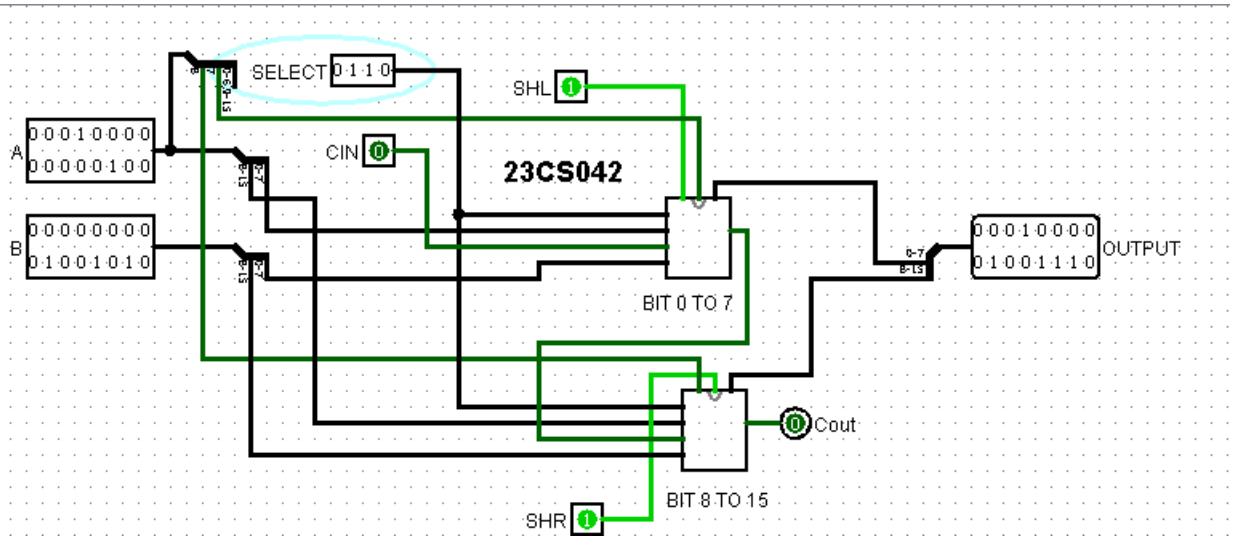

SELECT 0 0 1 0
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 1
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 1
OUTPUT
BIT 0 TO 7
Cout 0
BIT 8 TO 15
SHR 1

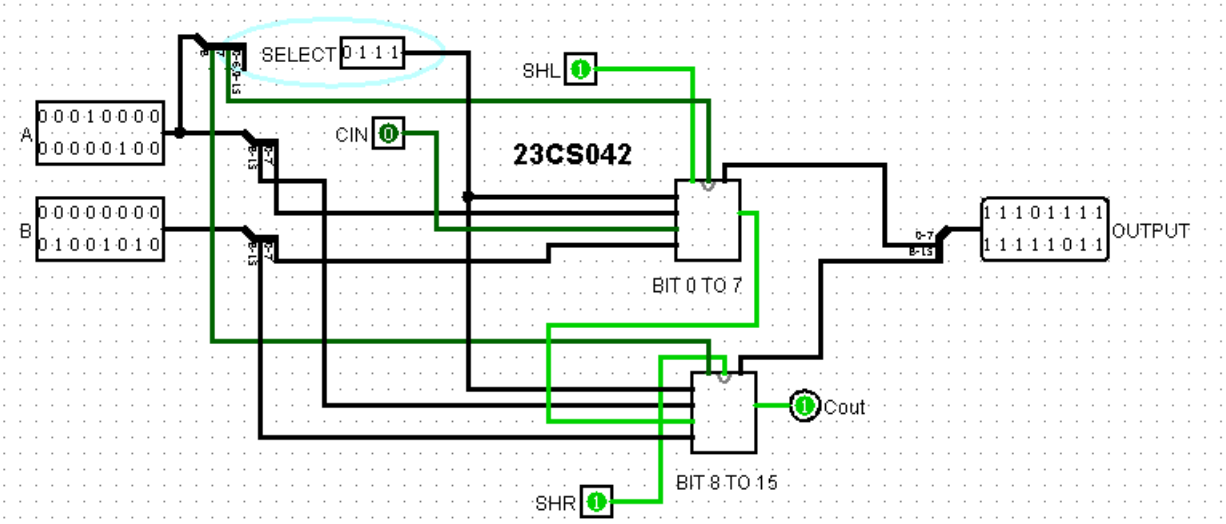

SELECT 0 0 1 1
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 0
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 0 0 0 0 1 1 1
OUTPUT
BIT 0 TO 7
Cout 1
BIT 8 TO 15
SHR 1

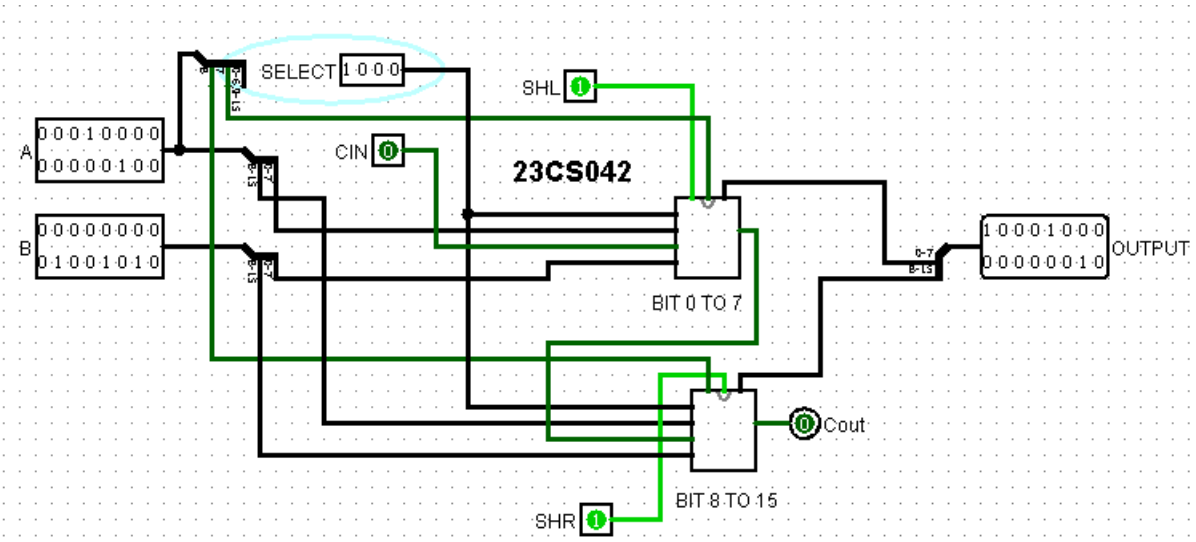

SELECT 0 0 1 1
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 1
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
OUTPUT
BIT 0 TO 7
Cout 1
BIT 8 TO 15
SHR 1

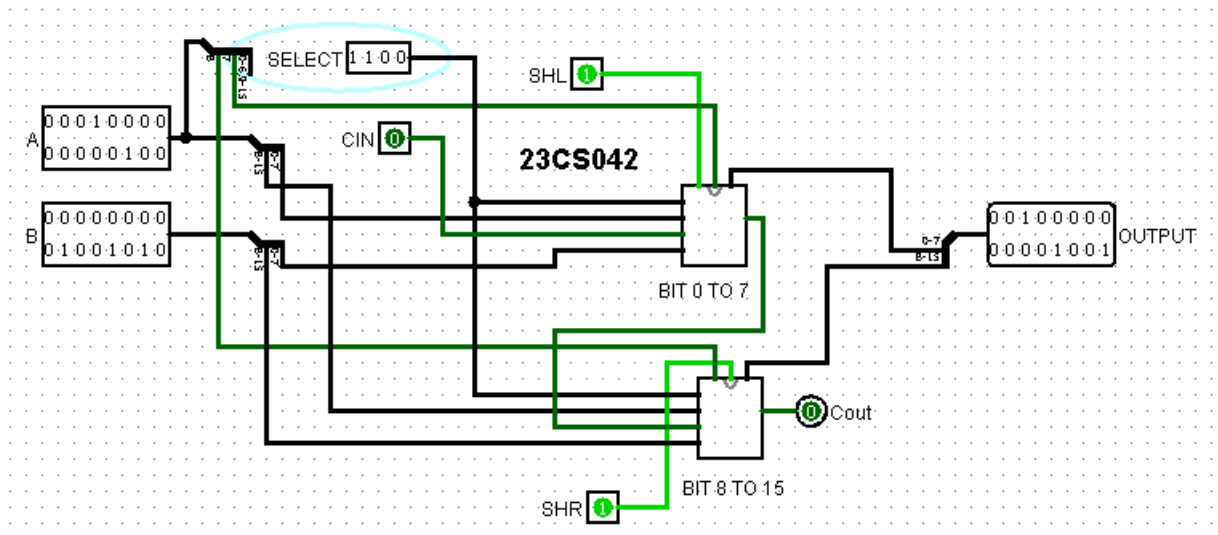

SELECT 0 1 0 0
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 0
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0
OUTPUT
BIT 0 TO 7
Cout 0
BIT 8 TO 15
SHR 1


SELECT 0 1 0 1
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 0
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 1 0 0 1 1 1 0
OUTPUT
BIT 0 TO 7
Cout 1
BIT 8 TO 15
SHR 1

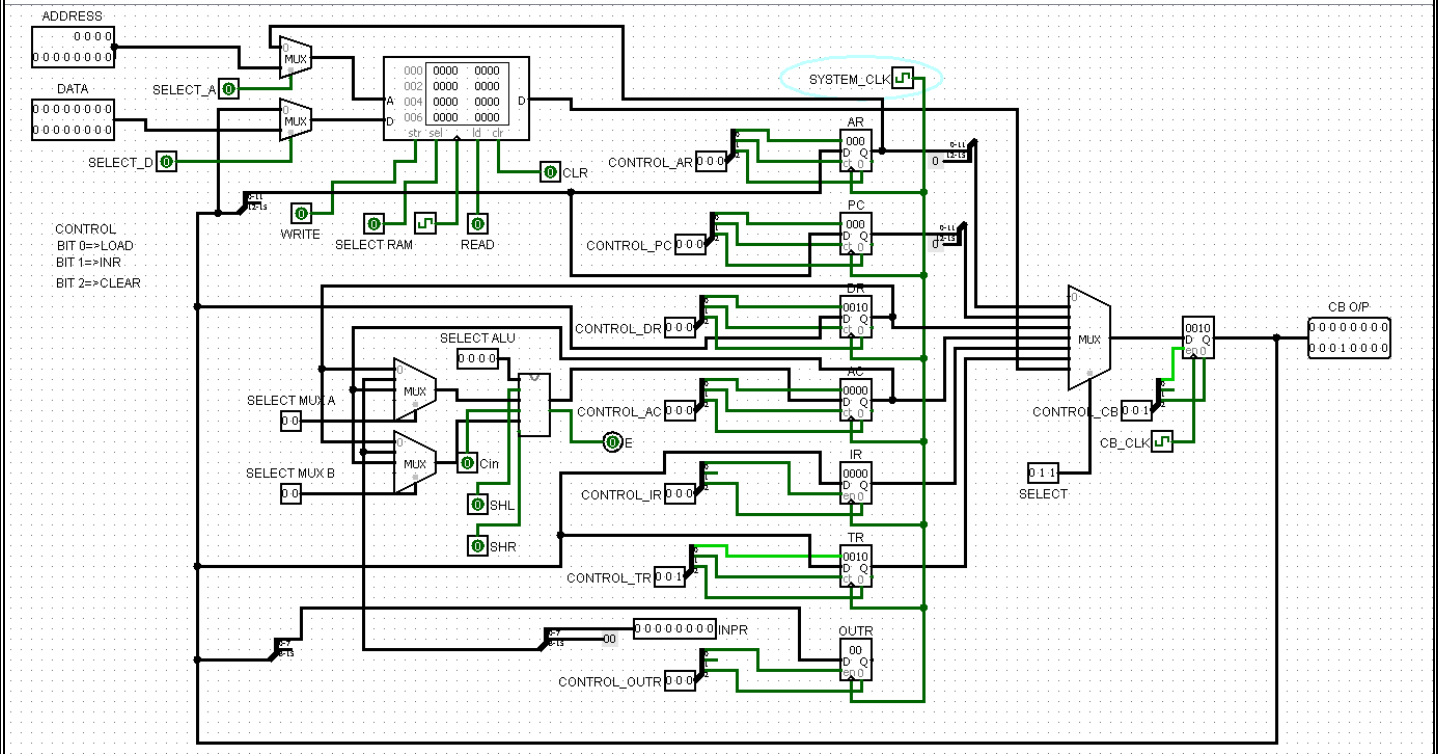

SELECT 0 1 1 0
SHL 1
A 0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN 0
23CS042
B 0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 0 1 0 0 0 0
0 1 0 0 1 1 1 0
OUTPUT
BIT 0 TO 7
Cout 0
BIT 8 TO 15
SHR 1


SELECT
0 1 1 1
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
1 1 1 0 1 1 1 1
1 1 1 1 1 0 1 1
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

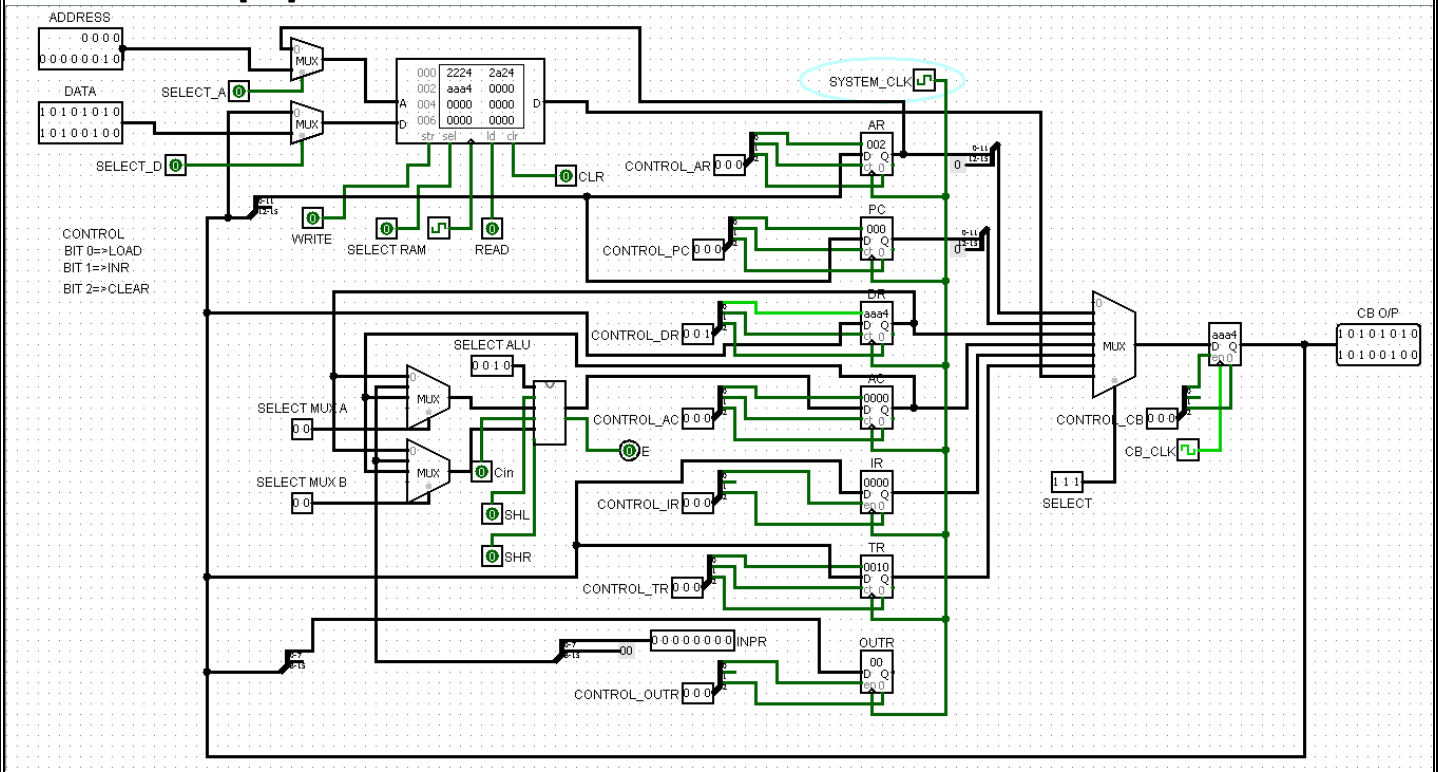

SELECT
1 0 0 0
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
1 0 0 0 1 0 0 0
0 0 0 0 0 0 1 0
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR


SELECT
1 1 0 0
SHL
A
0 0 0 1 0 0 0 0
0 0 0 0 0 1 0 0
CIN
23CS042
B
0 0 0 0 0 0 0 0
0 1 0 0 1 0 1 0
0 0 1 0 0 0 0 0
0 0 0 0 1 0 0 1
OUTPUT
BIT 0 TO 7
Cout
BIT 8 TO 15
SHR

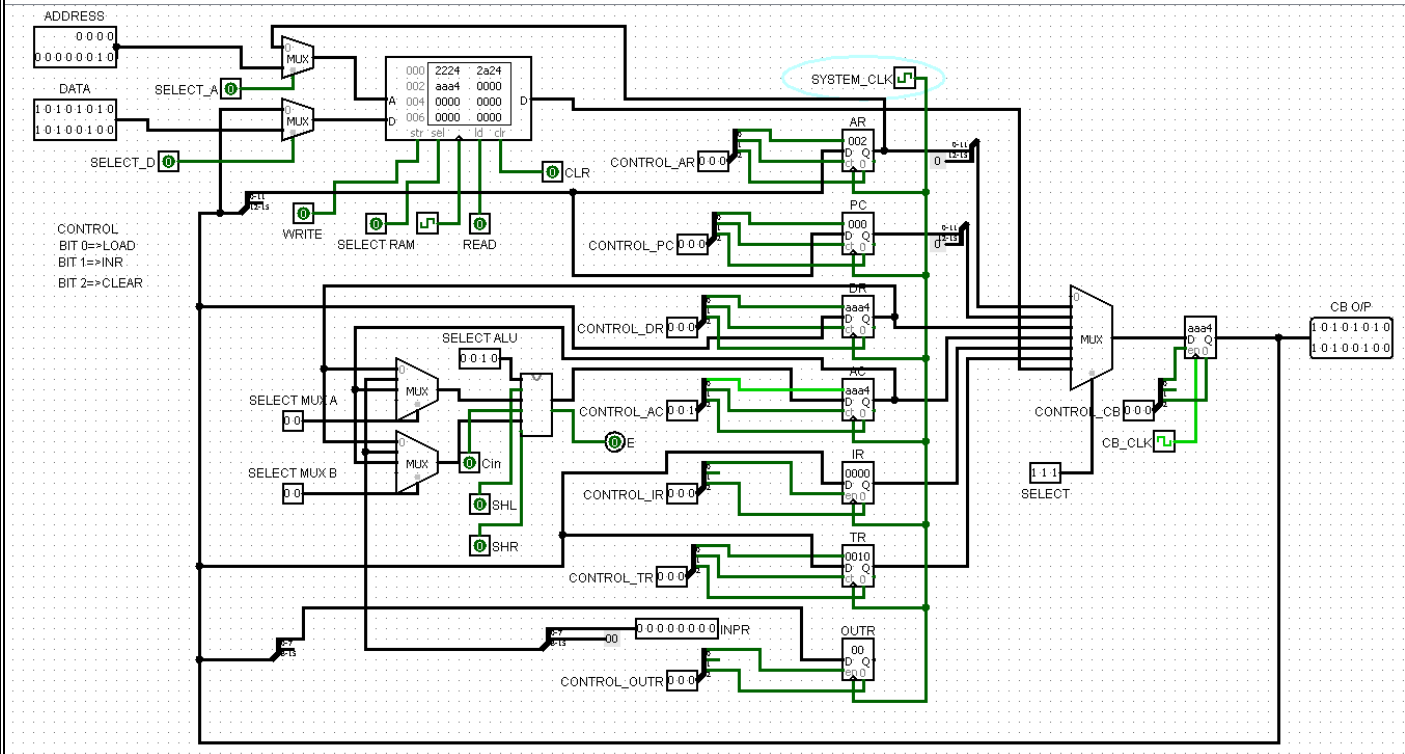
TR<-DR



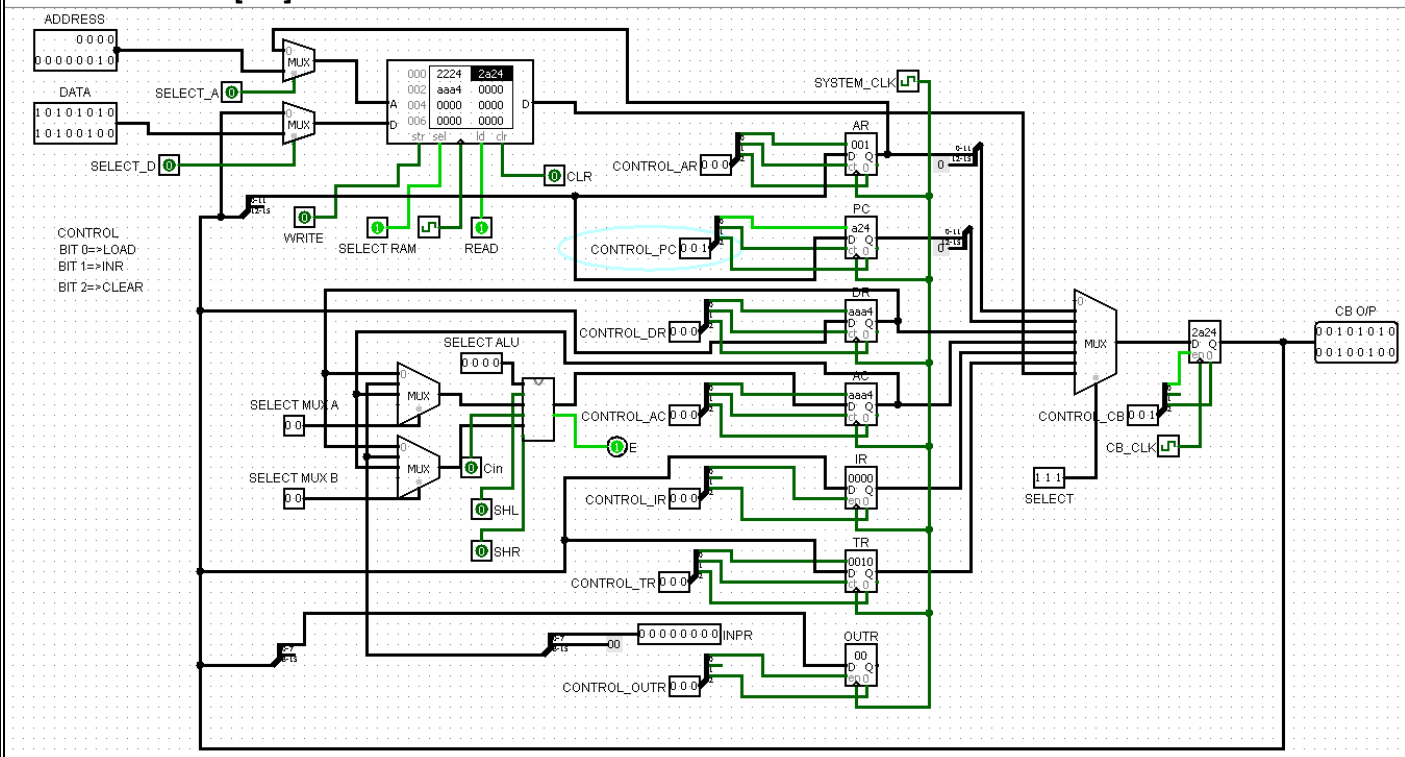
DR<-MEM[AR]



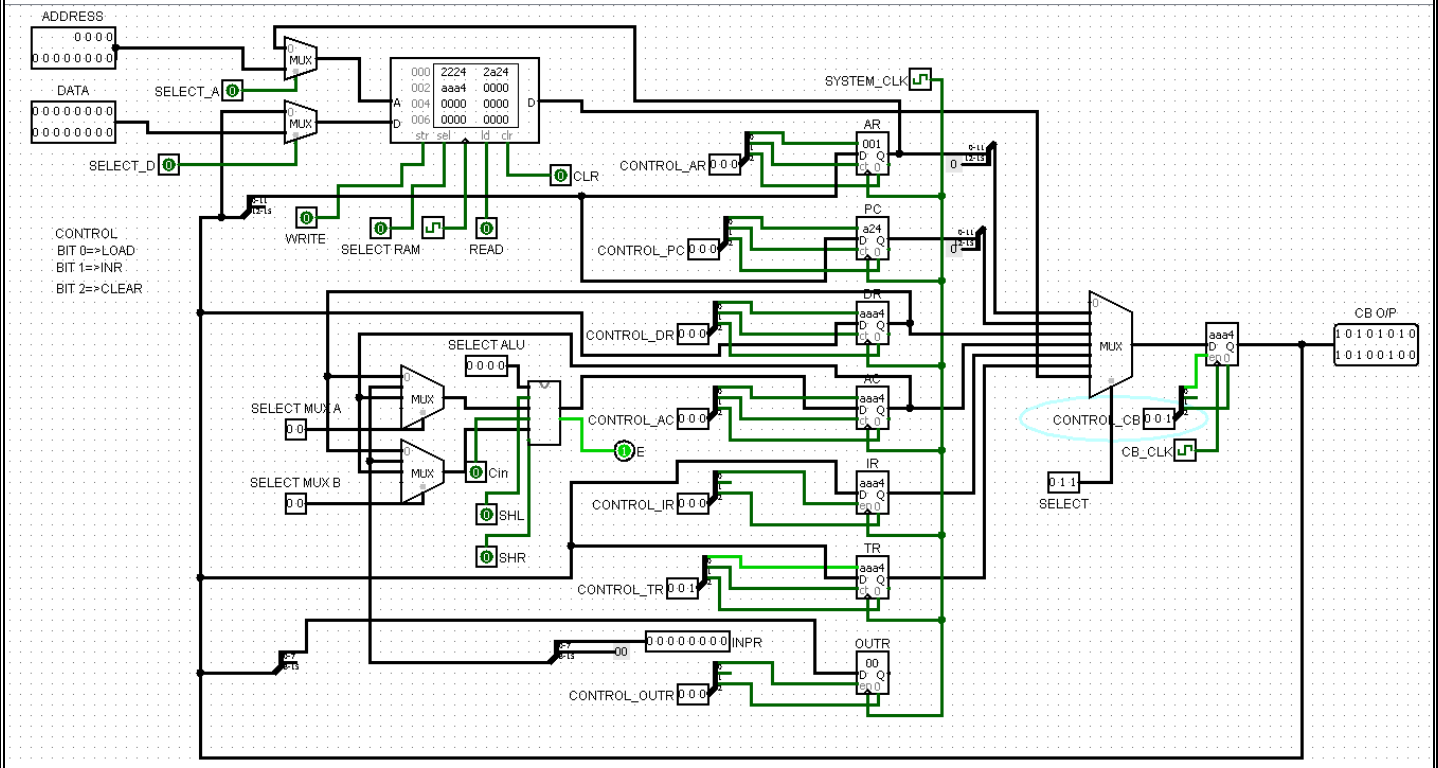
AC<-DR



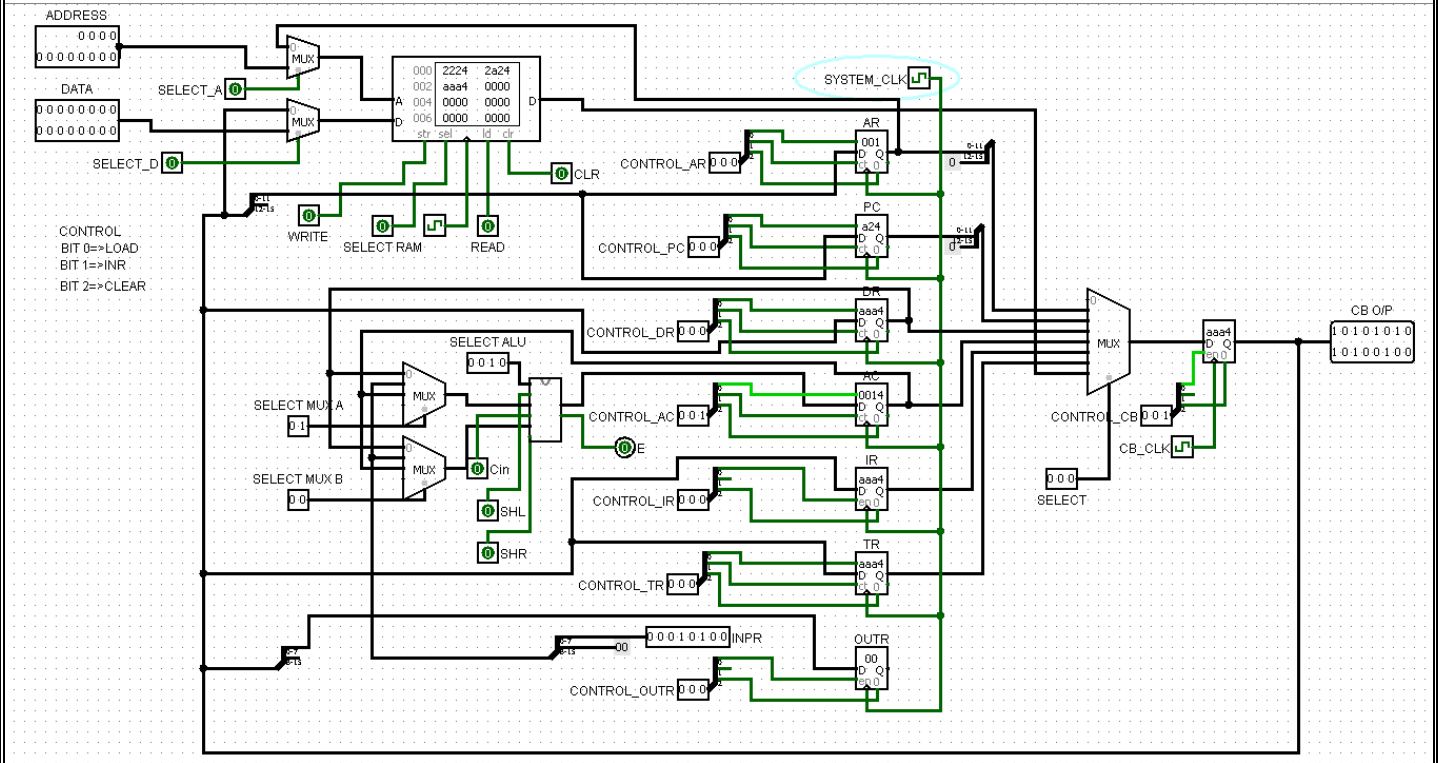
PC<-MEM[AR]



IR<-DR



AC<-INPR



CONCLUSION: