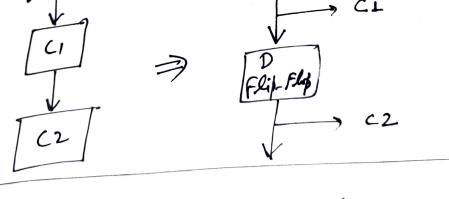
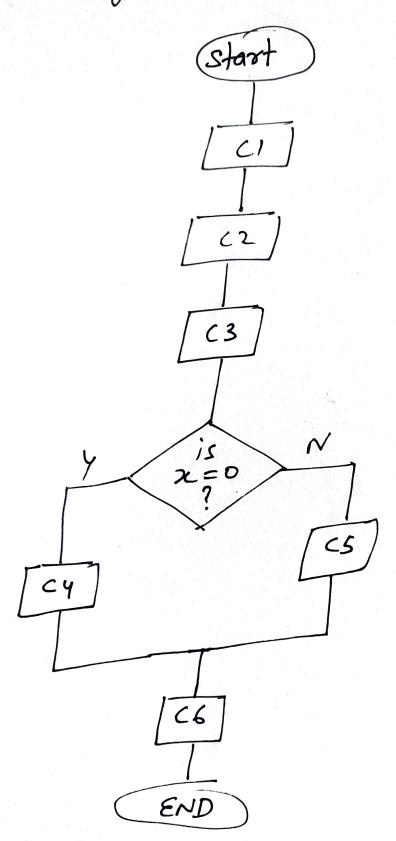
Hardwired Control Units:)
1) State Table Method 2) Delay & Element method (Flowedort method	d)
3.) Sequence Counter method (Red-world method)	
State table method Ty Iz In In instructions	و
ates $\begin{cases} I_1 & I_2 & \dots & I_n \\ I_n & \text{instructions} \\$	he B
	1 1 0
Behavior of CU is represented as output from - Control Signals are generated as output from Control Unit.	Tabel
- god for processor with less number of	
-> Redundancy is there in the circuit.	

Delay Element Method!
the behavior of CU is represented in the form of a flowchart.
form of a flow chart.
Each step in the flow chart represents a control signal to be produced.
a control signal to be practice.
Control Signals per 1011/190
require one i state casi
Hence between every two steps of the flowchart, there must be a delay
More must be a delay
Flowcher , The
element. The delay must be exactly of one The delay must be exactly of one T- state. This delay is achieved by D- flip flops. D- flip flops are inserted between
The delay is achieved by
T-state. The
The D Flip- Flops are inserted between The D Flip- Flops are inserted between
The transfer of the transfer o
every two consecutive control signals.
L CL
$\begin{bmatrix} c_1 \end{bmatrix}$
Flip Flip

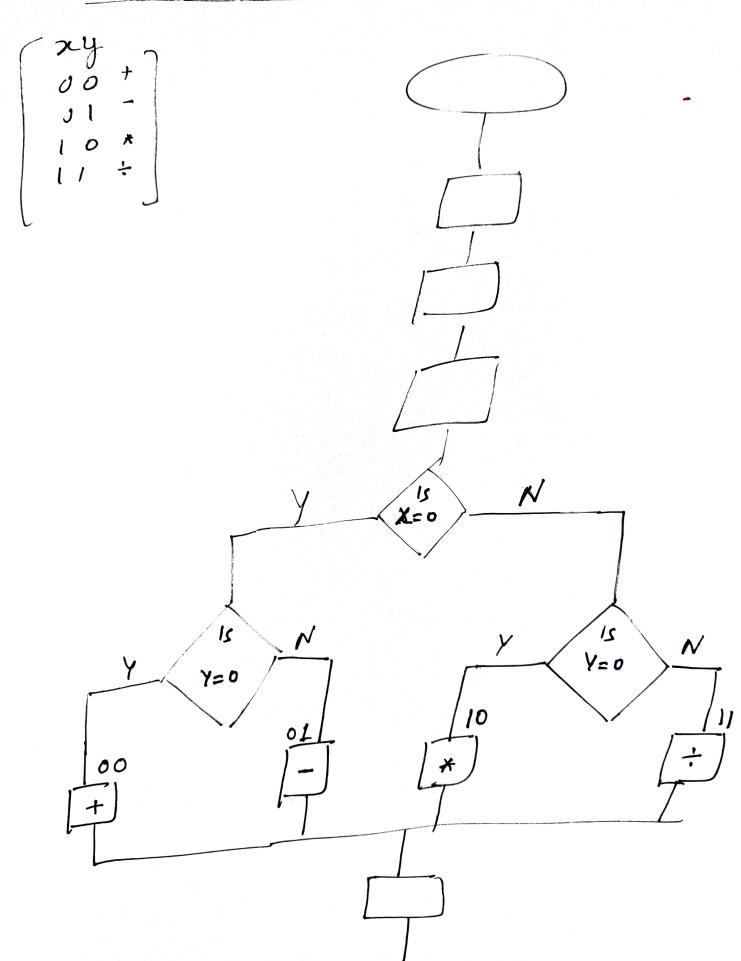


-> of all D. Flip-Flops only one will be active at a multiple entry print to combine two or more paths, we use an or gate. time.

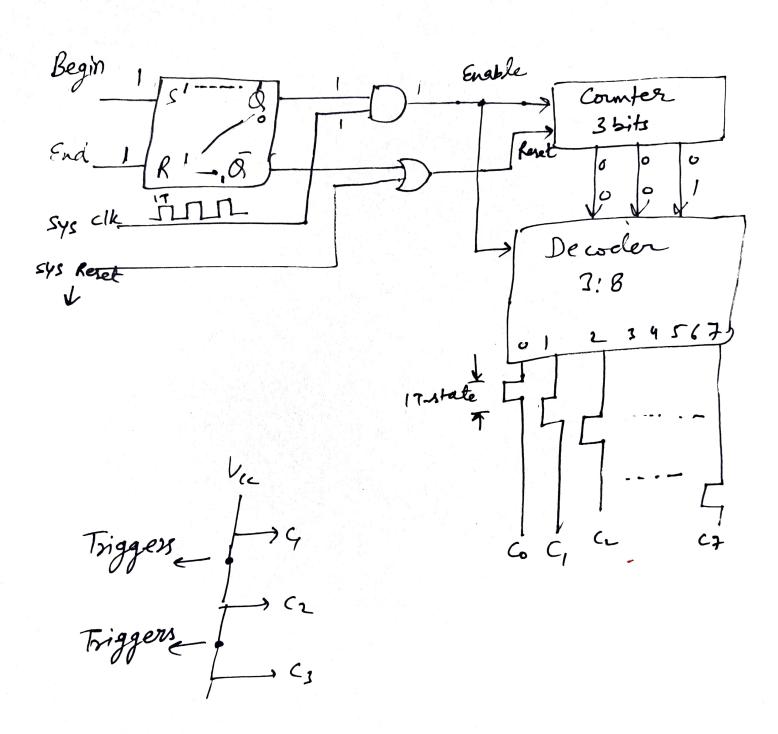
Delay clement method (Flow-chart)



four instructions:



Vcc Delay a before splithing mulhiple entry point → Each Delay elements produces the delay of one clock-cycle



- hardwired control unit.
- It follows the same logical approach of a flowchart, like the delay element method, but does not use all those unnecessary D Flip-Flops.
- > We need a delay of 1 T-state (one clock cycle) blur every two consecutive control signals.
- Adv: Avoids the use of two many

 D Flip Flops

General drawback:

1) Here are based on hardware, the circuit be comes more 4 more Complex.

- 2) such large circuits are difficult to make & Debug.
- s.) As the processor gets upgraded, the entire control unit has to be rederigned.