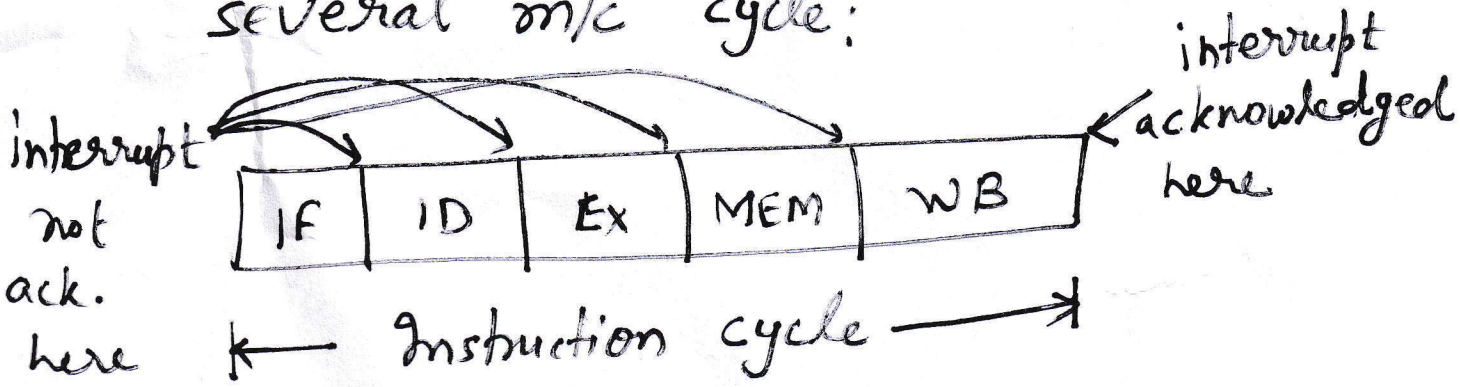
Instruction cycle :-

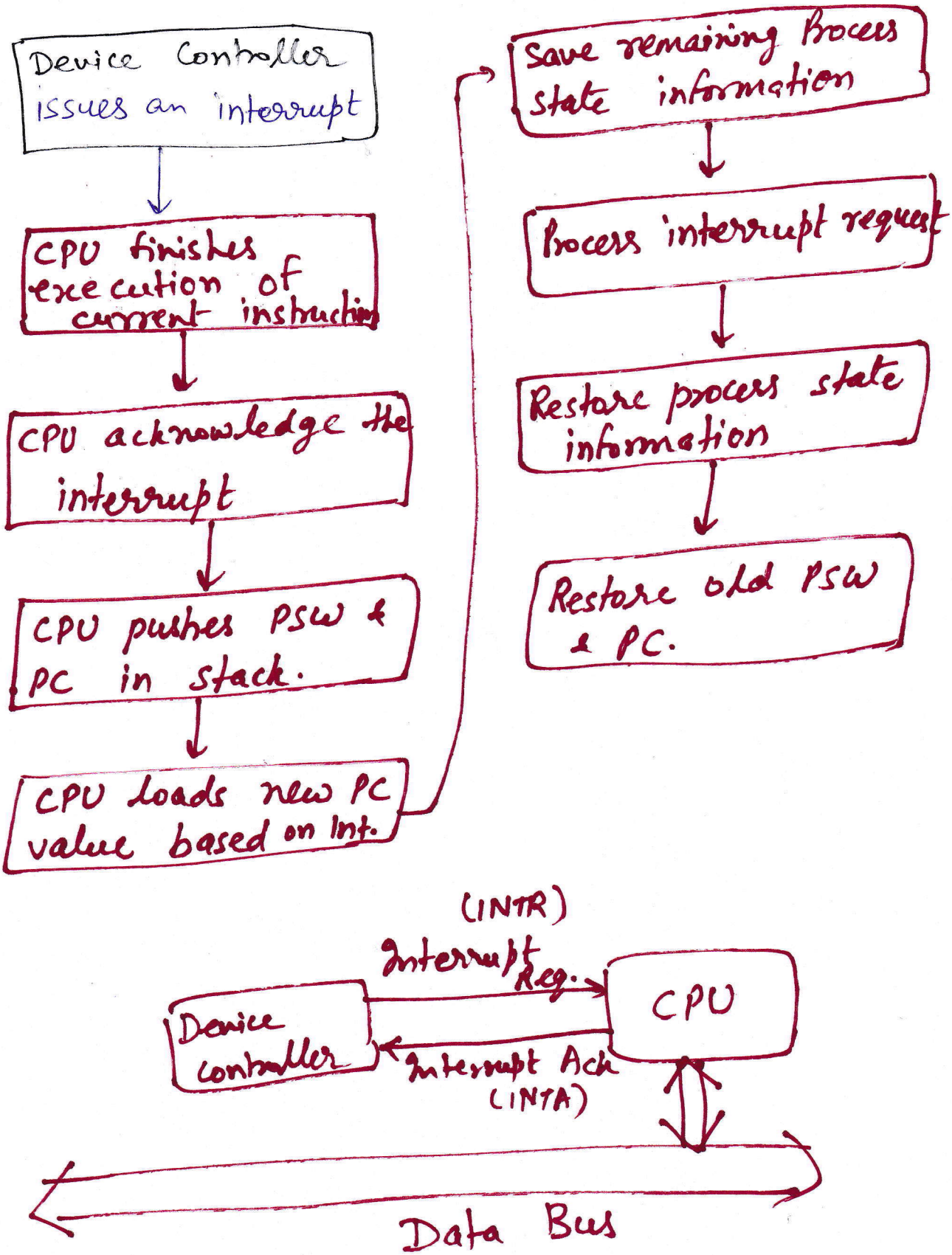
An instruction cycle consists of several m/c cycle:



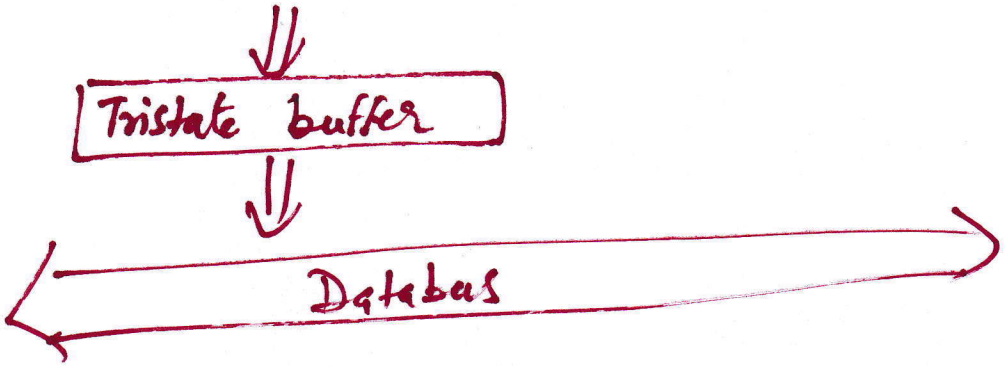
→ At the end of current instruction exe^n,
  └ PC & PSW saved automatically

→ The interrupt is acknowledged, the interrupt vector obtained, control is transferred to respective ISR.

→ After handling the interrupt, the ISR executes a special Return :- RTI (Return from interrupt).


Device Controller issues an interrupt
CPU finishes execution of current instruction
CPU acknowledge the interrupt
CPU pushes PSW & PC in stack.
CPU loads new PC value based on Int.
Save remaining Process state information
Process interrupt request
Restore process state information
Restore old PSW & PC.
(INTR)
Interrupt Req.
Device controller
CPU
Interrupt Ack (INTA)
Data Bus

→ How is the interrupt vector sent on the data bus in response to INTA ?



→ Multiple Devices Interrupting the CPU.