

image_sen



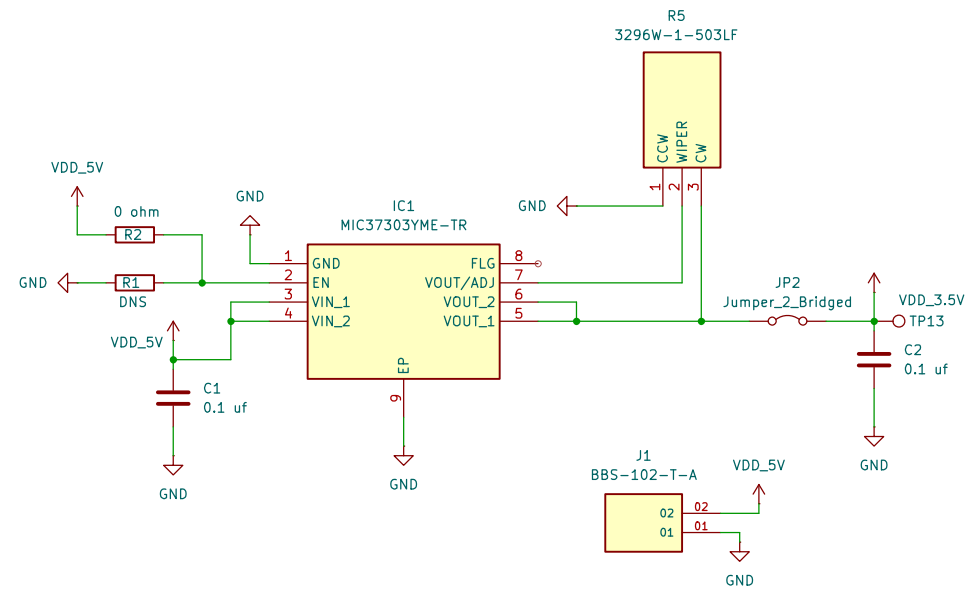
File: image_sen.kicad_sch

SENSOR

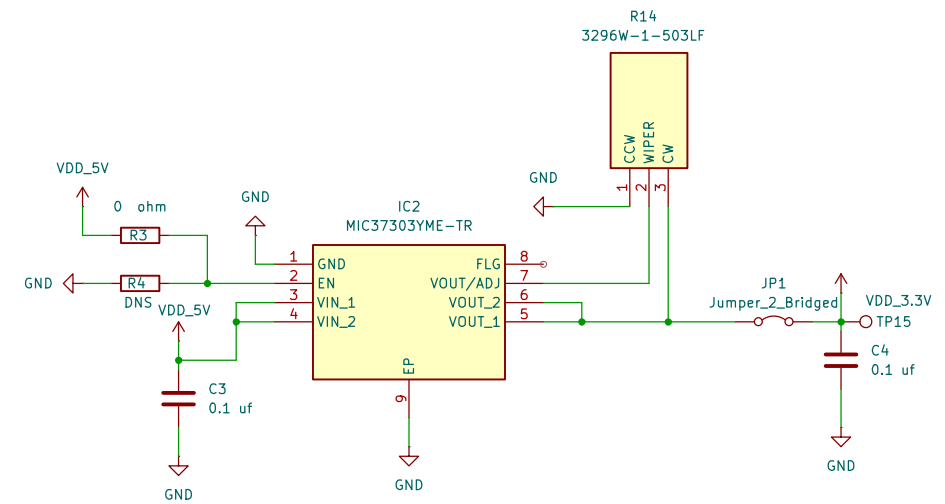


File: SENSOR_CIRCUIT.kicad_sch

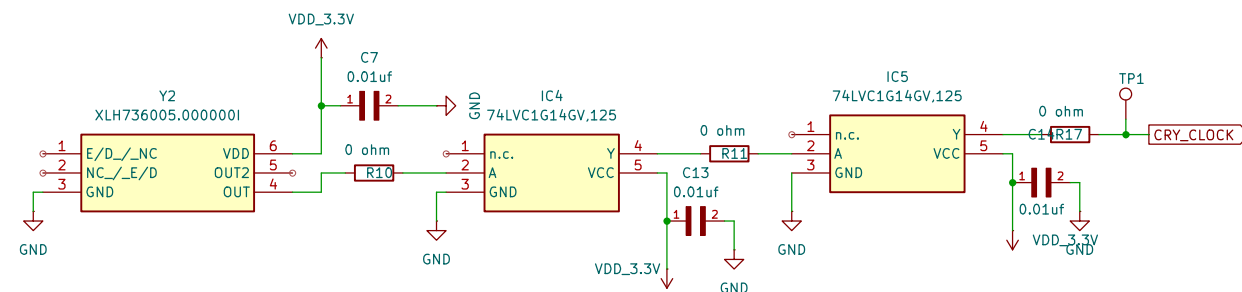
Power Circuit



Power Circuit



Crystal Oscillator



Conn_01x10_Pin

Sensor Circuit

GND 12 11 10 9 8 7 6 5 4 3 2 1

DATA+ DATA-

SEN_CLOCK

VDD_3.5V

SCL

SDA

CLOCK- CLOCK+

GND

U1

TP9 TP10 TP11 TP12

CLOCK- CLK- CLK+ DATA- DATA+

TP3 TP4

SDA SCL

VDD

CLOCK

TP2

SEN_CLOCK

VDD_3.5V

R6 10 k ohm

R7 10 k ohm

C6 0.1uf

GND

H1 H2 H3 H4 H5 H6 H7 H8

Mounting Hole

Conn_01x10_Pin

[illegible]

The diagram shows a 3-bit signal labeled **CRY_CLK** on the left. Three lines extend from this signal to three inputs on the right. The top line is labeled **3** and connects to the **CRY_CLOCK** input. The middle line is labeled **2** and connects to the **SEN_CLOCK** input. The bottom line is labeled **1** and connects to the **FPGA_CLOCK** input.

The schematic diagram illustrates the clock and data input sections of the DS90LV001TLD_NOPB IC. The top section, labeled IC3, shows the clock input (CLK-) and (CLK+) pins connected to a 100 ohm resistor (R8) and a 10uF capacitor (C11) to VDD_3.3V. The bottom section, labeled IC7, shows the data input (DATA-) and (DATA+) pins connected to a 100 ohm resistor (R9) and a 10uF capacitor (C8) to VDD_3.3V. Both sections include a 0.1uF capacitor (C10 and C12) to GND. The IC is labeled IC3 and IC7.