

# DSPIC Final Project

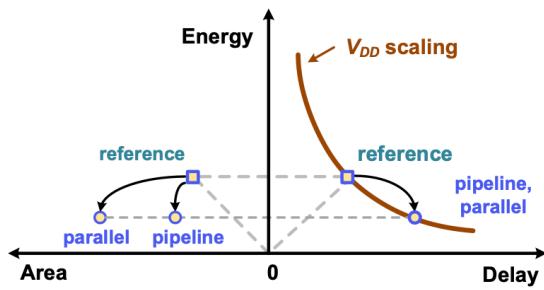
111061547 蕭翔

## 優化目標：

在作業四中，我使用了 direct form 去進行 FIR 運算，但根據上課所教，此種方法會造成 critical path 過長，以及資源利用不均衡的缺點。

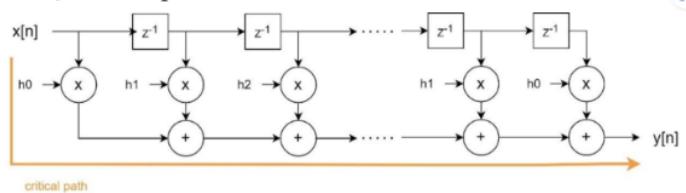
且 Direct form 的主要問題在於它對硬體資源的需求隨著 taps 數量的增加而劇烈增加，特別是對乘法器和加法器的需求。這不僅增加了硬體成本，也導致更長的處理時間和更高的功耗。

另外，由於所有的乘法操作和加法操作都集中在一個單獨的時鐘週期內，這會造成信號路徑上的延遲累積，進而影響整體系統的性能。



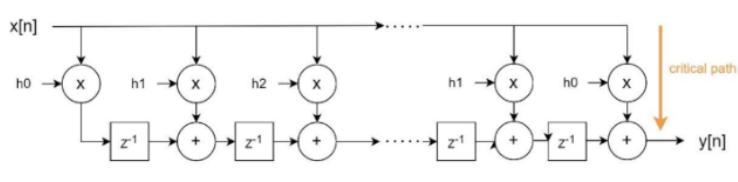
因此根據上圖，我設計了 transposed form 以及 pipeline direct form，去進行硬體的優化，讓 clock speeds 加快，且 critical path 從原本的 1 個乘法器+ (Tap\_num-1) 個加法器，降低到 1 個乘法器以及 1 個加法器，最後和原始的電路進行比較，看 power ,utilization ,timing 是否都有所改善。

Hw4 使用的 dsp structure 為 direct form。



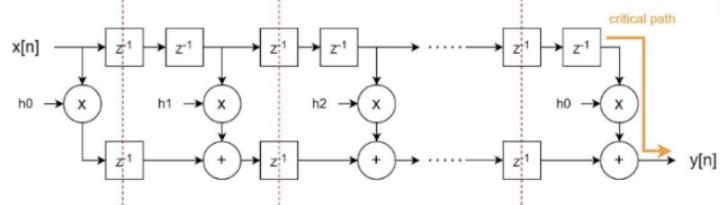
改善過後的兩種架構，如下。

Transposed form



(Figure 2) Transposed Form FIR filter

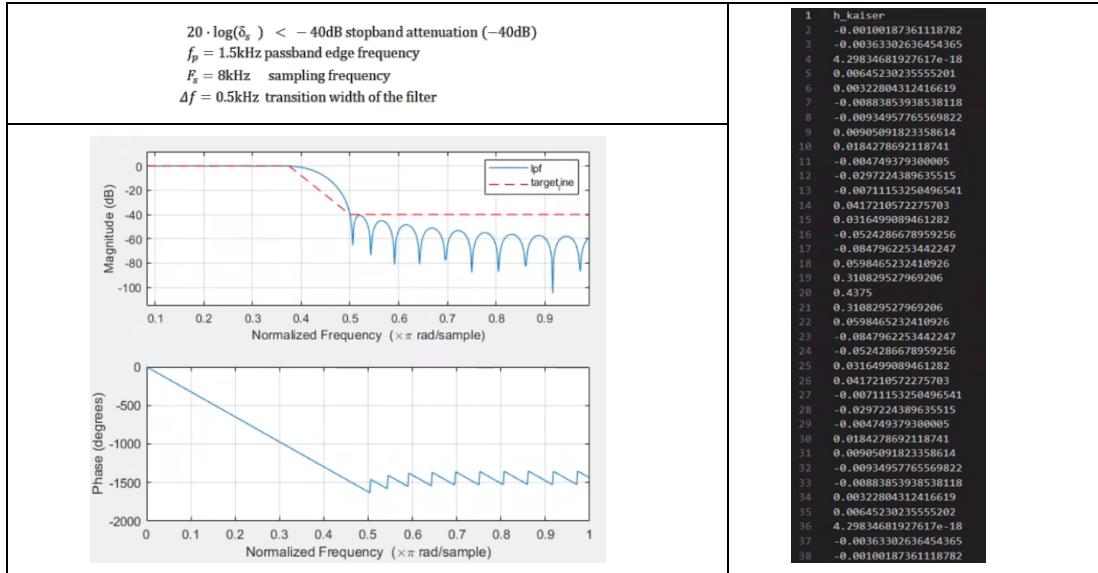
Pipeline direct form



(Figure 3) Pipelined Direct Form FIR Filter

## Software:

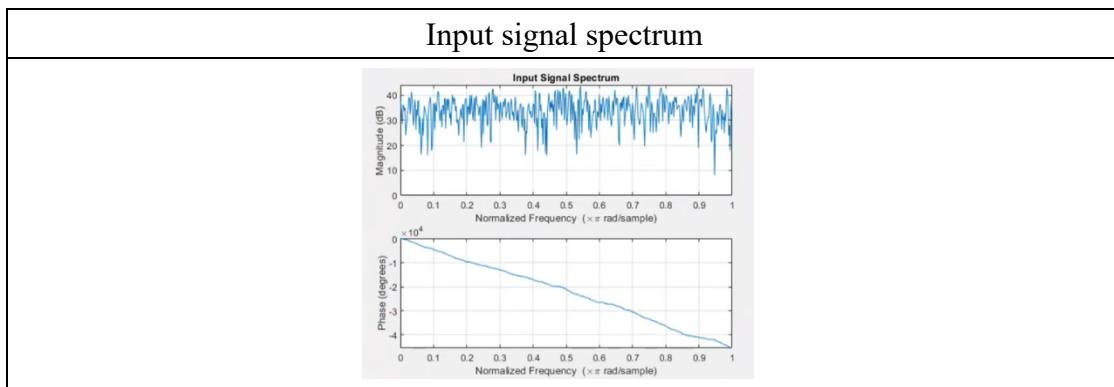
根據作業四的規格去出發，且使用 Kaiser window 去尋找 tap 以利用於後續的 Cpp 模擬運算，且找出了 37 個 tap，成果如右圖以及下圖

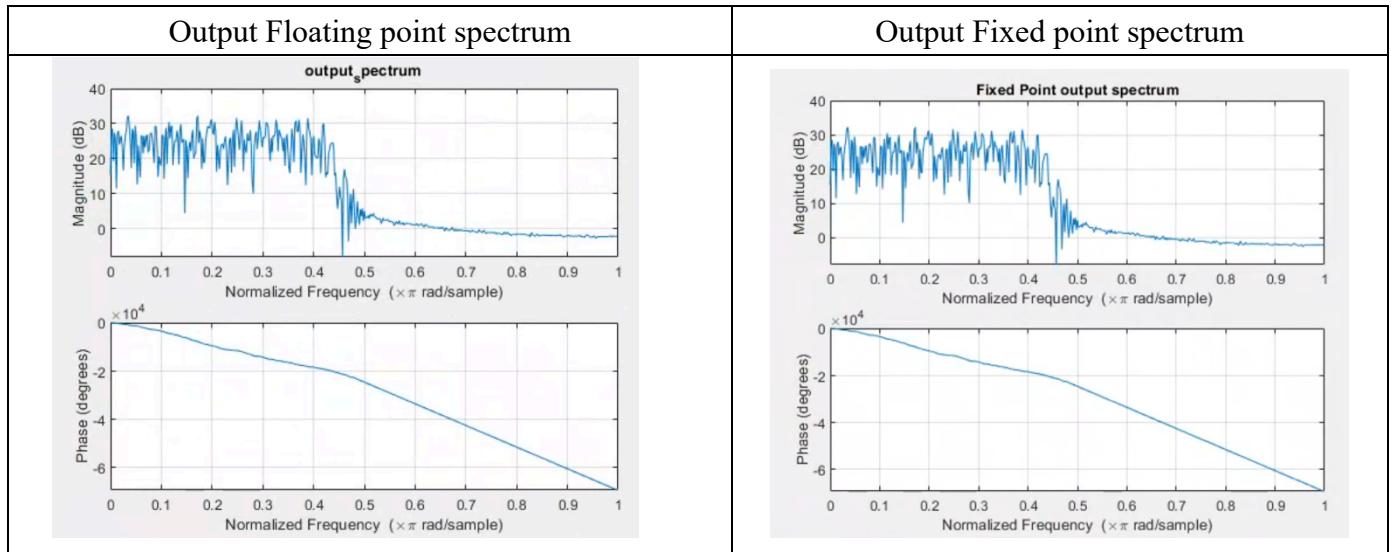


接著就進行作業 4 的 C/C++的浮點數以及定點數的模擬，一開始需要先建立一組 random 的 input signal 且 average power=1，因此我創建一份 500 筆在 [-50,50]的 uniform distribution 的隨機數列，並且計算平方和，且除以 length 讓他們都平均功率=1，當作 input signal，且每次 compile 一次 C++，都會產生不同的 random input，好讓我可以完成隨機三組以上的 FIR 濾波器的硬體模擬。

有了上述所需要的 random input，接著就根據 quantize 的定義去依序去算出 output，且我使用了兩種 function，一種是 filt\_fp 這種是屬於計算 floating point 的 output，其中不需要經過一些量化過程，只需要創造一個可以進行 shift 的 input buffer 再將 MATLAB 算出來的 coef 進行卷積就可以得出結果，且 C++會自動將硬體所需要的 data 紙自動存在 data/HW\_input.txt, data/HW\_golden.txt, data/HW\_coef.txt，方便做保存以及測試。

另外一種 function 是 fixed point 的計算叫做 filt\_quant，這種計算過程需要加入 input\_WL, MAC\_WL 以及 tap\_num，因為定點數的運算有需要對輸出做到位移以及截斷 bits 的操作，另外也有添加 noise，這裡也用了一個布林值來去決定是否要增加噪音。

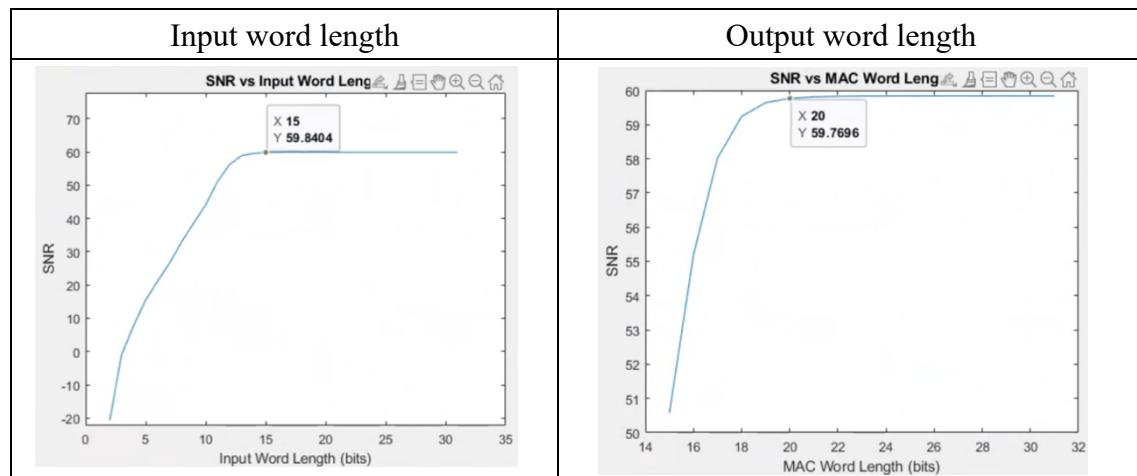
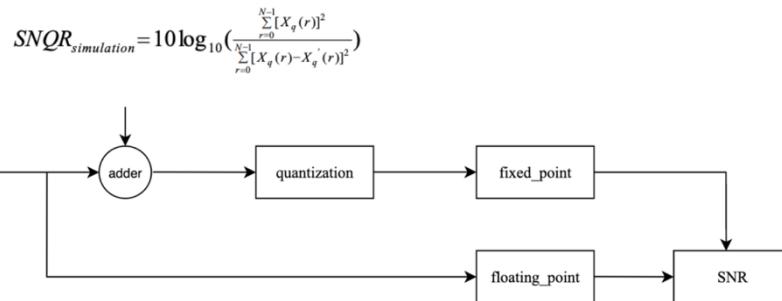




而 SNR 的計算方式是使用下圖結構的方式去計算，將量化過後的 fp 的 signal 放在分子進行平方和，分母則為量化過後的(fp signal -fixed signal)的平方，最後再取  $10 \cdot \log_{10}$  作為 SNR\_value。

接着進行 word\_length 的尋找，我使用迴圈將 input signal 的 SNR\_value 從 0 開始往上數，且可以發現，當 **input\_word\_length=15bits** 時，SNR 曲線會趨近平緩，因此這裡即可以設定 **input\_word\_length=15bits** 去進行 mac\_word\_length 的模擬。進行 mac\_word\_length 的模擬時，使用 **input\_word\_length=15** 開始進行迴圈上數，可以發現在 20bits 時會趨近平緩，這時即可設定

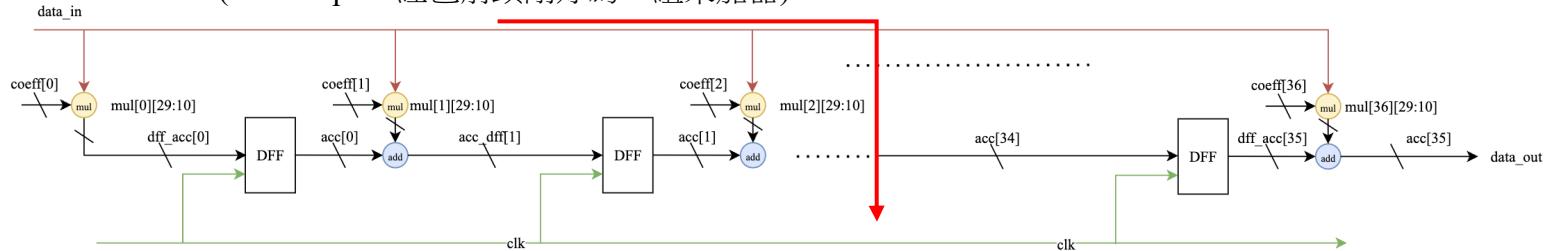
**Input word\_length =15bits , Mac word\_length=20bits**。



## Hardware:

### Transposed Form Block Diagram:

(Critical path 紅色箭頭剛好為一組乘加器)



設定 inWL=15bits 以及 macWL=20bits 進行運算，但因為 data 和 coeff 的位寬皆為 15bits，因此兩者做乘法結果的位寬我設定為 inWL\*2-1=29bits，但是因為 SNR 模擬 mac\_word length 的結果為 20bits，因此需要取[29:10]當作 data\_out 的位寬，才會符合 C/C++模擬出來的 golden data 的結果。

且 transposed form 和 direct form 的差異在於 direct form 是把 DFF 放在 data\_in 的路徑上面，但是 transposed form 則是將 DFF 放在累加器的路徑上面，因此需要設定 dff\_acc[19:0]經過一個 DFF 輸出產生 acc[19:0]，將第一組 data 和 coeff 相乘的結果設定為 mul[idx]，且使用迴圈形式直接展開，完成 37 組 tap 對 data 的相乘，並且將相乘結果和上一級產生出來的 acc[idx-1]做相加，即可以送到下一級的 dff\_acc[idx]，並且將 acc[35]輸出給 data\_out，和 golden data 做比對，經過這些過程，即可以實現出 transposed form 的 FIR 運算。

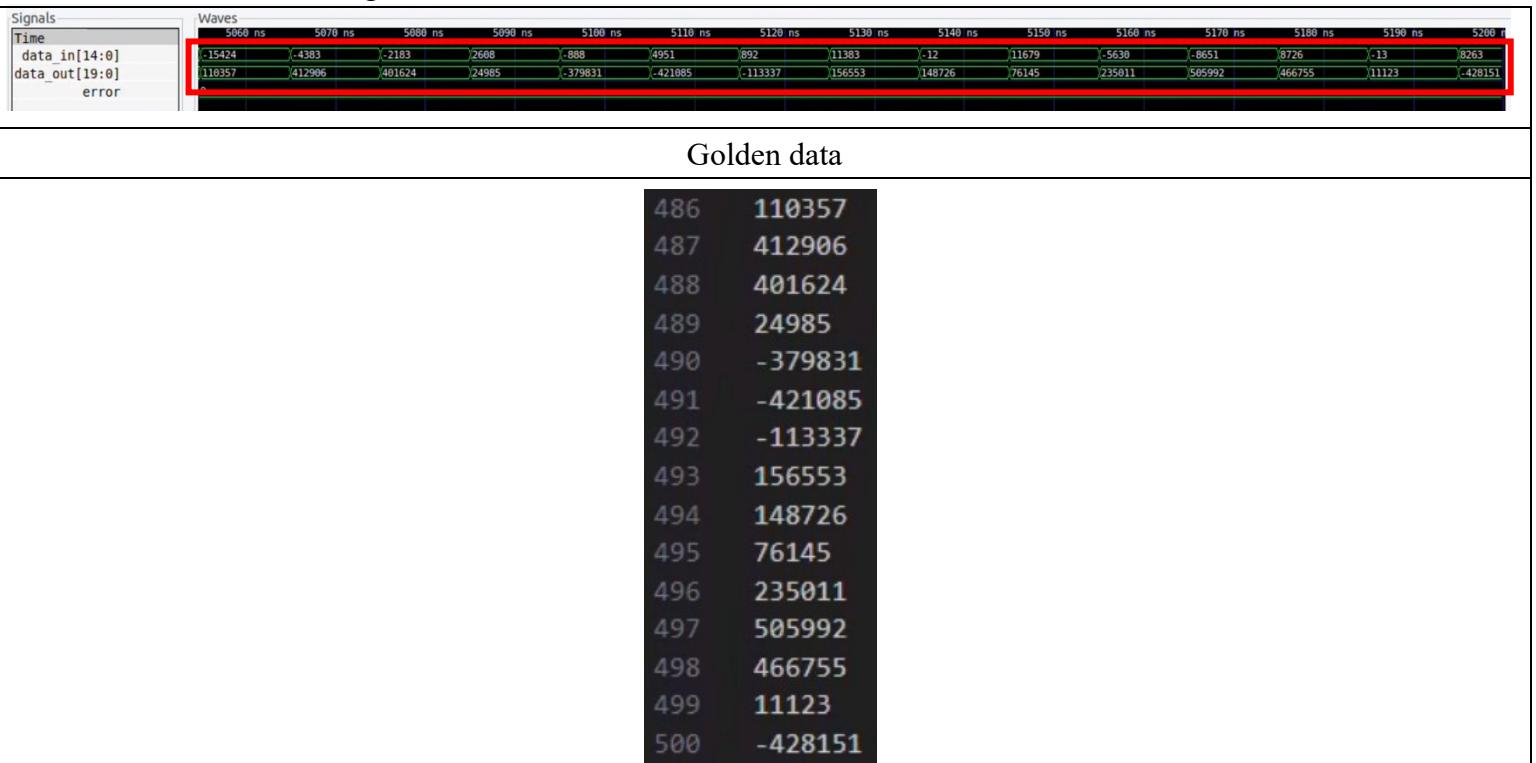
### Transposed Form Simulation Result:

使用 C++隨機產生出三組 500 筆不同的 random data 放入此 FIR 進行比對，隨機產生一組信號通過測試的話會輸出下圖：cycle time :5200ns

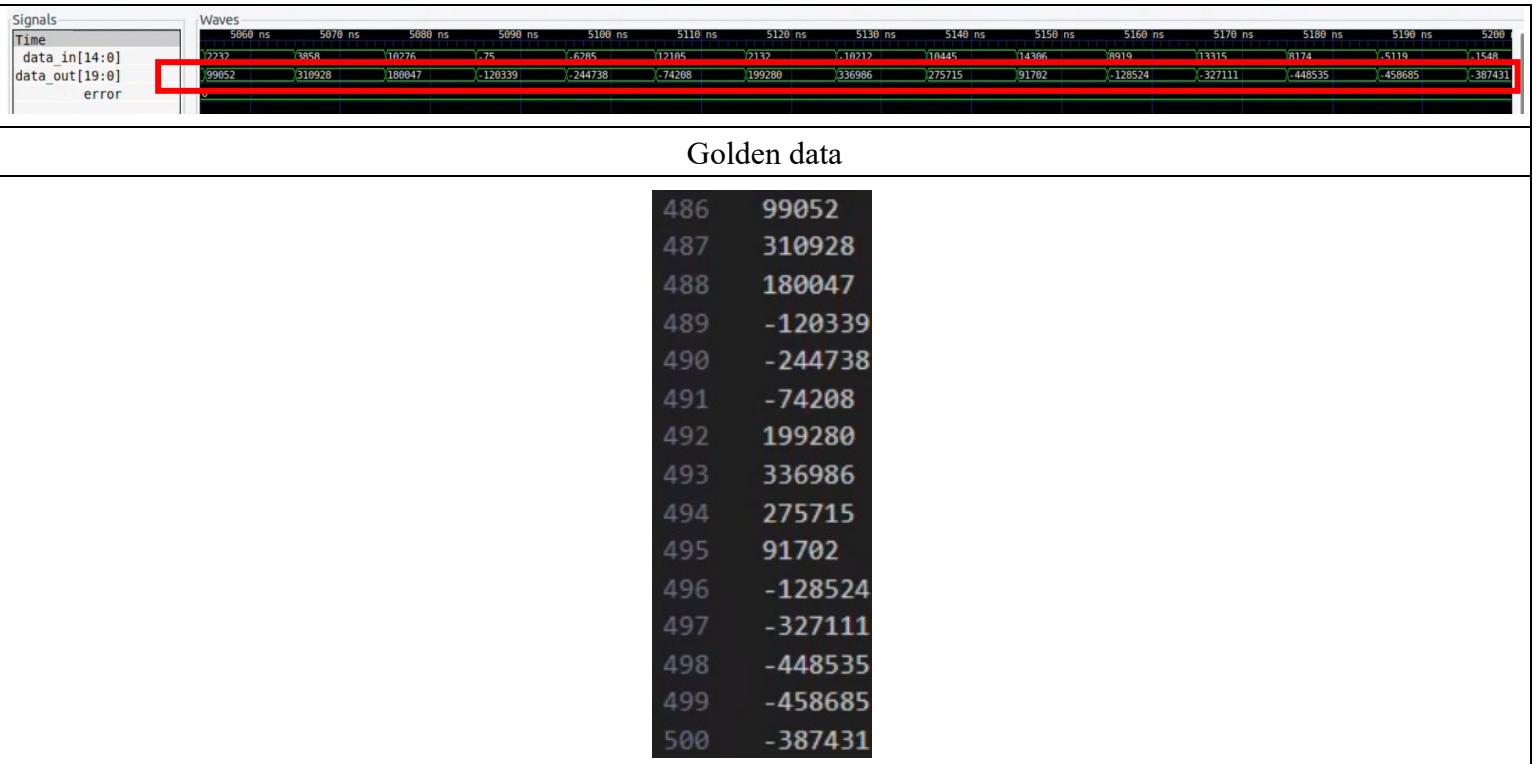
```
[PASS][Pattern]-41649=-41649
[PASS][Pattern]-19281=-19281
[PASS][Pattern]152842=152842
[PASS][Pattern]311104=311104
[PASS][Pattern]207081=207081
[PASS][Pattern]-135822=-135822
[PASS][Pattern]-409441=-409441
[PASS][Pattern]-381572=-381572
[PASS][Pattern]-143318=-143318
[PASS][Pattern]67245=67245
[PASS][Pattern]151953=151953
[PASS][Pattern]179299=179299
[PASS][Pattern]215145=215145
[PASS][Pattern]256804=256804
[PASS][Pattern]275387=275387
[PASS][Pattern]239965=239965
[PASS][Pattern]103640=103640
All answers match golden
$finish called at time : 5200 ns
```

使用 gtkwave 進行波形檢視（因為空間有限，因此我只放 wave 的後面幾筆 data 以及相對應的 golden data 當作參考）

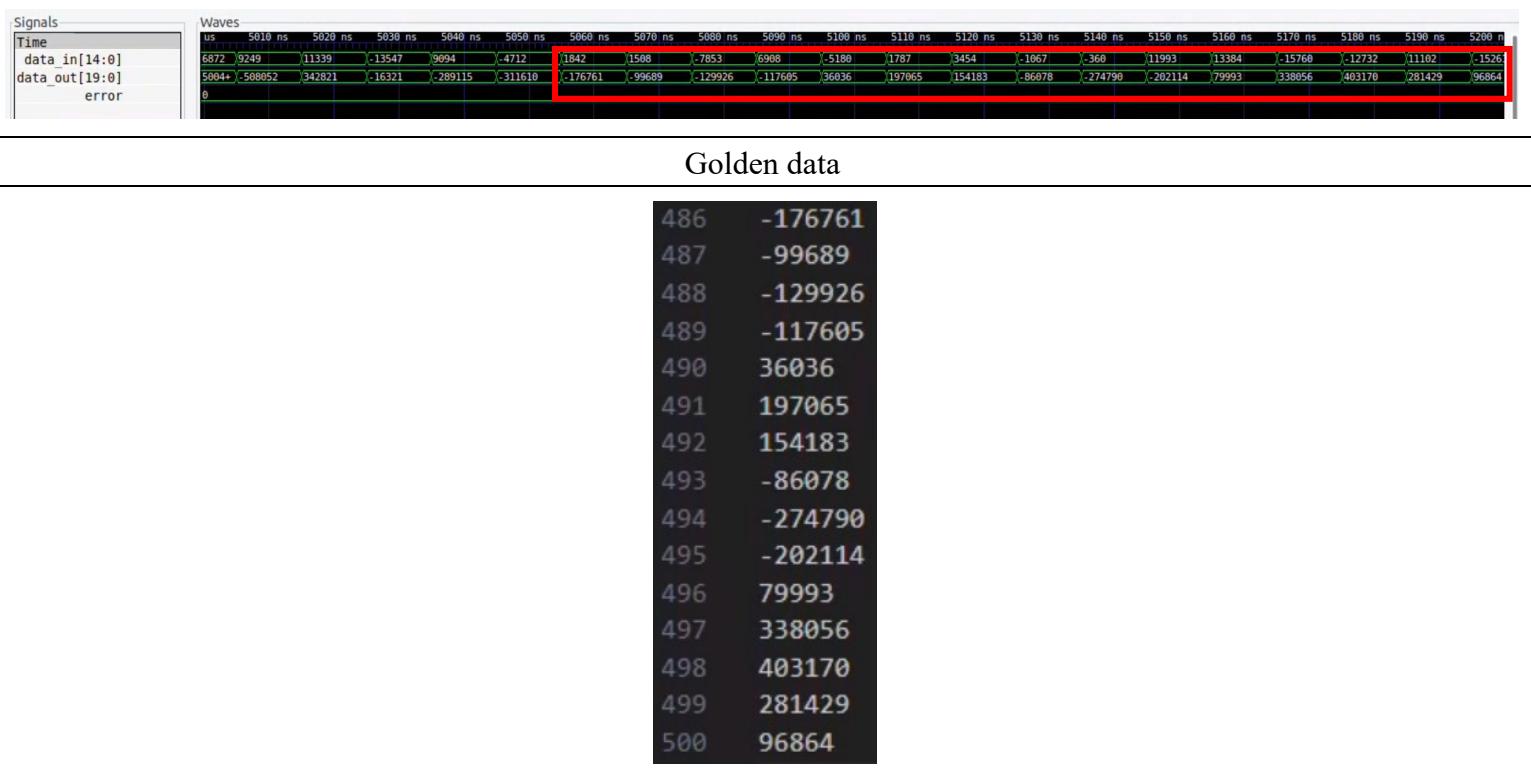
#### Random signal set one:



#### Random signal set two:



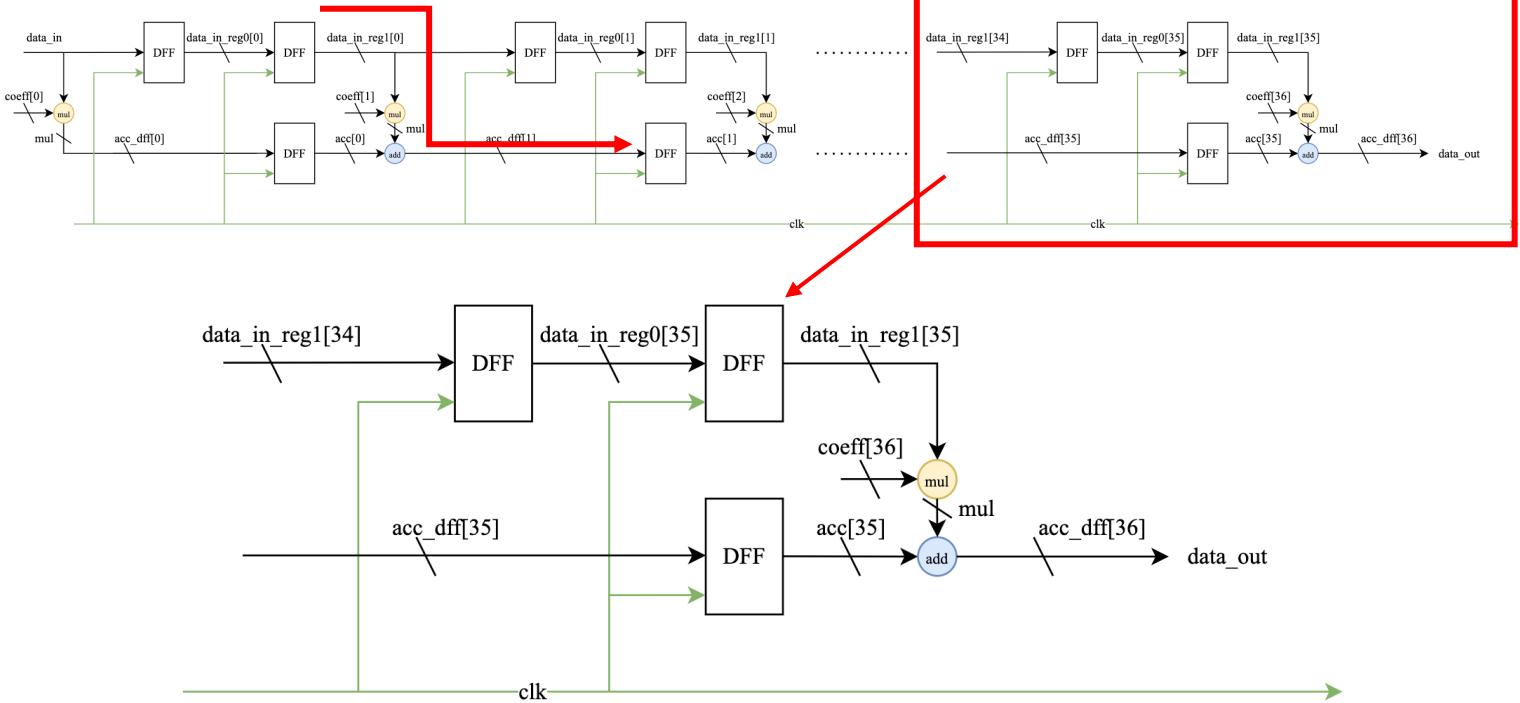
### Random signal set three:



以上為三組隨機信號送給 transposed form 形式的 FIR 運算結果，都符合 C/C++模擬出來的 golden data。

### Pipline Direct Form Block Diagram:

為了讓 direct form 的 critical path 降為一組乘加器（紅色箭頭），因此進行 pipeline 的設計，電路 block diagram 的結果如下



在這次的 pipeline 設計中，為了要讓 critical path 縮短成一組乘加器，所以需要在 data\_in 的 path 以及 acc 的 path 多放上一個 DFF，因此必須要分別設定 data\_in\_reg0 以及 data\_in\_reg1，data\_in\_reg1 主要是用於進行乘加操作，而一開始的 acc[0] 則是由 data\_in 的第一筆資料直接和 coeff[0] 做乘法輸出給 acc[0]，之後的邏輯也是一樣，運用 data\_in\_reg[i] 和 coeff[i+1] 做相乘，再和前一級的累加結果 acc[i] 做相加，輸出給 acc\_dff[i+1]，再送進 DFF 提供給下一層的乘加運算進行操作，最後進行最後一層的操作將 acc\_dff[36] 輸出給 data\_out，因為最後輸出並不需要再經過 DFF，即可以輸出結果。

其中因為輸出位寬 mac\_WL=20bits 的限制，因此還是需要將 mul 取 [29:10] 再送給 acc 進行加法運算，這樣運算結果才會符合一開始軟體運算時設定的位寬限制。

### Pipeline direct Form Simulation Result:

Cycle time : 5375ns

隨機產生一組信號通過測試的話會輸出下圖 cycle time :5375ns

```
[PASS][Pattern 492]67245=67245
[PASS][Pattern 493]151953=151953
[PASS][Pattern 494]179299=179299
[PASS][Pattern 495]215145=215145
[PASS][Pattern 496]256804=256804
[PASS][Pattern 497]275387=275387
[PASS][Pattern 498]239965=239965
[PASS][Pattern 499]103640=103640
All answers match golden
$finish called at time : 5375 ns
```

因為實現 pipeline structure 多加了 35 級的 DFF，因此在 testbench 需要多 delay 350ns 才可以開始進行 golden data 和 data\_out 的比對。



使用 C++ 產生出三組 500 筆的 random data 進行 pipeline FIR 運算  
(因為空間有限，因此我只放 wave 的頭跟尾以及相對應的 golden data)

### Random data set one:



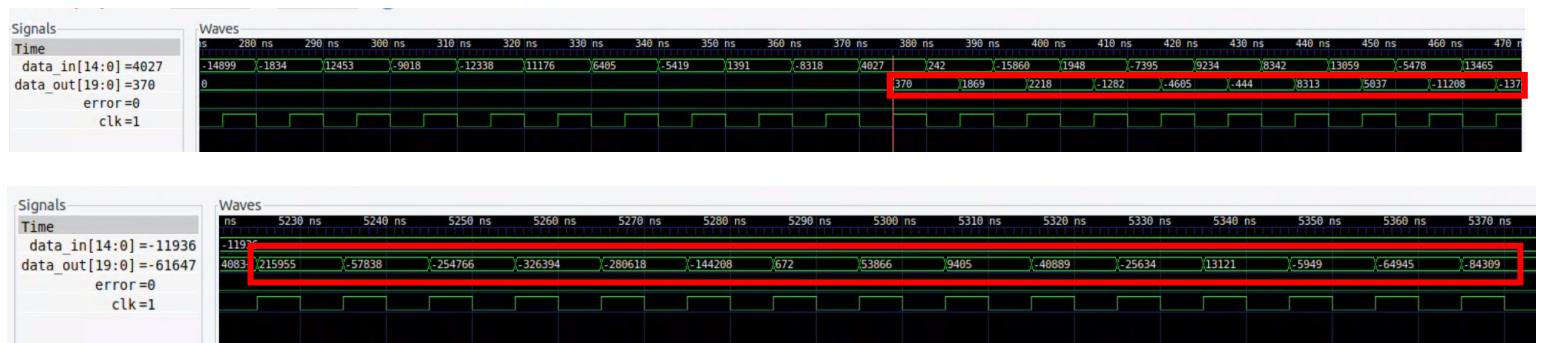
## Random data set two:



### Golden data

|    |        |     |         |
|----|--------|-----|---------|
| 1  | 546    | 487 | 80705   |
| 2  | 1472   | 488 | -73565  |
| 3  | -1209  | 489 | -121874 |
| 4  | -976   | 490 | 71086   |
| 5  | 2778   | 491 | 348528  |
| 6  | 3003   | 492 | 459339  |
| 7  | -1850  | 493 | 375177  |
| 8  | -5579  | 494 | 282620  |
| 9  | -1739  | 495 | 299246  |
| 10 | 6253   | 496 | 349875  |
| 11 | 7673   | 497 | 327724  |
| 12 | -5359  | 498 | 231202  |
| 13 | -15880 | 499 | 96027   |
| 14 | 1295   | 500 | -69681  |
| 15 | 28639  |     |         |
| 16 | 14067  |     |         |

### Random data set three:



### Golden data

|    |         |     |         |
|----|---------|-----|---------|
| 1  | 370     | 483 | 27969   |
| 2  | 1869    | 484 | 341014  |
| 3  | 2218    | 485 | 408317  |
| 4  | -1282   | 486 | 215955  |
| 5  | -4605   | 487 | -57838  |
| 6  | -444    | 488 | -254766 |
| 7  | 8313    | 489 | -326394 |
| 8  | 5037    | 490 | -280618 |
| 9  | -11208  | 491 | -144208 |
| 10 | -13747  | 492 | 672     |
| 11 | 12149   | 493 | 53866   |
| 12 | 26770   | 494 | 9405    |
| 13 | -7076   | 495 | -40889  |
| 14 | -44987  | 496 | -25634  |
| 15 | -10712  | 497 | 13121   |
| 16 | 70120   | 498 | -5949   |
| 17 | 51235   | 499 | -64945  |
| 18 | -145614 | 500 | -84309  |
| 19 | -372237 |     |         |
| 20 | -408982 |     |         |

以上為三組隨機信號送給 pipeline direct form 形式的 FIR 運算結果，都符合 C/C++模擬出來的 golden data。

## Synthesis Result: 使用 pynq-Z2 去合成

### Power:

|                                     |                |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
|-------------------------------------|----------------|---|----------------------|---------|----------------------|---------------|----------------------|-----|-----------------------|--------|-----------------|----------------|----------------|----------|-------------------------------------|-----|-------------------|-----|----------|---------------|---------|---------------|----------|---------------|--------|---------------|------|---------------|------|---------------|----------------|---------------|
| <u>Direct form</u>                  | 0.182W         | <p><b>Summary</b></p> <p>Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.</p> <table border="1"> <tr><td>Total On-Chip Power:</td><td>0.182 W</td></tr> <tr><td>Design Power Budget:</td><td>Not Specified</td></tr> <tr><td>Power Budget Margin:</td><td>N/A</td></tr> <tr><td>Junction Temperature:</td><td>27.1°C</td></tr> <tr><td>Thermal Margin:</td><td>57.9°C (4.8 W)</td></tr> <tr><td>Effective 8JA:</td><td>11.5°C/W</td></tr> <tr><td>Power supplied to off-chip devices:</td><td>0 W</td></tr> <tr><td>Confidence level:</td><td>Low</td></tr> </table> <p><a href="#">Launch Power Constraint Advisor</a> to find and fix invalid switching activity</p> <p><b>On-Chip Power</b></p> <table border="1"> <tr><td>Dynamic:</td><td>0.214 W (67%)</td></tr> <tr><td>Clocks:</td><td>0.032 W (15%)</td></tr> <tr><td>Signals:</td><td>0.030 W (14%)</td></tr> <tr><td>Logic:</td><td>0.033 W (15%)</td></tr> <tr><td>DSP:</td><td>0.055 W (26%)</td></tr> <tr><td>I/O:</td><td>0.064 W (30%)</td></tr> <tr><td>Device Static:</td><td>0.108 W (33%)</td></tr> </table> | Total On-Chip Power: | 0.182 W | Design Power Budget: | Not Specified | Power Budget Margin: | N/A | Junction Temperature: | 27.1°C | Thermal Margin: | 57.9°C (4.8 W) | Effective 8JA: | 11.5°C/W | Power supplied to off-chip devices: | 0 W | Confidence level: | Low | Dynamic: | 0.214 W (67%) | Clocks: | 0.032 W (15%) | Signals: | 0.030 W (14%) | Logic: | 0.033 W (15%) | DSP: | 0.055 W (26%) | I/O: | 0.064 W (30%) | Device Static: | 0.108 W (33%) |
| Total On-Chip Power:                | 0.182 W        |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Design Power Budget:                | Not Specified  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power Budget Margin:                | N/A            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Junction Temperature:               | 27.1°C         |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Thermal Margin:                     | 57.9°C (4.8 W) |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Effective 8JA:                      | 11.5°C/W       |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power supplied to off-chip devices: | 0 W            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Confidence level:                   | Low            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Dynamic:                            | 0.214 W (67%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Clocks:                             | 0.032 W (15%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Signals:                            | 0.030 W (14%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Logic:                              | 0.033 W (15%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| DSP:                                | 0.055 W (26%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| I/O:                                | 0.064 W (30%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Device Static:                      | 0.108 W (33%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| <u>Transposed form</u>              | 0.322W         | <p><b>Summary</b></p> <p>Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.</p> <table border="1"> <tr><td>Total On-Chip Power:</td><td>0.322 W</td></tr> <tr><td>Design Power Budget:</td><td>Not Specified</td></tr> <tr><td>Power Budget Margin:</td><td>N/A</td></tr> <tr><td>Junction Temperature:</td><td>28.7°C</td></tr> <tr><td>Thermal Margin:</td><td>56.3°C (4.7 W)</td></tr> <tr><td>Effective 8JA:</td><td>11.5°C/W</td></tr> <tr><td>Power supplied to off-chip devices:</td><td>0 W</td></tr> <tr><td>Confidence level:</td><td>Low</td></tr> </table> <p><a href="#">Launch Power Constraint Advisor</a> to find and fix invalid switching activity</p> <p><b>On-Chip Power</b></p> <table border="1"> <tr><td>Dynamic:</td><td>0.119 W (53%)</td></tr> <tr><td>Clocks:</td><td>0.026 W (22%)</td></tr> <tr><td>Signals:</td><td>0.015 W (13%)</td></tr> <tr><td>Logic:</td><td>0.013 W (11%)</td></tr> <tr><td>DSP:</td><td>0.040 W (34%)</td></tr> <tr><td>I/O:</td><td>0.024 W (20%)</td></tr> <tr><td>Device Static:</td><td>0.106 W (47%)</td></tr> </table> | Total On-Chip Power: | 0.322 W | Design Power Budget: | Not Specified | Power Budget Margin: | N/A | Junction Temperature: | 28.7°C | Thermal Margin: | 56.3°C (4.7 W) | Effective 8JA: | 11.5°C/W | Power supplied to off-chip devices: | 0 W | Confidence level: | Low | Dynamic: | 0.119 W (53%) | Clocks: | 0.026 W (22%) | Signals: | 0.015 W (13%) | Logic: | 0.013 W (11%) | DSP: | 0.040 W (34%) | I/O: | 0.024 W (20%) | Device Static: | 0.106 W (47%) |
| Total On-Chip Power:                | 0.322 W        |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Design Power Budget:                | Not Specified  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power Budget Margin:                | N/A            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Junction Temperature:               | 28.7°C         |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Thermal Margin:                     | 56.3°C (4.7 W) |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Effective 8JA:                      | 11.5°C/W       |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power supplied to off-chip devices: | 0 W            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Confidence level:                   | Low            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Dynamic:                            | 0.119 W (53%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Clocks:                             | 0.026 W (22%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Signals:                            | 0.015 W (13%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Logic:                              | 0.013 W (11%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| DSP:                                | 0.040 W (34%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| I/O:                                | 0.024 W (20%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Device Static:                      | 0.106 W (47%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| <u>Pipeline Direct form</u>         | 0.225W         | <p><b>Summary</b></p> <p>Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.</p> <table border="1"> <tr><td>Total On-Chip Power:</td><td>0.225 W</td></tr> <tr><td>Design Power Budget:</td><td>Not Specified</td></tr> <tr><td>Power Budget Margin:</td><td>N/A</td></tr> <tr><td>Junction Temperature:</td><td>27.6°C</td></tr> <tr><td>Thermal Margin:</td><td>57.4°C (4.8 W)</td></tr> <tr><td>Effective 8JA:</td><td>11.5°C/W</td></tr> <tr><td>Power supplied to off-chip devices:</td><td>0 W</td></tr> <tr><td>Confidence level:</td><td>Low</td></tr> </table> <p><a href="#">Launch Power Constraint Advisor</a> to find and fix invalid switching activity</p> <p><b>On-Chip Power</b></p> <table border="1"> <tr><td>Dynamic:</td><td>0.119 W (53%)</td></tr> <tr><td>Clocks:</td><td>0.026 W (22%)</td></tr> <tr><td>Signals:</td><td>0.015 W (13%)</td></tr> <tr><td>Logic:</td><td>0.013 W (11%)</td></tr> <tr><td>DSP:</td><td>0.040 W (34%)</td></tr> <tr><td>I/O:</td><td>0.024 W (20%)</td></tr> <tr><td>Device Static:</td><td>0.106 W (47%)</td></tr> </table> | Total On-Chip Power: | 0.225 W | Design Power Budget: | Not Specified | Power Budget Margin: | N/A | Junction Temperature: | 27.6°C | Thermal Margin: | 57.4°C (4.8 W) | Effective 8JA: | 11.5°C/W | Power supplied to off-chip devices: | 0 W | Confidence level: | Low | Dynamic: | 0.119 W (53%) | Clocks: | 0.026 W (22%) | Signals: | 0.015 W (13%) | Logic: | 0.013 W (11%) | DSP: | 0.040 W (34%) | I/O: | 0.024 W (20%) | Device Static: | 0.106 W (47%) |
| Total On-Chip Power:                | 0.225 W        |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Design Power Budget:                | Not Specified  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power Budget Margin:                | N/A            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Junction Temperature:               | 27.6°C         |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Thermal Margin:                     | 57.4°C (4.8 W) |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Effective 8JA:                      | 11.5°C/W       |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Power supplied to off-chip devices: | 0 W            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Confidence level:                   | Low            |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Dynamic:                            | 0.119 W (53%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Clocks:                             | 0.026 W (22%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Signals:                            | 0.015 W (13%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Logic:                              | 0.013 W (11%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| DSP:                                | 0.040 W (34%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| I/O:                                | 0.024 W (20%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |
| Device Static:                      | 0.106 W (47%)  |   |                      |         |                      |               |                      |     |                       |        |                 |                |                |          |                                     |     |                   |     |          |               |         |               |          |               |        |               |      |               |      |               |                |               |

### Timing:

| <u>Direct form</u>  | clk periods = 10ns, clk frequency = 100Mhz |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
|---|--|---|------|-------------|--------------------------------------|----------------------------------|--|--------------------------------------|----------------------------------|---|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
| <b>Design Timing Summary</b>  |  |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
| <table border="1"> <thead> <tr> <th>Setup</th> <th>Hold</th> <th>Pulse Width</th> </tr> </thead> <tbody> <tr> <td>Worst Negative Slack (WNS): 8.732 ns</td> <td>Worst Hold Slack (WHS): 0.152 ns</td> <td>Worst Pulse Width Slack (WPWS): 4.500 ns</td> </tr> <tr> <td>Total Negative Slack (TNS): 0.000 ns</td> <td>Total Hold Slack (THS): 0.000 ns</td> <td>Total Pulse Width Negative Slack (TPWS): 0.000 ns</td> </tr> <tr> <td>Number of Failing Endpoints: 0</td> <td>Number of Failing Endpoints: 0</td> <td>Number of Failing Endpoints: 0</td> </tr> <tr> <td>Total Number of Endpoints: 540</td> <td>Total Number of Endpoints: 540</td> <td>Total Number of Endpoints: 556</td> </tr> </tbody> </table> <p>All user specified timing constraints are met.</p> |  | Setup   | Hold | Pulse Width | Worst Negative Slack (WNS): 8.732 ns | Worst Hold Slack (WHS): 0.152 ns | Worst Pulse Width Slack (WPWS): 4.500 ns | Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): 0.000 ns | Total Pulse Width Negative Slack (TPWS): 0.000 ns | Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 | Number of Failing Endpoints: 0 | Total Number of Endpoints: 540 | Total Number of Endpoints: 540 | Total Number of Endpoints: 556 |
| Setup   | Hold                                       | Pulse Width                                       |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
| Worst Negative Slack (WNS): 8.732 ns  | Worst Hold Slack (WHS): 0.152 ns           | Worst Pulse Width Slack (WPWS): 4.500 ns          |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
| Total Negative Slack (TNS): 0.000 ns  | Total Hold Slack (THS): 0.000 ns           | Total Pulse Width Negative Slack (TPWS): 0.000 ns |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
| Number of Failing Endpoints: 0  | Number of Failing Endpoints: 0             | Number of Failing Endpoints: 0                    |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |
| Total Number of Endpoints: 540  | Total Number of Endpoints: 540             | Total Number of Endpoints: 556                    |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                |                                |                                |

| <u>Transposed form</u>               | clk periods = 3ns, clk frequency = 333.333Mhz   |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
|--------------------------------------|---|---|------|-------------|--------------------------------------|----------------------------------|--|--------------------------------------|----------------------------------|---|--------------------------------|--------------------------------|--------------------------------|---------------------------------|---------------------------------|---------------------------------|
| <b>Design Timing Summary</b>         |   |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
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| Setup                                | Hold  | Pulse Width                                       |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Worst Negative Slack (WNS): 0.412 ns | Worst Hold Slack (WHS): 0.152 ns  | Worst Pulse Width Slack (WPWS): 0.845 ns          |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): 0.000 ns  | Total Pulse Width Negative Slack (TPWS): 0.000 ns |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Number of Failing Endpoints: 0       | Number of Failing Endpoints: 0  | Number of Failing Endpoints: 0                    |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Total Number of Endpoints: 686       | Total Number of Endpoints: 686  | Total Number of Endpoints: 699                    |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| <u>Pipeline Direct form</u>          | clk periods = 8ns, clk frequency = 125Mhz   |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| <b>Design Timing Summary</b>         |   |   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
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| Setup                                | Hold  | Pulse Width                                       |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Worst Negative Slack (WNS): 0.448 ns | Worst Hold Slack (WHS): 0.083 ns  | Worst Pulse Width Slack (WPWS): 3.020 ns          |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Total Negative Slack (TNS): 0.000 ns | Total Hold Slack (THS): 0.000 ns  | Total Pulse Width Negative Slack (TPWS): 0.000 ns |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Number of Failing Endpoints: 0       | Number of Failing Endpoints: 0  | Number of Failing Endpoints: 0                    |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |
| Total Number of Endpoints: 1723      | Total Number of Endpoints: 1723   | Total Number of Endpoints: 1742                   |      |             |                                      |                                  |  |                                      |                                  |   |                                |                                |                                |                                 |                                 |                                 |

## Utilization:

| <u>Direct form</u>     | <table> <thead> <tr> <th>Name</th><th>Slice LUTs (53200)</th><th>Slice Registers (106400)</th><th>DSPs (220)</th><th>Bonded IOB (125)</th><th>BUFGCTRL (32)</th></tr> </thead> <tbody> <tr> <td>N fir</td><td>313</td><td>555</td><td>35</td><td>37</td><td>1</td></tr> </tbody> </table> <p><b>Summary</b></p> <table> <thead> <tr> <th>Resource</th><th>Utilization</th><th>Available</th><th>Utilization %</th></tr> </thead> <tbody> <tr> <td>LUT</td><td>313</td><td>53200</td><td>0.59</td></tr> <tr> <td>FF</td><td>555</td><td>106400</td><td>0.52</td></tr> <tr> <td>DSP</td><td>35</td><td>220</td><td>15.91</td></tr> <tr> <td>IO</td><td>37</td><td>125</td><td>29.60</td></tr> </tbody> </table> <p>Utilization (%)</p>                                      | Name                     | Slice LUTs (53200) | Slice Registers (106400) | DSPs (220)    | Bonded IOB (125) | BUFGCTRL (32) | N fir       | 313 | 555 | 35 | 37 | 1 | Resource | Utilization | Available | Utilization % | LUT | 313 | 53200 | 0.59 | FF | 555 | 106400 | 0.52 | DSP | 35 | 220 | 15.91 | IO | 37 | 125 | 29.60 |
|------------------------|---|--------------------------|--------------------|--------------------------|---------------|------------------|---------------|-------------|-----|-----|----|----|---|----------|-------------|-----------|---------------|-----|-----|-------|------|----|-----|--------|------|-----|----|-----|-------|----|----|-----|-------|
| Name                   | Slice LUTs (53200)  | Slice Registers (106400) | DSPs (220)         | Bonded IOB (125)         | BUFGCTRL (32) |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| N fir                  | 313   | 555                      | 35                 | 37                       | 1             |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| Resource               | Utilization   | Available                | Utilization %      |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| LUT                    | 313   | 53200                    | 0.59               |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| FF                     | 555   | 106400                   | 0.52               |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| DSP                    | 35  | 220                      | 15.91              |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| IO                     | 37  | 125                      | 29.60              |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
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| Name                   | Slice LUTs (53200)  | Slice Registers (106400) | DSPs (220)         | Bonded IOB (125)         | BUFGCTRL (32) |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| N fir_trans            | 666   | 698                      | 18                 | 37                       | 1             |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| Resource               | Utilization   | Available                | Utilization %      |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| LUT                    | 666   | 53200                    | 1.25               |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| FF                     | 698   | 106400                   | 0.66               |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| DSP                    | 18  | 220                      | 8.18               |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |
| IO                     | 37  | 125                      | 29.60              |                          |               |                  |               |             |     |     |    |    |   |          |             |           |               |     |     |       |      |    |     |        |      |     |    |     |       |    |    |     |       |

| Name  | <sup>1</sup> | Slice LUTs<br>(53200) | Slice Registers<br>(106400) | DSPs<br>(220) | Bonded IOB<br>(125) | BUFGCTRL<br>(32) |     |    |        |    |    |    |     |     |    |     |
|---|--------------|-----------------------|-----------------------------|---------------|---------------------|------------------|-----|----|--------|----|----|----|-----|-----|----|-----|
| N fir_pipe  |              | 711                   | 1730                        | 35            | 37                  | 1                |     |    |        |    |    |    |     |     |    |     |
| <b>Summary</b>  |              |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| Resource  | Utilization  | Available             | Utilization %               |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| LUT   | 711          | 53200                 | 1.34                        |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| LUTRAM  | 30           | 17400                 | 0.17                        |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| FF  | 1730         | 106400                | 1.63                        |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| DSP   | 35           | 220                   | 15.91                       |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| IO  | 37           | 125                   | 29.60                       |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| <table> <tr> <td>LUT</td> <td>1%</td> </tr> <tr> <td>LUTRAM</td> <td>1%</td> </tr> <tr> <td>FF</td> <td>2%</td> </tr> <tr> <td>DSP</td> <td>16%</td> </tr> <tr> <td>IO</td> <td>30%</td> </tr> </table> |              |                       |                             |               |                     |                  | LUT | 1% | LUTRAM | 1% | FF | 2% | DSP | 16% | IO | 30% |
| LUT   | 1%           |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| LUTRAM  | 1%           |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| FF  | 2%           |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| DSP   | 16%          |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |
| IO  | 30%          |                       |                             |               |                     |                  |     |    |        |    |    |    |     |     |    |     |

Conclusion:

|             | Direct form                                  | Transposed form                                 | Pipeline direct form                        |
|-------------|--|---|---|
| Timing      | clk periods = 10ns<br>clk frequency = 100Mhz | clk periods = 3ns<br>clk frequency = 333.333Mhz | clk periods = 8ns<br>clk frequency = 125Mhz |
| Power       | 0.182W                                       | 0.322W  | 0.225W                                      |
| Utilization | LUT:313<br>FF:555<br>DSP:35<br>IO:37         | LUT:666<br>FF:698<br>DSP:18<br>IO:37            | LUT:711<br>FF:1730<br>DSP:35<br>IO:37       |

Direct form 的 clk period 為最長代表他在同個時間週期處理的時間最久，符合 critical time 為最長的結論 Pipeline direct form 也有效縮短 clk periods，另外 power 部分，因為 transposed form 的 clk freq 為最大，power 的公式也跟 freq 有關，因此他 power 為最大。

Pipeline direct form 在 LUT 和 FF 的使用上都顯示出最高的利用率，這表示它能夠提供更加強大和靈活的處理能力。然而，power 以及 Area 也有可能最大。

綜合以上，Transposed form 在 clk periods 上表現最好，但以較高的功耗和較高的 LUT 及 FF 資源利用率為代價。

Direct form 在功耗上最為優化，但 clk periods 最長，處理速度可能較慢。

Pipeline direct form 在資源利用率上最高，但是 clk period 並沒有降到預期得 3ns，這部分我猜可能是 vivado 硬體乘加器的限制，導致我的 pipeline 合成並沒有達到預期的只有一組乘加器，但是可以確定的是，我在模擬波形時，有確實達到預期的 critical path 等於一組乘加器的結果。

## Run Code

如果助教需要跑我的 code，以下是我的流程。

### Software:

首先先讓 C++ code 產生 random data。

```
● ubuntu@ubuntu2004:~/dspic_final_submit/dsp_final$ g++ hw4.cpp -o dspic.exe
● ubuntu@ubuntu2004:~/dspic_final_submit/dsp_final$ ./dspic.exe
Average power = 1
```

且此 data 會自動存在下面路徑上

/dspic\_final\_submit/dsp\_final/data/HW\_input.txt

/dspic\_final\_submit/dsp\_final/data/HW\_golden.txt

提供硬體相對應的資料去做比對。

如下圖擷取 testbench 使用的絕對路徑所示：

```
initial begin
    rst_n = 1'b0;
    f_data = $fopen("/home/ubuntu/dspic_final_submit/dsp_final/data/HW_input.txt","r");
    f_golden = $fopen("/home/ubuntu/dspic_final_submit/dsp_final/data/HW_golden.txt", "r");
    #100;
    rst_n = 1'b1;
```

### Hardware:

我的 testbench 分別寫了三份

| pipeline   | Direct form  | Transposed form  |
|--|--|--|
| <pre>5 module fir_pipe_tb; 6     parameter inWL = 15; 7     parameter macWL = 20; 8     parameter Data_Num =500; 9 10    reg signed [inWL-1:0] in; 11    reg signed [inWL-1:0] tap; 12    wire signed [macWL-1:0] out; 13    reg clk; 14    reg rst_n; 15 16 17    fir_pipe U0( 18        .clk(clk), 19        .rst_n(rst_n), 20        .data_in(in), 21        .data_out(out) 22    ); 23</pre> | <pre>1 `timescale 1ns / 1ps 2 //direct form 3 module fir_tb; 4     parameter inWL = 15; 5     parameter macWL = 20; 6     parameter Data_Num =500; 7 8     reg signed [inWL-1:0] in; 9     reg signed [inWL-1:0] tap; 10    wire signed [macWL-1:0] out; 11    reg clk; 12    reg rst_n; 13    //this is for test direct form module 14 15    fir U0( 16        .clk(clk), 17        .rst_n(rst_n), 18        .data_in(in), 19        .data_out(out) 20    ); 21</pre> | <pre>1 `timescale 1ns / 1ps 2 //transposed form tb 3 4 module fir_trans_tb; 5     parameter inWL = 15; 6     parameter macWL = 20; 7     parameter Data_Num =500; 8 9     reg signed [inWL-1:0] in; 10    reg signed [inWL-1:0] tap; 11    wire signed [macWL-1:0] out; 12    reg clk; 13    reg rst_n; 14 15    //this is for test transposed form module 16 17    fir_trans U0( 18        .clk(clk), 19        .rst_n(rst_n), 20        .data_in(in), 21        .data_out(out) 22    ); 23</pre> |

且需要把相對應的 module 從此檔案

/dspic\_final\_submit/dsp\_final/fir/include.rtl.list.xsim

Uncomment 想要測試的電路即可。

```
1 module fir_pipe_tb;
2     parameter inWL = 15;
3     parameter macWL = 20;
4     parameter Data_Num =500;
5
6     reg signed [inWL-1:0] in;
7     reg signed [inWL-1:0] tap;
8     wire signed [macWL-1:0] out;
9     reg clk;
10    reg rst_n;
11
12
13    fir_pipe U0(
14        .clk(clk),
15        .rst_n(rst_n),
16        .data_in(in),
17        .data_out(out)
18    );
19
```

```

1 #firpipe:
2     #rm -rf xsim.dir/ *.log *.pb *.jou *.wdb
3     #xvlog -f ./include.rtl.list.xsim ./tb/fir_pipe_tb.v
4     #xelab -top fir_pipe_tb -snapshot fir_pipe_tb_elab
5     #xsim fir_pipe_tb_elab -R
6
7
8 #fir:
9     #rm -rf xsim.dir/ *.log *.pb *.jou *.wdb
10    #xvlog -f ./include.rtl.list.xsim ./tb/fir_pipe_tb.v
11    #xelab -top fir_pipe_tb -snapshot fir_pipe_tb_elab
12    #xsim fir_pipe_tb_elab -R
13
14 firtrans:
15     rm -rf xsim.dir/ *.log *.pb *.jou *.wdb
16     xvlog -f ./include.rtl.list.xsim ./tb/fir_trans_tb.v
17     xelab -top fir_trans_tb -snapshot fir_trans_tb_elab
18     xsim fir_trans_tb_elab -R
19
20
21 clean:
22     rm -rf xsim.dir/ *.log *.pb *.jou *.wdb
23
24

```

另外我寫一份 makefile 路徑：[/dspic\\_final\\_submit/dsp\\_final/fir/Makefile](#)

分別方便測試三個電路，但是再測一個電路時，需要把另外兩個給 comment 掉

如上圖所示，如果需要測試 transposed form，需要把圈起來部分 comment 掉

最後在 [dspic\\_final\\_submit /dsp\\_final/fir/](#)

分別打上相對應電路的 comment

| Direct form | Transposed form | Pipeline direct form |
|-------------|-----------------|----------------------|
| make fir    | make firtrans   | make firpipe         |

即可模擬

```

$ ubuntu@ubuntu2004:~/dspic_final_submit/dsp_final/fir$ make firpipe
rm -rf xsim.dir/ *.log *.pb *.jou *.wdb
xvlog -f ./include.rtl.list.xsim ./tb/fir_pipe_tb.v
INFO: [VRFC 10-2263] Analyzing Verilog file "/home/ubuntu/dspic_final_submit/dsp_final/fir/rtl/fir_direct_pipe.v" into library work
INFO: [VRFC 10-311] analyzing module fir_pipe
INFO: [VRFC 10-2263] Analyzing Verilog file "/home/ubuntu/dspic_final_submit/dsp_final/fir/tb/fir_pipe_tb.v" into library work
INFO: [VRFC 10-311] analyzing module fir_pipe_tb

```

如果成功會輸出下圖：

這是 pipeline direct form 的從 C++ 產生隨機一組信號的模擬結果

```
[PASS][Pattern 490]61278=61278
[PASS][Pattern 491]139707=139707
[PASS][Pattern 492]15622=15622
[PASS][Pattern 493]-185205=-185205
[PASS][Pattern 494]-271306=-271306
[PASS][Pattern 495]-194989=-194989
[PASS][Pattern 496]-68585=-68585
[PASS][Pattern 497]27954=27954
[PASS][Pattern 498]137117=137117
[PASS][Pattern 499]264440=264440
All answers match golden
$finish called at time : 5375 ns : File "/home/ubuntu/dspic_final_submit/dsp_final/fir_tb/fir_tb.v" Line 87
exit
INFO: [Common 17-206] Exiting xsim at Sun Jan  7 12:16:21 2024...
ubuntu@ubuntu2004:~/dspic_final_submit/dsp_final/fir$
```