gmZPU SoC Datasheet

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1 Introduction

The gmZPU System-on-Chip (SoC) combines the zpu zealot medium core [2] with two WISHBONE B4 [1] buses. One of the WISHBONE buses connects internal devices to the zpu. The other WISHBONE bus is exported for external devices. Figure 1 shows the top-level block diagram of the gmZPU SoC.

The zpu data bus is 32 bits wide. The address bus is 18 bits wide. The Memory Management Unit (MMU) decodes the 18-bit address into chip-select and reduced address bus for the main components of the SoC interconnect fabric:

- RAM
- phiIO basic zpu I/O
- WISHBONE controller 0 (WB0)
- WISHBONE controller 1 (WB1)

2 Notation

BUS(1:0) Bit 1 downto 0 of bus BUS.

3 Memory map

The 8 most significant bits of the zpu address bus select one of the core components linked directly to the zpu. Table 1 shows how these bits are decoded.

Table 1: Address decoding

17	16	15	14	13	12	11	10	chip select
0	X	X	X	X	X	X	X	RAM
1	0	X	X	X	X	X	X	phiIO
1	1	0	X	X	X	X	X	WB0 control
1	1	1	0	0	0	0	X	WB0 slave 0
1	1	1	0	0	0	1	X	WB0 slave 1

Each core component has a specific address bus width. Table 2 shows the base address of each of the core components shown in 1. Along with the base address is the size of the address bus to that device.

Table 2: Address map and sizes

Device	Base	Size	Bytes
RAM	0x00000	0x20000	128k
phIO	0x20000	0x10000	64k
WB0 control	0x30000	0x08000	32K
WB0 slave 0	0x38000	0x00800	2K
WB0 slave 1	0x38800	0x00800	2k

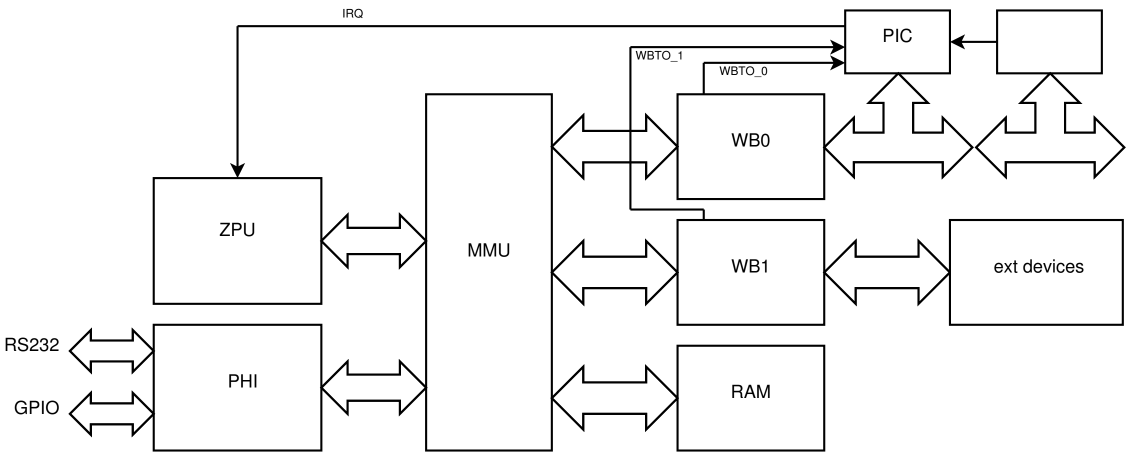

Figure 1: Block diagram

4 Internal devices

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4.1 Programmable Interrupt Controller (PIC)

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References

[1] OpenCores *Wishbone B4, WISHBONE System-on-Chip (SoC)Interconnection Architecture for Portable IP Cores* `http://opencores.org/opencores,wishbone` 2010.

[2] Zylin Consulting *Zylin ZPU* `http://opensource.zylin.com/zpu.htm`.

[3] Sonologic *gmzpu github repository* `http://github.com/sonologic/gmzpu`.