Interrupt Controller Datasheet

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1 Introduction

The Sonologic Programmable Interrupt Controller is a WISHBONE B4 [1] compliant interrupt controller. The interrupt controller is a WISHBONE slave device. It offers a variable amount of interrupt banks. Each bank has three configuration registers and one status register. An interrupt bank contains a variable amount of interrupt lines. Interrupt lines can trigger on the rising edge, falling edge and level. Interrupt lines can be individually masked.

2 Notation

BUS(1:0) Bit 1 downto 0 of bus BUS.

3 Design units

The top design unit is *interrupt_controller*. Figure 1 contains the block diagram of the *interrupt_controller* design unit.

The *interrupt_controller* can have a variable amount of register banks. The register bank is described in design unit *interrupt_regs*. A register bank implements four registers:

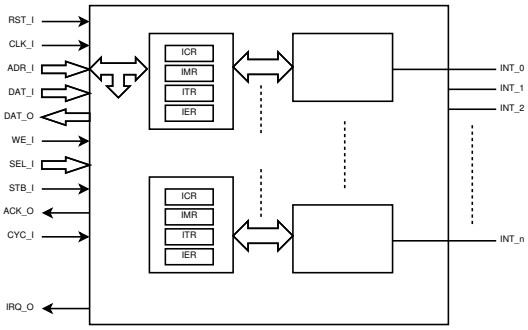

Figure 1: Block diagram

ICR Interrupt Cause Register

IMR Interrupt Mask Register

ITR Interrupt Type Register

IER Interrupt Edge Register

The width of registers is variable. Each of the bits in the four registers are connected to an instantiation of the *interrupt_line* design unit. Figure 2 shows the functional diagram of the *interrupt_line* design unit.

3.1 Design constraints

The address bus (ADR_I) must be able to address each register in each register bank. Each register bank occupies 4 words. The

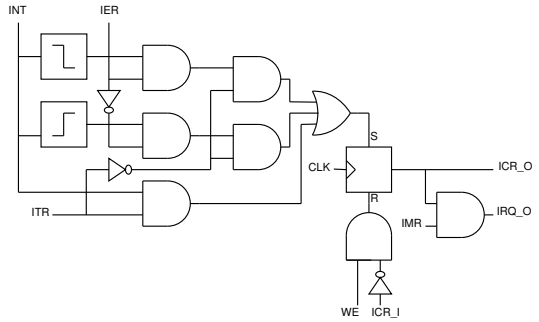

Figure 2: Functional diagram interrupt line

two least significant bits of the address bus address each of the 4 registers. The minimum length of the address bus is two bits when the design has only one register bank.

For additional register banks the bits down to the third least significant bit select the the register bank. To address N_BANKS register banks the

4 Application

The reference design uses the gmzpu [2] cpu with the zwishbone controller. The reference application of the design entity has a data width of 32 bits and an address width of 16 bits. One interrupt bank (of 32 interrupt lines) is used.

References

[1] OpenCores *Wishbone B4, WISHBONE System-on-Chip (SoC)Interconnection Architecture for Portable IP Cores* `http://opencores.org/opencores,wishbone` 2010.

[2] Sonologic *gmzpu github repository* `http://github.com/sonologic/gmzpu`.