TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Define computer architecture. Discuss the limitations of using single bus system to connect different devices. What does width of address bus represent in a system? [2+2+2]
2. Design an 2-bit ALU that can perform subtraction, AND, OR and XOR. [8]
3. Write a code for Y=(A+B)/C + D/(E*F) using three address, two address, one address and zero address instruction format. [8]
4. Differentiate hardwired and micro-programmed control unit. Draw and explain block diagram of micro-programmed sequencer for control memory. [10]
5. Derive expression showing speed up ratio equals number of segments in pipeline. Discuss in detail about data dependency problem that arises in pipelining along with its solution. [3+5]
6. Write an algorithm for non restoring division. Perform the 10/3 using restoring division algorithm. [3+7]
7. Multiply -6×-11 using Booths Multiplication algorithm. [6]
8. Write characteristics of memory system? Suppose main memory has 64 blocks and cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [4+6]
9. Explain three reasons behind the requirement of I/O interfaces. Why memory address spaces are reduced memory mapped I/O ? Describe DMA controller with suitable block diagram. [3+2+5]
10. Explain inter-processor synchronization with example. [4]

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