TRIBHUVAN UNIVERSITY
INSTITUTE OF ENGINEERING
Examination Control Division
2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture *(CT 603)*

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ *Attempt **All** questions.*
- ✓ *The figures in the margin indicate **Full Marks**.*
- ✓ *Assume suitable data if necessary.*

1. Draw the instruction cycle state diagram with example. [6]
2. Write down the code to evaluate Y = (A - B/C)*[D + (E*G)] in three address, two address, one address and zero address instruction formats. [8]
3. Define addressing modes. Mention the different types of addressing modes and comparison between them. [2+6]
4. How address of micro instruction is generated by next address generator in control unit? Explain with suitable diagram. [8]
5. Explain four stage instruction pipeline and also draw a time-space diagram for four segments having six tasks. [10]
6. Explain the Booth's algorithm for multiplication. Multiply 10 × (-5) using Booth's multiplication algorithm. [5+5]
7. Comparison between restoring and non-restoring division algorithms with example. [6]
8. Define cache mapping techniques. Explain direct mapping technique with suitable diagram. Why replacement algorithm is necessary in associative mapping? Justify. [2+4+4]
9. Comparison between program I10, Interrupt driven I10 and direct memory access. Why data communication processor is required in an I10 organization. [8+2]
10. Discuss about hypercube interconnection network with example. [4]

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