SKEWED CMOS INVERTER

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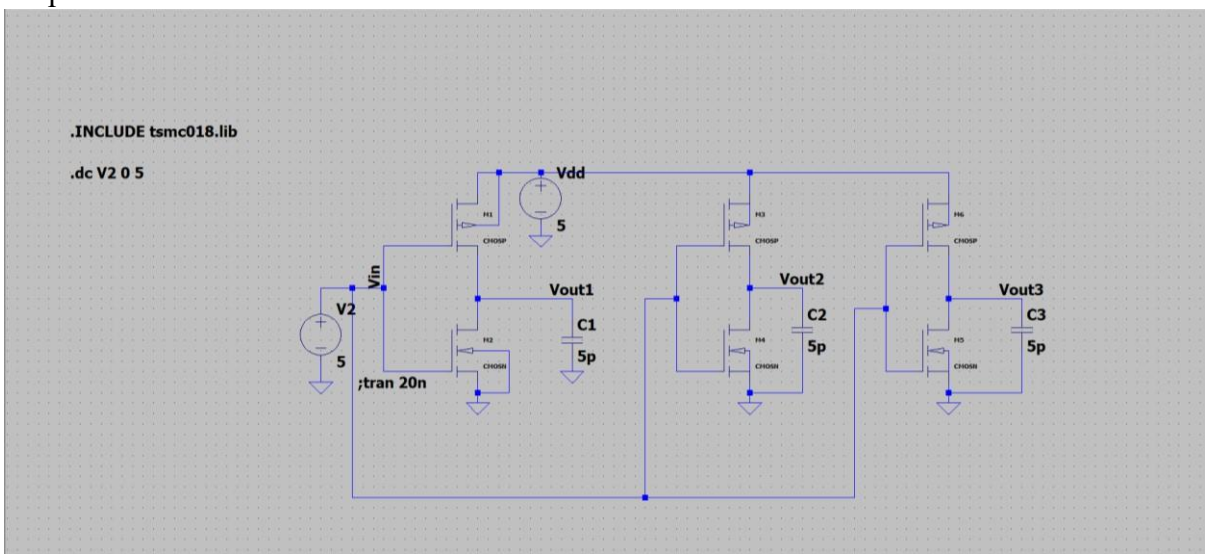
Part i.

The voltage transfer characteristics of a CMOS inverter represent the relationship between the input voltage(Vin) and output voltage(Vout) of the inverter. In a CMOS inverter, the transfer characteristics have a unique S-shape curve with a sharp transition from logic high to logic low states. When the input voltage is lower than the threshold voltage of the MOSFETs, the output voltage remains high, and when the input voltage is higher than the threshold voltage, the output voltage switches to low. For an equal rise time and fall time delay, the transition between high and low states occurs at the midpoint of the input voltage range. Additionally, the gain of a CMOS inverter is very high, and the output voltage swing is nearly equal to the supply voltage. Therefore, a CMOS inverter is an ideal component for digital logic circuits, as it provides fast and reliable logic level conversion.

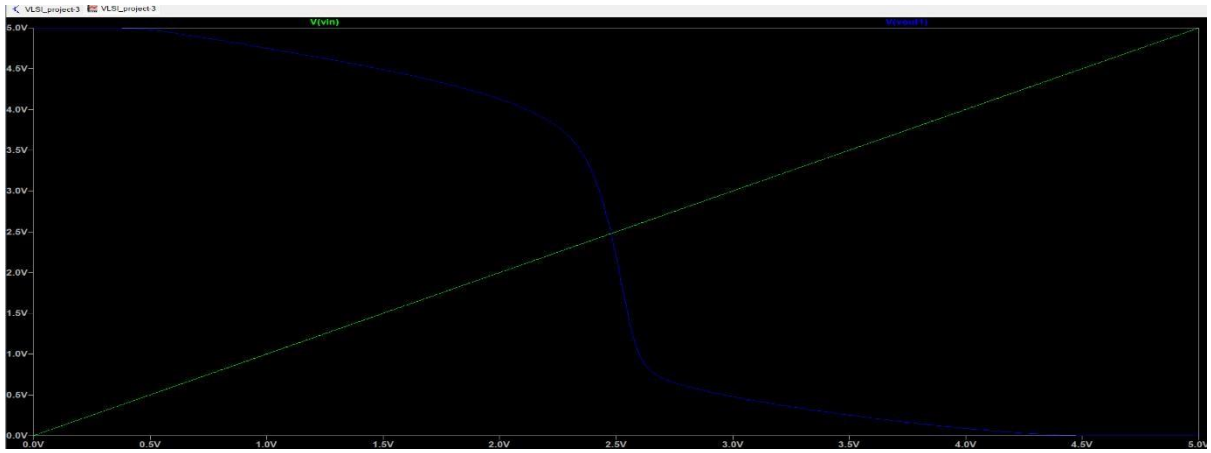
We have simulated a CMOS inverter with channel length L=180nm for both NMOS and PMOS, and NMOS channel width W=400nm, while PMOS channel width W=800nm(to maintain equal risetime and fall time delays).

LTspice schematic file: a1.asc and a2.asc



The above circuit have been simulated, and following results are obtained:

Plot:



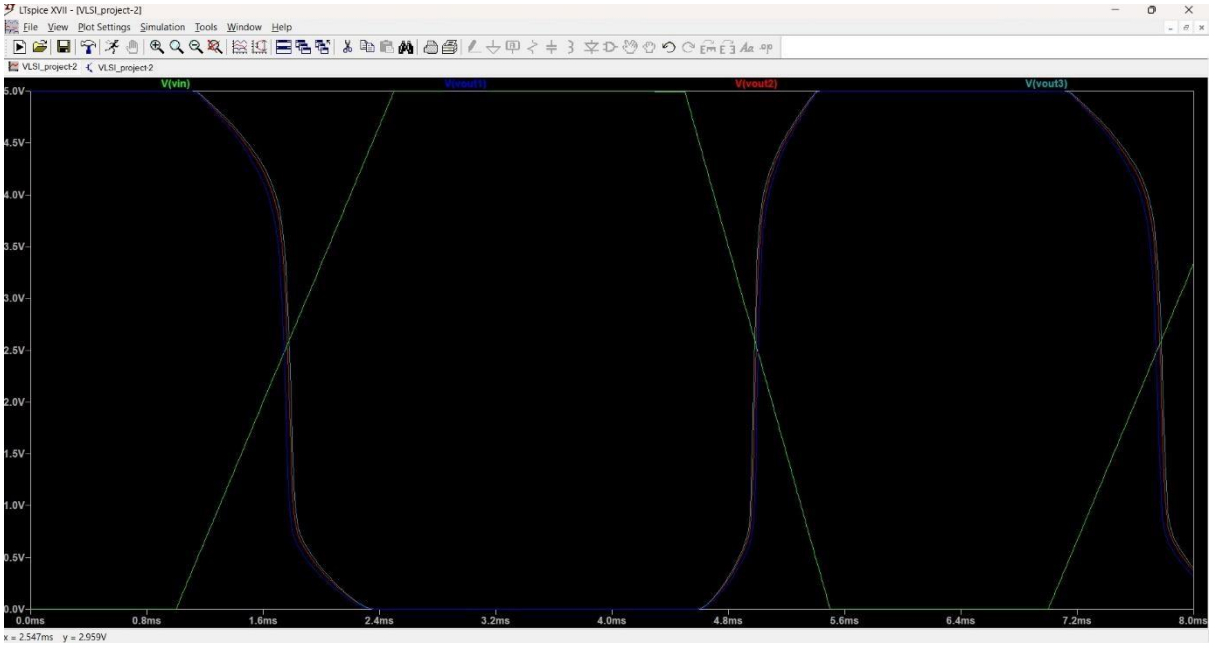
Part ii.

Transient analysis of a CMOS inverter involves the study of how the output voltage changes in response to changes in the input voltage. During transient analysis, LTSpice simulates the circuit's behavior over a specific period, typically a few nanoseconds, by solving the differential equations that govern the MOSFET behavior. The analysis is typically performed by applying a step function or a pulse input to the input of the inverter and observing the resulting output waveform. The analysis takes into account the capacitive and resistive effects of the circuit elements, which affect the rise time, fall time, propagation delay, and settling time of the output waveform. The transient analysis of a CMOS inverter is essential for understanding the circuit's performance and ensuring that it meets the design specifications for a particular application. By analyzing the transient response, designers can optimize the inverter's performance, improve its switching speed, and minimize its power consumption.

LTspice schematic file: b.asc Simulation

results:

Plot:



Observations:

As we increase the sizing factor(S=1,2,4), we can observe that there is a parallel shift in the output transient voltage waveform.

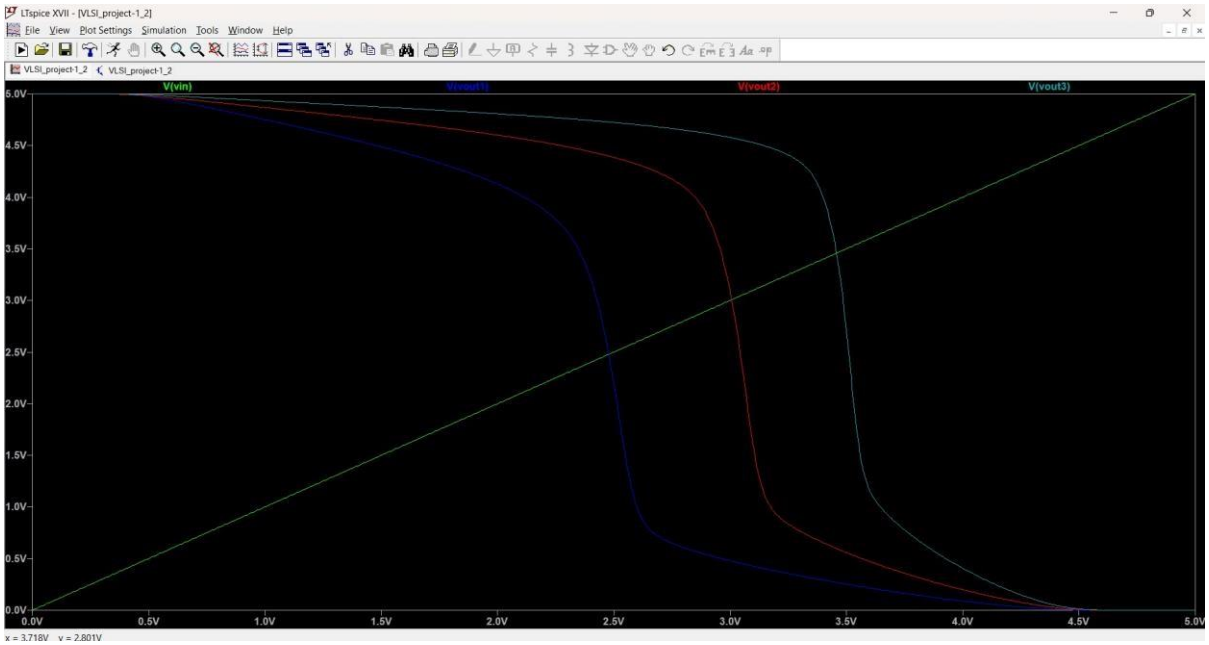
Part iii.

When simulating the voltage transfer characteristics of a CMOS inverter, varying the width of the NMOS and PMOS transistors can have a significant impact on the circuit's performance.

When the NMOS width is kept constant and the PMOS width is scaled by a factor of S=1, 2, or 4, the VTC curve shifts along the input voltage axis. Specifically, the transition threshold voltage decreases as the PMOS width increases, resulting in a steeper slope of the VTC curve. This leads to an increase in the inverter's gain and a decrease in the propagation delay.

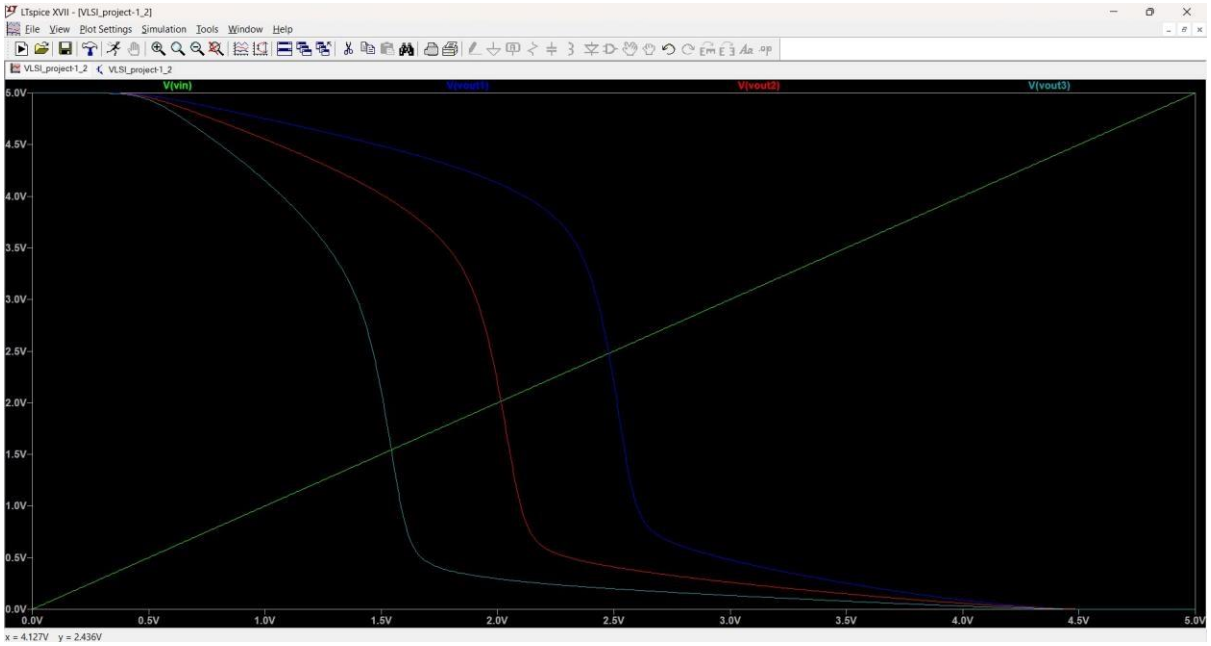
LTspice schematic file: c1.asc and c2.asc

Voltage Transfer Characteristics(VTC) plot:



When the PMOS width is kept constant and the NMOS width is scaled by S=1, 2, or 4, the VTC curve shifts along the output voltage axis. Specifically, the transition threshold voltage increases as the NMOS width increases, leading to a flatter slope of the VTC curve. This results in a decrease in the inverter's gain and an increase in the propagation delay.

VTC plot:

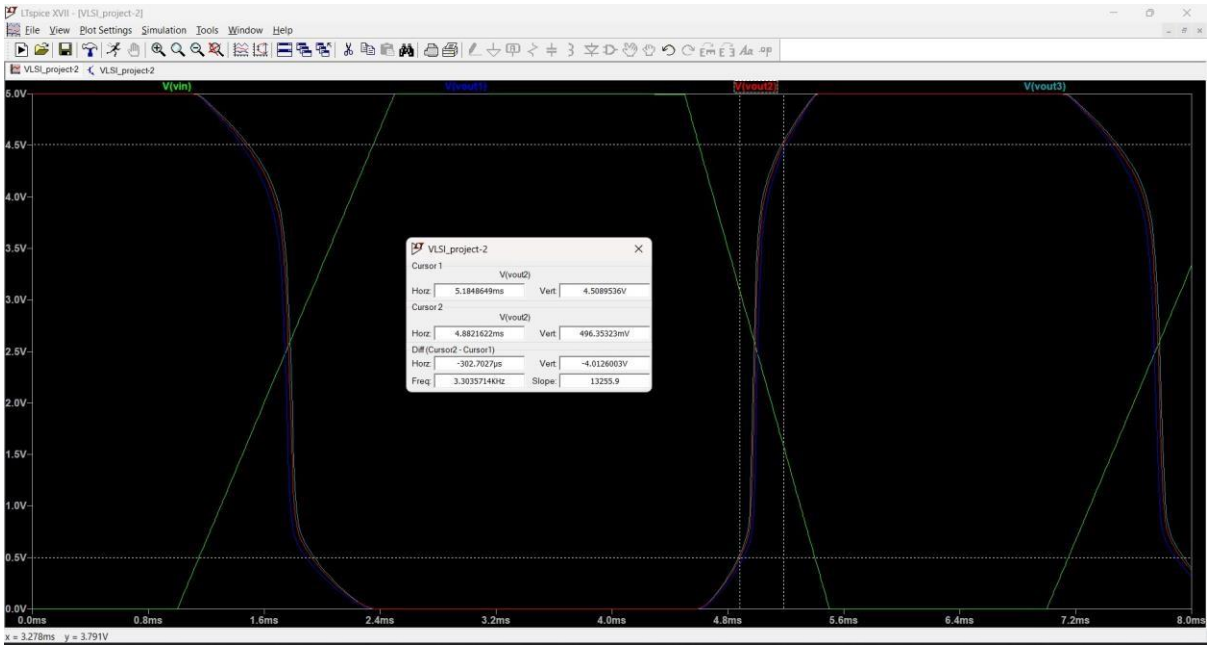


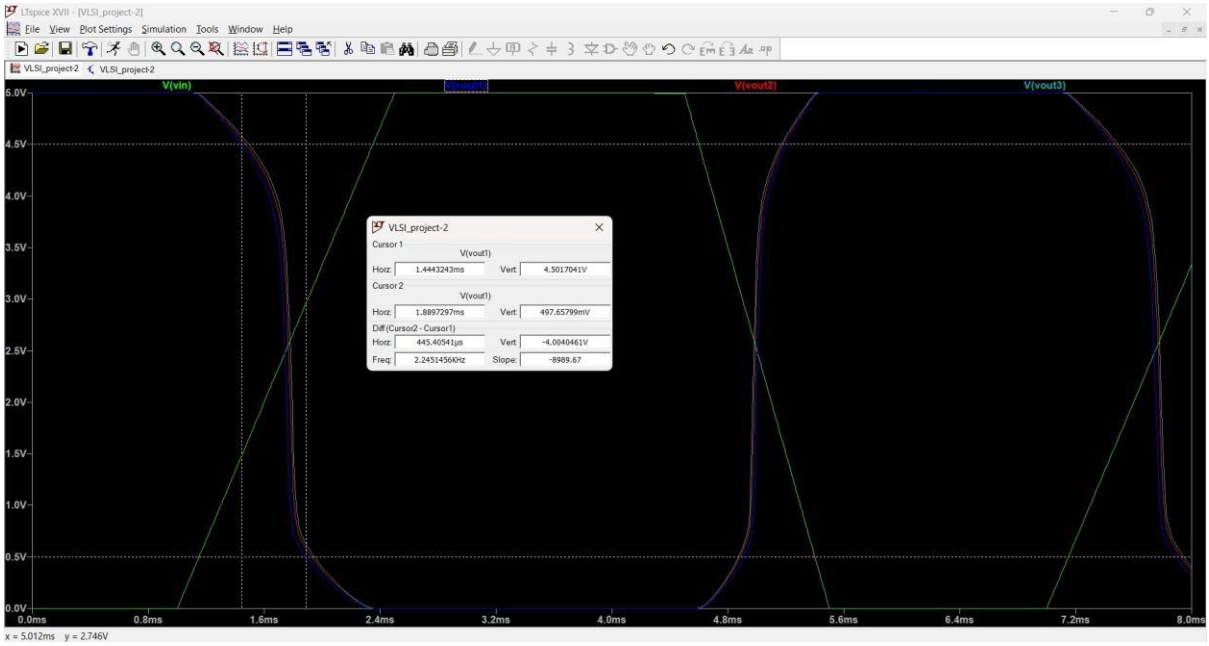
Part iv.

The rise time and fall time of the output voltage waveform are important parameters that affect the performance of the inverter. The rise time is the time taken for the output voltage to change from 10% of Vout(max.) to 90% of Vout(max.), while the fall time is the time taken for the output voltage to change from 90% of Vout(max.) to 10% of Vout(max.).

When there is no external load capacitance, the rise and fall times of the output voltage waveform are relatively short, as there is less capacitance to charge and discharge. However, when there is an external load capacitance of 5pF, the rise and fall times of the output voltage waveform increase significantly due to the additional capacitance that must be charged and discharged. This increase in rise and fall time can cause a delay in the switching of the output voltage and affect the inverter's overall performance.

LTspice schematic file: d.asc





Observations:

** When there is NO external load capacitance, Rise time=Fall time=0.44ms.

** When there is an external load capacitance of 5pF, Rise time=Fall time=0.25ms.

**** Along with this document, we are submitting the LTspice schematic,tsmc 180nm CMOS transistors, and the result waveforms.**

**** To run the LTspice schematic, copy the tsmc transistor component files into LTspiceXVII>>lib>>sym directory.**

**** In the schematic, set the DC sweep to linear for VTC simulation, transient for rise time-fall time analysis, and pulsating input for multi-size(S=1,2,4) CMOS inverters.**