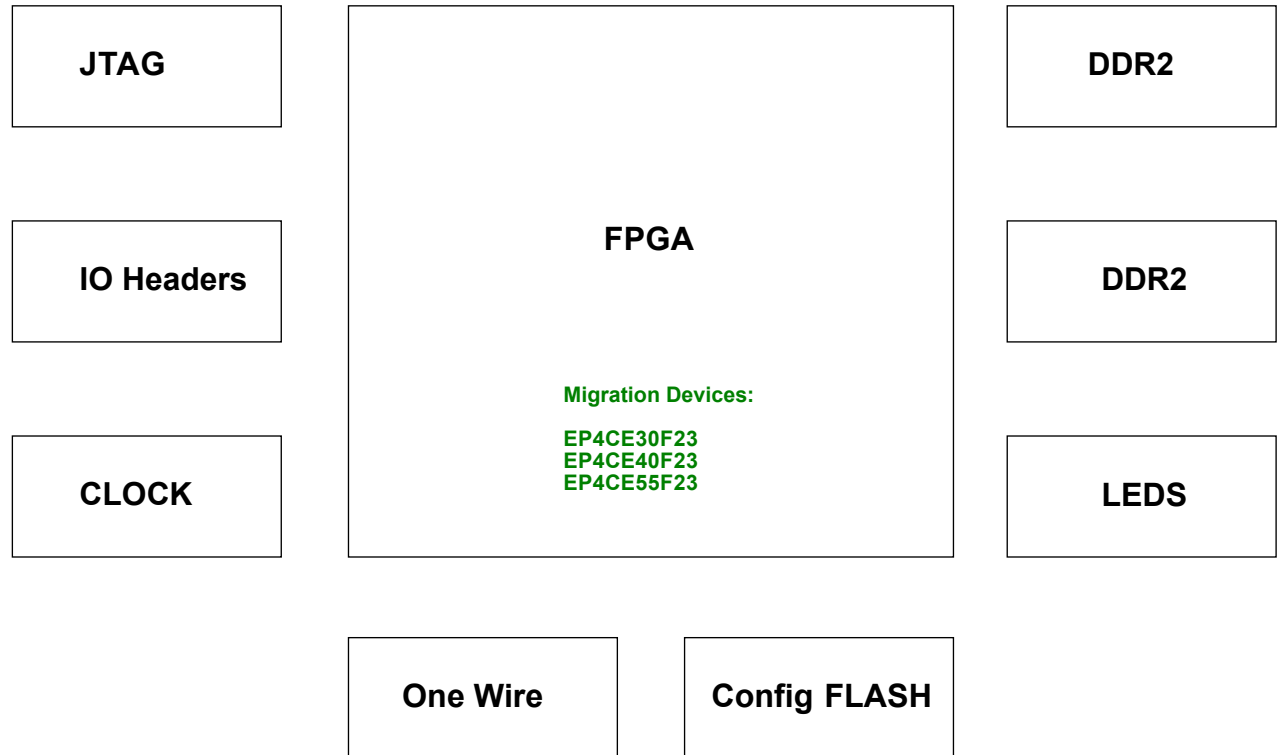


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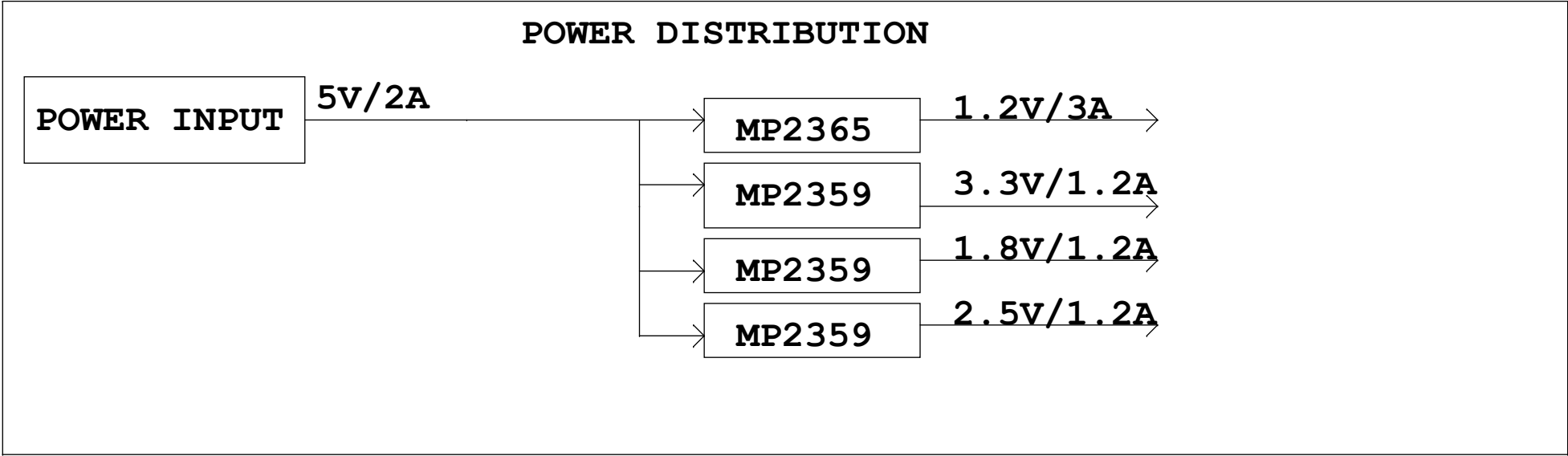
PAGE01: BLOCK DIAGRAM
PAGE02: POWER DISTRIBUTION
PAGE03: DDR2 L BANK
PAGE04: DDR2 U BANK
PAGE05: FPGA BANK 1 AND 2
PAGE06: FPGA BANK 3 AND 4
PAGE07: FPGA BANK 5 AND 6
PAGE08: FPGA BANK 7 AND 8
PAGE09: FPGA CLOCK AND VREF
PAGE10: FPGA CONFIG
PAGE11: FPGA POWER
PAGE12: System Power Supply
PAGE13: Connectors ANG One Wire

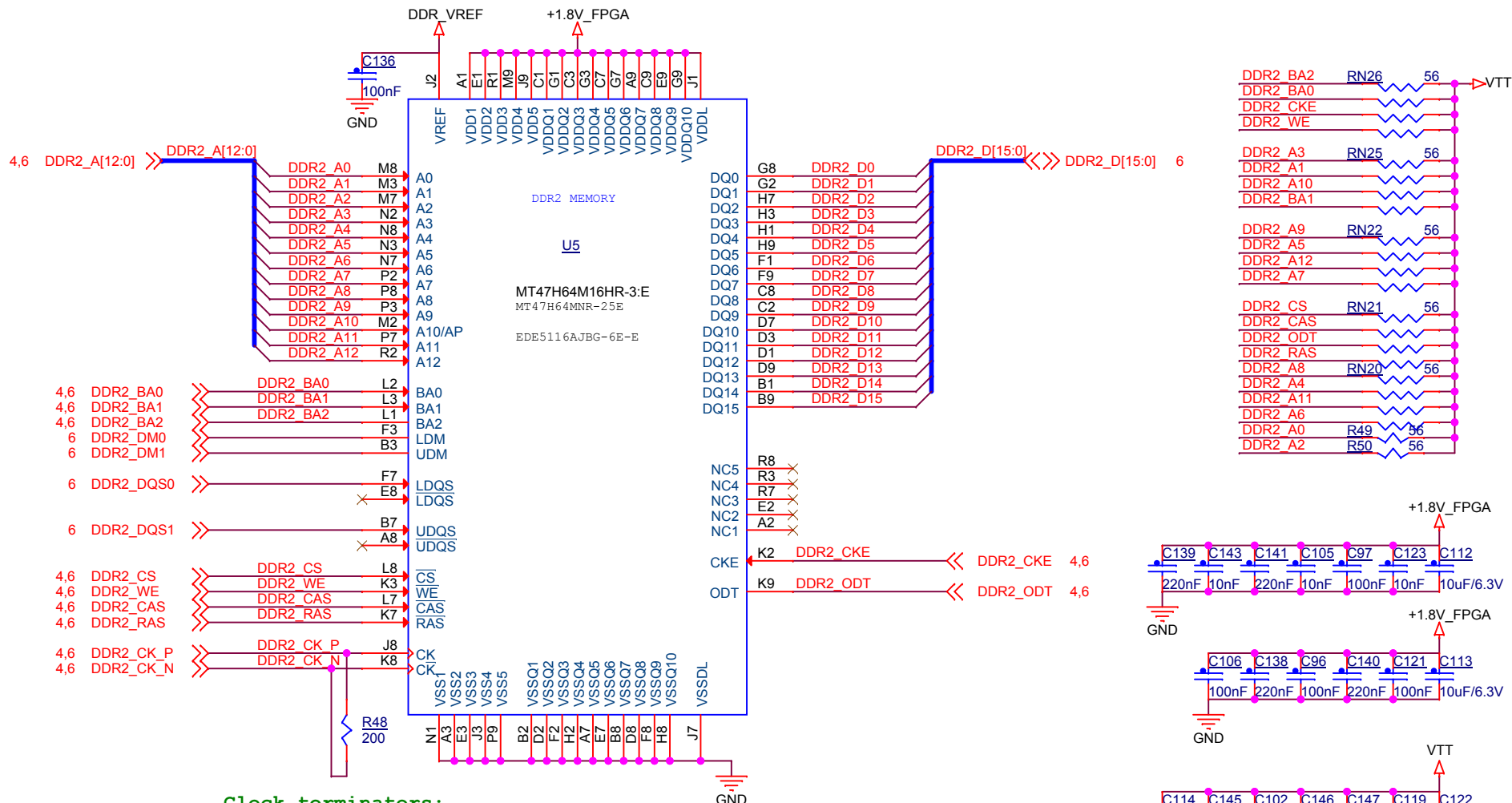
BLOCK DIAGRAM



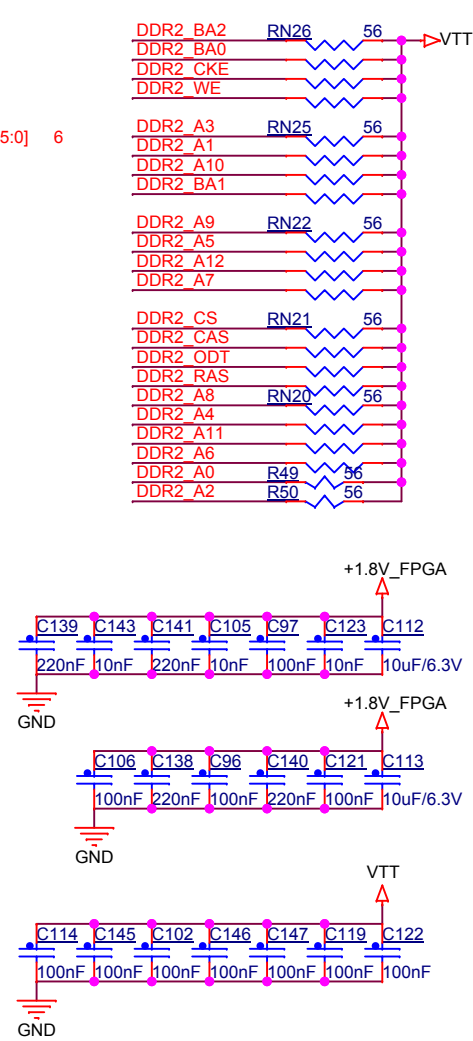
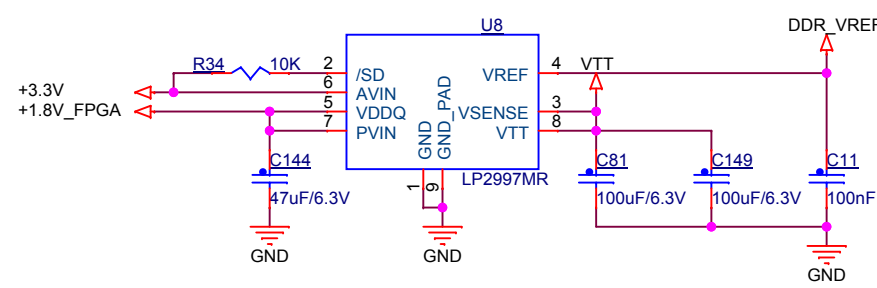
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Title		ALTERA Cyclone IV FPGA Core	
Size	Document	Number	Rev
A3	Block Diagram		V1.1
Date:	Friday, September 04, 2015		Sheet 1 of 13

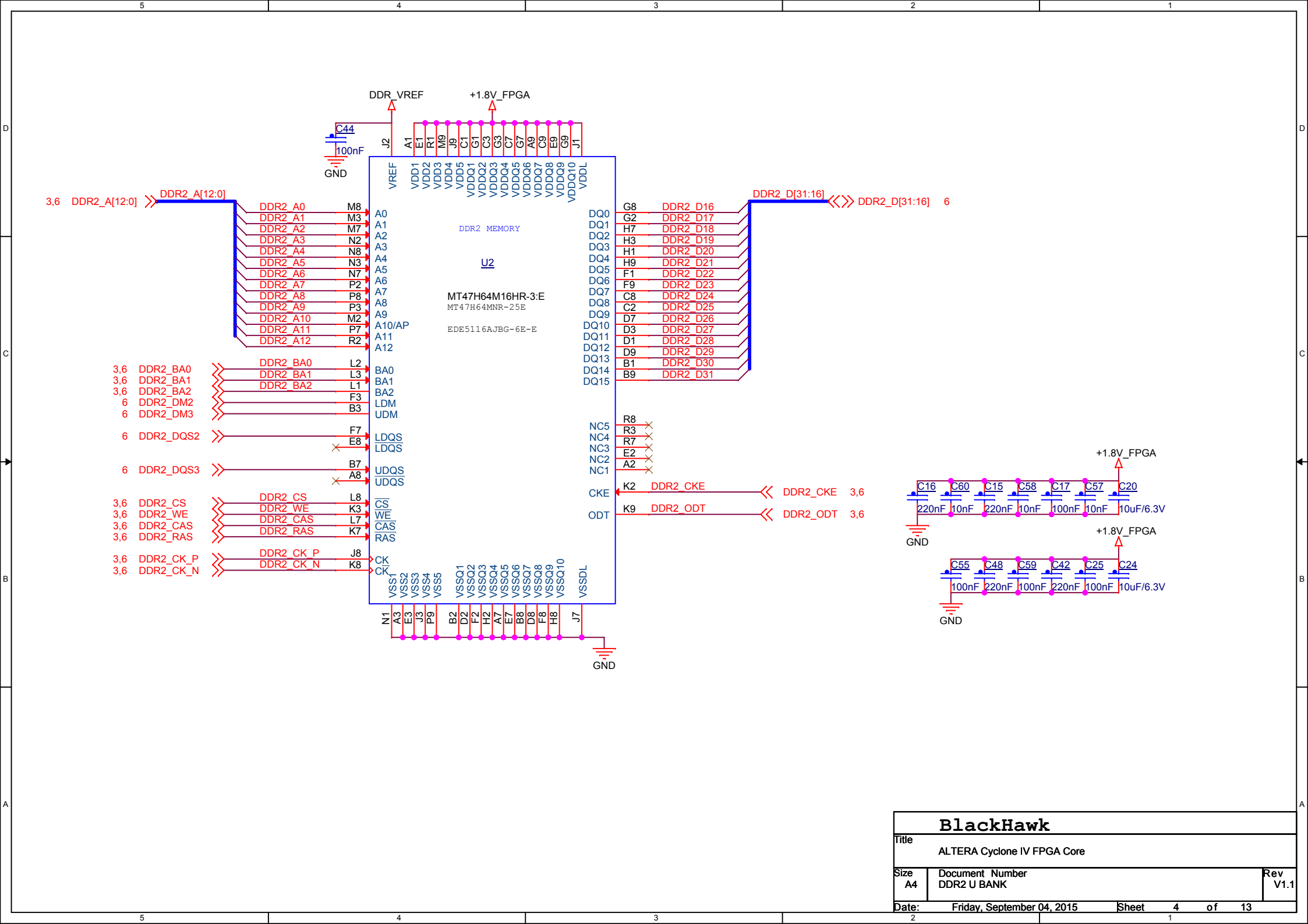
POWER CONSUMPTION							
COMPONENTS	VOTAGE&CURRENT						
	1 . 2V	1 . 8V	2 . 5V	3 . 3V			
FPGA	TBD	TBD	TBD	TBD			

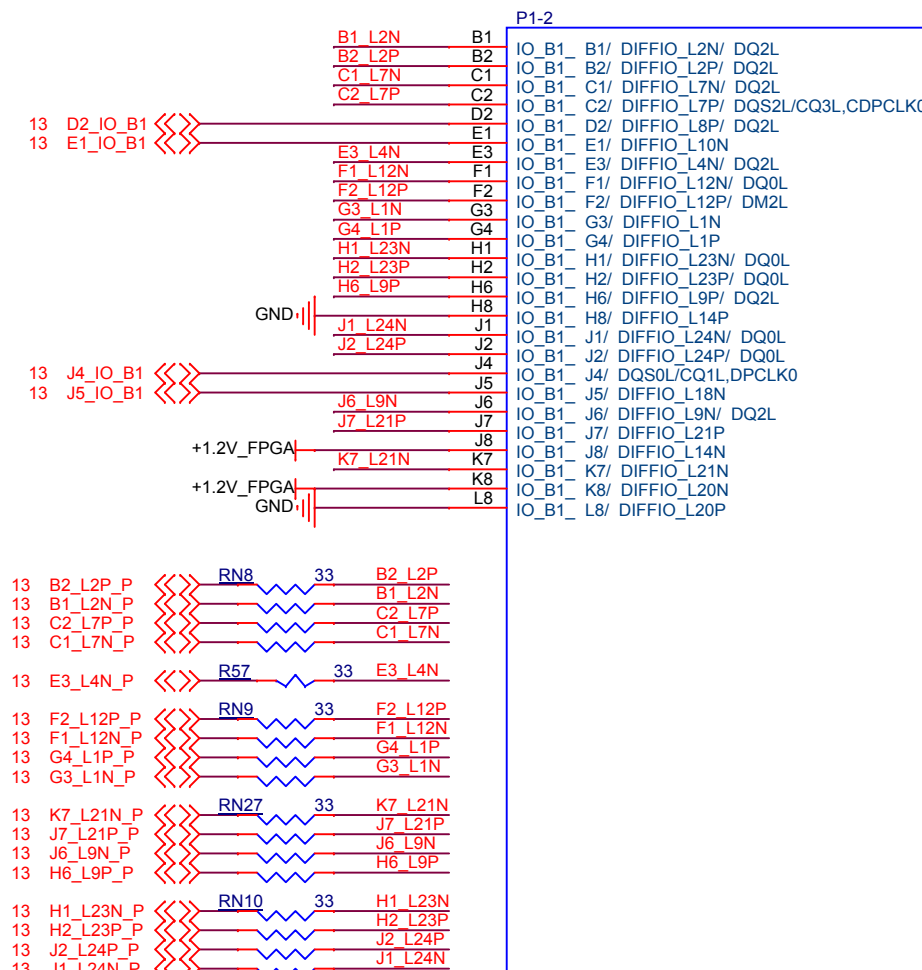




Clock terminators:
Place at end of route at DDR pair

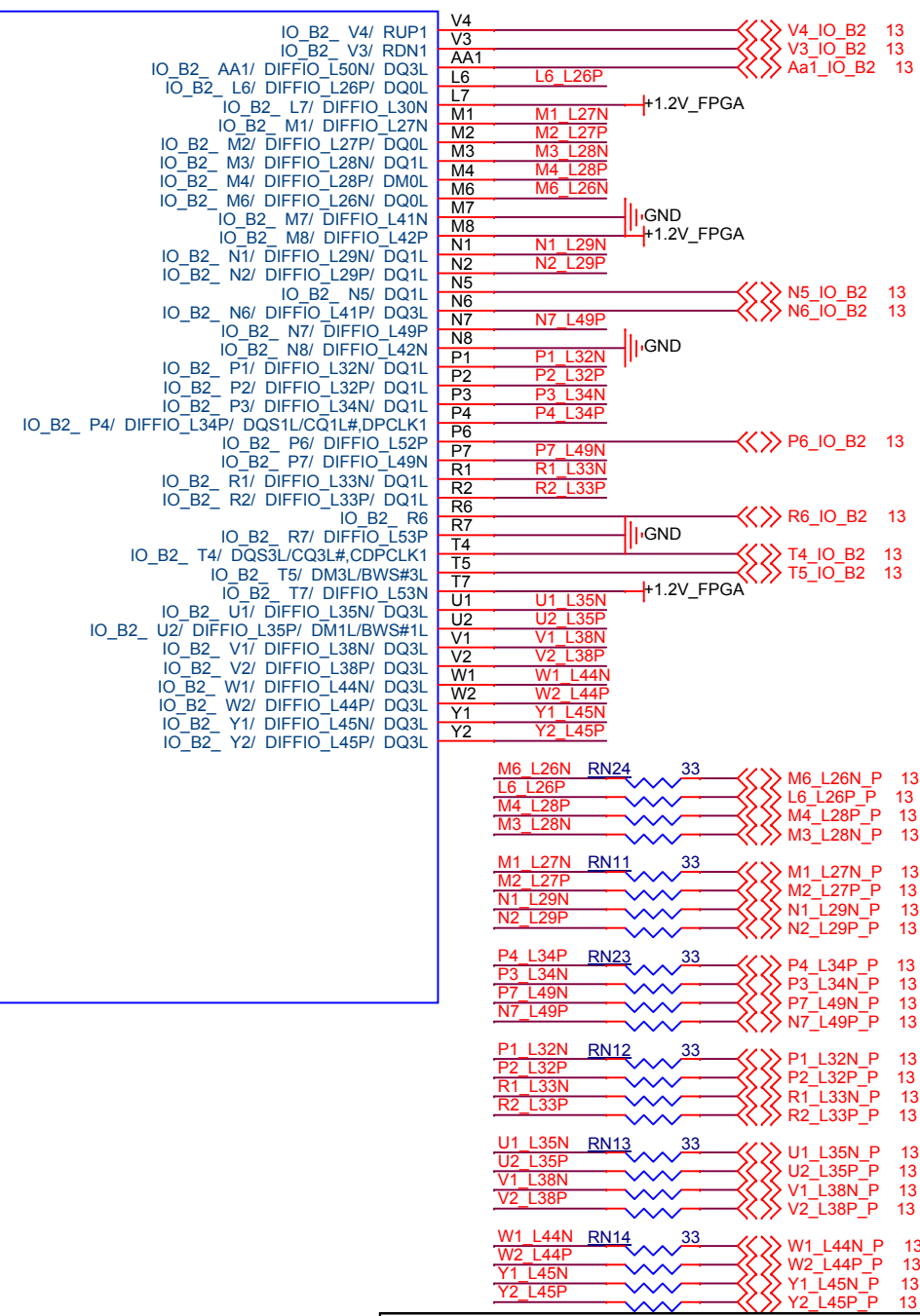
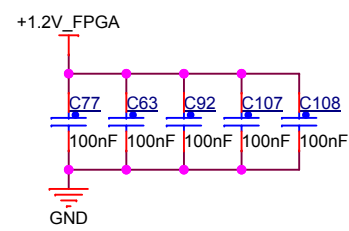




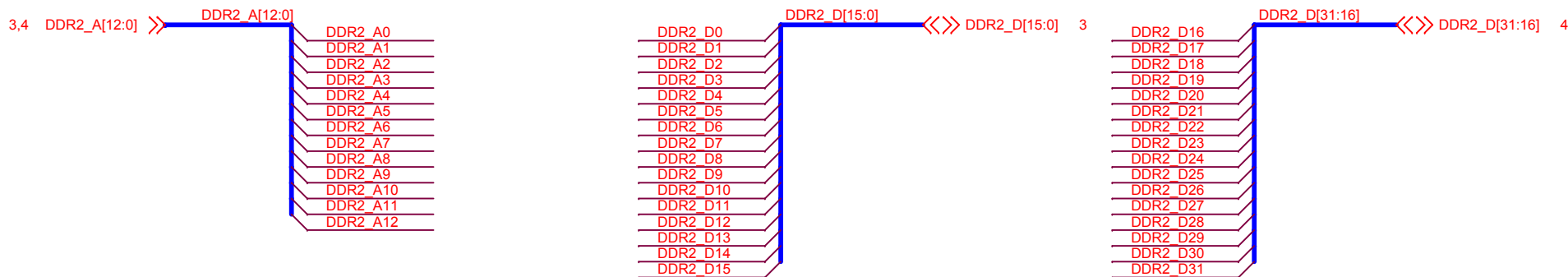
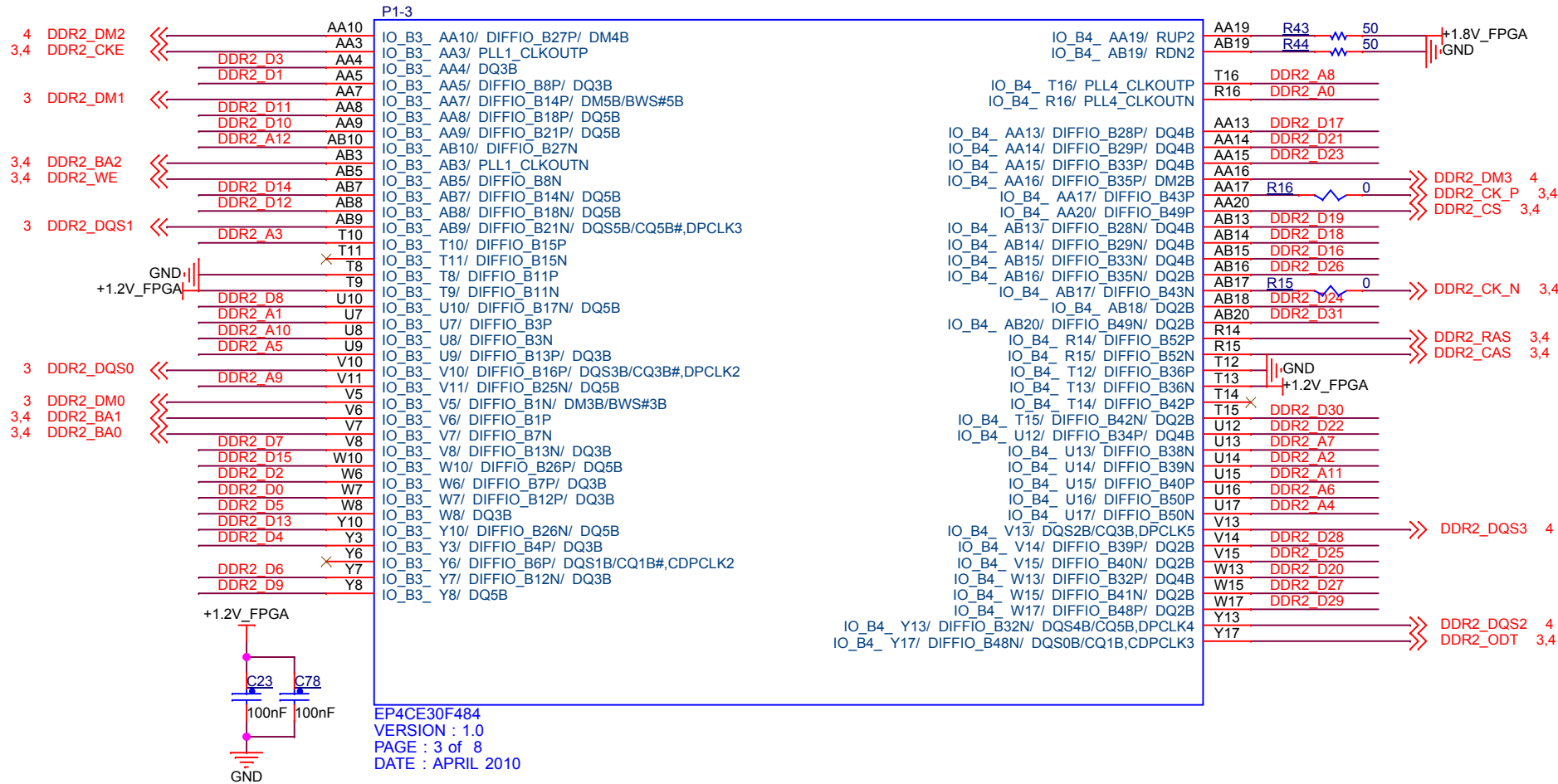


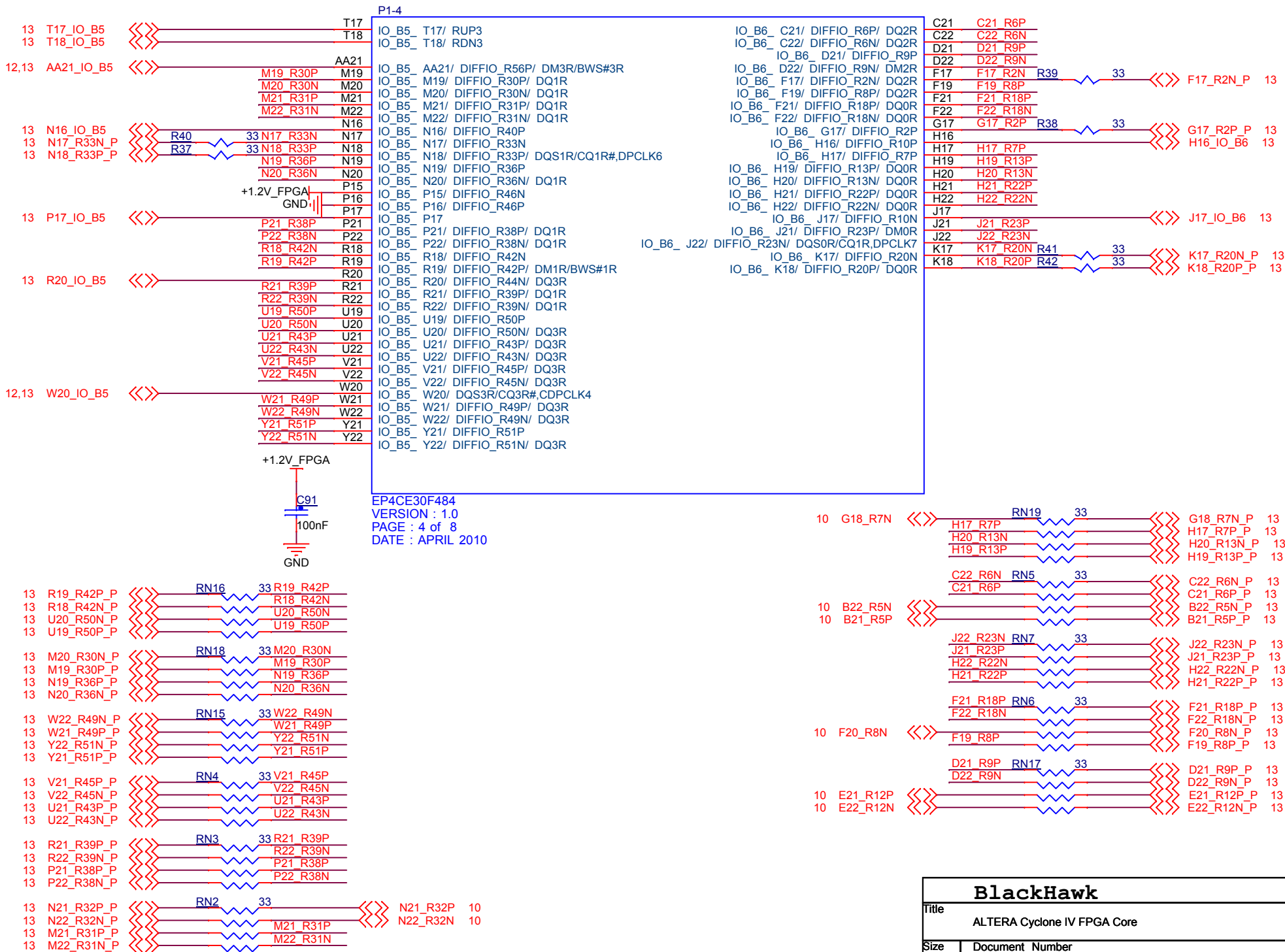
P1-2

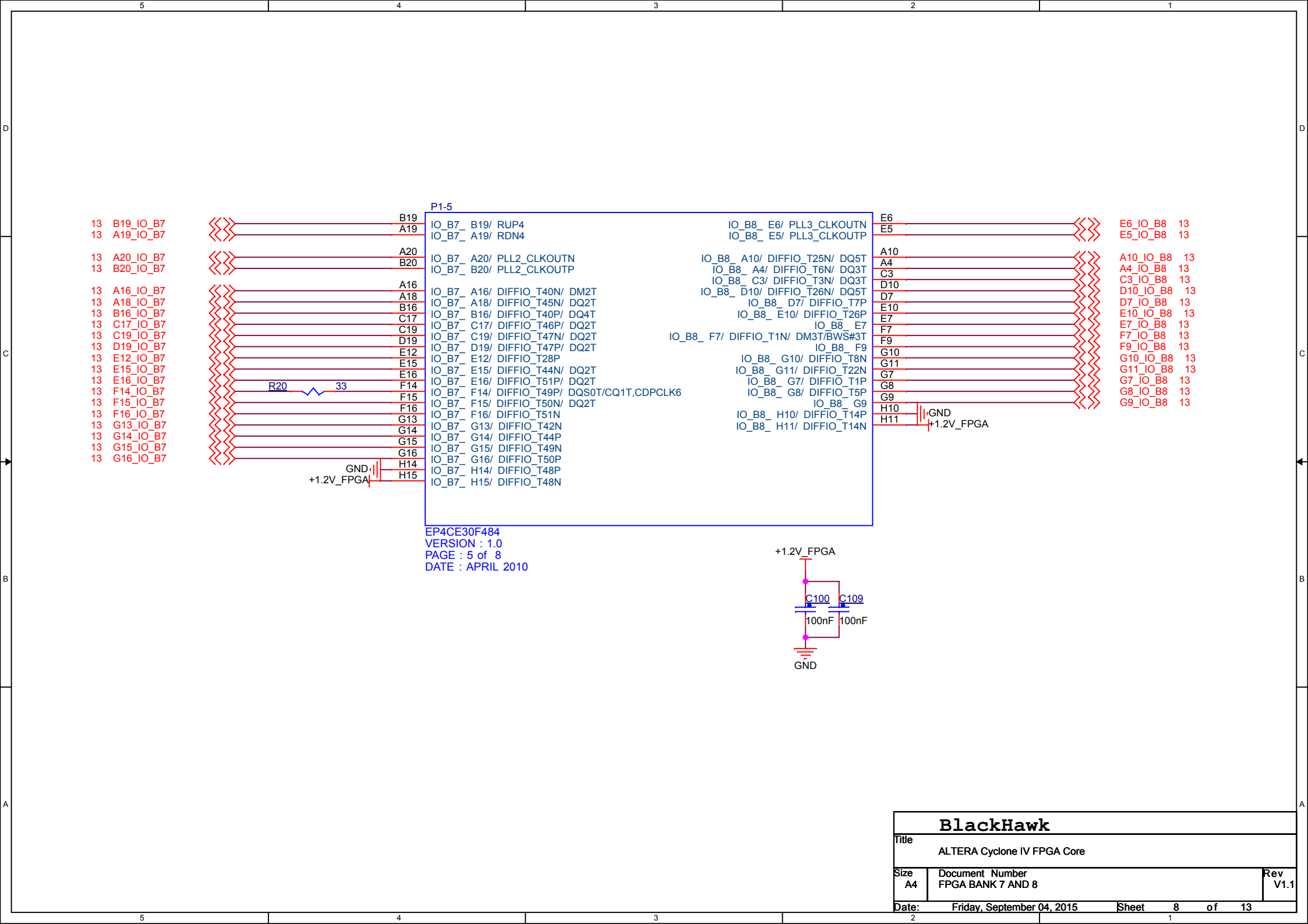
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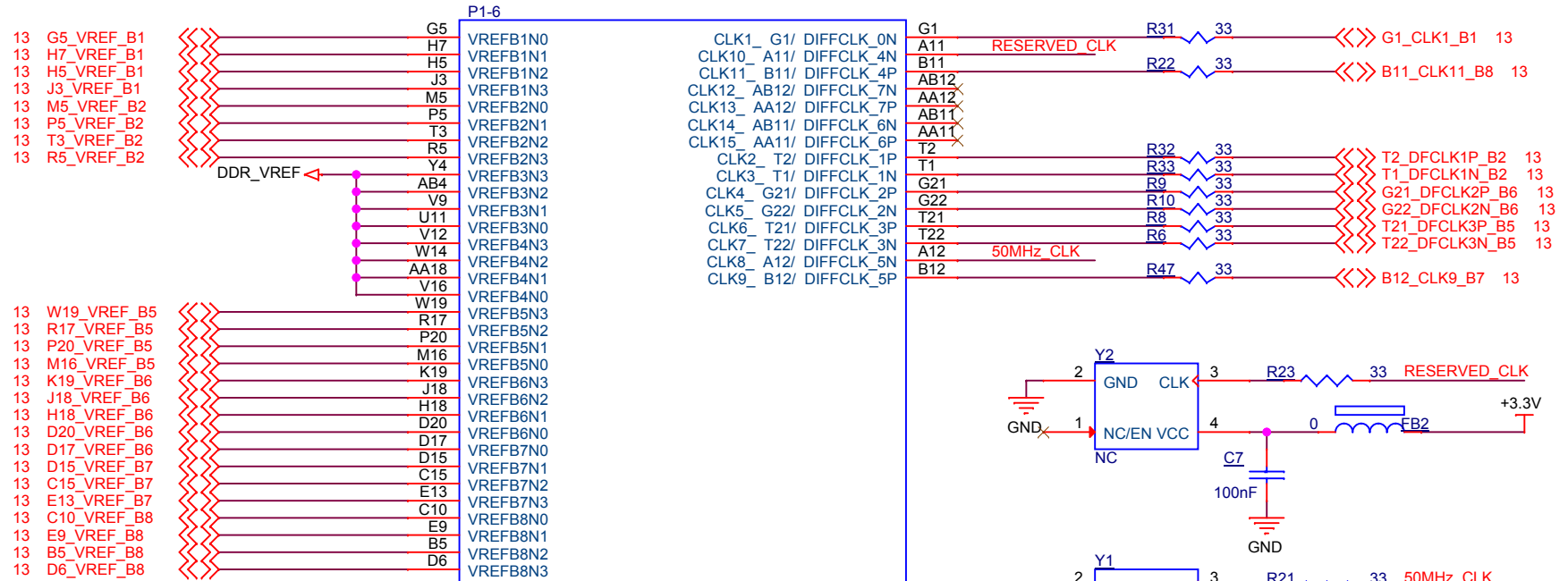


BlackHawk			
Title			
ALTERA Cyclone IV FPGA Core			
Size	Document Number		Rev
A4	FPGA BANK 1 AND 2		V1.1
Date:	Friday, September 04, 2015	Sheet	5 of 13

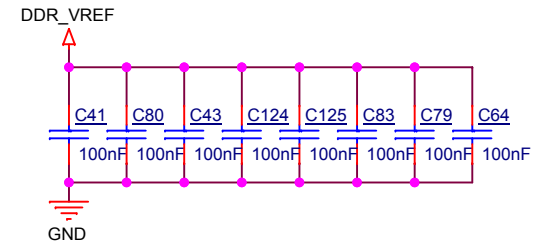
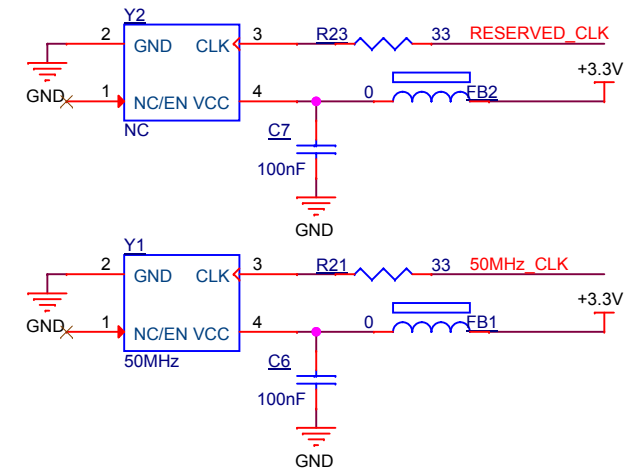


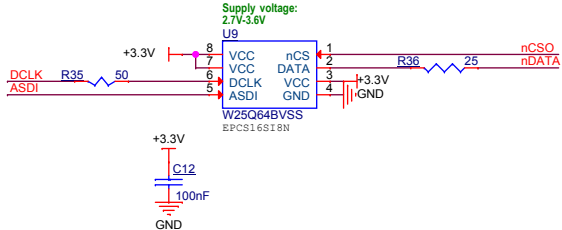
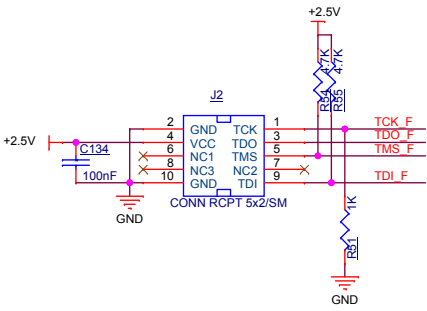
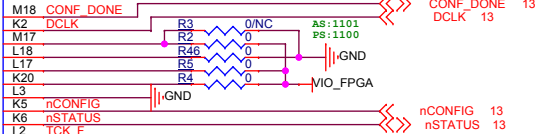
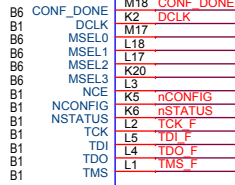
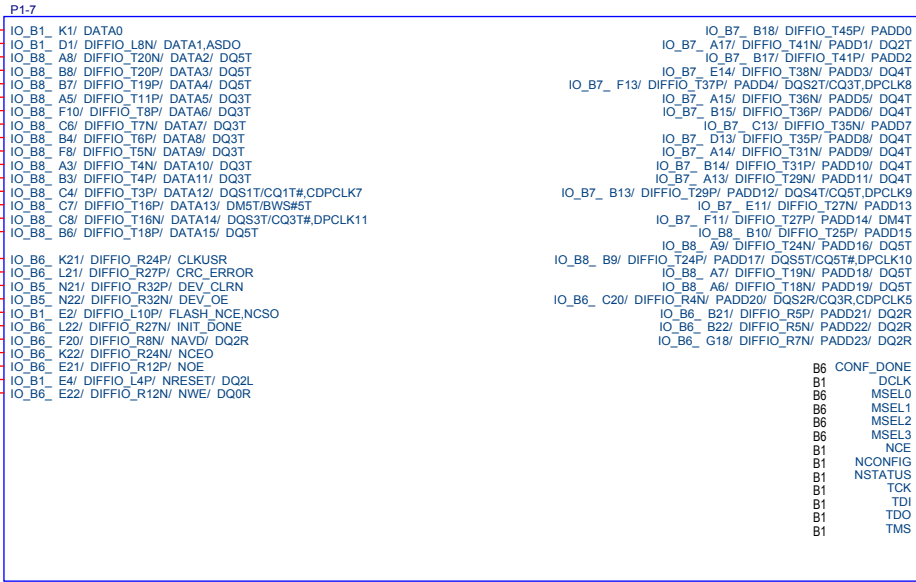
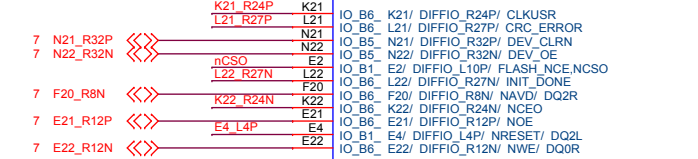
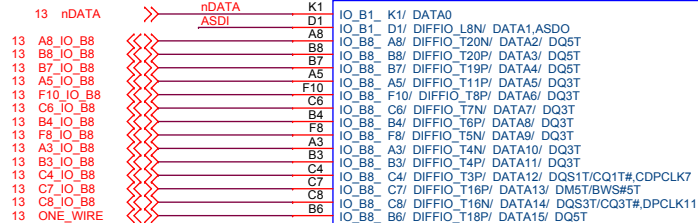


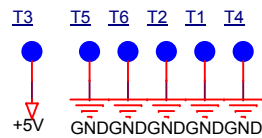
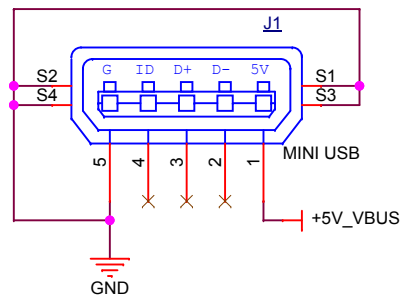
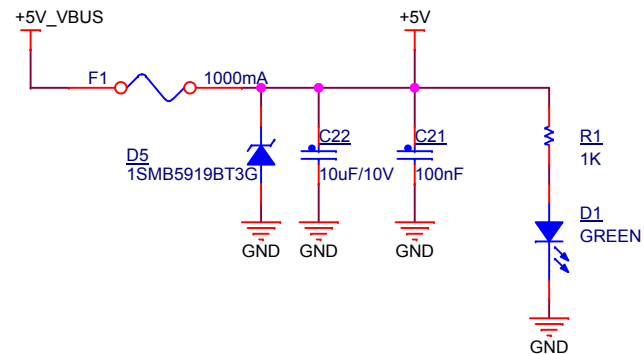
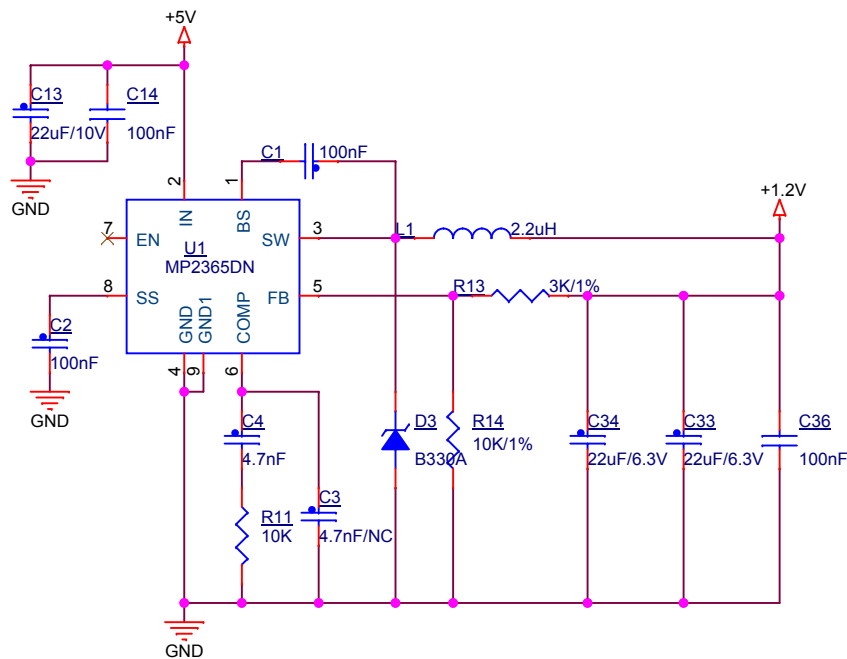




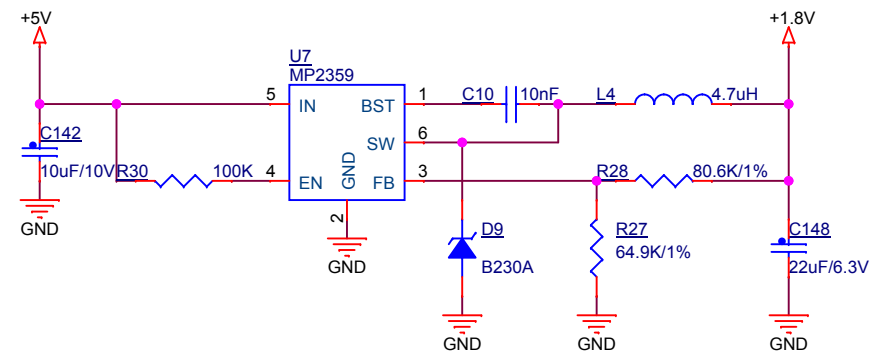
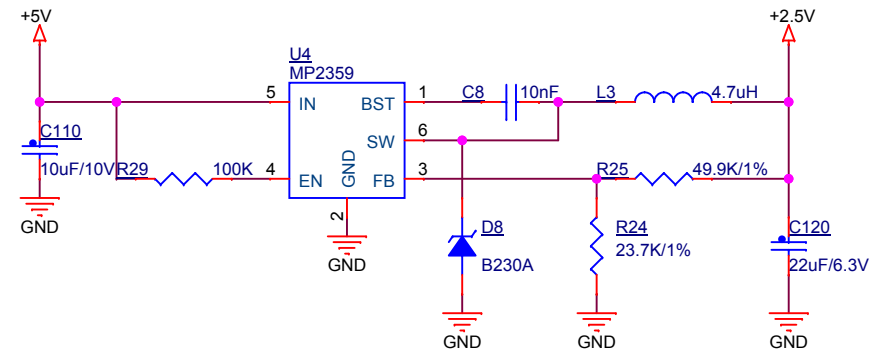
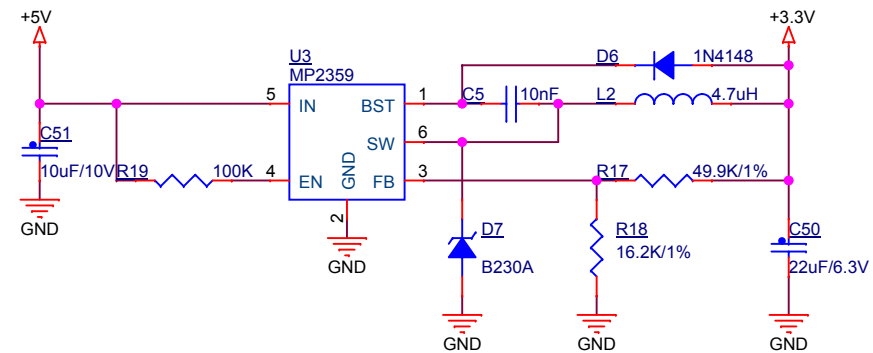
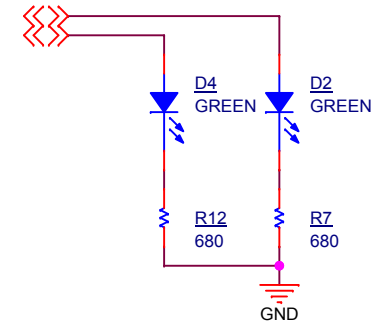
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7,13 AA21_IO_B5
7,13 W20_IO_B5



BlackHawk			
Title			
ALTERA Cyclone IV FPGA Core			
Size	Document	Number	Rev
A4	System	Power Supply	V1.1
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IO_B8:
Constraint:1442mil

IO_B8:
Constraint 1142mil

Config

IO_B1:
Constraint 1200mil

IO_LVDS:
Constraint 713mil

IO_B2:
Constraint 1141mil

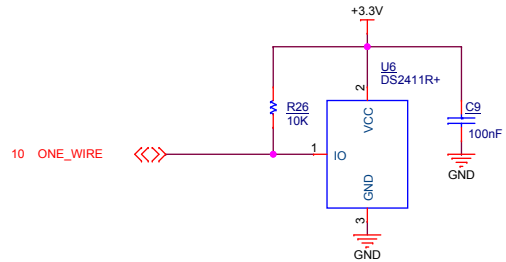
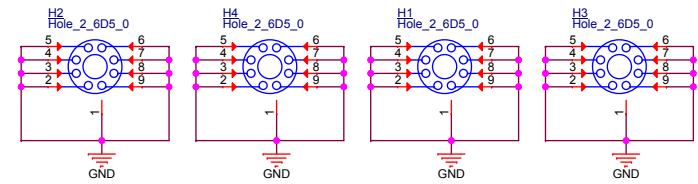
IO_B7:
Constraint 1660mil

IO_B67:
Constraint 1146mil

IO_B5:
Constraint 1320mil

notes:
pin 59 to 124 do not change target define

notes:
pin 55 to 128 do not change target define



BlackHawk			
Title			
ALTERA Cyclone IV FPGA Core			
Size A3	Document Number Connectors ANG One Wire		Rev V1.1
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