Five-Stage Pipeline CPU

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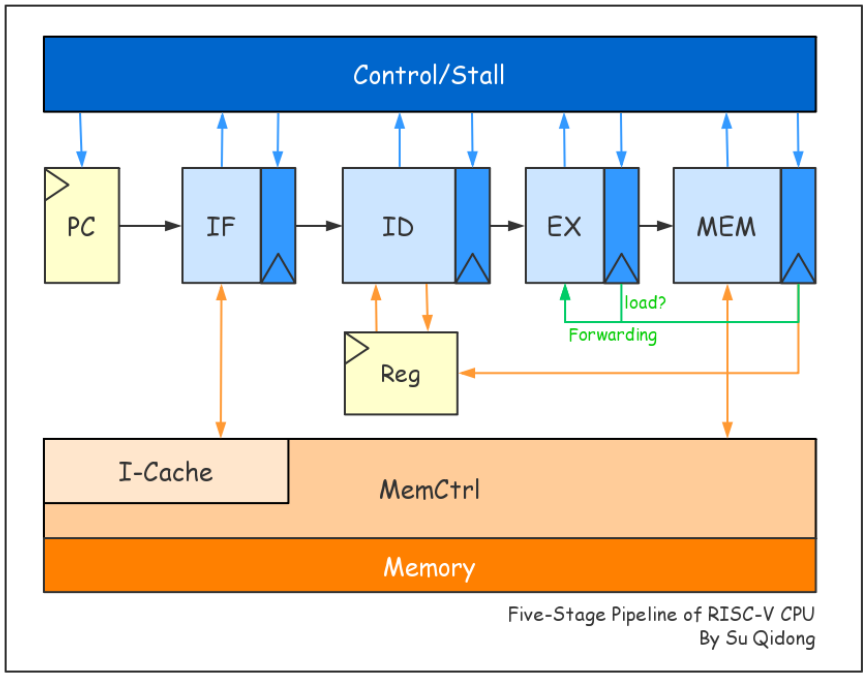
General Design

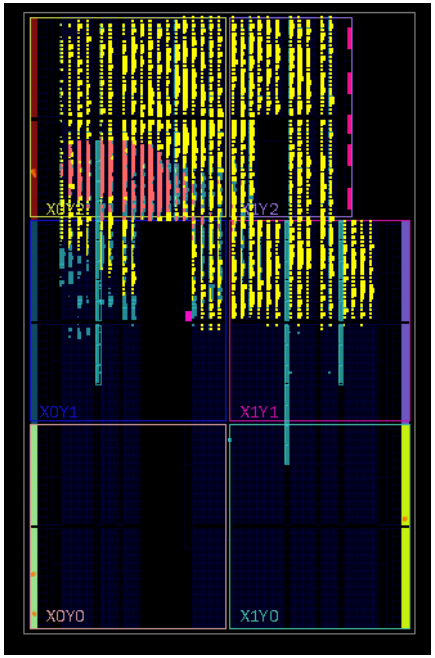
懒得做

- Keep it simple and stupid
- A ordinary 5-five pipeline



Pipeline

- Cache?
  - Without cache -> 5 cycles to fetch an instruction
  - Fake pipeline
  - I-Cache is necessary



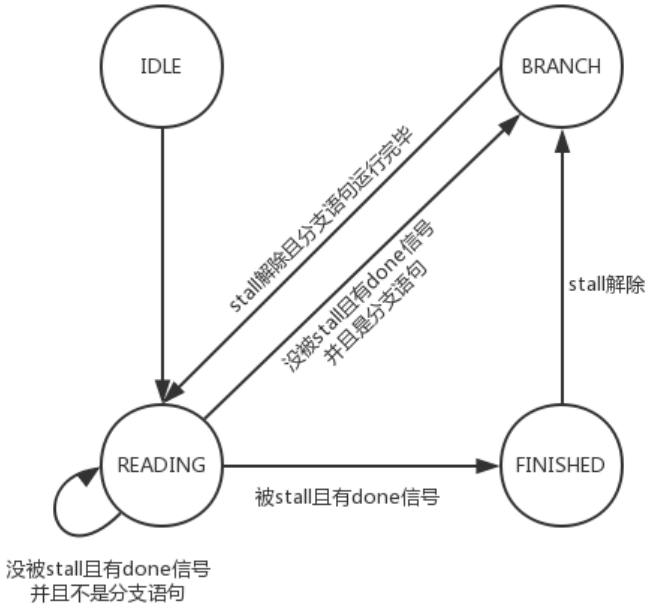
Cache

- 1 KB I-Cache
- D-Cache?
  - Timing fail
  - Very limited size

Control

- Structural hazard between MEM and IF
- Hazard control unit -> MemCtrl

- Automata
- Avoid useless cycles



Prediction?

- Dynamic ?
  - Too complicated
- Static ?
  - Always take
    - Require to calculate the address before EX
  - Always don’t take

Boost!

- Eg. Pi
- 100MHz -> 150MHz
- 2.4s -> 1.6s

- In fact, I didn’t do anything.

Balance

- Design
  - Sophisticated
  - Simple

- High clock rate = Performance?