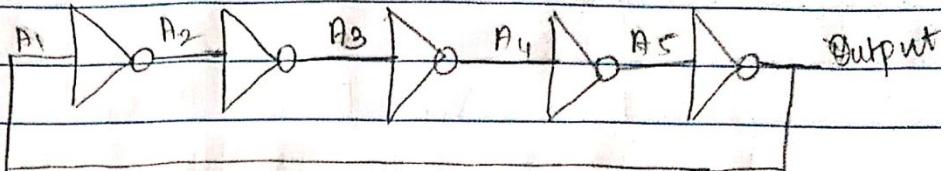


RING OSCILLATOR SCHEMATIC TO LAYOUT DESIGN REPORT

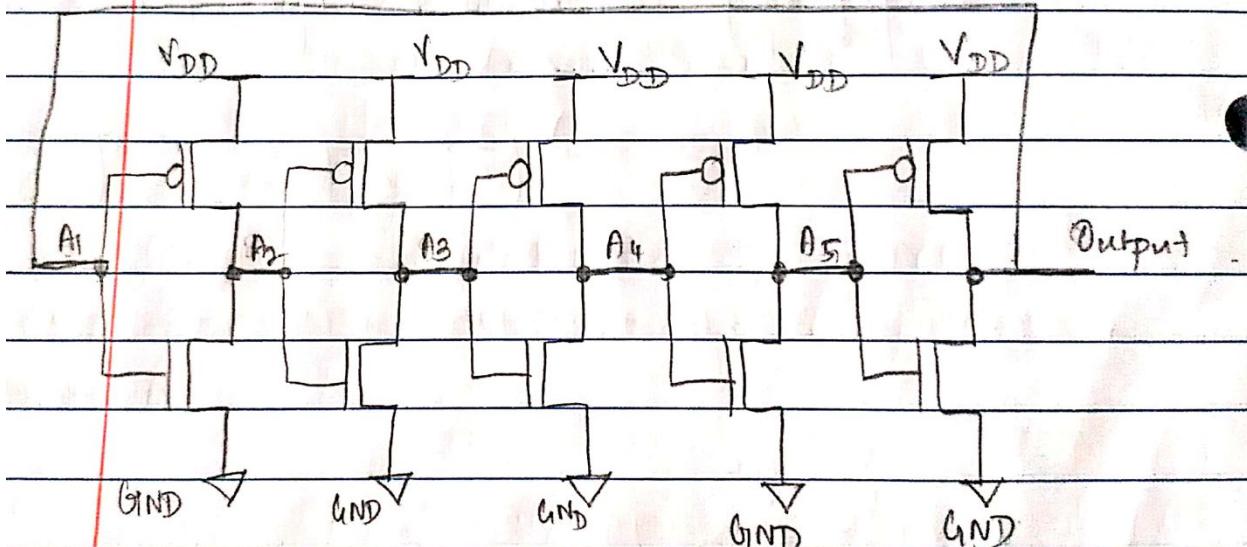
Soorya Nivedha Ashokan

Schematic of Ring Oscillator:

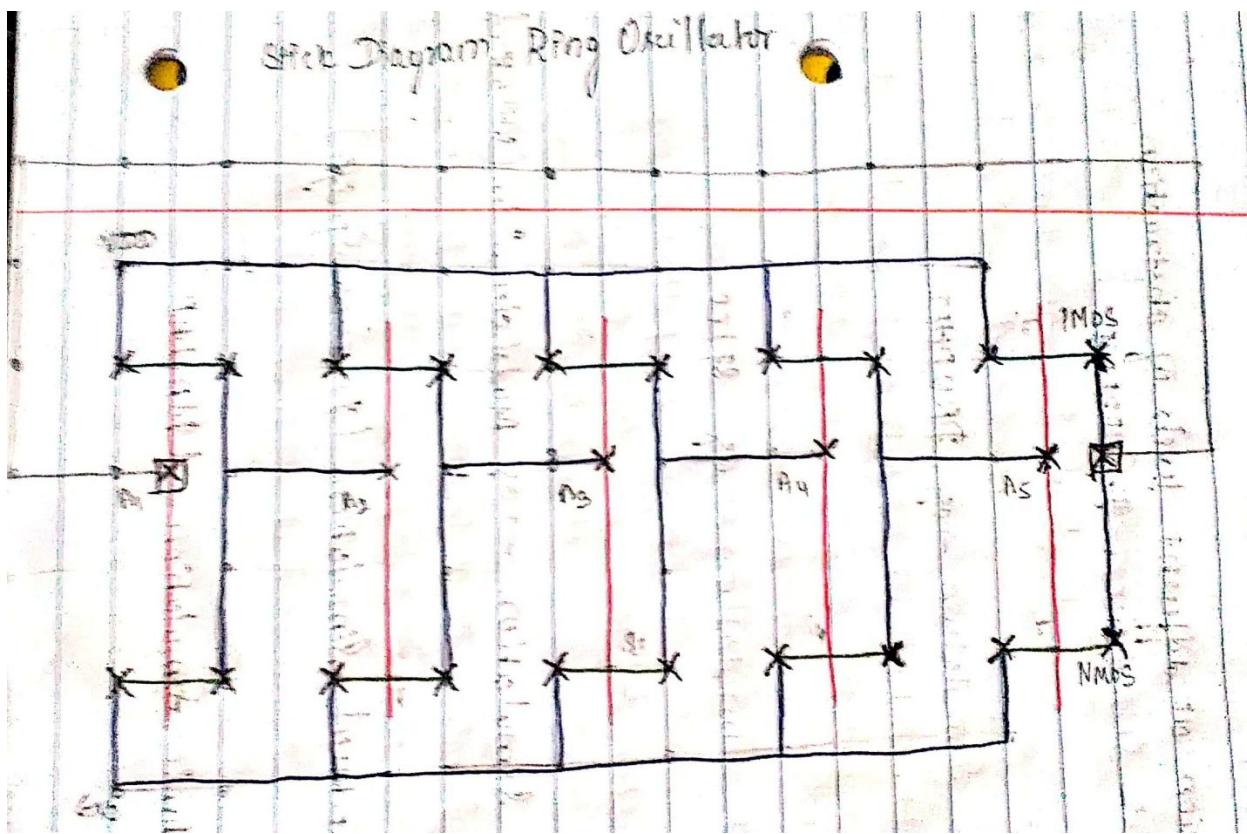
a) Ring Oscillator [5 inverters]



Transistor level schematic:



Stick Diagram for Ring Oscillator:



Note: Please ignore the contact cross at the output of A₅, by mistake I drew that cross in pen couldn't erase, only via is needed there. Also at A₁ poly I have used metal 1 to connect to poly and used metal 2 to connect to metal 1 while doing layout, but not sure how to show metal 1 there in stick diagram.

Ring Oscillator Layout Design and Simulation Report

Step 1: Leaf Cell Creation

1. Created a new design layout named as Design Project
2. Created the following leaf cells and did DRC rule check
 - NMOS transistor
 - PMOS transistor
 - CMOS Invertor
3. Created the following via and contact cells
 - MACON – Metal 1 to Active
 - MPCON – Metal 1 to poly
 - NWTIE – Metal 1 to N-well
 - SBTIE - Metal 1 to P-well
 - M12VIA – Metal 1 to Metal 2

Figure 1 shows the NMOS & PMOS transistor leaf cells , contacts and via cells created (created individually, but copied in single file for screen shot)

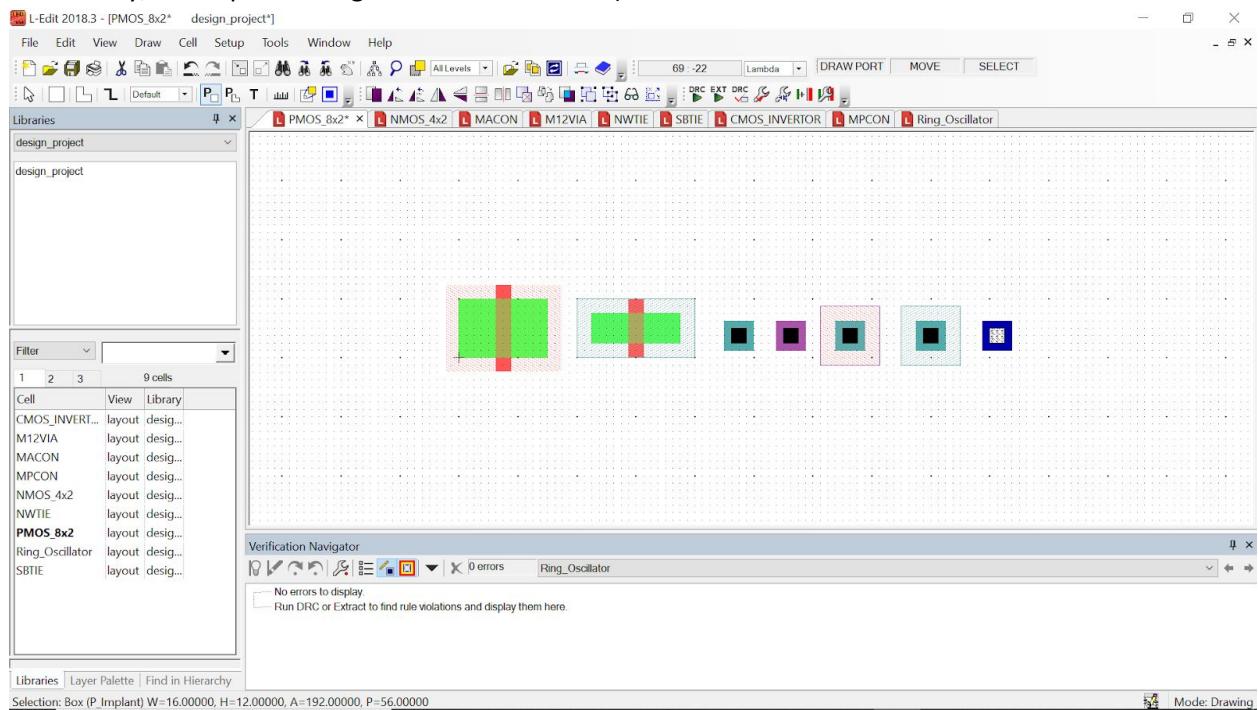


Figure2 shows the Invertor leaf cell & DRC clean status

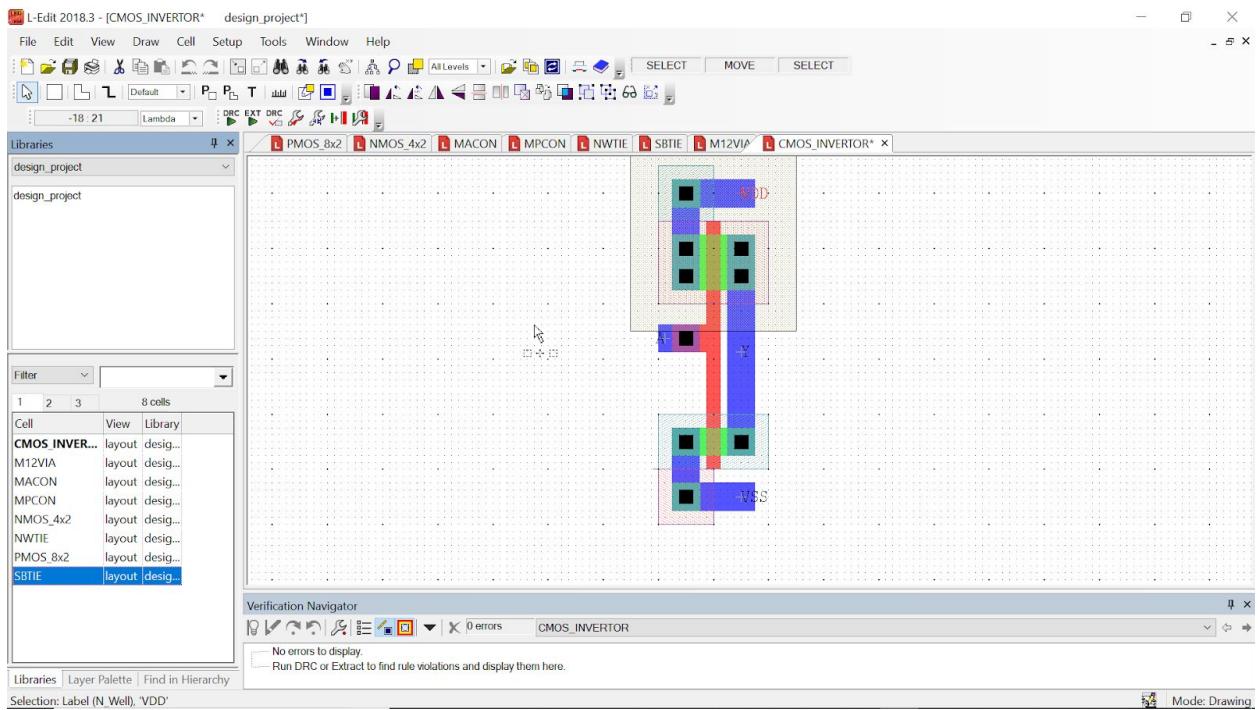


Figure 3 shows the Ring Oscillator Design using the above mentioned leaf cells and DRC clean status

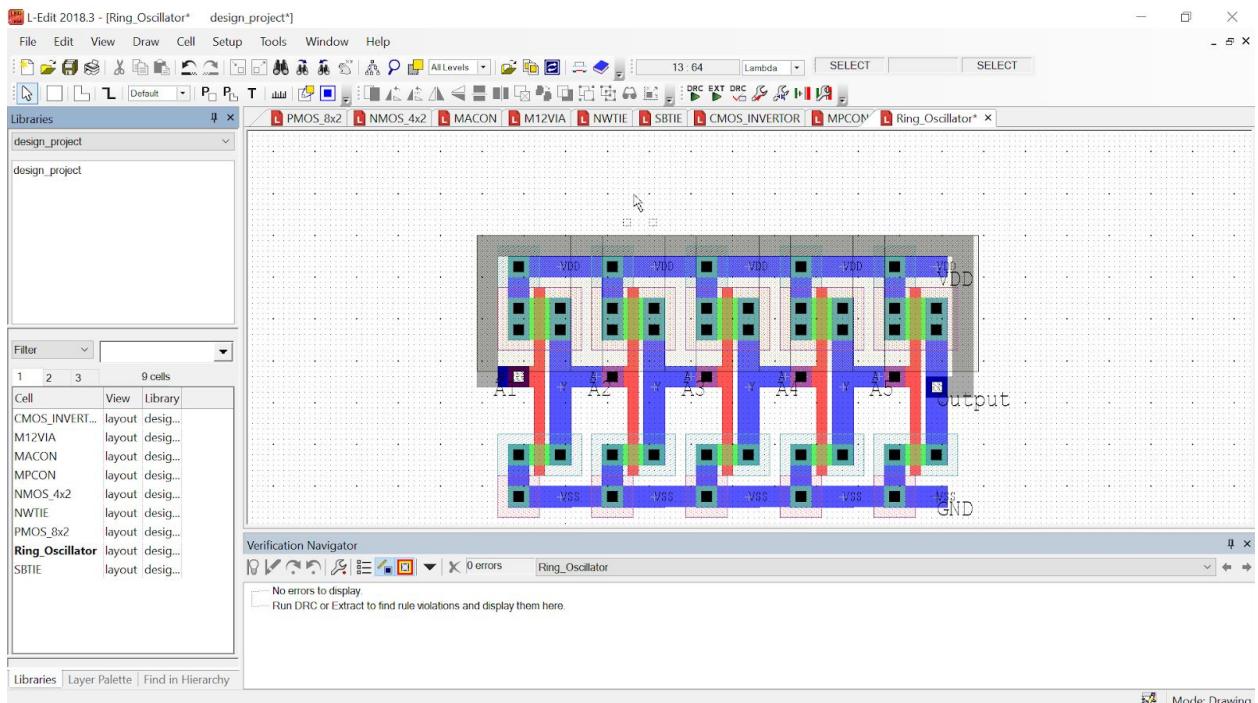
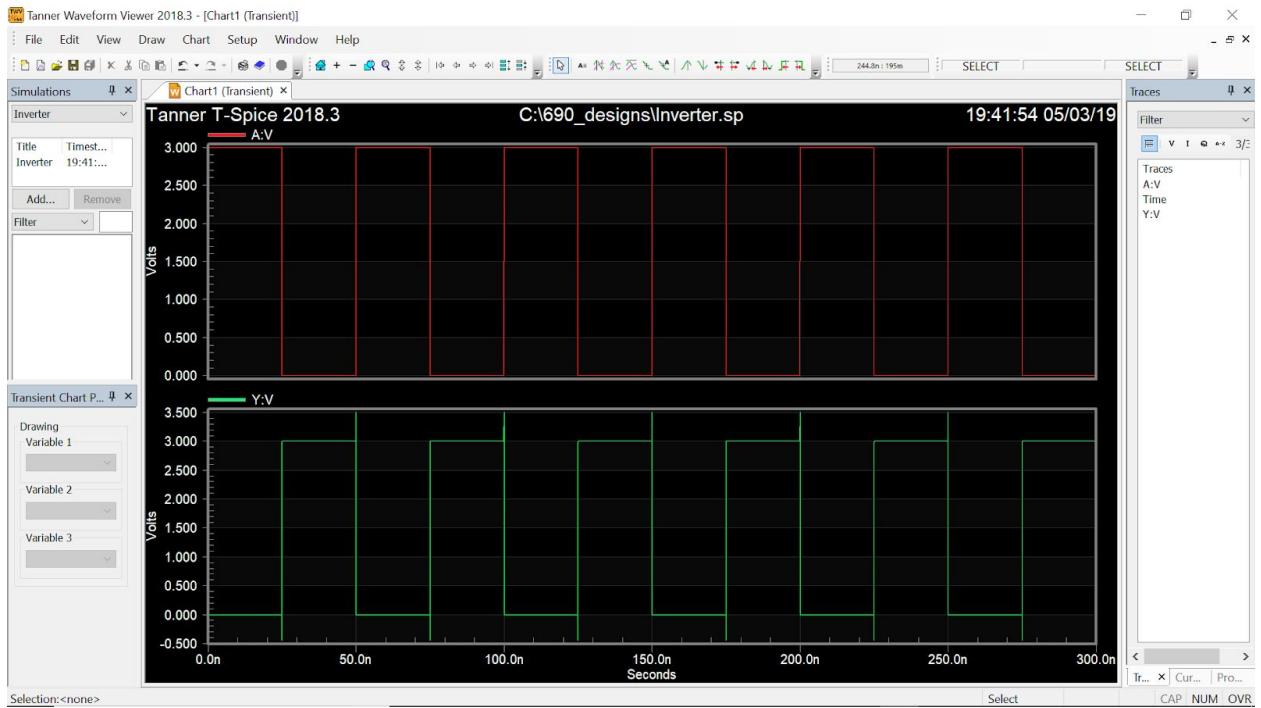


Figure 4 shows T-SPICE simulation Netlist & simulation result for CMOS Invertor

The screenshot shows the T-SPICE 2018.3 interface. On the left, the 'Inverter' netlist window displays the SPICE code for a CMOS inverter design. The code includes parameters for MOSFETs, voltage sources (VSS, VDD), and simulation commands like .tran and .print. On the right, the 'Simulation Status' window provides details about the completed simulation: Input file 'Inverter.sp', Progress 'Simulation completed', Total nodes 5, Active devices 2, Independent sources 3, and a summary of model counts. Below these are timing statistics: Parsing (0.02s), Transient Analysis (65.53s), Output (3.03s), and Total (66.42s). The status message 'Simulation completed' is shown at the bottom.

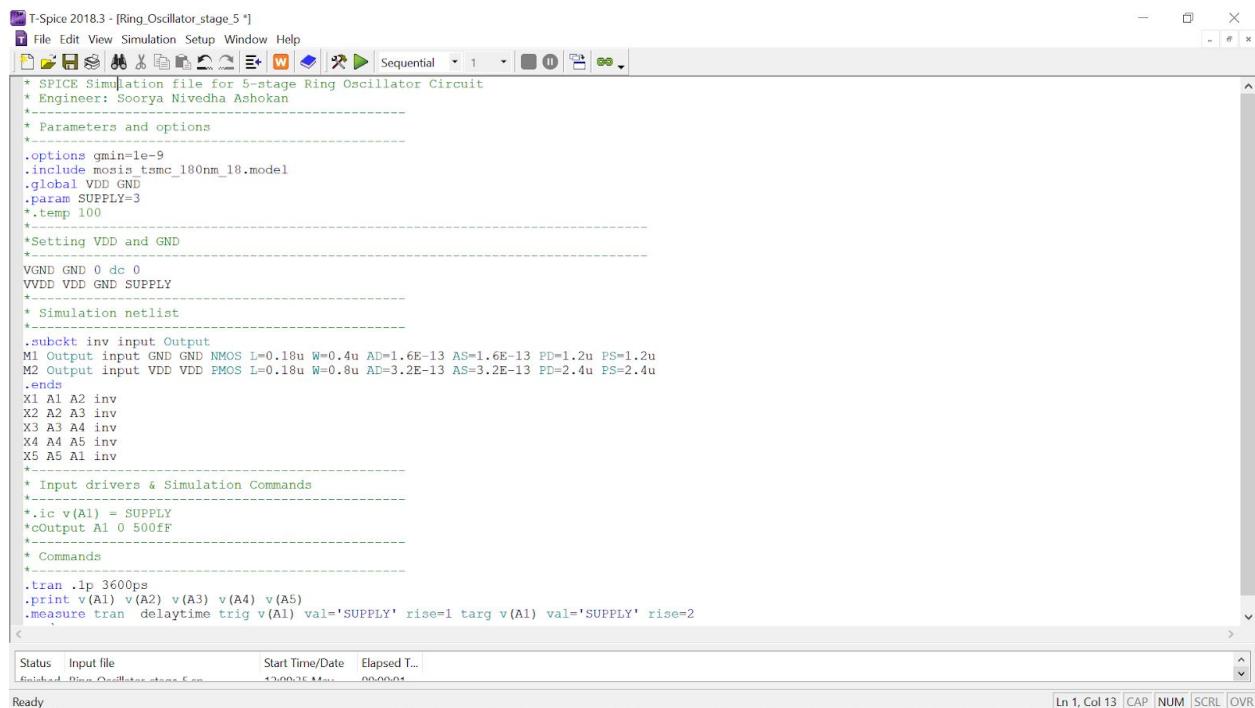
Figure 5 shows the waveform result for CMOS Invertor



Netlist Parameters usage details:

1. Using the command “.param SUPPLY=3”, I have changed the values of supply voltage and measured the frequency of Oscillation for 2.5V, 3V and 3.5V
2. Using the command “.temp 100”, I have changed the values of operating temperature and measured the frequency of Oscillation for -25C, 25C and 100C
3. Using the command “.measure …”, I have measured the delay between first rise and second rise of signal A1 to calculate the frequency of oscillation of the signal
4. Using the command “.ic V(A1) = SUPPLY”, Initiallized a value to the A1 to avoid initial metastability
5. Using the command “.cOutput A1 0 500fF”, I have changed the values of the load capacitance as 5fF, 50fF & 500fF and observed how the frequency of oscillation change as a function of load capacitance on the output of the oscillator

Figure 6 shows T-SPICE simulation Netlist for Ring Oscillator



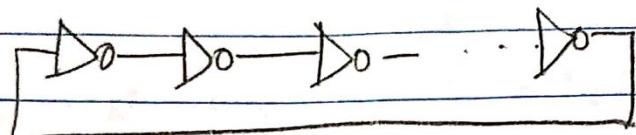
The screenshot shows the T-SPICE 2018.3 interface with the title bar "T-Spice 2018.3 - [Ring_Oscillator_stage_5.sch]". The menu bar includes File, Edit, View, Simulation, Setup, Window, and Help. Below the menu is a toolbar with various icons. The main window displays the SPICE simulation netlist for a 5-stage ring oscillator circuit. The netlist includes parameters for NMOS and PMOS transistors, simulation commands like .options, .param, .temp, and .tran, and specific circuit connections for the five stages (A1 to A5). At the bottom, there is a status bar showing "Ready" and a terminal window with the message "Completed: Ring_Oscillator_stage_5.sch".

```
* SPICE Simulation file for 5-stage Ring Oscillator Circuit
* Engineer: Soorya Nivedha Ashokan
* -----
* Parameters and options
* -----
.options qmin=1e-9
.include mosis tsmc_180nm_18.model
.global VDD GND
.param SUPPLY=3
.temp 100
* -----
*Setting VDD and GND
* -----
VGND GND 0 dc 0
VVDD VDD GND SUPPLY
* -----
* Simulation netlist
* -----
.subckt inv input Output
M1 Output input GND NMOS L=0.18u W=0.4u AD=1.6E-13 AS=1.6E-13 PD=1.2u PS=1.2u
M2 Output input VDD PMOS L=0.18u W=0.8u AD=3.2E-13 AS=3.2E-13 PD=2.4u PS=2.4u
.ends
X1 A1 A2 inv
X2 A2 A3 inv
X3 A3 A4 inv
X4 A4 A5 inv
X5 A5 A1 inv
* -----
* Input drivers & Simulation Commands
* -----
.ic v(A1) = SUPPLY
.cOutput A1 0 500fF
* -----
* Commands
* -----
.tran .lp 3600ps
.print v(A1) v(A2) v(A3) v(A4) v(A5)
.measure tran delaytime trig v(A1) val='SUPPLY' rise=1 targ v(A1) val='SUPPLY' rise=2
```

I have scanned the calculation I did in note book and added as an image here

Ring oscillator : when $N = \text{odd}$,

o for N gate delay, 1 for N gate delay, thus
keep on oscillating, since there is no proper condition
for it to settle.



logical effort : $g = 1$

electrical effort : $h = 1$

parasitic delay : $p = 1$

stage delay $d = g \cdot h + p = 2$

frequency : $f_{\text{osc}} = \frac{1}{2 \cdot N \cdot d} = \frac{1}{4N\tau}$

If $N = 31$

0.64μm process : $\tau = 60 \text{ ps}$, $f = 135 \text{ MHz}$

65nm proc : $(\tau = 3 \text{ ps})$, $f = 2.7 \text{ GHz}$

τ -calculation

We know frequency of an N -stage ring oscillator.

$$f_{osc} = \frac{1}{4NT} \Rightarrow T = \frac{1}{4Nf_{osc}}$$

case 1: $N = 5$

$$f_{osc} = 3.74495367 \text{ GHz}$$

$$f_{osc} = 3.74 \text{ GHz}$$

$$T = \frac{1}{4 \times 5 \times 3.74 \times 10^9}$$

$$T = 0.01336 \times 10^{-9}$$

case 2: $N = 5$

$$f_{osc} = 3.84995938 \text{ GHz}$$

$$f_{osc} = 3.85 \text{ GHz}$$

$$T = \frac{1}{4 \times 5 \times 3.85 \times 10^9}$$

$$T = 0.01298 \times 10^{-9}$$

case 3: $N = 5$

$$f_{osc} = 3.46403123 \text{ GHz} = 3.46 \text{ GHz}$$

$$T = \frac{1}{4 \times 5 \times 3.46 \times 10^9}$$

$$T = 0.01445 \times 10^{-9}$$

Case 4: $N = 5$

$$f_{osc} = 3.7936411 \text{ GHz} = 3.79 \text{ GHz}$$

$$\tau = \underline{1}$$

$$\boxed{\tau = 0.0132 \times 10^{-9}}$$

Case 5: $N = 5$, $f_{osc} = 3.97364993 \text{ GHz}$

$$\tau = \underline{1}$$

$$4 \times 5 \times 3.97 \times 10^9$$

$$\boxed{\tau = 0.01259 \times 10^{-9}}$$

Case 6: $N = 5$, $f_{osc} = 4.03299474 \text{ GHz}$

$$\tau = \underline{1}$$

$$4 \times 5 \times 4.03 \times 10^9$$

$$\boxed{\tau = 0.0124 \times 10^{-9}}$$

Case 7: $N = 5$, $f_{osc} = 3.0516293 \text{ GHz}$

$$\tau = \underline{1}$$

$$4 \times 5 \times 3.05 \times 10^9$$

$$\boxed{\tau = 0.01639 \times 10^{-9}}$$

Case 8: $N = 5$, $f_{osc} = 3.52362432 \text{ GHz}$

$$\tau = \underline{1}$$

$$4 \times 5 \times 3.52 \times 10^9$$

$$\boxed{\tau = 0.0142 \times 10^{-9}}$$

Case 9: $N = 5$, $f_{osc} = 3.88494804 \text{ GHz}$

$$\tau = \underline{1}$$

$$4 \times 5 \times 3.88 \times 10^9$$

$$\boxed{\tau = 0.01288 \times 10^{-9}}$$

Summary of change in τ as a function of temperature and supply voltage

Observation:

- Change of τ with respect to supply voltage and temperature is shown in the table
- Case 6 shows that the circuit runs faster at -25C with supply Voltage as 2.5V

Cases	Supply Voltage	Temperature	Frequency of Oscillation	τ
Case 1	3V	25C	3.74495367GHz	0.01336ns
Case 2	3.5V		3.84995938Ghz	0.01298ns
Case 3	2.5V		3.46403123GHz	0.01445ns
Case 4	3V	-25C	3.7936411GHz	0.0132ns
Case 5	3.5V		3.97364993Ghz	0.01259ns
Case 6	2.5V		4.03299474GHz	0.0124ns
Case 7	3V	100C	3.0516293GHz	0.01639ns
Case 8	3.5V		3.52362432GHz	0.0142ns
Case 9	2.5V		3.88494804GHz	0.01288ns

Summary of change in the frequency of oscillation as a function of load capacitance on the output of the oscillator

Observation:

As load capacitance increases, the change in state of the stages got delayed due to the time taken by the capacitor to discharge.

Cases	Load Capacitance	Frequency of Oscillation
Case 1	0	3.74483587GHZ
Case 2	5fF	3.24699993GHZ
Case 3	50fF	1.91307229GHz
Case 4	500fF	487.376937MHz

Results without using “ .ic v(A1) = SUPPLY ” for Initialization.

Temperature: 25C

Voltage: 3V

Figure 7 shows Expanded View of Output of each stage without Initialization:

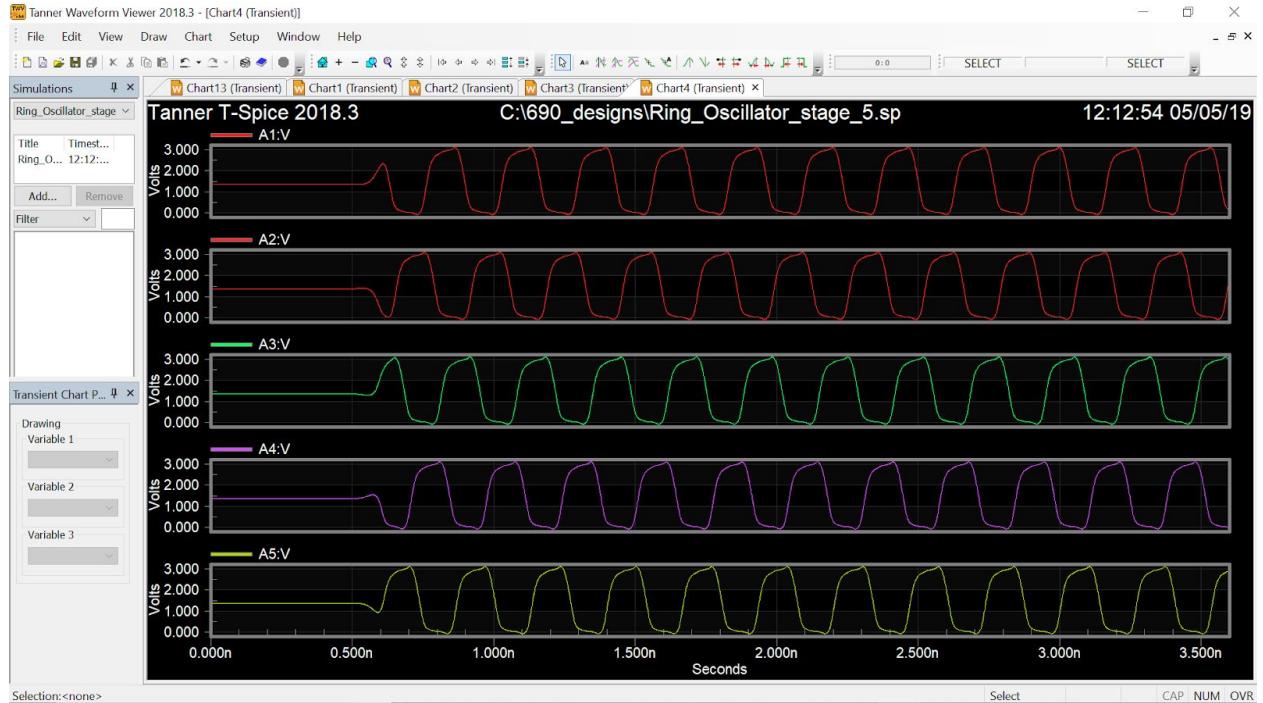
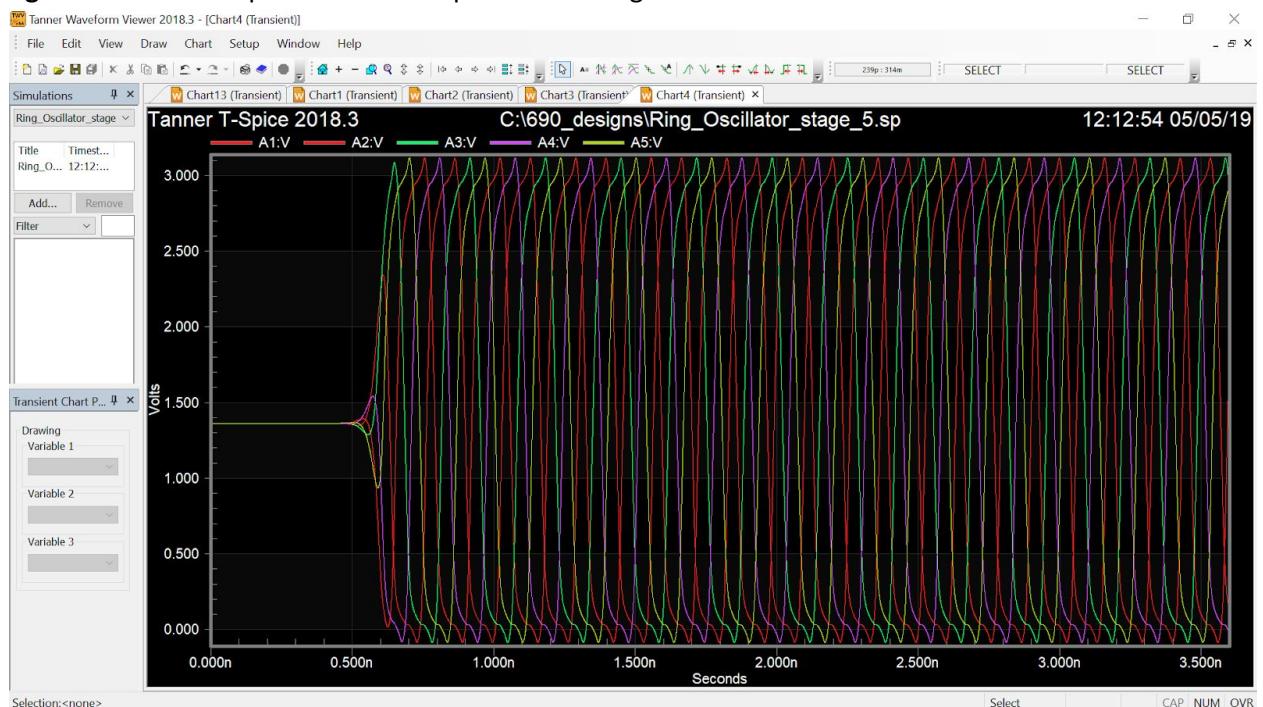


Figure 8 shows Collapsed View of Output of each stage without Initialization:



Results using “ .ic v(A1) = SUPPLY ” for Initialization to avoid metastable state:

Case 1: Temperature: 25C

Voltage: 3V

Measurement result summary:

Delay time = 267.0260ps A1(first rise to second rise)

Frequency of Oscillation: 3.74495367GHz

Figure 9 shows Expanded View of Output of each stage with Initialization:

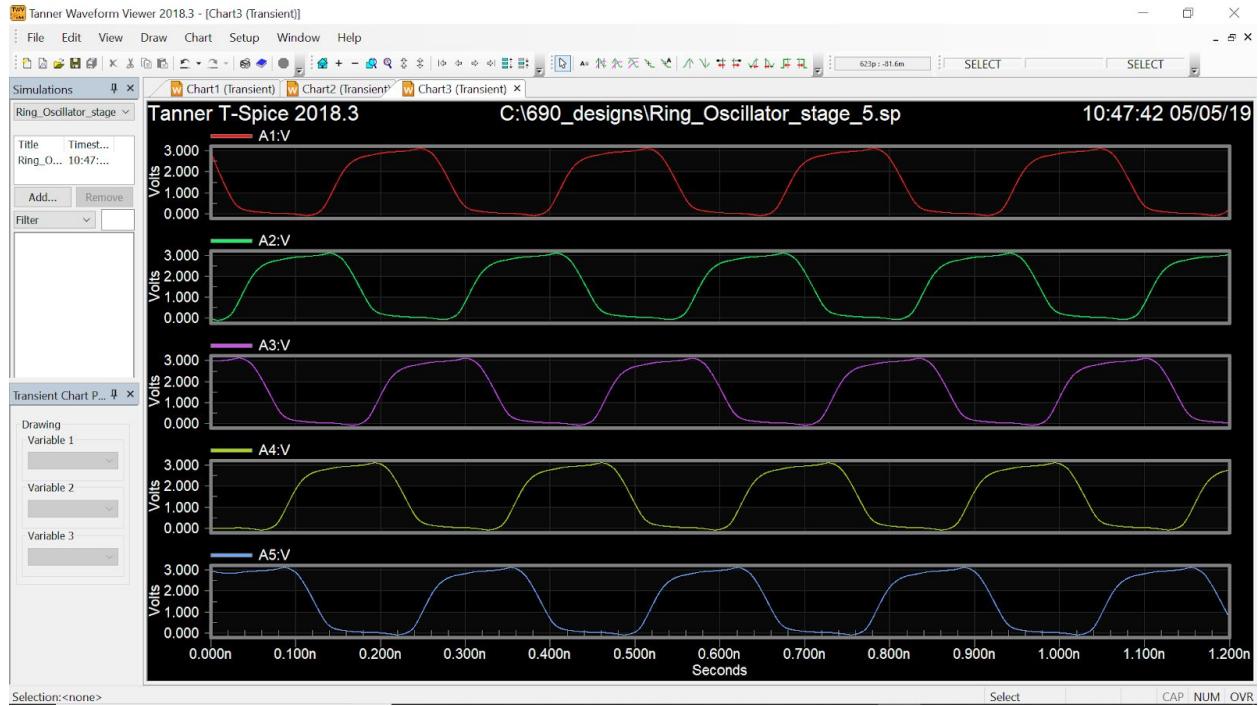
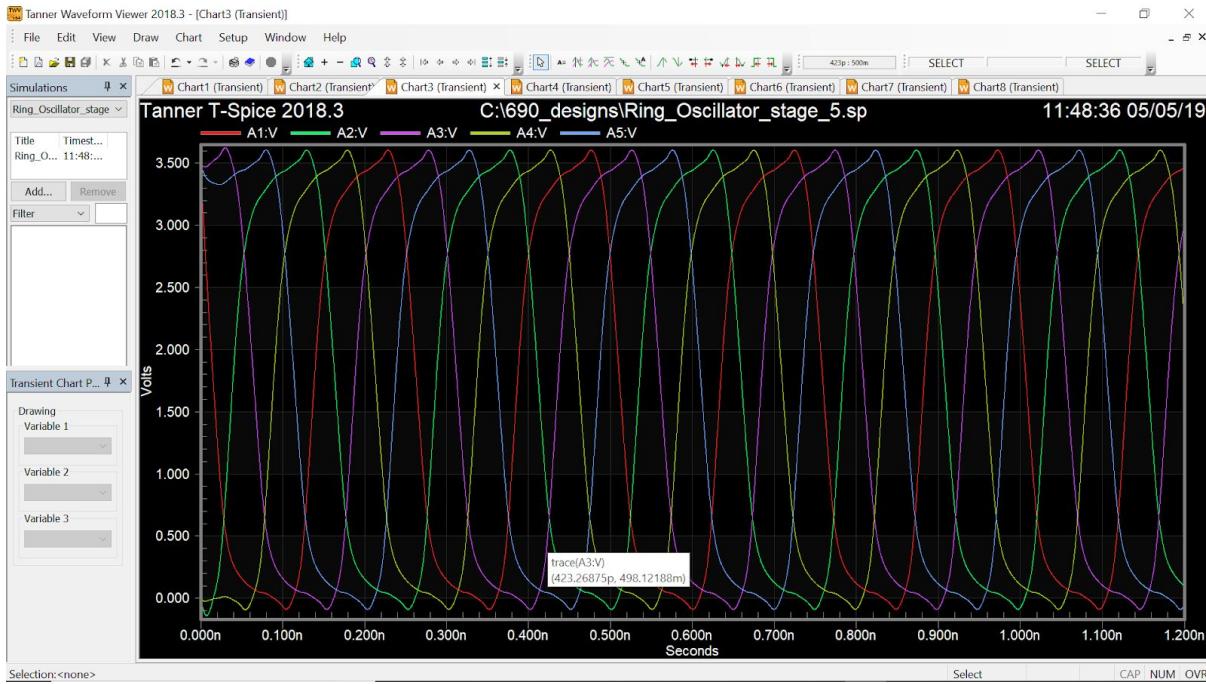


Figure 10 shows Collapsed View of Output of each stage with Initialization:



Case2: Temperature: 25C

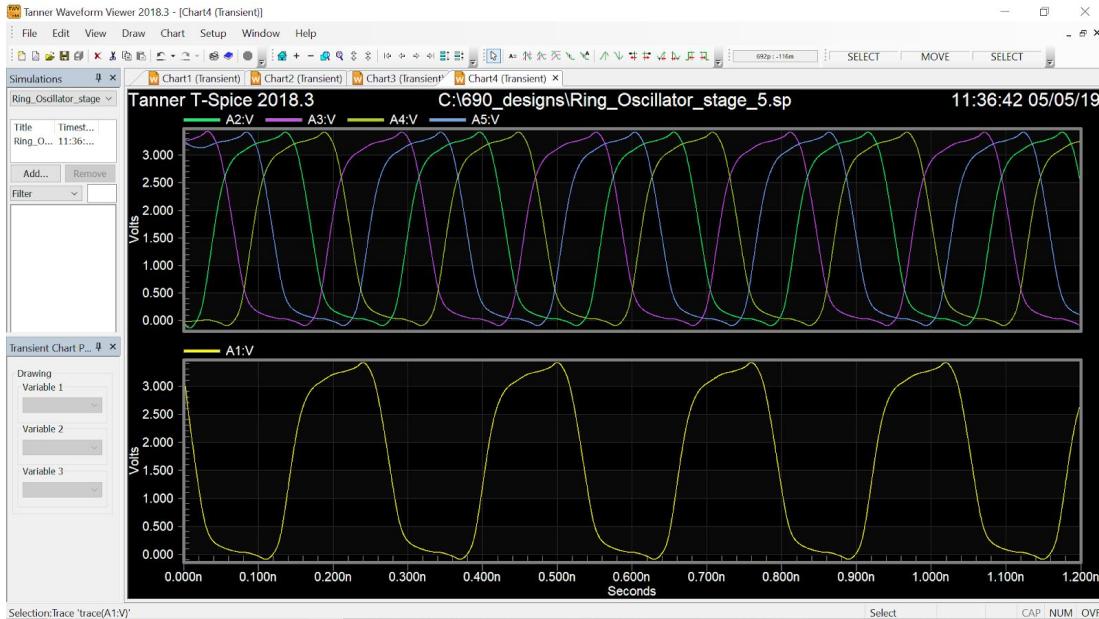
Voltage: 3.5V

Measurement result summary

Delay time = 259.7430ps A1(first rise to second rise)

Frequency of Oscillation: 3.84995938Ghz

Figure 11 shows the waveform for case 2



Case 3: Temperature: 25C

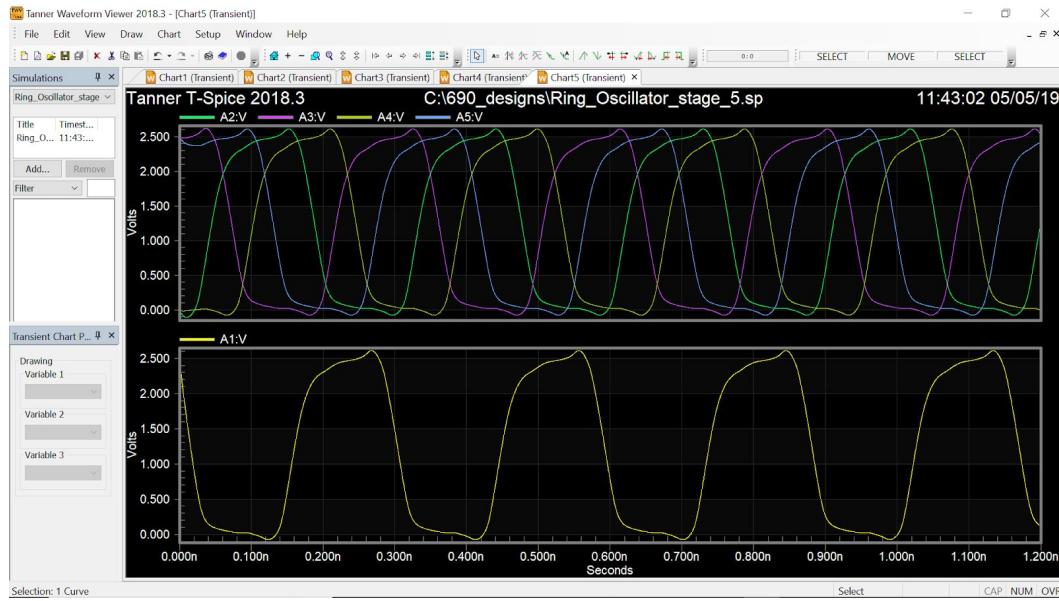
Voltage: 2.5V

Measurement result summary

Delay time = 288.6810ps A1(first rise to second rise)

Frequency of Oscillation: 3.46403123GHz

Figure 12 shows the waveform for case 3



Case 4: Temperature: -25C

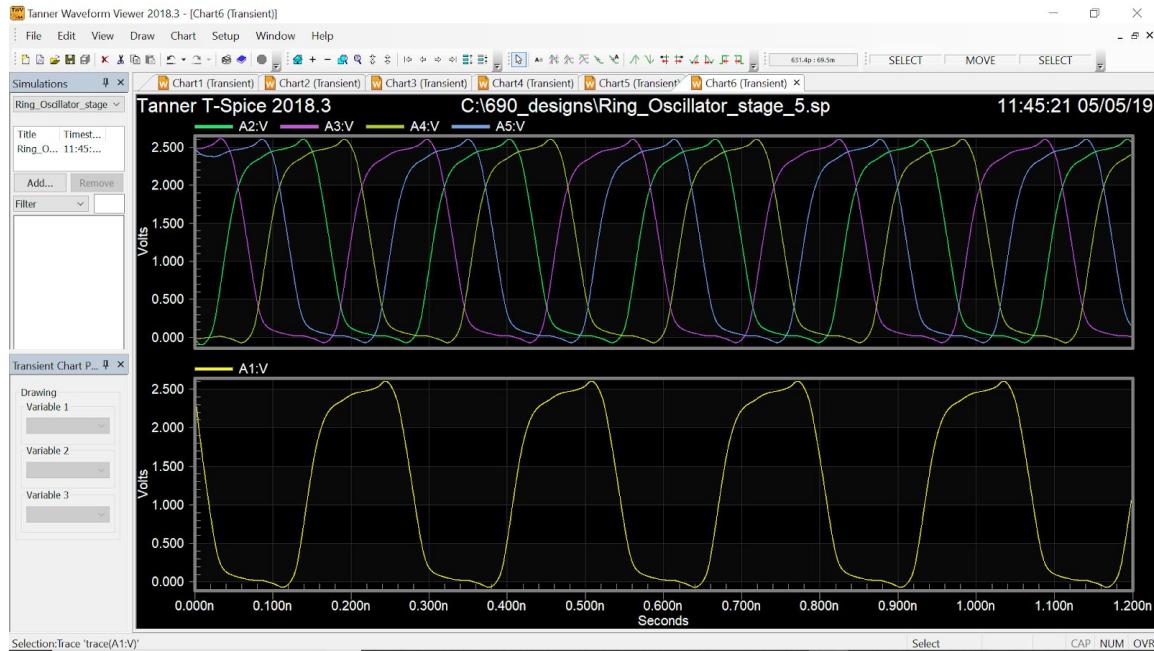
Voltage: 2.5V

Measurement result summary

Delay time = 263.5990ps A1(first rise to second rise)

Frequency of Oscillation: 3.7936411GHz

Figure 13 shows the waveform for case 4



Case 5: Temperature: -25C

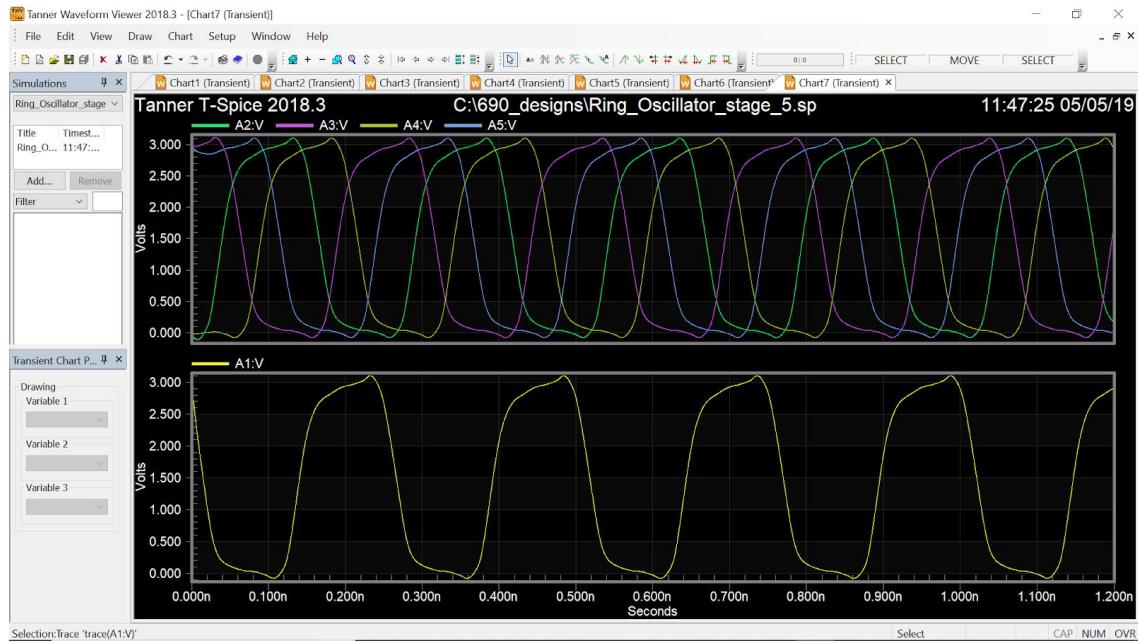
Voltage: 3V

Measurement result summary

Delay time = 251.6578ps A1(first rise to second rise)

Frequency of Oscillation: 3.97364993Ghz

Figure 14 shows the waveform for case 5



Case 6: Temperature: -25C (No much change in waveform, hence only measured the values)

Voltage: 3.5V

Measurement result summary

Delay time = 247.9547ps A1(first rise to second rise)

Frequency of Oscillation: 4.03299474GHz

Case 7: Temperature: 100C

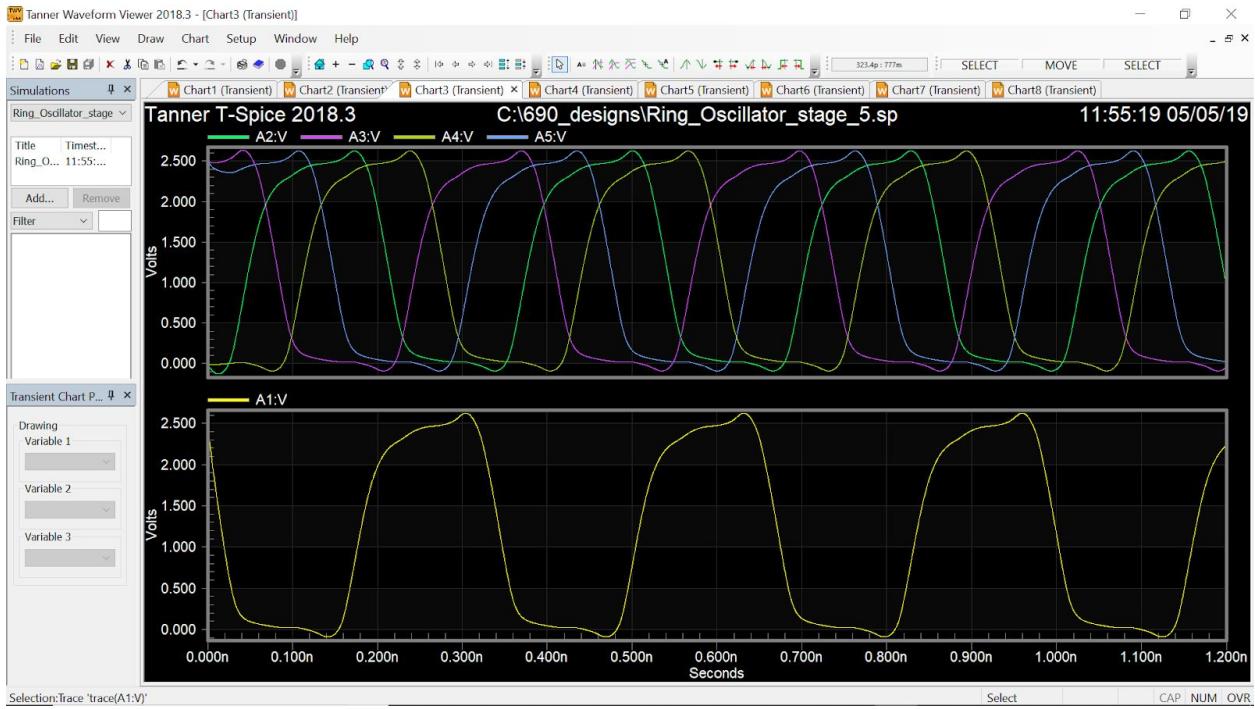
Voltage: 2.5V

Measurement result summary

Delay time = 327.6938ps A1(first rise to second rise)

Frequency of Oscillation: 3.0516293GHz

Figure 15 shows the waveform for case 7



Case 8: Temperature: 100C (No much change in waveform, hence only measured the values)

Voltage: 3V

Measurement result summary

Delay time = 283.7987ps A1(first rise to second rise)

Frequency of Oscillation: 3.52362432GHz

Case 9: Temperature: 100C (No much change in waveform, hence only measured the values)

Voltage: 3.5V

Measurement result summary

Delay time = 257.4037ps A1(first rise to second rise)

Frequency of Oscillation: 3.88494804GHz

Results with respect to change in Load Capacitance

By varying the Load capacitance value using the temperature: 25C (default) & Voltage: 3V. I have observed the frequency of oscillation change as a function of load capacitance on the output of the oscillator.

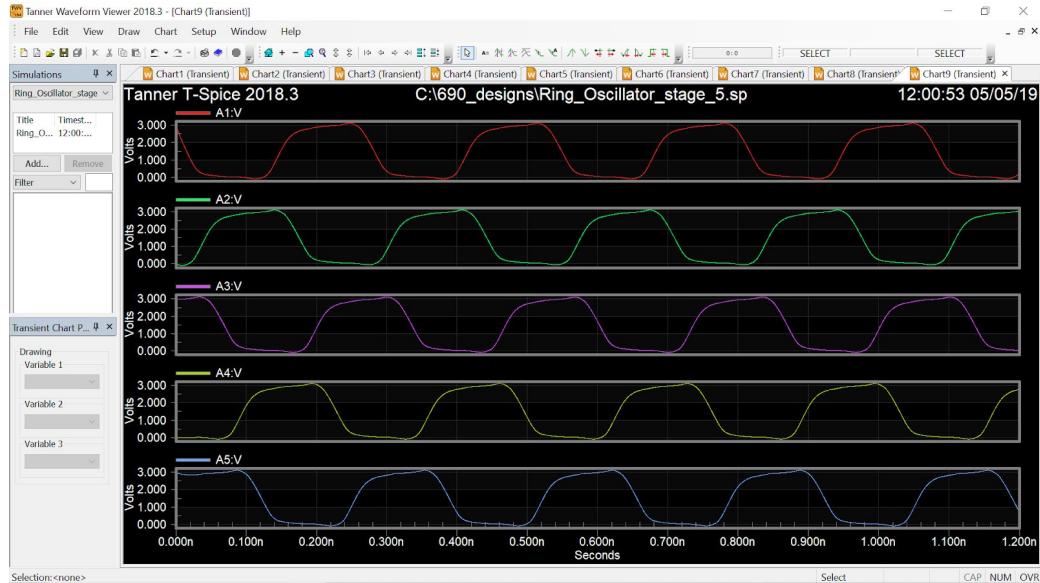
Case 1: NO Load Capacitance

Measurement result summary

Delay time = 267.0344ps A1(first rise to second rise)

Frequency of Oscillation: 3.74483587GHz

Figure 16 shows the waveform for case 1 with No load capacitance



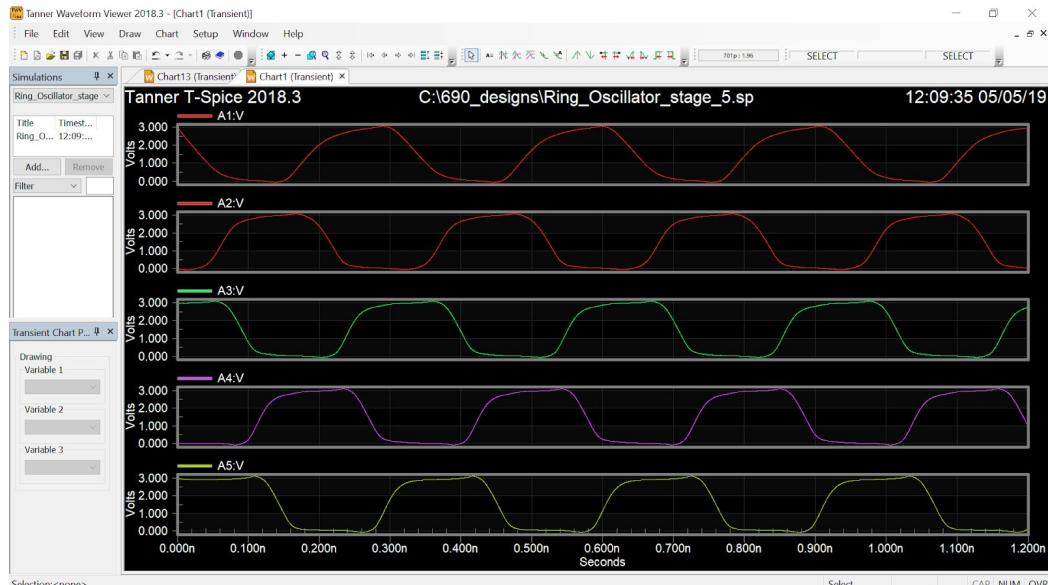
Case 2: Load Capacitance = 5fF

Measurement result summary

Delay time = 307.9766ps A2(first rise to second rise)

Frequency of Oscillation: 3.24699993GHz

Figure 16 shows the waveform for case 2 with load capacitance = 5fF



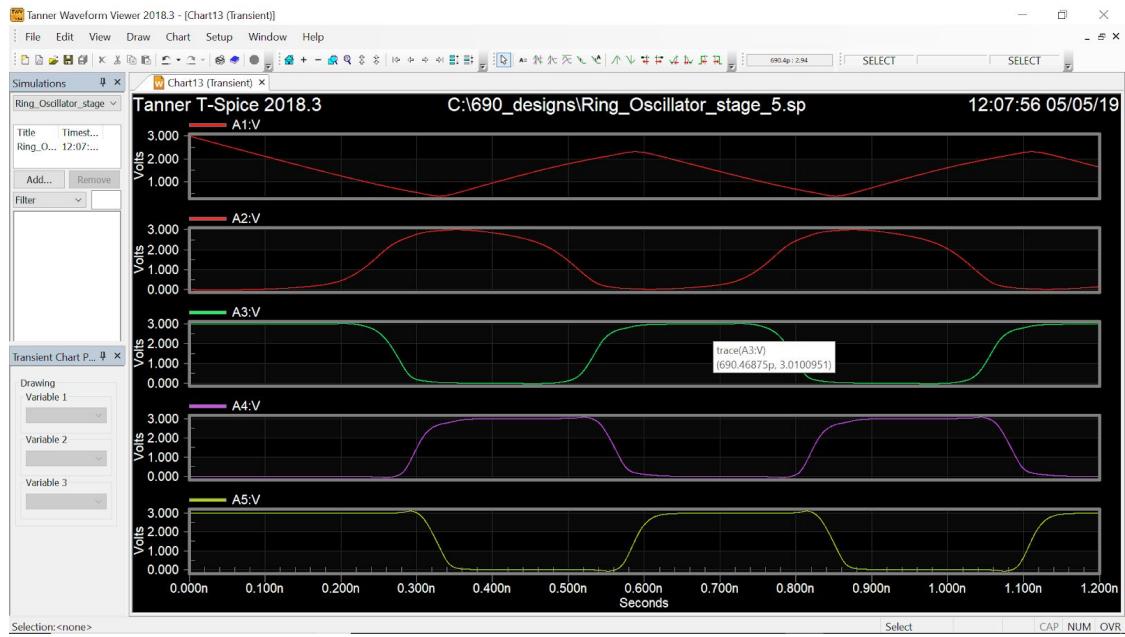
Case 3: Load Capacitance = 50fF

Measurement result summary

Delay time = 522.7194ps A2(first rise to second rise)

Frequency of Oscillation: 1.91307229GHz

Figure 17 shows the waveform for case 3 with load capacitance = 50fF



Case 4: Load Capacitance = 500fF

Measurement result summary

Delay time = 2.0518ns A3(first rise to second rise)

Frequency of Oscillation: 487.376937MHz

Figure 18 shows the waveform for case 4 with load capacitance = 500fF

