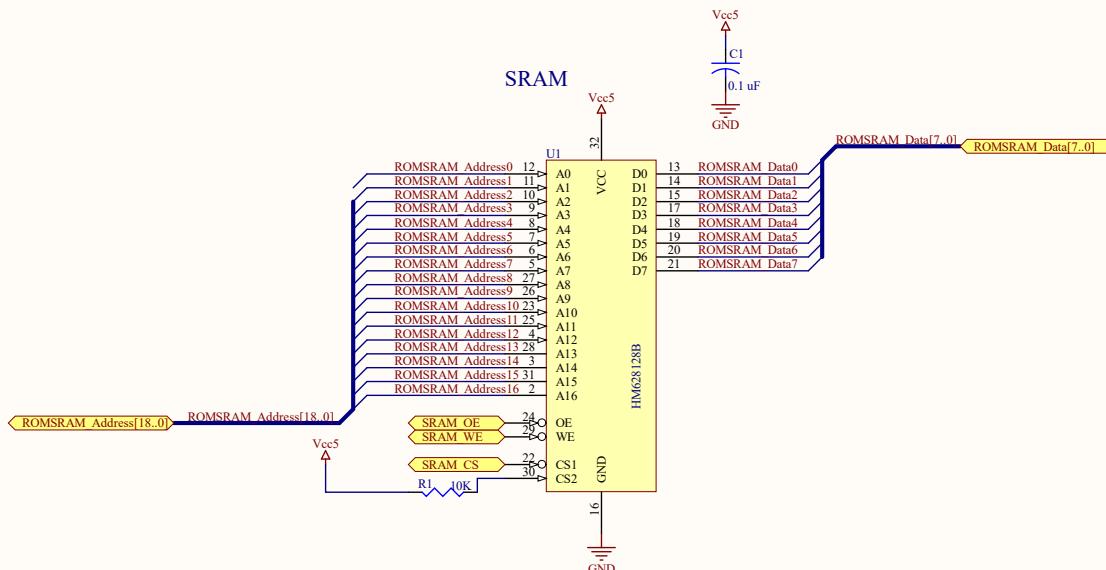


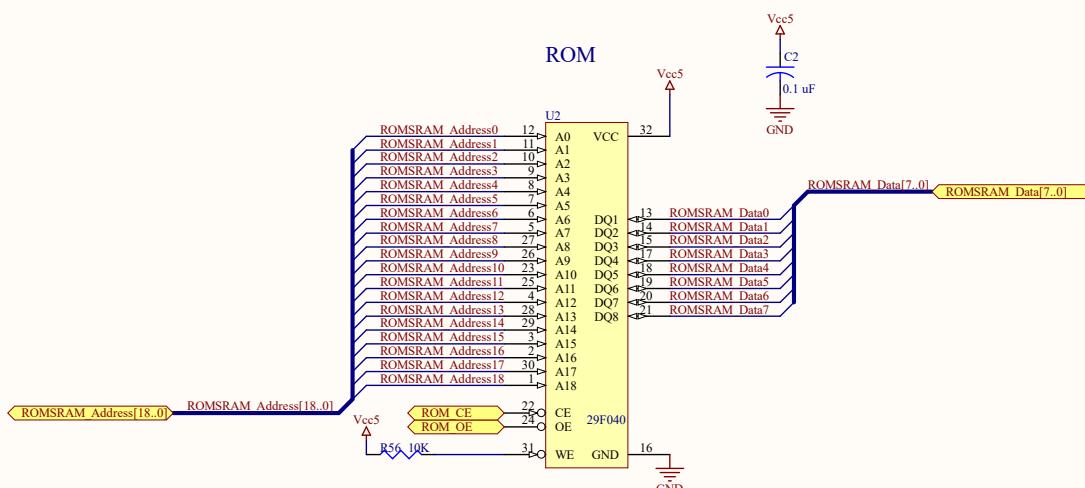
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Size	Number	Revision
D		v2.0
Date:	12/21/2011	Sheet 1 of 6
Date:	C:\Users\JFNGA\Schibec	Drawn By: Sophia Lin

A

**SRAM**

B

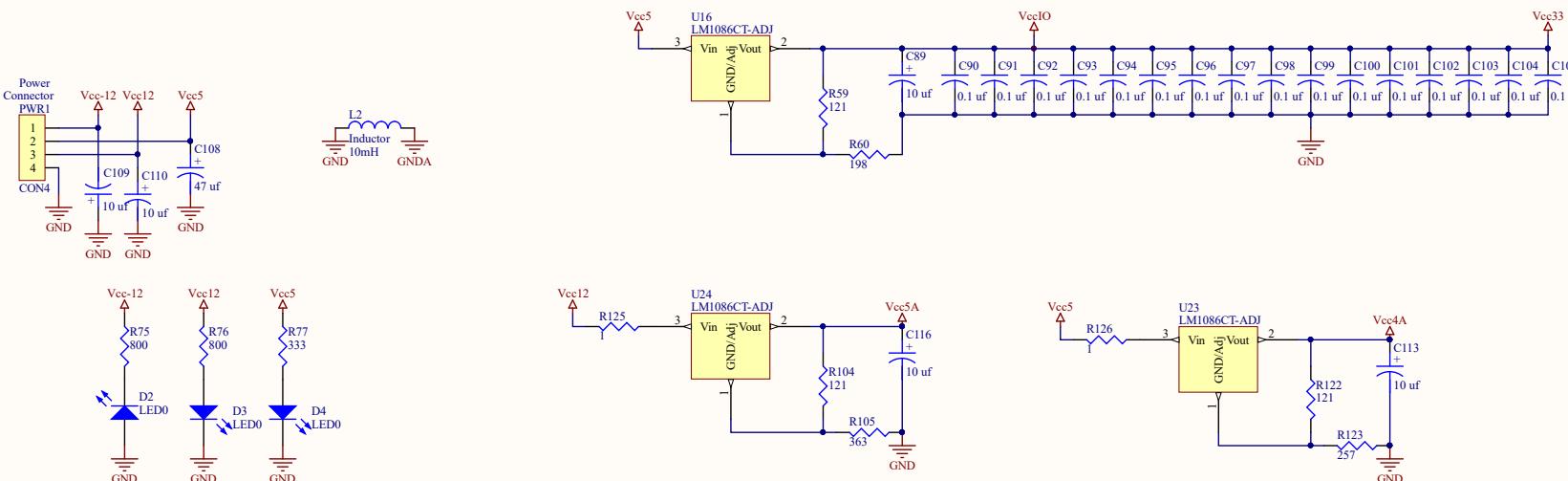
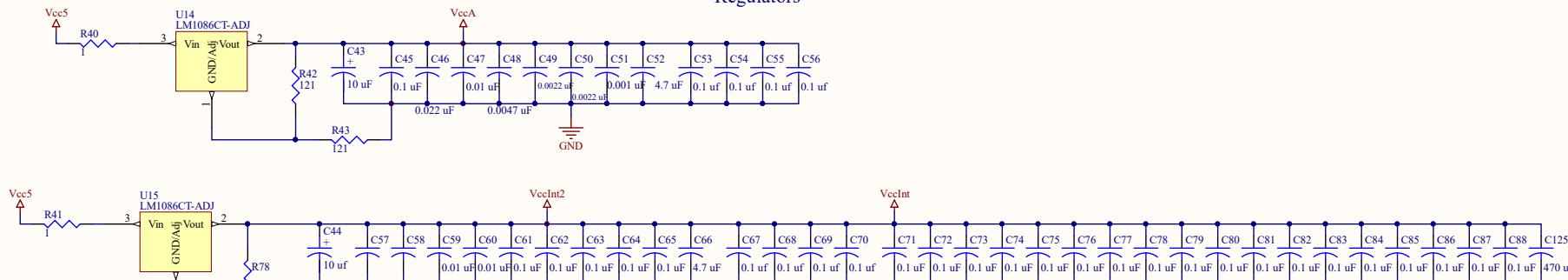
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**ROM**

C

B

Title		
SRAM and ROM		
Size	Number	Revision
B		v2.0
Date:	12/21/2017	Sheet 4 of 6
File:	C:\Users\...\Memory.SchDoc	Drawn By: Sophia Liu

**Regulators**

Title Power circuitry		Revision v2.0
Size B	Number	
Date: 12/21/2017	Sheet 3 of 6	
File: C:\Users\...\Power.SchDoc	Drawn By: Sophia Liu	

A

A

B

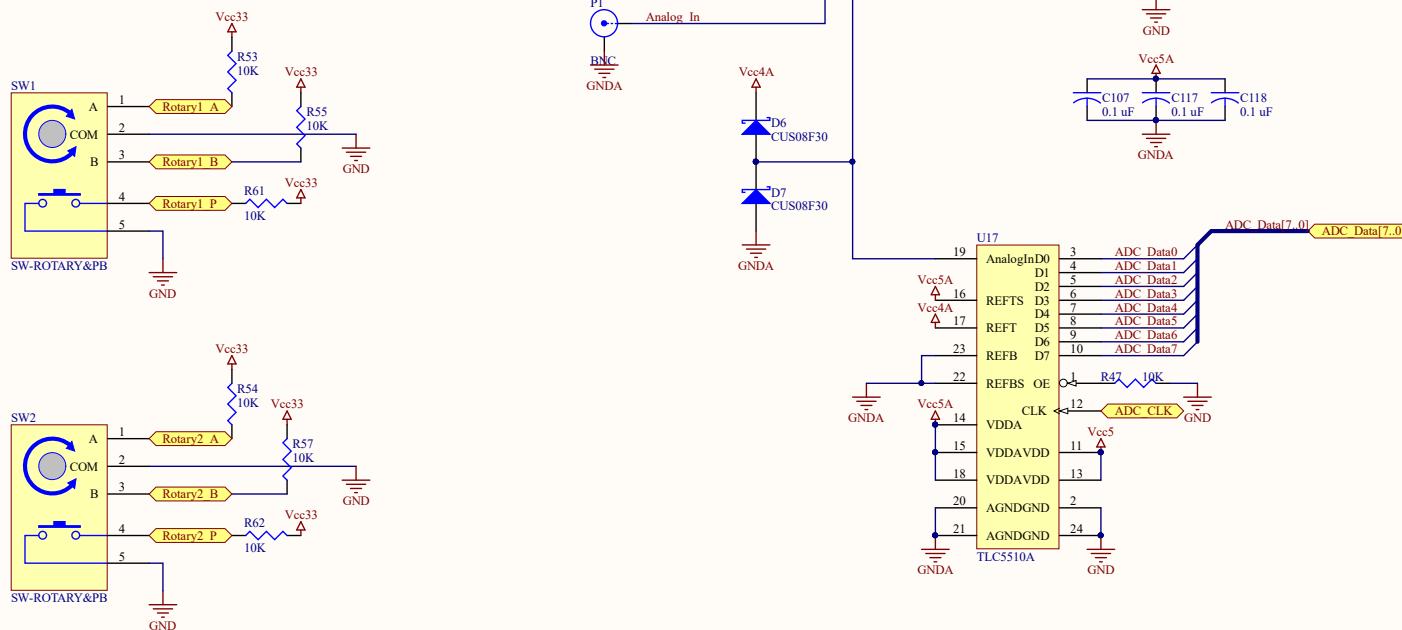
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C

C

D

D

Title  
User and Analog Input

Size	Number	Revision
		v2.0

Date: 12/21/2017

File: C:\Users\...\User\_Analog\_Input.SchDoc

Sheet 5 of 6

Drawn By: Sophia Liu

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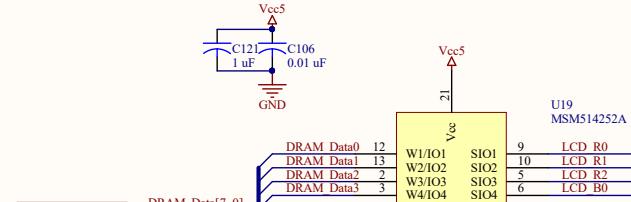
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6

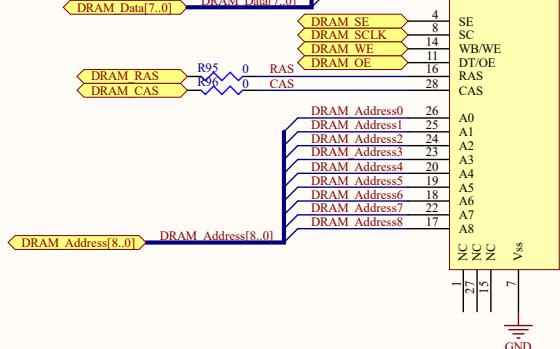
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A



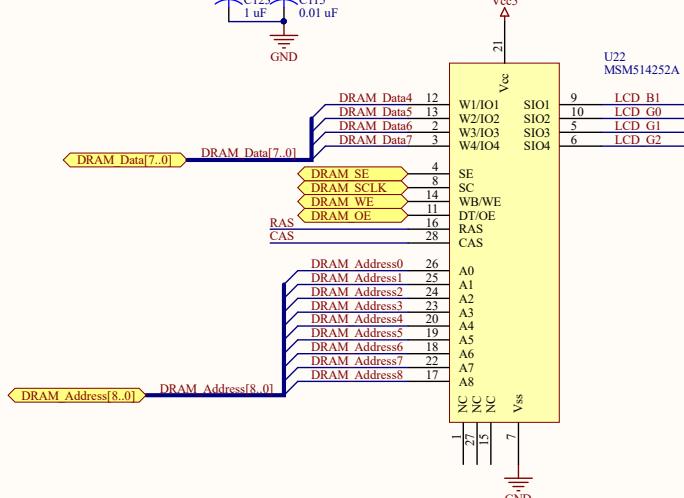
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B



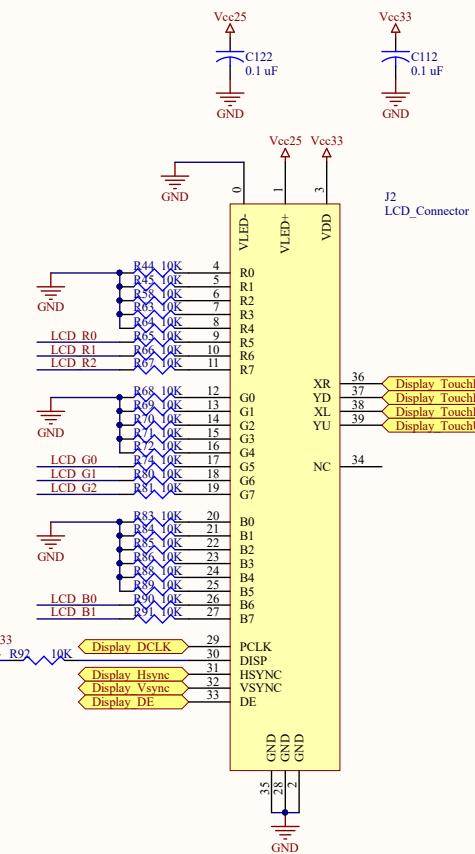
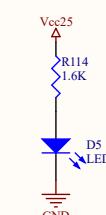
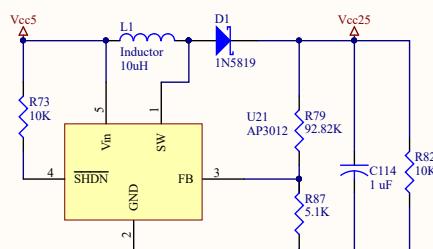
C

C



D

D



Title VRAM and LCD		
Size	Number	Revision v2.0
Date: 12/21/2017		Sheet 6 of 6
File: C:\Users\...\VRAM_LCD.SchDoc		Drawn By: Sophia Liu

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