Cyclone III Pins

Pin	Active	Direction	Connection	Use
VCCINT	N/A	N/A	1.2 V	Power
VCCIO1	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO2	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO3	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO4	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO5	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO6	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO7	N/A	N/A	3.3 V	I/O supply voltage pin
VCCIO8	N/A	N/A	3.3 V	I/O supply voltage pin
VCCA1	N/A	N/A	2.5 V	Analog power for PLL1
VCCA2	N/A	N/A	2.5 V	Analog power for PLL2
VCCA3	N/A	N/A	2.5 V	Analog power for PLL3
VCCA4	N/A	N/A	2.5 V	Analog power for PLL4
VCCD_PLL1	N/A	N/A	1.2 V	Digital power for PLL1
VCCD_PLL2	N/A	N/A	1.2 V	Digital power for PLL2
VCCD_PLL3	N/A	N/A	1.2 V	Digital power for PLL3
VCCD_PLL4	N/A	N/A	1.2 V	Digital power for PLL4
GND	N/A	N/A	Ground	Device ground pins
GNDA1	N/A	N/A	Analog Ground	PLL1, analog circuits ground
GNDA2	N/A	N/A	Analog Ground	PLL2, analog circuits ground

Pin	Active	Direction	Connection	Use
GNDA3	N/A	N/A	Analog Ground	PLL3, analog circuits ground
GNDA4	N/A	N/A	Analog Ground	PLL4, analog circuits ground
CLK0/DIFFCLK_0p	N/A	Input	Clock	Clock input
CLK1/DIFFCLK_0n	N/A	Input	Clock	Backup clock input
CLK2/DIFFCLK_1p	N/A	Input	Ground	Unused, connect to ground
CLK3/DIFFCLK_1n	N/A	Input	Ground	Unused, connect to ground
CLK4/DIFFCLK_2p	N/A	Input	Ground	Unused, connect to ground

CLK5/DIFFCLK_2n	N/A	Input	Ground	Unused, connect to ground
CLK6/DIFFCLK_3p	N/A	Input	Ground	Unused, connect to ground
CLK7/DIFFCLK_3n	N/A	Input	Ground	Unused, connect to ground
CLK8/DIFFCLK_5n	N/A	Input	Ground	Unused, connect to ground
CLK9/DIFFCLK_5p	N/A	Input	Ground	Unused, connect to ground
CLK10/DIFFCLK_4n	N/A	Input	Ground	Unused, connect to ground
CLK11/DIFFCLK_4p	N/A	Input	Ground	Unused, connect to ground
CLK12/DIFFCLK_7n	N/A	Input	Ground	Unused, connect to ground
CLK13/DIFFCLK_7p	N/A	Input	Ground	Unused, connect to ground
CLK14/DIFFCLK_6n	N/A	Input	Ground	Unused, connect to ground
CLK15/DIFFCLK_6p	N/A	Input	Ground	Unused, connect to ground
nCE	Low	Input	Ground	Active-low chip enable, tie to ground to enable
nCONFIG	Low	Input	VCCIO	Configuration control input, connect to VCCIO (resets at low)
nSTATUS	N/A	Bi	Pull high	Configuration status pin, pull high

Pin	Active	Direction	Connection	Use
CONF_DONE	N/A	Bi	Pull high	Configuration status pin, pull high
DATA0	N/A	Input	Serial	Serial config device DATA pin
DCLK	N/A	Output	Serial	Serial config device DCLK pin
MSEL0	N/A	Input	Mode select	Configuration input pin
MSEL1	N/A	Input	Mode select	Configuration input pin
MSEL2	N/A	Input	Mode select	Configuration input pin
TCK	High	Input	JTAG	JTAG input pin
TDI	High	Input	JTAG	JTAG input pin
TDO	High	Output	JTAG	JTAG output pin
TMS	High	Input	JTAG	JTAG input pin
IO4/DIFFIO_L1p	High	Output	ROM	ROM output enable
IO5/DIFFIO_L1n	High	Output	ROM	ROM chip enable
IO6	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO9	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO12/DATA1	N/A	Output	Serial	Serial config device ASDO, used to read out configuration data
IO13/VREFB1N0	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO14/FLASH_nCE/nCS0	N/A	Output	Serial	Serial config device nCSO, output control signal to enable config device
IO18	N/A	Output	ROM/SRAM	ROM/SRAM address bus

IO21/DIFFIO_L6p	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO22/DIFFIO_L6n	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO37/DIFFIO_L8p	N/A	Output	ROM/SRAM	ROM/SRAM address bus

Pin	Active	Direction	Connection	Use
IO38/DIFFIO_L8n	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO39	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO41/DIFFIO_L10p	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO43/DIFFIO_L10n	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO44/DIFFIO_L11p	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO45/DIFFIO_L11n	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO46/VREFB2N0	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO49/DIFFIO_L13p	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO50/DIFFIO_L13n	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO51/RUP1	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO52/RDN1	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO55	N/A	Output	ROM/SRAM	ROM/SRAM address bus
IO56/DIFFIO_L15p	Low	Output	SRAM	SRAM write enable input
IO57/DIFFIO_L15n	Low	Output	SRAM	SRAM output enable input
IO63/DIFFIO_B2p	Low	Output	SRAM	SRAM chip select input
IO64/DIFFIO_B2n	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO65	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO68	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO69/PLL1_CLKOUTp	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO70/PLL1_CLKOUTn	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO71/DIFFIO_B4p	N/A	I/O	ROM/SRAM	ROM/SRAM data bus

Pin	Active	Direction	Connection	Use
IO72/DIFFIO_B4n	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO73	N/A	I/O	ROM/SRAM	ROM/SRAM data bus
IO76/VREFB3N0	High	Output	Buffer	ROM/SRAM data bus direction
IO78	N/A	I/O	DRAM	DRAM data bus
IO80	N/A	I/O	DRAM	DRAM data bus
IO81/DIFFIO_B7p	N/A	I/O	DRAM	DRAM data bus
IO82/DIFFIO_B7n	N/A	I/O	DRAM	DRAM data bus
IO83	N/A	I/O	DRAM	DRAM data bus

IO84	N/A	I/O	DRAM	DRAM data bus
IO87	N/A	I/O	DRAM	DRAM data bus
IO88	N/A	I/O	DRAM	DRAM data bus
IO93/DIFFIO_B13p	High	Output	Buffer	DRAM data bus direction
IO94/DIFFIO_B13n	N/A	Output	DRAM	DRAM address bus 2
IO95	N/A	Output	DRAM	DRAM address bus 3
IO98/DIFFIO_B16p	N/A	Output	DRAM	DRAM address bus 4
IO99/DIFFIO_B16n	N/A	Output	DRAM	DRAM address bus 5
IO100	N/A	Output	DRAM	DRAM address bus 6
IO103	N/A	Output	DRAM	DRAM address bus 7
IO106	N/A	Output	DRAM	DRAM address bus 8
IO107/VREFB4N0	N/A	Output	DRAM	DRAM address bus 9
IO108/DIFFIO_B20p	N/A	Output	DRAM	DRAM address bus 9

Pin	Active	Direction	Connection	Use
IO109/DIFFIO_B20n	Low	Output	DRAM	DRAM CAS
IO110	Low	Output	DRAM	DRAM RAS
IO111/RUP2	Low	Output	DRAM	DRAM mask enable/write enable
IO112/RDN2	Low	Output	DRAM	DRAM data transfer/output enable
IO113	N/A	Output	DRAM	DRAM serial clock input
IO114	Low	Output	DRAM	DRAM serial port enable
IO117/PLL4_CLKOUTp	High	Output	Buffer	Buffer direction
IO118/PLL4_CLKOUTn	N/A	I/O	Buffer	Extra I/O
IO119/DIFFIO_B25p	N/A	I/O	Buffer	Extra I/O
IO120/DIFFIO_B25n	N/A	I/O	Buffer	Extra I/O
IO126/RUP3	N/A	I/O	Buffer	Extra I/O
IO127/RDN3	N/A	I/O	Buffer	Extra I/O
IO128	N/A	I/O	Buffer	Extra I/O
IO131/DIFFIO_R13n	N/A	I/O	Buffer	Extra I/O
IO132/DIFFIO_R13p	N/A	I/O	Buffer	Extra I/O
IO133/VREFB5N0	N/A	I/O	Buffer	Extra I/O
IO134/DIFFIO_R12n	N/A	I/O	Buffer	Extra I/O
IO135/DIFFIO_R12p	N/A	I/O	Buffer	Extra I/O
IO137/DIFFIO_R11n	N/A	I/O	Buffer	Extra I/O
IO139/DIFFIO_R11p	N/A	I/O	Buffer	Extra I/O
IO142/DIFFIO_R10n	N/A	I/O	Buffer	Extra I/O

Pin	Active	Direction	Connection	Use
IO143/DIFFIO_R10p	N/A	I/O	Buffer	Extra I/O
IO144/DIFFIO_R9n/ DEV_OE	N/A	I/O	Buffer	Extra I/O
IO145/DIFFIO_R9p/ DEV_CLRn	High	Output	Buffer	Buffer direction
IO146	High	Input	Display	Display touch panel right
IO147/DIFFIO_R7n	High	Input	Display	Display touch panel down
IO148/DIFFIO_R7p	High	Input	Display	Display touch panel left
IO159/DIFFIO_R5n/ INIT_DONE	N/A	Output	VCCIO	Status pin
IO160/DIFFIO_R5p/ CRC_ERROR	High	Input	Display	Display touch panel up
IO161	Low	Input	Reset chip	Reset watchdog output
IO162/DIFFIO_R4n/nCEO	Low	Input	Reset chip	Reset signal
IO164/DIFFIO_R4p/ CLKUSR	Low	Input	Reset chip	Reset power-fail output
IO166	N/A	Output	Reset chip	Reset watchdog input
IO167/DIFFIO_R3n	N/A	Output	Display	Display DCLK
IO168/DIFFIO_R3p	N/A	Output	Display	Display HSYNC signal
IO169/VREFB6N0	N/A	Output	Display	Display VSYNC signal
IO171	High	Output	Display	Display data enable
IO173	N/A	Output	Buffer	Extra I/O
IO176/DIFFIO_R1n	N/A	Output	Buffer	Extra I/O
IO177/DIFFIO_R1p	N/A	Output	Buffer	Extra I/O
IO181	N/A	Input	Rotary encoder 1	Rotary A
IO182/DIFFIO_T23n	N/A	Input	Rotary encoder 1	Rotary B

Pin	Active	Direction	Connection	Use
IO183/DIFFIO_T23p	High	Input	Rotary encoder 1	Rotary Press
IO184	N/A	Input	Rotary encoder 2	Rotary A
IO185/PLL2_CLKOUTn	N/A	Input	Rotary encoder 2	Rotary B
IO186/PLL2_CLKOUTp	High	Input	Rotary encoder 2	Rotary Press
IO187/RUP4	N/A	Input	Buffer	Extra I/O
IO188/RDN4	N/A	Input	Buffer	Extra I/O
IO189	N/A	I/O	Buffer	Extra I/O
IO194	N/A	I/O	Buffer	Extra I/O
IO195/VREFB7N0	N/A	I/O	Buffer	Extra I/O
IO196/DIFFIO_T19n	N/A	I/O	Buffer	Extra I/O

IO197/DIFFIO_T19p	N/A	I/O	Buffer	Extra I/O
IO200	N/A	I/O	Buffer	Extra I/O
IO201	N/A	I/O	Buffer	Extra I/O
IO202/DIFFIO_T15n	N/A	I/O	Buffer	Extra I/O
IO203/DIFFIO_T15p	High	Output	Buffer	Buffer direction
IO207	High	Output	Buffer	Buffer direction
IO214	N/A	I/O	Buffer	Extra I/O
IO216	N/A	I/O	Buffer	Extra I/O
IO217	N/A	I/O	Buffer	Extra I/O
IO218/DIFFIO_T10n/ DATA2	N/A	I/O	None	Unused, leave unconnected
IO219/DIFFIO_T10p/ DATA3	N/A	I/O	None	Unused, leave unconnected

Pin	Active	Direction	Connection	Use
IO221/DATA4	N/A	I/O	None	Unused, leave unconnected
IO223/VREFB8N0	N/A	I/O	Buffer	Extra I/O
IO224	N/A	I/O	Buffer	Extra I/O
IO226/DATA5	N/A	I/O	None	Unused, leave unconnected
IO230/DIFFIO_T6n	N/A	I/O	DRAM	ADC data bus
IO231/DIFFIO_T6p/ DATA6	N/A	I/O	None	Unused, leave unconnected
IO232/DATA7	N/A	I/O	None	Unused, leave unconnected
IO233	N/A	I/O	DRAM	ADC data bus
IO234/DIFFIO_T2n	N/A	I/O	DRAM	ADC data bus
IO235/DIFFIO_T2p	N/A	I/O	DRAM	ADC data bus
IO236	N/A	I/O	DRAM	ADC data bus
IO237/DIFFIO_T1n	N/A	I/O	DRAM	ADC data bus
IO238/DIFFIO_T1p	N/A	I/O	DRAM	ADC data bus
IO239/PLL3_CLKOUTn	N/A	I/O	DRAM	ADC data bus
IO240/PLL3_CLKOUTp	High	Output	ADC	ADC clock input