Sitronix

ST7037-G4

4 x 320 Dot LCD Controller/Driver

1. INTRODUCTION

The ST7037 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 320 segment and 4 common driver circuits. This chip is connected directly to a microprocessor, accepts 4-line/3-line serial peripheral interface (SPI) and 8080 parallel interface, display data can stores in an on-chip display data RAM of 4 x 320 x 3bits. It performs display data RAM read/write operation with no external operating clock to minimize power consumption.

2. FEATURES

Single-chip LCD Controller & Driver

Driver Output Circuits

320 segment outputs / 4 common

On-chip Display Data Ram

- Capacity: 4X320x3=3840bits
- Four gray display is available

Microprocessor Interface

- 8 bi-directional parallel interface with 8080-series
- 3-line SPI (9-bits) , 4-line(8bits) serial peripheral interface

On-chip Low Power Analog Circuit

- Generation of LCD supply voltage (externally V0IN voltage supply is possible)
- Generation of intermediate LCD bias voltages
- Oscillator requires no external components
- Voltage converter (x2~x4)
- Voltage regulator
- Voltage follower

With External /RST (reset) pin

Logic Supply Voltage Range

- VDDI (VDD, VDD1)-VSS：2.8V~3.3V
- VDDA (VDD2, VDD3)-VSS：2.8V~3.3V

LCD Driving Voltage Range (VOP=V0-VSS)

- 6 V to 13.2 V
- For one duty application, the VOP range can be down to 3V
- LCD frame frequency Max:150HZ

Support Master/Slave

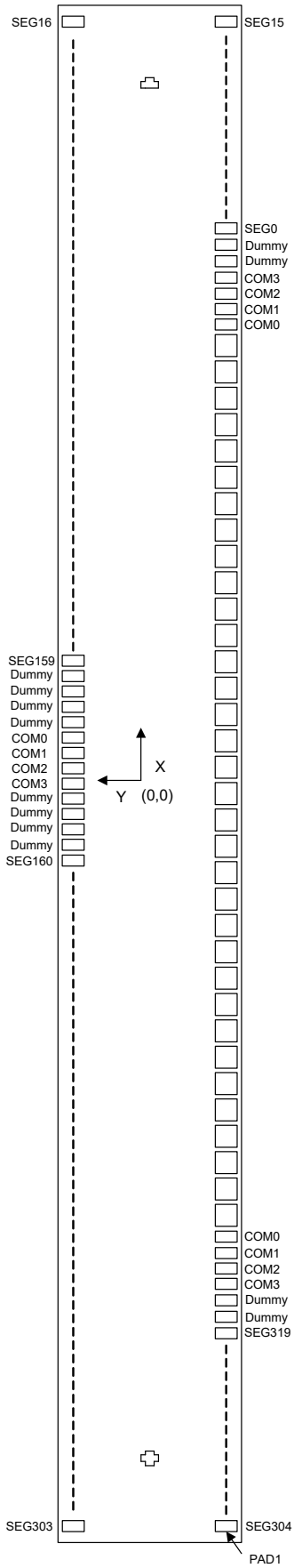
Temperature Range : -30 ~85℃

Package Type :COG

Design for consumer applications; this product is not designed for use in cars, motorcycles, marine equipment, aircraft equipment, military equipment and other applications in extreme environment.

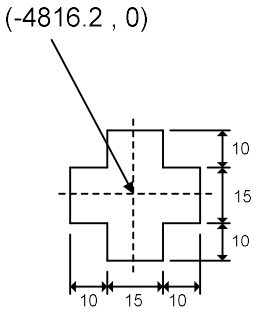
ST7037-G4	8080 8bit parallel interface 4-Line , 3-Line serial interface	ST

3. ST7037 Pad Arrangement (COG)

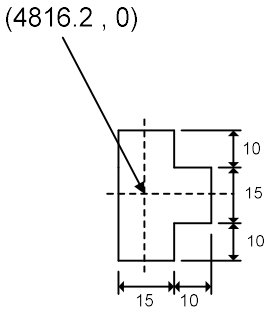


Unit:um

Part Number	ST7037-G4
Chip Size	10056 x 706
Bump Height	15
Thickness	300
Bump Size	
PAD No.	**Size**
1~22 , 124~445	17 x 112.5
23~34	63 x 57
35~43 , 46~123	68 x 52
44 , 45	25.5 x 52
Bump Space	
1~22 , 124~445	16
23~34 , 35~123	17
22-23 , 123-124	20.5



L-Mark



R-Mark

4. Pad Center Coordinates

NO.	NAME	X	Y
1	SEG304	-4933.5	-237.75
2	SEG305	-4900.5	-237.75
3	SEG306	-4867.5	-237.75
4	SEG307	-4834.5	-237.75
5	SEG308	-4801.5	-237.75
6	SEG309	-4768.5	-237.75
7	SEG310	-4735.5	-237.75
8	SEG311	-4702.5	-237.75
9	SEG312	-4669.5	-237.75
10	SEG313	-4636.5	-237.75
11	SEG314	-4603.5	-237.75
12	SEG315	-4570.5	-237.75
13	SEG316	-4537.5	-237.75
14	SEG317	-4504.5	-237.75
15	SEG318	-4471.5	-237.75
16	SEG319	-4438.5	-237.75
17	Dummy	-4405.5	-237.75
18	Dummy	-4372.5	-237.75
19	COM3	-4339.5	-237.75
20	COM2	-4306.5	-237.75
21	COM1	-4273.5	-237.75
22	COM0	-4240.5	-237.75
23	T11	-4180	-265.5
24	T10	-4100	-265.5
25	T9	-4020	-265.5
26	T8	-3940	-265.5
27	T7	-3860	-265.5
28	T6	-3780	-265.5
29	T0	-3700	-265.5
30	T5	-3620	-265.5
31	T4	-3540	-265.5
32	T3	-3460	-265.5
33	T2	-3380	-265.5
34	T1	-3300	-265.5
35	SYNC	-3217.5	-268
36	Dummy	-3132.5	-268
37	Dummy	-3047.5	-268
38	Dummy	-2962.5	-268
39	IF2	-2877.5	-268
40	IF1	-2792.5	-268
41	CL	-2707.5	-268
42	MS	-2622.5	-268
43	DON	-2537.5	-268
44	VSS	-2473.75	-268
45	VDD	-2431.25	-268
46	/RST	-2367.5	-268

NO.	NAME	X	Y
47	/CS	-2282.5	-268
48	/WR	-2197.5	-268
49	/RD	-2112.5	-268
50	A0	-2027.5	-268
51	D0	-1942.5	-268
52	D1	-1857.5	-268
53	D2	-1772.5	-268
54	D3	-1687.5	-268
55	D4	-1602.5	-268
56	D5	-1517.5	-268
57	D6	-1432.5	-268
58	D7	-1347.5	-268
59	VDD	-1262.5	-268
60	VDD	-1177.5	-268
61	VDD	-1092.5	-268
62	VDD	-1007.5	-268
63	VDD1	-922.5	-268
64	VDD1	-837.5	-268
65	VDD2	-752.5	-268
66	VDD2	-667.5	-268
67	VDD2	-582.5	-268
68	VDD2	-497.5	-268
69	VDD3	-412.5	-268
70	VDD3	-327.5	-268
71	VSS	-242.5	-268
72	VSS	-157.5	-268
73	VSS	-72.5	-268
74	VSS	12.5	-268
75	VSS1	97.5	-268
76	VSS1	182.5	-268
77	VSS3	267.5	-268
78	VSS3	352.5	-268
79	VSS2	437.5	-268
80	VSS2	522.5	-268
81	VSS2	607.5	-268
82	VSS2	692.5	-268
83	Vref	777.5	-268
84	V1	862.5	-268
85	V1	947.5	-268
86	V2	1032.5	-268
87	V2	1117.5	-268
88	V3	1202.5	-268
89	V3	1287.5	-268
90	V4	1372.5	-268
91	V4	1457.5	-268
92	V0OUT	1542.5	-268

NO.	NAME	X	Y
93	V0OUT	1627.5	-268
94	V0IN	1712.5	-268
95	V0IN	1797.5	-268
96	V0IN	1882.5	-268
97	V0IN	1967.5	-268
98	CAPX	2052.5	-268
99	CAPX	2137.5	-268
100	CAP1N	2222.5	-268
101	CAP1N	2307.5	-268
102	CAP3P	2392.5	-268
103	CAP3P	2477.5	-268
104	CAP1N	2562.5	-268
105	CAP1N	2647.5	-268
106	CAP1P	2732.5	-268
107	CAP1P	2817.5	-268
108	CAP2P	2902.5	-268
109	CAP2P	2987.5	-268
110	CAP2N	3072.5	-268
111	CAP2N	3157.5	-268
112	CAPX	3242.5	-268
113	CAPX	3327.5	-268
114	CAP2N	3412.5	-268
115	CAP2N	3497.5	-268
116	Dummy	3582.5	-268
117	Dummy	3667.5	-268
118	VLCDOUT	3752.5	-268
119	VLCDOUT	3837.5	-268
120	VLCDIN	3922.5	-268
121	VLCDIN	4007.5	-268
122	VLCDIN	4092.5	-268
123	VLCDIN	4177.5	-268
124	COM0	4240.5	-237.75
125	COM1	4273.5	-237.75
126	COM2	4306.5	-237.75
127	COM3	4339.5	-237.75
128	Dummy	4372.5	-237.75
129	Dummy	4405.5	-237.75
130	SEG0	4438.5	-237.75
131	SEG1	4471.5	-237.75
132	SEG2	4504.5	-237.75
133	SEG3	4537.5	-237.75
134	SEG4	4570.5	-237.75
135	SEG5	4603.5	-237.75
136	SEG6	4636.5	-237.75
137	SEG7	4669.5	-237.75
138	SEG8	4702.5	-237.75
139	SEG9	4735.5	-237.75
140	SEG10	4768.5	-237.75

NO.	NAME	X	Y
141	SEG11	4801.5	-237.75
142	SEG12	4834.5	-237.75
143	SEG13	4867.5	-237.75
144	SEG14	4900.5	-237.75
145	SEG15	4933.5	-237.75
146	SEG16	4933.5	237.75
147	SEG17	4900.5	237.75
148	SEG18	4867.5	237.75
149	SEG19	4834.5	237.75
150	SEG20	4801.5	237.75
151	SEG21	4768.5	237.75
152	SEG22	4735.5	237.75
153	SEG23	4702.5	237.75
154	SEG24	4669.5	237.75
155	SEG25	4636.5	237.75
156	SEG26	4603.5	237.75
157	SEG27	4570.5	237.75
158	SEG28	4537.5	237.75
159	SEG29	4504.5	237.75
160	SEG30	4471.5	237.75
161	SEG31	4438.5	237.75
162	SEG32	4405.5	237.75
163	SEG33	4372.5	237.75
164	SEG34	4339.5	237.75
165	SEG35	4306.5	237.75
166	SEG36	4273.5	237.75
167	SEG37	4240.5	237.75
168	SEG38	4207.5	237.75
169	SEG39	4174.5	237.75
170	SEG40	4141.5	237.75
171	SEG41	4108.5	237.75
172	SEG42	4075.5	237.75
173	SEG43	4042.5	237.75
174	SEG44	4009.5	237.75
175	SEG45	3976.5	237.75
176	SEG46	3943.5	237.75
177	SEG47	3910.5	237.75
178	SEG48	3877.5	237.75
179	SEG49	3844.5	237.75
180	SEG50	3811.5	237.75
181	SEG51	3778.5	237.75
182	SEG52	3745.5	237.75
183	SEG53	3712.5	237.75
184	SEG54	3679.5	237.75
185	SEG55	3646.5	237.75
186	SEG56	3613.5	237.75
187	SEG57	3580.5	237.75
188	SEG58	3547.5	237.75

NO.	NAME	X	Y
189	SEG59	3514.5	237.75
190	SEG60	3481.5	237.75
191	SEG61	3448.5	237.75
192	SEG62	3415.5	237.75
193	SEG63	3382.5	237.75
194	SEG64	3349.5	237.75
195	SEG65	3316.5	237.75
196	SEG66	3283.5	237.75
197	SEG67	3250.5	237.75
198	SEG68	3217.5	237.75
199	SEG69	3184.5	237.75
200	SEG70	3151.5	237.75
201	SEG71	3118.5	237.75
202	SEG72	3085.5	237.75
203	SEG73	3052.5	237.75
204	SEG74	3019.5	237.75
205	SEG75	2986.5	237.75
206	SEG76	2953.5	237.75
207	SEG77	2920.5	237.75
208	SEG78	2887.5	237.75
209	SEG79	2854.5	237.75
210	SEG80	2821.5	237.75
211	SEG81	2788.5	237.75
212	SEG82	2755.5	237.75
213	SEG83	2722.5	237.75
214	SEG84	2689.5	237.75
215	SEG85	2656.5	237.75
216	SEG86	2623.5	237.75
217	SEG87	2590.5	237.75
218	SEG88	2557.5	237.75
219	SEG89	2524.5	237.75
220	SEG90	2491.5	237.75
221	SEG91	2458.5	237.75
222	SEG92	2425.5	237.75
223	SEG93	2392.5	237.75
224	SEG94	2359.5	237.75
225	SEG95	2326.5	237.75
226	SEG96	2293.5	237.75
227	SEG97	2260.5	237.75
228	SEG98	2227.5	237.75
229	SEG99	2194.5	237.75
230	SEG100	2161.5	237.75
231	SEG101	2128.5	237.75
232	SEG102	2095.5	237.75
233	SEG103	2062.5	237.75
234	SEG104	2029.5	237.75
235	SEG105	1996.5	237.75
236	SEG106	1963.5	237.75

NO.	NAME	X	Y
237	SEG107	1930.5	237.75
238	SEG108	1897.5	237.75
239	SEG109	1864.5	237.75
240	SEG110	1831.5	237.75
241	SEG111	1798.5	237.75
242	SEG112	1765.5	237.75
243	SEG113	1732.5	237.75
244	SEG114	1699.5	237.75
245	SEG115	1666.5	237.75
246	SEG116	1633.5	237.75
247	SEG117	1600.5	237.75
248	SEG118	1567.5	237.75
249	SEG119	1534.5	237.75
250	SEG120	1501.5	237.75
251	SEG121	1468.5	237.75
252	SEG122	1435.5	237.75
253	SEG123	1402.5	237.75
254	SEG124	1369.5	237.75
255	SEG125	1336.5	237.75
256	SEG126	1303.5	237.75
257	SEG127	1270.5	237.75
258	SEG128	1237.5	237.75
259	SEG129	1204.5	237.75
260	SEG130	1171.5	237.75
261	SEG131	1138.5	237.75
262	SEG132	1105.5	237.75
263	SEG133	1072.5	237.75
264	SEG134	1039.5	237.75
265	SEG135	1006.5	237.75
266	SEG136	973.5	237.75
267	SEG137	940.5	237.75
268	SEG138	907.5	237.75
269	SEG139	874.5	237.75
270	SEG140	841.5	237.75
271	SEG141	808.5	237.75
272	SEG142	775.5	237.75
273	SEG143	742.5	237.75
274	SEG144	709.5	237.75
275	SEG145	676.5	237.75
276	SEG146	643.5	237.75
277	SEG147	610.5	237.75
278	SEG148	577.5	237.75
279	SEG149	544.5	237.75
280	SEG150	511.5	237.75
281	SEG151	478.5	237.75
282	SEG152	445.5	237.75
283	SEG153	412.5	237.75
284	SEG154	379.5	237.75

NO.	NAME	X	Y
285	SEG155	346.5	237.75
286	SEG156	313.5	237.75
287	SEG157	280.5	237.75
288	SEG158	247.5	237.75
289	SEG159	214.5	237.75
290	Dummy	181.5	237.75
291	Dummy	148.5	237.75
292	Dummy	115.5	237.75
293	Dummy	82.5	237.75
294	COM0	49.5	237.75
295	COM1	16.5	237.75
296	COM2	-16.5	237.75
297	COM3	-49.5	237.75
298	Dummy	-82.5	237.75
299	Dummy	-115.5	237.75
300	Dummy	-148.5	237.75
301	Dummy	-181.5	237.75
302	SEG160	-214.5	237.75
303	SEG161	-247.5	237.75
304	SEG162	-280.5	237.75
305	SEG163	-313.5	237.75
306	SEG164	-346.5	237.75
307	SEG165	-379.5	237.75
308	SEG166	-412.5	237.75
309	SEG167	-445.5	237.75
310	SEG168	-478.5	237.75
311	SEG169	-511.5	237.75
312	SEG170	-544.5	237.75
313	SEG171	-577.5	237.75
314	SEG172	-610.5	237.75
315	SEG173	-643.5	237.75
316	SEG174	-676.5	237.75
317	SEG175	-709.5	237.75
318	SEG176	-742.5	237.75
319	SEG177	-775.5	237.75
320	SEG178	-808.5	237.75
321	SEG179	-841.5	237.75
322	SEG180	-874.5	237.75
323	SEG181	-907.5	237.75
324	SEG182	-940.5	237.75
325	SEG183	-973.5	237.75
326	SEG184	-1006.5	237.75
327	SEG185	-1039.5	237.75
328	SEG186	-1072.5	237.75
329	SEG187	-1105.5	237.75
330	SEG188	-1138.5	237.75
331	SEG189	-1171.5	237.75
332	SEG190	-1204.5	237.75

NO.	NAME	X	Y
333	SEG191	-1237.5	237.75
334	SEG192	-1270.5	237.75
335	SEG193	-1303.5	237.75
336	SEG194	-1336.5	237.75
337	SEG195	-1369.5	237.75
338	SEG196	-1402.5	237.75
339	SEG197	-1435.5	237.75
340	SEG198	-1468.5	237.75
341	SEG199	-1501.5	237.75
342	SEG200	-1534.5	237.75
343	SEG201	-1567.5	237.75
344	SEG202	-1600.5	237.75
345	SEG203	-1633.5	237.75
346	SEG204	-1666.5	237.75
347	SEG205	-1699.5	237.75
348	SEG206	-1732.5	237.75
349	SEG207	-1765.5	237.75
350	SEG208	-1798.5	237.75
351	SEG209	-1831.5	237.75
352	SEG210	-1864.5	237.75
353	SEG211	-1897.5	237.75
354	SEG212	-1930.5	237.75
355	SEG213	-1963.5	237.75
356	SEG214	-1996.5	237.75
357	SEG215	-2029.5	237.75
358	SEG216	-2062.5	237.75
359	SEG217	-2095.5	237.75
360	SEG218	-2128.5	237.75
361	SEG219	-2161.5	237.75
362	SEG220	-2194.5	237.75
363	SEG221	-2227.5	237.75
364	SEG222	-2260.5	237.75
365	SEG223	-2293.5	237.75
366	SEG224	-2326.5	237.75
367	SEG225	-2359.5	237.75
368	SEG226	-2392.5	237.75
369	SEG227	-2425.5	237.75
370	SEG228	-2458.5	237.75
371	SEG229	-2491.5	237.75
372	SEG230	-2524.5	237.75
373	SEG231	-2557.5	237.75
374	SEG232	-2590.5	237.75
375	SEG233	-2623.5	237.75
376	SEG234	-2656.5	237.75
377	SEG235	-2689.5	237.75
378	SEG236	-2722.5	237.75
379	SEG237	-2755.5	237.75
380	SEG238	-2788.5	237.75

NO.	NAME	X	Y
381	SEG239	-2821.5	237.75
382	SEG240	-2854.5	237.75
383	SEG241	-2887.5	237.75
384	SEG242	-2920.5	237.75
385	SEG243	-2953.5	237.75
386	SEG244	-2986.5	237.75
387	SEG245	-3019.5	237.75
388	SEG246	-3052.5	237.75
389	SEG247	-3085.5	237.75
390	SEG248	-3118.5	237.75
391	SEG249	-3151.5	237.75
392	SEG250	-3184.5	237.75
393	SEG251	-3217.5	237.75
394	SEG252	-3250.5	237.75
395	SEG253	-3283.5	237.75
396	SEG254	-3316.5	237.75
397	SEG255	-3349.5	237.75
398	SEG256	-3382.5	237.75
399	SEG257	-3415.5	237.75
400	SEG258	-3448.5	237.75
401	SEG259	-3481.5	237.75
402	SEG260	-3514.5	237.75
403	SEG261	-3547.5	237.75
404	SEG262	-3580.5	237.75
405	SEG263	-3613.5	237.75
406	SEG264	-3646.5	237.75
407	SEG265	-3679.5	237.75
408	SEG266	-3712.5	237.75
409	SEG267	-3745.5	237.75
410	SEG268	-3778.5	237.75
411	SEG269	-3811.5	237.75
412	SEG270	-3844.5	237.75
413	SEG271	-3877.5	237.75
414	SEG272	-3910.5	237.75
415	SEG273	-3943.5	237.75
416	SEG274	-3976.5	237.75
417	SEG275	-4009.5	237.75
418	SEG276	-4042.5	237.75
419	SEG277	-4075.5	237.75
420	SEG278	-4108.5	237.75
421	SEG279	-4141.5	237.75
422	SEG280	-4174.5	237.75

NO.	NAME	X	Y
423	SEG281	-4207.5	237.75
424	SEG282	-4240.5	237.75
425	SEG283	-4273.5	237.75
426	SEG284	-4306.5	237.75
427	SEG285	-4339.5	237.75
428	SEG286	-4372.5	237.75
429	SEG287	-4405.5	237.75
430	SEG288	-4438.5	237.75
431	SEG289	-4471.5	237.75
432	SEG290	-4504.5	237.75
433	SEG291	-4537.5	237.75
434	SEG292	-4570.5	237.75
435	SEG293	-4603.5	237.75
436	SEG294	-4636.5	237.75
437	SEG295	-4669.5	237.75
438	SEG296	-4702.5	237.75
439	SEG297	-4735.5	237.75
440	SEG298	-4768.5	237.75
441	SEG299	-4801.5	237.75
442	SEG300	-4834.5	237.75
443	SEG301	-4867.5	237.75
444	SEG302	-4900.5	237.75
445	SEG303	-4933.5	237.75

5. BLOCK DIAGRAM

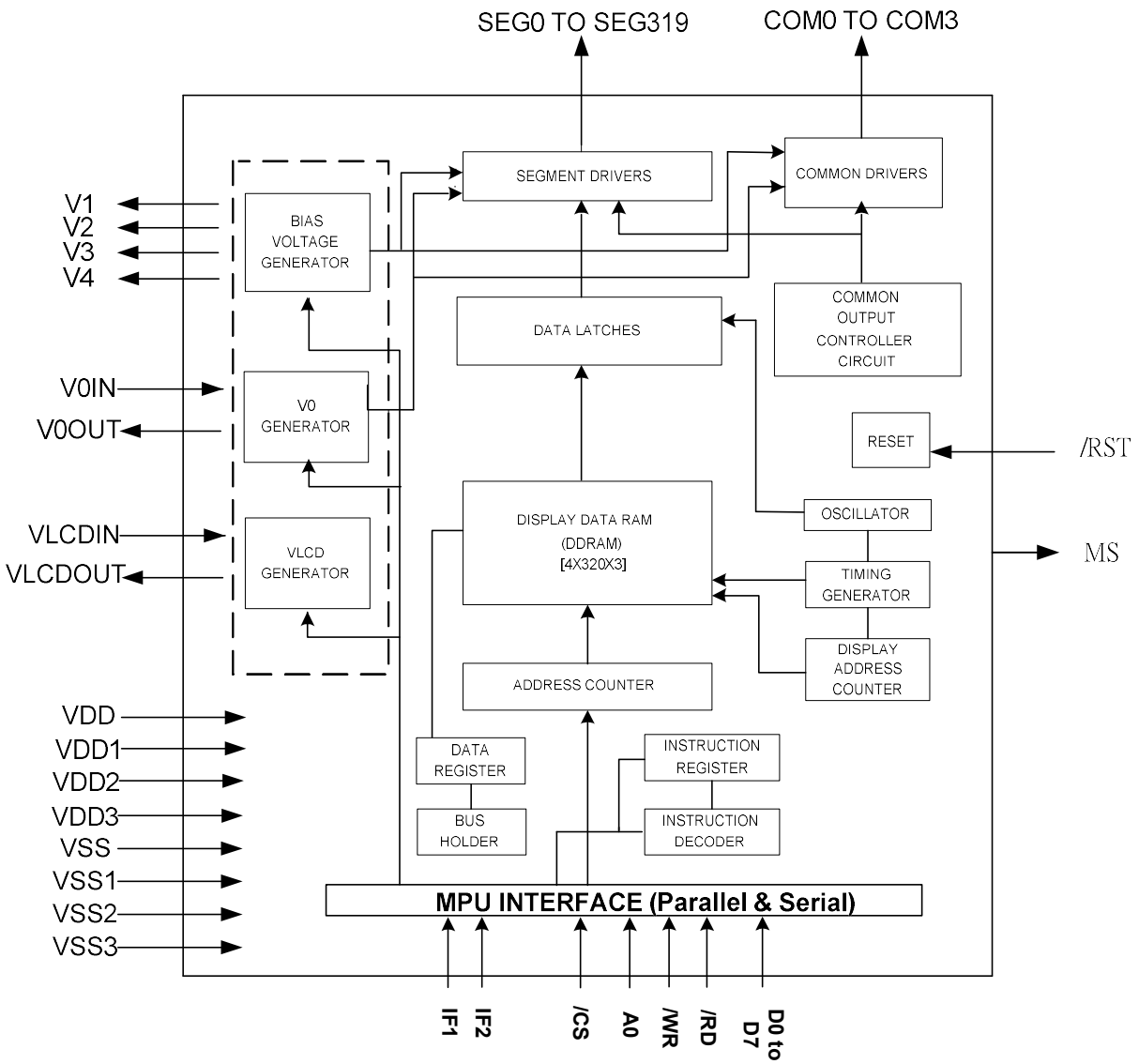


Figure 1

6. PIN DESCRIPTION

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="3">LCD driver outputs</td></tr>
<tr><td>SEG0 to SEG319</td><td>O</td><td>LCD segment driver outputs.
This display data and the M signal control the output voltage of segment driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Segment drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Sleep in mode</td><td>VSS</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COM0 to COM3</td><td>O</td><td>LCD column driver outputs.
This internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><td rowspan="2">Display data</td><td rowspan="2">M (Internal)</td><td colspan="2">Common drover output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">VSS</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Sleep in mode</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td colspan="3">MICROPROCESSOR INTERFACE</td></tr>
<tr><td>/CS</td><td>I</td><td>Chip select input pins.
Data and instruction input/output is enabled only when /CS is " L ".
When chip select is non-active, D0~D7 are high impedance.</td></tr>
<tr><td>/RST</td><td>I</td><td>Reset input pin.
When /RST is " L ", initialization is being execute.</td></tr>
<tr><td>IF[2:1]</td><td>I</td><td>Parallel or serial data input select input：
<table>
<tr><th>IF2</th><th>IF1</th><th>MPU interface type</th></tr>
<tr><td>H</td><td>H</td><td>80 series 8-bit parallel</td></tr>
<tr><td>H</td><td>L</td><td>No Use</td></tr>
<tr><td>L</td><td>H</td><td>4SPI (8-bit serial)</td></tr>
<tr><td>L</td><td>L</td><td>3SPI (9-bit serial)</td></tr>
</table></td></tr>
<tr><td>A0</td><td>I</td><td>Register select input pin.
In 8080 or 4SPI parallel interface：
A0= “H”：D0 to D7 are data input.
A0= “L”：D0 to D7 are instruction input.
In 3SPI serial interface：
A0 pad should connect to VDD.</td></tr>
<tr><td>/WR</td><td>I</td><td>Read / Write execution control pin. (This pin is used only in parallel interface)
Write enable clock input pin. D0 to D7 are latched at the rising edge of the /WR signal.
When in serial interface, connect this pin to VDD.</td></tr>
<tr><td>/RD</td><td>I</td><td>Read / Write execution control pin. (This pin is used only in parallel interface)
Read enable clock input pin. When /RD is “L”, D0 to D7 are in output status.
When in serial interface, connect this pin to VDD.</td></tr>
<tr><td>D0 to D7</td><td>I/O</td><td>In 8080 parallel interface：
80-8bit：D0 to D7 connect to the standard 8bit MPU bus.
In 3SPI or 4SPI serial interface：
D0 pad will be used for SI (data) function.
D1 pad will be used for SCK (clock) function.
D2 to D7 should connect to VDD.</td></tr>
</table>

Power Supply Pins		
VDD	**Supply**	Power supply for digital circuit.
VDD1	**Supply**	Power supply for digital circuit.
VDD2	**Supply**	Power supply for analog circuit.
VDD3	**Supply**	Power supply for analog circuit.
VSS	**Supply**	Ground level of digital circuit.
VSS1	**Supply**	Ground level of digital circuit.
VSS2	**Supply**	Ground level of analog circuit.
VSS3	**Supply**	Ground level of analog circuit.
VLCDOUT	**Supply**	If the internal voltage generator is used, the VLCDIN & VLCDOUT must be connected together. If an external supply is used, this pin must be left open.
VLCDIN	**Supply**	An external VLCD supply voltage can be supplied using the VLCDIN pad. In this case, VLCDOUT has to be left open, and the internal voltage generator has to be programmed to zero.
V0IN V0OUT V1 V2 V3 V4	**I/O**	LCD driver supply voltages V0IN & V0OUT must be connected together. When the internal voltage generator or the external VLCD voltage supply is used, an external Vop voltage supply voltage can be supplied using the V0IN pad. In this case, VLCDOUT & V0OUT must be left open, and V0IN & VLCDIN must be connected together. Voltages should have the following relationship; When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias. (Refer to 10. Voltage Converter Circuit)
LCD Power Supply Pins		
CAP1N	**O**	DC/DC voltage converter. Connect capacitors between this terminal and the CAP1P, CAP3P terminal.
CAP2N	**O**	DC/DC voltage converter. Connect capacitors between this terminal and the CAP2P, terminal.
CAP1P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAP2P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
CAP3P	**O**	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
CAPX	**O**	DC/DC voltage converter. Connect to VLCDOUT directly.
Vref	**O**	Reference voltage, let this pin open.

System Control		
MS	**I**	Master/Slave mode pin Master mode connects MS to VDD. Slave mode connect MS to VSS.
CL	**I/O**	Master/Slave Clock pin When using Master/Slave mode, both of CL should be connected to each other. If not this pin should open.
SYNC	**I/O**	Master/Slave Sync pin When using Master/Slave mode, both of SYNC should be connected to each other. If not this pin should open
DON	**I/O**	Master/Slave Display ON/OFF pin When using Master/Slave mode, both of DON should be connected to each other. If not this pin should open
Test Pin		
T0~T11	**-**	T0~T11 are test pins. T0 and T10 pins must connect to VSS. (Refer application note) And do not use T1~T9 and T11. Let T1~T9 and T11 pins open.
Dummy	**-**	Dummy pins and let them open.

ST7037 I/O PIN ITO Resistance Limitation：

PIN Name	ITO Resister
T0~T11 ,Dummy	No Limitation
Vref,	Floating
VDD, VDD1~VDD3, VSS, VSS1~VSS3, V0IN , V0OUT, VLCDIN,VLCDOUT V1 , V2 , V3 , V4, CAP1P~CAP4P,CAPX	<100Ω
V0IN , V0OUT, V1 , V2 , V3 , V4 (Master / Slave Mode)	<50Ω
/CS, A0, /RD, /WR, MS, IF[2:1], D0 …D7	<1KΩ
/RST	<10KΩ

7. FUNCTIONS DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There is a /CS pin for chip selection. The ST7037 can communicate with an MPU when /CS is "L". When /CS is “H”, the internal shift register and the counters are reset.

Selecting Parallel / Serial interface

ST7037 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by IF pins.

Parallel / Serial Interface Mode

I/F Mode		I/F Description	Pin Assignment						
IF2	IF1		/CS	A0	E_RD	RW_WR	Used Data Bus	D1	D0
H	H	80 serial 8-bit parallel	/CS	A0	/RD	/WR	D7~D2	D1	D0
H	L	No Use	-	-	-	-	-	-	-
L	H	4SPI mode (8-bit)	/CS	A0	--	--	--	SCK	SI
L	L	3SPI mode (9-bit)	/CS	--	--	--	--	SCK	SI

8080 Parallel interface

The ST7037 identifies the type of the data bus signals according to the combination of A0, /RD and /WR signals, as show as follow：

8080-series			Description
A0	/RD	/WR	
H	↓	H	Display data read out
H	↓	H	Register status read
L	H	↑	Instruction write
H	H	↑	Display data write

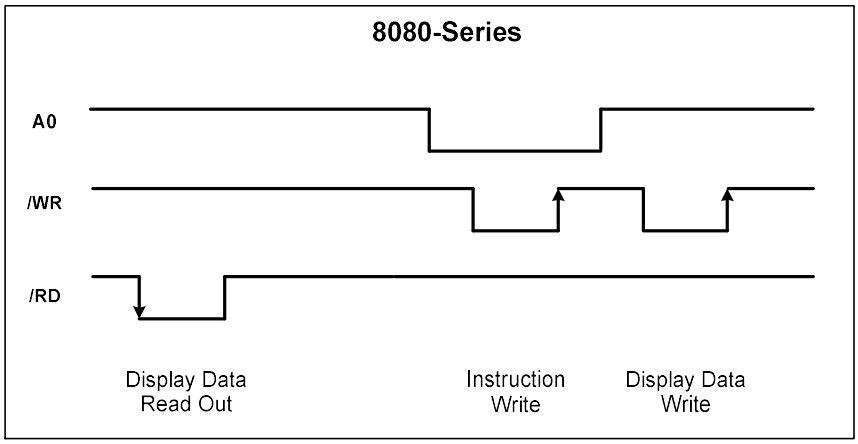


Figure 2

3SPI (9-bit) and 4SPI (8-bit) interface

The 3SPI (9-bit) serial interface uses three pins /CS, SI and SCK to enter commands and data. Meanwhile, the 4SPI (8-bit) serial interface uses four pins /CS, SI, SCK, and A0 for the same purpose. Data read is not available in the serial interface.

(1) 3SPI (9-bit) serial interface
When entering data (parameters): SI= HIGH at the rising edge of the 1st SCK.

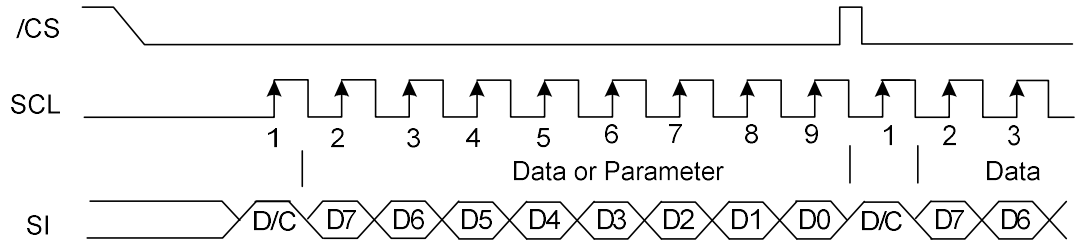


Figure 3

When entering command: SI= LOW at the rising edge of the 1st SCK.

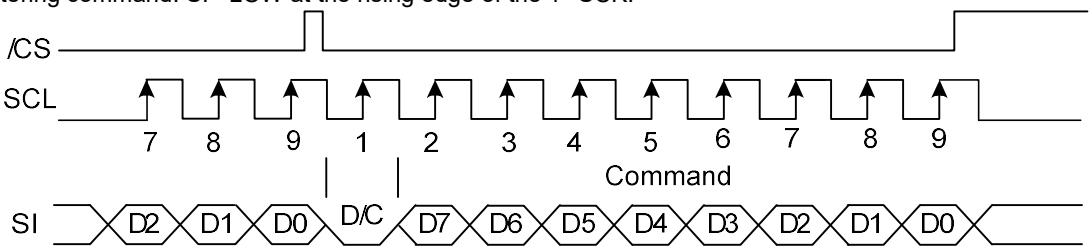


Figure 4

(2) 4SPI (8-bit) serial interface
When entering data (parameters): A0= HIGH at the rising edge of the 8th SCK.

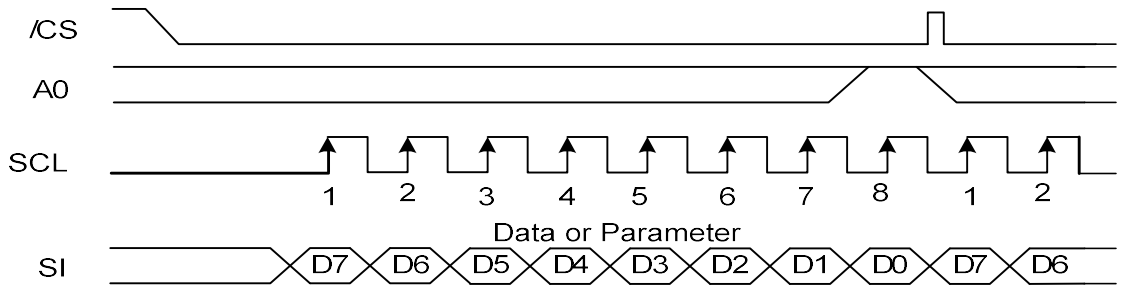


Figure 5

When entering command: A0= LOW at the rising edge of the 8th SCK

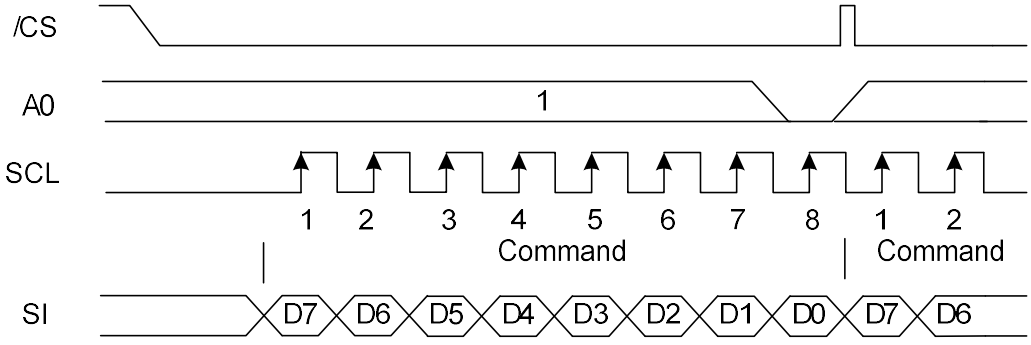


Figure 6

DISPLAY DATA RAM (DDRAM)

The ST7037 contains a 4x320x3 bit static RAM that stores the display data. The display data RAM store the dot data for the LCD. There is a direct correspondence between X-address and column output number. It is 4-row by 320-column addressable array. Each pixel can be selected when the row and column addresses are specified. Data is written through D0 to D7. The display data of D0 to D7 from the microprocessor correspond to the LCD common lines. The microprocessor can write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

Row Address Circuit

Row address circuit has a 1-bit present counter that provides row address to the Display Data RAM (DDRAM). The Display Data RAM (DDRAM) row address is specified by the row address set command.

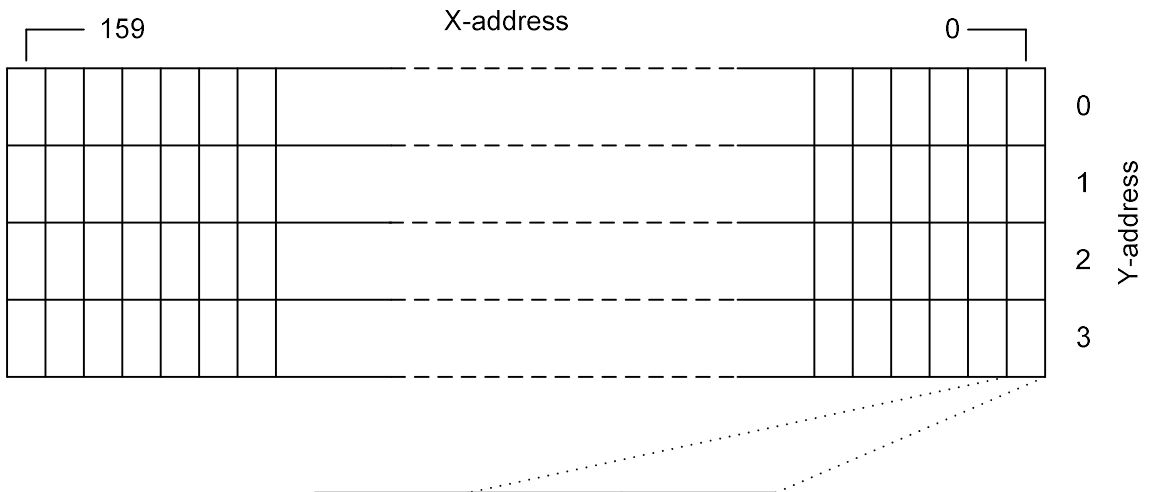
Column Address Circuit

Column address circuit has a 9-bit preset counter that provides column address to the Display Data RAM (DDRAM). The Display Data RAM (DDRAM) column address is specified by the column address set command. The specified column address is incremented (+1) with each display data write command. This allows the MPU display data to be accessed continuously.

ADDRESSING

The display RAM has a matrix of 4x320x3 bits. The address pointer addresses the columns. The address ranges are: X→ 0 to 319 (100111111), Y(0 (0). Addresses outside these ranges are not allowed. The X address increases horizontally after each byte . After the end of X address (X = 319) X return to 0 and Y return to the begin address.

Data Format



SEG out	SEG1				SEG0			
Data	D7	D6	D5	D4	D3	D2	D1	D0
Data Format	X	F2	F1	F0	X	F2	F1	F0

Figure 7

Display Data RAM

It is 320 X 4 X 3 bits capacity RAM prepared for storing dot data. Refer to the following memory map for the RAM Configuration.

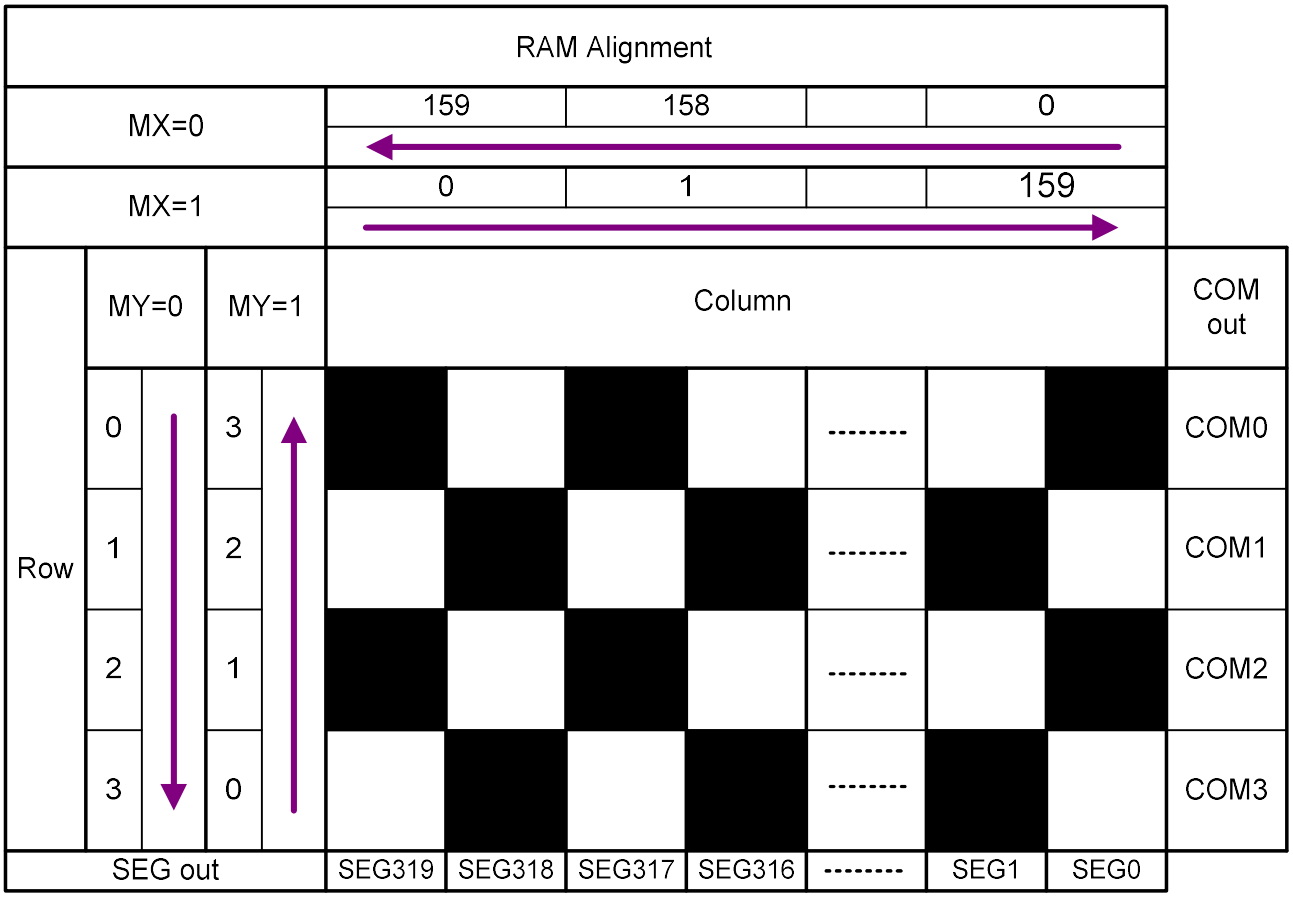
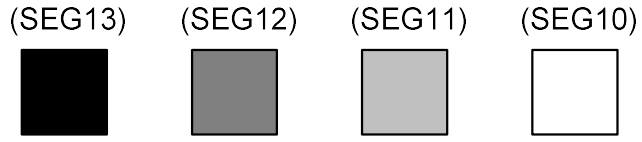


Figure 8

RAM Write




```
Write_command(0x2A);      // Column address set
Write_data(0x05);         // set start address at 5 (SEG10 and SEG11)
Write_data(0x9F);         // set end address at 159

Write_command(0x2C);      // Memory write
Write_data(0x10);         // 0H = White     , 1H = Light gray
Write_data(0x73);         // 3H = Dark gray, 7H = Black
```

Gray Set				
F2	**F1**	**F0**	**Display Dot**	
0	0	0	White	
0	0	1	Light gray	
0	1	1	Dark gray	
1	1	1	Black	

Note: In this case. The LCD is normal white

8. RESET CIRCUIT

Setting /RST to"L" or Reset instruction can initialize internal function.
When /RST becomes "L", following procedure is occurred.

-- Oscillator circuit is stopped
-- The LCD power supply circuit is stopped
-- Display OFF
-- Display all point OFF
-- Segment/Common output go to the VSS level
Display normal
Row address：0
Column address：0
Power control [OSC BST FOL V0 VREF] = All OFF
All registers are default value

9. INSTRUCTION TABLE

COMMAND	CODE										DESCRIPTION
	HEX	A0	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	00	0	0	0	0	0	0	0	0	0	No Operation
Software reset	01	0	0	0	0	0	0	0	0	1	Software reset
Sleep in	10	0	0	0	0	1	0	0	0	0	Sleep in mode
Sleep out	11	0	0	0	0	1	0	0	0	1	Sleep out mode
Inverse display off	20	0	0	0	1	0	0	0	0	0	Display Inversion off
Inverse display on	21	0	0	0	1	0	0	0	0	1	Display Inversion on
Exit all point on	22	0	0	0	1	0	0	0	1	0	Exit all point on
Enter all point on	23	0	0	0	1	0	0	0	1	1	Enter all point on
Display off	28	0	0	0	1	0	1	0	0	0	Display off
Display on	29	0	0	0	1	0	1	0	0	1	Display on
Column address set	2A	0	0	0	1	0	1	0	1	0	Column address set
	-	1	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	Column start address
	-	1	CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0	Column end address
Row address set	2B	0	0	0	1	0	1	0	1	1	Row address set
	-	1	0	0	0	0	0	0	RS1	RS0	Row start address
	-	1	0	0	0	0	0	0	RE1	RE0	Row end address
Memory write	2C	0	0	0	1	0	1	1	0	0	Write data to memory
Memory read	2E	0	0	0	1	0	1	1	1	0	Read data from memory
Duty set	B0	0	1	0	1	1	0	0	0	0	Duty set
	-	1	0	0	0	0	0	0	DT1	DT0	Range 1 to 4 duty
Frame Frequency	B2	0	1	0	1	1	0	0	1	0	Frame Frequency
	-	1	0	0	0	1	FR3	FR2	FR1	FR0	
LCD scan set	B7	0	1	0	1	1	0	1	1	1	LCD scan set
	-	1	MY	MX	0	0	MS	0	0	0	Master/Slave enable
Enter Read modify	B8	0	1	0	1	1	1	0	0	0	Enter Read modify
Exit Read modify	B9	0	1	0	1	1	1	0	0	1	Exit Read modify
Vop set	C0	0	1	1	0	0	0	0	0	0	Vop set
	-	1	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	Range 6V to 13.2V
	-	1	0	0	0	0	0	0	0	Vop8	
Bias selection	C3	0	1	1	0	0	0	0	1	1	Bias selection
	-	1	0	0	0	0	0	0	0	BS	
Power Control	D2	0	1	1	0	1	0	0	1	0	Power Control
	-	1	0	0	0	OSC	BST	FOL	V0	VREF	

INSTRUCTION DESCRIPTION

NOP(00H)

Non-operation command

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	0	No Operation

Software reset(01H)

When this command is written, it causes a software reset. It resets the commands and parameters to their default. This command doesn't change DDRAM content.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	0	0	0	0	1	Software reset

Sleep in(10H)

This command causes the LCD module to enter the minimum power consumption mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	0	Sleep in mode

Sleep out(11H)

This command turns off sleep in mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	0	1	0	0	0	1	Sleep out mode

Inverse display off(20H)

This command is used to leave inverse display mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	0	Inverse display off (Normal display)

Inverse display on(21H)

This command is used to enter inverse display mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	0	1	Inverse display on

Exit all points on(22H)

This command is used to exit all display points on mode . This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	1	0	Exit all point on

Enter all points on(23H)

This command is used to enter all display points on mode. This command will not change any status or memory data.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	0	0	1	1	Enter all point on

Display off(28H)

This command is used to enter into display off mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	0	Display off

Display on(29H)

This command is used to enter into display on mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	0	1	Display on

Column address set(2AH)

This command defines column start address and end address data will be written.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	1	0	Column address set
1	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0	Column start address
1	CE7	CE6	CE5	CE4	CE3	CE2	CE1	CE0	Column end address

Row address set(2BH)

This command defines Row start address and end address data will be written.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	0	1	1	Row address set
1	0	0	0	0	0	0	RS1	RS0	Row start address
1	0	0	0	0	0	0	RE1	RE0	Row end address

Memory write(2CH)

This command is executed before write data to memory.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	0	0	Write data to memory

Memory read(2EH)

This command is executed before read data from memory.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	0	0	1	0	1	1	1	0	Read data from memory

This command is only support 8080-8 bit or 8080-4bit

Duty set(B0H)

This command is used to set the duty of COM

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	0	0	0	Duty set
1	0	0	0	0	0	0	DT1	DT0	Duty selection

DT[1:0]		Duty mode
0	0	1 duty
0	1	2 duty
1	0	3 duty
1	1	4 duty (Default)

Notes

1. When one duty is selected, COM0~COM3 output waveform is equal. Under this condition, COM0~COM3 could be connected together.

Frame frequency (B2H)

This command is used to set frame frequency.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	0	1	0	Frame frequency set
1	0	0	0	1	FR3	FR2	FR1	FR0	Frame frequency registers set

FR[3:0]				Frame frequency	FR[3:0]				Frame frequency
0	0	0	0	50HZ	1	0	0	0	105HZ
0	0	0	1	60HZ	1	0	0	1	110HZ
0	0	1	0	70HZ (Default)	1	0	1	0	115HZ
0	0	1	1	75HZ	1	0	1	1	120HZ
0	1	0	0	80HZ	1	1	0	0	130HZ
0	1	0	1	85HZ	1	1	0	1	140HZ
0	1	1	0	90HZ	1	1	1	0	150HZ
0	1	1	1	100HZ	1	1	1	1	Reserved

LCD scan set (B7H)

This command is used to set LCD scan .

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	0	1	1	1	LCD scan set and MS set
1	MY	MX	0	0	MS	0	0	0	LCD direction selection, Master/Slave

MY :

when set "0" , COM0 to COM3 (Default)

set "1" , COM3 to COM0

MX :

when set "0" , SEG0 to SEG319 (Default)

set "1" , SEG319 to SEG0

MS:

when set "0" , Master/Slave disable (Default)

set "1" , Master/Slave enable

Enter read modify (B8H)

This command is used to enter read modify mode.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	1	0	0	0	Enter read modify mode

Normally, the counter of address will increase (+1) after execute memory read (0x2E) sequence. But when enter read modify mode , the counter will stop counting.

Exit read modify (B9H)

This command is used to exit read modify mode,

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	0	1	1	1	0	0	1	Exit read modify mode

Vop set (C0H)

This command is used to set the optimum LCD supply voltage V0..

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	0	0	0	0	Vop set
1	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	Set the registers of Vop
1	-	-	-	-	-	-	-	Vop8	

The Vop value is programmed via the Vop[8:0] registers

The default value in this register is 7DH (8V)

V0 = a + (Vop[8:0]) x b

SYMBOL	Value	Unit
a	3	V
b	0.04	V

Ex: Vop[8:0] = 111 1110 (7DH)

V0 = 3 + 125 x 0.04 = 8V

VOP[8:0]	V0	Notes
001001011	6 V	**Vop range : 6V~13.2V**
001001100	6.04 V	
001001101	6.08 V	
⋮	⋮	
011111101	13.12 V	
011111110	13.16 V	
011111111	13.2 V	

Bias selection (C3H)

This command is used to select LCD bias ratio of the voltage required to drive LCD.

A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	0	0	0	1	1	Bias selection
1	0	0	0	0	0	0	0	BS	Set the registers of bias

BS	Bias value
0	1/2 bias (Default)
1	1/3 bias

Power control (D2)

This command is used to set power register.

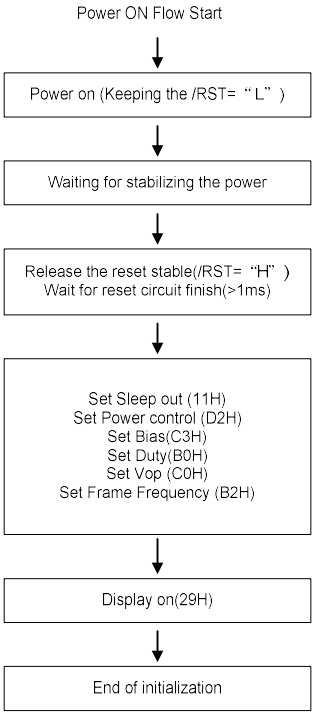
A0	D7	D6	D5	D4	D3	D2	D1	D0	Description
0	1	1	0	1	0	0	1	0	Power Control
1	0	0	0	OSC	BST	FOL	V0	VREF	

Power register	Set ‘0’	Set ‘1’
OSC	OSC on	OSC off (Default)
BST	Booster on	Booster off (Default)
FOL	Follower on	Follower off (Default)
V0	V0 regulator on	V0 regulator off (Default)
VREF	Vref regulator on	Vref regulator off (Default)

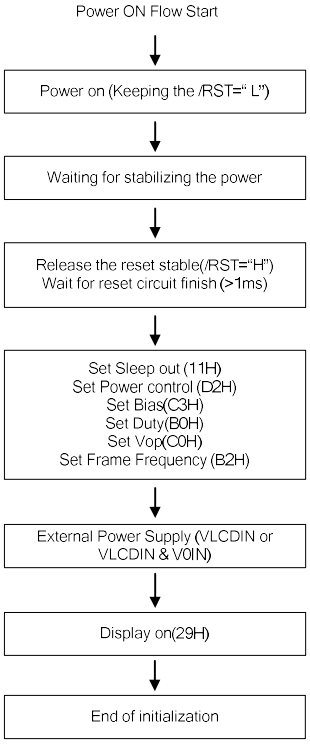
Command Description

☐ Referential instruction setup flow for power on:

I. Internal Power ON Flow



II. External Power ON Flow



Note:

1. **Power Control Setting of Internal Power Supply**

   Write(Command, 0xD2); // Power Control

   /*Internal VLCD supply (VLCDIN) */

   Write(Data, 0x00); // All Power Register ON

2. **Power Control Setting of External Power Supply**

   Write(Command, 0xD2); // Power Control

   /*External VLCD supply (VLCDIN) */

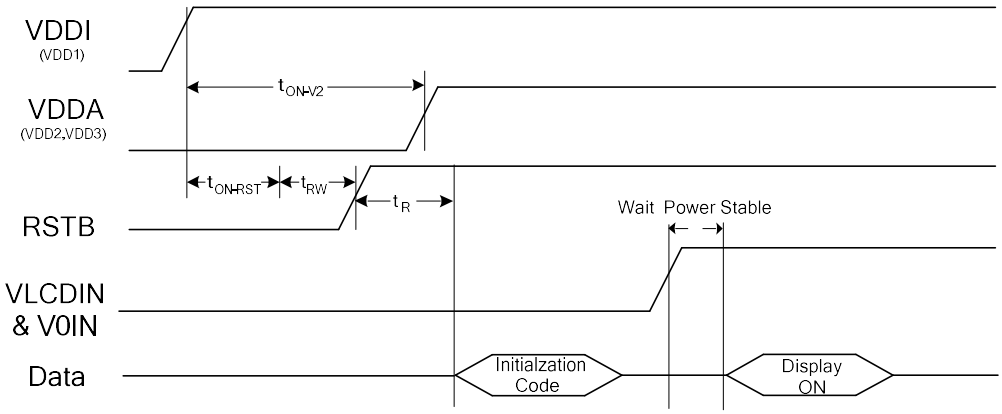
   Write(Data, 0x08); // OSC, FOL, V0, VREF ON; BST OFF

   or

   /*External Vop supply (VLCDIN shorted with V0IN)*/

   Write(Data, 0x0A); //OSC, FOL, VREF ON; BST, V0 OFF

☐ Referential Power ON Sequence

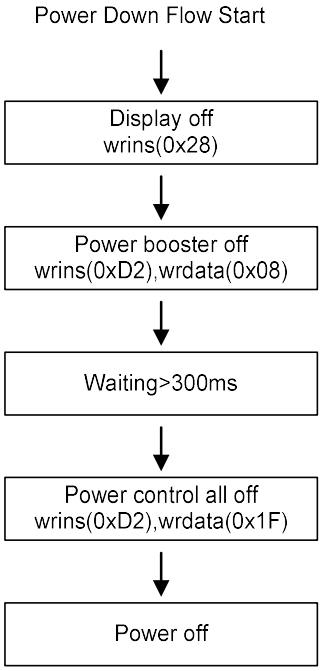


Timing Requirement:

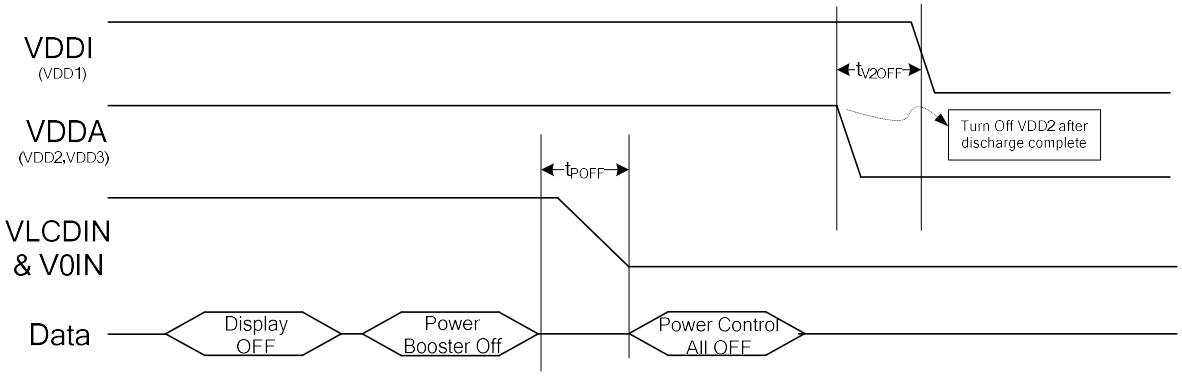
Item	Symbol	Requirement	Note
VDDA power delay	t_{ON-V2}	$0 \le t_{ON-V2}$	● Applying VDDI and VDDA in any order will not damage IC.
RSTB input time	t_{ON-RST}	No Limitation	● If RSTB is Low, High or unstable during power ON, a successful hardware reset by RSTB is required after VDDI is stable. ● RSTB=L can be input at any time after power is stable. ● t_{RW} & t_R should match the timing specification of RSTB. ● To prevent abnormal display, the recommended timing is: $0 \le t_{ON-RST} \le 30$ ms.
	tR	-	● tR > 2us
	tRW	-	● tRW > 2us

☐ Referential instruction setup flow for power down:

I. Internal Power OFF Flow



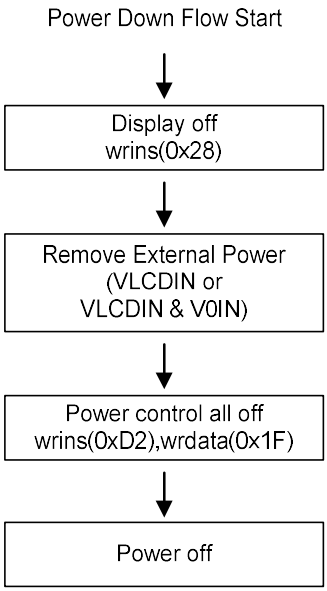
☐ Referential Power OFF Sequence



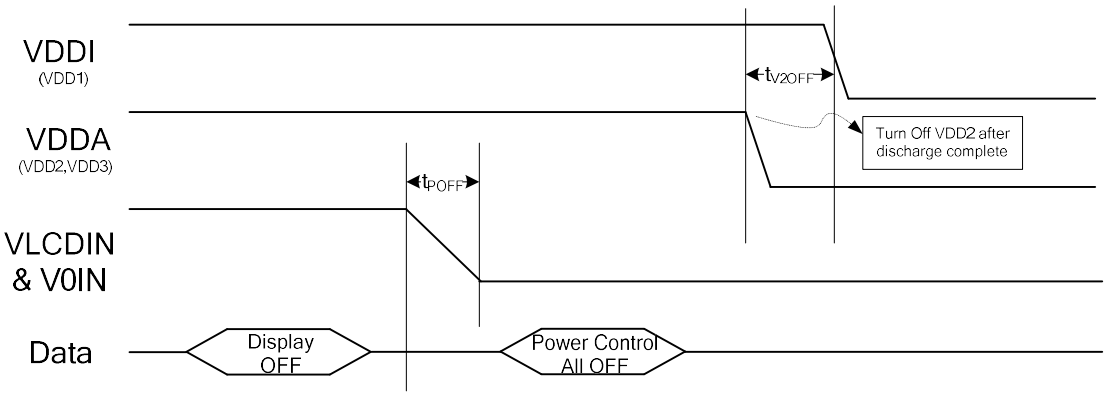
Note:

1. t_{POFF}: >300ms.
2. t_{V2OFF}: Period between VDDI and VDDA OFF time. ≧ 0 ms (min).
3. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.

II. External Power OFF Flow



☐ Referential External Power OFF Sequence



Note:

4. t_{POFF} According to external power supply discharge time.
5. t_{V2OFF}: Period between VDDI and VDDA OFF time. ≧ 0 ms (min).
6. It is NOT recommended to turn VDDI OFF before VDDA. Without VDDI, the internal status cannot be guaranteed and internal discharge-process maybe stopped. The un-discharged power maybe flows into COM/SEG output(s) and the liquid crystal in panel maybe polarized.

Initial code example (Single chip mode)

```
wrins(0x11);       // sleep out
wrins(0xD2);       // set power control
wrdata(0x00);      // all power on

wrins(0xC0);       // set Vop
wrdata(0x96);      // set Vop 9V
wrdata(0x00);

wrins(0xC3);       // set Bias
wrdata(0x01);      // set 1/3 Bias

wrins(0xB0);       // set Duty
wrdata(0x03);      // set 1/ 4 duty

wrins(0x2A);       // set SEG address
wrdata(0x00);      // set Start at SEG0
wrdata(0x1F);      // set End at SEG63

wrins(0x2B);       // set COM address
wrdata(0x00);      // set Start at COM0
wrdata(0x03);      // set Start at COM3

wrins(0xB2);       // set frame frequency
wrdata(0x1D);      // set frame 140Hz

wrins(0x29);       // Display on
```

Initial code example (Master / Slave mode)

Set Initial Code for Slave:

```
Command_slave(0x11);          // sleep out
Command_slave(0xB7);          // LCD scan set
Data_slave(0x08);             // Master/Slave Enable
Command_slave(0xD2);          // set power control
Data_slave(0x18);             // power all off

Command_slave (0x2A);         // SEG address set
Data_slave (0x00)             // set start address
Data_slave (0x1F);            // set end address
Command_slave (0x2B);         // COM address set
Data_slave (0x00)             // set start address
Data_slave (0x03);            // set end address

Command_slave (0x2C);         // Memory write
Data_slave (0x10);            // Seg40: 0H = White ,SEG41: 1H = Light gray
Data_slave (0x73);            // Seg42:3H = Dark gray, Seg43: 7H = Black
                              // Please refer to Spec. - RAM write
```

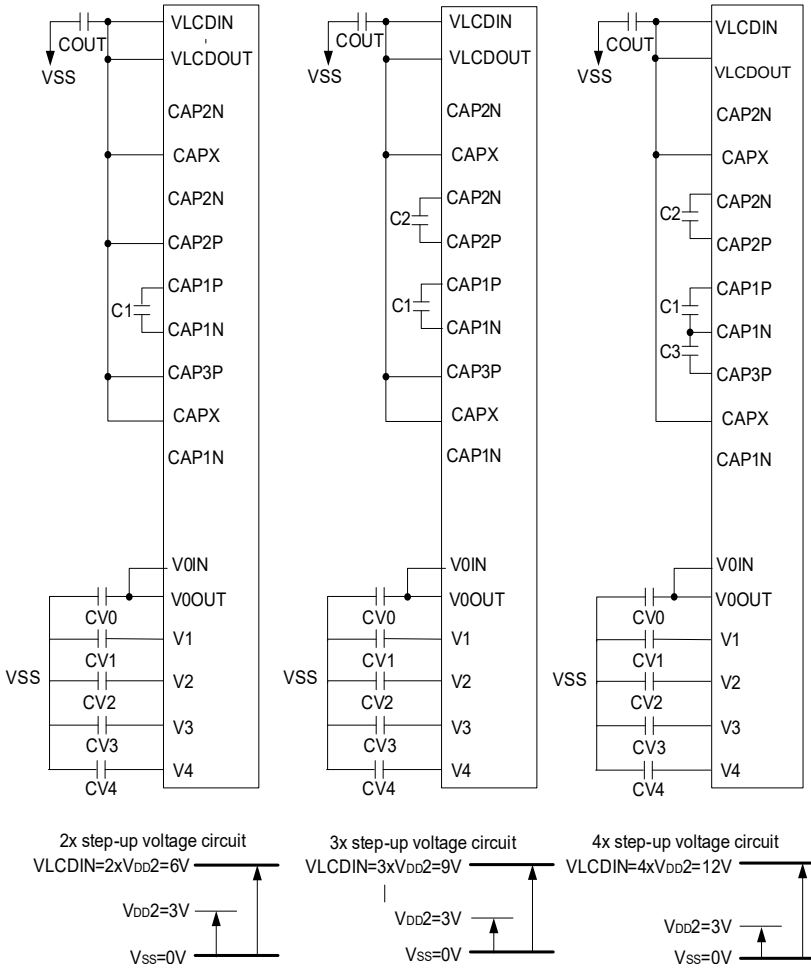
Set Initial Code for Master:

```
Command_master(0x11);         // sleep out
Command_master(0xB7);         // LCD scan set
Data_master(0x08);            // Master/Slave Enable
Command_master(0xD2);         // set power control
Data_master(0x00);            // all power on
Command_master(0xC0);         // set Vop
Data_master(0x32);            // set Vop 5V
Data_master(0x00);

Command_slave (0x2A);         // SEG address set
Data_slave (0x00)             // set start address
Data_slave (0x1F);            // set end address
Command_slave (0x2B);         // COM address set
Data_slave (0x00)             // set start address
Data_slave (0x03);            // set end address
```

```
Command_slave (0x2C);          / Memory write
Data_slave (0x10);             // Seg40: 0H = White ,SEG41: 1H = Light gray
Data_slave (0x73);             // Seg42:3H = Dark gray, Seg43: 7H = Black
                               // Please refer to Spec. - RAM write
Command_master(0xB2);          // set frame frequency
Data_master(0x12);             // set frame 70Hz

Command_master(0x29);          // Display on
```

10. Voltage Converter Circuit

The Step-up Voltage Circuits



The critical operating voltage of capacitor is determined by following calculations.

Booster capacitors:
C1 > VDD2 X 1
C2 > VDD2 X 2
C3 > VDD2 X 3

COUT > VDD2 X Booster Step

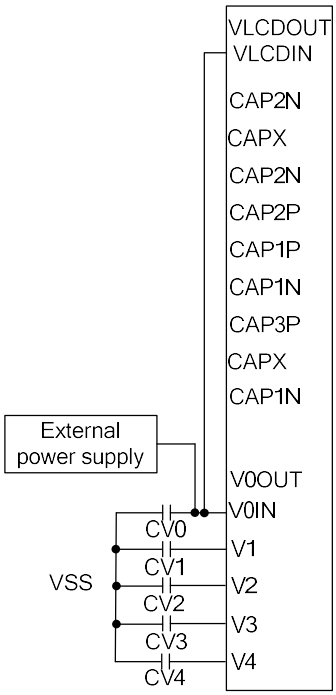
Follower output capacitors:
CV0 > V0
CV1 > V0 X [(N-1)/N]
CV2 > V0 X [(N-2)/N]
CV3 > V0 X [2/N]
CV4 > V0 X [1/N]
note: N = VLCD Bias

Figure 9

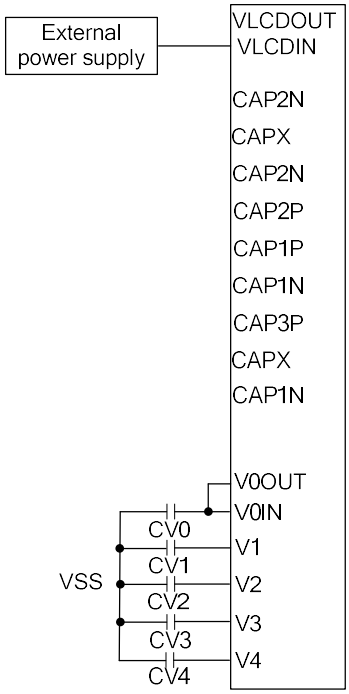
Power	Internal voltage generator	External VLCD supply voltage	External Vop supply voltage	External V0~V4 supply voltage
V0IN	Must be connected with V0OUT	Must be connected with V0OUT	External Power Supply	External Power Supply
V0OUT	Must be connected with V0IN	Must be connected with V0IN	Floating	Floating
VLCDIN	Must be connected with VLCDOUT	External Power Supply	Must be connected with V0IN	Must be connected with V0IN
VLCDOUT	Must be connected with VLCDIN	Floating	Floating	Floating

The External Power Circuits

(1)When the Voltage Follower circuit alone is used
(External Vop supply voltage)



(2)When the V0 voltage regulator internal resistor is used
(External VLCD supply voltage)



(3)When the V0 bulit-in power is not used
(External V0~V4 supply voltage)

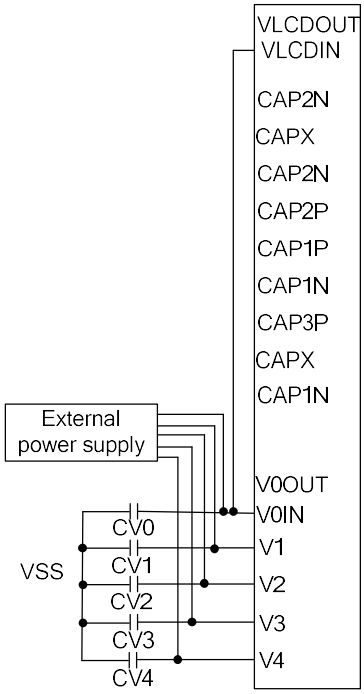


Figure 10

11. ABSOLUTE MAXIMUM VALUES

In accordance with the Absolute Maximum Rating System; see notes 1 and 2. (VSS=0V)

Parameter	Symbol	Conditions	Unit
Power Supply Voltage 1	VDDI (VDD, VDD1)	-0.3 ~ +4	V
Power Supply Voltage 2	VDDA (VDD2, VDD3)	-0.3 ~ +4	V
Power Supply Voltage 3	VLCD - VSS, V0 – VSS	-0.3 ~ +14.5	V
Power Supply Voltage 4	V1, V2, V3, V4	0.3 to V0	V
Input Voltage	VIN	-0.3 ~ 4	V
Output Voltage	VO	-0.3 ~ 4	V
Operating Temperature	TOPR	–30 ~ +85	°C
Storage Temperature	TSTR	–55 ~ +105	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.
3. Insure that the voltage levels of VLCD, V0, V1 and V2 are always such that：

   VLCD ≧ V0 ≧ V1 ≧ V2 ≧ VSS

12. HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

13. DC CHARACTERISTICS

(VSS=0V, Ta = 25°C)

Item		Symbol	Condition		Rating			Units	Applicable Pin
					Min.	Typ.	Max.		
Operating Voltage 1		VDDI (VDD, VDD1)	(Relative to VSS)		2.5	-	3.6	V	VSS
Operating Voltage 2		VDDA (VDD2, VDD3)	(Relative to VSS)		2.5	-	3.6	V	VSS
High-level Input Voltage		VIH	-		0.7 x VDDI	-	VDDI	V	
Low-level Input Voltage		VIL	-		VSS	-	0.3 x VDDI	V	
High-level Output Voltage		VOH	1 mA		0.8 x VDDI	-	VDDI	V	
Low-level Output Voltage		VOL	-		VSS	-	0.2 x VDDI	V	
Input leakage current		ILI	VIN=VDDI or VSS		–1.0	-	1.0	μA	
Liquid Crystal Driver ON Resistance		RON	Ta = 25°C △V=10% (Relative To VSS)	VLCDIN = 8.0 V	-	0.6	0.9	KΩ	COMn SEGn
					-	1	1.5		
Frame frequency		FR	VDDI=VDDA=3.0V Booster X4 V0 – VSS = 8V FR[7:0] = 0x12		63	70	77	Hz	
Internal Power	Supply Step-up output voltage Circuit	V0OUT	VDDI=VDDA=3.3V Booster X4 (Relative To VSS)		6	-	13.2	V	V0OUT
	Voltage regulator Circuit Operating Voltage	V0IN	VDDI=VDDA=3.3V Booster X4 (Relative To VSS)		6	-	13.2	V	V0IN

DC Current Consumption：

During Display, with the Internal Power Supply ON, current consumed of total ICs

Test pattern	Symbol	Condition	Rating			Units	Notes
			Min.	Typ.	Max.		
Display Pattern SNOW	ISS	VDDI=VDDA=3.0V Booster X4 V0 – VSS = 8V Ta = 25°C	—	250	500	μA	
Sleep In Mode	ISS	VDDI=VDDA=3.0V Booster X4 V0 – VSS = 8V Ta = 25°C	—	3	10	μA	

(Note：Bare die)

Notes to the DC characteristics

1. The maximum possible V0 voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock is applied.
3. Sleep in mode. During sleep in all static currents are switched off.
4. When Vop external voltage applied to V0IN pin; V0IN is not connected with V0OUT.
5. The current consumption is DC characteristic of ST7037.

14. TIMING CHARACTERISTICS

Parallel Interface Characteristics (8080 MCU)

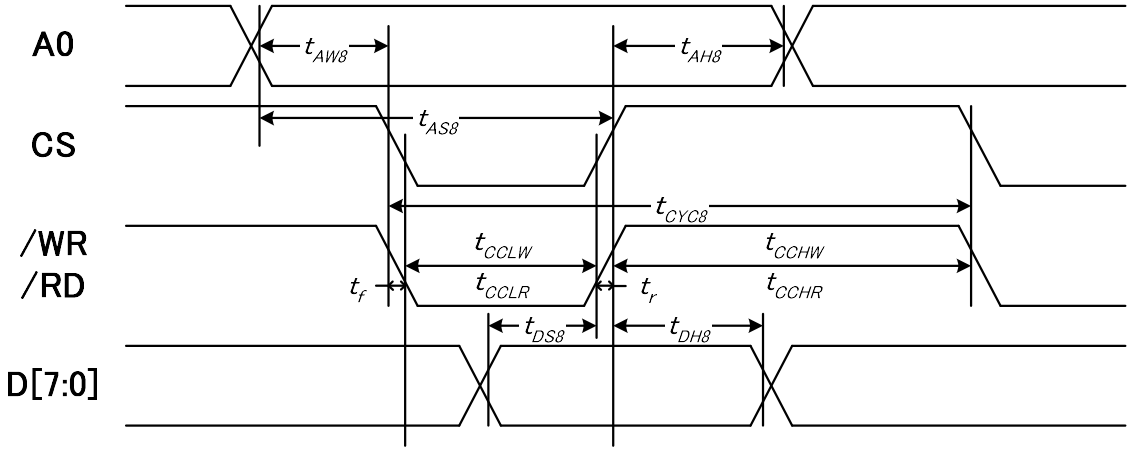


Figure 11 8080 Parallel Interface Timing Chart

(VSS=0V, VDDI=2.8~3.3V, VDDA=3.0V, Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		30	—	ns
Address hold time		tAH8		180	—	
System cycle time	/WR	tCYC8		400	—	
/WR L pulse width (WRITE)		tCCLW		220	—	
/WR H pulse width (WRITE)		tCCHW		180	—	
/RD L pulse width (READ)	RD	tCCLR		220	—	
/RD H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D[7:0]	tDS8		100	—	
WRITE Data hold time		tDH8		100	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDDI as the standard.

Serial Interface Characteristics (3-Line Interface)

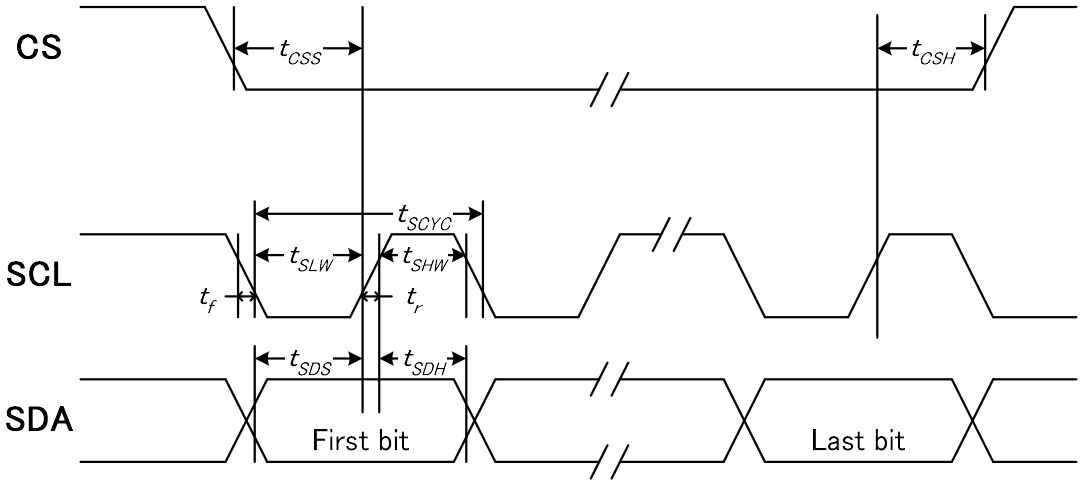


Figure 12 3SPI Serial Interface Timing Chart

(VSS=0V, VDDI=2.8~3.3V, VDDA=3.0V, Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCK	tSCYC		100	—	ns
SCK “H” pulse width		tSHW		50	—	
SCK “L” pulse width		tSLW		50	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCK time	CS	tCSS		30	—	
CS-SCK time		tCSH		60	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDDI as the standard.

Serial Interface Characteristics (4-Line Interface)

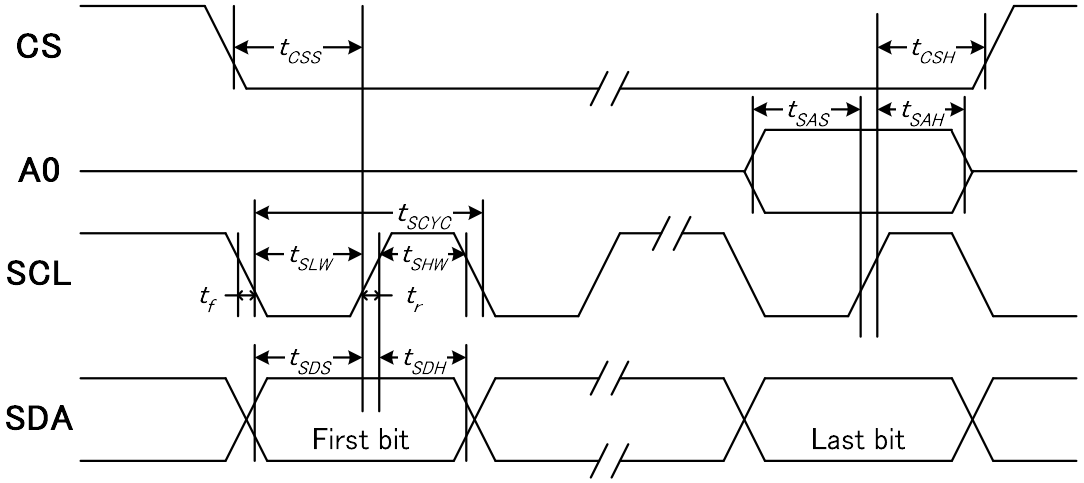


Figure 13 4SPI Serial Interface Timing Chart

(VSS=0V, VDDI=2.8~3.3V, VDDA=3.0V, Ta = 25°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period	SCK	tSCYC		100	—	ns
SCK “H” pulse width		tSHW		50	—	
SCK “L” pulse width		tSLW		50	—	
Address setup time	A0	tSAS		30	—	
Address hold time		tSAH		20	—	
Data setup time	SDA	tSDS		30	—	
Data hold time		tSDH		20	—	
CS-SCK time	CS	tCSS		30	—	
CS-SCK time		tCSH		75	—	

*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDDI as the standard.

RESET TIMING

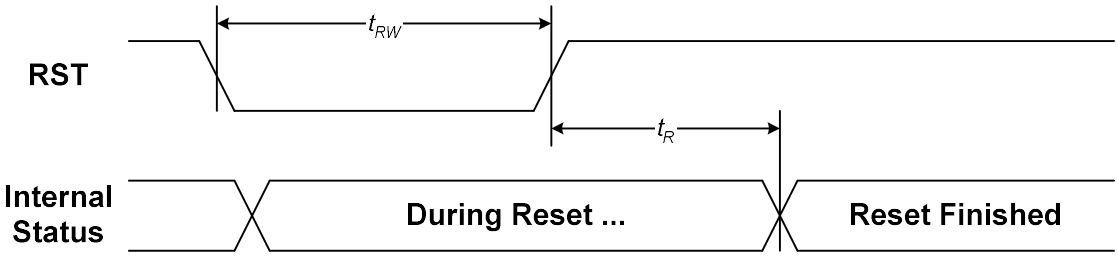


Figure 14 Reset Timing Chart

(VSS=0V, VDDI=2.8~3.3V, VDDA=3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		—	2	us
Reset “L” pulse width	tRW		2	—	

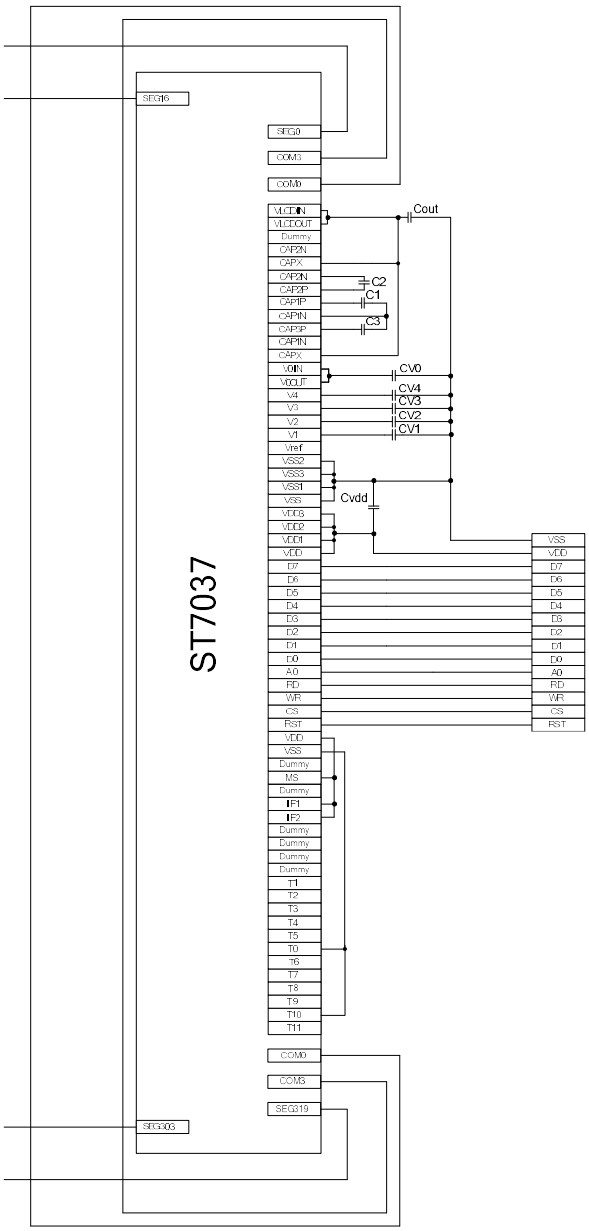
*1 The input signal rise and fall time (tr, tf) are specified at 15 ns or less.

*2 All timing is specified using 20% and 80% of VDDI as the standard.

15. APPLICATION NOTE

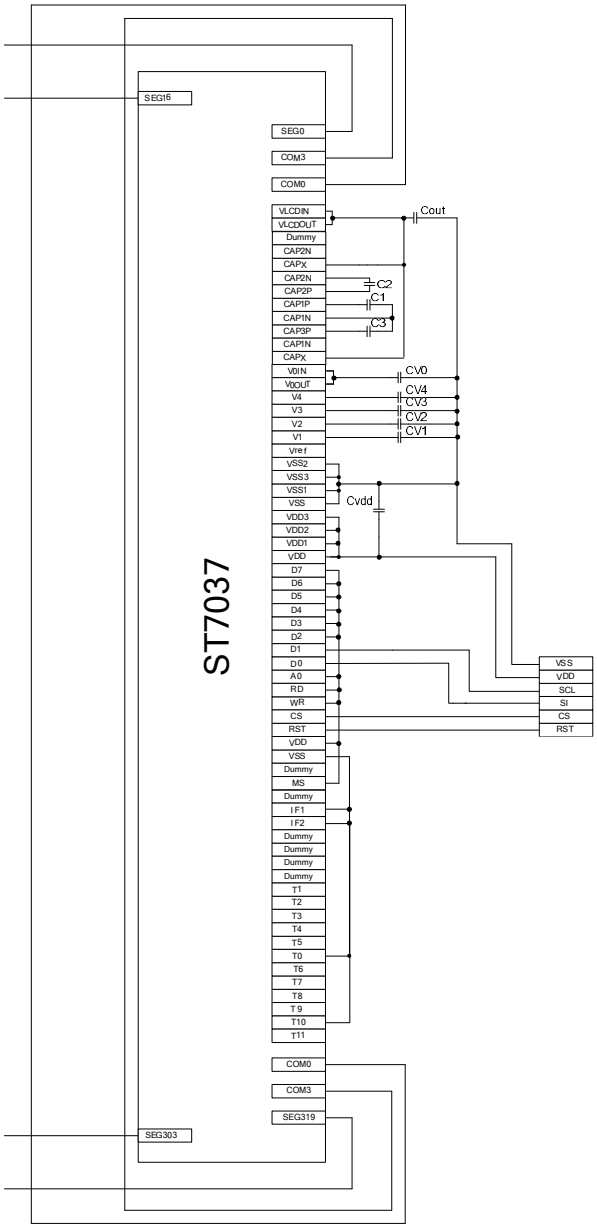
ST7037(1/4Duty)

Resolution 4COM x 320SEG
Internal analog circuit
Interface : 8080-8bit
Internal OSC
Booster X4
Capacitor :
CVdd,CV0~CV4 = 1uF
Cout,C1 ~ C3 = 1uF ~2.2uF(depend on LCD loading)



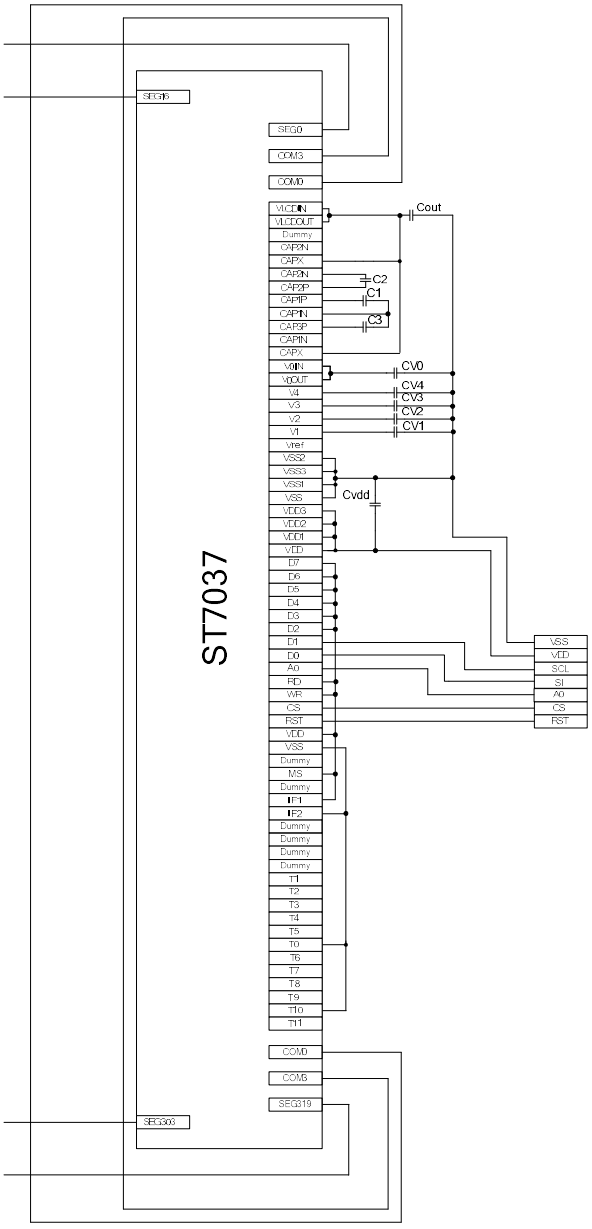
ST7037(1/4Duty)

Resolution 4COM x 320SEG
Internal analog circuit
Interface : 3 Line SPI
Internal OSC
Booster X4
Capacitor :
CVdd,CV0~CV4 = 1uF
Cout,C1 ~ C3 = 1uF ~2.2uF(depend on LCD loading)

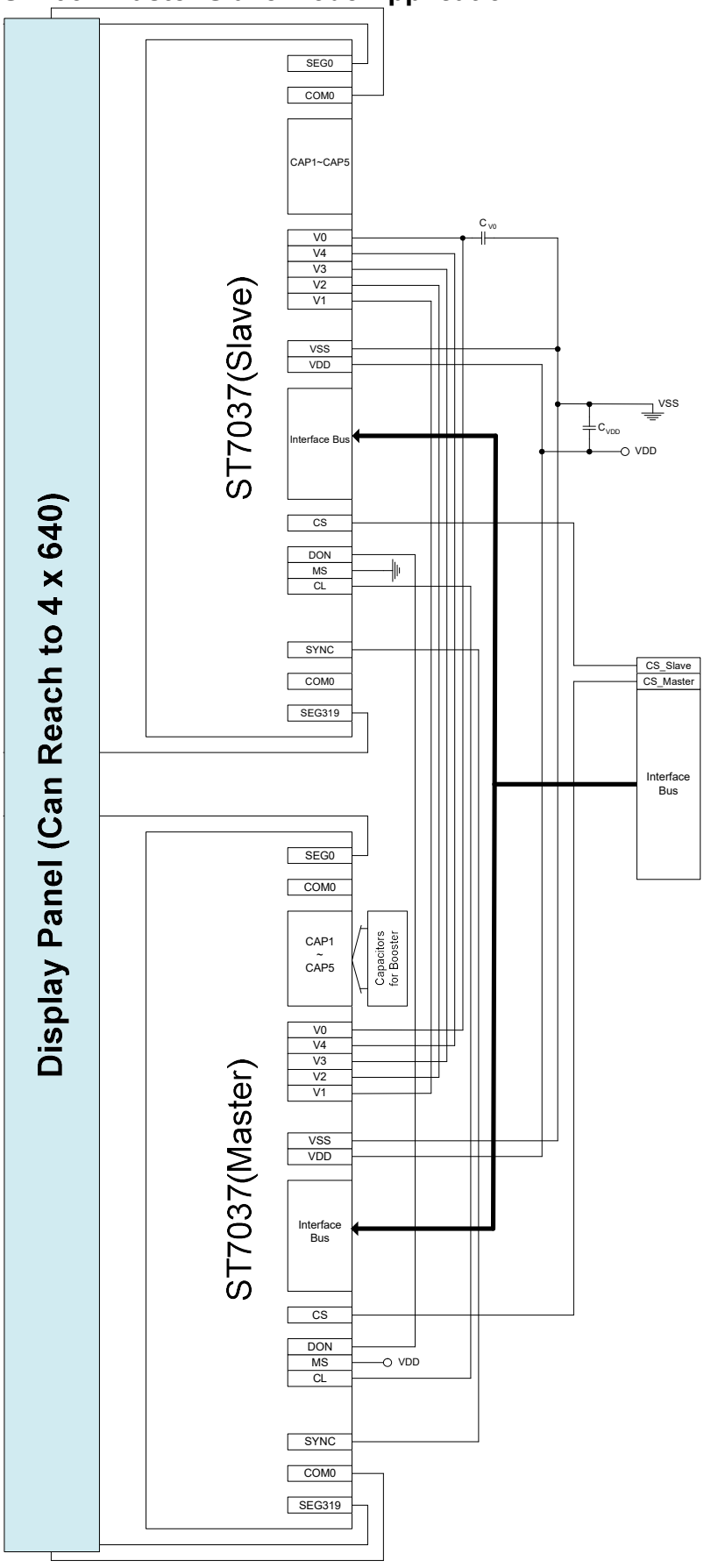


ST7037(1/4Duty)

Resolution 4COM x 320SEG
Internal analog circuit
Interface : 4 Line SPI
Internal OSC
Booster X4
Capacitor :
CVdd,CV0~CV4 = 1uF
Cout,C1 ~ C3 = 1uF ~2.2uF(depend on LCD loading)



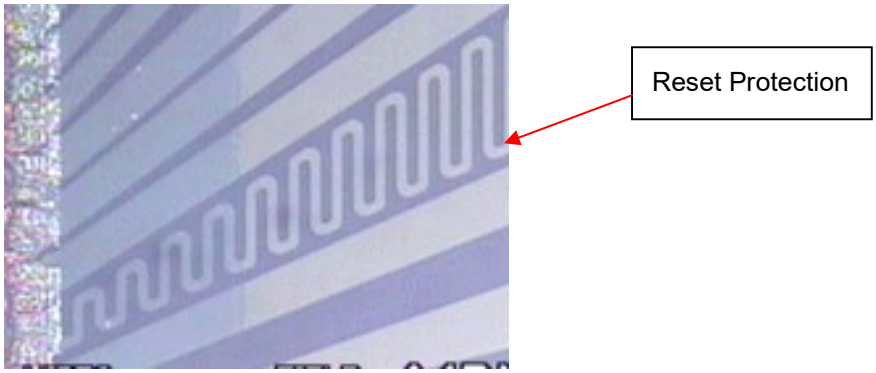
ST7037 Master/Slave Mode Application



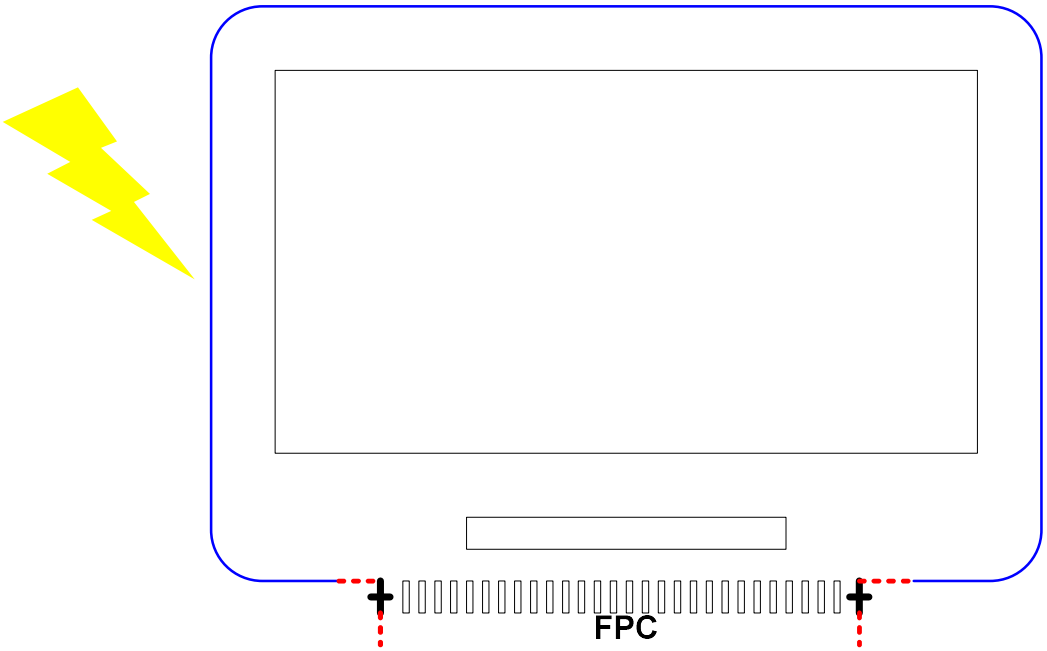
(1) The “MS” pin of the master device is connected to VDD;
The “MS” pin of the slave device is connected to VSS.
(2) The master device-output pins V0, CLK, DON, SYNC need to be connected to the slave device.
(3) The signal of CS_Master and CS_Slave controls the devices separately
(4) The interface bus includes A0, /WR, /RD , /RST, D0~D7.
(5) The ITO resistance of V0~V4 pin needs to be < 50 Ω.

◆ **For ESD protection of the LCM, here are some recommendations:**

1. RST (Reset pin): Please increase the resistance of this pin. Here is an example:



2. ESD Protection Ring: “Shielding Ground” is the first protection of ESD. By connecting the “Blue” (ITO) ring to the FPC, the protection ring is finished.

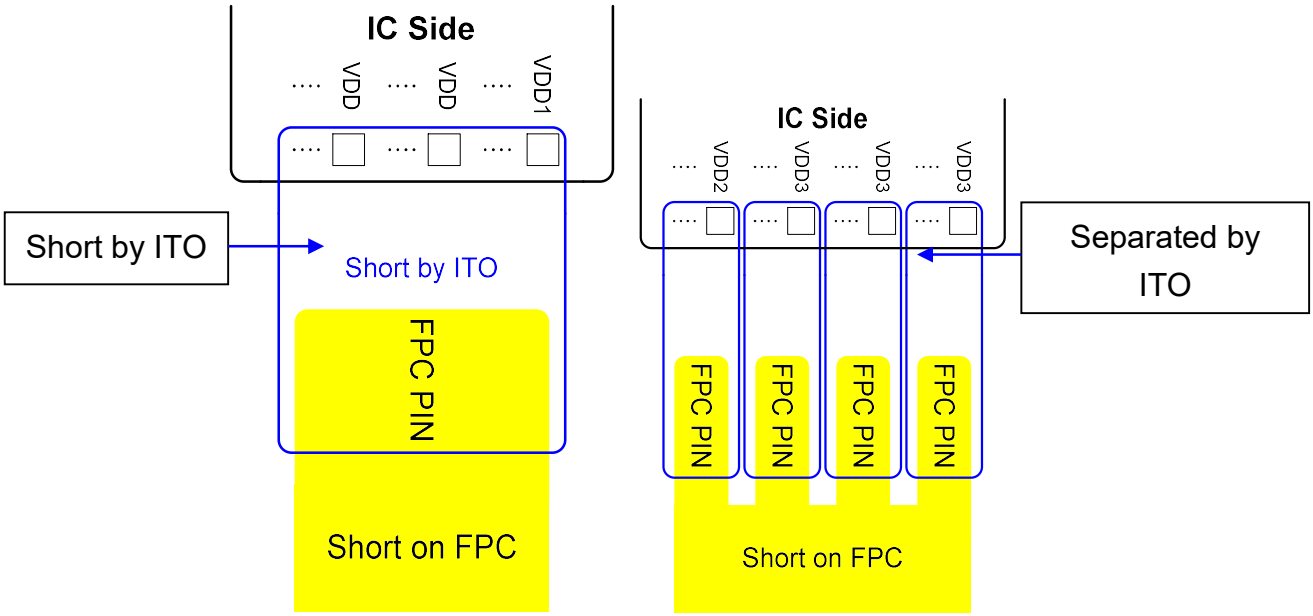


◆ **VDD, VDD1, VDD2, VDD3, VSS, VSS1, VSS2 & VSS3：**

To avoid the noise in different power system affect other power system, please separate different power source on ITO layout (VDD and VDD1 can be short together to get better performance).

To reduce the ITO resistance, the power source should have enough trace width (includes ITO width and FPC trace width). So the separated ITO traces should be connected together by FPC.

=> The recommended solution is shown below.



Specification Revision History		
Version	**Date**	**Description**
0.1	2011/02/24	1.Preliminary Version
0.2	2011/07/08	1.Remove 8080-4Bit 2.Modified Booster levels
0.3	2012/02/03	1.Modified application circuit for T10.
1.0	2012/04/12	1.Add V0IN & V0OUT pin description 2.Modified voltage converter circuit 3.Remove preliminary 4.Add duty set notes 5.Add Vop set notes. 6.Modified absolute maximum values 7.Modified DC characteristics 8.Release version
1.1	2012/10/16	1. Increasing the application of master / slave mode
1.2	2012/10/29	1.Modified the typing error of the application note
1.2a	2013/05/09	1. Modify operating temperature range.
1.2b	2013/11/07	1. Modify operating and storage temperature range.
1.2c	2014/05/13	1. Modify operating temperature range.
1.3	2018/04/30	1. Modify operating temperature range to -30°C ~+85°C.
1.4	2018/12/28	1. Add Vop range for 1 duty application 2. Modify MS instruction
1.5	2021/01/04	1.Modify Part Number to ST7037-G4 2. Modify Power On/Off Flow 3. Add Product Application Description