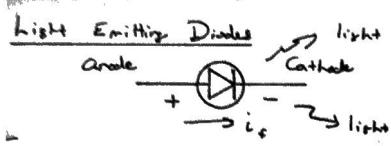


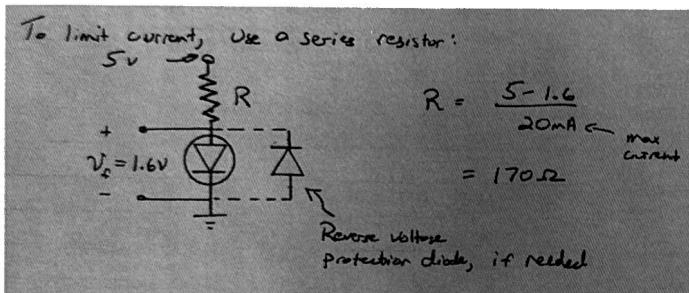
I. The Blinking Light:

Incandescent Lamp: A filament heated until it glows. Works with AC or DC, may be controlled and dimmed with switches, semiconductors, etc.

Light Emitting Diodes:

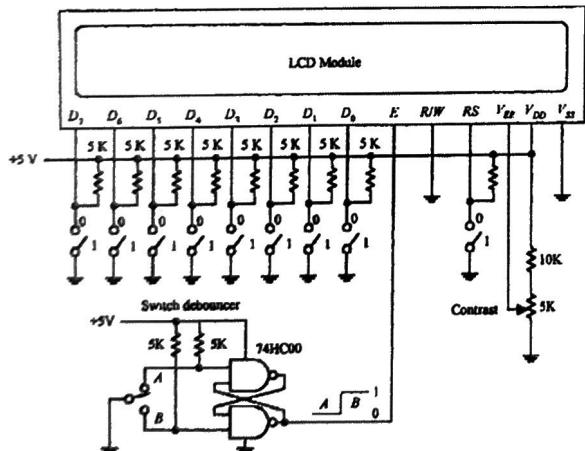


- Forward current typically limited to 10-20 mA.
- Maximum reverse voltage may be small, e.g., 5 V
- Forward voltage drop may range from 0.6 V to 2.2 V or more, depending on the LED technology.
- Limited spectral (color) output

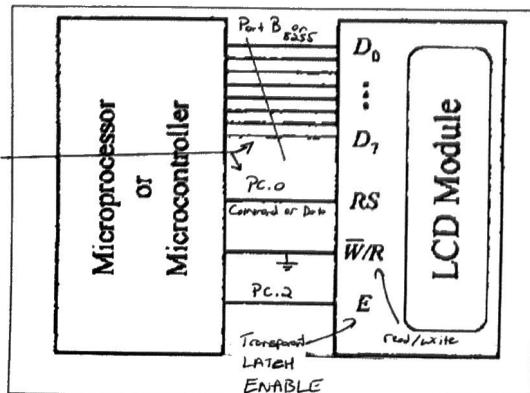


1

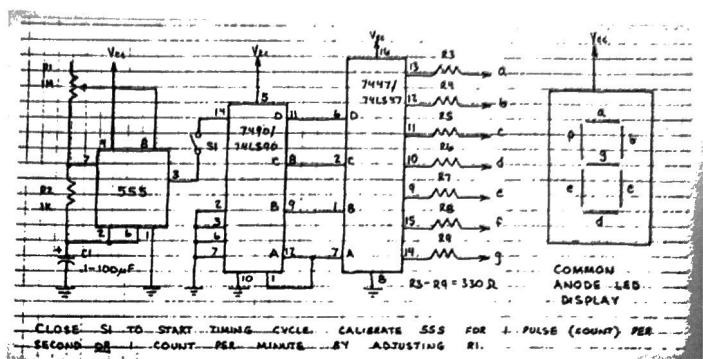
Test hookup described in Scherz:



The panel might connect to a microcontroller this way:

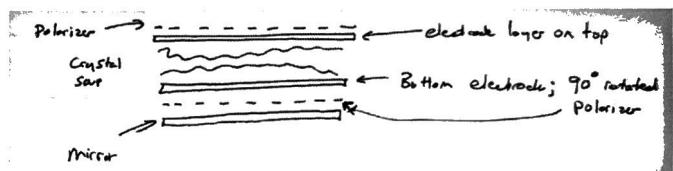


Multi-segment LED displays - useful for digits:



II. Liquid Crystal Displays:

LCD displays work by controlling the polarization of light traveling through an optical "sandwich":



(This is discussed in Scherz.)

2

Sample programming plan:

On our staff nerd kit, "W" is the MINMON write command. Port A = FE08, Port B = FE09, Port C = FE0A, control register is at FE0B.

The Hitachi 44780 controller used in our display has created a ubiquitous standard. Typical programming plan:

- Activate the 8255: (all 3 ports output)
WFE0B = 80
- Set display for 8 bit communication, 5x7 character set:
WFE0A = 00 (lower the "E" line)
WFE09 = 38
WFE0A = 04 (raise the "E" line)
WFE0A = 00 (lower the E line, latching command)
- Turn display on, hide cursor:
WFE09 = 0C
WFE0A = 04 (raise the "E" line)
WFE0A = 00 (lower the E line, latching command)
- Clear display:
WFE09 = 01
WFE0A = 04 (raise the "E" line)
WFE0A = 00 (lower the E line, latching command)
- Set RAM address to zero:
WFE0A = 00 (lower the "E" line)
WFE09 = 80
WFE0A = 04 (raise the "E" line)
WFE0A = 00 (lower the E line, latching command)
- "Wash, rinse, repeat" to display characters ☺:
WFE0A = 01 (lower the "E" line)
WFE09 = 39 (displays a "9")
WFE0A = 05 (raise the "E" line)
WFE0A = 01 (lower the E line, latching command)

LCD Instruction Set

INSTRUCTION	R/S	R/W	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Clear Display	0	0	0	0	0	0	0	0	0	1
Display & Cursor Home	0	0	0	0	0	0	0	0	1	X
Character Entry Mode	0	0	0	0	0	0	0	1	I/D	S
Display & Cursor On/Off	0	0	0	0	0	0	1	D	C	B
Display/Cursor Shift	0	0	0	0	0	1	D/C	R/L	X	X
Function Set	0	0	0	0	1	DL	N	F	X	X
Set CGRAM Address	0	0	0	1	A	A	A	A	A	A
Set Display Address	0	0	1	A	A	A	A	A	A	A
Poll the "Busy Flag"	0	0	BF	X	X	X	X	X	X	X
Write Character to Display ^a	1	0	D	D	D	D	D	D	D	D
Read Character on Display ^b	1	1	D	D	D	D	D	D	D	D

- I/D = Increment (I/D = 1)/Decrement (I/D = 0) each byte written to display
 S = Display shift on (S = 1), Display shift off (S = 0)
 D = Turn display on (D = 1), Turn display off (D = 0)
 C = Show cursor (C = 1), Hide cursor (C = 0)
 B = Underline cursor (B = 0, C = 1), Blink cursor (B = 1, C = 1)
 D/C = Move display (D/C = 1), Move cursor (D/C = 0)
 R/L = Direction of shift: Shift right (R/L = 1), Shift left (R/L = 0)
 DL = Set data interface length: 8-bit interface (DL = 1)^a, 4-bit interface (DL = 0)
 N = Number of display lines: 2 line mode (N = 1), 1 line mode (N = 0)^a
 F = Character font format: 5 x 10 dot (F = 1), 5 x 7 dot (F = 0)^a
 BF = Poll the Busy Flag: controller not busy (BF = 0), controller busy (BF = 1)
 A = CGRAM or display address bit
 D = Character data bit
 a = Write character to display at the current cursor position
 b = Read character on display at the current cursor position
 X = Don't care
 * = Initialization settings

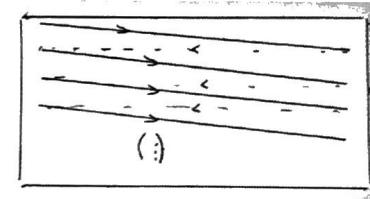
5

LCD Character Codes

Char. code

00000000	0JP'P - タミウ
xxxx0001	!1AQa9. ラツカド
xxxx0010	"2BRbr'イ"×ゼ
xxxx0011	#3CScs. ウタモエ
xxxx0100	\$40Tdt. エトナヒ
xxxx0101	%5EUeu. オナコス
xxxx0110	&6FUVfv. フカニヨ
xxxx0111	'7GW9w. フクシラ
xxxx1000	(8HXhx. イクネリ
xxxx1001)9IYi. ハケルル
xxxx1010	*:JZJzz. エコハレ
xxxx1011	+;Klk. オサヒロ
xxxx1100	,<L¥1. ハシフワ
xxxx1101	-=M]m. ユスヘン
xxxx1110	.>N^n. ハセホ
xxxx1111	/?O_0. ハツラ

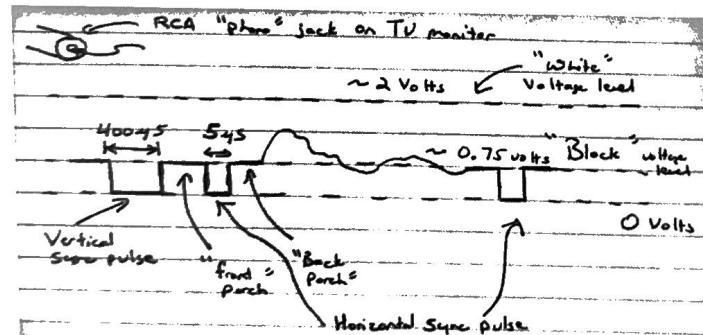
III. Composite video monitors:
"Scans" the screen:



Scans from the top to the bottom 60 times a second.
Scans a (slightly diagonal) horizontal line ~ 15750 times per second. Can vary between 15250 and 16250 Hz. Generally approximately 256 horizontal lines for "NTSC" TV standard.

6

How do we "take control" of a display with a composite input? Feed it an analog signal ("composite"):



- Vertical sync pulse returns the "gun" to the upper left corner of the screen.
- Horizontal sync pulse returns the "gun" to the left side of the screen to start a new "line".
- The shape and width of the sync pulses must be carefully controlled. Incorrect syncs can lead to a wavy or unreadable display.

Use sync generator chips to simplify raster timing.

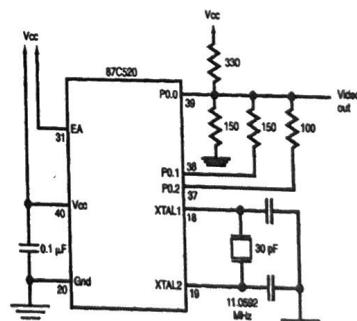
MM5321 and LM 1882 are classic "sync generators"

8275 and 6847 are classic "video display generators" or "controllers"

There are many other modern examples, with variants for fancier displays, e.g., VGA, component video, HDMI, etc.

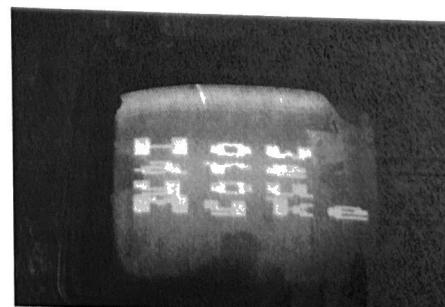
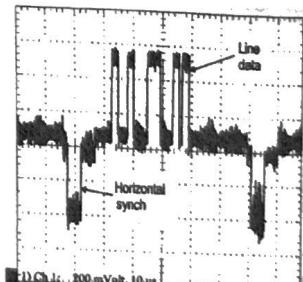
Or, you can actually generate the correct timing pulses directly with your microcontroller!

From Predko's "8051 Microcontroller": (I haven't tried this particular implementation, but the idea is generally sound...)



He's using Port 0 to create an informal video DAC (recall our discussion of the R2R ladder circuit).

"Video out" waveform created by his microcontroller



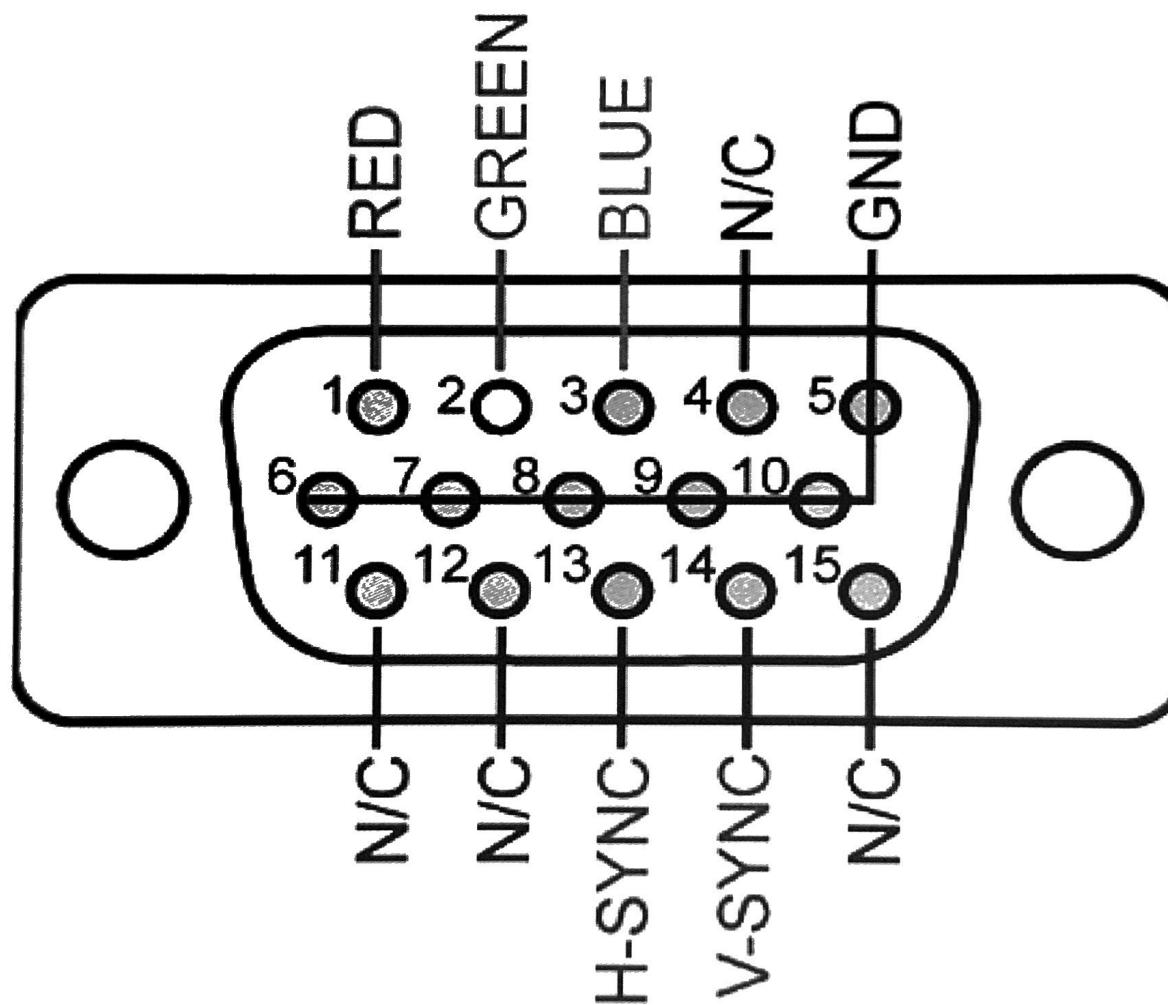
As seen on the video monitor

7

8

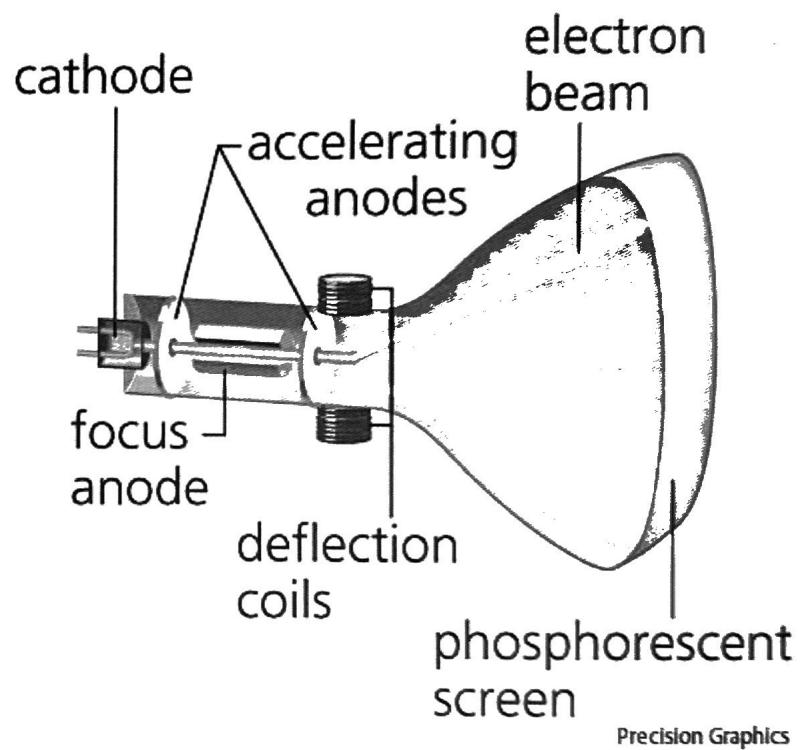
VGA Connection: D15 Sub-Miniature

VGA port, view from Wire Side



VGA: How does it work?

- > the image is drawn line by line, frame by frame
- > the monitor draws the image using 5 signals: **Hsync**, **Vsync**, **Red**, **Green**, and **Blue**
- > each end of **line** is signaled by a **sync pulse** from **Hsync**
- > each end of **frame** is signaled by a different sync pulse from **Vsync**

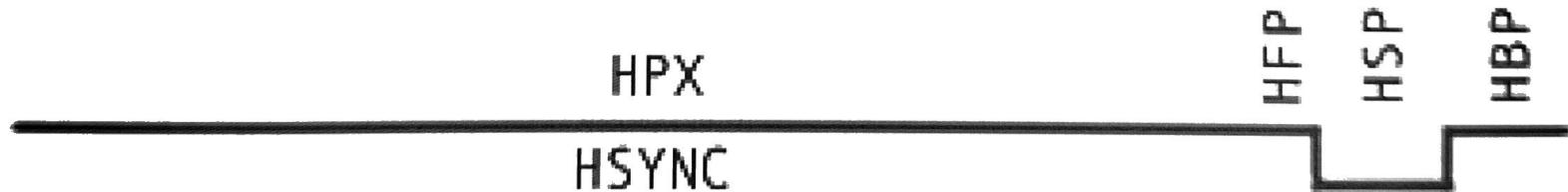


Syncing: Horizontal Sync

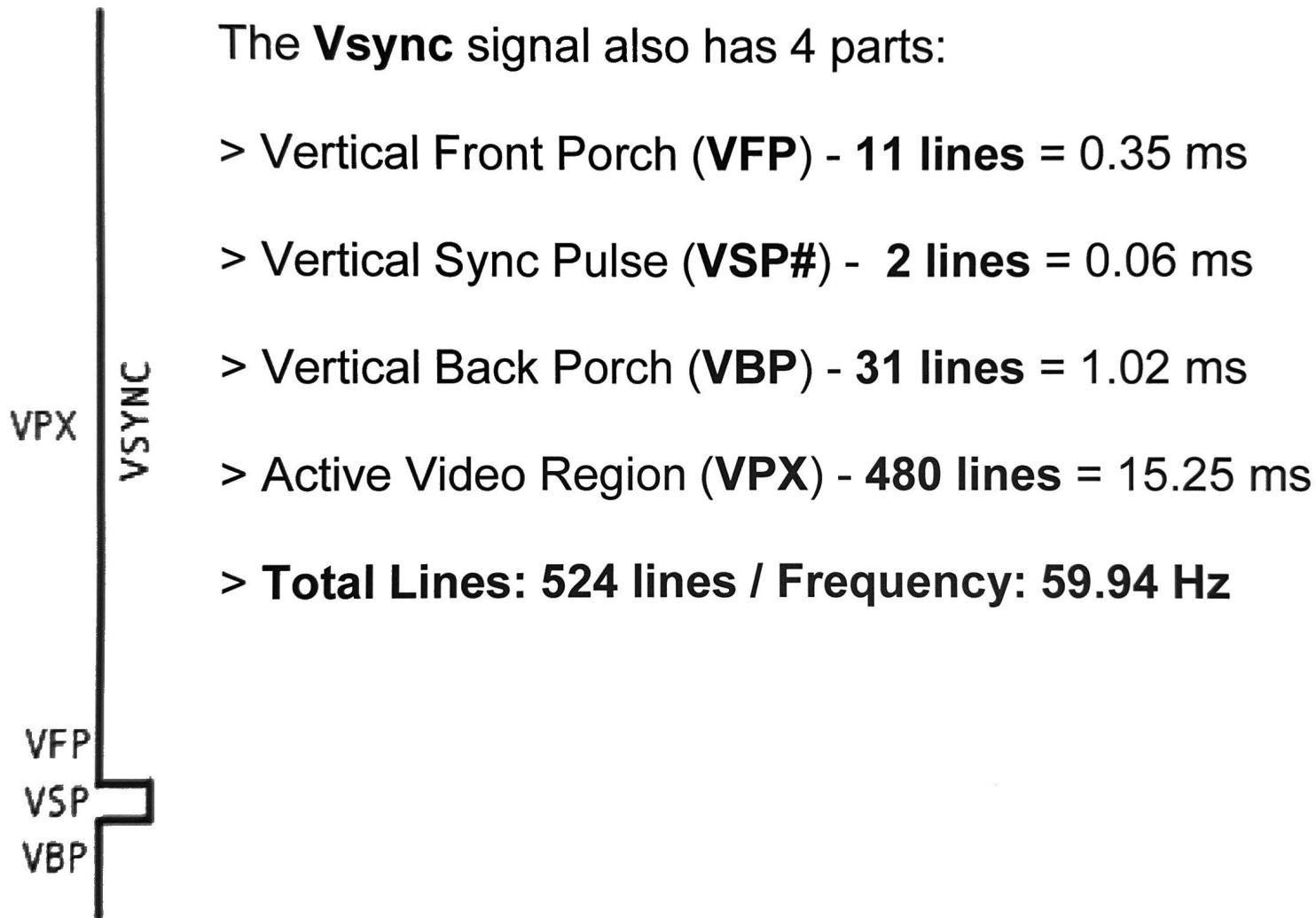
The **Hsync** signal has 4 parts:

- > Horizontal Front Porch (**HFP**) - **0.94 μs**
- > Horizontal Sync Pulse (**HSP#**) - **3.77 μs**
- > Horizontal Back Porch (**HBP**) - **1.89 μs**
- > Active Video Region (**HPX**) - **25.17 μs**
- > **Total Time: 31.77 μs / Frequency: 31.4686 KHz**

indicates signal is active low



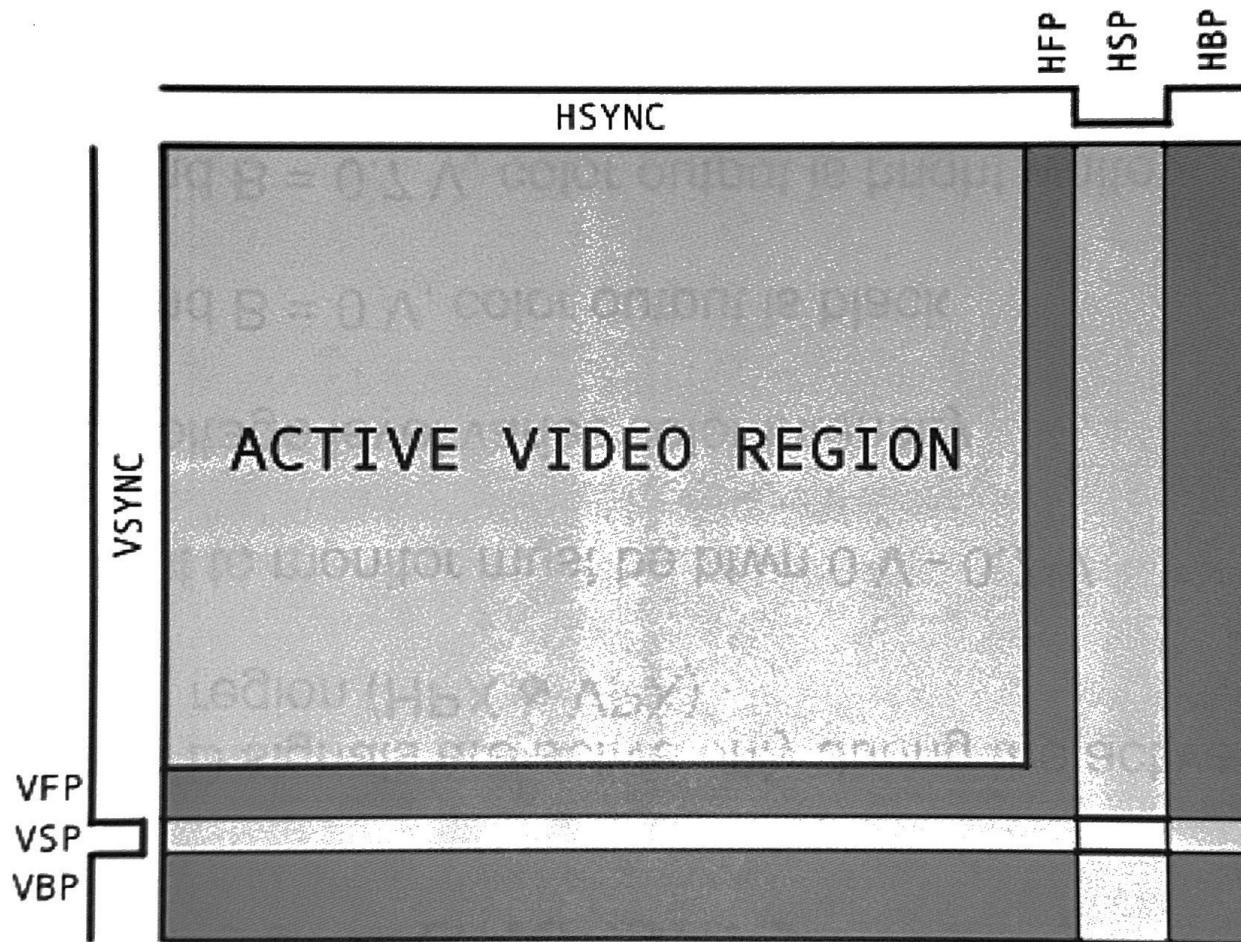
Syncing: Vertical Sync



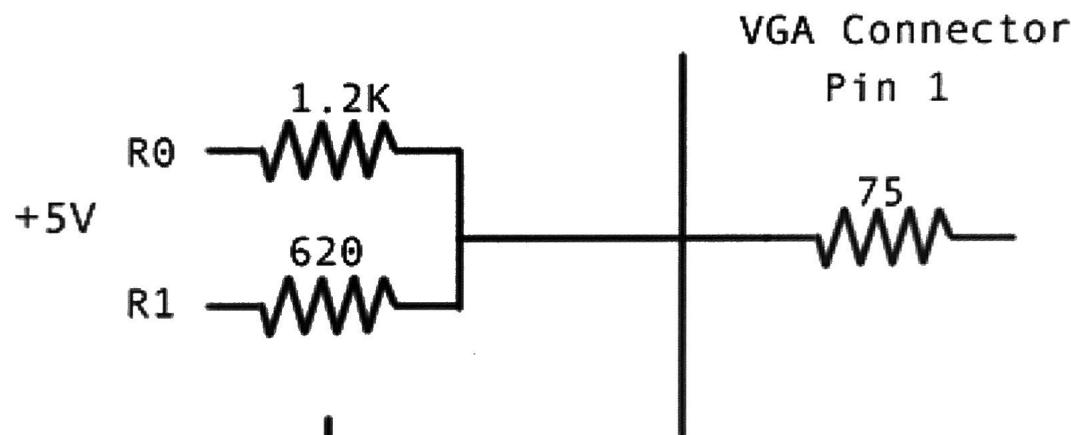
Red, Green, and Blue

- > R, G, and B signals are active only during the active video region (HPX & VPX)
- > RGB input to monitor must be btwn 0 V - 0.7 V
- > varying voltage level varies color intensity
- > if R, G, and B = 0 V, color output is black
- > if R, G, and B = 0.7 V, color output is bright white

Active Video vs. Sync



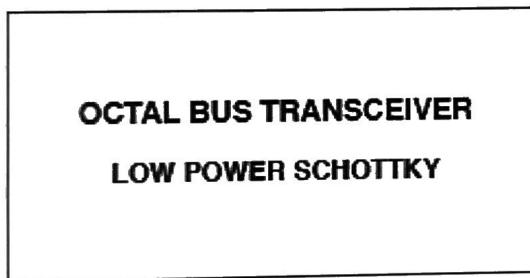
Creating Color! (6-bit resistor DAC)



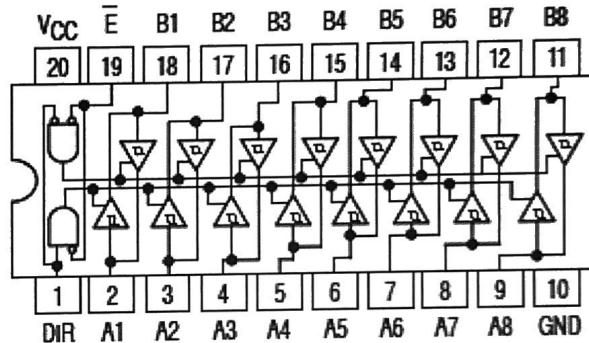
R1, R0	Voltage
0, 0	0 V
0, 1	0.29 V
1, 0	0.54 V
1, 1	0.77 V

The 74LS245

Port 1's internal 30K resistors and the VGA connector's 75 Ohm impedance requires a buffer between the 89C430 and the VGA connector/DAC.



LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)



TRUTH TABLE

INPUTS		OUTPUT
E	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Schematic

