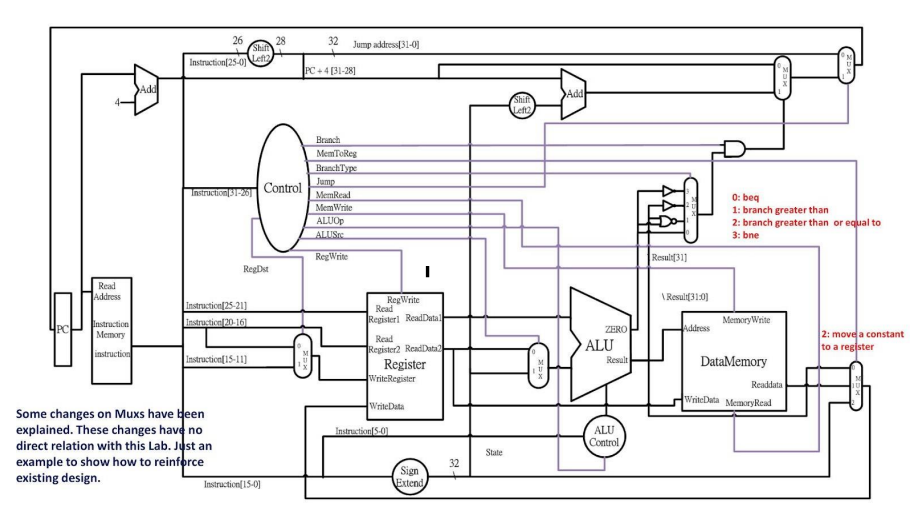
**Computer Organization Lab3**

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**Architecture diagrams:**



**Hardware module analysis:**

**Since this lab is build based on lab2, so lots of structure are the same, I only introduce the different part.**

**Decoder:**

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自動產生的描述

**Since we need to add more instructions, some output need to have more bits and need to add more output ports. Like regdst and memorywrite.**

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自動產生的描述

**After declaring the registers, we follow the MIPS code to assign value and do the corresponding movement of the given op code.**

**ALUCTRL:**

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自動產生的描述

**We assign extra control value for the new instructions according to the given ALUOP.**

**MUX3to1:**

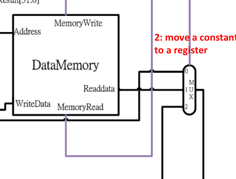
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自動產生的描述

**Since the structure exists 3to1’s mux, we create a mux3to1 module to help us complete the CPU.**

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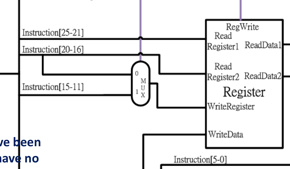
自動產生的描述



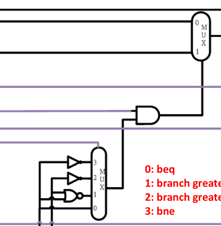
**Above code is for the mux below.**

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自動產生的描述



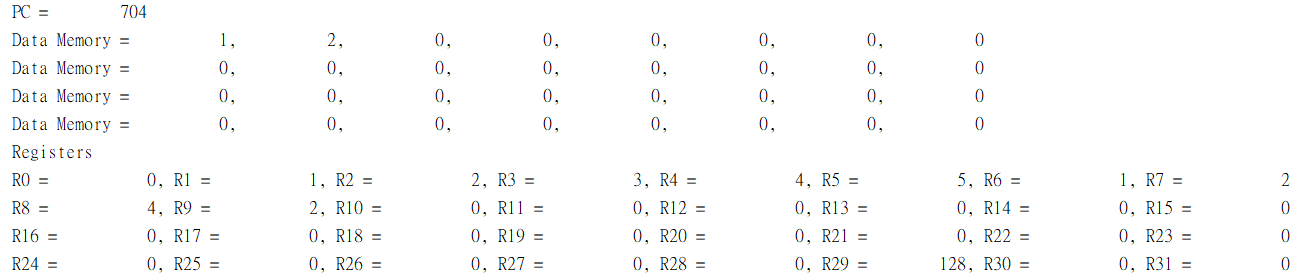
**Above code is for the below mux , for jal , we assign 11111 for muxtoreg.**



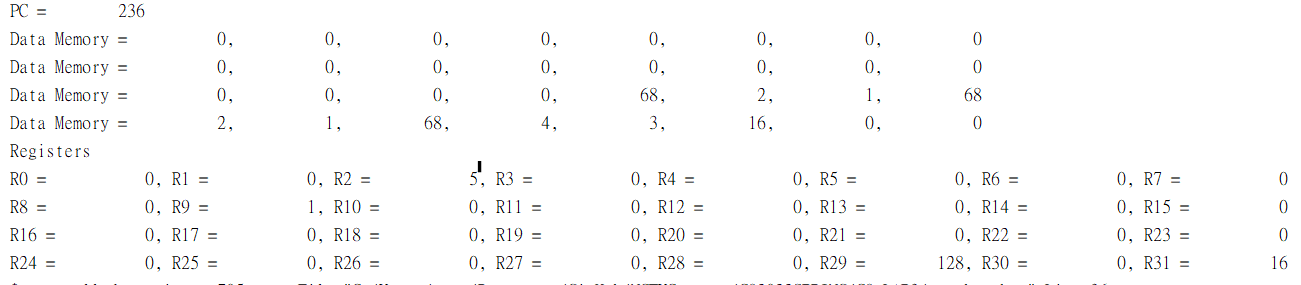
**This 4to1mux’s output can be simplified into adder\_select(zero&branch) in the code, so we don’t need a mux to generate control for the 2to1mux.**

**Finished part:**

**Data1:**



**Data2:**



**Both result satisfies the answer.**

**Problems you met and solutions:**

**I once find the output is slightly different from the answer, but I don’t think my structure is wrong, after many double-checks, I find the problem is I have a register’s size too small, after adding an extra bit, the output is correct.**

**Summary:**

**This lab is very similar to lab2, so I first think it’s easy, but after having many bugs on my design, I find myself too careless on my coding, the structure is similar indeed, but it has a lot of details to check, which are so small that you wouldn’t expect to have problem, I think I need to be careful on my next design.**