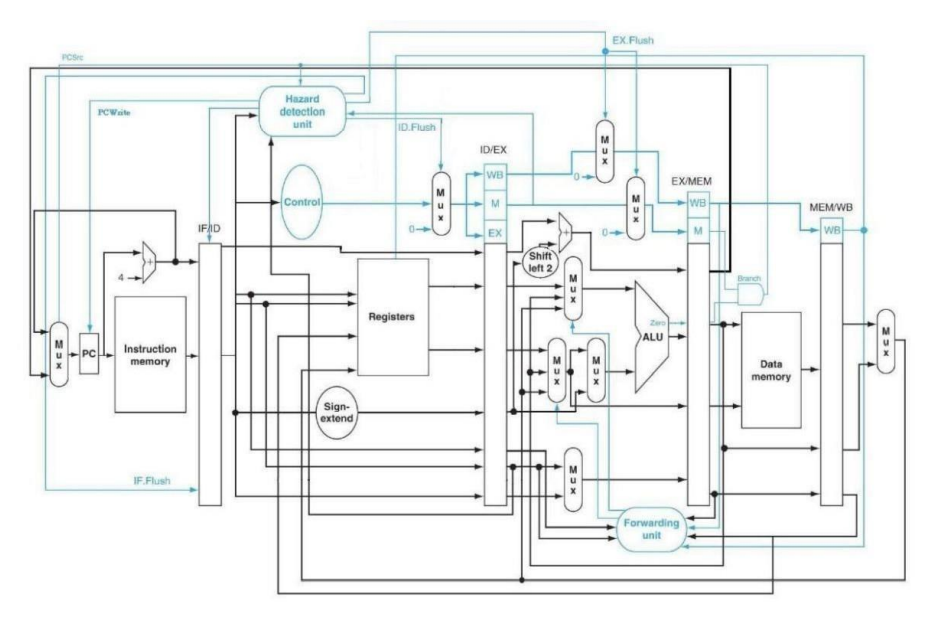
**Computer Organization Lab5**

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**Architecture diagrams:**



**Hardware module analysis:**

**Forwarding unit:**

**We assign value of forwarding A and B by the below table:**

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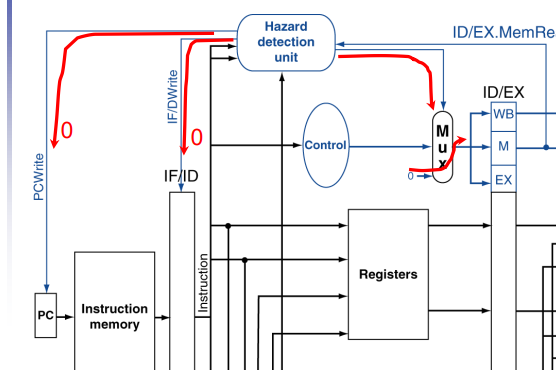
自動產生的描述

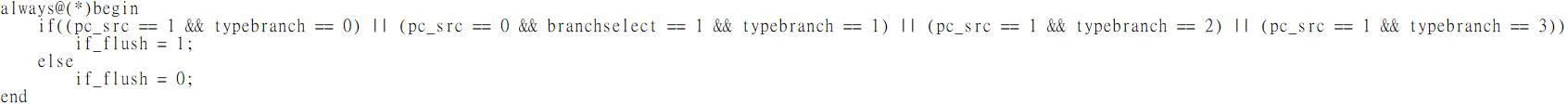
**Hazard detection:**

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自動產生的描述

**If above situation happens, or instructions need to branch, we need to flush the pipe register of below.**





**(The if conditions will be explained in alu)**

**And we need to control the write register signal to 0 to prevent the register’s value is changed into the wrong value.**

**Decoder:**

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自動產生的描述

**We assign additional variables for extra branch instructions, and since branch has new types, we assign a new register branchtype to tell which branch instruction it is.**

**ALU\_ctrl:**

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自動產生的描述

**According to the new opcode, we assign new control value to ALU.**

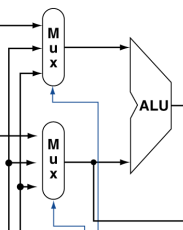
**ALU:**

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自動產生的描述

**Ctrl4 is for bgt, ctrl6 is for beq and bne, ctrl7 is for bge. If these need to branch, the zero will be set into 1 except bne, after anding zero and branch, we send the value to hazard detect to check whether we need to flush instructions.**

**Mux3to1:**



**We add 3to1 mux for the alu and the control is the forward unit output.**

**Pipe\_reg:**

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自動產生的描述

**We add some variables for data hazard. Bratype(branchtype) is generated in decoder and inputs in hazard detection.**

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自動產生的描述

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自動產生的描述

**And we have the new added module for forwarding and hazard detection unit.**

**Finished part:**

**Data1:(clock15)**

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自動產生的描述

**Data2:(clock59)**

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自動產生的描述

**Problems you met and solutions:**

**I had trouble on the program counter since I think my design is correct, but it still failed to read data. After asking classmates for help, I find out that I need to add write signal as additional input, after debugging the problem was solved.**

**Summary:**

**The concept of this lab is far more difficult from the previous ones, not only we need to take care of the forwarding and hazard detect, but we need to add additional instructions for branch, this is the most difficult part, it took me 2 days to finish only a portion of it, after that, I find myself exhausted for debugging, but it’s good to know that the semester is finally over, what a relief.**