KHULNA UNIVERSITY OF ENGINEERING & TECHNOLOGY

PROJECT REPORT

DESIGN & IMPLEMENTATION OF A DIGITAL CLOCK BASED ON 59 SECONDS & MINUTES.

SUBMITTED BY:

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- **Objectives:**

- To implement the concepts of synchronous counter and know about its' applications.

- To implement the concepts of Flip-Flops and learn about its' various applications.

- To apply some critical logics in circuit design.

- To implement and utilize multiple circuits and integrate them into a single circuit.

- To know about the working method of a digital clock.

- To implement the topics learnt throughout the semester.

- **Introduction:**

In the dynamic realm of digital electronics and embedded systems, the pursuit of designing an advanced digital clock has been a captivating exploration. A digital clock runs on the principle of counter. The counters are designed by flip flops. To display the time, seven segment display is used. Now we had to design a clock which will skip the 17^{th} second & 17^{th} minute.

Project Details:

- Firstly, we have designed and implemented circuit for a 0 to 9 (mod 10) counter.

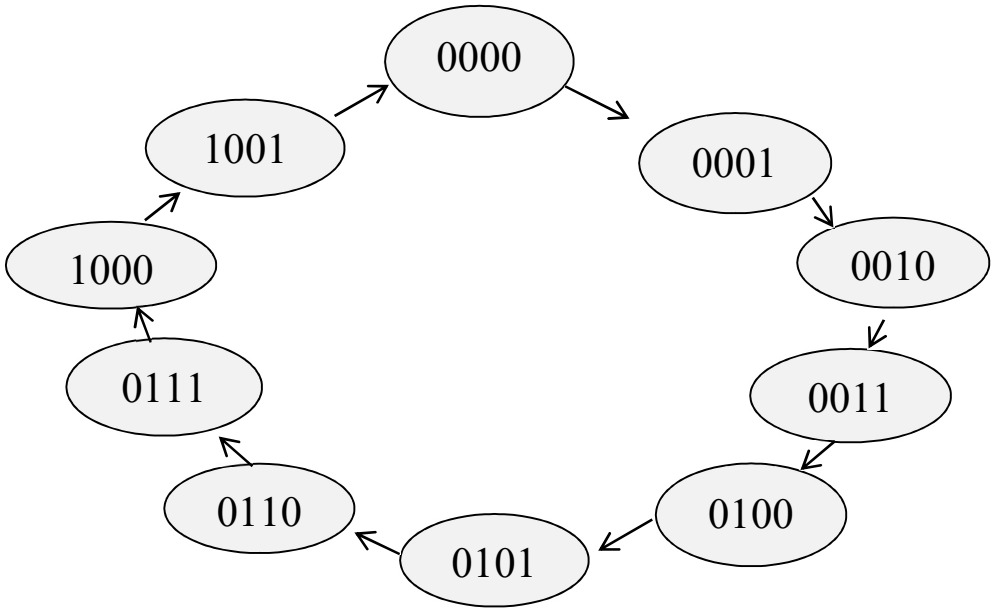


Fig: State Diagram for a O to 9 (mod 10) counter

State table for 0 to 9 (mod 10) counter using J-K Flip-Flops:

Present State				Next state				JK flip flop input							
Q3	Q2	Q1	Q0	$Q3^+$	$Q2^+$	$Q1^+$	$Q0^+$	J3	K3	J2	K2	J1	K1	J0	K0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

Determining Boolean expressions using K-Map:

FOR J3:

Q3Q2 \ Q1Q0	00	01	11	10
00				
01			1	
11	X	X	X	X
10	X	X	X	X

J3 = Q2.Q1.Q0

FOR J2:

Q3Q2 \ Q1Q0	00	01	11	10
00		1		
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J2 = Q1.Q0

FOR J1:

Q3Q2 \ Q1Q0	00	01	11	10
00		1	X	X
01		1	X	X
11	X	X	X	X
10			X	X

AS IN J0 THERE IS NO 0,THE FUNCTION FOR J0 SHOULD BE 1. J0 = 1

J1 = Q3'Q0;

FOR K3:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	X
01	X	X	X	X
11	X	X	X	X
10		1	X	X

K3 = Q0

FOR K2:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	X
01			1	
11	X	X	X	X
10	X	X	X	X

K2 = Q1.Q0

FOR K1:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	1	
01	X	X	1	
11	X	X	X	X
10	X	X	X	X

K1 = Q0.

K0=1.

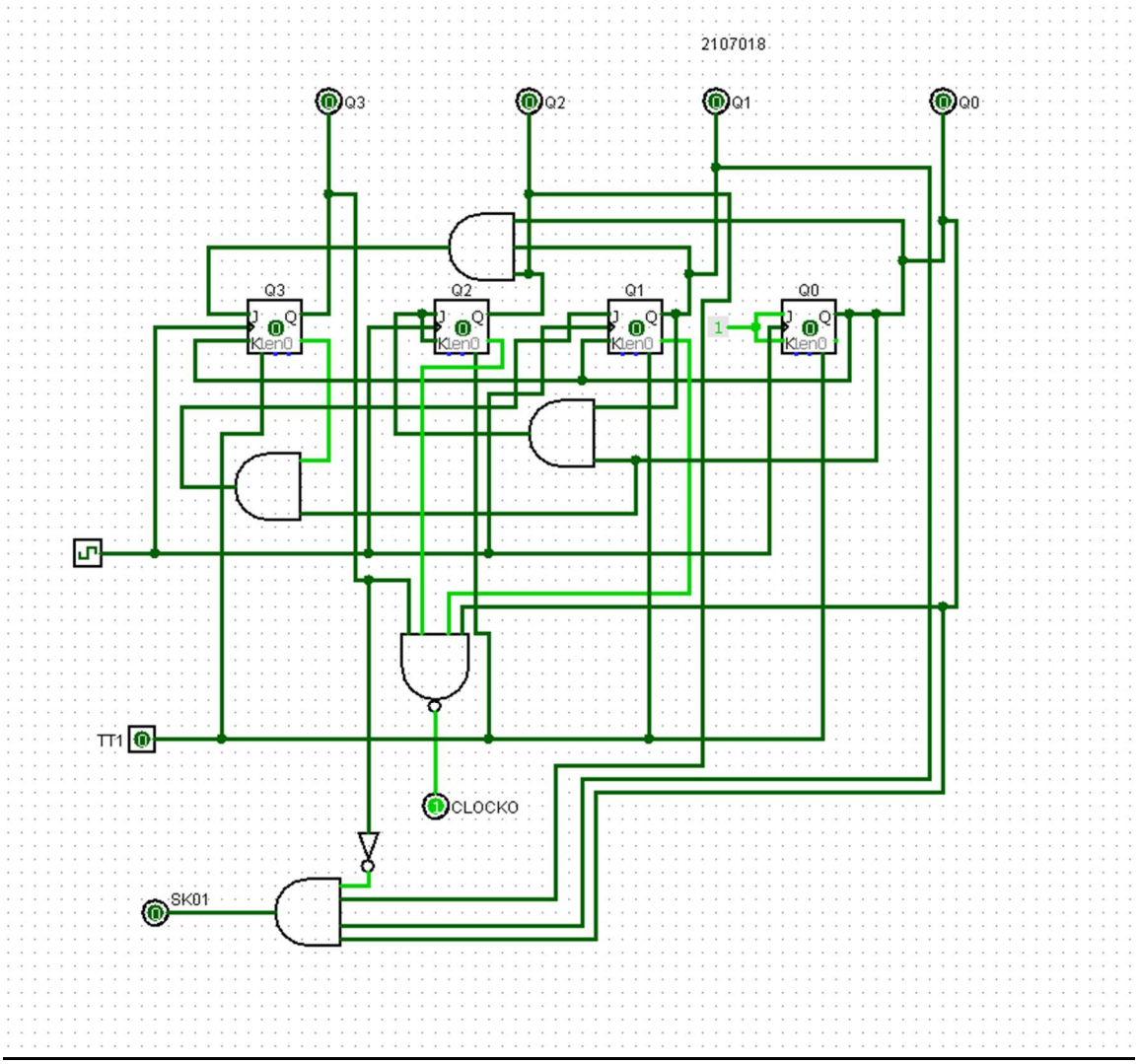


Fig: 0 to 9 (mod 10) counter

Here this is a 0 to 9 (mod 10) counter. This counter is used to count the right digit of the second, minute, and hour.

Here the counter is implemented with J-K flip-flops according to the functions stated above. Then clock pulse was given. When the counter gets 0, it gives an output 1 which was passed to the left digits of seconds, minutes and hours as clock signal.

- Secondly, we have designed and implemented circuit for 0 to 5 (mod 6) counter.

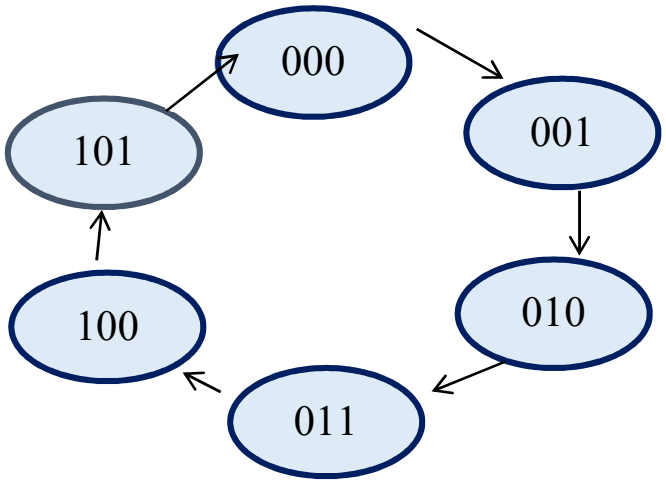


Fig: State Diagram for 0 to 5 (mod 6) counter

State table for 0 to 5 (mod 6) counter using J-K Flip-Flops:

Present State				Next state				JK flip flop input					
Q3	**Q2**	**Q1**	**Q0**	**$Q3^+$**	**$Q2^+$**	**$Q1^+$**	**$Q0^+$**	**J2**	**K2**	**J1**	**K1**	**J0**	**K0**
0	0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	X	0	1	X
0	0	1	1	0	1	0	0	1	X	X	1	X	1
0	1	0	0	0	1	0	1	X	0	0	X	1	X
0	1	0	1	0	0	0	0	X	1	0	X	X	1

Determining Boolean expressions using K-Map:

For J2:

Q3Q2 \ Q1Q0	00	01	11	10
00		1		
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J2=Q1.Q0

For K2:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	X
01		1	X	X
11	X	X	X	X
10	X	X	X	X

K2=Q0

For J1:

Q3Q2 \ Q1Q0	00	01	11	10
00		1	X	X
01			X	X
11	X	X	X	X
10	X	X	X	X

J1=Q2'Q0

The k map for K1 is same as J1. So,
K1 = Q2'Q0.
J0 = K0 = 1
J3=K3=0(GRND)

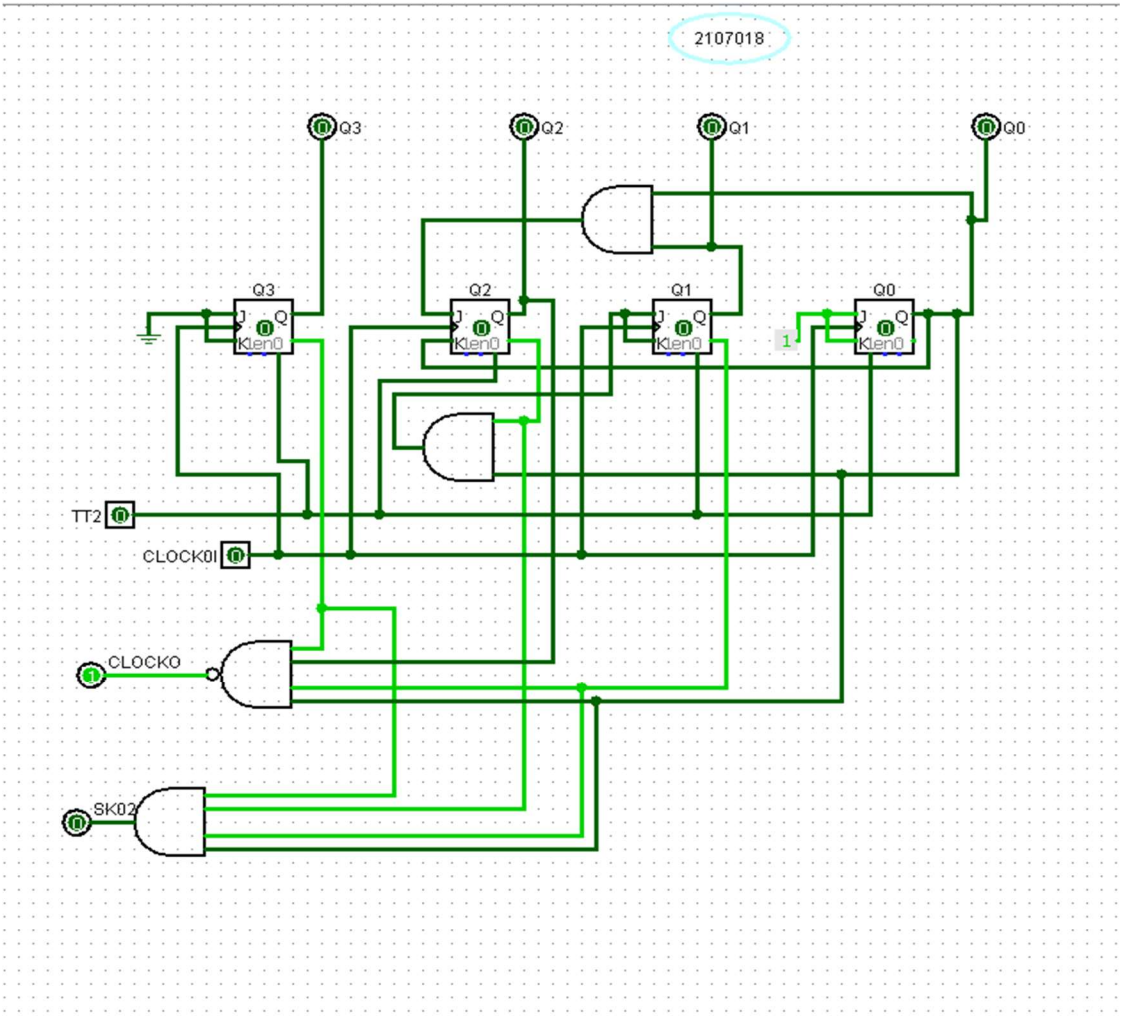


Fig: 0 to 5 (mod 6) counter

Here this is a 0 to 5 (mod 6) counter. This counter is used to count the left digit of the second and minute.

Here the counter is implemented with J-K flip-flops according to the functions stated above. Here the clock pulse was given from right digit of the second and right digit of the minute. When the counter gets 0, it gives an output 1 which was passed to the left digits of minutes and hours as clock signal.

- Then, we have designed and implemented circuit for 0 to 2 (mod 3) counter.

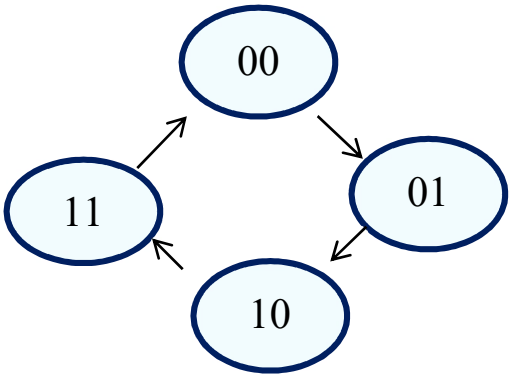


Fig: State Diagram for 0 to 2 (mod 3) counter

State table for 0 to 9 (mod 10) counter using J-K Flip-Flops:

Present State				Next state				Flip-flop inputs			
Q3	**Q2**	**Q1**	**Q0**	**$Q3^+$**	**$Q2^+$**	**$Q1^+$**	**$Q0^+$**	**J1**	**K1**	**J0**	**K0**
0	0	0	0	0	0	0	1	0	X	1	X
0	0	0	1	0	0	1	0	1	X	X	1
0	0	1	0	0	0	0	0	X	1	0	X

Here,

J2=K2=0(GRND)

J3=K3=0(GRND)

Determining Boolean expressions using K-Map:

FOR J1:

Q3Q2 \ Q1Q0	00	01	11	10
00		1	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J1 = Q0

FOR K1:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	X	X	1
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

K1 = 1

FOR J0:

Q3Q2 \ Q1Q0	00	01	11	10
00	1	X	X	
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

J0 = Q1'

FOR K0:

Q3Q2 \ Q1Q0	00	01	11	10
00	X	1	X	X
01	X	X	X	X
11	X	X	X	X
10	X	X	X	X

K0 = 1

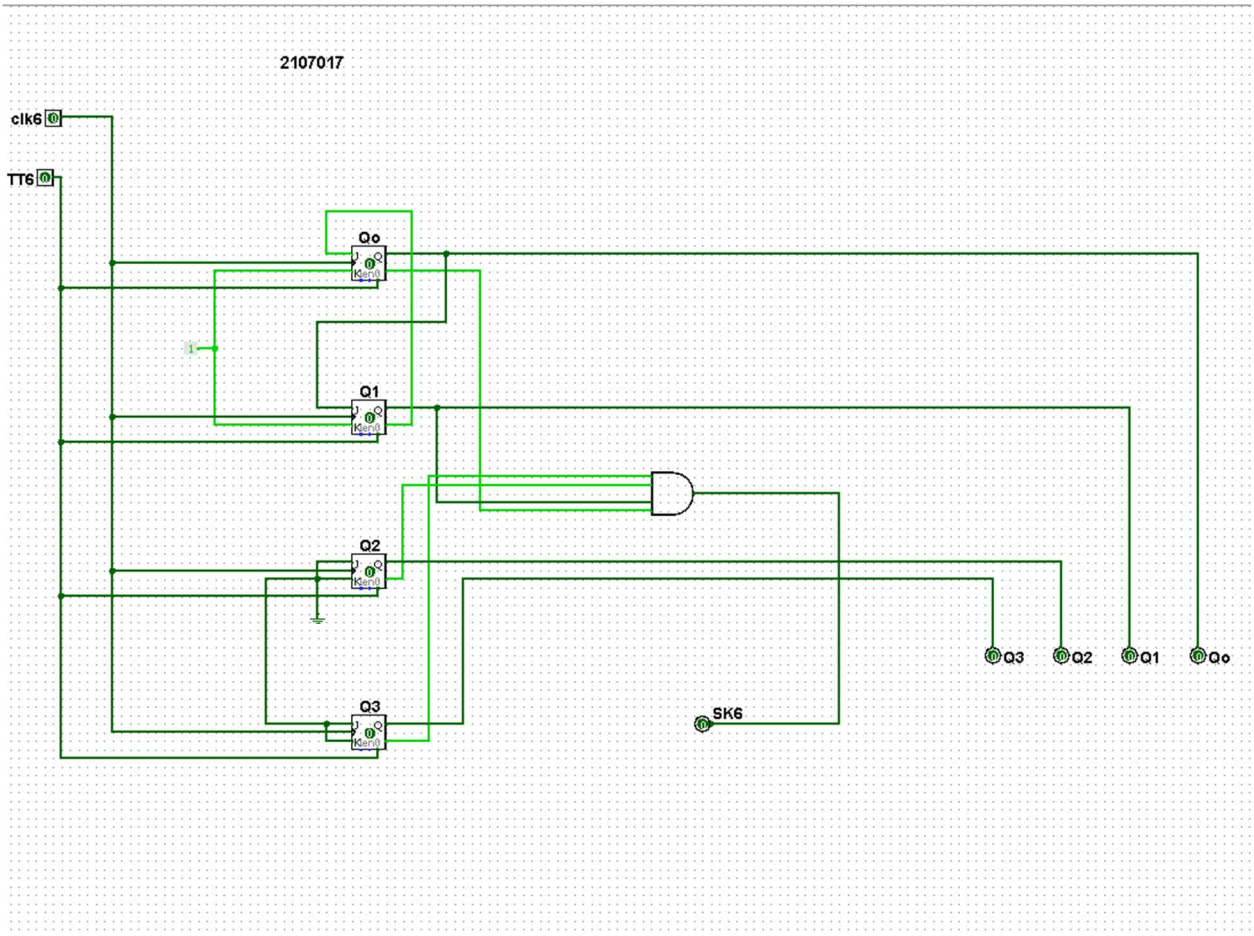


Fig: 0 to 2 (mod 3) counter

Here this is a 0 to 2 (mod 3) counter. This counter is used to count the left digit of the hour.

Here the counter is implemented with J-K flip-flops according to the functions stated above. Here the clock pulse was given from right digit of hour.

- We have also designed and implemented decoder circuit for displaying digits (0-9) in a 7 segment display.

Truth table for seven segment display:

Input				Output						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

Boolean Functions :

- a=A+C+BD+B’D’
- b=B’+C’D’+CD
- c=B+C’+D
- d=B’D’+CD’+BC’D+A
- e=B’D’+CD’
- f=A+C’D’+BC’+BD’
- g=B’C+CD’+BC’+A

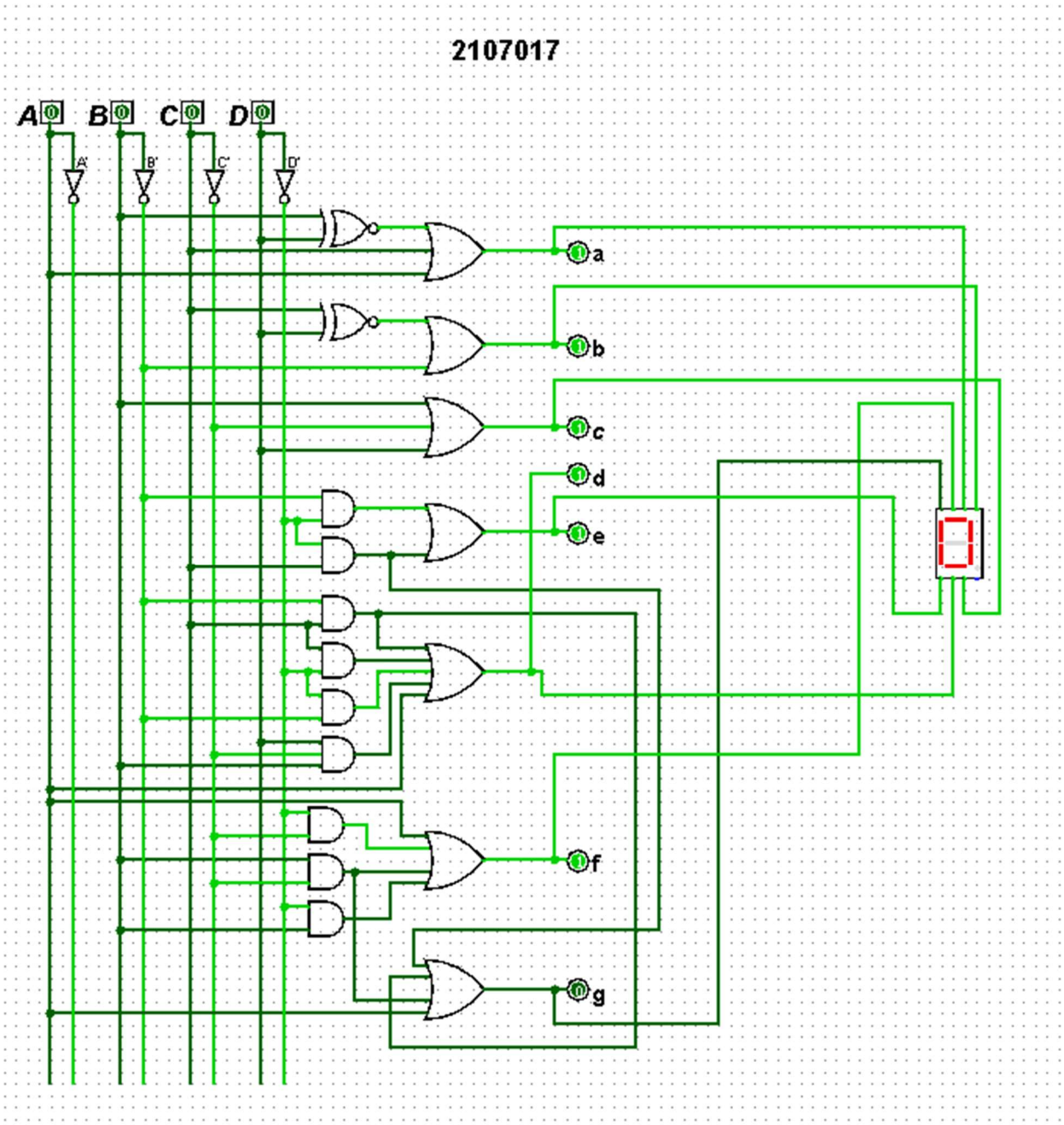
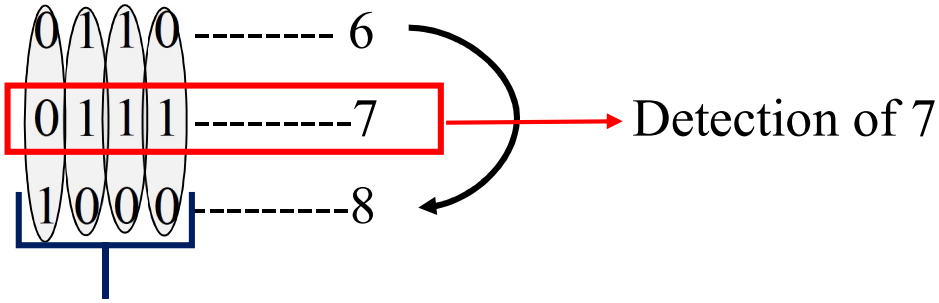


Fig: 7 segment decoder

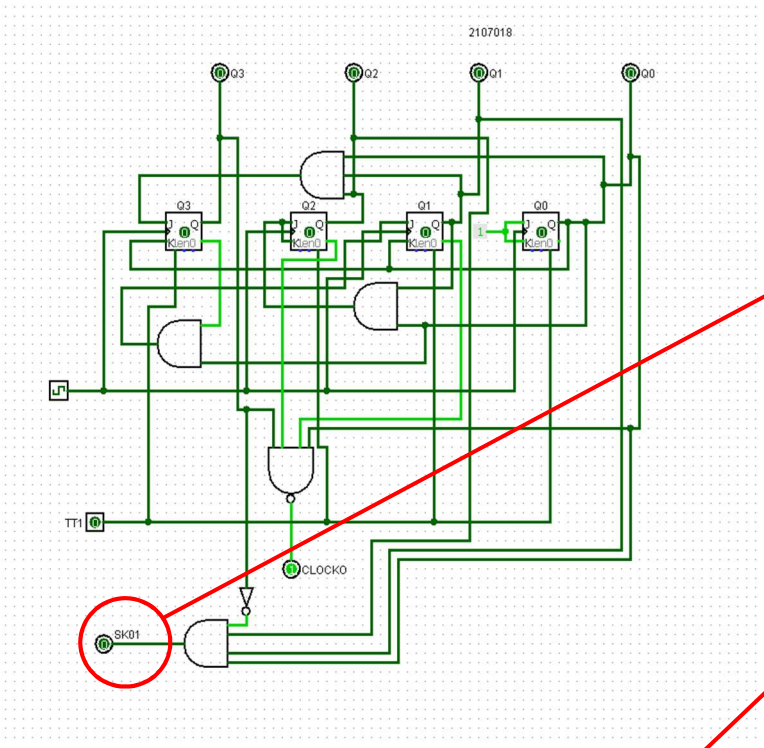
Here this is a 7 segment decoder circuit which displays digits (0 to 9). This is used to display the counting digits of the clock of second, minute and hour.

- We have implemented logics to skip 17th second and minute in our clock.

To skip the 17th second, 6 was detected in the right digit of the second. It was passed as output to main. Then 1 was detected in the left digit of the second. This was also passed to main function. The output from those circuits were ANDed and it was passed to the preset pin of the Q0 flip flop.

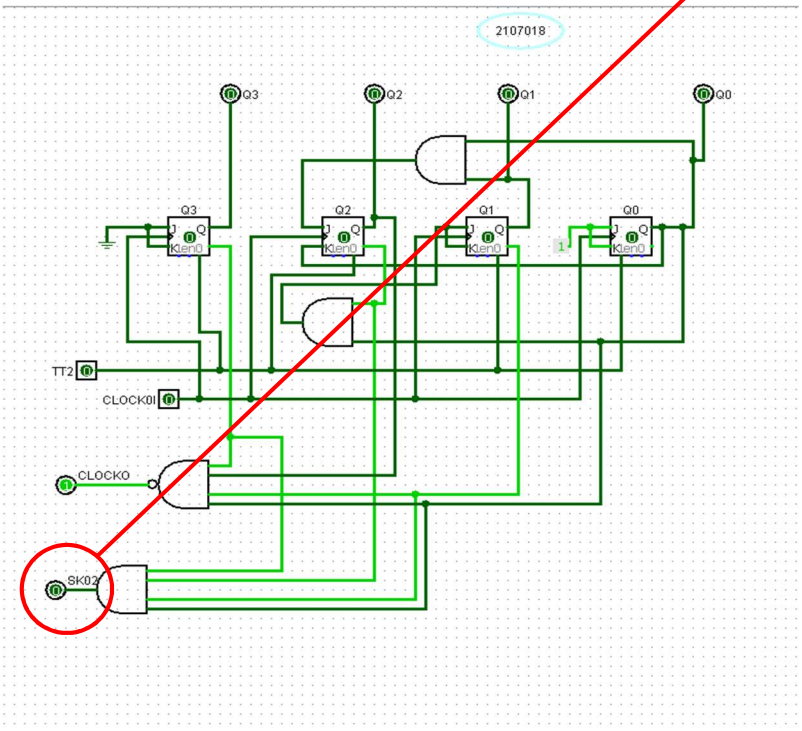


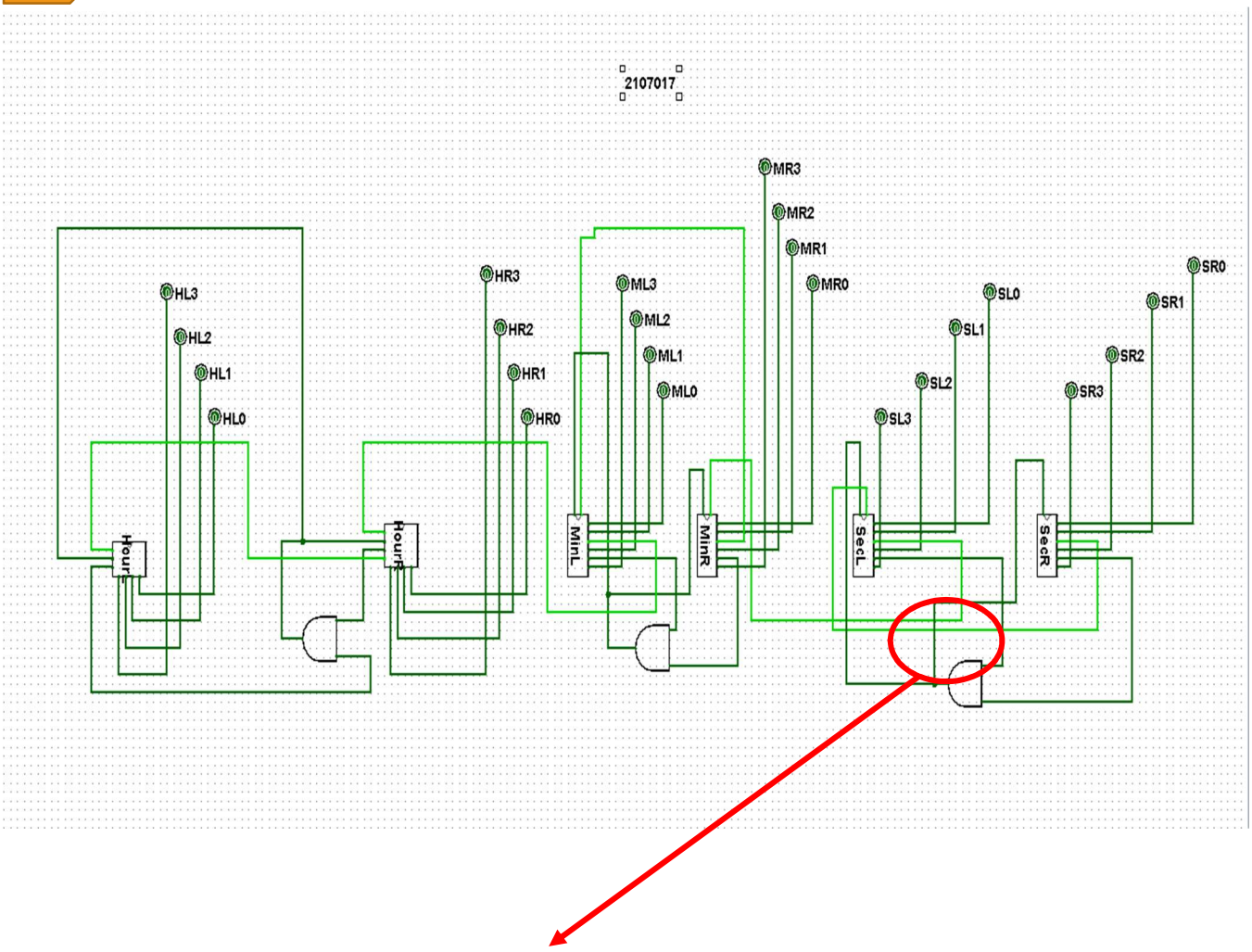
To skip 7, All the four bits need to be changed as shown in the picture. But in this logic it will always skip 17, 27, 37, 47, 57 . But we only need to skip 17, the rest of the numbers should remain unchanged. So an output will be passed from the minute left and second left after detecting 1. And the output of 7 detection and output of 1 detection got ANDed and passed to the preset pins of the flip-flops in the second right and in the minute right. Thus the 17th was skipped in the second and minute section.



This detects 7

This detects 1



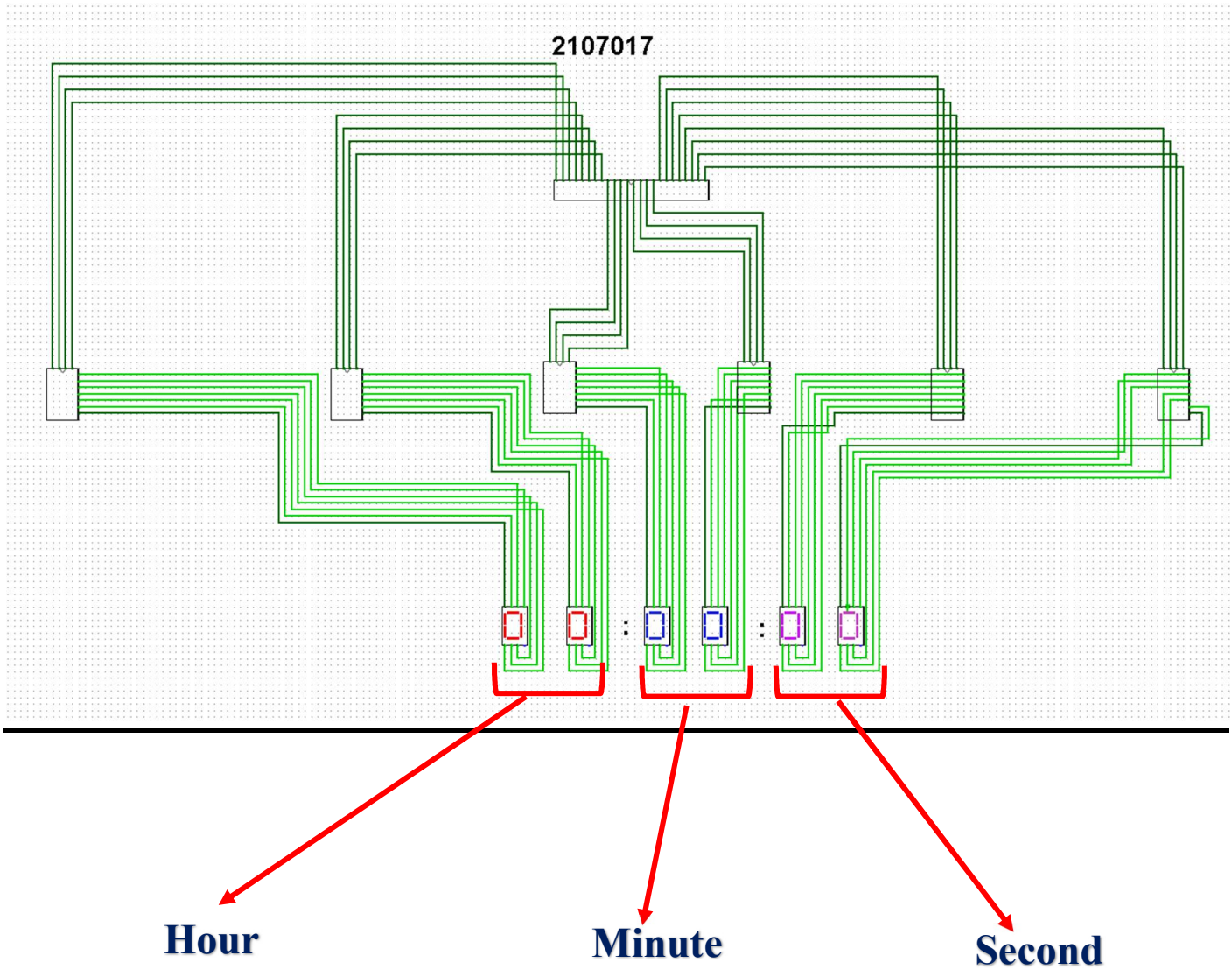


Here detection of & and detection of 1 are being ANDed

- It is a 24 hour clock.

It is a 24 hour format clock which means it will be reset when the clock shows 23:59:59. To do this, in the hour left circuit detects 2 and the hour right circuit detects 4 ,when both 2 and 4 detected at a time the output are passed through an AND gate and the output from the AND gate is passed to reset for both hour left and hour right circuit.

Main Clock Diagram:



- **Required Components:**

1. IC 7408 (AND Gate)
2. IC 7400 (NAND Gate)
3. IC 7404 (NOT Gate)
4. IC 7432 (OR Gate)
5. IC 7486 (XNOR Gate)
6. IC 7476 (J-K Flip-Flop)
7. Constant [1]
8. Ground [0]
9. 7 Segment Display

- **Discussions:**

In the pursuit of completing our clock project, we encountered various challenges that demanded meticulous planning, design considerations, and collaborative problem-solving. The primary goal was to design a clock that accurately counts the right digit of seconds, minutes, and hours, resetting to zero at the appropriate intervals and also build and implement logics for skipping 17^{th} digit in second and minute.

- **Conclusion:**

Our clock project successfully addressed the challenges encountered during its development. Throughout the development process, we consulted resources such as the "Digital Logic Design" book and leveraged online references like Wikipedia to deepen our understanding and overcome specific challenges. The successful completion of the clock project not only demonstrates our technical skills but also underscores the significance of effective collaboration and problem-solving in engineering projects.