Physics-Based Circuit-Compatible SPICE Model for Ferroelectric Transistors

Ahmedullah Aziz, Swapnadip Ghosh, Suman Datta, *Fellow, IEEE*, and Sumeet Kumar Gupta, *Member, IEEE*

***Abstract*— We present a SPICE model for ferroelectric transistors (FEFETs) based on time-dependent Landau–Khalatnikov equation solved self-consistently with the transistor equations. The model also considers depolarization fields due to non-ideal contacts. We experimentally characterize FE films to calibrate our model, based on which we analyze the device and circuit implications of FEFETs. We discuss the dependence of the ON current and gate capacitance of FEFETs on the FE thickness and FE material parameters. A ring oscillator analysis shows delay reduction up to 97% at iso-energy for FEFETs compared with MOSFETs at V_{DD} < 0.4 V. FEFET-based SRAMs show 47%–68% larger read stability and 50%–57% lower access time, albeit with an increase in the write time.**

***Index Terms*— Circuit-compatible model, depolarization field, ferroelectric FET, Landau Khalatnikov equation, negative capacitance, SPICE, SRAM.**

I. Introduction

FERROELECTRIC field effect transistor (FEFET) is an emerging steep switching device, which utilizes the negative capacitance of the ferroelectric (FE) to induce a voltage step-up action in the gate stack (Fig. 1) [1]. While the device aspects of FEFETs are being widely investigated [2]–[4], exploration of FEFET-based circuits requires a circuit compatible model to enable efficient design and analysis.

In this letter, we present a physics-based circuit-compatible SPICE model for FEFETs based on single-domain approximation. The model employs time-dependent Landau Khalatnikov (LK) equation to obtain the relationship between electric-field (E) and polarization (P) of the FE. LK equation is coupled with the transistor models in a self-consistent fashion to predict the characteristics of FEFETs. Distinct from the previous modeling techniques for FEFETs, which employ device simulators [4] [5] to integrate 1-D LK equation with transistor models, the proposed approach solves these equations entirely in SPICE. Hence, our model facilitates self-consistent coupling of the FE capacitance (C_{FE}) with the capacitance of the underlying MOSFET (C_{MOS} – Fig. 1) and other circuit capacitances, considering polarization transients. Further, unlike previous circuit compatible models of FE (*not* FEFET) that are based on approximate solutions of LK equation [6], [7], our model solves the time-dependent LK equation *exactly* and couples the solution to transistor models.

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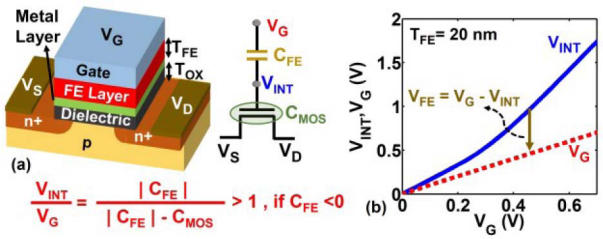

Fig. 1. (a) Ferroelectric transistor (FEFET). The metal layer below FE may or may not be present. (b) Voltage step-up action in FEFET showing $V_{INT}/V_G > 1$.

II. Physics-Based SPICE Model

To model FEFETs in SPICE, we first obtain the equivalent circuit for time (t)-dependent LK equation [6], given below.

$$E - \rho dP/dt = \alpha P + \beta P^3 + \gamma P^5 \tag{1}$$

Here, α, β and γ are the static parameters of the FE and ρ is the kinetic coefficient. Let V_{FE} be the voltage across FE, and A_{FE} and T_{FE} be its area and thickness, respectively. Thus, using $E = V_{FE}/T_{FE}$ and defining $Q_P = A_{FE}P$, we obtain

$$V_{FE} = (\rho \frac{T_{FE}}{A_{FE}} \frac{dQ_P}{dt}) + (T_{FE}\{\frac{\alpha Q_P}{A_{FE}} + \frac{\beta Q_P^3}{A_{FE}^3} + \frac{\gamma Q_P^5}{A_{FE}^5}\}) \tag{2}$$

Noting that Q_P is the charge and dQ_P/dt is the current, we model (2) in SPICE with a non-linear capacitor (C_{LK}) in series with a resistor ($R_{LK} = \rho T_{FE}/A_{FE}$) [7], as shown in Fig. 2(a). The first and second terms on the right hand side of (2) represent the voltage drops across R_{LK} (V_{R_LK}) and C_{LK} (V_{C_LK}), respectively.

To model C_{LK} in SPICE, we express Q_P as a function of V_{C_LK} and a feedback voltage (V_{FB}) given by

$$V_{FB} = (\beta T_{FE} Q_P^3/A_{FE}^3 + \gamma T_{FE} Q_P^5/A_{FE}^5) \tag{3}$$

From (3) and the second term in (2),

$$Q_P = (A_{FE}/\alpha T_{FE})(V_{C\_LK} - V_{FB}) \tag{4}$$

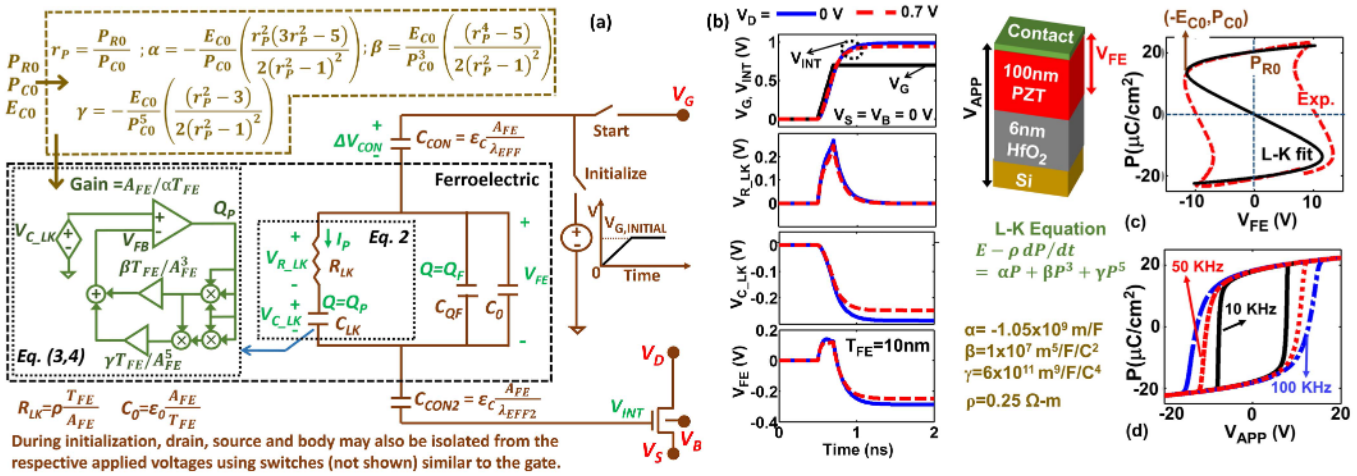

Fig. 2. (a) Proposed SPICE model for FEFETs (b) An example response of V_{INT}, V_{C_LK}, V_{R_LK}, V_{FE} to the gate voltage (V_G). (c) Calibration of model with experiments (Exp.) and (d) FE response to varying triangular pulse frequency of applied voltage (V_{APP}).

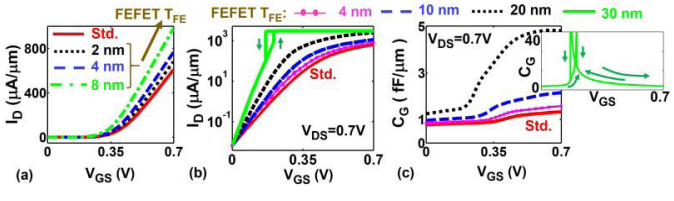

Fig. 3. (a-b) Current (I_D) and (c) gate capacitance (C_G) versus gate-to-source voltage (V_{GS}) of FEFETs and standard MOSFETs (Std.). Frequency of applied voltage for quasi-DC simulation = 10KHz.

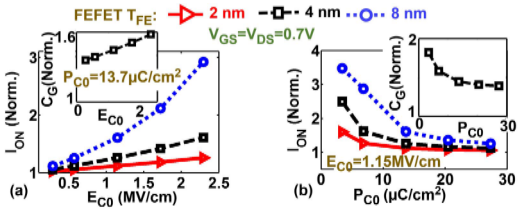

Fig. 4. ON current (I_{ON}) and gate capacitance (C_G) (normalized with respect to MOSFET) versus (a) E_{C0} and (b) P_{C0}.

Fig. 2(a) shows the equivalent circuit for (3) and (4). We model C_{LK} as a charge conserved capacitor [8] with charge = Q_P.

The total charge in the FE (Q_{FE}) is given by

$$Q_{FE} = A_{FE}(\varepsilon_0 E + P) = ((\varepsilon_0 A_{FE}/T_{FE})V_{FE} + Q_P) \quad (5)$$

Here, ε_0 is vacuum permittivity. We model FE using a capacitor C_0 (= $\varepsilon_0 A_{FE}/T_{FE}$) in parallel with R_{LK}-C_{LK} network (Fig. 2(a)).

In Fig. 2(a), we also show expressions for α, β and γ in terms of P_{R0} (= $|P|$ @ $E = 0$), E_{C0} (= $|E|$ @ $dE/dP = 0$ on the S curve – Fig. 2(c)) and P_{C0} (= $|P|$ @ $E = E_{C0}$). These expressions have been derived analytically using static L-K equation. These formulae can be used to simplify the model calibration since P_{R0}, E_{C0} and P_{C0} can be readily estimated from the *P-E* experimental data.

The model also includes the effect of fixed charges (Q_F) in the FE using a charge-conserved capacitor (C_{QF} - Fig. 2(a)). Additionally, we model the depolarization field [9] associated with non-ideal contacts. We assume the charge density of the contact (ρ_{CON}) to be exponentially decaying along the contact thickness (T_M) with a screening length λ [10]. The depolarization leads to a voltage drop ΔV_{CON}, obtained from Poisson's equation as:

$$\Delta V_{CON} = (\lambda_{EFF} Q_{FE})/(\varepsilon_C A_{FE}) \quad (6)$$

Here, ε_C is the permittivity of the contact and λ_{EFF} is given by

$$\lambda_{EFF} = \lambda - T_M(\exp(-T_M/\lambda))/(1 - \exp(-T_M/\lambda)) \quad (7)$$

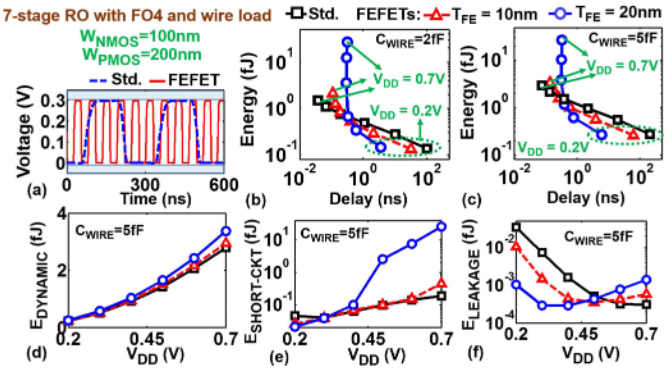

Fig. 5. (a) Ring oscillator (RO) waveforms at V_{DD} = 0.3V (b-c) Energy-delay of MOSFET (Std.) and FEFET-based inverters for different wire capacitance (C_{WIRE}) (d-f) Comparison of dynamic ($E_{DYNAMIC}$), short-circuit ($E_{SHORT-CKT}$) and leakage energy ($E_{LEAKAGE}$).

Thus, the contact is modeled as a capacitor C_{CON} = $\varepsilon_C A_{FE}/\lambda_{EFF}$.

To model FEFETs, we connect the equivalent circuit for FE and capacitor C_{CON} in series with MOSFET/FinFET (Fig. 2), which may be based on BSIM [11], predictive technology [12] or other foundry models. Note that the effect of dielectric in the gate stack of FEFET is included in the MOSFET/FinFET model. If the gate stack has a metal in between the FE and the dielectric [13], an additional capacitor C_{CON2} may be used (Fig. 2). When the model is invoked in the transient simulations in SPICE, Kirchoff's current and voltage laws

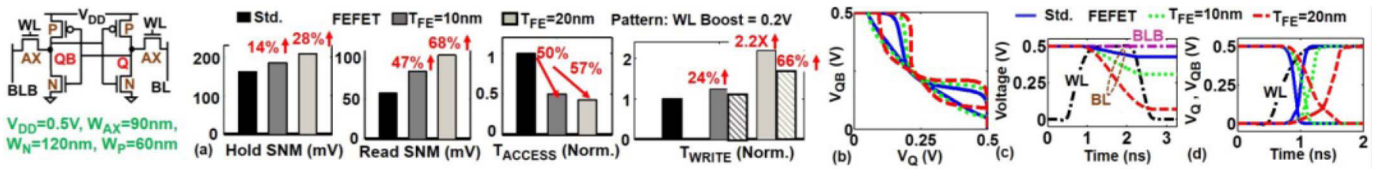

Fig. 6. Comparison of MOSFET (Std.) and FEFET-SRAMs: (a) read/hold static noise margin (SNM), access time (T_{ACCESS}), write time (T_{WRITE}), (b) read butterfly curves and timing waveforms during (c) read and (d) write.

(KCL/KVL) ensure that the capacitor current (CdV/dt), charge ($= \int CdV$) and the voltage division between FE (V_{FE}) and MOSFET (V_{INT}) are consistent. In Fig. 2(b) we show how V_{INT}, V_{C_LK}, V_{R_LK} and V_{FE} evolve as the gate voltage V_G is applied. Voltage step-up ($V_{INT}/V_G > 1$) and negative V_{FE} (due to $C_{FE} < 0$) can be clearly observed.

Note, the position dependence of E along the gate length is neglected in the FE but considered in the channel (via MOSFET models). Under this assumption, FE can be thought to perceive an average E. This is the result of single domain approximation. In addition, the model neglects the static gate current of FEFETs. It is noteworthy that before starting the simulations, the voltages on the capacitors (C_{LK}, C_{MOS} and C_{CON}) may need to be initialized by applying a ramp voltage at the gate terminal as shown in Fig. 2(a). This generates the capacitor current and sets the initial capacitor values consistent with the initial V_G. Once the correct initial values are set, the input voltages are applied to perform the simulations. The model, being based on the capacitors, cannot be used for direct current (DC) analysis in SPICE. The DC response is obtained with quasi-DC simulations based on applying a triangular input pulse of appropriate frequency ($\ll$1/time constants of the device and polarization switching).

III. Calibration and Simulation Details

To calibrate our model, we grew 100nm lead zirconium titanate (PZT) films on hafnium oxide (HfO_2) buffer and silicon substrate using pulsed vapor deposition. Taking into account the capacitance of HfO_2 buffer, we extract the static L-K coefficients from experimental P-E loop (Fig. 2(c)). The value of ρ is calculated by considering the polarization switching time ~200ps [14]. The response of the FE model with varying frequency of the triangular pulse of the applied voltage (Fig. 2(d)) is consistent with previous works [5], [7]. This behavior is attributed to the lag in the response of P to varying E due to the dissipative forces. The contacts are considered to be near-ideal ($\lambda \ll T_M$) and $Q_F = 0$ is assumed. We employ the calibrated FE model in conjunction with the 45nm MOSFETs [12]. Note, the model can also be used for other FE materials and device structures like FinFETs.

IV. Device Simulations

In this section, we present the FEFET characteristics employing the proposed model. FEFETs exhibit lower sub-threshold swing (SS) and higher ON current (I_{ON}) with the same OFF current (I_{OFF}) due to negative C_{FE} (Fig. 3). This is accompanied by an increase in the gate capacitance (C_G). The reason is that negative C_{FE} in series with the underlying MOSFET capacitance (C_{MOS}) increases the overall capacitance ($|C_{FE}|C_{MOS}/(|C_{FE}|\text{-}C_{MOS})$). I_{ON} and C_G increase and SS reduces with increasing FE thickness (T_{FE}). For $T_{FE} >= 30$ nm, hysteretic transfer characteristics are observed (Fig. 3(b)) and C_G shows a non-monotonic behavior, exhibiting a peak when $|C_{FE}| \approx C_{MOS}$.

In addition to T_{FE}, the characteristics of FEFETs can be optimized by selecting suitable FE materials (Fig. 4). Higher E_{C0} and lower P_{C0} leads to a decrease in $|C_{FE}|$ and boost in the voltage step-up action (Fig. 1) increasing I_{ON} and C_G.

V. Circuit Simulations

A. Ring Oscillator (RO) Analysis

Fig. 5 (a-b) shows the energy versus delay of MOSFET- and FEFET-based inverters, obtained using RO simulations. FEFETs exhibit up to 97% lower delay at iso-energy for supply voltage (V_{DD}) < 0.4V due to increase in I_{ON}. At higher V_{DD}, the speed of FEFETs is limited by (a) the FE polarization transients (dependent on $\rho dP/dt$ and R_{LK}-Fig. 2) and (b) increase in C_G. Fig. 5 shows that the benefits of FEFETs at low V_{DD} increase for larger wire capacitance (C_{WIRE}). This is because C_{WIRE} mitigates the effect of increase in C_G of FEFETs. Increasing T_{FE} (while maintaining non-hysteretic operation) reduces the delay for $V_{DD} < 0.4$V. FEFETs exhibit larger dynamic energy due to higher C_G. The short circuit energy for FEFETs is larger, especially at high V_{DD}. This is due to steep switching, which makes it harder to turn OFF the device (as $|V_{GS}|$ reduces) and easier to turn it ON (as $|V_{GS}|$ increases). The leakage energy of FEFETs ($V_{DD} \times I_{OFF} \times$ RO Time Period) is larger at high V_{DD} and smaller at low V_{DD}, similar to the delay.

B. SRAM Analysis

Our analysis on 6T SRAMs (Fig. 6) shows that FEFETs offer higher read stability, lower access time and larger hold stability due to higher I_{ON}/I_{OFF} enabling faster discharge of the bit-line and better voltage retention. However, FEFETs exhibit write time penalty, which may be mitigated by using write assist techniques such as word-line boost [15] (Fig. 6).

VI. Summary

We presented a SPICE model for FEFETs based on the *exact* solution of the time-dependent LK equation coupled with transistor equations. SPICE-based implementation enables self-consistent solution of FE polarization transients during circuit operation and couples the negative capacitance of FE with other capacitances in a circuit. We showed the application of our model to perform device, logic and SRAM analysis.

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