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# Ferroelectric Synaptic Transistor Network for Associative Memory

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**Brain-inspired associative memory is meaningful for pattern recognitions and image/speech processing. Here, a ferroelectric synaptic transistor network is proposed that is capable of associative learning and one-step recalling of a whole set of data from only partial information. The competition between an external field and the internal depolarization field governs the ferroelectric creep of domain walls and offers each single ferroelectric synapse a full and subfemtojoule-energy-cost Hebbian synaptic plasticity, including short-term memory (STM) to long-term memory (LTM) transition, and remarkably both spike-timing-dependent plasticity (STDP) and spike-rate-dependent plasticity (SRDP). Assisted by the third terminal to control the ferroelectric domain dynamics, self-adaptive coupling between neurons is realized by updating synaptic weight concurrently. Pavlov's dog experiment and multiassociative memories are demonstrated in this ferroelectric synaptic transistor network. Such ferroelectric synaptic transistor network is available for building multilayer neural networks and provides new avenues for associative-memory information processing.**

## 1. Introduction

The brain-inspired associative memory involves a conditioning process, capable of recalling memory from its fragments or constituents. Such memory has attracted tremendous attention not only for practical applications in pattern recognitions and image/speech processing, but also because of its significant role in thinking procedure and artificial intelligence. A connection of recurrent neural network, including the auto-associative Hopfield neural network (HNN)[1] and hetero-associative bidirectional associative memories (BAM) neural network,[2] is proven to be effective for implementing the associative memory function.[3] Hardware implementation of HNN or BAM neural network with complementary metal-oxide-semiconductor (CMOS) circuits[4] and energy-efficient memristor[5,6] has been testified. However, the unique synaptic weight matrix referring for the so-called objective pattern needs to be precalculated and programed in the HNN or BAM neural network, and the recalling process which is in a form that neurons gradually switch to prestored states costs several or even dozens of iterations.[5] This unfortunately drags down the speed of information processing. One alternative strategy is the one-step recalling through coupling between features among the pattern, like the coupling of neurons in Pavlov's dog experiment.[7] The hardware implementation of synaptic weight updating for coupling of neurons requests elaborate neural systems[8,9] or strict functionality from artificial synapses,[10] known as Hebbian law[11] including spike-rate-dependent plasticity (SRDP)[12] and spike-timing-dependent

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plasticity (STDP).[13] This one-step recalling neural network is not reported yet mostly due to the disparity of bio-plausible characteristics in state-of-the-art artificial synapses and the lake of matched connection structure with efficient algorithm.

On the material level, the memristor, an electronic device whose resistance depends on the history of the electrical signal it has experienced, stands out as a promising candidate for an electronic equivalent to the synapse for artificial neural networks.[14,15] The mostly reported memristors are based on atomic/ionic transport in filament-forming metal oxides[16] or phase transition in phase change memory materials.[17] Their analog memristive behavior accelerates the development of artificial neural network (ANN) chips,[18] whereas the monotonous dynamics is incompetent for the spiking neural networks (SNNs) in which low-overhead online learning, including associative memory, is enabled by inherent local training rules as in biological nervous systems. Consequently, the present SNN chips are at a very rudimentary level.[18] Zhu et al. demonstrated that the ionic-gating synaptic transistors, capable of mimicking the internal ion dynamic inside a synapse, present rich synaptic functionalities including SRDP, dynamic filtering, etc., with remarkable linearity, symmetry, and ultralow energy consumption.[19] The Pavlov's dog conditioning experiment is realized using an ionic liquid synergistic gating transistor,[20] retaining difficulty to expand them in a neural network for complex functions. Besides, electronic memristors based on ferroelectric materials are recently proposed to successfully emulate synaptic behaviors in more precise, efficient and homogenous manners.[21–23] The ferroelectric synaptic weight for a neural network could be corroborated by a multilevel memory effect in forms including ferroelectric capacitors,[24] ferroelectric transistors,[25–27] and ferroelectric tunnel junctions (FTJs).[22,28] Specially, combination of ferroelectrics and 2D semiconductors attracts much attention due to its robust performance and scalability.[29] The competition between external electric field stimuli and real-time evolving internal depolarizing field on the ferroelectric double-well potential results in abundant domain dynamics, providing the exciting possibility of more bio-plausible characteristics to ferroelectric synapses, whereas not confirmed yet.

Here we fabricate ferroelectric synaptic transistors to mimic biological synapse, as sketched in **Figure 1**a, in which 2D $MoS_2$ and ferroelectric poly(vinylidene fluoride) copolymer P(VDF-TrFE) (70:30 mol%) films afford the channel and gate dielectric, respectively. Despite that P(VDF-TrFE) possess ferroelectricity even at thin films of 2 nm thickness, to alleviate the influence of following electrode deposition process on ferroelectricity of thin organic polymer films, two spin-coating layers (≈100 nm) thick P(VDF-TrFE) films are used in this work. The ferroelectric creep motion of domain walls being sensitive to competition of external and internal depolarization fields provides the single three-terminal ferroelectric synapse the ability for whole Hebbian synaptic plasticity, including short-term memory (STM) to long-term memory (LTM) transition, SRDP and

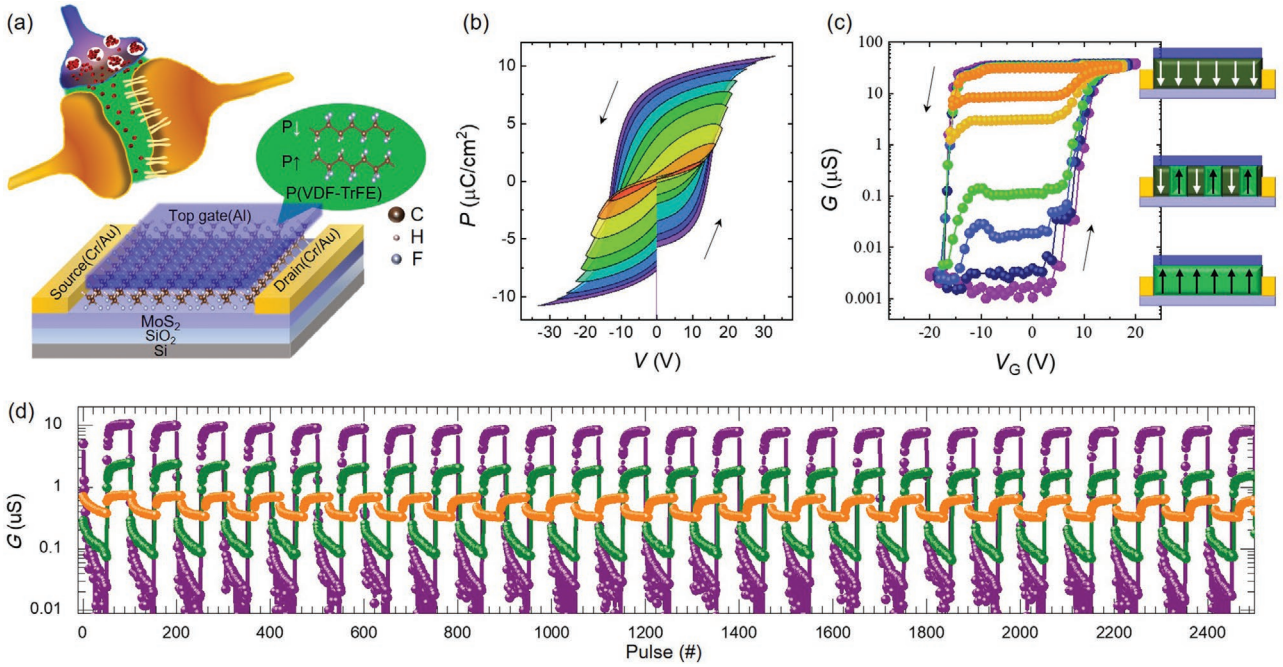


**Figure 1.** Device structure and electrical characteristics of a ferroelectric synaptic transistor. a) The diagram of the designed device. The channel conductance tuned by ferroelectric polarization of P(VDF-TrFE) layer emulates the biological synaptic weight. Inset shows a multiterminal biological synapse for comparison. b) Polarization versus voltage (*P*–*V*) hysteresis loops of a ferroelectric P(VDF-TrFE) capacitor under various voltage amplitudes. The frequency of applied triangular voltage is 1000 Hz. c) Channel conductance hysteresis loops of a ferroelectric synaptic transistor under voltage sweepings with amplitudes of ±20, ±18.5, ±18, ±17.5, −16 to 17.5, and −15.5 to 16.5 V, respectively. The cross sections of transistors in the right panel represent downward polarization (high channel conductance), mixed polarization (intermediate channel conductance), and upward polarization (low channel conductance) states, respectively. d) Evolution of channel conductance as a function of the different voltage pulse sequences. Alternated +6 and −10 V pulse trans for orange color, +7, −11 V for dark green color and +8, −12 V for purple color, both the pulse width and internal time span are 20 ms. The conductance noise below 0.05 μS is limited by our measurement instrument.

STDP. The energy consumption for every synaptic operation is less than 1 fJ. Using three-terminal ferroelectric synapses, we propose an associative spiking neural network (aSNN) that is capable of associative learning and one-step recalling of all the data from partial information. The third terminal is used to control the ferroelectric domain dynamics and self-adaptive coupling between neurons is therefore realized by updating concurrently synaptic weight. Pavlov's dog conditioning experiment and multiassociative memories are demonstrated in this ferroelectric synaptic transistor network. Building multilayer neural networks using the as-proposed aSNN provides the possibility for associative memory without changing the original learning tasks of the neural networks. This work affords a springboard for the development of neuromorphic hardware systems using ferroelectric synaptic transistors.

## 2. Ferroelectric Synaptic Transistor as Three-Terminal Synapses

In a ferroelectric synaptic transistor, the ferroelectric domain configurations in the gate dielectric tune the carrier concentration of semiconductor channel layer, and hence program multiple channel conduction states, making them ideal for artificial synapses.[23] Figure 1a shows a biological synapse and side-view schematic of an organic ferroelectric synaptic transistor, respectively. The $MoS_2$ channel (5 μm long and 5 μm wide) serves as the synapse transmitting information via connecting to presynaptic neuron and postsynaptic neuron. The synaptic weight represented by various channel conductance is modulated via the gate voltage. To confirm the ferroelectric characteristics of the P(VDF-TrFE) thin film in our study, Figure 1b displays typical polarization–voltage ($P$–$V$) hysteresis loops of Al/P(VDF-TrFE) (≈100 nm thick, in accord with the gate layer in $MoS_2$ ferroelectric synaptic transistor)/Al capacitor with various amplitudes. A remnant polarization ($P_r$) of about 8 μC cm$^{-2}$ and a coercive voltage of ±12 V can be extracted from the saturated polarization loop with a ±34 V sweep. The discontinuous polarization on $V_g$ = 0 V is due to the depolarization process, as discontinuous triangular voltage waves are used to measure these polarization hysteresis loops. When the maximum voltage of the hysteresis sweep decreases, shrinking loops and multilevel polarization are observed in terms of the polarization amplitude level determined by the peak voltage of the hysteresis loops.

Along with the bipolar switching behavior of P(VDF-TrFE) polarization, the $MoS_2$ channel conductance in the organic ferroelectric synaptic transistor, was measured as a function of the amplitude of the bipolar write voltage pulses ($V_{write}$, ≈5 ms) applied to the gate electrode. As shown in Figure 1c, the channel conductance was switched between low (OFF) and high (ON) conductance in a hysteresis and multilevel manner as the $P_r$ in $P$–$V$ loops (Figure 1b). The quantitative agreement between the coercive field of P(VDF-TrFE) and the threshold field of conductance modulation indicates that the observed resistance evolution is ascribed to ferroelectric polarization reversal. The upward or downward polarization state of P(VDF-TrFE) would cause the depletion or accumulation of electrons in $MoS_2$ channel, resulting in two distinctive channel conductance values. The violet curve in Figure 1c gives the largest ON/OFF ratio of $10^4$ with a write pulse window of ± 20 V, which is larger than the coercive voltage of P(VDF-TrFE), corresponding to totally downward and upward states of ferroelectric polarization. Importantly, a broad range of intermediate channel conductance states can be stabilized during the bipolar switching process through explicitly controlling the peak voltage of the hysteresis sweep and correspondingly changing the relative fraction of ferroelectric polarization configuration. Despite some depolarization occurs during the voltage back sweeping process, these conductance hysteresis loops unequivocally demonstrate the existence of stabilized intermediate conductance states. This persistent and multilevel tuning of $MoS_2$ channel conductance by nonvolatile ferroelectric polarization in P(VDF-TrFE) gate layer provides a feasible access to emulate the plastic changes of synaptic weights. Figure 1d shows that the channel conductance increases gradually under voltage pulse sequences with various amplitudes (+6, +7, +8 V) and decreases gradually under voltage pulse sequences with different amplitudes (−10, −11, −12 V), implying a long-term potentiation (LTP) and long-term depression (LTD) process as in biological synapses. The modulation of channel conductance by polarization reversal in the ferroelectric gate layer allows the ferroelectric synaptic transistor for various biomimetic applications. For example, lee et al. reported an artificial tactile sensory organ utilizing synaptic transistor with gate dielectric of ferroelectric nanocomposite of BTO and P(VDF-TrFE) covered by a triboelectric layer.[30]

## 3. Creeping of Ferroelectric Domain Walls and STM to LTM Transition in Ferroelectric Synaptic Transistors

The switching of ferroelectrics in defect-free single-crystal is expected to be intrinsic and in a homogeneous way.[31] However experimentally, switching of ferroelectrics occurs in an extrinsic manner including domain nucleation and anisotropic propagation of domain walls, due to the presence of defects lowering the barrier for polarization reversal. The propagation of domain walls can be described by a creep process,[32,33] recently illuminated by first-principles-based molecular dynamics simulations.[34] Upon applying electric field, the time evolution of ferroelectric polarization $\Delta P(t)$ can be described by Kolmogorov–Avrami–Ishibashi (KAI) model,[35] which is given by the compressed exponential function

$$\frac{\Delta P(t)}{2P_r} = 1 - \exp\left[-\left(\frac{t}{t_0}\right)^n\right] \quad (1)$$

where $t_0$ is the characteristic switching time proportional to the reciprocal creep velocity of domain walls, $P_r$ is the remnant polarization of the film, and the Avrami index $n$ depends on the dimensionality of the domains.

In the case of ferroelectric polymer films, after thermal annealing process, P(VDF-TrFE) films are a mixture of crystalline and amorphous regions with a crystallinity of 50%.[36] As shown in **Figure 2**a, crystalline lamellas are surrounded by amorphous regions. In the crystalline lamellas, the copolymer

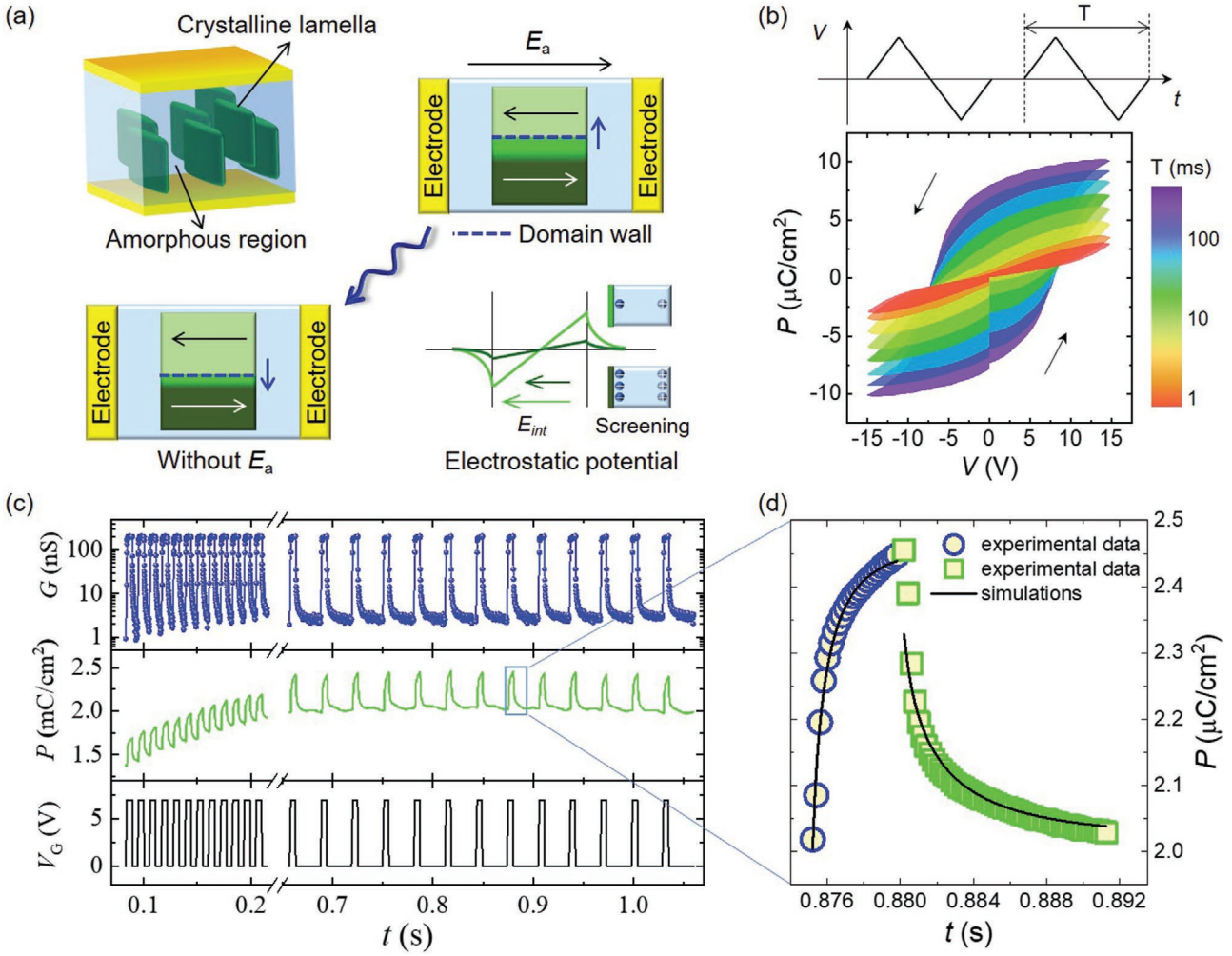


**Figure 2.** The creeping of ferroelectric domain walls and STM to LTM transition in a ferroelectric synaptic transistor. a) Schematic of the creeping process of ferroelectric domain walls. P(VDF-TrFE) films are a mixture of crystalline and amorphous regions with a crystallinity of 50% in which crystalline lamellas are surrounded by amorphous regions (top left panel). The domain wall is forced to creep up to realize rightward polarization under rightward electric field $E_a$ ($E_a > E_c$) (top right panel). The electrostatic potential at fresh switched region (highlighted by green) is rather steep resulting in huge internal field ($E_{int}$), while the electrostatic potential at relative old switched region (highlighted by dark green) is softened by sufficient screening from relaxational dipoles or space charges in amorphous regions (bottom right panel). The initial huge $E_{int}$ (larger than $E_c$, highlighted by green) will trigger depolarization process and compel the domain wall creep down (bottom left panel). b) *P*–*V* hysteresis loops of the Al/P(VDF-TrFE)/Al ferroelectric capacitor under a series of periodic triangular waveforms with *T* of 1, 2, 5, 10, 20, 50, 100, and 200 ms, respectively. The top panel shows the periodic triangular waveforms with alterable *T* and internal time span "Δ*t*" between triangular waveforms. c) Evolution of channel conductance and gate polarization as a function of positive voltage pulse sequences inputted from gate. d) Simulations for switching and depolarizing process of ferroelectric domains.

is in all-trans (TTTT) conformation to form the $\beta$ polar phase with nonpolar boundary formed by trans-gauche-trans-gauche' (TGTG') conformation. Ferroelectric behavior primarily stems from the crystalline lamellas but is influenced by the amorphous regions. For example, the serial amorphous regions result in incomplete compensation for interfacial charges of ferroelectric lamella, inducing huge depolarization field ($E_{dep}$) opposite to polarization direction in the ferroelectric domains. The value of $E_{dep}$ is described by classical electrostatic model[37]

$$E_{dep} = -\frac{P_r}{\varepsilon_0\varepsilon_f + \varepsilon_0\varepsilon_s\left(\frac{d_f}{d_s}\right)} \quad (2)$$

where $\varepsilon_0$, $\varepsilon_f$, $d_s$, and $d_f$ are the vacuum permittivity, static dielectric constant of the material, thickness of serial amorphous regions, and thickness of ferroelectric lamella along normal direction of electrode, respectively. Given a similar permittivity for ferroelectric region and amorphous region, even one-tenth thick serial amorphous region can induce $E_{dep}$ magnitude of 100 MV m$^{-1}$, higher than the experimental coercive field ($E_c$) of 50–100 MV m$^{-1}$.[38] This $E_{dep}$ makes the ferroelectric domains unstable and easily switchable by reverse voltage. On the other hand, the relaxational dipoles or space charges in amorphous regions also play a role to screen interfacial charges by polarization, giving rise to strong imprint effect.[39] The imprint field ($E_{imp}$) alleviates $E_{dep}$, making difficult the switching of

ferroelectric domains. The vector sum of $E_{dep}$ and imprint field ($E_{imp}$), yields an internal electric field ($E_{int}$) inside ferroelectric domains. The $E_{imp}$ is along polarization direction (opposite to $E_{dep}$) with a magnitude being smaller than $E_{dep}$, thus $E_{int}$ is opposite to polarization direction with an amplitude of $E_{int} = E_{dep} - E_{imp}$. The value of $E_{int}$ can be obtained by differentiating electrostatic potential as shown in Figure 2a.

The existence of $E_{int}$ permits extra domain switching dynamics. For these fresh (just at the end of the switching process) domains, if $E_{int}$ is larger than $E_c$, the domain is not thermodynamically stable and depolarization process occurs.[37] Note that the value of $E_{imp}$, which depends on the screening degree by the amorphous region, always increases with time after the formation of ferroelectric domains. Thus, the ferroelectric domain dynamics can be tuned, through the evolution of $E_{int}$ magnitude ($E_{dep} - E_{imp}$) and the formation history of domains by applied voltage bias. As shown in Figure 2a, let us assume two domains in one crystalline lamella to align leftward and rightward as indicated by light green and dark green area, respectively, with the inset arrows pointing the polarization direction. If we consider the case when the polarization state has been transiently set with a rightward electric field $E_a$ ($E_a > E_c$), the domain wall is compelled to creep up to realize rightward polarization. For the dark green rightward domain, which experiences $E_a$ in the same direction to polarization for a long time, the screening from relaxational dipoles or space charges in amorphous regions (labeled as vast charges in inset of electrostatic potential) is much strong, and the electrostatic potential (highlighted by dark green) is reduced by $E_{imp}$. Then the dark green rightward domain is stable since the much-reduced $E_{int}$ (highlighted by dark green) is smaller than $E_c$.

However, for the region of fresh rightward domain (highlighted by green), the screening from amorphous regions (labeled as few charges in inset of electrostatic potential) is deficient and the electrostatic potential (highlighted by green) is slightly affected by the negligible $E_{imp}$. The initial huge $E_{int}$ (larger than $E_c$ as discussed above, highlighted by green) will trigger depolarization process and force the domain wall to creep down.

During the depolarization process, $E_{int}$ is not a constant since both polarization[37] and $E_{imp}$[39] are time-dependent. The depolarization dynamics is expected to be more complicated than that in polarization switching under uniform electric field. Experimentally, the characteristics of depolarization could be analyzed from a stretched exponential function[40]

$$P(t) = P(0)\exp\left[-\left(\frac{t}{\tau_{bs}}\right)^{n}\right] \quad (3)$$

where $P$ (0) represents the value of the initial polarization before depolarizing, $\tau_{bs}$ is the characteristic time of back switching (depolarizing), and $n$ is the stretched exponent.

Qualitatively, the phenomenological analysis above is experimentally corroborated by polarization versus voltage ($P$–$V$) hysteresis loops with fixed amplitude and alterable excitation period (frequency). As shown in Figure 2b, when the period of applied triangular voltage is as short as 1 ms, a spot of polarization switches for the application of the triangular voltage and depolarizes almost completely as the voltage fades away, forming the anticlockwise $P$–$V$ hysteresis loops with non-cross "8" shape (highlighted by red color). This corresponds to the situation of fresh domains where $E_{int} > E_c$. As the period increases with a constant amplitude of 15 V, more and more domains are thermodynamically stable, retaining multiple permanent polarization in the $P$-$V$ hysteresis loops. This corresponds to the situation of domains that have experienced the same direction between polarization and $E_a$ for a long time where $E_{int} < E_c$. Through tuning the period of voltages, multilevel polarization states of ferroelectrics are thereby achieved. This original finding inspires the realization of spike rate-based synaptic functions using ferroelectric synapses.

As shown in Figure 2c, a sequence of positive voltage pulses, with constant amplitude ($V$ = 7 V), fixed width ($W$ = 5 ms) and variable time interval ($t_i$), is applied to the gate electrode of P(VDF-TrFE) ferroelectric synaptic transistor. Real-time evolution of both channel conductance and gate polarization (up to down) are monitored simultaneously by dealing with transient currents through channel and ferroelectric gate layer, respectively. The polarization switches and depolarizes as the voltage pulse sets on and off, respectively. As can be seen from 0.65 to 1.05 s in Figure 2c, the fresh-switched polarization depolarizes completely after each voltage pulses, similar with the response of polarization for triangular voltage with period of 1 ms and amplitude of 15 V (red color loop in Figure 2b) due to the $E_{int} > E_c$. Note that the polarization switching under voltage pulses with $t_i$ = 25 ms is slightly affected by previous ones (from 0.65 to 1.05 s in Figure 2c). But for $t_i$ = 5 ms, clear additive effect is observed. The polarization increases circuitously since the following stimulating voltage pulse compels new polarization switching before it depolarizes to previous state (from 0.1 to 0.2 s in Figure 2c). After accumulating the duration time for experiencing $E_a$ with the same direction to polarization through multiple voltage pulses, these switched domains by multiple voltage pulses could be stabilized due to the much-reduced $E_{int}$ which is smaller than $E_c$, as described by dark green rightward domains in Figure 2a. These multiple voltages, with $t_i$ = 5 ms, result in permanent polarization as shown by the variation of polarization value from 1.5 μC cm$^{-2}$ ($t$ = 0.1 s) to 2 μC cm$^{-2}$ ($t$ = 0.7 s) in Figure 2c.

Concomitantly to the evolution of polarization, the channel conductance increases gradually as the switched polarization propagates in a zigzag way from up to down for $t_i$ = 5 ms and oscillates around a constant value for $t_i$ = 25 ms (Figure 2c). The channel conductance relaxation due to depolarizing of the ferroelectric P(VDF-TrFE) gate layer actually corresponds to an STM behavior, while the pinned channel conductance by remnant polarization behaves like a long-term memory (LTM). The STM to LTM transition in these ferroelectric synaptic transistors is realized by tuning $t_i$ (Figure 2c). The STM realized in ferroelectric synaptic transistors endows the ferroelectric synapses with the new opportunity of reservoir computing in which complex and temporal data, such as handwritten digit recognition,[41] isolated spoken-digit recognition and chaotic system forecasting,[42] are efficiently computed with low-training cost by compressing features from high-dimensional feature space into temporal inputs.

As previously discussed, the polarization fluctuation could be described by a to-and-fro creeping of domain walls. The polarization switching and depolarizing process are well described

with equations (1) and (3) (Figure 2d), respectively. The fitting gives $n = 0.53$ for domain switching which is used for domain depolarizing to ensure the same domain wall information for the switching and depolarizing processes. The obtained characteristic switching times are $t_0 = 0.42$ ms and $t_{bs} = 1.24$ ms, meaning that the creep velocity of domain walls is about three times slower in depolarizing process than that in switching process. These domain dynamics allow a precise tuning of polarization for spike-based synaptic functions.

## 4. Hebbian Synaptic Plasticity in Ferroelectric Synaptic Transistors: Both SRDP and STDP

In the learning process of neural networks, the synaptic weight can be short-term/long-term potentiated (synaptic weight strengthening) or depressed (synaptic weight weakening) according to neuron activity and/or local dynamics, which is referred as Hebbian synaptic plasticity.[11] SRDP and STDP are the two classical Hebbian learning rules as already experimentally verified in the mammalian hippocampus and visual cortex.[12,13] SRDP involves the effect of the spike frequency on the synaptic weight modification while STDP stipulates the effect of the precise timing between electrical spike signals from neighboring neurons. SRDP of Bienenstock–Cooper–Munro (BCM) type, responding to instantaneous firing rates rather than individual spikes, reconstructs the synaptic weight over time, which is crucial for processing of visual information, learning and memory storage.[43] Experimental evidences showing that both SRDP and STDP coexist at the same biological synapses have been obtained.[12,13,44] However, whereas several works already reported the STDP behavior,[22,25,45]

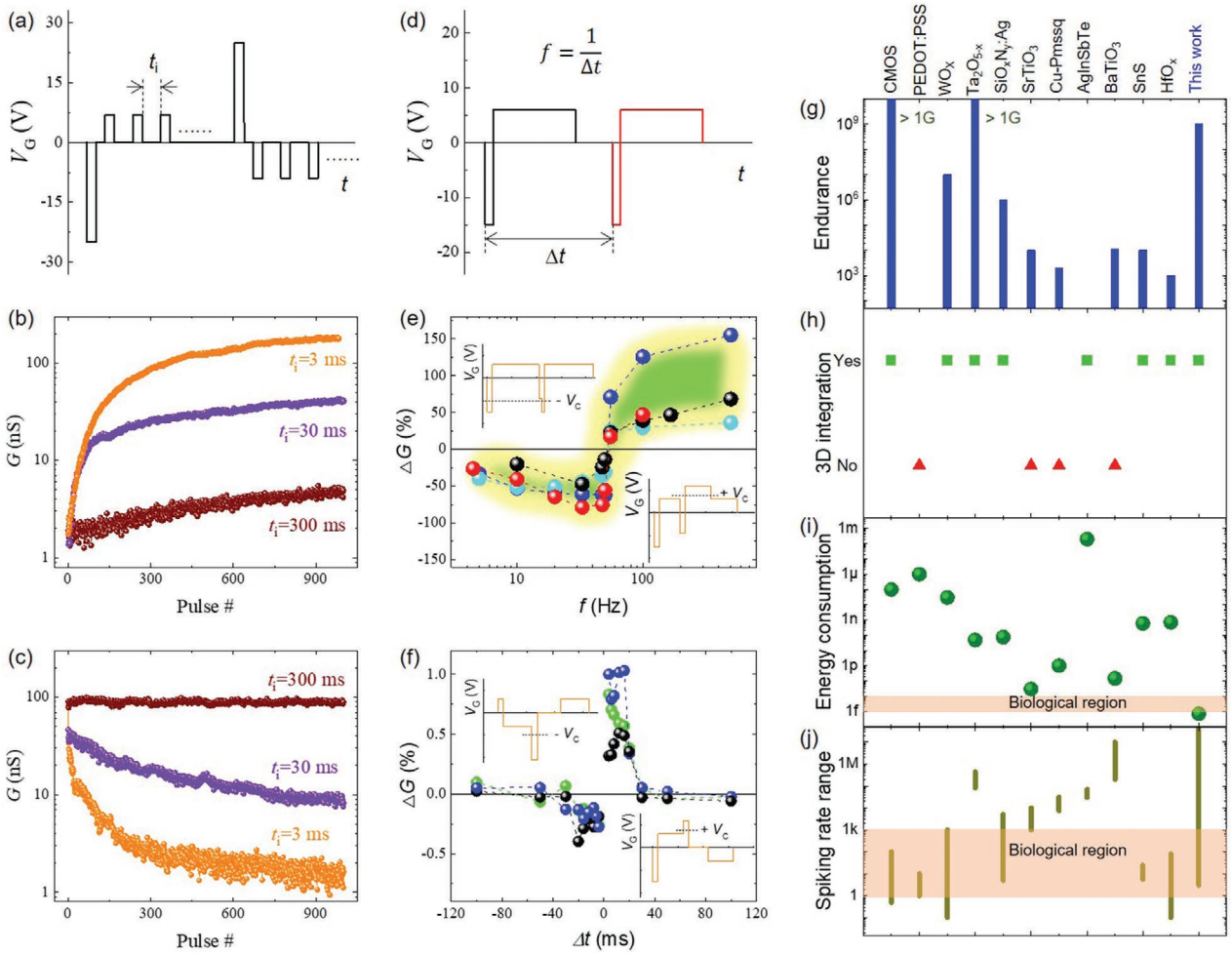


**Figure 3.** Hebbian synaptic plasticity in ferroelectric synaptic transistor: both SRDP and STDP. a) The voltage pulse sequence applied to the gate. Here the pulse with high amplitude is used to preset the channel to low or high conductance state. The internal time ($t_i$) between two sequent pulses can be altered. The channel conductance as a function of b) positive or c) negative voltage pulse sequences shown in (a). d) Two consecutive pulses with variable delay ($\Delta t$) applied to the gate. e) Measurements of SRDP of BCM type in which the synaptic weight presents a first LTD and then LTP depending on the instantaneous spiking rates. Inset shows two examples of voltage waveforms with different frequency. f) Measurements of STDP by applying spike pairings, a presynaptic one followed by a postsynaptic one with a delay of $\Delta t$. Pre–post pairing ($\Delta t > 0$) induces LTP and post–pre pairing ($\Delta t < 0$) induces LTD. The inset shows combined waveforms ($V_{pre} - V_{post}$) for timing difference of $\Delta t = \pm 12$ ms, respectively. Comparison in performance of g) endurance, h) compatibility for 3D integration, i) energy consumption of every synaptic operation, and j) spiking rate range between our device with reported spike rate-based artificial synapses.

experimental demonstrations of SRDP in ferroelectric synapses are still lacking while crucial for the development of bio-inspired synapses.

To test and verify the effect of the spiking rate on our ferroelectric synapses, voltage pulses with three kinds of $t_i$ ($t_i$ = 3, 30, and 300 ms) are inputted on the gate ($V$ = 7 V, $W$ = 5 ms in **Figure 3**b and $V$ = –12 V, $W$ = 5 ms in Figure 3c). As the voltage waveform shows in Figure 3a, before applying pulses with variable $t_i$, these ferroelectric synapses are first manipulated to low or high conductance state. From Figure 3b,c, we can clearly see that the change of channel conductance is dramatically weakened as the spike rate decreases ($t_i$ increases). Similar with STM to LTM transition, the observed feature in our ferroelectric synapses can be understood by the polarization dynamics, i.e., the longer $t_i$ allows sufficient polarization depolarizing, resulting in less switched polarization and smaller change of channel conductance.

To further develop SRDP of the BCM-type where a high-frequency (low-frequency) train of presynaptic pulses results in potentiation (depression) of the synaptic strength,[43] we designed a pulse waveform including a negative voltage pulse ($V$ = –15 V, $W$ = 2 ms) that is greater than the negative coercive voltage of ferroelectrics P(VDF-TrFE), followed by a positive voltage pulse ($V$ = +6 V, $W$ = 20 ms) that does not reach the positive coercive voltage but not less than half of it. In order to verify the frequency-dependence of the synaptic weight, we applied two consecutive pulse waveforms mentioned above to the gate of ferroelectric synapse with a set of periods ($\Delta t$) (Figure 3d). As shown in Figure 3e, for low frequency (e.g., $f = 1/\Delta t$ = 5 Hz), the two waveforms have no overlap and only the negative voltage exceeds the coercive voltage, the conductance of ferroelectric synapse decreases ($\Delta G < 0$, synapse weakening) and the absolute value of synaptic weight variation shows incremental trend as the frequency increases, in line with Figure 3c. When the two applied waveforms begin to overlap (i.e., $f = 1/\Delta t$ = 45.5 Hz), the synaptic weight turns to weaken because the amplitude of negative voltage in the second waveform is slightly compensated by the positive part of the first one, with overlapped part below the coercive field and the remaining one still above the coercive field. An example (i.e., $f = 1/\Delta t$ = 47.6 Hz) is displayed in upper inset of Figure 3e. With further increasing the frequency, the negative voltage in the second waveform will be totally below the coercive field, while the positive voltage in the second waveform starts to overlap with the positive part of the first one and exceeds the coercive field. In-between (around 50 Hz), the negative and positive voltage have an equivalent influence in the manipulation of conductance, thus the synaptic weight remains unchanged. Keeping increasing the frequency, the positive voltage plays a dominant role and the conductance of ferroelectric synapse increases ($\Delta G > 0$, synapse strengthening), an example (i.e., $f = 1/\Delta t$ = 100 Hz) of which is shown in the lower inset of Figure 3e. The entire process of SRDP measurement on our ferroelectric synaptic transistor under different frequency is summarized in Figure 3e. It nicely follows a typical BCM learning rule in which the synaptic weight presents a first LTD and then LTP depending on the instantaneous spiking rates. This observation in ferroelectric synaptic transistors is consistent with the experimental report on biological visual cortex.[12]

The timing effect of spikes on synaptic weight (STDP) in ferroelectric synaptic transistors is then represented by applying spike pairings, a presynaptic one followed by a postsynaptic one with the same waveform shape as in SRDP measurements, to the gate electrode. A smaller amplitude of 6 V instead of 15 V in front part of postsynaptic spike signal is used to achieve the asymmetry of conductance switching in ferroelectric synaptic transistors (Figure 1d). The inset of Figure 3f shows combined waveforms ($V_{pre} - V_{post}$) for timing difference of $\Delta t = \pm 12$ ms, respectively. As demonstrated in Figure 3f, the amplitude mechanism[25] results in the STDP learning rule, where pre–post pairing ($\Delta t > 0$) induces LTP and post-pre pairing ($\Delta t < 0$) induces LTD.

For synapses in the cerebral cortex of the mammalian brain, it is now widely accepted that both SRDP and STDP learning rules are controlled by so-called NMDA receptor (NMDAR)-mediated intracellular calcium dynamics.[46,47] Here in our ferroelectric synaptic transistors, we argue that the intracellular calcium dynamics in bio-synapses can be successfully simulated by ferroelectric domain dynamics in artificial ferroelectric-synapses, where tuning the ferroelectric domain wall motion reconciles both SRDP and STDP rules. Note that implementation of Hebbian synaptic plasticity capable of both SRDP and STDP learning rules has been attempted using analog very-large-scale-integrated (aVLSI) circuits.[46] Compared with the aVLSI implementation of Hebbian synaptic plasticity, our single ferroelectric synaptic transistor interestingly takes advantage of not only simplicity, low power and high density, but also higher imitativeness to biological brain.

Performance of endurance (Figure 3g), compatibility for 3D integration (Figure 3h), energy consumption of every synaptic operation (Figure 3i) and spiking rate range (Figure 3j) of our device are compared with reported spike rate-based artificial synapses that utilizing elements including CMOS circuits,[46] PEDOT,[48] $WO_x$,[49] $Ta_2O_{5-x}$,[50] $SiO_xN_y$:Ag,[15] STO,[51] Cu-Pmssq,[52] AgInSbTe,[53] $BaTiO_3$,[54] SnS[55] and $HfO_x$.[56] Strikingly, our ferroelectric synaptic transistor is the only one that satisfies simultaneously all conditions including low-energy consumption (less than 1 fJ, see note S1, Supporting Information), high fatigue durability (prior to 1 G),[25] compatibility for 3D integration and responsivity to spikes in brain-like rate range. In the ferroelectric synaptic transistor, the energy consumed by every synaptic operation is a breakthrough since it is even lower than the consumption in biological system of 1–10 fJ. The speed of polarization reversal in P(VDF-TrFE) films can be as fast as less than 1 μs.[33] Recently, Sayani et al. demonstrated that synaptic operation relied on polarization reversal in P(VDF-TrFE) films can be realized by 20-ns voltage pulses.[57] Thus, ferroelectric synaptic transistors respond to spikes in a rate range of 3 Hz to 50 MHz, covering the dynamics in biological systems. These brain-like characteristics and large-scale integration properties make ferroelectric synaptic transistors very competitive and attractive for exploring and realizing brain-inspired functions.

## 5. Ferroelectric Synaptic Transistor Network for Associative Learning

Associative learning (or conditioning) is a process of forming a connection between environment and organism's own

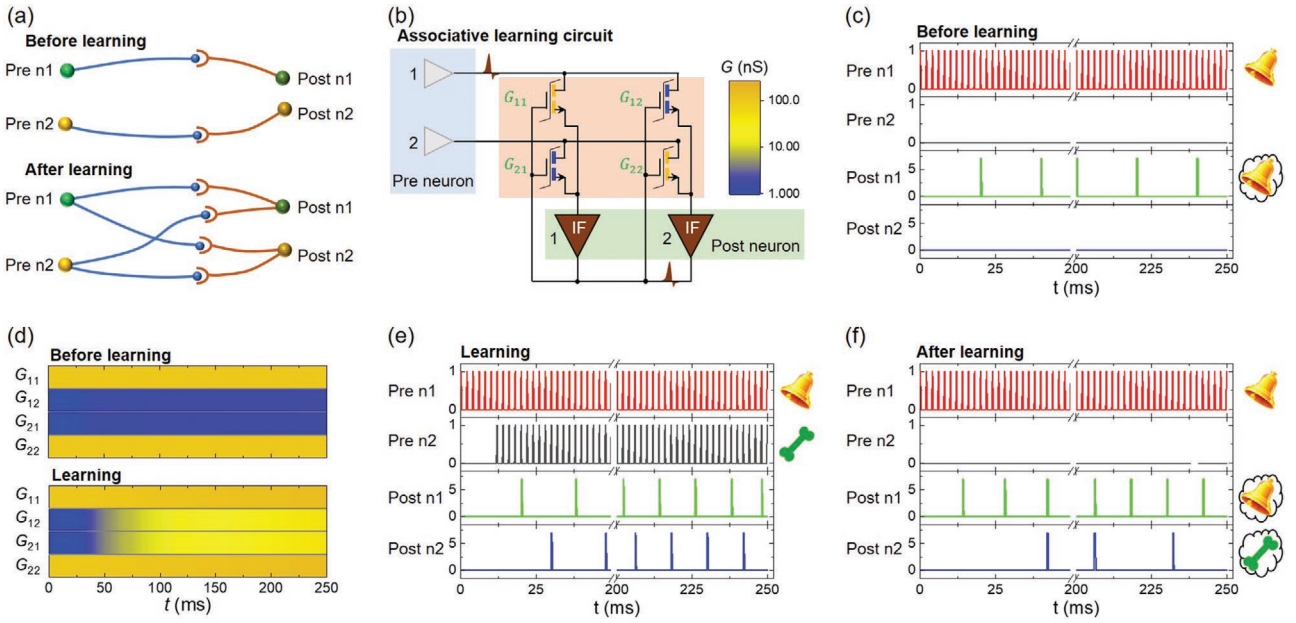


**Figure 4.** Associative learning realized by ferroelectric synaptic transistor network. a) A proposed associative learning rule by creating new connection between neurons. b). The designed associative learning circuit consisting of four ferroelectric synaptic transistors ($T_{11}$, $T_{12}$, $T_{21}$, and $T_{22}$) and four integrate-and-fire (IF) neurons (pre $n_1$, pre $n_2$, post $n_1$, and post $n_2$). Initially, the conductance of transistors is $G_{11}$ = 100 nS, $G_{12}$ = 1 nS, $G_{21}$ = 1 nS, and $G_{22}$ = 100 nS, respectively. c) The input pulse sequences in the input port 1, 2 (top panel) and the firing of post $n_1$, post $n_2$ (bottom panel) before learning. d) The evolution of $G_{11}$, $G_{21}$, $G_{12}$, and $G_{22}$ before (top panel) and during (bottom panel) learning process. The input pulse sequences in the input port 1, 2 (top panel) and the firing of post $n_1$, post $n_2$ (bottom panel) e) during and f) after learning.

reactions. As a concrete manifestation, the experience of two events together will lead to association between their internal characteristics, consequently, when one thing enters consciousness the other would be recalled. In our ferroelectric synaptic transistors, the three-terminal structure has the advantage of direct feedback modulation to synaptic weight from the gate electrode, enabling concurrent learning. We designed an aSNN using the ferroelectric synaptic transistors and integrate-and-fire (IF) neurons, in which the associative learning is accomplished by creating new connection between neurons (**Figure 4**a). Pavlov's dog experiment as an example of associative learning is demonstrated bellow.[9]

Figure 4b illustrates the circuit of the designed aSNN, consisting of four ferroelectric synaptic transistors ($T_{11}$, $T_{12}$, $T_{21}$, and $T_{22}$) as described above and four IF neurons (pre $n_1$, pre $n_2$, post $n_1$, and post $n_2$) in which pre $n_1$ and pre $n_2$ receive "bell" and "bone" stimulus, respectively, while post $n_1$ and post $n_2$ represent "pricking up ears" and the "reaction of secreting saliva," respectively. The transistors in a column are organized by connecting the source and gate, while the transistors in a row are arranged by connecting the drain. The drain terminal of up row and down row are used as the input port of bell signal and bone signal, respectively, modeling the presynaptic neurons. Meanwhile the inputs of post $n_1$ and post $n_2$ are connected with the source of left column and right column, respectively, and the output of post $n_1$ and post $n_2$ are connected to the gate of left column and right column. It is assumed that the post-synaptic neurons will fire when the membrane potential has been integrated beyond the threshold value (i.e., ten successive pulses applied to it). Correspondingly, the output signal was transmitted to the gate, thereby programming the synapse. For initial state, the conductance of $T_{11}$, $T_{12}$, $T_{21}$, and $T_{22}$ are set to $G_{11}$ = 100 nS, $G_{12}$ = 1 nS, $G_{21}$ = 1 nS, and $G_{22}$ = 100 nS, respectively.

First, only bell signal (periodic pulse train of 500 Hz) was fed to input port 1, as displayed in the top panel of Figure 4c. Because of the initial conductance distribution, the individual bell signal can hardly arrive post $n_2$ on account of low conductance state of $T_{12}$ so that the post $n_2$ is not able to fire, but easily arrives neuron $n_1$ due to the high conductance state of $T_{11}$. With a certain number of pulses (ten pulses) transmitted to the post $n_1$, it integrates the bell signal and fires at a certain frequency (≈50 Hz), just as shown in the third panel of Figure 4c. That is to say, if the dog just hears the bell, it will only prick up its ears but not stimulate secretion of saliva. The evolution of $G_{11}$, $G_{12}$, $G_{21}$, and $G_{22}$ during the process is reflected in Figure 4d. For only one firing neuron, the frequency of pulses applied to the synaptic gate is too low to cause an obvious change in the conductance of transistors (Figure 3b). Similarly, the individual bone signal would merely fire post $n_2$ without any synaptic weight update either.

Then we train the aSNN through applying both "bone" and "bell" stimuli with a short time interval ($\delta_t$ = 12 ms) for a sufficient time. Under this circumstance, the firing of "salivation" post $n_2$ would be induced by stimulus from the $T_{22}$ synapse, while that of "pricking" post $n_1$ would be triggered by the $T_{11}$ synapse. Figure 4e shows the input pulse sequences in the input pre n1 and pre n2 (top panel) and the firing of post $n_1$ and post $n_2$ (bottom panel). With the addition of the output of both fired post neurons, the frequency of pulses applied to the gate is sufficiently high (≈100–250 Hz) to potentiate the $T_{12}$ and $T_{21}$ synapses, as revealed in Figure 4d and thus creates the association

between the "pricking" and the "salivation." Finally, the association was verified using only the "bell" stimulus, which successfully triggers the "salivation" post $n_2$ (see in Figure 4f). Noted that the difference between the frequency of post $n_1$ and post $n_2$ is owing to the difference between the conductance of transistor $T_{11}$ and $T_{12}$ ($G_{11} = 150$ nS, $G_{12} = 50$ nS). Utilizing the as-designed aSNN and SRDP property of the three-terminal ferroelectric synaptic transistors, associative learning is therefore successfully implemented by creating new connections between neurons. The association degree between post $n_1$ and post $n_2$ depends on the conductance enhance of $G_{12}$ and $G_{21}$. Correspondingly, the association will decay or even disappear if the conductance of $G_{12}$ and $G_{21}$ decreases. The power of conductance decrease in our ferroelectric synaptic transistor is the polarization relaxations, which is a slow depolarization process. This is similar with the building of association and natural forgetting in biological system. On the other hand, once the long-term memory is formed due to the vast polarization reversal and their long retention time. The association between neurons is hardly disappeared by itself. Erasing the association process is also usual necessary, which asks uninterrupted depolarization process. The domain dynamics in ferroelectrics is sensitive to the amplitude of applied voltage and is extremely slow under a small voltage.[33] The experiment-measured polarization switching time increases for more than seven orders of magnitude as the decrease of applied voltage amplitude.[58] Thus, a constant small voltage bias with opposite polar on all gate, at cost extra energy consumption, is an effective modulation for accelerating the depolarization process and the association erasing process.

As a basic function of the biological brain, associative memory is not only significant for Pavlovian conditioning (Figure 4) but as well for recalling memory from partial information. Following is a case of multiassociate memories realized using this aSNN. **Figure 5**a shows aSNN which is trained

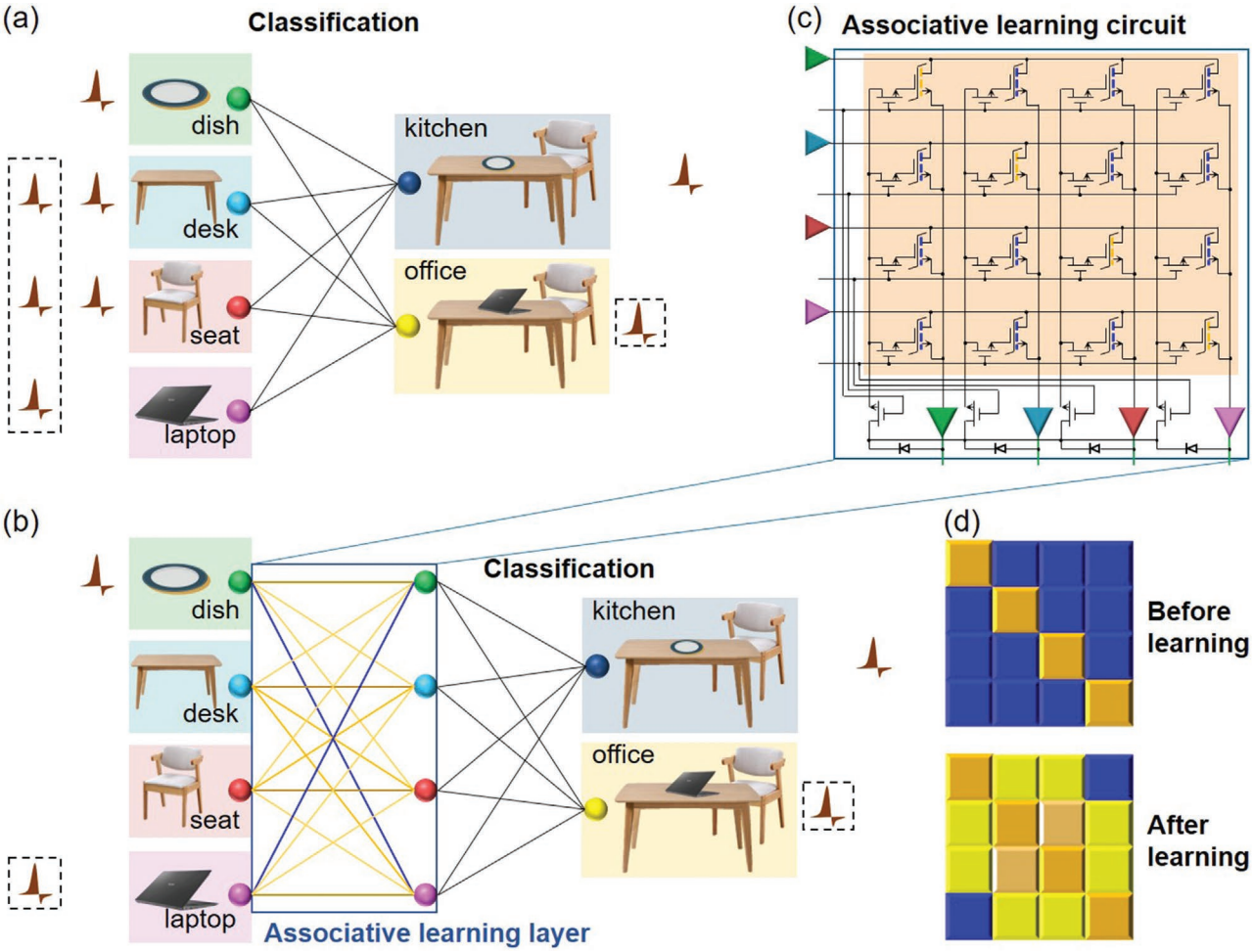


**Figure 5.** Associative learning in multilayer neural networks. a) Profile of an SNN, which is aimed to be capable of that the neuron on behalf of kitchen (dark blue) will fire when dish (green), desk (light blue) and seat (red) appear at the same time, while the neuron on behalf of office (yellow) will fire when laptop (purple), desk and seat present simultaneously. b) A conceptual graph of multilayer neural networks with an associative learning layer after learning process. The yellow (blue) lines connecting the balls from first and second columns, referring high (low) conductance, denote the relevance (irrelevance) between two items. c) The circuit of associative learning layer comprised of four parallel simple SNNs as in Figure 4a. The serial transistors and switches are used to inhibit sneak issue, in which transistors are switched ON after the corresponding neuron active and sustain for the learning or inference period. d) The conductance matrix of synapses array in associative learning circuit before (top panel) and after (bottom panel) learning process.

for realizing that the neuron on behalf of kitchen (dark blue) will fire when dish (green), desk (light blue) and seat (red) appear at the same time, while the neuron on behalf of office (yellow) will fire when laptop (purple), desk and seat are present simultaneously. Ref [26] gives one solution for this kind of training. Associative learning can be carried out by employing the associative learning circuit in Figure 5c, where four simple aSNNs, like in Figure 4a, are connected in parallel to establish relationships between any two of dish, desk, seat and laptop. The serial transistors are used to inhibit sneak current issues, in which transistors are switched ON only for active input neuron and sustained for the learning or inference period. Figure 5d shows the synaptic conductance matrix before and after learning process. The multiassociate memories are expressed in Figure 5b. The balls with different colors represent the four input ports. The yellow (blue) lines connecting the balls from first and second columns, referring high (low) conductance, denote the relevance (irrelevance) between two items. As seen from conductance matrix of synapses array in associative learning circuit (Figure 5d), before training, only the association (high conductance along diagonal positions and otherwise low conductance) between the same item exists, while after training any two of the items reinforces each other except the pair of dish and laptop. As shown in Figure 5b, when merely the dish signal arrives, desk neuron and seat neuron will be also activated, signifying the classification of kitchen. Analogously, the office will be discerned when only the laptop appears. If three items turn up simultaneously, the two neurons will both fire but at different frequency where the kitchen (office) neuron would possess higher frequency when dish (laptop) signal appears. Taking the earlier-one-win mechanism, in which the neuron that reaches the threshold at the earliest will fire a spike and send inhibitive lateral connections to other slower neurons in the same layer to prevent them from possible firing,[59] the classification for kitchen and office is still successful. This means that the scene of kitchen or office can be recalled by associative memorization by inserting the associative learning layer in the classification neural network without influencing its original tasks.

The success of associative memory in the ferroelectric synaptic transistor network is very attractive for artificial intelligence and recognition tasks in rough environments, such as plate numbers with dirty spots or human faces with masks. As demonstrated in **Figure 6**, plate numbers can be recalled successfully from their incomplete pixels. Figure 6a shows the human associative memorization for recalling a leopard from its unique spots. Analogously, the recalling of handwritten numbers is demonstrated by a simplified ferroelectric synaptic transistor network. The hardware and topological structure of the neuromorphic network constituted by ferroelectric synaptic transistors is displayed in Figure 6b,c. Each pixel in number images is analogized as voltage pulse trains. 10 voltage pulses stand for one pixel. The gray-level disperse in output images is due to the different number of fires from integrate-and-fire

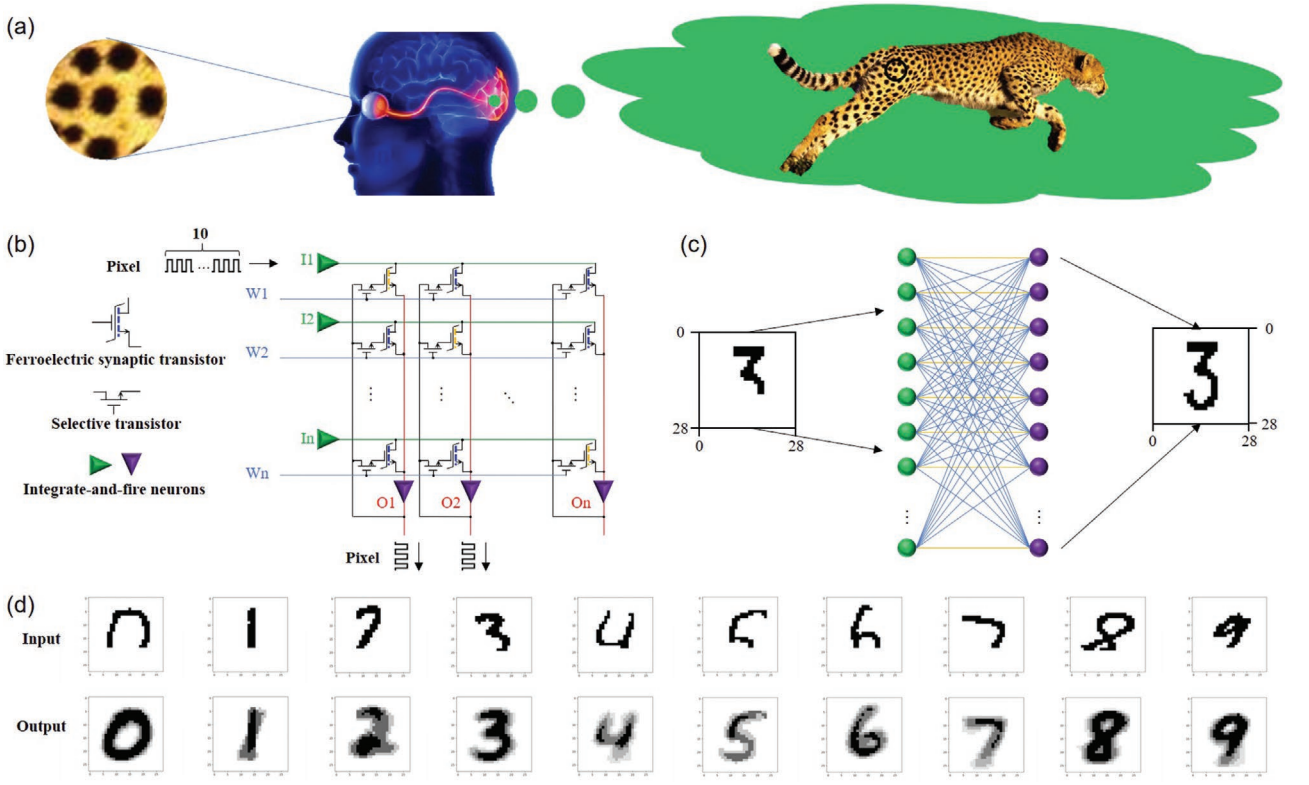


**Figure 6.** Associative memory based on the ferroelectric synaptic transistor network. a) The human associative memorization for recalling a leopard from its unique spots. b) The hardware structure of the simplified ferroelectric synaptic transistor network for associative memory. c) The topological structure of neuromorphic network in (b). d) A simulation shows that whole number pixels (bottom panels) are outputted from the hardware (one number for one hardware) even only their incomplete pixels are inputted.

neurons in which the number of fires is normalized to present the output image. As the simulation shows in Figure 6d, after online training with 600 different handwritten pictures, whole number pixels (bottom panels) are outputted successfully from hardware (one number for one hardware) even only their incomplete pixels (top panels) are inputted. Excitingly, multiassociative memories are also available in this simplified ferroelectric synaptic transistor network. As demonstrated in Figure S3 (Supporting Information), whole number pixels (bottom panels) are outputted from the hardware ("1," "2," "3," and "4" number for one hardware) even only their incomplete pixels are inputted. The proposed ferroelectric synaptic transistor network is superior to conventional auto-associative HNN (note S5, Supporting Information) because of its unique characteristics including self-adaptive learning, one-step recalling and availability to SNNs multilayering.

## 6. Conclusions

Ferroelectric memory is widely accepted as potential synaptic devices taking advantage of its nonvolatile, low power and robust switching dynamics. One concerns for reported ferroelectric synapses is the dissimilar response to rate-based stimuli compared with biological synapses, for example, the absence of STM and rate-based BCM learning rule, which is crucial for associating and learning. Here we clarify that the synergetic effect of depolarization field and imprint field arising from nonideal part of ferroelectric films would induce the evolution of internal electric field over time inside ferroelectric domains, contributing to-and-fro creep motion of ferroelectric domain walls in response to voltage pulses. These properties allow STM and rate-based BCM learning rule in ferroelectric synapses.

All kinds of spike-based Hebbian synaptic plasticity including STM to LTM transition, SRDP (BCM rule) and STDP, were realized in single ferroelectric synaptic transistor in which energy consumption is less than 1 fJ for every synaptic operation. This inspires a persuasive and anticipant envision that the ferroelectric domain walls, existing as intermediate states of polarization reversal, are ideal for simulating neuronal ion channel and intracellular ionic dynamics which dominate the Hebbian synaptic plasticity in a biological synapse. Compared with the aVLSI implementation of full Hebbian synaptic plasticity, our single ferroelectric synaptic transistor shows superior features, not only simplicity, low power and high density, but also higher imitativeness to biological brain.

On the neural network level, we propose a ferroelectric synaptic transistor network that is capable of associative learning and one-step recalling of the entire set of data from only partial information. Assisted by the third terminal to control the ferroelectric domain dynamics, self-adaptive coupling between neurons is successfully realized by concurrently updating synaptic weight. Using this ferroelectric synaptic transistor network, Pavlov's dog experiment and multiassociative memories are demonstrated. Interestingly, this aSNN provides a smart building block for multilayer neural networks with the ability of associative memory without changing their original learning tasks and for artificial intelligence and recognition tasks in a rough environment. Our work shows that ferroelectric synaptic transistors are very competitive and promising for mimicking bio-inspired functions and would open new avenues for associative-memory hardware neuromorphic computation.

As for hardware realization of the designed ferroelectric synaptic network and its extension in multilayers SNNs, first, appropriate spiking neuron devices need to be explored to form the monolithically integrated deeper SNNs. Secondly, despite of a high memory density using 2D semiconductors, the technique of large-area 2D semiconductors with uniform electronic properties is still unmatured, which limits the yield and lateral size of arrays. These issues we believe will be conquered as the development of artificial neurons[60] and engineering of 2D semiconductors.

## 7. Experimental Section

*Device Fabrication and Electrical Measurements*: Triple layers of $MoS_2$ were prepared by mechanical stripping method from commercially available crystals of molybdenite (SPI Supplies brand Moly Disulfide) using the Scotch-tape micromechanical cleavage technique pioneered for the production of graphene. Triple layers of $MoS_2$ were deposited on an ≈285 nm thick $SiO_2$ dielectric layer on top of a highly doped p-type Si wafer (resistivity $<5 \times 10^{-3}$ Ω cm). The electrical contacts were patterned on top of $MoS_2$ flakes using electron beam lithography and conventional lift-off technique. The device was then annealed at 200 °C in a vacuum tube furnace for 2 h (100 sccm Ar) to form ohmic contact and thus decrease contact resistance. First, the P(VDF-TrFE) (70:30 mol%) ferroelectric polymer power was dissolved in the diethyl carbonate with 2.5 wt%. Then the P(VDF-TrFE) films with a thickness of ≈100 nm were prepared by spin coating on the top of source and drain electrodes and $MoS_2$. After that, the P(VDF-TrFE) films were annealed at 135 °C for 4 h to improve the crystallinity. Finally, 10 nm Al top gate electrode were deposited by electron beam evaporation through a shadow mask to construct ferroelectric transistor. The channel $MoS_2$ length ($L$) and width ($W$) of the fabricated transistor are 5 and 5 µm, respectively. The *P–V* hysteresis loop of the P(VDF-TrFE) capacitor was investigated using a Radiant Precision LC system at a test frequency of 10 kHz. All the electrical measurements were performed at room temperature in atmosphere using a Keithley 4200A-SCS parameter analyzer with remote preamplifiers. All the channel conductance was collected by applying a DC bias (0.5 V) between source and drain.

*Simulation*: The aSNN using synapses and neurons to realize associative learning was built with MATLAB Simulink. The threshold voltage of the neurons using in this network was $V_{TH} \approx 3.7$ mV. The weight update rule in the simulation is as followings

$$\begin{cases} G\left(t_s^{i+1}\right) = G\left(t_s^{i}\right) + \Delta G \\ \Delta G = \alpha e^{-\Delta t_s^i/\tau} + \beta \end{cases} \quad (4)$$

where $t_s^i$ is the time when neuron $n_2$ fires and emits the $i$th pulse; $\Delta G$ is the conductance change; $t_s^i = t_s^{i+1} - t_s^i$ is the time interval when neuron $n_2$ emits two adjacent pulses.

Equation (4) is fitted from Figure 3b. The fitted parameters are $\alpha$ = 1.165 nS, $\beta$ = 0.416 nS, and $\tau$ = 19.476 ms, respectively.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

Data available on request from the authors.

## Keywords

associative memory, ferroelectrics, PVDF, synapses, synaptic transistors

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