

TOPICAL REVIEW

## Ferroelectric field-effect transistors based on HfO<sub>2</sub>: a review

To cite this article: Halid Mulaosmanovic *et al* 2021 *Nanotechnology* **32** 502002

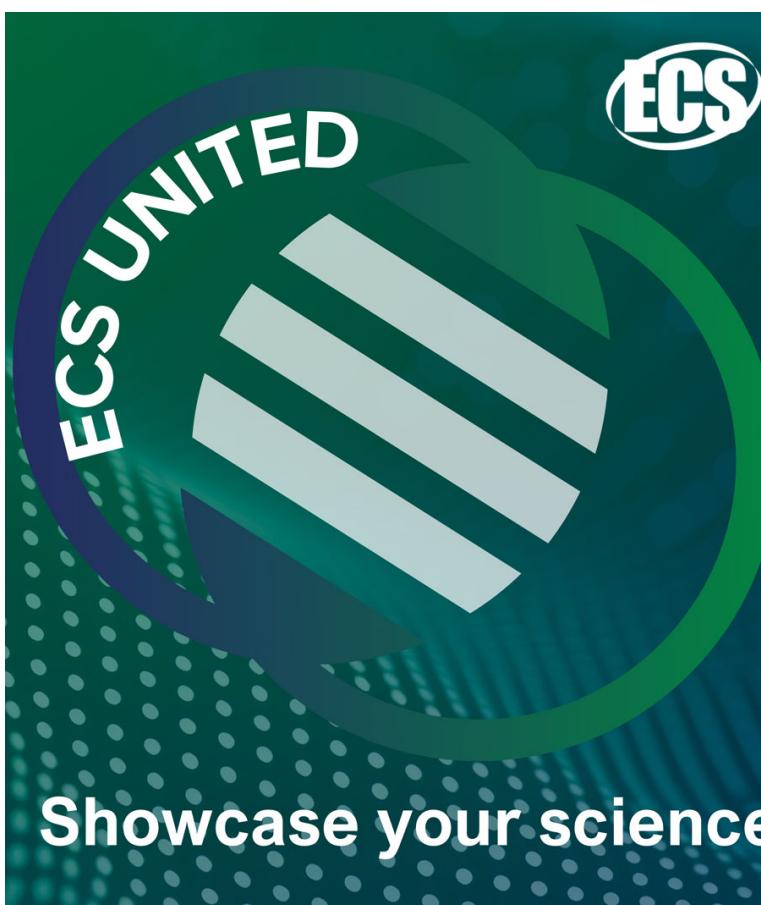
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## Topical Review

# Ferroelectric field-effect transistors based on HfO<sub>2</sub>: a review

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Received 14 March 2021, revised 2 June 2021

Accepted for publication 27 July 2021

Published 22 September 2021



### Abstract

In this article, we review the recent progress of ferroelectric field-effect transistors (FeFETs) based on ferroelectric hafnium oxide (HfO<sub>2</sub>), ten years after the first report on such a device. With a focus on the use of FeFET for nonvolatile memory application, we discuss its basic operation principles, switching mechanisms, device types, material properties and array structures. Key device performance metrics such as cycling endurance, retention, memory window, multi-level operation and scaling capability are analyzed. We also briefly survey recent developments in alternative applications for FeFETs including neuromorphic and in-memory computing as well as radiofrequency devices.

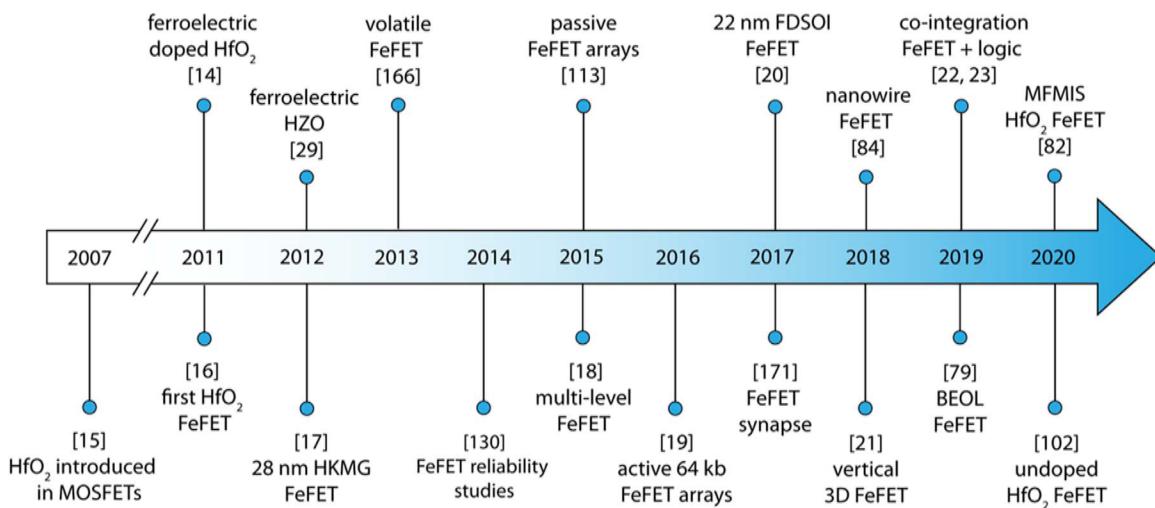
Keywords: ferroelectric field-effect transistor, ferroelectric hafnium oxide, ferroelectric memory, ferroelectric switching, solid-state memory, ferroelectric FET (FeFET), nonvolatile memory

(Some figures may appear in colour only in the online journal)

### 1. Introduction

The idea of using a ferroelectric material to modulate the surface conductivity of a semiconductor layer was originally proposed by Bell Labs in 1957 [1–4]. One objective was to create a device capable of switching and storing information in a nonvolatile manner, which can be read out nondestructively [3]. The first experimental reports of such devices, which today are called ferroelectric field-effect transistors (FeFETs), date back to the 1960s [5, 6], when thin-film transistors based on cadmium sulfide (CdS) were deposited upon a thin layer of ferroelectric triglycine sulfate (TGS). Moll and Tarui [5] demonstrated that the remanent polarization of the TGS crystal could indeed control the space charge within the CdS semiconductor and induce a variation in device resistance of 25%. Zuleeg and Wieder [6] reported that such a ferroelectric field-effect also resulted in changing the threshold voltage ( $V_T$ ) for the onset of drain current of the transistor, which is the most distinctive attribute of the FeFETs as we it also know today.

The advent of new ferroelectric materials, such as simple and layered perovskites, as well as advances in growing thin films prompted the evolution of the FeFET technology. In 1974, S-Y Yu [7] reported the first FeFET having a metal–ferroelectric–semiconductor (MFS) structure, fabricated on a bulk semiconductor (silicon) using a ferroelectric bismuth titanate film. This device structure had the advantage of being compatible with planar silicon technology and is very similar to that of the conventional metal oxide semiconductor FET (MOSFET), except that the gate oxide is replaced by an active ferroelectric layer. However, the MFS structure displayed certain integration drawbacks that motivated the introduction of a buffer interlayer between the ferroelectric and semiconductor (MFIS FeFET). Many different perovskite ferroelectrics came into play, including lead zirconate titanate (PZT) and strontium bismuth tantalate (SBT). In the 2000s, these devices attracted considerable attention of researchers and industry, reaching sophisticated levels of integration and showing very promising memory performance [8]. For



**Figure 1.** Evolution of  $\text{HfO}_2$ -based FeFET devices and their derivatives from the establishment of  $\text{HfO}_2$  as standard gate dielectric in CMOS technology and the discovery of ferroelectricity in  $\text{HfO}_2$  until today.

example, Sakai *et al* [9] demonstrated SBT-based FeFETs with a large memory window and almost unlimited cycling endurance ( $>10^{12}$ ), and later on, a proper functionality in nonvolatile logic (NVL) circuits [10] and in 64 kbit NAND memory arrays [11].

Nevertheless, despite continuous technology improvements and although the idea of using a FeFET as a non-volatile memory (NVM) element came up much earlier than the floating-gate memory transistor [12], the FeFET has never experienced the extraordinary evolution the flash memory technology had, thus failing to reach the market. There are several reasons for that, such as demanding integration of perovskite ferroelectrics on Si, large depolarization fields impairing data retention, and limited vertical and lateral device scaling. In fact, to achieve a reasonable memory window and low gate leakage, the perovskite ferroelectric layer has to be thicker than 100 nm [9, 13].

The discovery of ferroelectricity in hafnium oxide ( $\text{HfO}_2$ ) thin films, which was reported ten years ago [14], holds promise to solve or considerably mitigate many of the abovementioned issues of the perovskite FeFET technology. First,  $\text{HfO}_2$  has been massively used by the semiconductor industry as the gate dielectric in high- $k$  metal gate (HKMG) MOSFETs since its introduction in a manufacturing process by Intel in 2007 [15], hence displaying a full CMOS compatibility. Then, when compared to the perovskite ferroelectrics,  $\text{HfO}_2$  has a relatively wide band-gap ( $E_G \sim 5.3$  eV) and large band offset with Si, considerably reducing the parasitic leakage through the gate stack. Finally, the large coercive field ( $\sim 1 \text{ MV cm}^{-1}$ ) combined with comparably low permittivity ( $k \sim 30$ ) enables stable data retention and a reasonable memory window even at film thicknesses of a few nanometers. These attributes have led to very rapid advances of the  $\text{HfO}_2$ -based FeFET technology, as illustrated in figure 1: from the first experimental report of functional FeFETs in 2011 [16], over the device integration in the 28 nm HKMG technology [17] and its first multi-level storage demonstration in ultra-scaled devices [18], to larger memory

arrays [19] and integration in advanced planar [20] and vertical [21] technologies as well as the co-integration of logic and FeFET devices in close proximity sharing the same active area [22, 23]. The latter not only draws attention for embedded NVM applications, but also makes the FeFET highly attractive for neuromorphic and logic-in-memory computing concepts, as evidenced by the growing number of the related publications over the last years.

In this paper, we introduce the basic operation principles of the FeFET and review its main switching mechanisms (section 2), discuss possible device types, employed materials as well as FeFET array structures (section 3). Section 4 deals with the key device performance parameters such as memory window, endurance, retention and scaling. Finally, section 5 provides an overview on potential applications for memory devices and beyond, which is followed by concluding remarks in section 6.

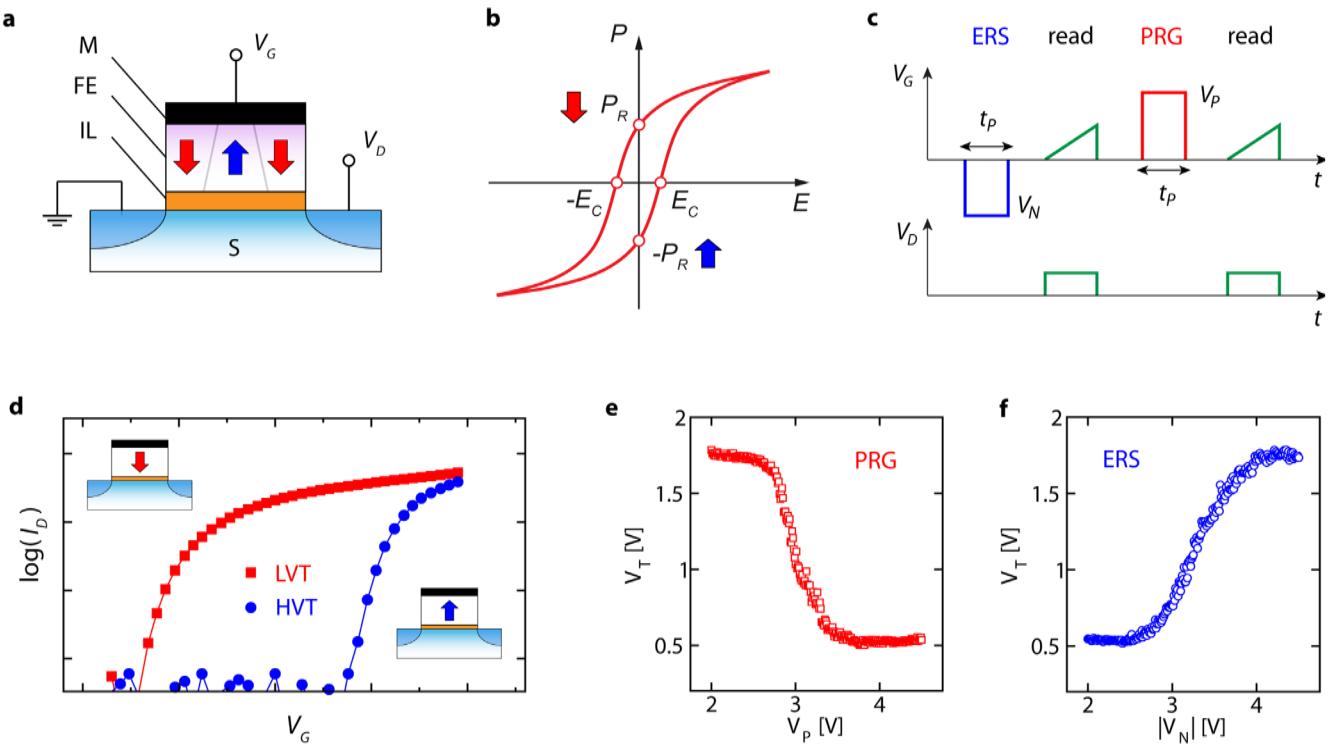
Despite the FeFET and the negative capacitance FET (NC-FET) [24] have a similar structure, the latter will not be object of this review article, whereas comprehensive overviews on the topic can be found elsewhere [25, 26].

## 2. Operation principles and switching mechanisms

### 2.1. Operation principles

Here we introduce the basic terminology and concepts regarding the operation of FeFETs. Figure 2(a) shows the sketch of the MFIS device structure, which is predominantly present in the literature and will be mainly considered in this review. Other FeFET types will be discussed in section 3. The MFIS stack comprises:

**Ferroelectric (FE) layer:** it is used to store information and is embedded into the gate stack of the transistor, building in this way a one-transistor (1T) memory cell. Typically, FE materials display a characteristic polarization–electric field ( $P-E$ ) hysteresis shown in figure 2(b). They possess two distinct yet equivalent polarization states, namely  $+P_R$  and



**Figure 2.** (a) Schematic structure of the MFIS FeFET, indicating the composition of the gate-stack and the adopted gate ( $V_G$ ) and drain ( $V_D$ ) voltages; (b) sketch of the FE  $P$ - $E$  hysteresis; (c)  $V_G$  and  $V_D$  pulses for write and read operations; (d) the resulting experimental  $I_D$ - $V_G$  curves for the LVT and HVT states. Reproduced from [27] with permission from the Royal Society of Chemistry; experimental PRG (e) and ERS (f) transitions as a function of pulse amplitude for a large-area FeFET ( $W = L = 1 \mu\text{m}$ ), showing more than 64 intermediate  $V_T$  states. Pulse width was  $t_P = 1 \mu\text{s}$ . © [2020] IEEE. Reprinted, with permission, from [28].

$-P_R$ , called remanent polarization. These remain stable even in the absence of the applied electric field  $E$ . The microscopic origin of the two  $P_R$  values is associated to the non-centrosymmetric crystalline structure of FE materials and to the consequent presence of permanent electric dipoles within the unit cell. The dipoles can assume two stable configurations, which are usually referred to as polarization ‘up’ and ‘down’ (indicated by arrows in figure 2(b)). The switching from one  $P$  state to the other is reversible and driven by the electric field, which has to be larger than a critical value called coercive field  $E_C$ . This review paper deals with  $\text{HfO}_2$ -based FE materials, which can consist of pure or doped  $\text{HfO}_2$ , as well as of the solid solution of  $\text{HfO}_2$  and  $\text{ZrO}_2$  at different concentrations [29], which is typically referred to as  $\text{Hf}_{1-x}\text{Zr}_x\text{O}_2$  or simply HZO. While the most robust FE properties are present in thin films of around 10 nm thickness, the ferroelectricity has been reported over a wide thickness range, spanning from 1 nm [30] to 1  $\mu\text{m}$  [31], and quite recently, even in bulk crystals [32]. Typical  $P_R$  and  $E_C$  values are  $10\text{--}40 \mu\text{C cm}^{-2}$  and  $1\text{--}2 \text{MV cm}^{-1}$ , respectively [33]. So far, ferroelectricity in  $\text{HfO}_2$  has been experimentally attributed to the orthorhombic ( $Pca2_1$ ) [14, 34] and rhombohedral ( $R3m$  or  $R3$ ) [35] crystalline phases, whereas first-principles calculations [36–38] suggest that, besides the former, some additional polar polymorphs might enable the FE properties in  $\text{HfO}_2$ .

**–Interfacial layer (IL):** it separates the FE layer from the semiconductor channel and is typically very thin (0.5–2 nm).

Although the IL may spontaneously grow (e.g. through thermal oxidation of the semiconductor), usually it is intentionally placed there and serves as a buffer layer with manifold functions, such as: (a) preventing the inter-diffusion of elements between the FE and the substrate; (b) enabling neat deposition and growth of the FE; (c) providing a high channel-interface quality, indispensable for a large carrier mobility and, thus, high transistor performance. Even if the IL does not store information by itself, it has a significant impact on the key memory figures of merit, like data retention and endurance, as will be exemplified in section 4.

**M** and **S** in figure 2(a) indicate metal gate and substrate (or semiconductor), respectively, like in conventional MOSFETs.

The key operation principle of a FeFET consists in the FE layer exerting the field-effect onto the transistor channel through the FE polarization charge  $P$ . In fact, as  $P$  within the FE represents the electric dipole moment per unit volume, the resulting surface charge at the FE-IL interface will modulate the conductivity of the channel via Coulomb coupling. By taking an n-channel FeFET as an example, the polarization pointing down attracts the minority carriers toward the channel, increasing its conductivity, thus yielding a low threshold voltage state (low- $V_T$  or LVT). Conversely, polarization pointing up tends to repel these carriers, decreasing the channel conductivity and inducing a high- $V_T$  state or HVT. Similarly to flash devices, these two distinct  $V_T$  values are used to store binary information. The operations of setting the

LVT and HVT states are generally called program (PRG) and erase (ERS), respectively, and are usually achieved by applying sufficiently large positive and negative voltage pulses at the gate, respectively, as depicted in figure 2(c). Figure 2(d) shows the obtained transfer curves (drain current–gate voltage,  $I_D-V_G$ ) for the LVT and HVT, which are separated by a voltage difference called memory window, given by  $MW = HVT - LVT$ .

For a sufficiently high  $P$  in the FE, the memory window is often approximated by a simplified expression [39, 40]:

$$MW = 2 \cdot \alpha \cdot E_C \cdot t_F, \quad (1)$$

where  $t_F$  is the thickness of the FE layer and  $\alpha$  is a parameter with a weak dependence on several material properties, such as the polarization  $P$  and the dielectric constant of the FE,  $\epsilon_F$ .  $\alpha$  is generally lower than 1 and can account for second-order effects that also contribute in reducing the MW. Thus, it can be considered a measure of ideality for a given FeFET. Considering that typical values for  $HfO_2$  films are  $E_C = 1 \text{ MV cm}^{-1}$ , and  $t_F = 10 \text{ nm}$ , the maximum MW for a MFIS-FeFET is 2 V. In section 4, various strategies for the MW enlargement will be discussed.

The way the write and read operations are carried out is essential to a correct determination of the two  $V_T$  states, hence, of the MW. Past reports [41] have shown that the best estimation is achieved when the two operations are temporally separated and both performed in a pulsed manner, as shown figure 2(c), whereas the  $I_D-V_G$  read sweep has to be as fast as possible. In contrast, many previous works adopt another approach, consisting of a slow forth and back  $V_G$  voltage sweep, which at the same time serves to write the state but also to read the  $I_D-V_G$  curves. This approach, however, requires caution, as it may severely disturb the written state, largely underestimating the MW, and may induce other effects such as apparent steep subthreshold slope and increased cycle-to-cycle variability [41].

Figures 2(e) and (f) show the PRG and ERS transitions as a function of the respective write pulse height. The switching is complete at a height of 4 V and pulse width of 1  $\mu\text{s}$ , thus testifying on the low-power operation of this memory concept. Figures 2(e) and (f) also illustrate that a continuum of intermediate  $V_T$  states exists besides the nominal LVT and HVT. These would correspond to different degrees of partially switched polarization in the FE, which can be represented by minor hysteresis loops (sub-loops), instead of the saturated loop in figure 2(b). Such different hysteresis topologies are commonly described by the Preisach model of hysteresis [42, 43].

## 2.2. Switching mechanisms

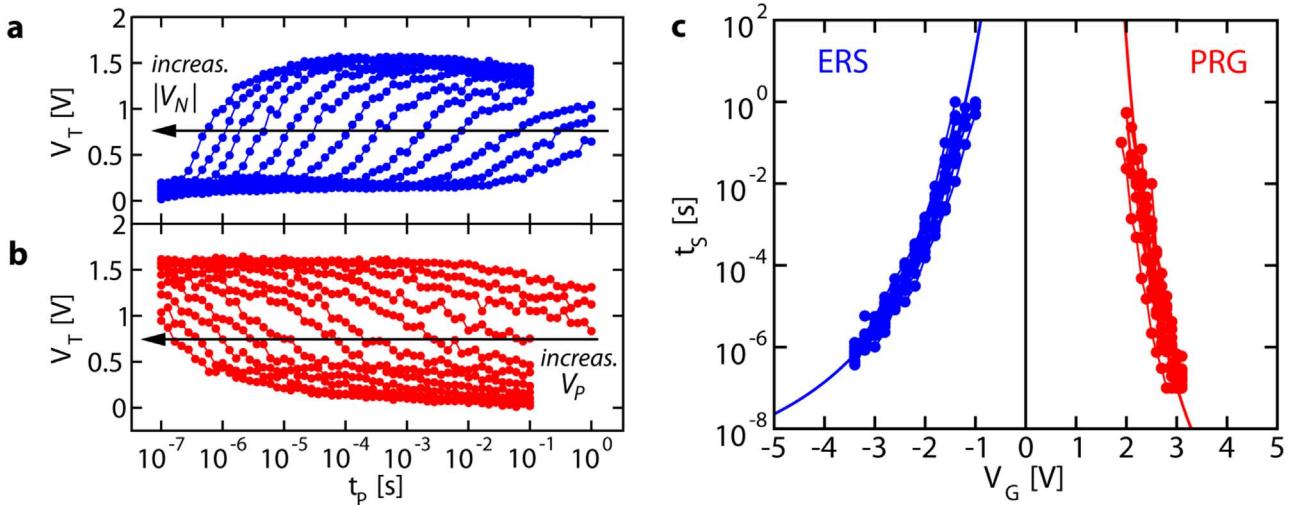
The static Preisach model of the FE hysteresis coupled with the transistor load lines can well capture both PRG (i.e. HVT  $\rightarrow$  LVT) and ERS (i.e. LVT  $\rightarrow$  HVT) switching transitions as a function of the pulse amplitude (figures 2(e), (f)) as well as provide a complete electrostatic description of the gate stack under various operation points of the FeFET [40]. However, as a static model, it is inapplicable for describing dynamic

reversal processes being dependent not only on electric fields but also on the duration of the applied excitation. In fact, as will be shown throughout this Section, the full switching in FeFETs can occur even at electric fields in the FE layer that are much lower than  $E_C$  (sub-coercive excitation), provided that the pulses are sufficiently long or sufficiently often repeated (accumulative excitation). Both switching types are not described by the static Preisach approach. Already in 1954, Merz [44] showed that the switching time in  $BaTiO_3$  exhibits an exponential dependence on the electric field and explained the reversal behavior with the nucleation of new FE domains and their subsequent growth. Different theories and refinements have followed since, and today, it is commonly accepted that the switching time in bulk, single crystals and epitaxial films is limited by the sideway motion and coalescence of the reversed domains (Kolmogorov-Avrami-Ishibashi or KAI model) [45], whereas the switching in thin, often polycrystalline films, is limited by the nucleation of the reversed domains over a broad time spectrum (Nucleation Limited Switching or NLS model) [46].

Müller *et al* [47] studied the polarization switching process in 10 nm thick Si doped  $HfO_2$  polycrystalline films in FE capacitor structures over an extended range of pulse times and amplitudes, and suggested it is in accordance with the NLS rather than with the KAI model. A similar and pronounced time-voltage switching dependence has been also observed in FeFETs [48, 49]. Mulaosmanovic *et al* [50] investigated the switching kinetics in nanoscale  $HfO_2$ -based FeFETs and showed that the classical nucleation theory can be applied to describe the FE reversal during the PRG and ERS transitions over a broad range of switching times, amplitudes and temperatures. Based on this, they derived a simple statistical model for domain switching and proposed an expression relating the switching time in a FeFET to the applied gate voltage:

$$t_S = t_0 \exp \left[ \frac{\alpha_N}{k_B T} \cdot \frac{1}{(V_G - V_0)^2} \right], \quad (2)$$

where  $k_B$  and  $T$  are the Boltzmann constant and temperature, respectively, whereas  $t_0$ ,  $\alpha_N$  and  $V_0$  are the minimum switching time, exponential constant and voltage offset [50, 51]. The exponential constant  $\alpha_N$  depends on the intrinsic properties of the FE material, including the polarization  $P$  and the surface energy (domain wall energy), and on the geometry of nucleating domains [50]. Figure 3 shows one such experiment, where the ERS and PRG transitions were studied by using pulse schemes in figure 2(c) with variable pulse widths  $t_P$  and amplitudes  $V_N$  and  $V_P$ , respectively. The resulting switching curves, which are here illustrated as the threshold voltage ( $V_T$ ) evolution as a function of  $t_P$  for different pulse amplitudes, evidence a significant time-voltage trade-off: the larger the pulse amplitude the shorter the switching time and vice versa. The relationship has an exponential character described by equation (2), which can be easily visualized in figure 3(c), showing the switching time  $t_S$ , defined as  $t_P$  necessary to switch half of the maximum MW, as a function of pulse amplitude. These experiments also



**Figure 3.** Switching kinetics in FeFETs: (a) ERS transition as a function of  $t_p$  for  $V_G = V_N$  from  $-3.4$  to  $-1$  V with step  $0.2$  V. (b) PRG transition for  $V_G = V_P$  from  $+2$  to  $+3.1$  V with step  $0.1$  V. (c) Extracted switching time  $t_S$  as a function of pulse amplitude  $V_G$  for several devices, showing the exponential character expressed in equation (2) (solid lines). The FeFET was a large-area device with  $W = L = 450$  nm. © [2020] IEEE. Reprinted, with permission, from [52].

indicate that the switching speed in FeFETs can be easily tuned spanning over 7 decades (from nanoseconds to seconds), just by varying the magnitude of the applied voltages by less than 2 V. This is of great importance for all of the potential applications (section 5).

Several research groups further investigated the switching kinetics, mostly in capacitor structures, confirming the suitability of the NLS model for describing the switching in thin HfO<sub>2</sub> films [53, 54]. For example, Gong *et al* [53] extracted the NLS modeling parameters for Al:HfO<sub>2</sub> FE capacitors, and used the model to predict the retention behavior at room and elevated temperatures. Alessandri *et al* [54] investigated the switching in HZO FE capacitors, and besides determining the main NLS parameters, they extracted the distribution of local field variations. They pointed out that a broad distribution favors partial polarization switching, whereas a narrow one is rather suitable for fast and full transitions between the saturated polarization states.

### 2.3. Size-dependent switching

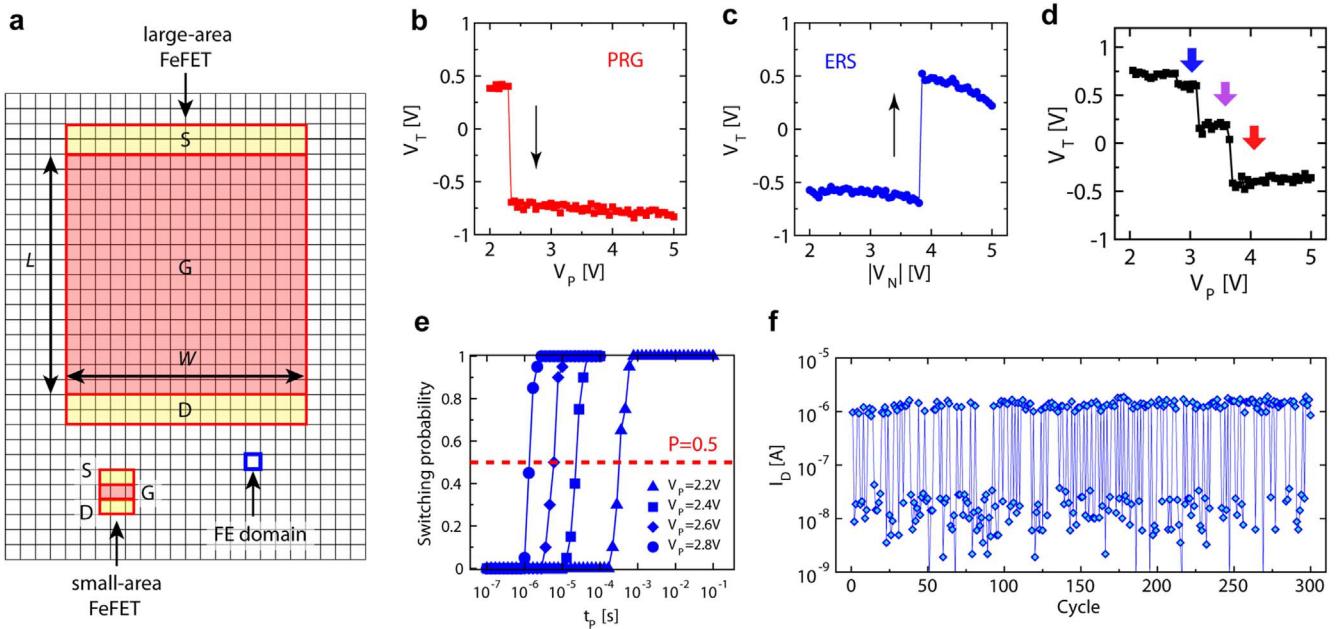
As exemplified in figures 2(e), (f), the PRG and ERS transitions are very gradual and exhibit many intermediate  $V_T$  levels (more than 64 levels) between the nominal LVT and HVT. However, this phenomenon appears to take place only in large-area devices. In fact, the channel width ( $W$ ) and length ( $L$ ) of the transistor in figures 2(e), (f) are  $W = L = 1 \mu\text{m}$ . In contrast, it has been reported that the switching in laterally scaled devices is rather abrupt [50], in some cases even digital, as shown in figures 4(b), (c) for a FeFET with  $W = 80$  nm,  $L = 30$  nm. This evidence indicates that the steepness of the switching transitions is largely size-dependent, which, in turn, suggests a dependence on the number of FE domains contained in the gate stack. Figure 4(a) illustratively describes this scenario: assuming that the domain size is 10–30 nm [50, 55], the gate area of the FeFETs with gradual switching is much larger than that of individual FE domains (large gate

size/domain size ratio), i.e. the polycrystalline FE layer contains many domains having a random orientation of the  $P$  axis. Hence, the gradual switching reflects the broad distribution of individual domain switching fields, i.e. spatial  $E_C$  nonuniformity. On the other hand, the abrupt switching is exhibited by devices with the gate size comparable to that of a single domain (small gate size/domain size ratio).

This suggests that such scaled devices are probably hitting the granularity limits of the FE layer, where each domain will have a significant effect on the channel. In fact, while some scaled devices show abrupt and single switching event (figures 4(b), (c)), others exhibit several discrete switching steps, as shown in figure 4(d). This was attributed to the switching of distinct, single domains (three domains are assumed and indicated by the arrows), having slightly different coercive voltages. It has been also shown that the obtained intermediate  $V_T$  states in figure 4(d) are very stable in time, or, in other words, single domains appear to have independent and steady retention [18].

Another marked property of ultra-scaled devices is stochastic switching. In fact, they exhibit a pronounced dispersion of switching voltages and times, which was explained by the statistical nature of ferroelectric nucleation and modeled as a simple Poisson process [50]. It implies that it is necessary to deal with a probability of switching for a certain set of pulse parameters as shown in figure 4(e), rather than to consider it as being a deterministic event. The extent of stochasticity can be well appreciated in figure 4(f), where a scaled FeFET was repeatedly programmed with a pulse parameter combination for which the switching probability is 50% according to figure 4(e), resulting in a random appearance of LVT and HVT in the outcome [56].

This intuitive picture of size-dependent switching can be further refined by considering the formation of one or more channel percolation paths between source and drain regions, which are induced by some preferentially reversed domains in



**Figure 4.** Size-dependent switching: (a) sketch of a large-area ( $W = L = 500$  nm) and a small-area ( $W = 80$  nm,  $L = 30$  nm) FeFET on top of the FE layer. ‘S’, ‘G’, and ‘D’ stand for source, gate and drain respectively. The FE is represented by a simplified reticle of square FE domains with a size of 30 nm; experimental PRG (b) and ERS (c) transitions as a function of pulse amplitude for a small-area FeFET, obtained by using the same excitation scheme adopted for figures 2(e), (f). Reprinted with permission from [50]. Copyright (2017) American Chemical Society; (d) three switching events in a scaled FeFET, associated with three distinct FE domains indicated by arrows. © [2015] IEEE. Reprinted, with permission, from [18]; (e) switching probability as a function of pulse amplitude and width. The curves can be fitted by assuming a Poisson process. Reprinted with permission from [50]. Copyright {2017} American Chemical Society; (f) stochastic switching over consecutive 300 trials at 50% of probability indicated by the horizontal dashed line in (e). © [2017] IEEE. Reprinted, with permission, from [56].

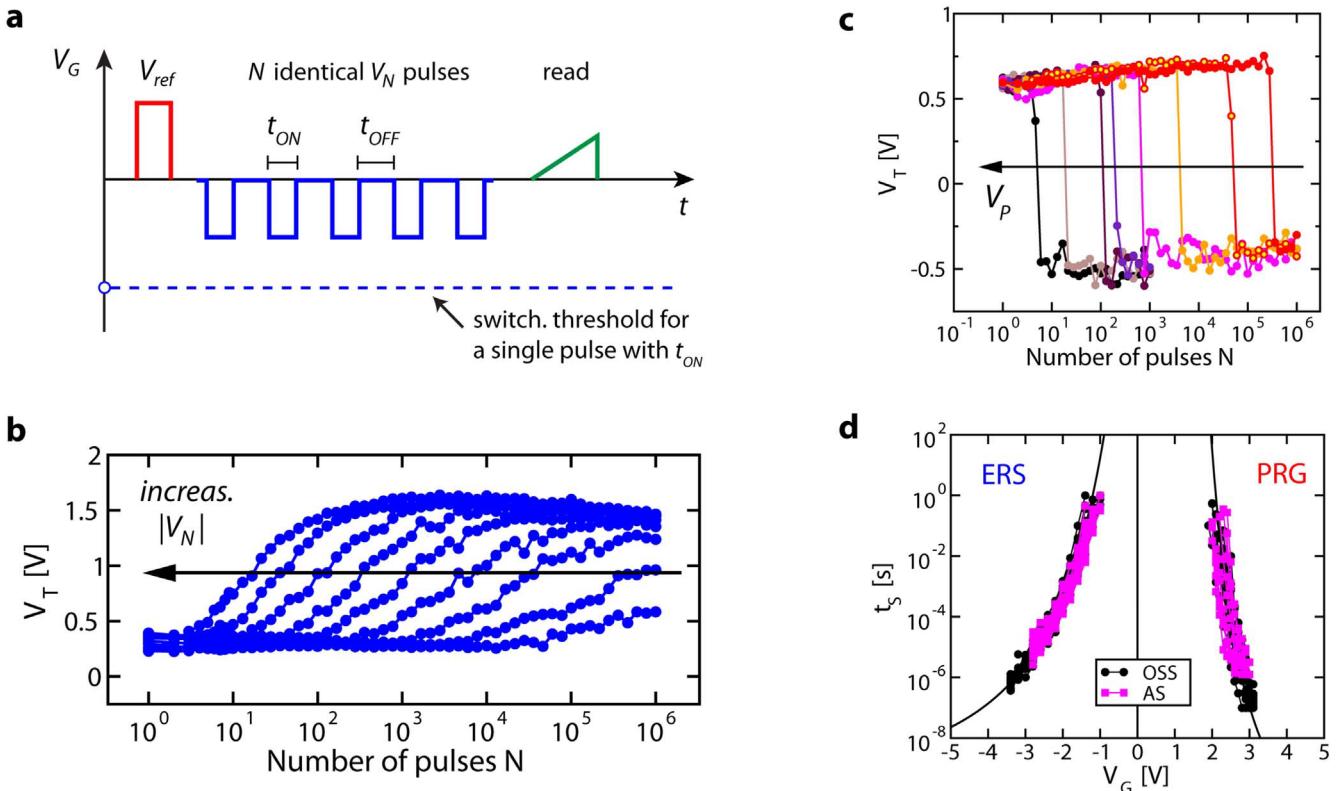
the FE, as recently suggested in [57, 58]. This would indicate that due to the spatial  $E_C$  nonuniformity in the FE layer, preferential clusters of reversed FE domains rather than the whole FE film rule the switching behavior of the device. Such an approach can help in predicting the steepness of the PRG and ERS transitions for any arbitrary device geometry, number of domains and their orientation within the gate-stack.

#### 2.4. Accumulative switching

Although most of the switching investigations concentrate on the effect of a single gate pulse on  $V_T$  (one-shot switching, OSS, figures 2–4), FeFETs can also experience partial or complete switching under a train of sub-critical (or sub-coercive) pulses. Here, the term ‘sub-critical’ indicates that each individual pulse in the train is insufficient to induce any appreciable switching effect, when considered in an OSS experiment. Figure 5 shows one such experiment for a large (figure 5(b)) and a scaled (figure 5(c)) device. Particularly interesting is the behavior of scaled devices (figure 5(c)), which abruptly undergo a transition to the other state only after a critical number of pulses is received [59]. In other words, the switching has an all-or-nothing character, which is maintained irrespective of the applied pulse amplitude. The lower the amplitude, the larger is the number of critical pulses needed to trigger the abrupt switching. This experimental evidence suggests that the device accumulates electrical excitation prior to the complete switching, the reason for which the term

‘accumulative switching’ (AS) has been proposed. AS has been also explained by the ferroelectric nucleation theory, arguing that the ‘accumulation’ of electrical pulses corresponds to the progressive formation of new FE nuclei [59]. This eventually leads to the full switching after a critical number of nuclei has been formed. It has been also shown that AS and OSS show the same time-voltage dependence [52], as illustrated in figure 5(d), where  $t_S$  for AS is the total pulse time given by the sum of each individual pulse duration  $t_{ON}$  in figure 5(a). This further suggests that common physical phenomena (i.e. FE nucleation) rule the two types of switching. Furthermore, Saha *et al* [60] and Alessandri *et al* [61] could reproduce and explain many of the AS properties by using the dynamic phase field modeling, and Monte Carlo simulations in the framework of the NLS theory, respectively.

Interestingly, the accumulation effect appears to be invariant with respect to the interval duration  $t_{OFF}$  between single pulses in figure 5(a), at least up to the maximum explored  $t_{OFF} = 10$  s [52]. It suggests that the formed nuclei do not rapidly decay over the investigated time. This observation could be of particular importance for FeFET array structures, where write and read operations provoke unwanted electrical disturbs on unselected cells. Such disturbs are usually in the form of sub-critical pulses, and can manifest as a train of pulses, which may ‘accumulate’ over time. Moreover, AS may find useful applications in neuromorphic devices based on FeFETs, as will be discussed in section 5.

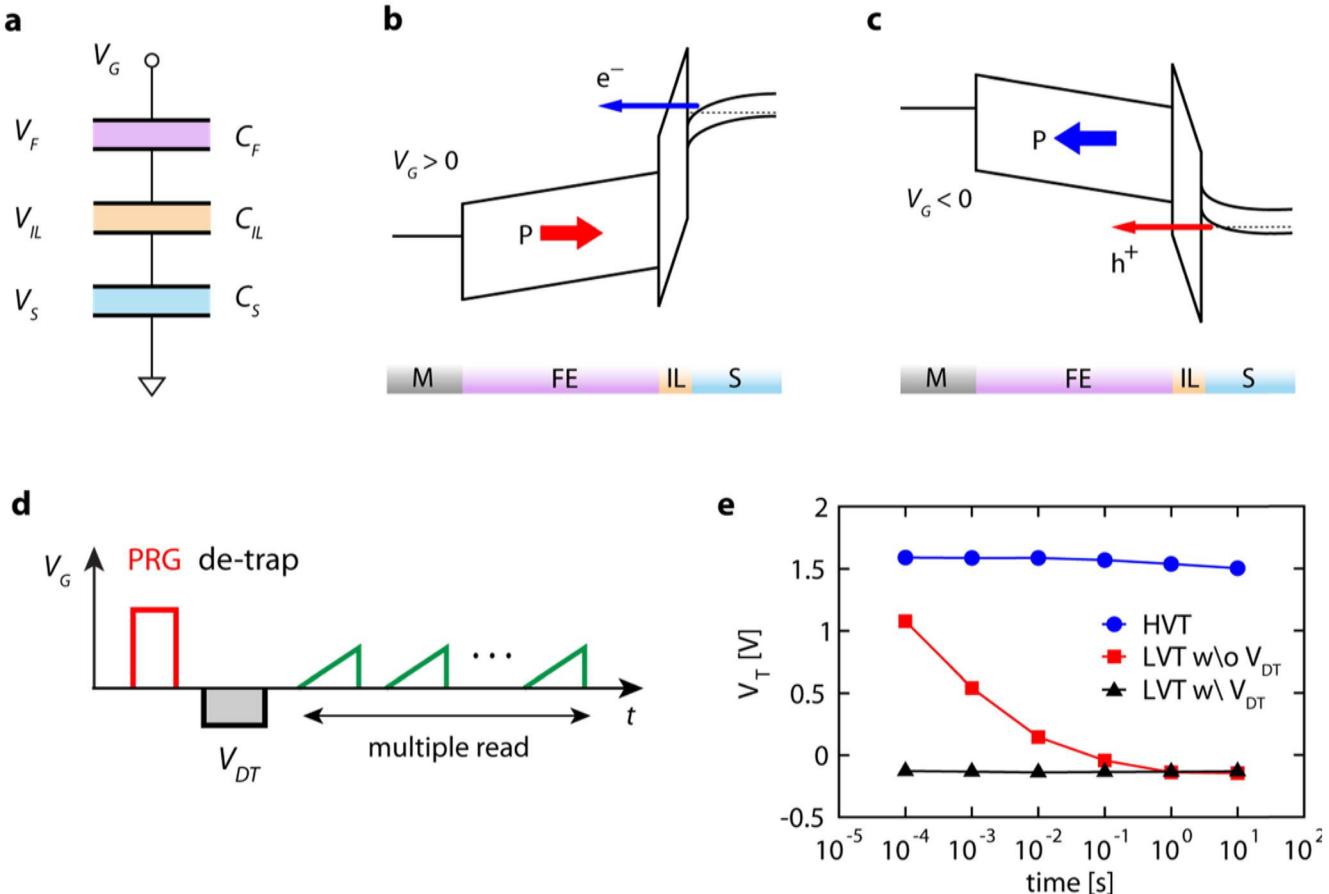


**Figure 5.** Accumulative switching (AS) in FeFETs and its relation to the one-shot switching (OSS): (a)  $V_G$  waveform for ERS AS test, where negative  $V_N$  sub-critical pulses of duration  $t_{ON}$  are applied. PRG AS test (not shown) would have the opposite polarity of write pulses. (b) ERS AS switching for the same large-area device of figure 3 ( $W = L = 450$  nm, gradual switching) for  $V_N$  from  $-2.6$  to  $-1$  V with steps  $0.2$  V, whereas  $t_{ON} = t_{OFF} = 1$   $\mu$ s. (c) PRG AS for a small-area device ( $W = 80$  nm,  $L = 30$  nm, abrupt and all-or-nothing switching) for  $V_P$  from  $2.3$  to  $3$  V in steps  $0.1$  V,  $t_{ON} = t_{OFF} = 1$   $\mu$ s. (d) OSS and AS show the same time-voltage dependence. © [2020] IEEE. Reprinted, with permission, from [52].

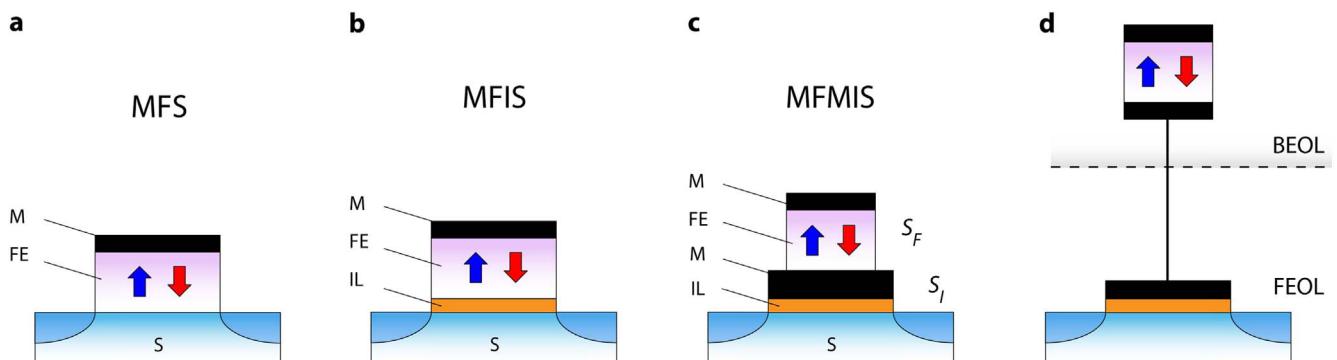
## 2.5. Charge trapping

The MW can experience a considerable reduction due to the injection of parasitic charges from the substrate into the gate stack. The charges are mainly injected and trapped upon the write operations, during which the voltage drops over the different layers in the stack are particularly enhanced. Figure 6(a) shows the capacitive voltage divider for an MFIS FeFET, indicating that the applied gate voltage  $V_G$  can be decomposed in voltage drops over the FE, the IL and the substrate, designated with  $V_F$ ,  $V_{IL}$  and  $V_S$ , respectively. Because of a large difference between the dielectric constants of the FE ( $HfO_2$ ) and IL ( $SiO_2$ ), the latter sustains a large  $V_{IL}$  during PRG/ERS, which consequently induces a particularly strong band bending as illustrated in figures 6(b), (c). This situation favors charge injection, which can occur in the Fowler-Nordheim, modified Fowler-Nordheim or even direct tunneling regime. In particular, electrons are injected during positive PRG pulses and holes during negative ERS pulses at the gate. Consequently, electrons and holes mainly impact the LVT and HVT state, respectively. Trapped charges tend to screen the FE polarization and thus diminish the ferroelectric field-effect onto the transistor channel. In fact, electrons shift the LVT to higher voltage values, whereas holes make the HVT appear lower than it actually is. This can in most severe cases lead to a complete loss of the MW at read-out

performed very shortly after the PRG operation. Fortunately, the effect of trapped charges is transient, as their confinement in the gate stack is not energetically favorable and they tend to leave it spontaneously. The spontaneous de-trapping time depends on the gate stack composition, but it is usually reported in the  $100$  ms– $1$  s range [28, 62], after which the full MW is recovered. This is exemplified in figures 6(d) and (e), which show the  $V_G$  waveform and the experimental results for the de-trapping test, where the spontaneous de-trapping of LVT is indicated by the red line. As the long de-trapping period may limit the read frequency of the device, strategies for a fast electrical de-trapping have been proposed [62], which effectively remove the parasitic charge in nanosecond to microsecond time range. This is achieved by applying the de-trapping pulses ( $V_{DT}$ ), whose amplitude is small enough to avoid any FE switching, yet large enough to expel the trapped charge. Figure 6(e) shows that a properly chosen  $V_{DT}$  can yield a full MW immediately after the write operation (black line). As will be discussed in section 4, charge trapping can have a determinant role for the FeFET reliability. At the moment, this is an increasingly studied topic [63–66] and a complete understanding of the trapping mechanisms, trap position as well as the impact on the device physics and performance (for example interplay between trapping and retention) is yet to be gained.



**Figure 6.** (a) Capacitive voltage divider in a MFIS FeFET; energy band diagrams during (b) PRG and (c) ERS operations, illustrating the injection of electrons ( $e^-$ ) and holes ( $h^+$ ), respectively. (d)  $V_G$  waveform for a short retention and de-trapping test after the PRG operation, with a de-trapping pulse ( $V_{DT}$ ); (e) the resulting experimental LVT evolution within the first few seconds, indicating the spontaneous de-trapping (red line, without  $V_{DT}$ ) and forced electrical de-trapping (black line, with  $V_{DT} = -2\text{ V}, 1\text{ }\mu\text{s}$ ). The HVT state evolution is given as a reference.



**Figure 7.** Basic FeFET gate-stack types: (a) MFS; (b) MFIS; (c) MFMIS; (d) a variant of MFMIS consisting of an MFM capacitor in BEOL connected with the transistor in FEOL area. ‘M’, ‘FE’, ‘IL’ and ‘S’ stand for metal, ferroelectric, interfacial layer and substrate (or silicon), respectively.  $S_F$  and  $S_I$  indicate the area of the MFM and MIS capacitor, respectively, in the MFMIS stack, which can be independently tailored.

### 3. Device types, materials and arrays

#### 3.1. Device Types

Over the years, various FeFET concepts have been proposed, which can be roughly classified in terms of their gate stack composition in three categories, as illustrated in figure 7:

(a) **MFS** (metal ferroelectric semiconductor): this is the simplest FeFET structure, where the FE layer is directly deposited on top of the semiconductor with ideally no IL between them. With regard to the capacitive voltage divider in figure 6(a), MFS FeFET maximizes the voltage drop over the FE layer ( $V_F$ ) with respect to the total  $V_G$ , because  $V_{IL}$  does

not exist, and enables a direct control of the transistor channel by the FE polarization charge. Although the very first FeFETs with perovskite FE layers indeed had the MFS stack [7, 67–69], such a structure presented several drawbacks, due to which the concept was abandoned. The major concerns were the inter-diffusion of elements between the FE and the substrate, and their chemical reactions. By taking an example of  $\text{PbTiO}_3/\text{Si}$  system [70], Pb and oxygen diffuse into Si substrate, whereas Si ingresses the FE film. Similar diffusion processes occur for PZT and SBT on Si. This has several consequences: it impacts the functionality of the transistor channel due to the presence of heavy metal impurities, it changes the stoichiometric composition of the FE layer, thus altering its properties, and it creates unintended transition  $\text{SiO}_2$  layers of poor electrical quality at the FE/Si interface [70, 71]. An additional issue for the MFS FeFETs is the excessive charge injection from the semiconductor into the FE layer [67], which screens the polarization charge and cancels the ferroelectric field-effect, thus nullifying the memory operation of the device.

When it comes to  $\text{HfO}_2$ -based ferroelectrics, similar chemical reactions may take place at the  $\text{HfO}_2/\text{Si}$  interface as well. In fact,  $\text{HfO}_2$  in contact with Si tends to form silicates [72] and silicides [73], which may severely impair the transistor operation. Nevertheless, the adoption of oxide based channel materials instead of Si may alleviate all of the mentioned problems. In the past, the integration of FeFETs with PZT as the FE layer and zinc oxide ( $\text{ZnO}$ ) [74] as well as indium tin oxide (ITO) [75] as the channel materials has been shown. Indium gallium zinc oxide (IGZO) is another oxide semiconductor, which was first reported in 2004 [76]. Among other exciting properties, it is also promising due to high mobility even in thin body transistor structures and easiness of 3D integration. FeFETs with an IGZO-based channel and perovskite [77] as well as organic polymer [78] as the FE layer have been reported in literature. Recently, Mo *et al* [79] have successfully demonstrated an HZO-based FeFET with an ultrathin IGZO channel. It displayed no inter-diffusion processes and a nearly zero low- $k$  dielectric IL between IGZO and HZO, thus ideally being an MFS FeFET. This resulted in a maximized voltage drop over the FE layer and minimized reliability concerns associated with the IL such as charge trapping and subthreshold slope degradation. Similarly, Halter *et al* [80] showed an HZO FeFET with tungsten oxide ( $\text{WO}_x$ ) as a channel material. An additional advantage of oxide based channel FeFETs is their easy fabrication in the back end of line (BEOL), where the size of the device and thermal budget can be relaxed compared to the front end of line (FEOL). It should be, however, noted that both of the mentioned devices in [79] and [80] are junctionless transistors, in the sense that the source and drain junctions are absent, so slightly deviating from the sketch in figure 7(a). The omitted requirement for source and drain implantation and thermal activation might be seen as an additional advantage over junction-based transistors [80].

(b) **MFIS** (metal ferroelectric insulator semiconductor): this gate stack solves the abovementioned issues of the MFS structure by introducing a thin buffer layer (IL) between the

FE and the semiconductor. However, the non-ferroelectric IL does not actively participate in the FE switching and information storage, yet consumes an additional voltage drop  $V_{IL}$  (figure 6(a)), so that a lower  $V_F$  drops over the FE as compared to the MFS stack. Moreover, as the IL introduces an additional capacitive element in series to the FE capacitance, the compensation of the FE polarization charge becomes less efficient. This induces the so called depolarization field  $E_{dep}$ , which may impair the stability of the stored polarization and therefore data retention. Nevertheless, proper stack engineering can circumvent many of the issues, resulting in high performance FeFETs [19, 81], which makes the MFIS structure attractive and predominantly studied in the literature at the moment.

(c) **MFMIS** (metal ferroelectric metal insulator semiconductor): it has a floating conductive layer M between the FE and the dielectric IL. On the one hand, as the FE is sandwiched between two conductive layers, a different matching of capacitances (figure 6(a)) as compared to MFIS is possible, which may significantly reduce  $E_{dep}$ , improving the data retention. On the other hand, an unintended injection of charge carriers into the floating gate (e.g. during PRG or ERS or due to the leakage through the stack), may overscreen the polarization charge and invalidate the FeFET operation. This becomes particularly critical over cycling, as the charges are hard to remove from the floating gate, and tend to accumulate with each cycle. It therefore requires a careful choice of layer materials and their thicknesses. In contrast to MFS and MFIS stacks, the MFMIS has a structural merit in that the MFM capacitor area ( $S_F$ ) and MIS capacitor area ( $S_I$ ) can be independently designed. Tokumitsu *et al* [71] reported that by adjusting the areal ratio  $S_I/S_F$ , and in particular, by making it larger than 1, it is possible to favorably match the charges in the stack, achieving a large MW and good data retention. Recent reports on  $\text{HfO}_2$ -based MFMIS FeFETs have also shown promising results. Yoon *et al* [82] fabricated an  $\text{Pt}/\text{FE}-\text{HfO}_2/\text{TiN}/\text{SiO}_2/\text{Si}$  MFMIS-FET by adopting a 10-nm-thick  $\text{Al:HfO}_2$  FE layer. By changing the  $S_I/S_F$  ratio from 8 to 32, they were able to increase the MW from 1 to 2.8 V, yet maintaining the retention and cycling endurance comparable to the ones in MFIS-FETs.

Figure 7(d) shows another type of the MFMIS FeFET, where however, the MFM stack and the underlying conventional MOSFET are fabricated in physically separated places, but are electrically coupled. For example, the MFM can be deposited in the BEOL whereas the MOSFET in the FEOL module. The advantage of this approach is that the fabrication of the FE capacitor (MFM) is dissociated from that of the underlying transistor, so that different thermal budgets, types of materials as well as MFM size tuning can be exploited, which in FEOL might not be admissible. Ni *et al* [83] reported one such structure having a 10 nm thick HZO MFM BEOL capacitor coupled to the gate of an FEOL MOSFET. They demonstrated that by optimizing the areal ratio between the MFM and MOSFET, the device could achieve low write voltages (<1.8 V), fast operation (<100 ns) and high write endurance (> $10^{10}$  cycles) without degradation, because no charge trapping was present.

It should be mentioned here that many different FeFET geometries are being considered at the moment, which go beyond the classical planar technology shown in figure 7, such as vertical (3D) [21], nanowire [84–86], recess-gate [87, 88] and gate-all-around (GAA) [89] structures. Nevertheless, with due simplifications, also these FeFETs can be easily classified according to figure 7, when the composition of their gate stack is taken into consideration.

### 3.2. Materials

The first demonstration of ferroelectricity in HfO<sub>2</sub> was made with capacitors having a thin HfO<sub>2</sub> film sandwiched between TiN top and bottom electrodes [14], whereas the first HfO<sub>2</sub>-based MFIS FeFETs [16] had the gate stack comprising TiN/Si:HfO<sub>2</sub>/SiO<sub>2</sub>/Si. The choice of these materials is not casual, but reflects the fact that such gate-stacks are adopted in conventional HKMG transistors by the semiconductor industry. The FeFETs that were reported over the following years have mainly kept this stack composition, as it is close to the base line transistor fabrication and thus relatively easy to implement with existing infrastructures. Nevertheless, some important variations and improvements have been made. For example, it is known that various doping species can stabilize the FE phase in HfO<sub>2</sub> [29, 90, 91], which, however, largely differ in their doping concentration window and thermal budget. While elements like Si, Al and La, which are commonly present in the semiconductor fabs, have a relatively narrow dopant concentration window (2–4 %cat for Si [92] and Al [93], 12 %cat for La [94]) and require high anneal temperatures (>700 °C), the Zr doping in HZO films offers a very broad dopant concentration window (>40 %cat) and comparably low anneal temperatures (<500 °C) [29]. This makes the former elements also suitable for a gate-first transistor fabrication process within the FEOL module, where the high temperature source and drain junction activation anneal occurs after the gate-stack with embedded FE layer has been already formed. In contrast, HZO FE films are more suitable for the gate-last approach, as such an activation anneal will favor the stabilization of the non-FE monoclinic over the FE orthorhombic phase, thus deteriorating the FE properties and the FeFET performance. When it comes to the BEOL FeFETs, HZO is probably the best choice, since BEOL generally requires a lower thermal budget.

Accordingly, the FeFETs reported in literature that were fabricated in a gate-first process, mainly employed the HfO<sub>2</sub> FE layer doped with Si [16, 19, 20, 41]. In contrast, the FeFETs with the HZO FE layer were mainly fabricated in the gate-last process [95–100] as well as in a BEOL module [79, 80]. Interestingly, Liu *et al* [101] reported a non-volatile FeFET containing a 4.2 nm thick pure ZrO<sub>2</sub> FE layer deposited on Ge(100) substrate. Although pure ZrO<sub>2</sub> thin films are known to display antiferroelectric behavior [29], which is generally not suitable for FeFETs as NVM cells, the authors stabilized the FE phase through a compressive strain induced by the Ge substrate. Choi *et al* [102] also reported MFMIS FeFETs where the FE layer was the undoped HfO<sub>2</sub> film. This large variety of hafnia based FE materials

exemplifies the wide range of degrees of freedom that can be adopted for the FeFET fabrication. However, it still remains to be understood, which of the FE compositions is optimal in terms of the key memory parameters such as MW, variability, endurance and retention.

The top metal electrode in HfO<sub>2</sub>-based MFM capacitors and in MFIS FeFETs is usually deposited at low temperatures and before applying the anneal treatment necessary for the FE film crystallization. This mechanical encapsulation is typically done with TiN and is believed to promote the stabilization of the FE orthorhombic phase in HfO<sub>2</sub>. Besides TiN, also other metal nitrides, such as TaN [99, 100], and HfN [97], as well as tungsten (W) [103, 104] have been successfully adopted in FeFETs as top gate electrodes, showing comparable results to the ones in FeFETs with TiN. Moreover, it has been shown that an oxide-type top electrode, such as ITO [102], can help in passivating the defective interface between top electrode and FE, yet providing the necessary capping and conductive electrode function. This result may be of particular importance for controlling the oxygen content in the FE layer, which in turn, may help to alleviate the associated reliability issues, such as wake-up and cycling endurance. The control of the oxygen content is especially critical to undoped FE HfO<sub>2</sub>, which is known to be highly sensitive upon the oxygen stoichiometry [105].

Finally, the IL material mainly adopted for MFIS FeFETs is SiO<sub>2</sub>, due to its excellent interface with Si, good insulating properties, low defectivity and compatibility with HfO<sub>2</sub> films in HKMG CMOS technology. However, when considering the MFIS gate stack and the typical values of the dielectric constants and thicknesses ( $\epsilon_{IL} = 3.9$ ,  $t_{IL} = 1$  nm,  $\epsilon_F = \epsilon_{HfO2} = 25$ ,  $t_F = 10$  nm), it becomes clear from the capacitive voltage divider in figure 6(a) that the voltage drop over the IL ( $V_{IL}$ ) and that over the FE layer ( $V_F$ ) are almost the same for a given  $V_G$ . This has at least three important consequences: (1) the write (PRG or ERS) voltage is inefficiently distributed over the FE, because a large voltage portion is lost on  $V_{IL}$ ; (2) a large  $V_{IL}$  induces an electrical stress onto IL, which leads to its wear out and eventually breakdown under continuous PRG/ERS cycling, as will be discussed in section 4; (3) a large  $V_{IL}$  promotes parasitic charge injection into the gate-stack, undermining the FeFET operation. It has been therefore proposed [87] that an IL with a much higher  $\epsilon_{IL}$  than that of SiO<sub>2</sub> is desirable to alleviate all of these problems. However, the introduction of such a layer imposes severe technological challenges, as it has to fulfill many requirements, including the thermodynamic stability in contact with Si, good electrical interface and large band offset with Si as well as the compatibility with high processing temperatures [106, 107]. This sensibly narrows down the spectrum of possible dielectrics. Nevertheless, there have been improvements in this direction, such as the employment of SiON as the IL [49, 81], which has a slightly higher  $\epsilon_{IL}$  than SiO<sub>2</sub>. Recently, Chan *et al* [108] demonstrated a HZO FeFET with a 1.2 nm thick nitrided aluminum oxide (AlON) as the IL, having the dielectric constant of around 9. This has lead to an enhancement of the MW (figure 9(e)) and of the reliability when compared to the FeFETs with the SiO<sub>2</sub>-based ILs.

### 3.3. Memory arrays

To realize a memory chip, the FeFETs have to be integrated into array architectures. Here, many transistors share the so called word-lines, source-lines and bit-lines connecting their gate, source and drain terminals, respectively. The floating gate flash memory is well known for array arrangements like NAND, common ground NOR, and AND. These can be adopted for FeFETs as well, due to the operational similarity between the two technologies. However, none of the three array configurations is superior in all aspects over the other two: while NAND configuration enables the highest device packing density (with the unit cell size of  $4 F^2$  in the planar flash technology, where  $F$  is the minimum feature size), its sequential read makes the single bit access slow and thus more suitable for data storage. On the other hand, NOR configuration is more than twice as large as NAND ( $10\text{--}12 F^2$ ), but in turn has a fast, random read access, thus being suitable for code storage and execution-in-place. AND configuration can be considered a variant of the NOR, with separate source-lines instead of a common ground, achieving more flexibility for the programming conditions. Depending on the realization of the bit-lines and source-lines (either diffused or metal lines) and their length, it can either be comparable to a common ground NOR (metal lines) or be closer to NAND (diffused lines), both in terms of size and speed. Nevertheless, all three array types have in common that the sharing of array lines leads to inevitable disturbs on unselected cells every time a selected cell undergoes a write/read operation. To contrast them, inhibition programming schemes are applied, among which the so called  $V_{DD}/2$  and  $V_{DD}/3$  schemes are commonly known for FeFETs [109]. In these schemes, unselected cells are exposed to a maximum of half or one third of the nominal write voltage  $V_{DD}$ , respectively. However, despite the inhibition techniques, Ullmann *et al* [109] have suggested that NAND and NOR arrays might not be suitable for FeFETs. In fact, the former present a large read disturb at unselected cells, whereas the latter exhibit large drain-source currents during the PRG/ERS operations because of the asymmetric architecture of the array with respect to the drain and source terminals, thus inducing significant power dissipation and reliability concerns. AND arrays, in turn, minimize the abovementioned problems through their symmetric structure (figure 8(a) shows a  $2 \times 2$  FeFET array), and offer the possibility of random access as well as a bit-wise program and erase operation. For this reason, the HfO<sub>2</sub>-based FeFET arrays have predominantly been studied in an AND arrangement in the last years.

In the works of Müller *et al* [111, 112], the experimental investigation on single HfO<sub>2</sub>-based FeFET cells and passive AND arrays suggested that the  $V_{DD}/3$  scheme is more suitable to inhibit disturbs than the  $V_{DD}/2$  scheme. In fact, with the former, the FeFETs can maintain an  $I_{ON}/I_{OFF} > 10^4$  even after  $10^6$  disturb cycles, whereas the stored state was lost almost after the first cycle with the latter scheme [111]. In 2016, Trentzsch *et al* [19] presented the first active AND arrays that included integrated periphery circuits such as write/read drivers and sense amplifiers. The arrays had the

size of 64 kbit and were fabricated in the 28 nm gate-first HKMG bulk CMOS technology by GLOBALFOUNDRIES. They could show a complete separation of the LVT and HVT states under a variety of data write patterns such as solid, stripe and checkerboard (figures 8(b) and (c)) as well as stable data retention and endurance up to  $10^5$  write cycles. In 2017 followed the demonstration of 32 Mbit arrays in the same technology [20], with PRG/ERS in the nanosecond range, a possibility of direct memory access mode and data retention at 300 °C.

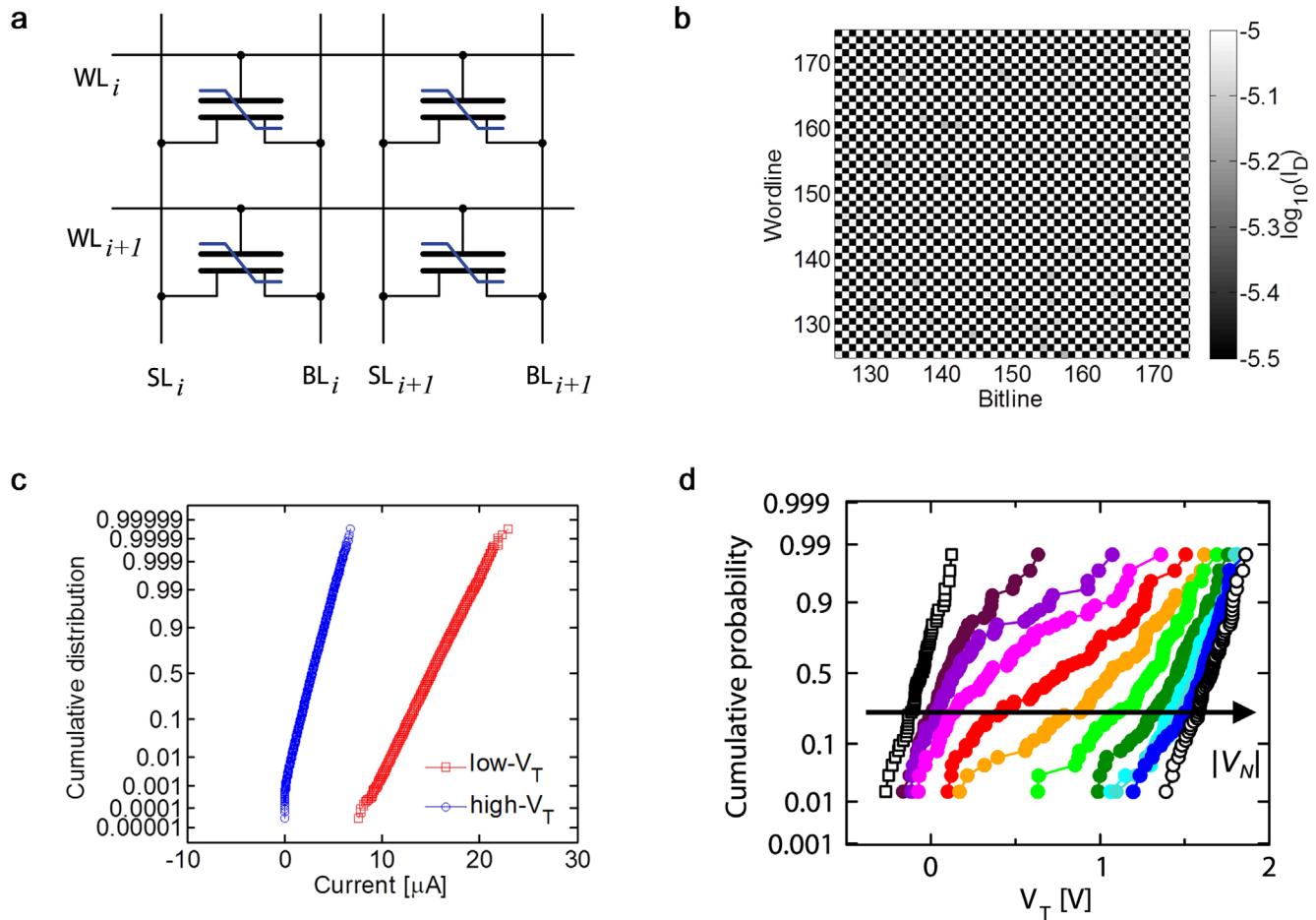
While those reports demonstrated the storage of only two binary states, i.e. LVT and HVT, it is also desirable to achieve multi-level capability in arrays. For this purpose, Mulaosmanovic *et al* [110] studied the partial polarization switching in 63 bit passive AND arrays. They showed that due to the polycrystalline FE film and the related cell-to-cell variations of the present technology, it is challenging to achieve a uniform multi-level  $V_T$  tuning across the array by using a single-shot write pulse of fixed amplitude and duration. Figure 8(d) shows that the intermediate  $V_T$  states, collected for a set of increasing ERS amplitudes, present much broader, non-gaussian and overlapping distributions, when compared to the nominal LVT and HVT. Instead, the authors suggested the adoption of  $V_T$  targeting schemes, such as incremental step program pulse (ISPP) known from the flash technology.

Despite the unfavorable predictions of [109], also NAND FeFET arrays could prove promising functionality. In fact, Zhang *et al* demonstrated 64 kbit NAND arrays with FeFETs based on perovskite SBT films [11]. Also HfO<sub>2</sub>-based FeFET NAND arrays were successfully reported [113]. They started to attract growing attention after the first publication on vertical FeFETs by Florent *et al* appeared [21]. With this device structure, the already existing 3D flash infrastructure may be readily employed to realize high density FeFET arrays.

## 4. Key device performance properties

### 4.1. Memory window and multi-level operation

To achieve a sufficiently large  $I_{ON}/I_{OFF}$  ratio, which is one of the requirements for a fast read-out of the FeFET cell, it is important to have widely separated the LVT and HVT distributions, i.e. a large MW. It follows from equation (1) in section 2 that the MW in MFIS FeFETs is proportional to the FE film thickness  $t_F$  and the coercive field  $E_C$ . However,  $E_C$  in hafnia based ferroelectrics is around 1 MV cm<sup>-1</sup> and appears to be largely invariant over a broad range of process parameters and film thicknesses (5 nm–1 µm) [31, 114]. Thus, to enlarge the MW, the increase of  $t_F$  remains a viable option. Indeed, the trend of increasing MW with  $t_F$  has been experimentally confirmed in FeFETs with  $t_F$  ranging from 5 to 20 nm [81, 115]. The FE film was fabricated by means of atomic layer deposition (ALD) and the maximum MW of around 3 V for  $t_F = 20$  nm was achieved with PRG/ERS pulses of +5V/−5V and duration 1 µs [81]. Figures 9(a)–(d) exemplarily illustrate the FeFETs and the corresponding MW increase when changing  $t_F$  from 10 nm to 20 nm. However,



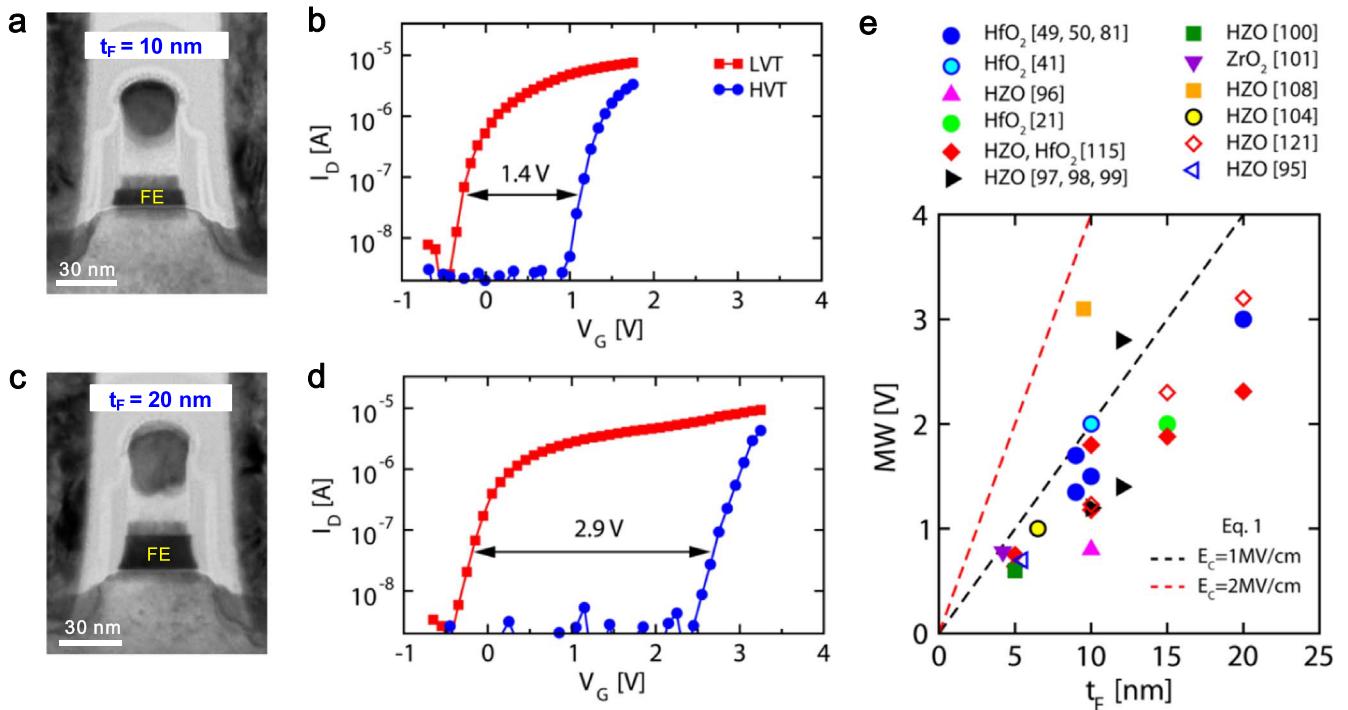
**Figure 8.** (a) Schematic structure of an AND array ( $2 \times 2$  FeFETs). WL, BL and SL indicate word-lines, bit-lines and source-lines, respectively; (b) checkerboard pattern and (c) the complete separation of the normally distributed LVT and HVT states in an active 64 kbit AND FeFET array. © [2017] IEEE. Reprinted, with permission, from [19]; (d) intermediate  $V_T$  states in a passive 63 bit array written with a one-pulse scheme (no target programming). Different colors in the direction of the arrow correspond to different ERS voltages  $V_N$  from  $-2.15$  to  $-3.5$  V in steps of  $150$  mV. Distributions in black are the nominal LVT and HVT. © [2020] IEEE. Reprinted, with permission, from [110].

the experimentally obtained MW progressively deviated from the theoretical one in equation (1) as  $t_F$  increased. This was attributed to the increased fraction of the monoclinic phase due to partial crystallization of the thicker film already during deposition [116], which leads to a significant degradation of FE properties for  $t_F > 20$  nm. To visualize this, figure 9(e) shows the values of MW as a function of  $t_F$  collected across various FeFET demonstrations in literature, and shows that the MW mainly remains below the maximum theoretical value expected from equation (1).

To prevent or alleviate this, at least two strategies can be pursued: (1) introduction of thin interlayers within the  $\text{HfO}_2$  and (2) adoption of other deposition techniques. Kim *et al* [117] demonstrated that the introduction of thin  $\text{Al}_2\text{O}_3$  interlayers within the FE film suppresses the continuous growth of grains and increases the amount of the orthorhombic FE phase in capacitor structures, preserving the good hysteresis up to  $t_F = 40$  nm. However, this results in an increase of the total coercive voltage and would consequently result in an increase of the switching voltage in FeFETs. In fact, there have been reports on such FeFETs, where thin

$\text{Al}_2\text{O}_3$  interlayers were used to separate blocks of single 5 nm thin FE layers, building in this way laminated FE structures in the gate stack [121]. In this way, a maximum MW of 3.2 V with four laminated HZO films was achieved, thus corresponding to a total  $t_F = 20$  nm. Nevertheless, this came at the expense of using +12 V/-12 V pulses for PRG/ERS operations, which is more than double of those adopted for FeFETs with a single FE layer of comparable  $t_F$  and MW [81]. The second strategy is to adopt other deposition techniques, for which no considerable degradation of FE properties occurs for increased  $t_F$ . For example, sputtering pure  $\text{HfO}_2$  by physical vapor deposition (PVD) [105] was shown to be an effective way in producing stable FE films with high remanent polarization over a wide thickness range (10–50 nm). Recently, chemical solution deposition [118, 119] and pulsed laser deposition (PLD) [31] proved to be advantageous for thicknesses beyond 100 nm, reaching even  $t_F = 1 \mu\text{m}$ , as reported in [31, 119].

An additional advantage of a large MW is the enhanced ability to store more than 1 bit of data per cell. This allows an increase in effective bit density without decreasing the feature



**Figure 9.** MW as a function of thickness of the FE layer ( $t_F$ ): cross-section TEM images of 28 nm HKMG bulk FeFETs and the respective  $I_D-V_G$  curves for the LVT and HVT states with (a), (b)  $t_F = 10$  nm [50] and (c), (d)  $t_F = 20$  nm [81]; © [2019] IEEE. Reprinted, with permission, from [81]. (e) Collection of the MW values reported across the literature for MFIS FeFETs and plotted as a function of  $t_F$  for different variants of hafnia and zirconia based FE materials. The dashed lines indicate the maximum theoretical value expected from equation (1) for  $E_C = 1$  and 2 MV cm<sup>-1</sup>.

size, as is commonly done for MLC (Multi-Level Cell) flash. For reliable MLC operation, several prerequisites have to be fulfilled, such as enough memory window between any two states as well as the steady retention over time, stable cycling endurance, good uniformity and immunity to disturbs for each state. Mulaosmanovic *et al* [18] first demonstrated the MLC capability in scaled Si doped  $\text{HfO}_2$  based FeFETs, showing that it is possible to program the device into intermediate  $V_T$  states, which had a low cycle-to-cycle variation and the same cycling endurance and data retention as the nominal LVT and HVT, i.e.  $10^5$  cycles and the extracted 10 years retention, respectively. It should be noticed that this was demonstrated on ultra-scaled devices ( $W = 80$  nm,  $L = 30$  nm), which are known to have abrupt switching and a lower number of intermediate  $V_T$  states. Obviously, by increasing the FeFET area, many intermediate states can be captured, as discussed in section 2.3. For example, Zeng *et al* [120] demonstrated a 2 bit/cell FeFET, having dimensions of  $W = 100$   $\mu\text{m}$  and  $L = 10$   $\mu\text{m}$ , which shows stable retention of the 4 states and clear separation up to 500 PRG/ERS cycles. Similarly, Ali *et al* [121] reported a 3 bit/cell in FeFETs with laminated FE layers. Most recently, there have been reports on FeFETs with 9- to 10-nm-thick FE layer having more than 10 stable  $V_T$  states [52, 80], which not only are attractive for MLC purposes but also for neuromorphic devices.

Nevertheless, several limitations of the MLC capability in FeFETs have to be considered. First, as previously discussed in section 2.3, the lateral size scaling, which is desirable for high density integration, leads to a considerable

or even complete loss of intermediate  $V_T$  states, and to an abrupt switching between the LVT and HVT, as demonstrated for ultra-scaled devices (FeFETs with  $L < 40$  nm) in our previous reports [50]. This is attributed to a decrease of the number of switchable FE domains in the gate stack upon scaling, thus to a decreasing gate size/domain size ratio [50]. One way to overcome this limitation without penalizing the integration density is to adopt advanced integration geometries for FeFETs, such FinFET, GAA or vertical 3D FeFETs, which intrinsically offer a larger area of the FE layer, thus larger gate size/domain size ratio. In addition, grain/domain size engineering will be helpful and is shown to be possible in hafnia-based ferroelectrics [117, 122, 123]. A second issue is the poor cell-to-cell uniformity of the intermediate  $V_T$  states even among large-area FeFETs, which is mainly due to the polycrystalline nature of the FE film. As discussed in section 3.3, this is evident already in small mini-arrays of 63 FeFETs [110] and can probably be overcome by further material improvements as well as adoption of suitable target programming schemes, like ISPP.

#### 4.2. Retention

The ability to retain the stored data over a long time, usually specified as 10 years at some elevated temperature, is a critical requirement to any nonvolatile memory technology. The retention loss in FeFETs is generally attributed to two factors: depolarization field  $E_{dep}$  and parasitic charge trapping [124].  $E_{dep}$  originates from an incomplete compensation of the

polarization charge in the FE layer by the confining non FE layers [125]. While in MFM capacitors the top and bottom metal electrodes provide sufficient charge compensation, thus having ideally  $E_{dep} = 0$ , the MFIS stack in FeFETs is always affected by a finite  $E_{dep}$ , even when no external voltages are applied ( $V_G = 0$  V). This occurs because of the finite dielectric constant of the IL and the semiconductor, and the resulting incomplete compensation of the polarization charge. Unfortunately,  $E_{dep}$  is always pointing in the direction of reducing the polarization in the FE and tends to diminish the memory retention time. It is therefore important to consider the relation of  $E_{dep}$  to the coercive field  $E_C$  for a given FE material: if  $E_{dep}/E_C \gg 1$ , the FE will experience a significant retention loss, whereas if  $E_{dep}$  is comparable or smaller than  $E_C$ , little loss would be expected. Gong and Ma [126] showed that a HfO<sub>2</sub> FE layer in a typical MFIS FeFET presents comparable  $E_{dep}$  and  $E_C$  values, whereas the perovskite FE films, like PZT or SBT, show a much higher  $E_{dep}/E_C$ . This is mainly due to the ten times higher  $E_C$  in HfO<sub>2</sub> as compared to PZT or SBT, which ensures a good retention for the former and very rapid retention loss for the latter materials.

Indeed, stable data retention has been shown in a large number of publications dealing with HfO<sub>2</sub>-based FeFETs [16, 18, 82, 95, 96, 99, 120], both at room and elevated temperatures. A commonly used method to estimate the retention capability is to extrapolate the  $I_{ON}/I_{OFF}$  ratio or the MW after 10 years time, which usually shows enough read margin for the distinction of the two logic states. Nevertheless, a realistic and reliable estimation should be performed by collecting statistical retention data on large memory arrays, at different temperatures to extract activation energies and, in particular, by understanding the rapidly failing tail bits. Steps in this direction have been recently made, where retention studies on a larger number of cells and in memory arrays at 125 °C [51], 250 °C [19] and 300 °C [20] have been shown. However, as monitoring the stored states over time and at various temperatures can be a time consuming and expensive process, a method for rapid retention assessment would be desirable. Recently, one such method has been proposed [51], which is based on the time-voltage switching kinetics in the FeFET (section 2.2) and the associated graphical representation in figure 3(c). In fact, by extending the fitting curve and extrapolating the switching time at  $V_G = 0$  V, which corresponds to the retention conditions, provides an estimate of the retention loss over time caused by  $E_{dep}$ . The method can be particularly useful for a fast retention screening between different FeFET fabrication processes.

Finally, many other phenomena potentially impacting data retention in FeFETs are less explored and remain to be understood, including the ferroelectric imprint, the role of parasitic charge injection and trapping as well the effect of extended write cycling. The latter is also commonly known as post-cycling retention and indicates the situation where many types of nonvolatile memories experience a degradation of data retention capability after they have been intensively cycled. In addition, ferroelectric imprint is a phenomenon that causes a shift of the  $P$ - $E$  hysteresis along the  $E$ -axis, making it asymmetric and favoring the stability of one  $P$  state over the

other [127]. It typically occurs when the FE material is kept in a defined  $P$  state for a longer time and is enhanced at elevated temperatures. It is obvious that imprint may stabilize the retention of the stored state, but make difficult the switching to the opposite state and can severely impair its retention. Clearly, this topic is essential to the FeFET reliability and will probably require similar imprint studies to the ones performed on HfO<sub>2</sub>-based MFM structures [128, 129].

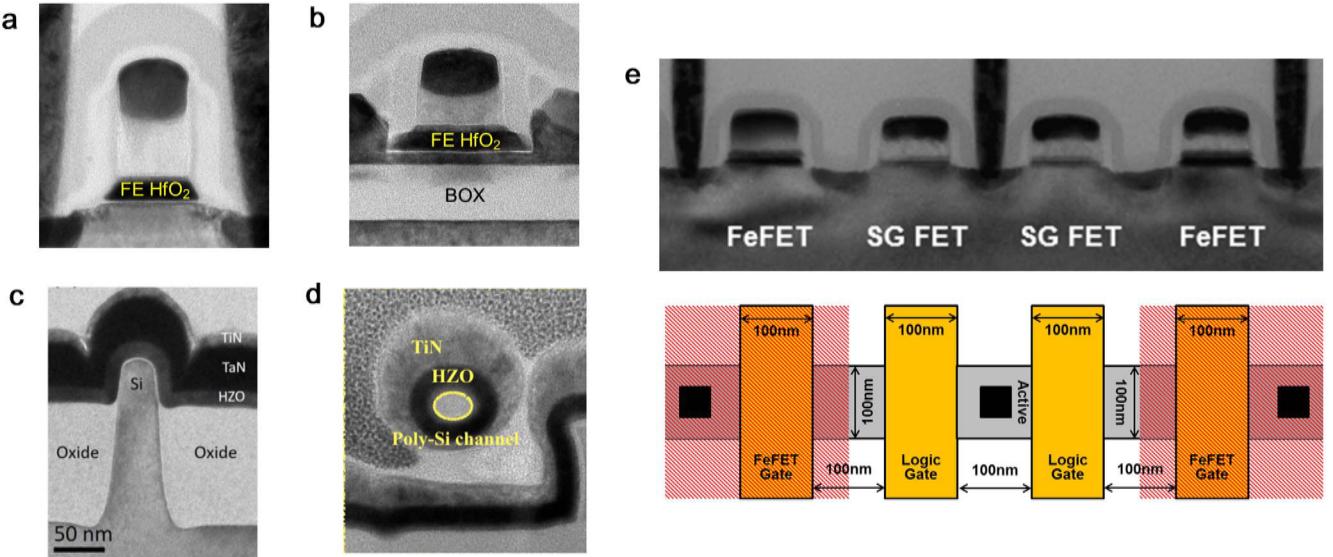
#### 4.3. Endurance

On the one hand, the large  $E_C$  in HfO<sub>2</sub> brings benefits in terms of stable data retention. On the other hand, it appears to be detrimental to the write cycling endurance. In fact, by considering the conservation of the electric displacement field in the MFIS gate stack, it follows:

$$D = \varepsilon_0 \varepsilon_F E_F + P_S = \varepsilon_0 \varepsilon_{IL} E_{IL}, \quad (3)$$

where  $\varepsilon_0$  is the vacuum permittivity,  $\varepsilon_F$  and  $\varepsilon_{IL}$  are dielectric constants of the FE and IL, respectively,  $E_F$  and  $E_{IL}$  are electric fields in the FE and IL, respectively, and  $P_S$  is the spontaneous polarization. If we, for simplicity, assume that the FE layer has  $E_F = E_C = 1$  MV cm<sup>-1</sup> at the moment of switching, and take the typical values, such as  $\varepsilon_{IL} = 3.9$ ,  $\varepsilon_F = \varepsilon_{HfO_2} = 25$ , we find that  $E_{IL} > 20$  MV cm<sup>-1</sup> for  $P_S > 5$  μC cm<sup>-2</sup>. Such a high electric field over a prolonged number of PRG/ERS cycles will inevitably induce degradation of the IL. In addition, large  $E_{IL}$  forces a severe band bending of the IL, as schematically depicted in figures 6(b)–(c) in section 2.5, which promotes the injection of electrons and holes in the gate stack during PRG and ERS operations, respectively. In fact, Yurchuk *et al* [62, 130] have shown that such a steady charge transfer through the IL under alternating PRG/ERS pulses leads to the interface wear out, and the consequent increase of the trap density. This progressively facilitates the permanent trapping of injected charges in the gate stack, which at the same time hinder the switching of FE domains and screen the effect of the FE polarization onto channel. As a result, the MW closes after  $10^4$ – $10^5$  bipolar write cycles. These are the typical endurance values reported by different research groups, which were collected on single devices and larger memory arrays. Yurchuk *et al* [130] concluded that the endurance failure is therefore caused by the degradation of the IL rather than of the FE layer itself. Indeed, it is known from the past studies [131] on MFM capacitors that FE HfO<sub>2</sub> can withstand more than  $10^{11}$  write cycles before a significant degradation sets in, confirming the former conclusion. Gong and Ma [132] also found that charge trapping and trap generation both contribute to the endurance failure in FeFETs, and suggested that the former phenomenon induces a  $V_T$  shift in the  $I_D$ – $V_G$  curves, whereas the latter one is responsible for the slope degradation of the curves.

To extend the number of write cycles, several strategies have been proposed, aiming either at preventing the IL degradation [87] or at mitigating/removing the post-cycling degradation effects [133]. Müller *et al* [87] suggested the following: (1) tailoring the FE polarization; (2) operating in sub-loop FE regime; and (3) tailoring the capacitive divider in figure 6(a). Regarding the FE polarization tailoring, it is clear



**Figure 10.** Scaling and advanced integration of FeFETs: (a) 28 nm bulk HKMG. © [2016] IEEE. Reprinted, with permission, from [19]; (b) 22 nm FDSOI. © [2017] IEEE. Reprinted, with permission, from [20]; (c) FinFET [138]; (d) gate-all-around (GAA). © [2020] IEEE. Reprinted, with permission, from [89]; (e) Co-integration of FeFETs and logic FETs on the same active area with 100 nm gate-to-gate distance. © [2020] IEEE. Reprinted, with permission, from [139]. It should be noted that (c) and (d) are relative to the NC-FET applications, but the integration of the FE layer is in principle similar for FeFETs as well.

from equation (3) that  $E_{IL}$  monotonically increases with  $P_S$ , which means that larger polarization is detrimental to the IL reliability and enhances charge trapping [62]. A decrease of  $P_S$  and/or control of the polarization axis via texture engineering could be helpful solutions [134]. When it comes to the capacitive divider, the goal is to tailor the material composition and/or the geometry of the stack in order to maximize the voltage drop over the FE, while minimizing the unnecessary drop over the IL. This not only will improve the write efficiency, but also enhance the IL reliability. As briefly discussed in section 3, this can be, for example, achieved by using an IL with a higher dielectric constant than that of SiO<sub>2</sub>. Although this is challenging, first promising reports on using AlON as the IL are already available [108]. Another viable direction is to adopt such gate stack geometries that match the capacitive divider in a way to minimize the  $E$  field across the IL. A typical example is the MFMIS FeFET with its tunable areal ratio  $S_F/S_I$ , as introduced in section 3.1. This strategy may be done on planar structures as well as 3D realizations, such as recess-gate structures [87], where  $S_F$  and  $S_I$  can be nearly independently tuned. Also MFIS recess-gate FeFETs may be beneficial in the same manner, as argued in [88].

Mulaosmanovic *et al* [133] proposed thermal treatments to extend the endurance. They demonstrated that by taking a device that experienced the post-cycling endurance failure (i.e. MW closure after  $10^5$  cycles) and by baking it at 300 °C for 2 h, a full recovery of the MW could be achieved. As this has limited practical utilization, they also showed that the same recovery, with a renewed  $10^5$ -cycling capability, can be also electrically achieved. This is obtained by inducing a considerable Joule heating in the FeFET channel region by means of intentionally large drain/source to body junction current. The result was explained by thermal healing of the

cycling induced damage in the IL, a phenomenon also known for other types of logic and memory devices [135].

Recently, HZO-based FeFETs enduring more than  $10^7$  to  $10^8$  write cycles have been reported [95, 104]. Although the origin of the improvement is still not completely investigated, lower post-metallization annealing temperatures ( $\leq 500$  °C) adopted for the crystallization of the FE HZO might be one explanation. In fact, it has been recently shown that reduced annealing temperatures lead to an improved interface (IL) quality [136], which, in turn, might enhance the cycling endurance.

#### 4.4. Scaling and variability

HfO<sub>2</sub>-based FeFETs have shown a remarkable scaling capability, as also exemplified by the timeline in figure 1 and by some recent integration examples in figure 10. The reasons are at least twofold: (1) HfO<sub>2</sub> films maintain their ferroelectricity even at aggressive vertical and lateral scaling, (2) availability of different yet mature deposition methods that allow for planar but also conformal 3D deposition of HfO<sub>2</sub> without impairing the FE properties. The former has led to demonstration of ultra-scaled FeFETs in the planar 28 nm HKMG bulk technology (figure 10(a)), having devices with lowest dimensions of  $W = 80$  nm and  $L = 30$  nm [50], which not only display excellent switching and large MW ( $>1.5$  V), but are also capable of multi-level storage [18]. Spurred on this advancement, a successful integration in 22 nm FDSOI followed (figure 10(b)) [20], reaching a device size of as low as  $W = 80$  nm,  $L = 20$  nm, which newly displayed a MW as large as 2 V for  $t_F = 10$  nm [41]. A further advantage of the latter technology is the presence of the back bias, which enables a  $V_T$  tuning independent of the ferroelectric field-effect [137].

On the other hand, the possibility of conformal 3D deposition of FE  $\text{HfO}_2$  films is very attractive and has in the past allowed the fabrication of 3D vertical deep trench capacitors with Al doped  $\text{HfO}_2$  thin films [140], reaching the aspect ratio of 13:1 and opening the avenue for high density 1T-1C FeRAM applications. Moreover, these assets are responsible for the recent demonstration of 3D vertical FeFETs [21], but also nanowire FeFETs [86, 104], as well as FinFETs [138, 141, 142] and GAA devices [89, 143] with embedded FE  $\text{HfO}_2/\text{HZO}$  (figures 10(c), (d)). The vast adoption of  $\text{HfO}_2$  films for conventional HKMG transistors and the dedicated integration know-how have recently facilitated the co-integration of FeFETs with logic transistors (figure 10(e)), sharing the same active area and having the gate-to-gate distance of only 100 nm [22]. This represents an appealing milestone for embedded NVM solutions but also novel computing concepts, such as logic-in-memory and neuromorphic hardware, where a fine-grained co-integration with conventional CMOS device is required [23]. It can be therefore concluded that the FE  $\text{HfO}_2$  can follow the most advanced integration schemes in the semiconductor industry.

Nevertheless, device scaling poses certain limits, especially when it comes to variability. While large-area FeFETs usually present uniform behavior of the two saturated states, as exemplified in figure 8(c) by the normal and tail-free distributions of 64 kbit arrays with device size  $W = L = 500$  nm, the scaled devices can display a significant device-to-device and cycle-to-cycle variability. At least three causes have been identified for this: (1) granularity of the FE layer [50]; (2) intrinsic stochasticity of the FE switching [50], (3) presence of non-FE grains in the FE layer [144]. Regarding the granularity, the FE  $\text{HfO}_2$  films adopted in FeFETs are mainly polycrystalline, and therefore consist of many grains, which are characterized by a random orientation of the polarization axis. As shown in section 2.3, the device scaling causes to hit the granularity limits of the film, especially when the gate (channel) size becomes comparable to the grain (domain) size. In this scenario, it is clear that the different  $P$  axis orientations and slightly different number of grains in the gate stack, both of which cannot be reliably controlled in the present technology, will contribute in increasing the device-to-device variability. In fact, it has been shown [50] that devices with  $W = 80$  nm and  $L = 30$  nm, which went through the same process on the same wafer, exhibit discrete  $V_T$  switching events, attributed to the reversal of single FE domains (figure 4), that however largely differ in switching voltages and number of switching events from device to device. This becomes obvious when comparing figures 4(b) and (d). Regarding the stochasticity, since the switching in scaled device involves only a countable number of domains, also intrinsically stochastic nature of FE switching emerges (figure 4). It has been found that this randomness can be modeled by a Poissonian statistics [50], and experimentally verified that the standard deviation of the switching time  $t_s$  can even extend over one decade around the mean  $t_s$ , which is responsible for a significant intra-device variability. Finally, a portion of the film may have dielectric, non FE grains. Liu and Su [144] have shown through simulations that, due to the

random mixture of dielectric and FE grains in the  $\text{HfO}_2$  film, the FeFET scaling substantially enhances the probability of forming paths of dielectric grains only between source and drain, which in turn considerably increases the MW fluctuations. To mitigate this, the authors suggested a reduction of the grain size. Therefore, strategies for increasing the spatial and switching uniformity of the FE film are needed to enable a variability-free scaling, and dedicated approaches such as epitaxial growth, texture control and grain size engineering are already starting to show promising results [117, 121, 134, 145, 146]. Moreover, as detailed in [56], electrical parameters have to be chosen such to avoid the stochastic switching, which is an intrinsic material property and might be hardly eliminated. For example, sufficiently long and/or sufficiently high amplitude pulses need to be applied during write to ensure deterministic switching, or in other words, pulse parameters ensuring that the switching probability is always  $P = 1$  for a given probability curve in figure 4(e).

Finally, variability sources other than those related to the FE film and its switching can play a critical role. For example, according to figure 9(e), the thickness of the FE  $\text{HfO}_2$  film has to be  $t_F > 7$  nm to achieve a reasonable MW, resulting in an equivalent oxide thickness (EOT) of at least 25 Å for the MFIS stack. This can enhance the short-channel effects with respect to conventional (non-FE)  $\text{HfO}_2$ -based MOSFETs. Furthermore, other variability factors such as metal gate work function variations, random dopant fluctuations and various interface roughness profiles should be taken into consideration as well [147].

## 5. Potential applications

### 5.1. Memory

The most obvious and historically supported application of FeFETs is to nonvolatile memory. Particularly attractive are embedded NVM solutions (e.g. alternative to embedded flash), especially given the recently demonstrated co-integration of FeFETs with logic devices in close proximity and on the same active area, as discussed in section 4 and shown in figure 10(e). In addition, the AND arrays and the dedicated positive source drain erase scheme [113] may enable the truly random access, thus increasing the speed and versatility of this type of memory. Moreover, the vertical FeFET integration may open the avenue for 3D NAND-like structures, with the advantage of exploiting the already existing knowledge and infrastructure of the flash technology. As many of the memory related parameters and concepts have been already discussed throughout this review, we will not further elaborate this topic but, instead, we provide a representative comparison of state-of-the-art FeFET technology with other NVM concepts in table 1. In many aspects, the FeFET matches or approaches the metrics of the flash cells, as is expected from the mutual structural and operational similarity. Nevertheless, the low power and fast write operation

**Table 1.** Benchmarking of various NVM technologies.

	NAND flash	NOR flash	PCM	RRAM	STT-MRAM	HfO <sub>2</sub> FRAM	HfO <sub>2</sub> FeFET
Cell concept	1T	1T	1T-1R	1T-1R	1T-1R	1T-1C	1T
Write voltage	>10 V	>10 V	<3 V	<3 V	<2 V	<3 V	<5 V
Write speed	<10 ms	<10 ms	<100 ns	<10 ns	<10 ns	<100 ns	<10 ns
$I_{ON}/I_{OFF}$ ratio	>10 <sup>8</sup>	>10 <sup>8</sup>	>10 <sup>4</sup>	>10 <sup>3</sup>	>2	>2	>10 <sup>8</sup>
Endurance	<10 <sup>5</sup>	<10 <sup>6</sup>	>10 <sup>10</sup>	>10 <sup>12</sup>	>10 <sup>15</sup>	>10 <sup>11</sup>	<10 <sup>8</sup>
Retention	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y	>10 y
Multibit	4	2	2	2	1	1	2-3
3D integration	yes	no	yes	yes	no	no	yes
References	[148]	[149]	[150]	[151]	[152]	[153]	This work

\*Notes: the values are only representative and taken mainly from single device structures, from the indicated references and references therein.

**Table 2.** Benchmarking of FeFETs using various FE material systems.

FE type	Perovskite	Organic polymer	2D material	III-V nitride	Fluorite-structure
Typical materials	SBT, PZT, PTO	P(VDF-TrFE)	CuInP <sub>2</sub> S <sub>6</sub>	Al <sub>1-x</sub> Sc <sub>x</sub> N	X:HfO <sub>2</sub> , HZO
Deposition	PLD, MOCVD	Spin coating	Exfoliation, PVD, CVD	Reactive sputtering	ALD, PVD
$\varepsilon_F$	150–1300	10–15	40–60	10–16	~30
$P_R$	2–40 $\mu\text{C cm}^{-2}$	<13 $\mu\text{C cm}^{-2}$	~4 $\mu\text{C cm}^{-2}$	100–140 $\mu\text{C cm}^{-2}$	10–40 $\mu\text{C cm}^{-2}$
$E_C$	10–100 kV cm <sup>-1</sup>	~500 kV cm <sup>-1</sup>	~300 kV cm <sup>-1</sup>	2–6 MV cm <sup>-1</sup>	1–2 MV cm <sup>-1</sup>
$t_F^a$	>100 nm	>200 nm	87–400 nm	100 nm	5–20 nm
Switching voltage	<9 V	10–60 V	<10 V	>50 V	<5 V
Memory window	1–4 V	10–20 V	3–4 V	~35 V	1.5–3.5 V
Endurance	>10 <sup>12</sup>	<10 <sup>4</sup>	10 <sup>4</sup>	~10 <sup>4</sup>	<10 <sup>8</sup>
Retention	>10 <sup>6</sup> s	>10 <sup>4</sup> s	>10 <sup>4</sup> s	~10 <sup>5</sup> s	>10 <sup>6</sup> s
Min. channel length	85 nm	>5 $\mu\text{m}$	1 $\mu\text{m}$	>3 $\mu\text{m}$	22 nm
CMOS friendly <sup>b</sup>	No	No	No	No	Yes
References	[8, 13, 161]	[154, 155]	[156, 162, 163]	[158, 164, 165]	This work

<sup>a</sup> Refers to the values reported in FeFET devices. In general, the respective materials may show ferroelectricity over a much broader  $t_F$  range.

<sup>b</sup> Compatibility with CMOS Front-End-of-Line (FEoL) module.

† Notes: the values in this table are taken from the indicated references and references therein.

makes it advantageous with respect to flash and rather comparable with other emerging NVM.

Although this article deals only with FeFETs based on FE HfO<sub>2</sub>, devices made from other FE materials are currently being under intense consideration as well, including materials such as perovskite oxides [13], organic polymers (e.g. poly-vinylidene fluoride and its derivative P(VDF-TrFE)) [154, 155], 2D ferroelectrics (e.g. CuInP<sub>2</sub>S<sub>6</sub> and  $\alpha$ -In<sub>2</sub>Se<sub>3</sub>) [156, 157] and III-V nitrides (e.g. Al<sub>1-x</sub>Sc<sub>x</sub>N) [158]. Table 2 provides an exemplary comparison between some of the most prominent FE properties of these materials as well as the respective key FeFET parameters. For simplicity, only the most representative materials for each FE system are considered. As previously discussed, HfO<sub>2</sub> based FeFETs present several advantages (FEoL CMOS compatibility, aggressive scaling, low-voltage operation and steady data retention). Nevertheless, other FE materials display peculiar properties that may be valuable in specific FeFET applications, for which HfO<sub>2</sub> is probably not the best choice. For example, organic FE materials have the merit of mechanical flexibility as well as low-cost and large-scale deposition on rigid but also bendable and rollable substrates. This makes them suitable for flexible NVM solutions for functional electronics

[154]. Furthermore, the emerging 2D FE materials offer merits like remarkable thickness scaling (down to atomic-scale monolayers), absence of dangling bonds, flexibility and band-gap tunability [156]. Interestingly, 2D ferroelectrics not only can be adopted as FE insulators within the gate stack (i.e. interposed between the gate electrode and the semiconductor substrate, as depicted in figure 7), but can also have semiconducting properties.  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> is one such 2D FE semiconductor [159] that has recently been used to demonstrate the so called ferroelectric semiconductor FET (FeS-FET) [160], where  $\alpha$ -In<sub>2</sub>Se<sub>3</sub> is employed as the channel material while the gate insulator is the dielectric. However, further research is necessary to assess the full reach of 2D FE materials in terms of integration and performance in FeFET devices.

Finally, it should be also mentioned, that besides NVM applications, there have been also proposals for volatile 1T DRAM-like concepts. Cheng and Chin [166] showed a FeFET having the TaN/30 nm HZO/3 nm SiO<sub>2</sub>/Si gate stack, which exhibited data retention of only a few seconds, probably due to large depolarization effects. The  $I_{ON}/I_{OFF}$  read window of 10<sup>3</sup> could be achieved after 10 s of retention at 25 °C, whereas the device had a very low DC leakage and

endured more than  $10^{12}$  cycles of  $+4V/-4V$  and 5 ns write pulses. This makes it an excellent candidate for fast and high density DRAM, because it does not require a storage capacitor, i.e. it belongs to the class of capacitor-less DRAM concepts [167–169].

### 5.2. Neuromorphic computing

Neuromorphic computing aims at overcoming the performance limitations of the present-day computer architectures and draws inspiration (directly or remotely) from the organization and function of the human brain. As such, the main building blocks to reproduce in a neuromorphic system are neurons and their interconnections, called synapses (figure 11(a)). NVM elements have been recognized as suitable candidates for the neuromorphic hardware, due to their rich physical properties and switching behaviors as well as high-density integration and connectivity [170].

FeFETs based on perovskite materials have already been proposed for such applications, including artificial neurons [172, 173], synapses [174, 175] and small neural networks [176, 177]. In 2017, a first demonstration of the artificial synapse was made with HfO<sub>2</sub>-based FeFETs [171], which were fabricated in the 28 nm HKMG bulk technology. The control of the partial polarization switching and the resulting gradual tuning of the transistor's conductivity (i.e. of the  $V_T$ ), as depicted in figures 11(b) and (d)–(f), made it possible to emulate analog synaptic weights and the processes of synaptic potentiation and depression. The authors also implemented the basic learning rule called spike timing dependent plasticity (STDP) and showed the possibility of weighted signal transmission in such synapses (figure 11(c)). The significant advantage of FeFETs is that both ERS and PRG transitions can be made very gradual, under various pulsing schemes. For example, figures 11(d)–(f) show that more than 64 intermediate  $V_T$  levels can be achieved with three different pulsing schemes (incremental pulse amplitude, incremental pulse width and incremental number of identical pulses). This is unlike many other synaptic proposals based on emerging memory devices [170], which typically have only one gradual transition, whereas the other is abrupt (e.g. the reset in phase change memories [178] or the set in filamentary resistive-switching memories [179]). The works following the synapse demonstration in [171] made several proposals for FeFETs as analog weights suitable for deep neural networks, including the devices realized in the planar gate-last [180], junctionless [142], nanowire [85] and BEOL [80] technology. However, as mentioned in the previous section, the device scaling may lead to binary (digital) and stochastic switching in FeFETs [50], resulting in a rapid loss of the analog conductance tuning. This may, in turn, require the adoption of other device geometries/modules, such as 3D FeFETs or BEOL FeFETs [80], where the device dimensions can be relaxed, providing a sufficient number of switchable domains in the gate-stack and thus, the multilevel behavior. Alternatively, other operational schemes may be necessary, e.g. multilevel synaptic weights could be represented by a number of binary switching

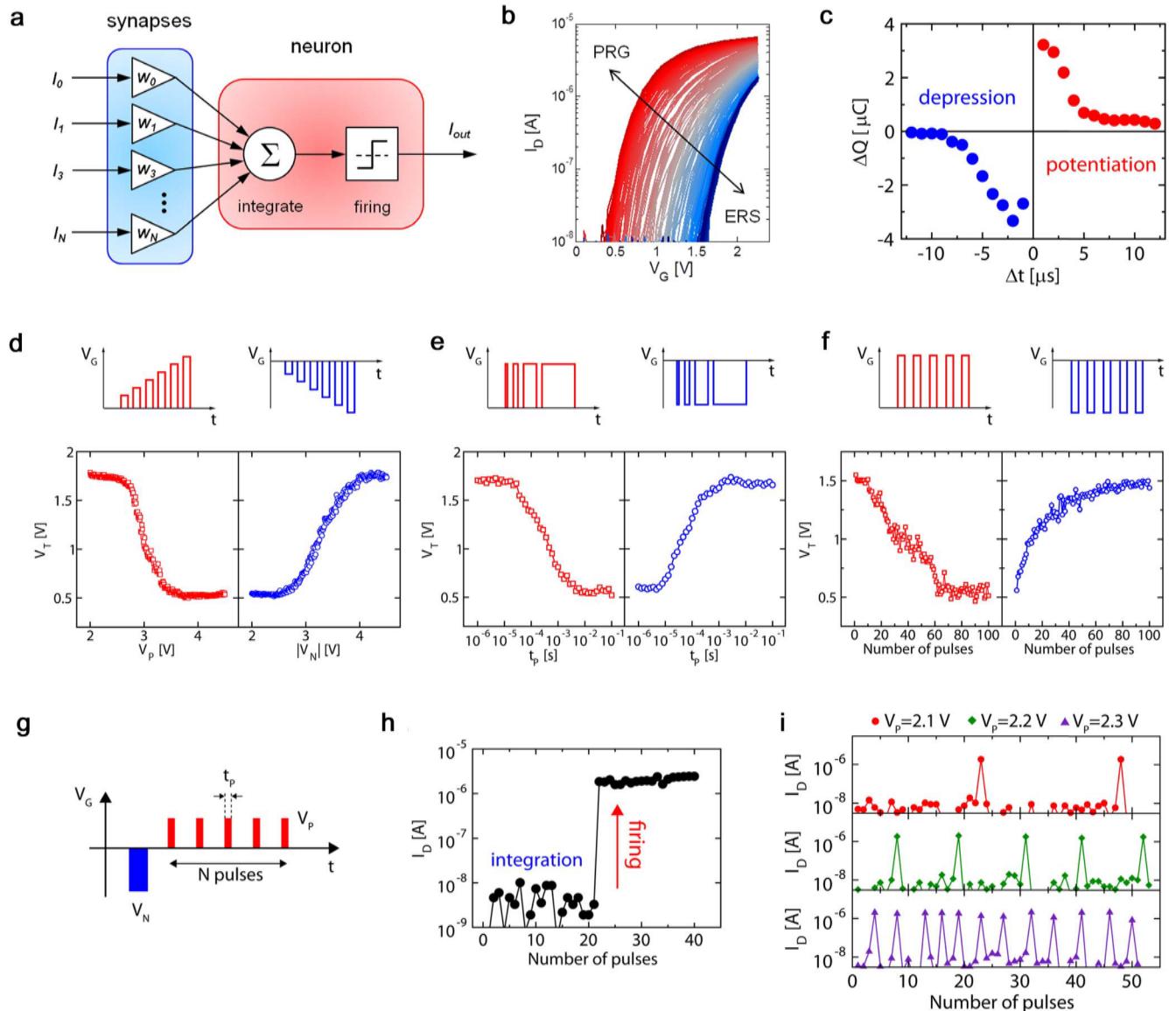
FeFETs connected in parallel and programmed in a stochastic way [181].

Also artificial neurons have been recently implemented with FeFETs [27, 182–184]. Mulaosmanovic *et al* [27] proposed the use of a single ultra-scaled FeFET to emulate the key neuronal behaviors. In fact, they exploited the AS and the resulting abrupt switching transitions typical for scaled devices (section 2) to implement the integrate-and-fire functionality (figures 11(g) and (h)), which resulted in a biologically plausible all-or-nothing spiking. Thanks to the time-voltage dependence of AS, the authors could also show the spiking frequency tuning (the stronger the neuronal excitation, the higher the spiking frequency) as shown in figure 11(i), and the possibility for setting the arbitrary refractory period and achieving 'leaky' integrate-and-fire behavior. The advantage of the FeFET-based neuron is that the incoming action potentials are integrated directly within the FE layer in the gate stack, so that no external integration capacitor is needed, making this a compact capacitor-less solution, unlike typical CMOS neurons [185]. Moreover, because of the all-or-nothing spiking, low static power consumption is expected during the spike integration stage. In addition, the intrinsic switching stochasticity in FeFETs can be exploited to mimic the firing randomness of the biological neurons [186].

The possibility to emulate both synapses and neurons and the easiness of the device integration in CMOS compatible environments, makes therefore FeFETs perfect candidates for large-scale all-ferroelectric neural networks. Table 3 provides a benchmarking summary of state-of-the-art embedded flash (eFLASH) and FeFET technologies with regard to neuromorphic computing, evidencing similarities but also significant advantages of FeFETs.

### 5.3. In-memory computing

Conventional computing based on the von-Neumann architecture is reaching its limits in terms of power consumption and data throughput. Two main factors responsible for this are the von-Neumann bottleneck [187] and the memory wall [188]. The former is specific for the von-Neumann architecture and arises because data and code are transferred sequentially by the same data bus. The latter is independent of the computational architecture, and indicates that over the last decades the access time of the memory unit has increased at a much slower pace than the processing speed of the logic unit. One approach to circumvent these issues is to integrate logic functionality into memory arrays, i.e. to merge logic and memory. Already in 1970, Stone proposed a 'Logic-in-Memory' (LiM) computer where each memory element had associated combinational logic [189]. In the last years, non-volatile memory devices have given the development of LiM new impetus, as those devices promise to dramatically decrease the power consumption [190]. In particular, HfO<sub>2</sub>-based FeFETs appear very attractive, because they reduce sneak-path currents due to the high  $I_{ON}/I_{OFF} (>10^6)$  [19] without requiring additional access transistors. Besides LiM, FeFETs can be also integrated into logic circuits to



**Figure 11.** FeFETs for neuromorphic hardware: (a) sketch of the basic neuromorphic building blocks; (b) continuous tuning of the  $I_D$ - $V_G$  curves. © [2020] IEEE. Reprinted, with permission, from [28]; (c) Experimental demonstration of STDP with a FeFET-synapse. © [2017] IEEE. Reprinted, with permission, from [171]; continuous  $V_T$  tuning for both PRG and ERS transitions under (d) incremental pulse amplitude; (e) incremental pulse width and (f) identical pulses; (g) The  $V_G$  waveform and (h) the resulting integrate-and-fire behavior of a scaled device [27]; (i) spiking frequency tuning of a FeFET-neuron through the time-voltage trade-off of the accumulative switching [27]. (g)-(i) are reproduced from [27] with permission from the Royal Society of Chemistry.

embed storage into classically volatile structures. To distinguish them from LiM, these are sometimes called NVL circuits. Here, FeFETs replace some of the conventional (volatile) MOSFETs and can store either the input values or the output results of a computation [191, 192]. Moreover, two different readout schemes have emerged, regardless whether the FeFETs are employed in LiM or NVL: (1) a single readout voltage is set between LVT and HVT to access the stored value [193, 194]; (2) two readout voltages are utilized that are either located below LVT and between LVT and HVT, hence performing AND logic together with the stored state of the FeFET, or between LVT and HVT and above HVT to perform OR logic with the stored state [192]. The

AND operation is equivalent to a binary multiply operation between two bits.

LiM exploits both types of readout within different frameworks. The first approach, i.e. using a single readout voltage, was pursued in LiM architectures where the stored values of different FeFET-based memory cells were logically linked directly in the memory array [194] or by modified bit-line sense amplifiers of the array [193–195]. That is, the sense amplifiers were located at the periphery of the memory array and performed either a standard readout of the array (memory mode) or conducted logic operations between the readout cell values (logic mode), such as AND, OR, XOR, and addition operations. The number and type of possible logic operations

**Table 3.** Benchmarking of eFLASH and FeFET technologies for neuromorphic hardware.

Performance metrics	Desired targets	eFLASH	FeFET
Most advanced technology	3–40 nm	28 nm	≤28 nm
Multilevel (Analog) States	4–64	Yes	Yes
PRG/ERS with identical pulses	10–10 <sup>3</sup> pulses	No	Yes
PRG/ERS energy consumption	<10 fJ/pulse	10 pJ/pulse	<10 fJ/pulse
Dynamic Range (on/off)	>100	10 <sup>3</sup> –10 <sup>4</sup>	10 <sup>2</sup> –10 <sup>4</sup>
Retention	>10y at 85 °C	> 10y at 125 °C	>10y at 125 °C
Endurance	>10 <sup>9</sup> cycles (min 10 <sup>5</sup> )	<10 <sup>6</sup>	<10 <sup>8</sup> → theor.: > 10 <sup>9</sup>
Symmetry of States	1	>1	~1
Switching Voltages	<1 V (<3.3 V)	12–18 V	2.5–5 V
CMOS logic mixable/compatible	Yes	No	Yes
PRG/ERS Speed	<100 ns	μs–ms	<10 ns
Read Current (fast read)	2–5 μA	2–5 μA	Scalable as of EOT
On-state Resistance	~1 MΩ (min. 100 kΩ)	100 kΩ–10 MΩ	100 kΩ–10 MΩ
Rad.-hard/magnet.-immune	Yes/Yes	No/Yes	Yes/Yes
Macro Size	mm <sup>2</sup> /32 Mb	~4.5	~4.5
eNVM cell size (28 nm node)	μm <sup>2</sup>	0.036–0.047	0.050–0.120
Mask-Adder (#)	0 (<4)	11	2–4
Technology maturity	Vol. Prod.	>25 y Vol. Prod.	R&D

\*Notes: the values are adapted from [139] and complemented with state-of-the-art industrial results.

are fixed during fabrication and depend on the implementation of the modified sense amplifier. Besides logic operations, this approach was exploited for the search function in secure homomorphically encrypted content addressable memories [195], for one- and for few-shot learning [196, 197]. The second approach, i.e. performing a logic operation within one FeFET, was pursued for simple logic gates [192], for ternary content addressable memory [198, 199] where one cell utilizes XOR logic, for half and full adder circuits [200] as well as for vector-matrix-multipliers (VMM) [201, 202]. The FeFET-based VMMs are a basic element of, for example, deep neural networks [201], and have been additionally exploited for optimizations via the least-squares minimization [202]. In general, computations within the memory array are very flexible in terms of possible logic operations because the logic functionality is determined by the number of utilized FeFETs and their stored states, not by the array periphery.

NVL aims to store one or more operands in a nonvolatile manner within a circuit to avoid the time- and power-intensive fetch of external data. However, as argued in [203], a steady rewriting of the stored value should be avoided to prevent the cycling endurance degradation of the HfO<sub>2</sub>-based FeFET. Hence, NVL gates and adder circuits [191, 192, 200] can take account of this circumstance by storing in FeFETs just those operands that change only occasionally. Additionally, nonvolatile flip-flops and latches establish a local and parallel computing that is resistant to power failures [204–206]. Rather than storing the input values of an operation, FeFETs backup the output of a latch circuit. Approaches towards nonvolatile field-programmable gate arrays proposed nonvolatile routing elements [207] to establish temporary routing paths, enabling a normally-off/instant-on computing. Nonvolatile look-up tables (LUTs) adopted FeFETs for the same reason [191, 200] but additionally reduced the transistor count noticeably compared to SRAM-based LUTs. By

integrating such a LUT into the first stage of a subsequent multiplexer, the transistor count can be reduced even further by at least 33% [200].

In summary, HfO<sub>2</sub>-based FeFETs have the potential to advance ‘beyond-von-Neumann computing’ utilizing LiM and NVL. Not only the ultra-dense co-integration with standard CMOS logic, as discussed in previous section [22], but also the low-power operation by avoiding sneak-path currents and by utilizing normally-off computing support this purpose.

#### 5.4. Other applications

The stochasticity of the abrupt switching in ultra-scaled devices (section 2) can be exploited in those applications, for which randomness and the related unpredictability of future events are of advantage, such as security applications. The probability of abrupt switching in scaled FeFETs from LVT to HVT and vice versa can be tailored by choosing appropriate pulse widths and amplitudes to be applied at the gate (figures 4(e) and (f)). The application of pulse parameters, for which the probability of switching is exactly 50%, translates in a situation where the chance of having LVT (logical ‘1’) or HVT (logical ‘0’) is equal. This feature has been proposed for the generation of random numbers [56], and it has been demonstrated that by repeating the switching cycles over a number of trials, a sequence of equally probable ‘ones’ and ‘zeros’ is obtained at the output (figure 4(f)). As the switching is abrupt and the  $I_{ON}/I_{OFF}$  ratio in FeFETs is orders of magnitude large, the easy distinction between both states is ensured. Nevertheless, although the concept is low-cost, compact and harnesses the material’s intrinsic stochasticity, thus is highly reliable in terms of unpredictability, the limited endurance in FeFETs (<10<sup>8</sup> cycles) may be a bottleneck for this kind of applications. In fact, random number generation applications usually require long binary streams that remain

unbiased over time, which in turn would require a device with an almost unlimited cycling endurance.

Another unconventional application regards the use of FeFETs for analog signal processing, and, in particular, for frequency multiplication and mixing. The transfer  $I_D-V_G$  curve can be tailored in a way to obtain a nearly symmetric, parabolic shape. This has been demonstrated by exploiting the gate-induced drain leakage current and the polarization switching, which contributed to shape the left and the right part of the  $I_D-V_G$  curve, respectively, in an independent manner [208]. Such symmetric curves naturally promote the second harmonic generation of the electrical signal. In fact, by applying at gate a sinusoidal voltage signal, which has the DC offset corresponding to the inflection point of the  $I_D-V_G$  parabola and has the frequency  $f_0$ , an output signal is obtained at the drain, with a frequency  $2f_0$ . The effect of frequency multiplication proved to be very efficient, achieving up to 96% of spectral purity for the double frequency at the output [209]. Such frequency manipulations with FeFETs were then used to demonstrate also other functionalities, such as binary frequency shift keying [208] and frequency mixing [209], which may find application in radiofrequency and signal transmission circuits.

Finally, the hysteretic behavior of FeFETs has been also proposed for nonlinear relaxation oscillators [210, 211], where the possibility of oscillator coupling via a capacitor and the resulting oscillation synchronization dynamics might be interesting for non-Boolean computing [212].

## 6. Conclusions

We have reviewed recent progress in FeFET technology enabled by ferroelectric  $\text{HfO}_2$  over the past ten years. While initial demonstrations of simple MFIS FeFETs show promising results in terms of retention (10 years), memory window ( $>3$  V), low-power and fast operation ( $<5$  V, 10 ns) and endurance ( $>10^5$  write cycles), many hurdles need to be overcome in order to start competing with the well-established flash technology. For instance, material and geometry optimization of both FE layer and IL needs to be done to overcome (1) inter-device variability coming from the polycrystalline and untextured FE films; (2) inter- and intra-device variability upon lateral device scaling; (3) insufficient MW due to vanishing FE properties at increased thicknesses of the FE; (4) sub-optimal  $k$ -value of the IL leading to sub-optimal write efficiency, interface degradation, charge injection and endurance limitation; (5) limited retention at elevated temperatures. Moreover, although first encouraging demonstrations of larger memory arrays have been reported, further effort in this direction has to be pursued in order to find suitable architectures for FeFETs while minimizing the area and power consumption as well as the impact of disturbs. While the knowledge from flash arrays can be very useful, it cannot be merely replicated to FeFETs, as the latter display much different operational and material properties. Larger arrays will also enable the collection of large statistics of key device metrics, which is particularly important in

understanding and judging retention and variability concerns. Finally, we also surveyed early work in using FeFETs as neuromorphic, logic and radiofrequency devices.

In conclusion, the vast and fascinating possibilities offered by FeFETs are yet to be explored. At the moment, the most obvious adoption is as fast, low-power, low-cost and high-density alternative to embedded flash, but these devices also seem to be perfect candidates for the nascent era of neuromorphic and in-memory computing.

## Acknowledgments

This work is funded by the German Bundesministerium für Wirtschaft (BMWI) and by the State of Saxony in the frame of the ‘Important Project of Common European Interest (IPCEI).’

## Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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