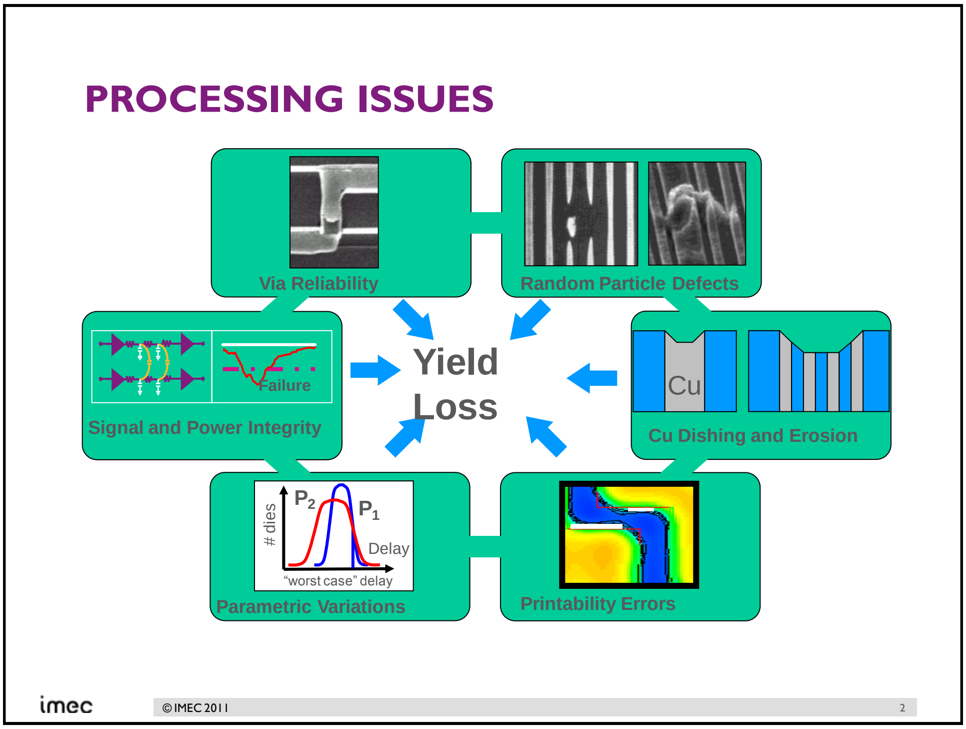
IMEC TRAINING

CLASSICAL DESIGN FLOW FOR TAPEOUT WITH UMC 90NM TECHNOLOGY VIA EUROPRACTICE

ATPG



PROCESSING ISSUES

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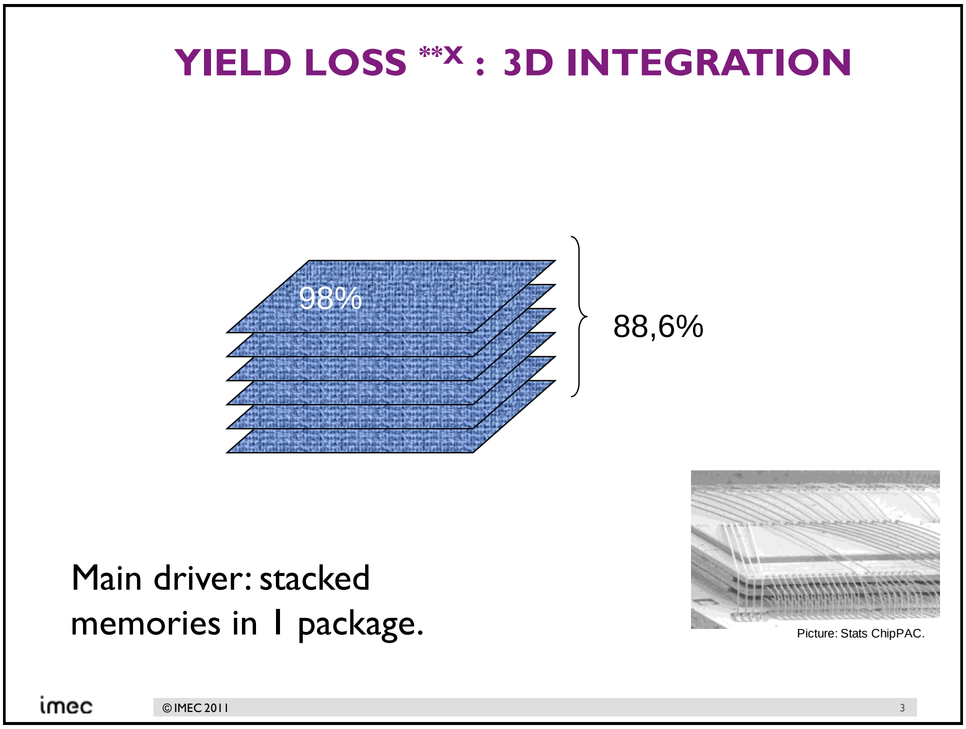

YIELD LOSS ^{**x} : 3D INTEGRATION

Main driver: stacked memories in 1 package.

Picture: Stats ChipPAC.

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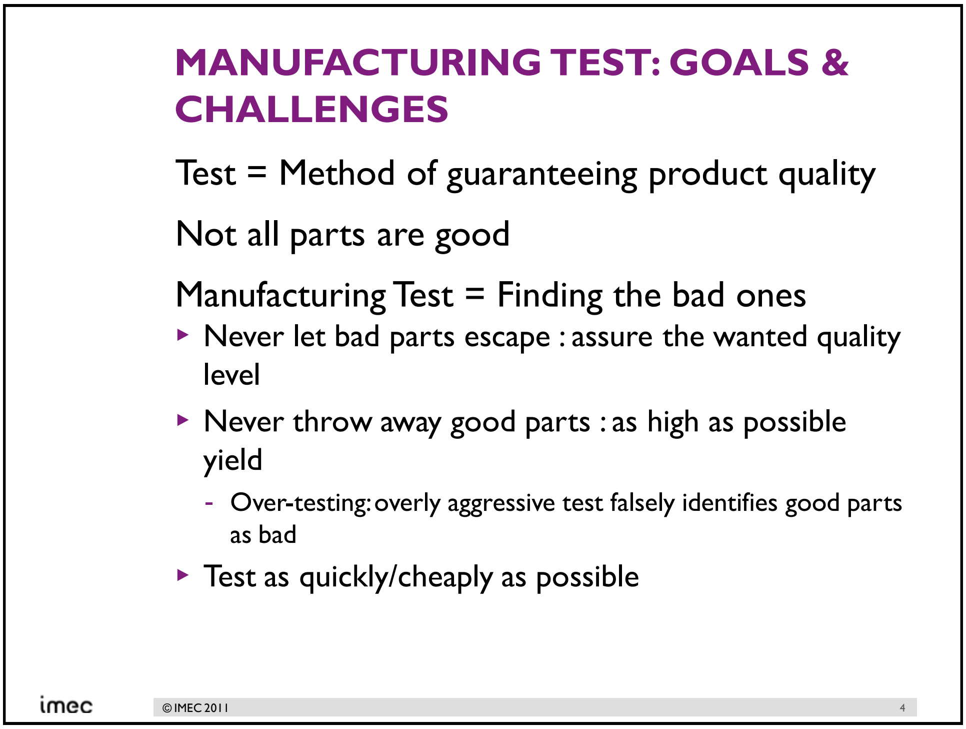

MANUFACTURING TEST: GOALS & CHALLENGES

Test = Method of guaranteeing product quality

Not all parts are good

Manufacturing Test = Finding the bad ones

- Never let bad parts escape : assure the wanted quality level
- Never throw away good parts : as high as possible yield
  - Over-testing: overly aggressive test falsely identifies good parts as bad
- Test as quickly/cheaply as possible

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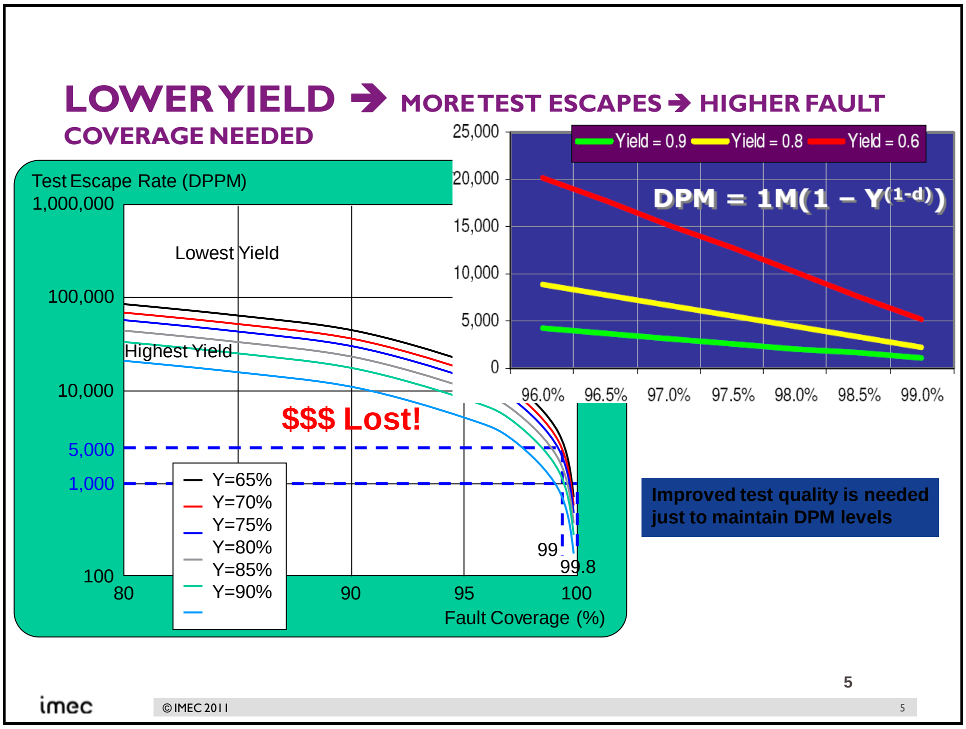

LOWER YIELD → MORE TEST ESCAPES → HIGHER FAULT COVERAGE NEEDED

$$DPM = 1M(1 - Y^{(1-d)})$$

Improved test quality is needed just to maintain DPM levels

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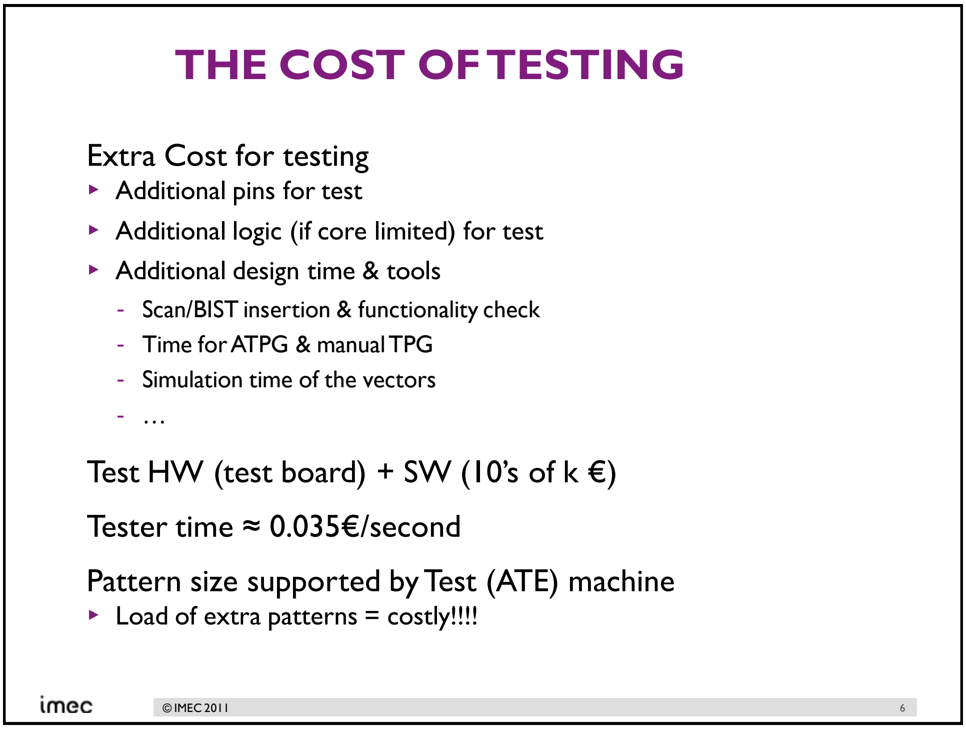

THE COST OF TESTING

Extra Cost for testing

- Additional pins for test
- Additional logic (if core limited) for test
- Additional design time & tools
  - Scan/BIST insertion & functionality check
  - Time for ATPG & manual TPG
  - Simulation time of the vectors
  - …

Test HW (test board) + SW (10's of k €)

Tester time ≈ 0.035€/second

Pattern size supported by Test (ATE) machine

- Load of extra patterns = costly!!!!

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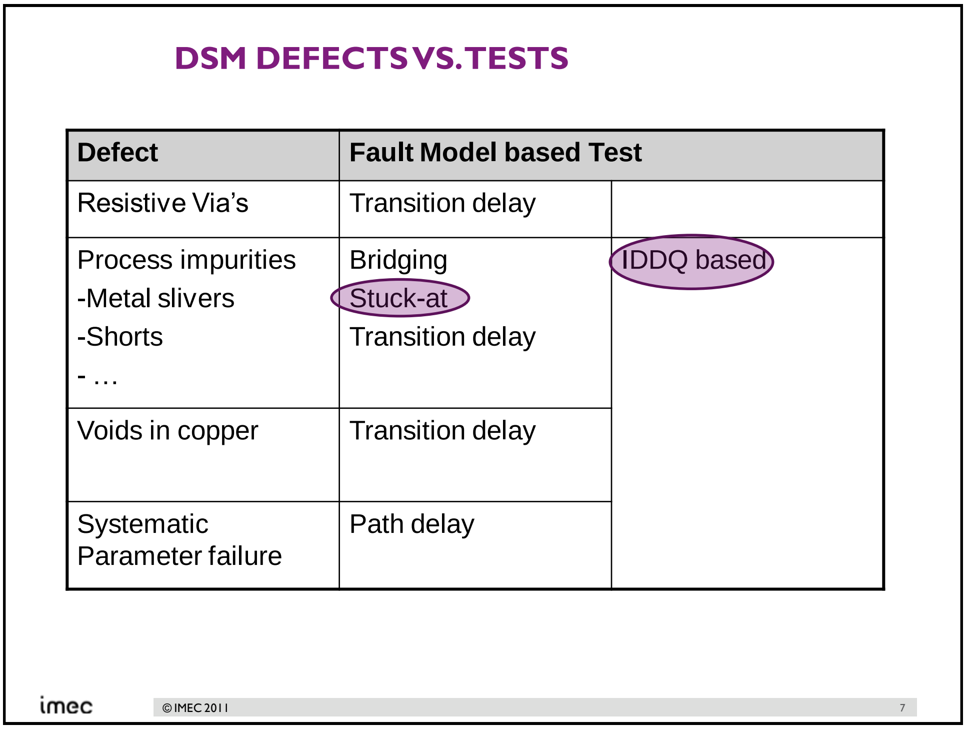

DSM DEFECTS VS. TESTS

Defect	Fault Model based Test	
Resistive Via's	Transition delay	
Process impurities -Metal slivers -Shorts - …	Bridging Stuck-at Transition delay	IDDQ based
Voids in copper	Transition delay	
Systematic Parameter failure	Path delay	

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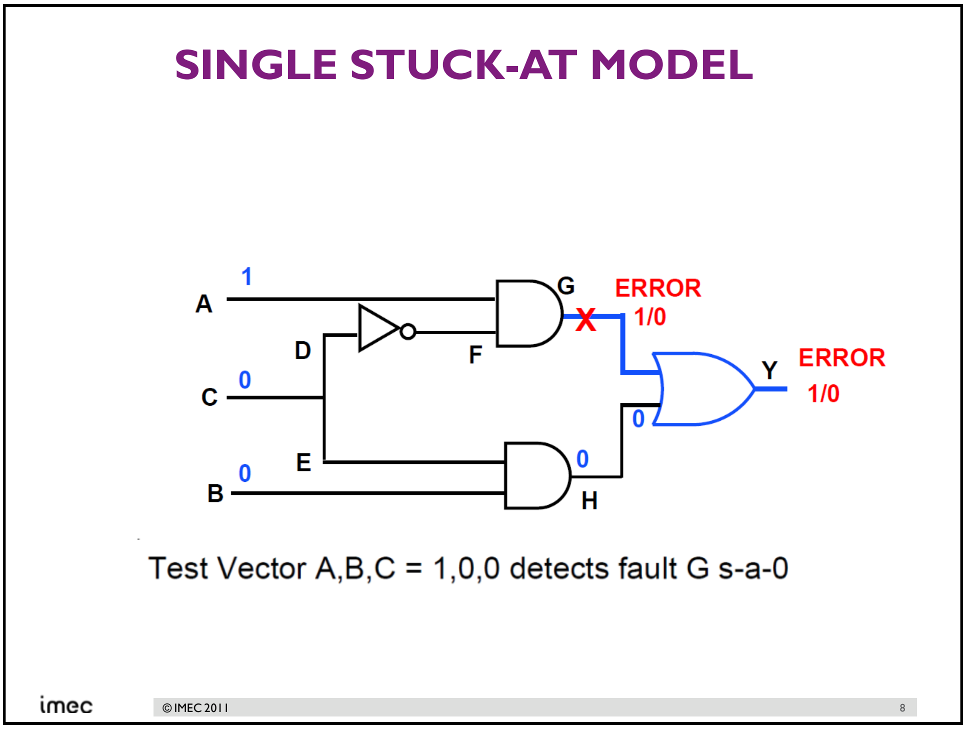

SINGLE STUCK-AT MODEL

Test Vector A,B,C = 1,0,0 detects fault G s-a-0

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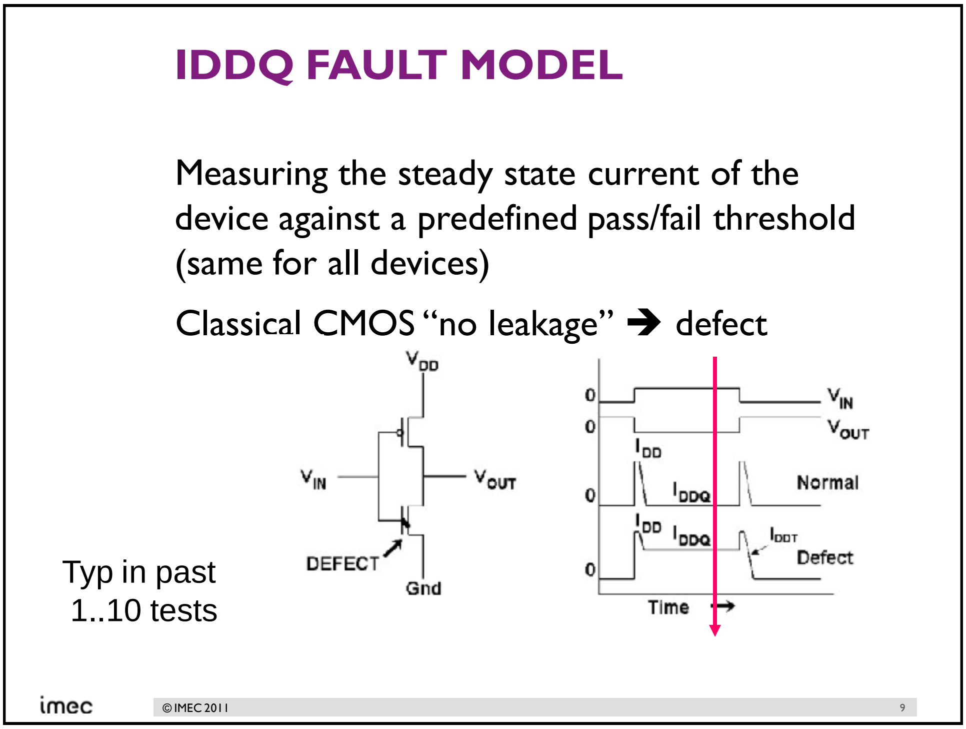
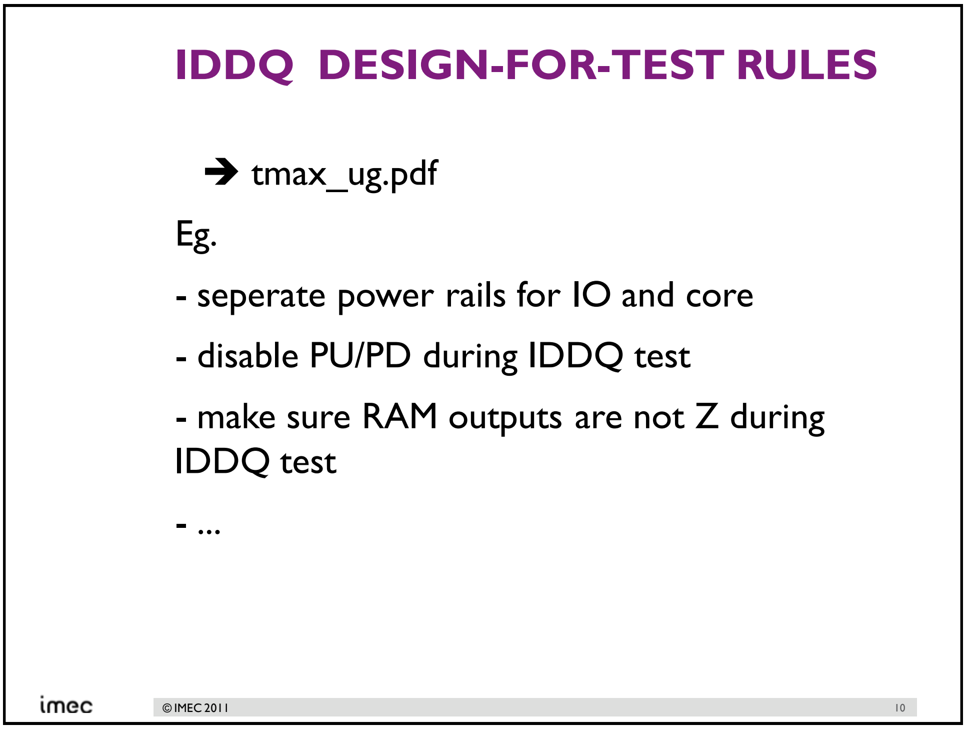


IDDQ FAULT MODEL

Measuring the steady state current of the device against a predefined pass/fail threshold (same for all devices)

Classical CMOS "no leakage" ➔ defect

Typ in past
1..10 tests



IDDQ DESIGN-FOR-TEST RULES

➔ tmax_ug.pdf

Eg.

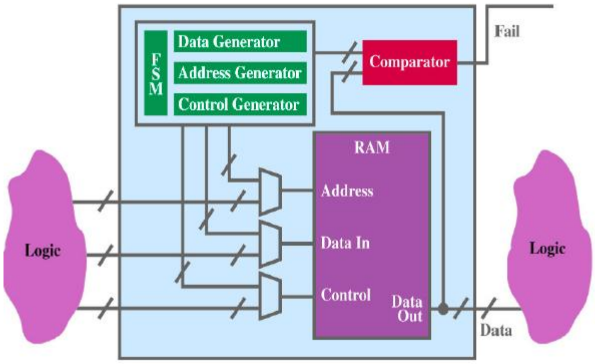
- seperate power rails for IO and core

- disable PU/PD during IDDQ test

- make sure RAM outputs are not Z during IDDQ test

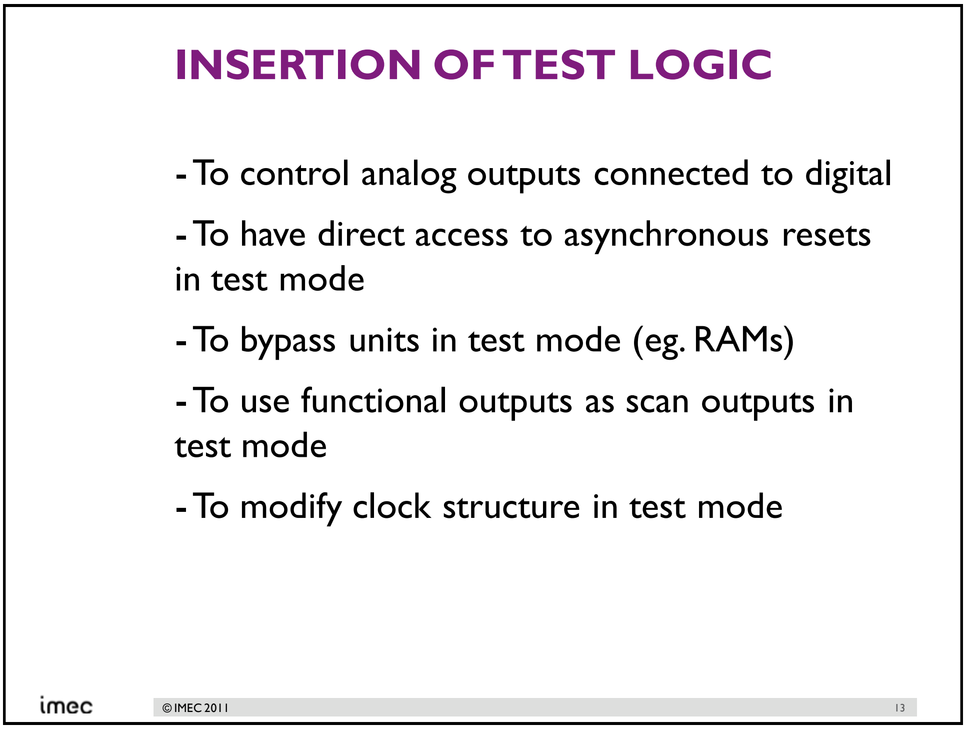
- ...

TESTING MEMORY ARRAYS



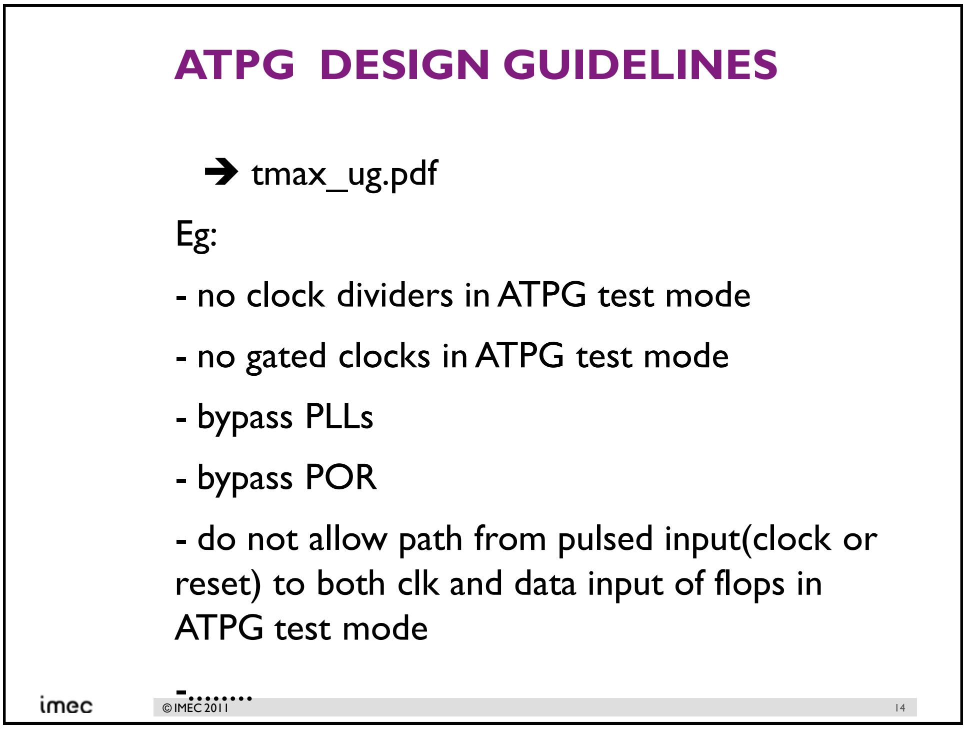
BASIC ATPG FLOW (LOW SPEED PAT)

- ❑Insertion of test logic and scan chains during rtl design & synthesis
- ❑Generation of the pre-layout patterns (stuck-at/iddq)
- ❑Verification(simulation) of pattern subset using dummy sdf
- ❑Layout (=> change of netlist)
- ❑Generation of the post-layout patterns (stuck-at/iddq)
- ❑Verification(simulation) of patterns (subset) using bc & wc sdf



INSERTION OF TEST LOGIC

- To control analog outputs connected to digital
- To have direct access to asynchronous resets in test mode
- To bypass units in test mode (eg. RAMs)
- To use functional outputs as scan outputs in test mode
- To modify clock structure in test mode

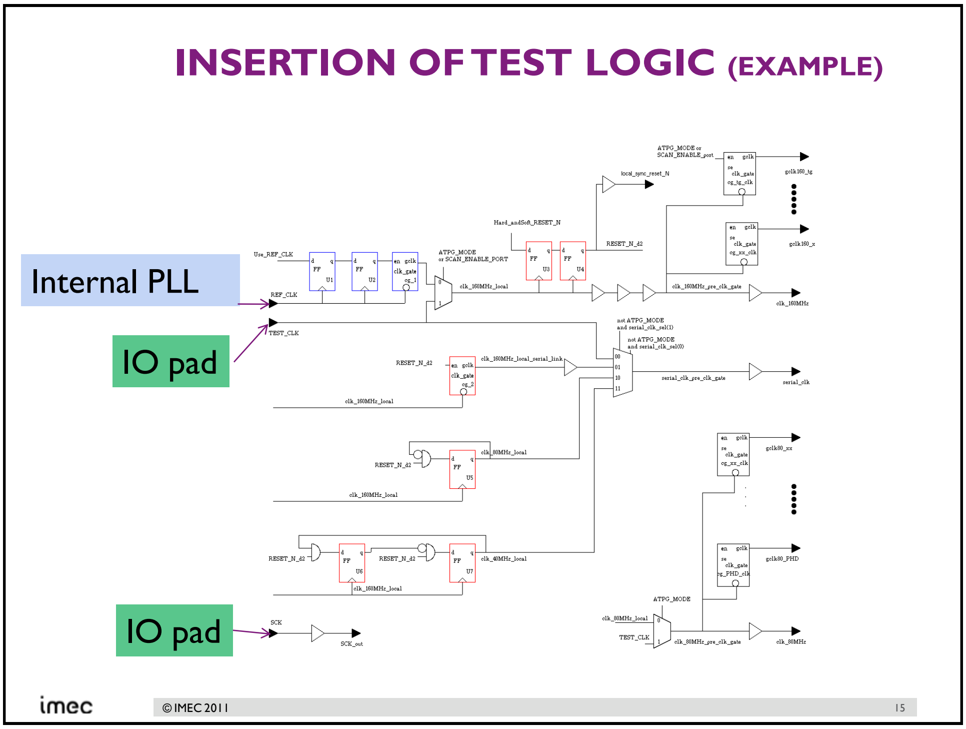


ATPG DESIGN GUIDELINES

➔ tmax_ug.pdf

Eg:

- no clock dividers in ATPG test mode
- no gated clocks in ATPG test mode
- bypass PLLs
- bypass POR
- do not allow path from pulsed input(clock or reset) to both clk and data input of flops in ATPG test mode
-………



INSERTION OF TEST LOGIC (EXAMPLE)

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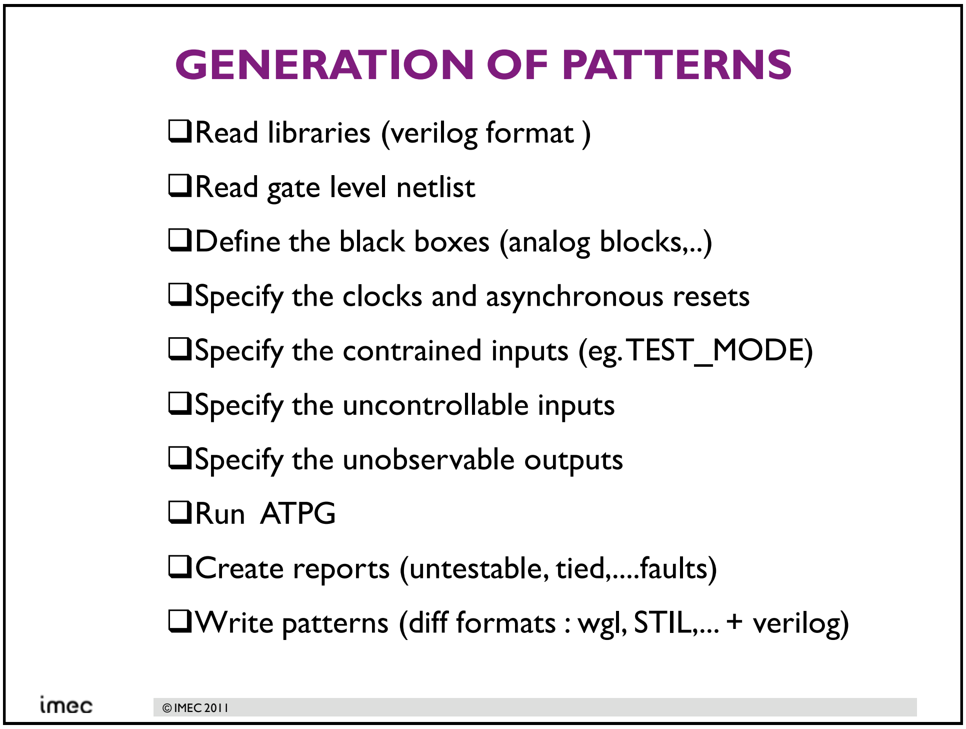

GENERATION OF PATTERNS

❑Read libraries (verilog format)

❑Read gate level netlist

❑Define the black boxes (analog blocks,..)

❑Specify the clocks and asynchronous resets

❑Specify the contrained inputs (eg. TEST_MODE)

❑Specify the uncontrollable inputs

❑Specify the unobservable outputs

❑Run ATPG

❑Create reports (untestable, tied,….faults)

❑Write patterns (diff formats : wgl, STIL,… + verilog)

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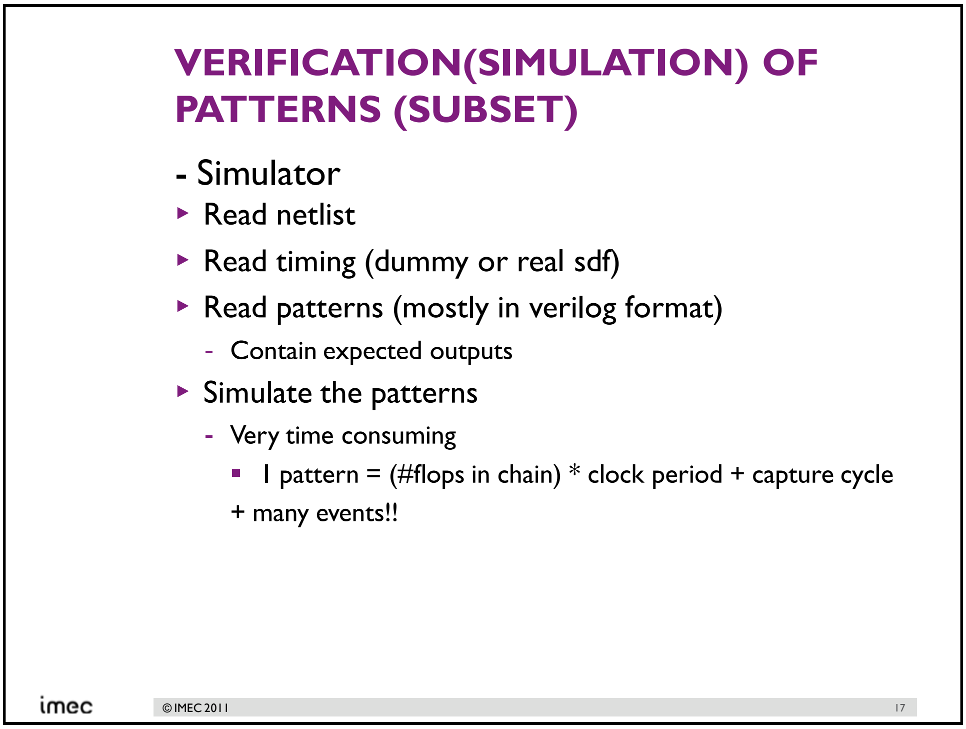

VERIFICATION(SIMULATION) OF PATTERNS (SUBSET)

- Simulator
- ▸ Read netlist
- ▸ Read timing (dummy or real sdf)
- ▸ Read patterns (mostly in verilog format)
  - Contain expected outputs
- ▸ Simulate the patterns
  - Very time consuming
    - ▪ 1 pattern = (#flops in chain) * clock period + capture cycle + many events!!

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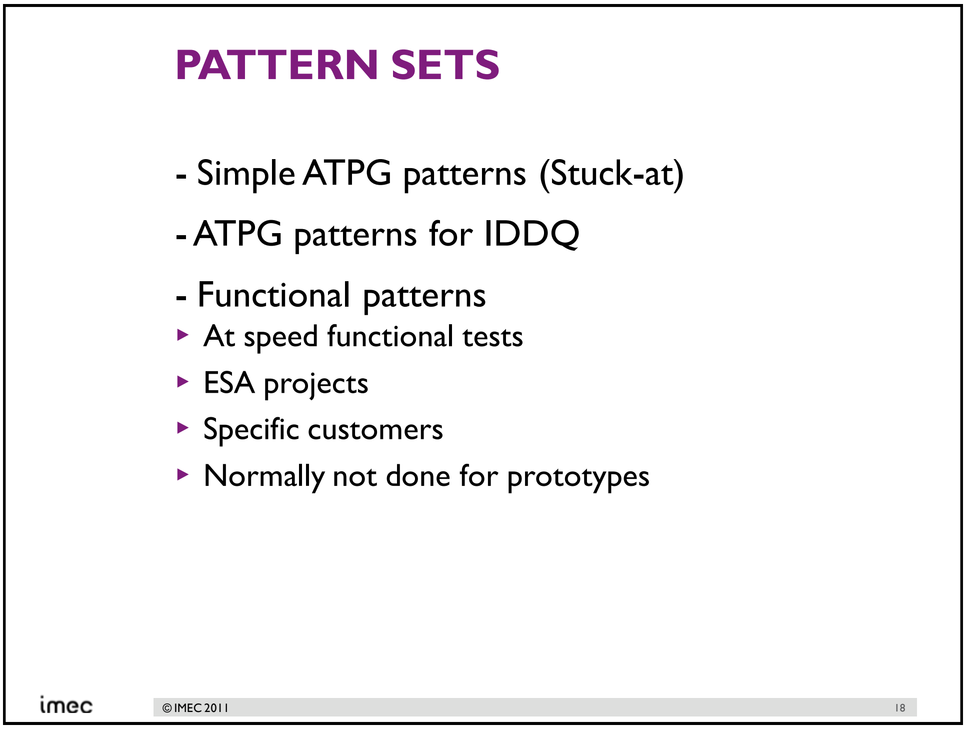

PATTERN SETS

- Simple ATPG patterns (Stuck-at)
- ATPG patterns for IDDQ
- Functional patterns
- ▸ At speed functional tests
- ▸ ESA projects
- ▸ Specific customers
- ▸ Normally not done for prototypes

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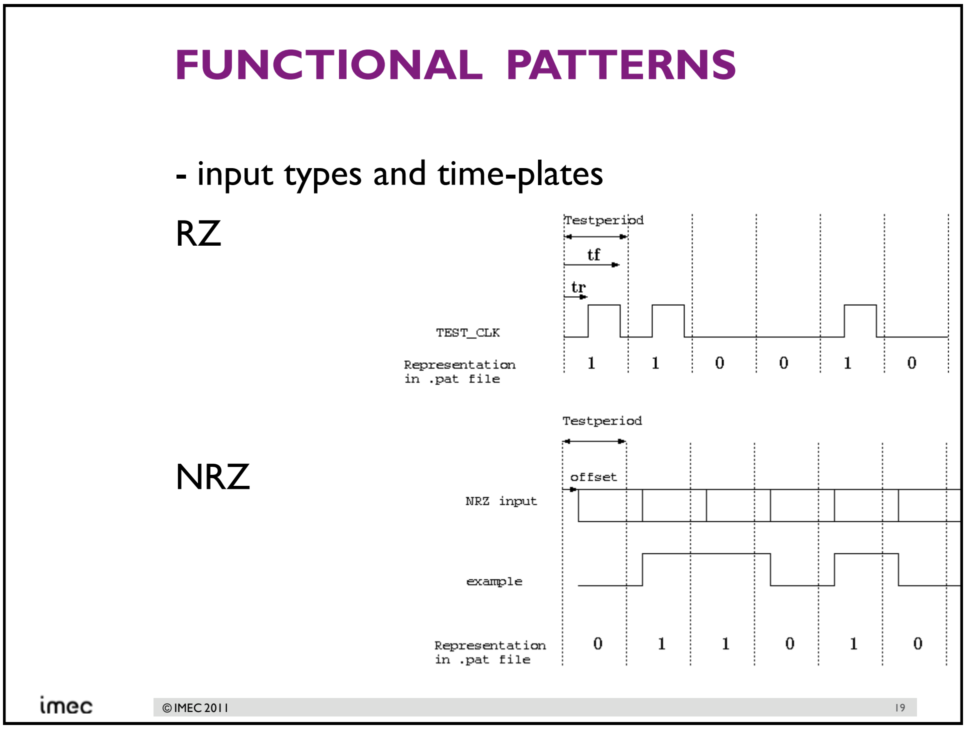

FUNCTIONAL PATTERNS

- input types and time-plates

RZ

NRZ

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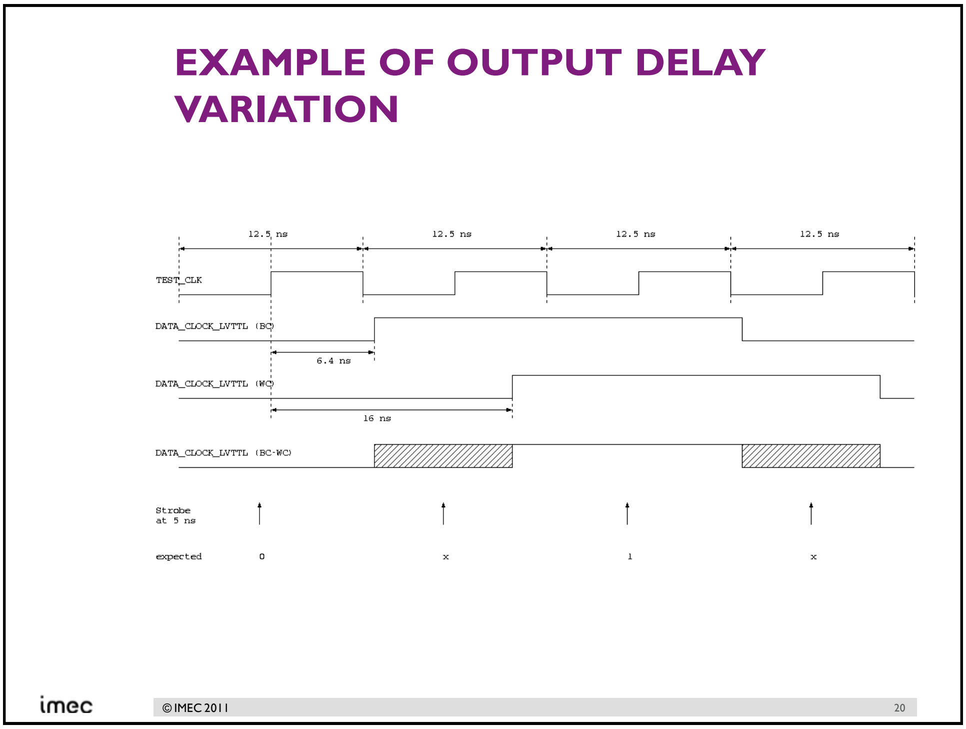

EXAMPLE OF OUTPUT DELAY VARIATION

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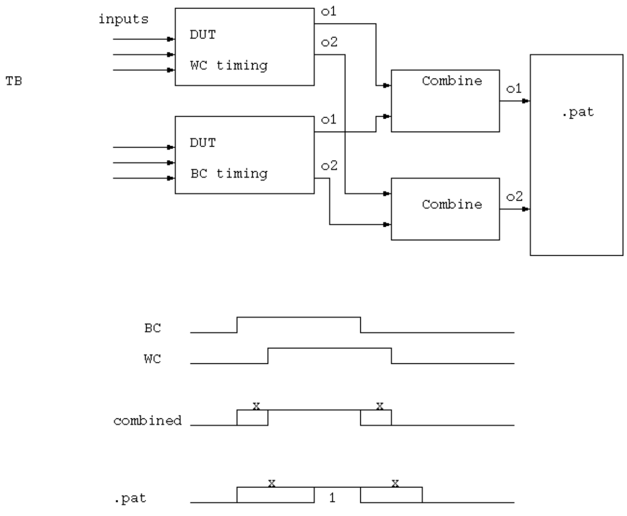
CREATION OF PATTERN FILE COMBINING DIFFERENT (P,V,T)



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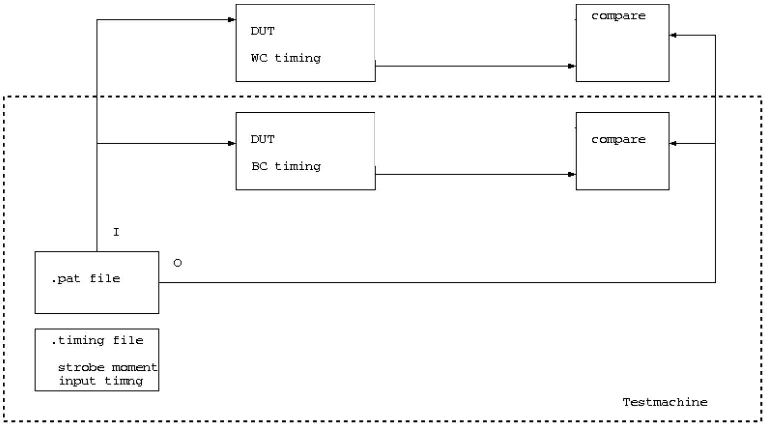
VHDL TESTMACHINE



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