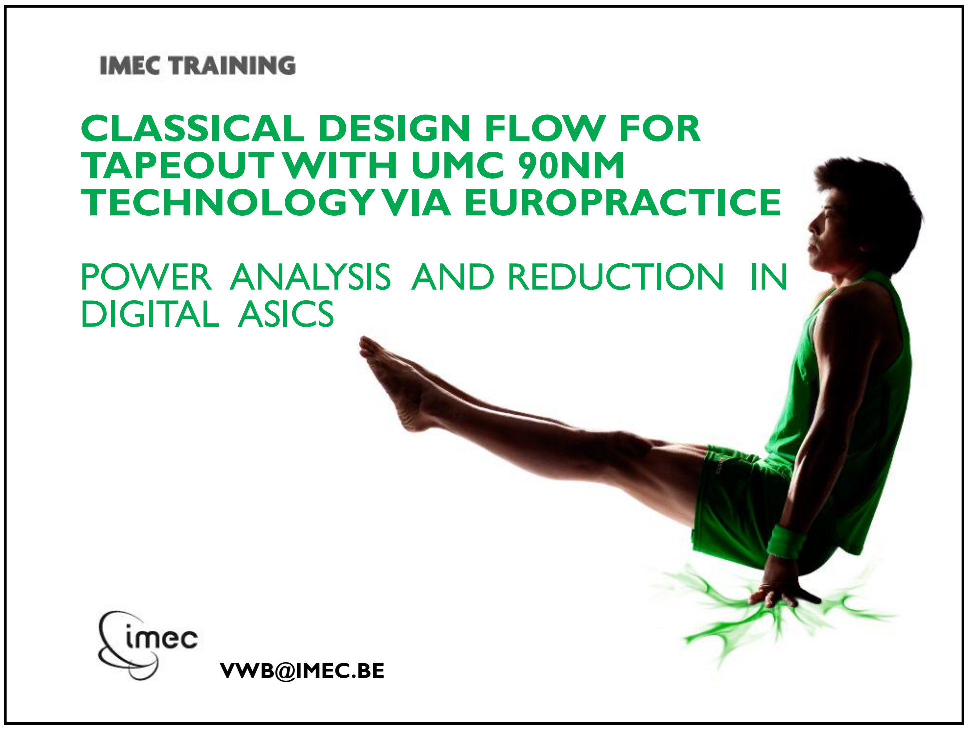
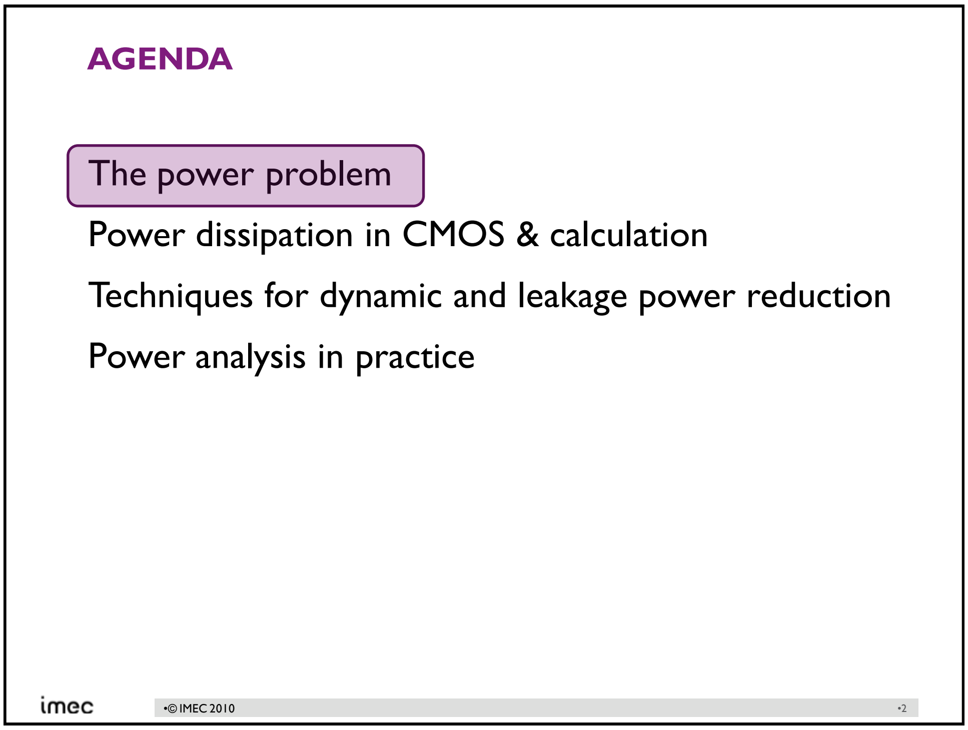


IMEC TRAINING

CLASSICAL DESIGN FLOW FOR TAPEOUT WITH UMC 90NM TECHNOLOGY VIA EUROPRACTICE

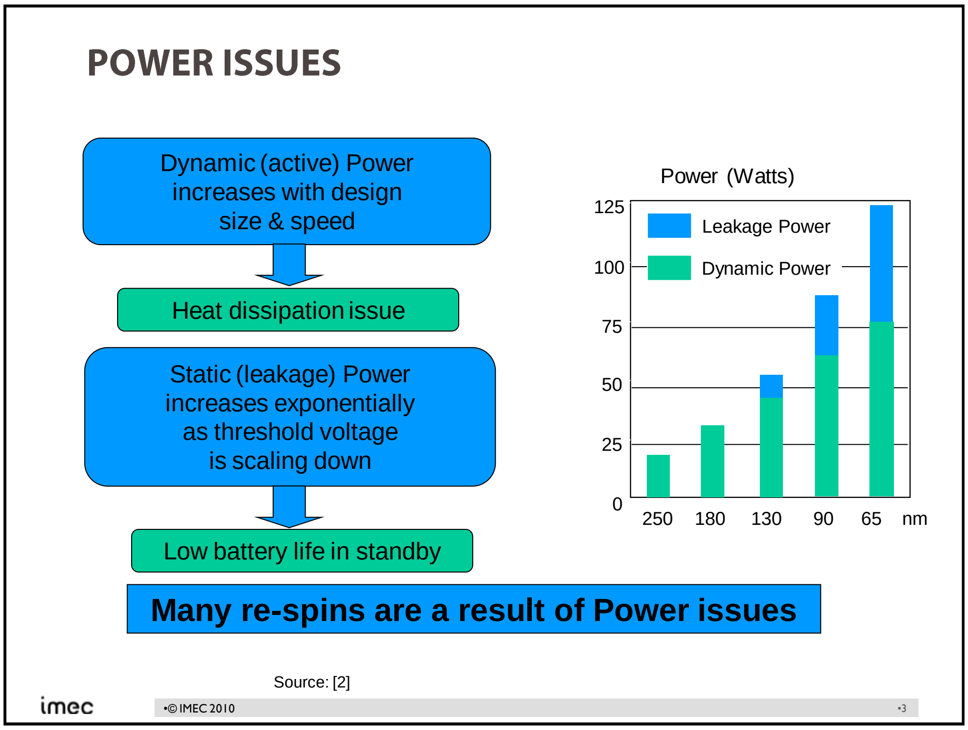
POWER ANALYSIS AND REDUCTION IN DIGITAL ASICS

VWB@IMEC.BE



AGENDA

- The power problem
- Power dissipation in CMOS & calculation
- Techniques for dynamic and leakage power reduction
- Power analysis in practice



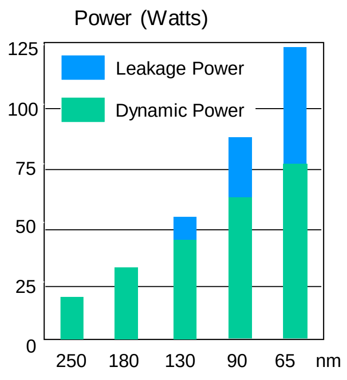
POWER ISSUES

Dynamic (active) Power increases with design size & speed

Heat dissipation issue

Static (leakage) Power increases exponentially as threshold voltage is scaling down

Low battery life in standby



Many re-spins are a result of Power issues

Source: [2]

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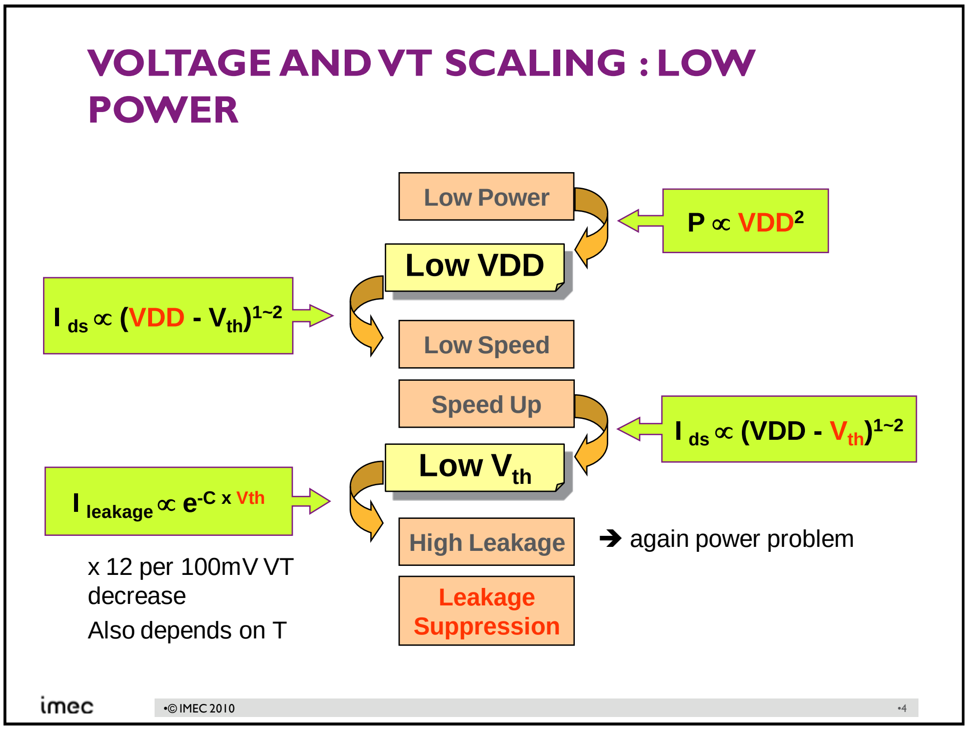

VOLTAGE AND VT SCALING : LOW POWER

Low Power

$P \propto VDD^2$

Low VDD

$I_{ds} \propto (VDD - V_{th})^{1\sim2}$

Low Speed

Speed Up

$I_{ds} \propto (VDD - V_{th})^{1\sim2}$

Low V_{th}

$I_{leakage} \propto e^{-C \times V_{th}}$

High Leakage → again power problem

Leakage Suppression

x 12 per 100mV VT decrease

Also depends on T

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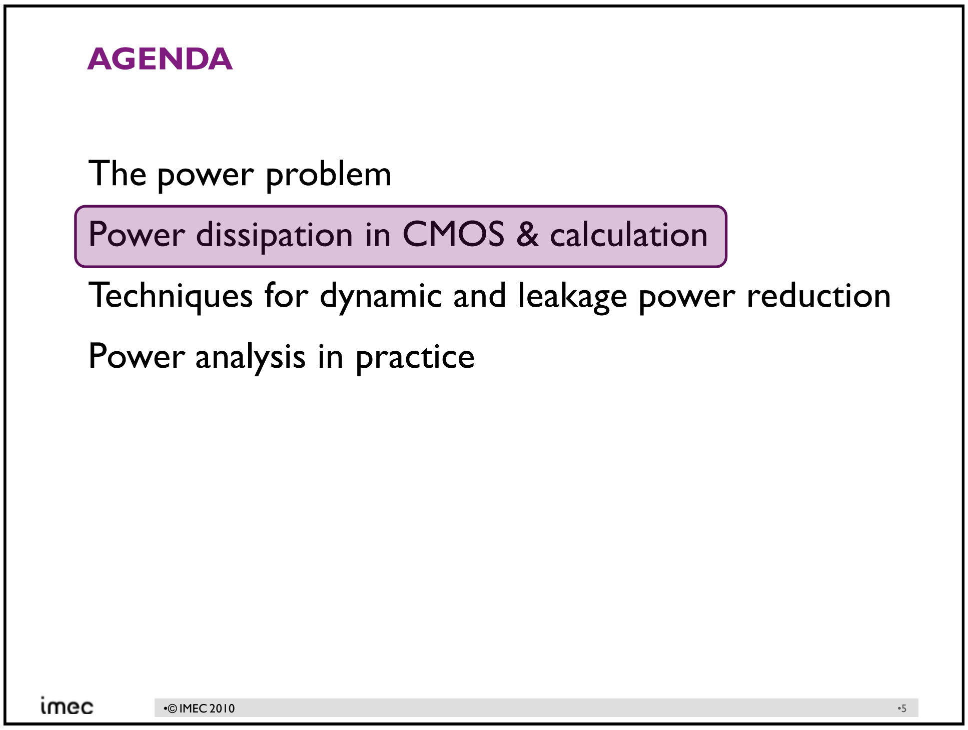

AGENDA

The power problem

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Power analysis in practice

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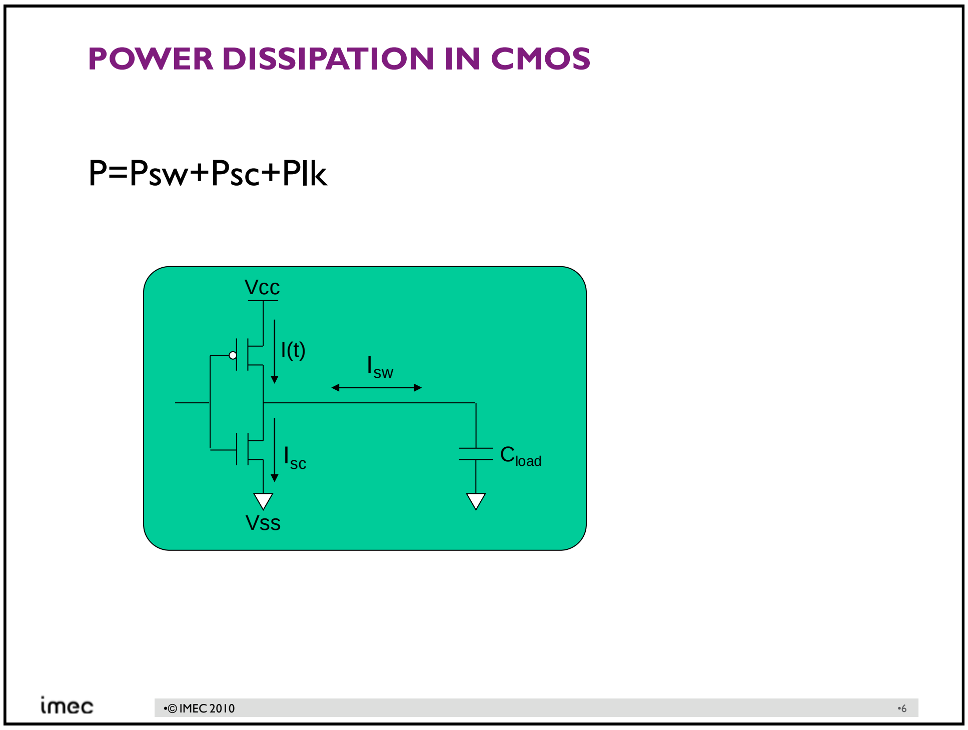
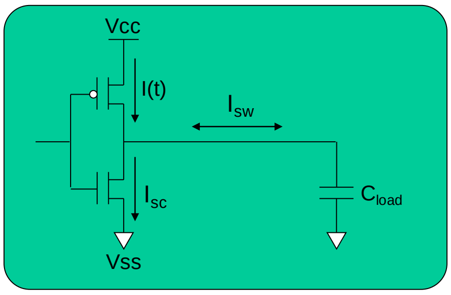


POWER DISSIPATION IN CMOS

P=Psw+Psc+Plk



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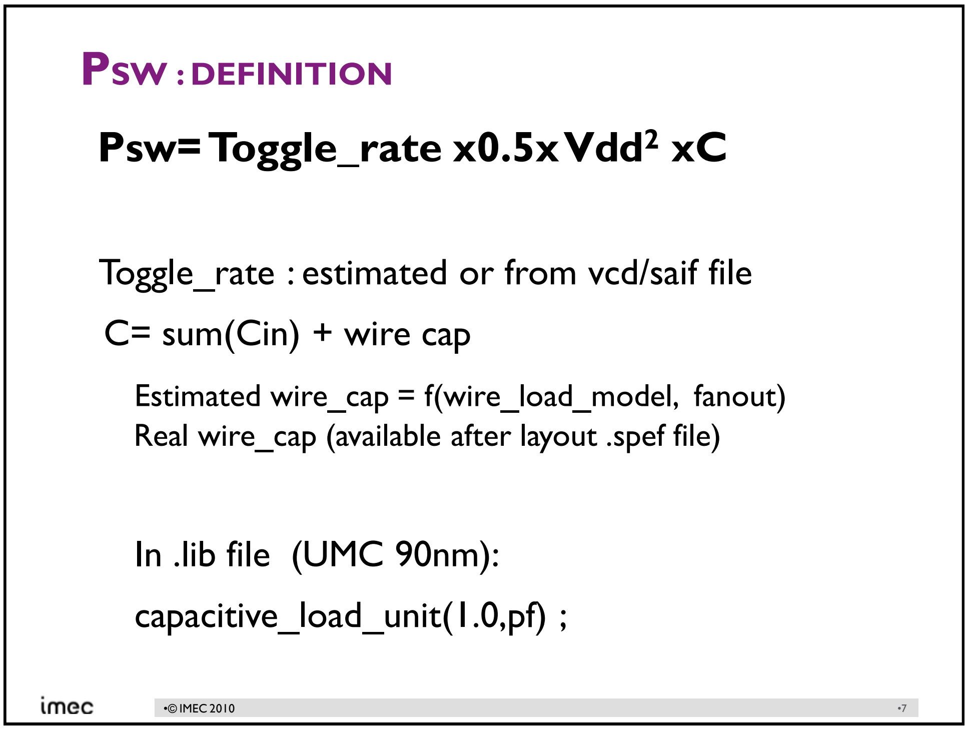

Psw : DEFINITION

Psw= Toggle_rate x0.5x Vdd^2 xC

Toggle_rate : estimated or from vcd/saif file

C= sum(Cin) + wire cap

Estimated wire_cap = f(wire_load_model, fanout)
Real wire_cap (available after layout .spef file)

In .lib file (UMC 90nm):

capacitive_load_unit(1.0,pf) ;

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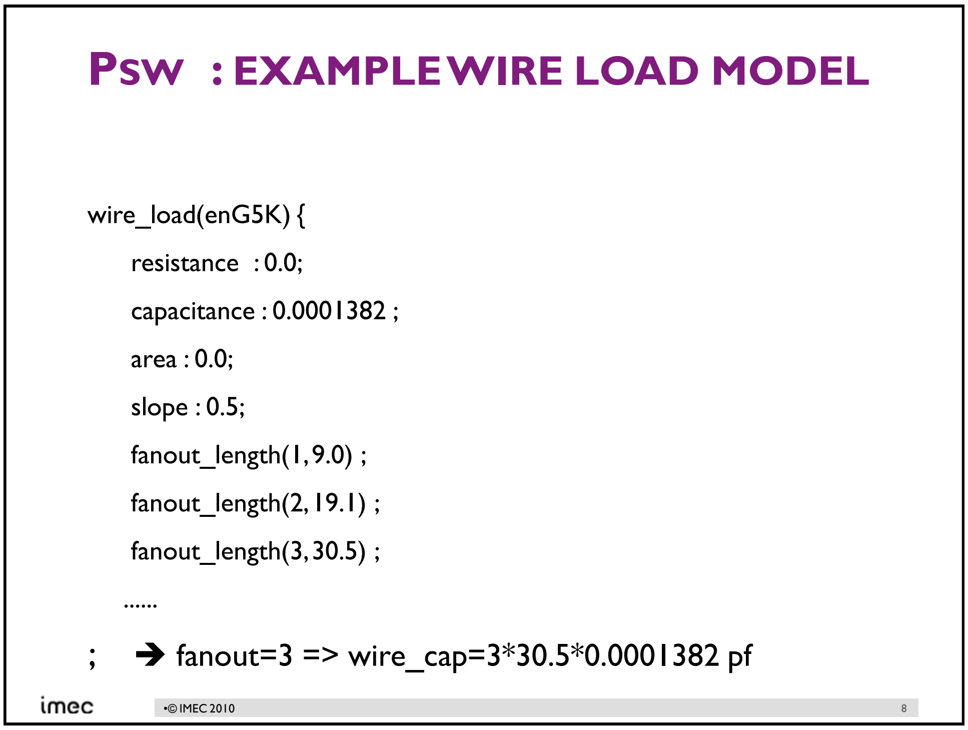

Psw : EXAMPLE WIRE LOAD MODEL

```
wire_load(enG5K) {
    resistance  : 0.0;
    capacitance : 0.0001382 ;
    area : 0.0;
    slope : 0.5;
    fanout_length(1, 9.0) ;
    fanout_length(2, 19.1) ;
    fanout_length(3, 30.5) ;
   ……
;
```

➔ fanout=3 => wire_cap=3*30.5*0.0001382 pf

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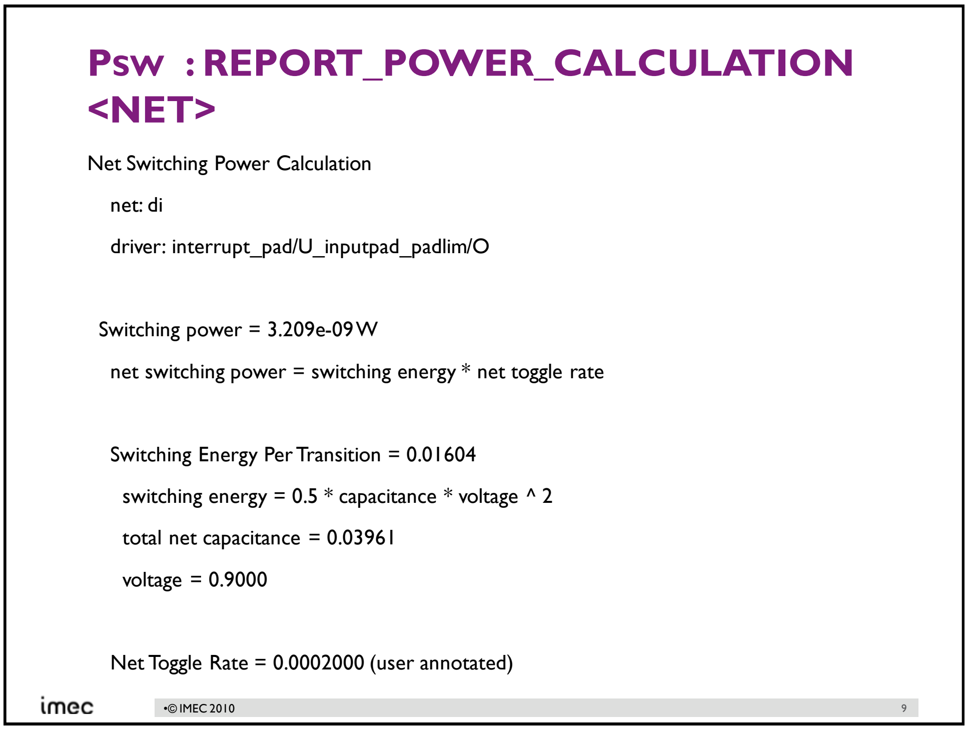

Psw : REPORT_POWER_CALCULATION <NET>

```
Net Switching Power Calculation
  net: di
  driver: interrupt_pad/U_inputpad_padlim/O

 Switching power = 3.209e-09 W
  net switching power = switching energy * net toggle rate

  Switching Energy Per Transition = 0.01604
    switching energy = 0.5 * capacitance * voltage ^ 2
    total net capacitance = 0.03961
    voltage = 0.9000

  Net Toggle Rate = 0.0002000 (user annotated)
```

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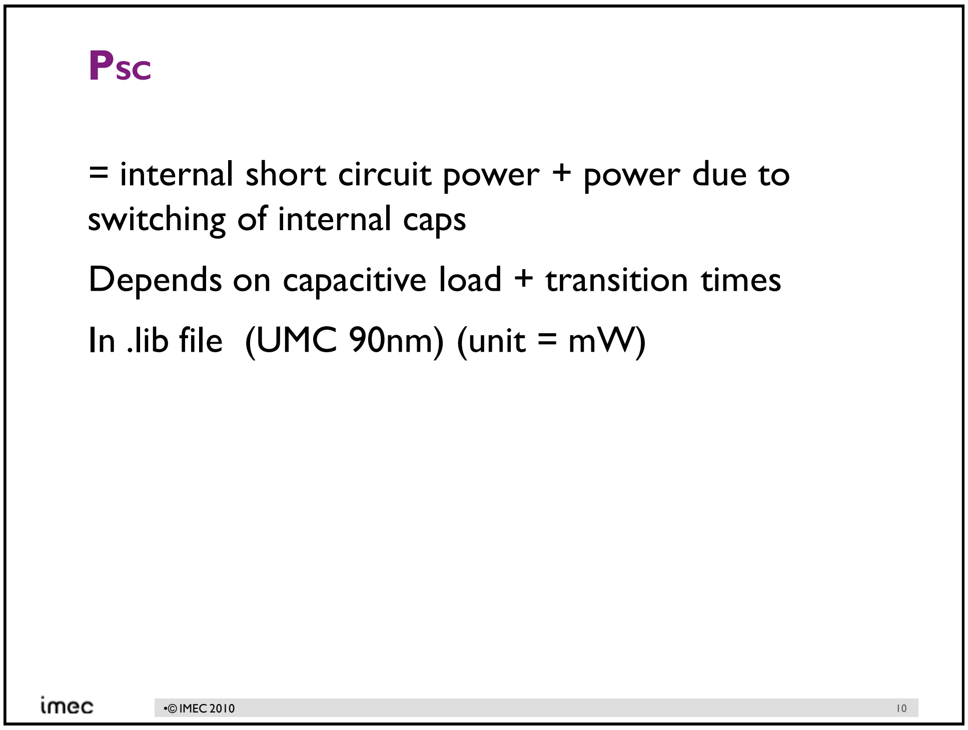

Psc

= internal short circuit power + power due to switching of internal caps

Depends on capacitive load + transition times

In .lib file (UMC 90nm) (unit = mW)

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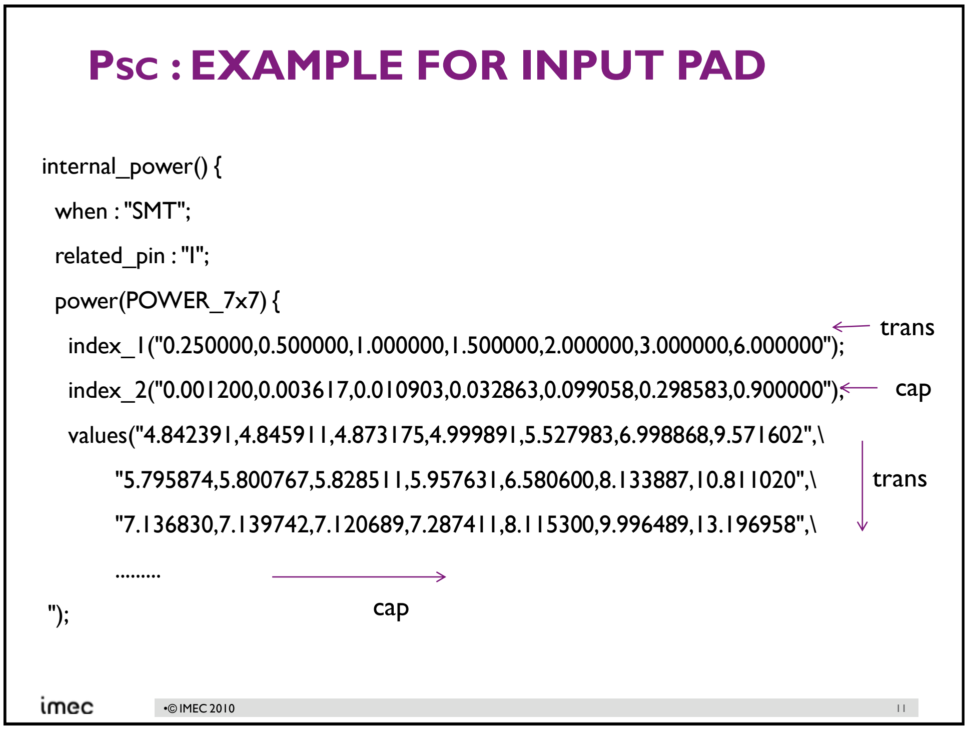

Psc : EXAMPLE FOR INPUT PAD

```
internal_power() {
  when : "SMT";
  related_pin : "I";
  power(POWER_7x7) {
    index_1("0.250000,0.500000,1.000000,1.500000,2.000000,3.000000,6.000000");   ← trans
    index_2("0.001200,0.003617,0.010903,0.032863,0.099058,0.298583,0.900000");   ← cap
    values("4.842391,4.845911,4.873175,4.999891,5.527983,6.998868,9.571602",\
           "5.795874,5.800767,5.828511,5.957631,6.580600,8.133887,10.811020",\     ↓ trans
           "7.136830,7.139742,7.120689,7.287411,8.115300,9.996489,13.196958",\
           .........              ————→
");                                  cap
```

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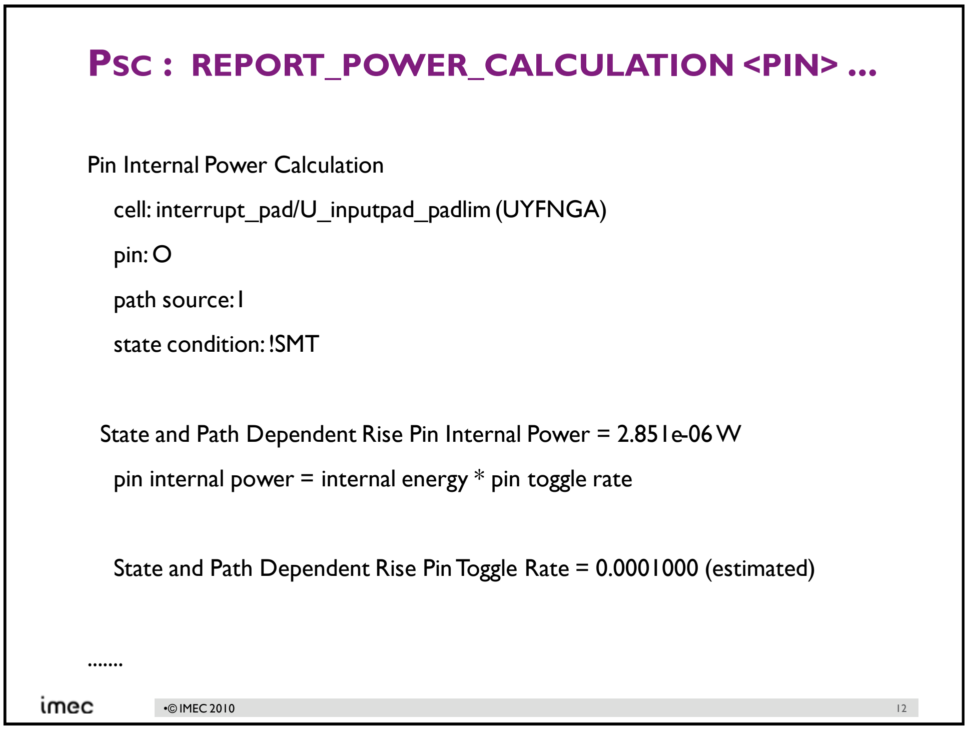

Psc : REPORT_POWER_CALCULATION <PIN> ...

```
Pin Internal Power Calculation
    cell: interrupt_pad/U_inputpad_padlim (UYFNGA)
    pin: O
    path source: I
    state condition: !SMT

  State and Path Dependent Rise Pin Internal Power = 2.851e-06 W
    pin internal power = internal energy * pin toggle rate

    State and Path Dependent Rise Pin Toggle Rate = 0.0001000 (estimated)

.......
```

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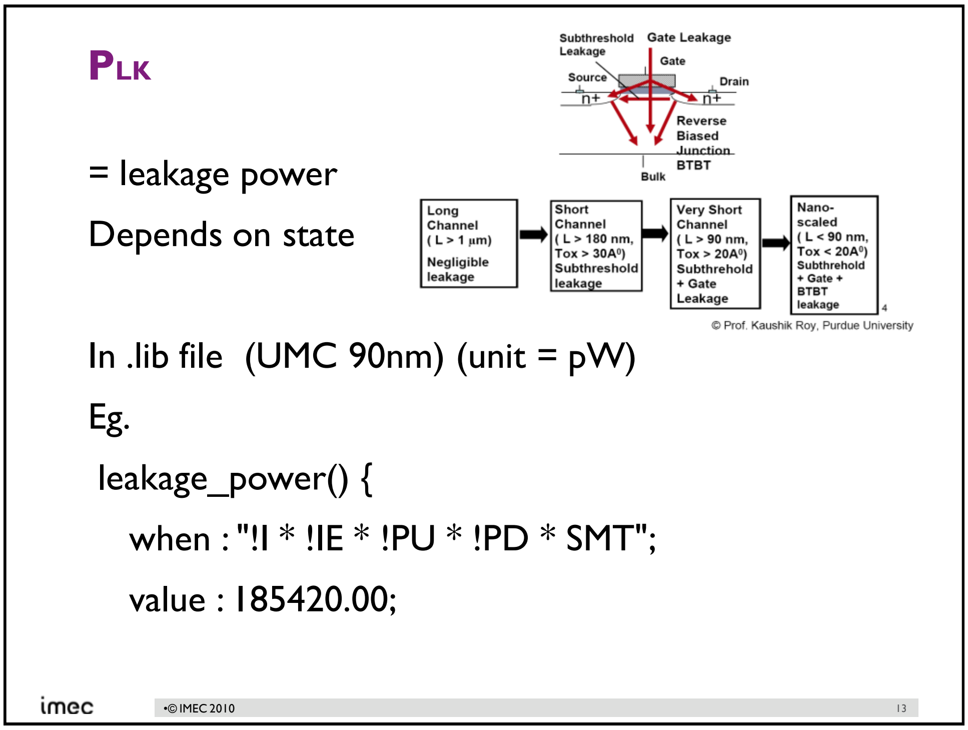
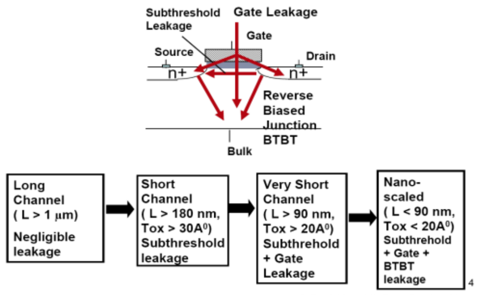


PLK

= leakage power

Depends on state


Subthreshold Leakage
Gate Leakage
Gate
Source
Drain
n+
n+
Reverse Biased Junction BTBT
Bulk
Long Channel (L > 1 μm) Negligible leakage
Short Channel (L > 180 nm, Tox > 30A⁰) Subthreshold leakage
Very Short Channel (L > 90 nm, Tox > 20A⁰) Subthrehold + Gate Leakage
Nano-scaled (L < 90 nm, Tox < 20A⁰) Subthrehold + Gate + BTBT leakage
4
© Prof. Kaushik Roy, Purdue University

In .lib file (UMC 90nm) (unit = pW)

Eg.

```
 leakage_power() {
    when : "!I * !IE * !PU * !PD * SMT";
    value : 185420.00;
```

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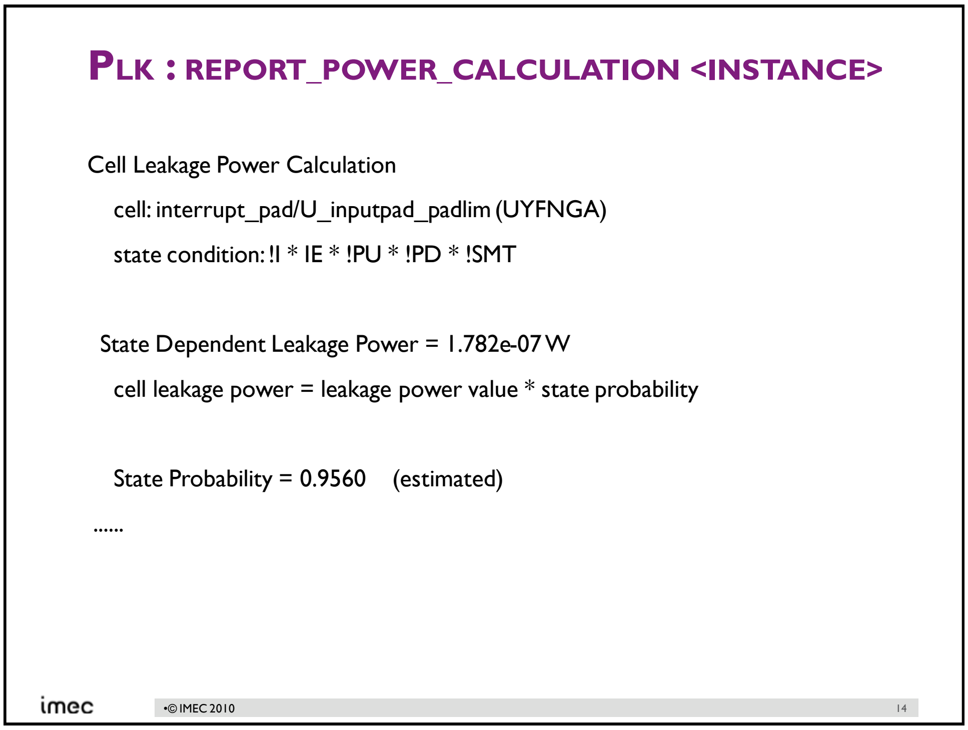

PLK : REPORT_POWER_CALCULATION <INSTANCE>

```
Cell Leakage Power Calculation
   cell: interrupt_pad/U_inputpad_padlim (UYFNGA)
   state condition: !I * IE * !PU * !PD * !SMT

  State Dependent Leakage Power = 1.782e-07 W
   cell leakage power = leakage power value * state probability

   State Probability = 0.9560     (estimated)
......
```

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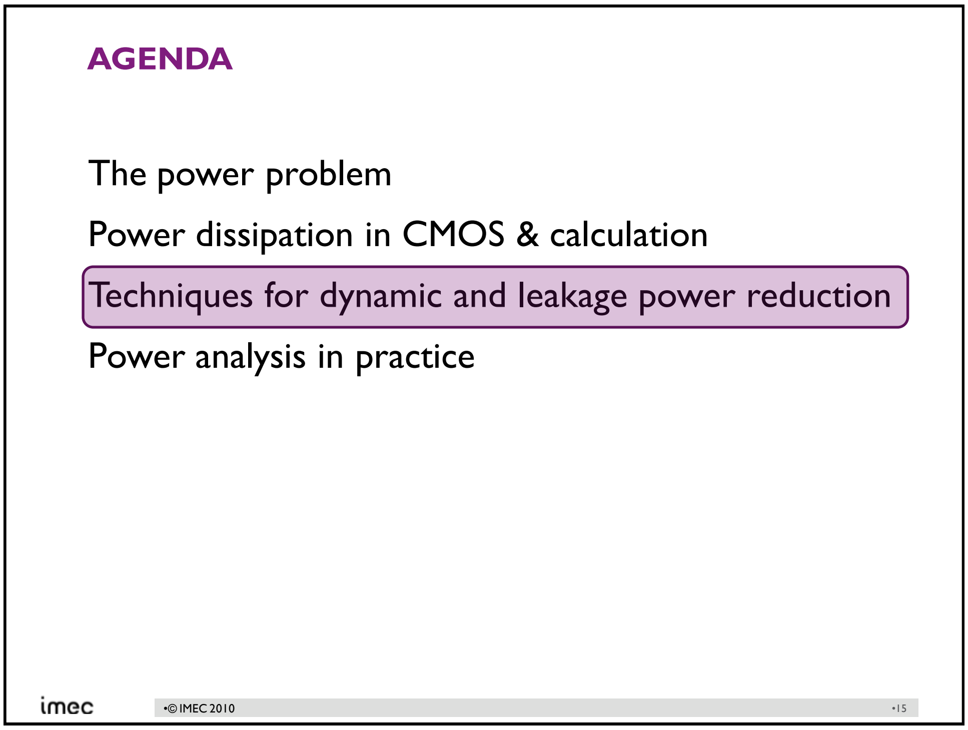

AGENDA

The power problem

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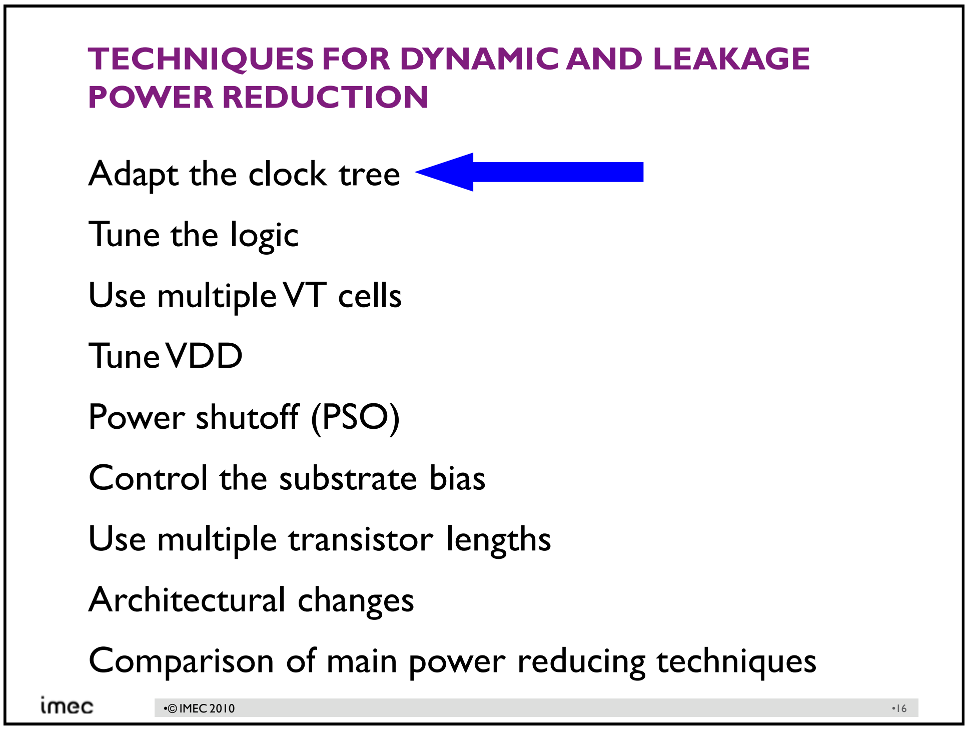

TECHNIQUES FOR DYNAMIC AND LEAKAGE POWER REDUCTION

Adapt the clock tree ←

Tune the logic

Use multiple VT cells

Tune VDD

Power shutoff (PSO)

Control the substrate bias

Use multiple transistor lengths

Architectural changes

Comparison of main power reducing techniques

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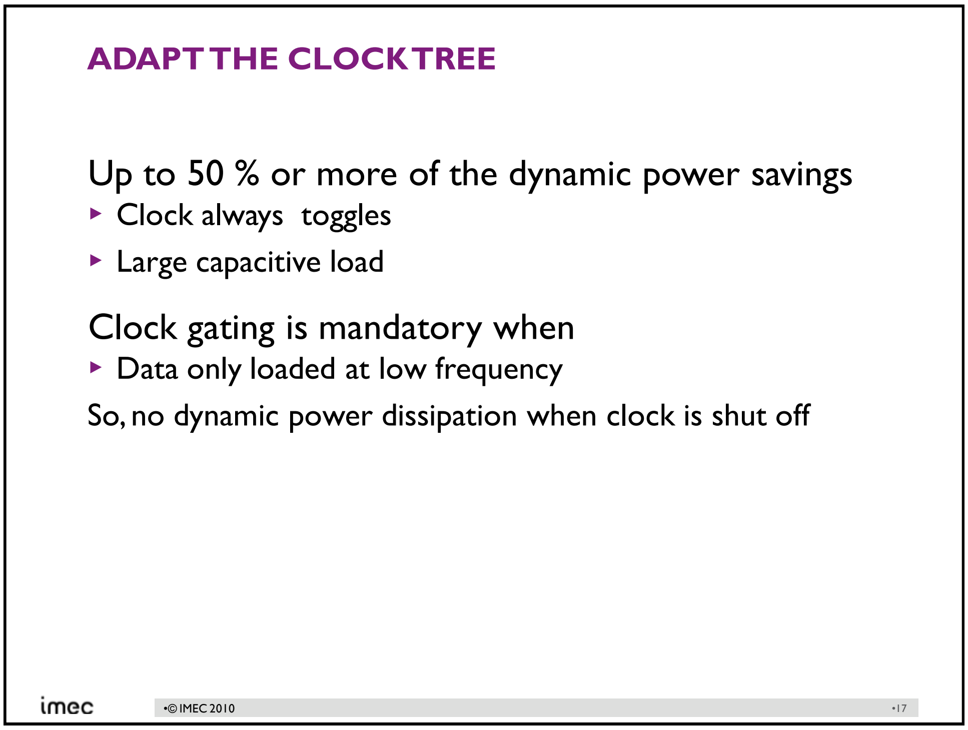

ADAPT THE CLOCK TREE

Up to 50 % or more of the dynamic power savings
- Clock always toggles
- Large capacitive load

Clock gating is mandatory when
- Data only loaded at low frequency

So, no dynamic power dissipation when clock is shut off

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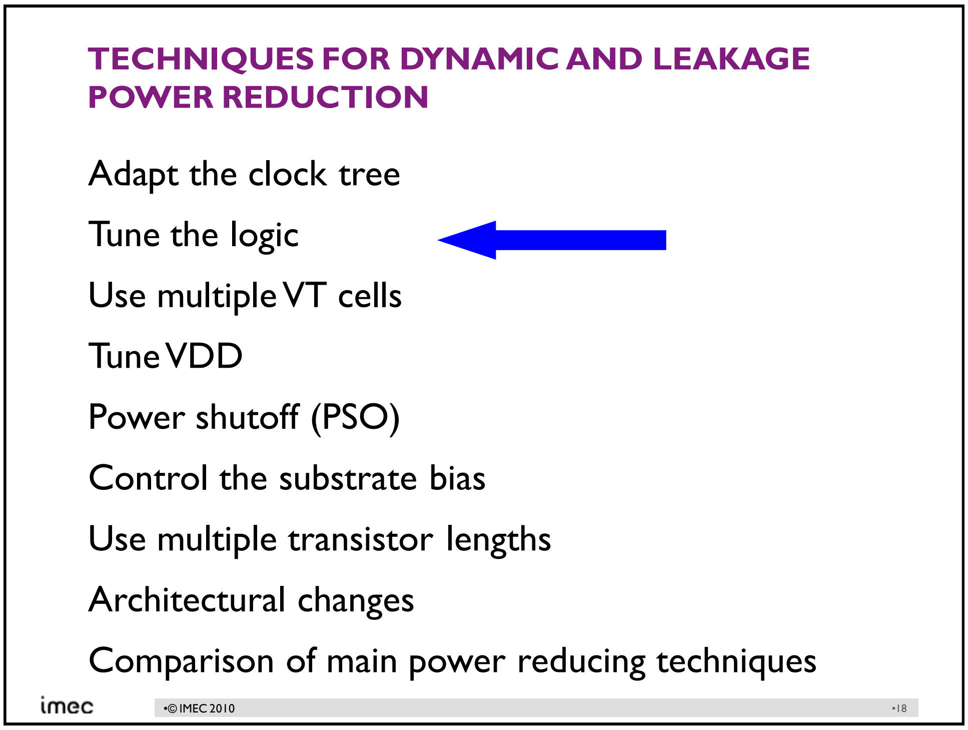

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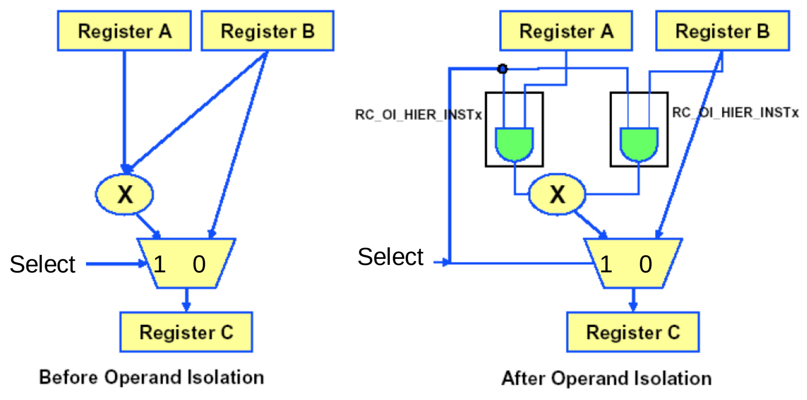
TUNE THE LOGIC

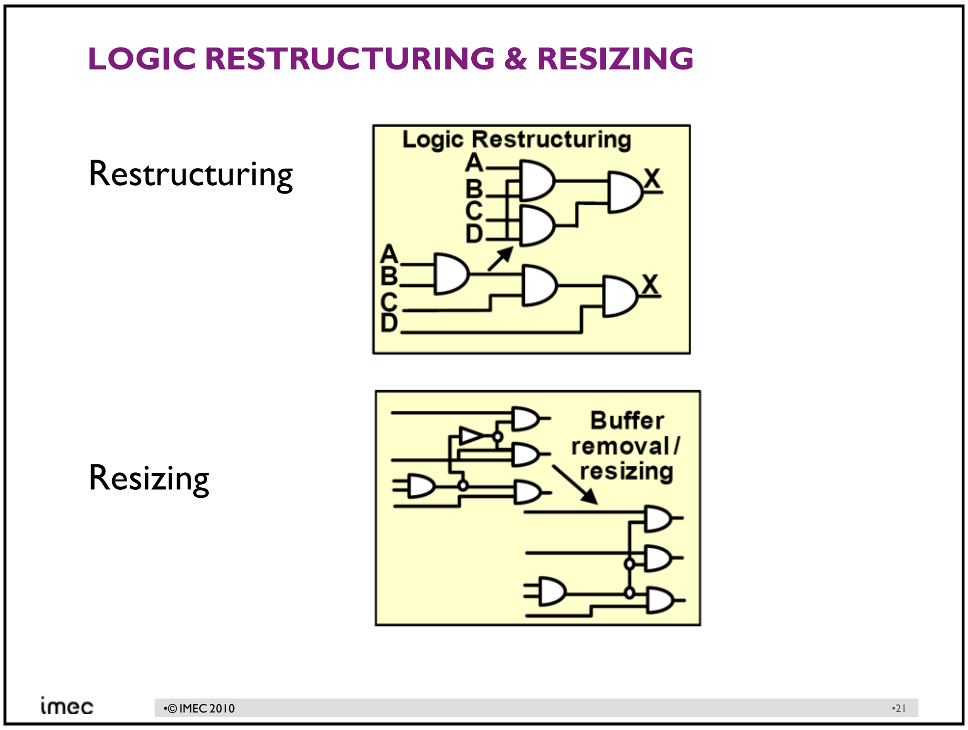
- Operand isolation
- Logic restructuring
- Logic resizing
- Transition rate buffering
- Pin swapping

} Reduce dynamic power

OPERAND ISOLATION

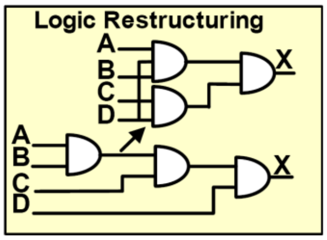


Select = 0
➔ unneeded power
when A changes

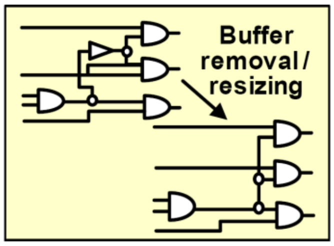


LOGIC RESTRUCTURING & RESIZING

Restructuring



Resizing



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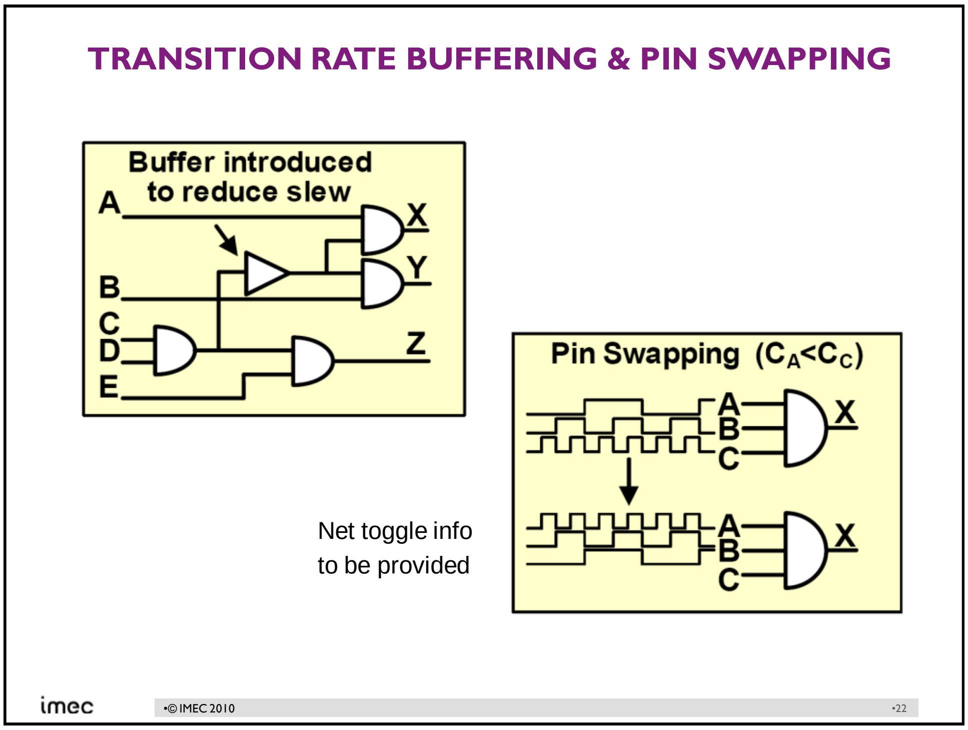
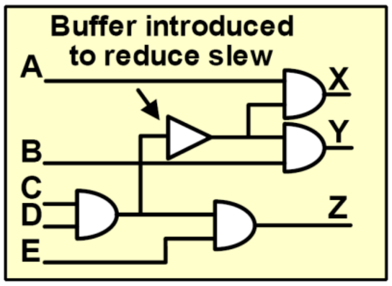
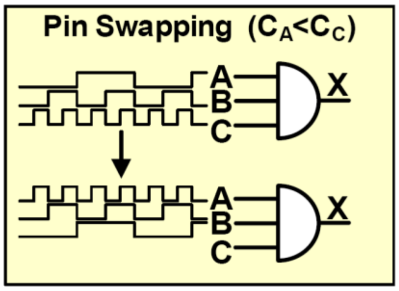


TRANSITION RATE BUFFERING & PIN SWAPPING





Net toggle info
to be provided

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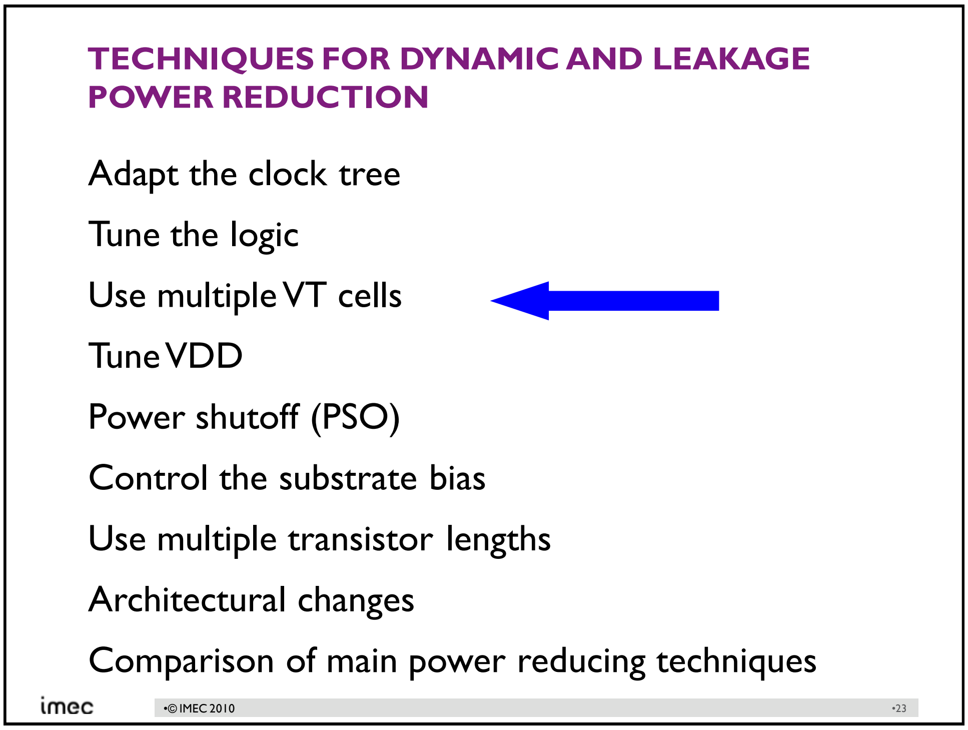

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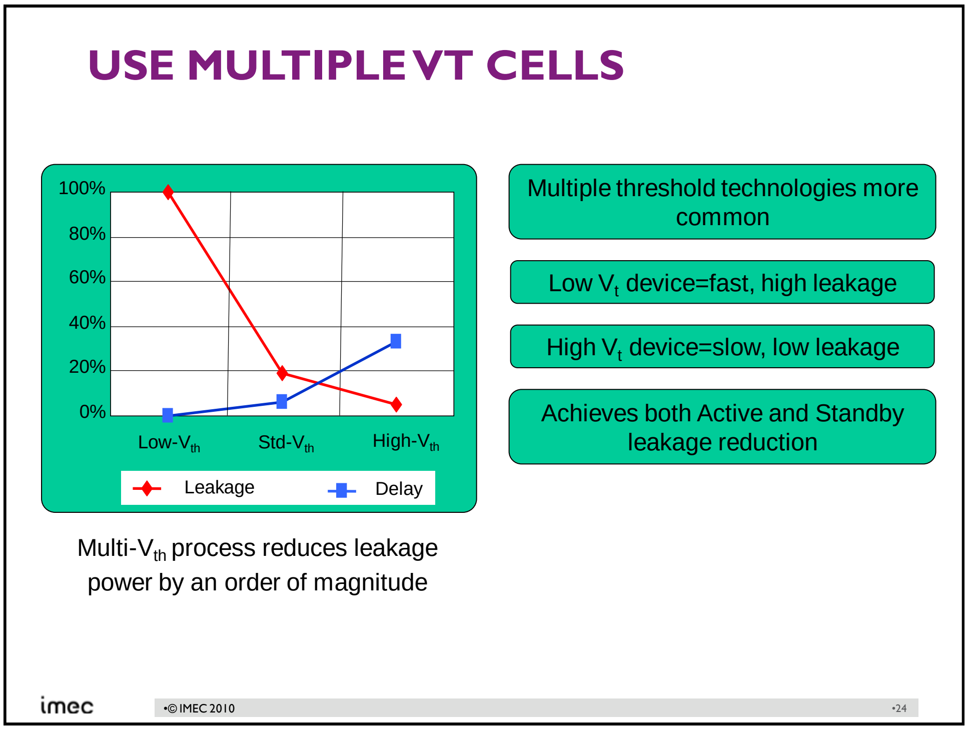
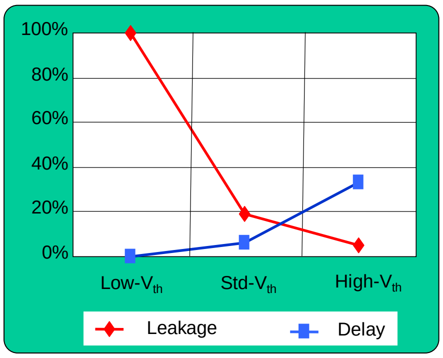


USE MULTIPLE VT CELLS



Multi-V_{th} process reduces leakage power by an order of magnitude

Multiple threshold technologies more common

Low V_t device=fast, high leakage

High V_t device=slow, low leakage

Achieves both Active and Standby leakage reduction

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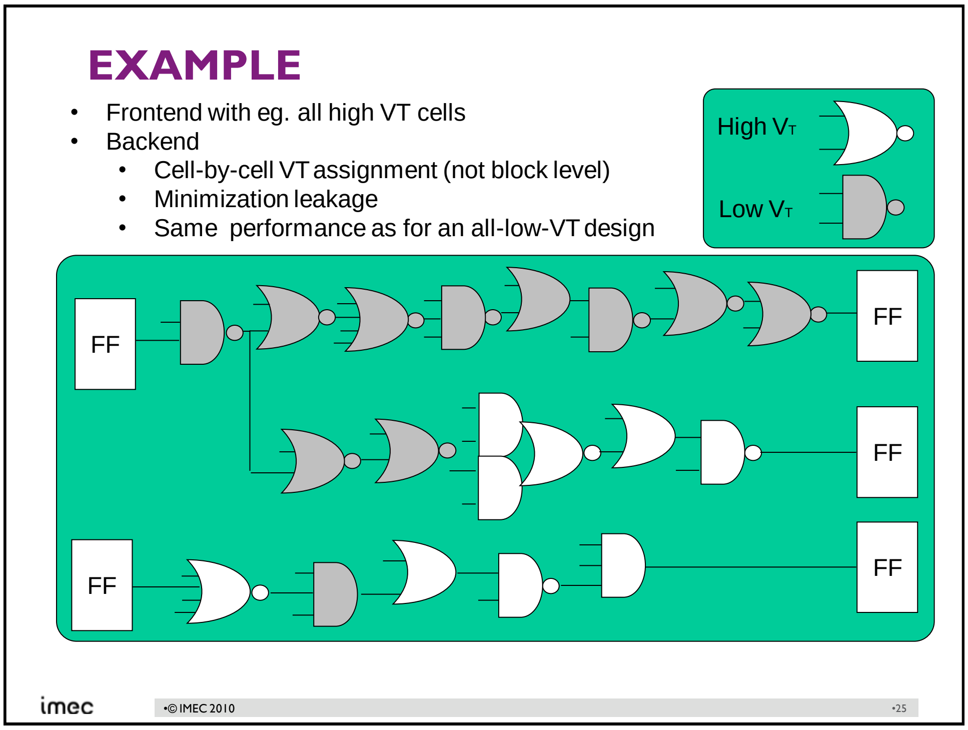
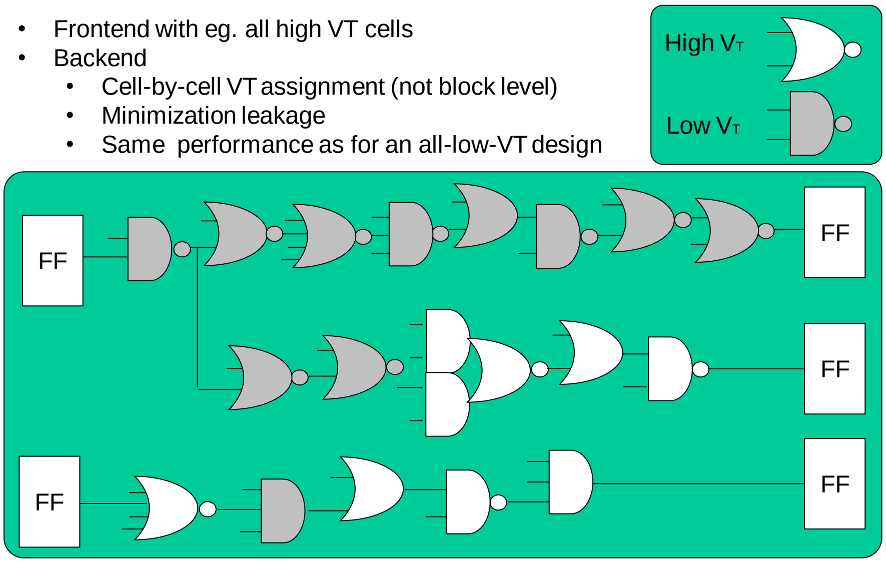
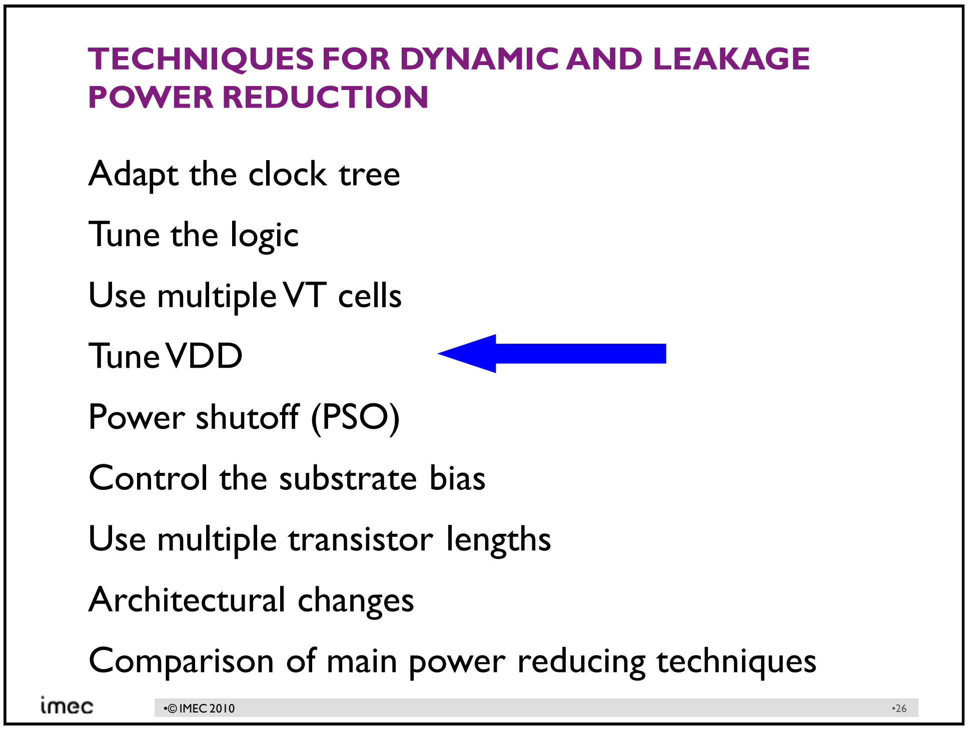


EXAMPLE

- Frontend with eg. all high VT cells
- Backend
  - Cell-by-cell VT assignment (not block level)
  - Minimization leakage
  - Same performance as for an all-low-VT design





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TUNE VDD

MSV (multi supply voltage) design

Dynamic voltage scaling

Dynamic voltage and frequency scaling

MSV (MULTI SUPPLY VOLTAGE) DESIGN

Reduce V when timing not critical
Increase V only when needed

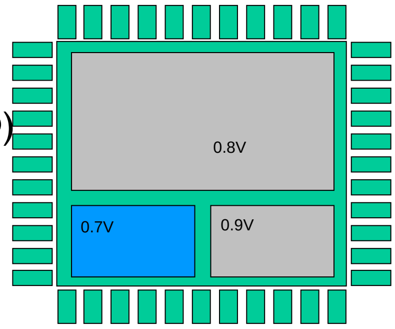
UMC 90 nm
Faraday libs: 1.0 – 1.2V

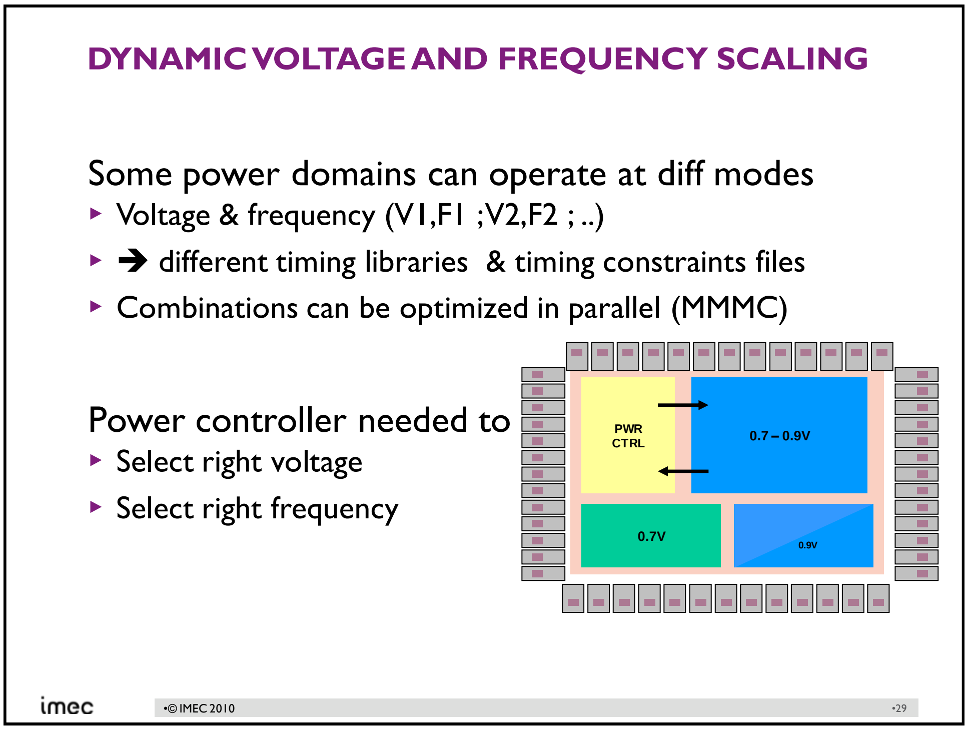
Multiple voltage domains

Assign different libraries to the domains(characterized for diff VDD)

Assign modules to the domains

Level shifter insertion

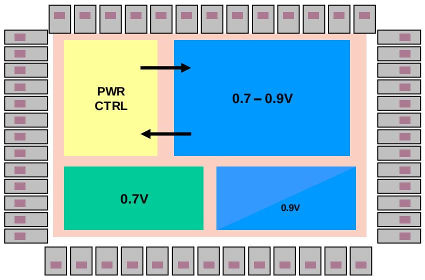




DYNAMIC VOLTAGE AND FREQUENCY SCALING

Some power domains can operate at diff modes
- Voltage & frequency (V1,F1 ;V2,F2 ; ..)
- ➔ different timing libraries & timing constraints files
- Combinations can be optimized in parallel (MMMC)

Power controller needed to
- Select right voltage
- Select right frequency



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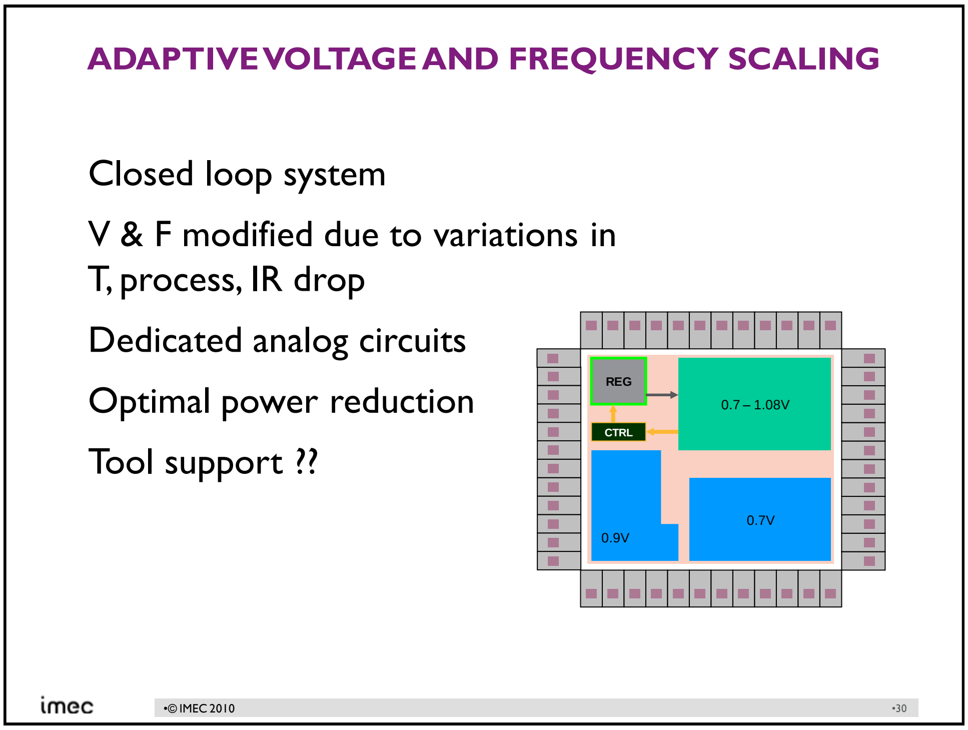


ADAPTIVE VOLTAGE AND FREQUENCY SCALING

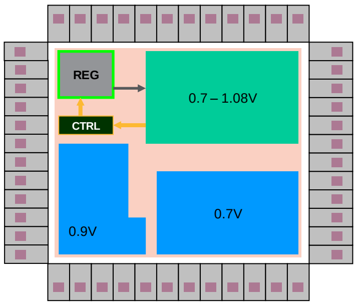
Closed loop system

V & F modified due to variations in T, process, IR drop

Dedicated analog circuits

Optimal power reduction

Tool support ??



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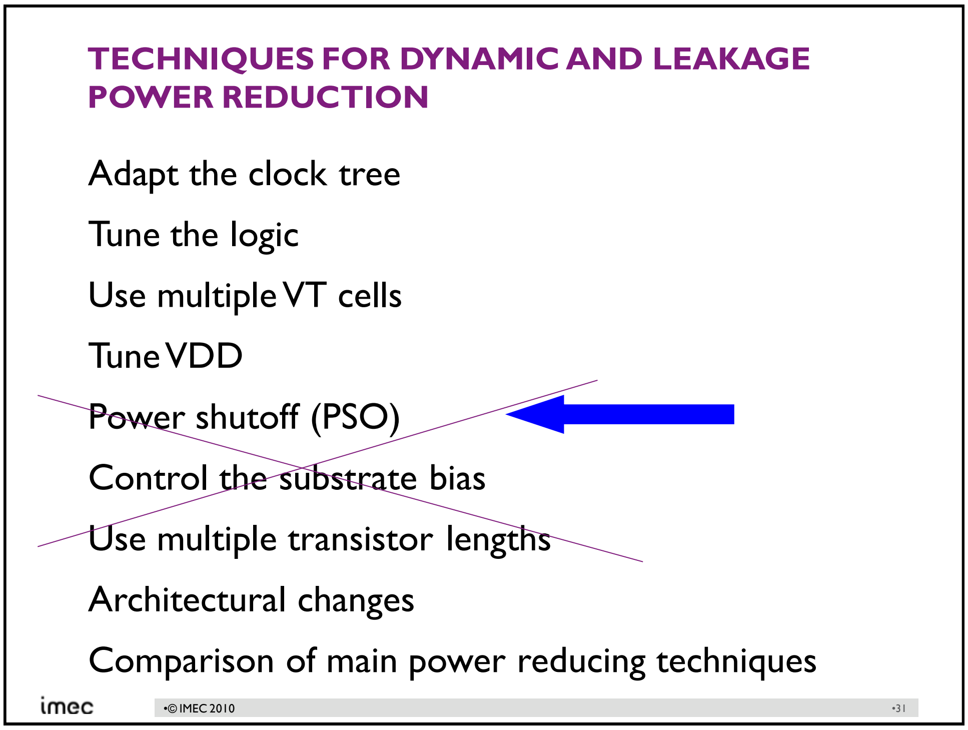

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Tune VDD

~~Power shutoff (PSO)~~

~~Control the substrate bias~~

~~Use multiple transistor lengths~~

Architectural changes

Comparison of main power reducing techniques

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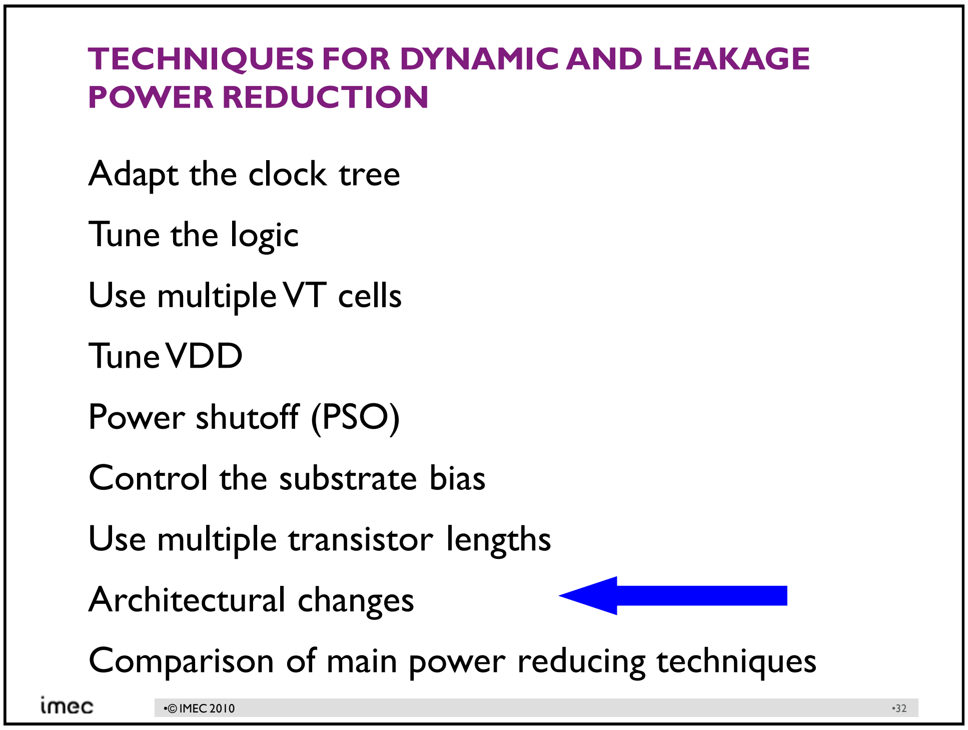

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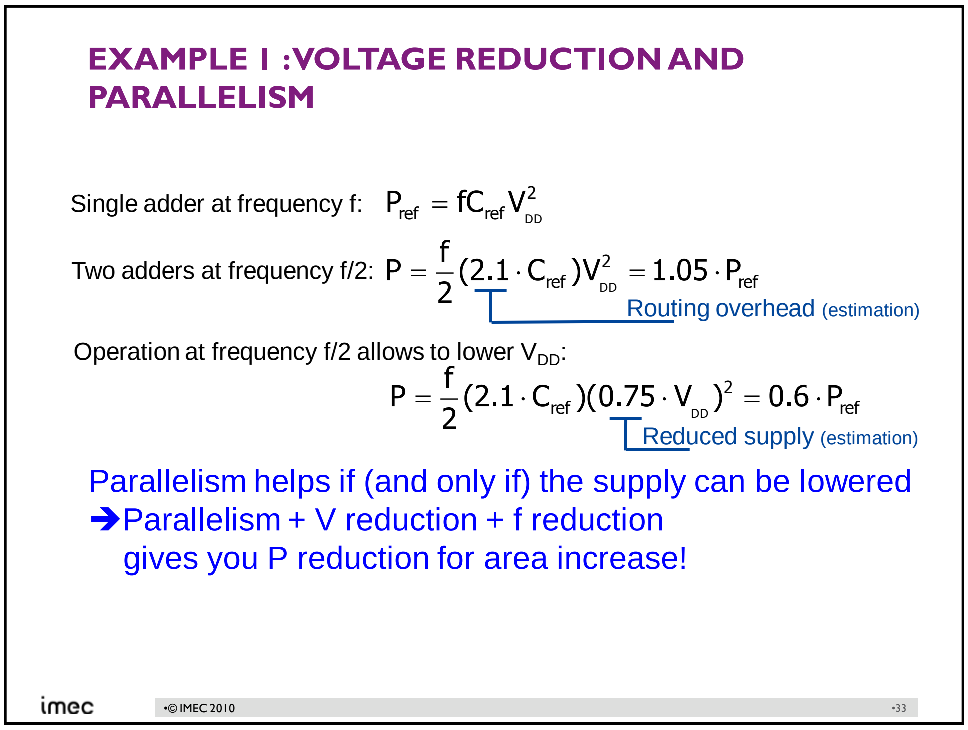

EXAMPLE 1 :VOLTAGE REDUCTION AND PARALLELISM

Single adder at frequency f: $P_{ref} = fC_{ref}V_{DD}^2$

Two adders at frequency f/2: $P = \frac{f}{2}(\underbrace{2.1}_{\text{Routing overhead (estimation)}} \cdot C_{ref})V_{DD}^2 = 1.05 \cdot P_{ref}$

Operation at frequency f/2 allows to lower V_{DD}:

$$P = \frac{f}{2}(2.1 \cdot C_{ref})(\underbrace{0.75}_{\text{Reduced supply (estimation)}} \cdot V_{DD})^2 = 0.6 \cdot P_{ref}$$

Parallelism helps if (and only if) the supply can be lowered
➔Parallelism + V reduction + f reduction
gives you P reduction for area increase!

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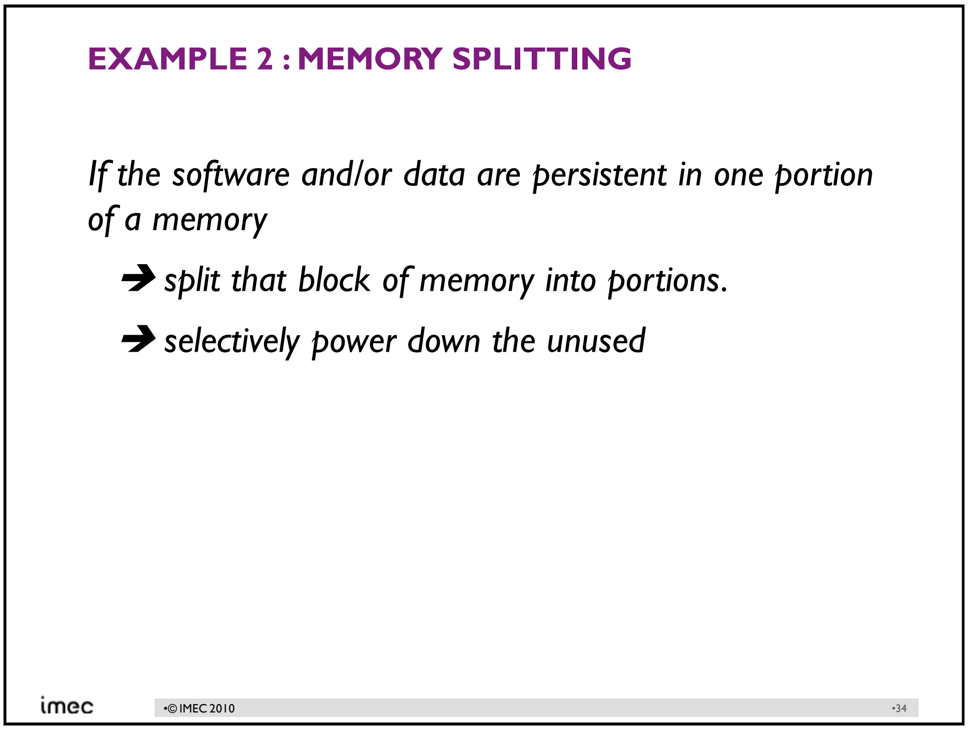

EXAMPLE 2 : MEMORY SPLITTING

If the software and/or data are persistent in one portion of a memory

➔ *split that block of memory into portions.*

➔ *selectively power down the unused*

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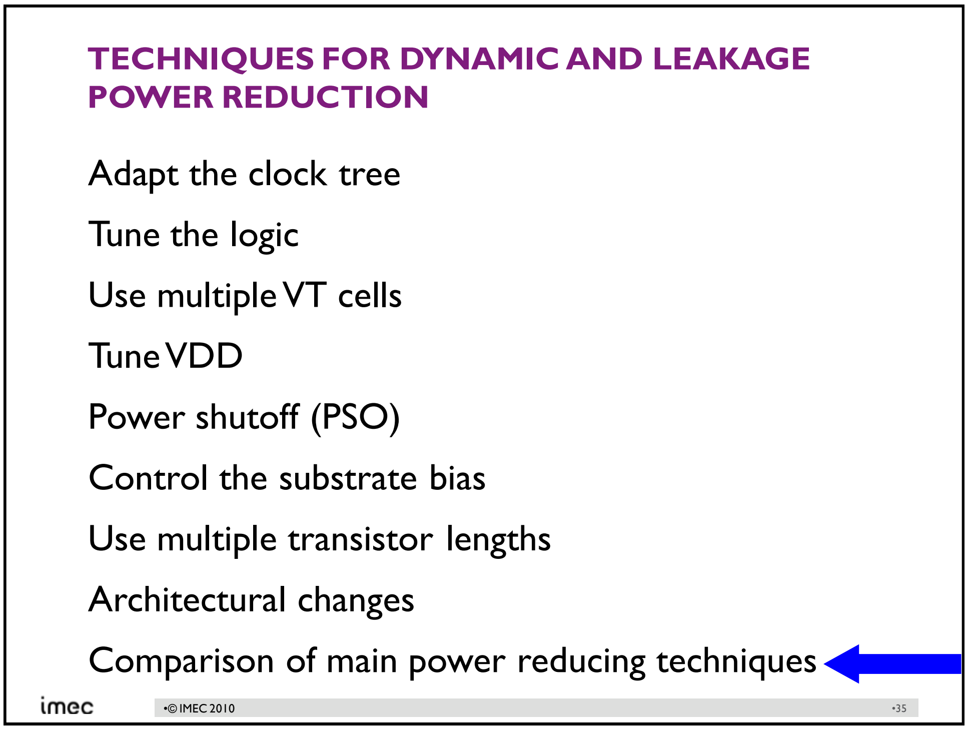

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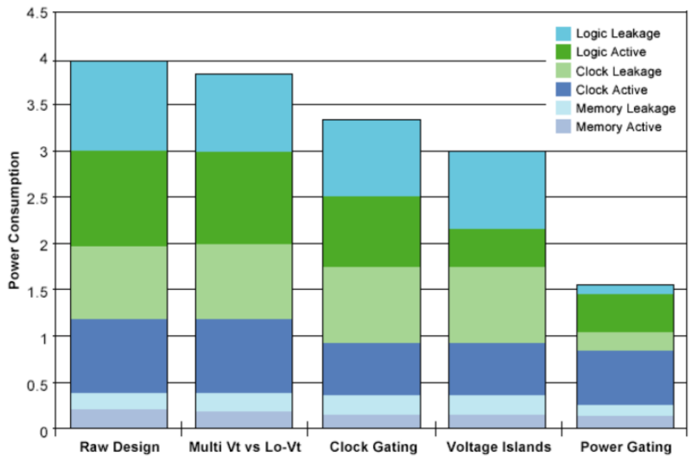
COMPARISON OF MAIN POWER REDUCING TECHNIQUES



Power reduction techniques. Courtesy Chip Design magazine, 2007

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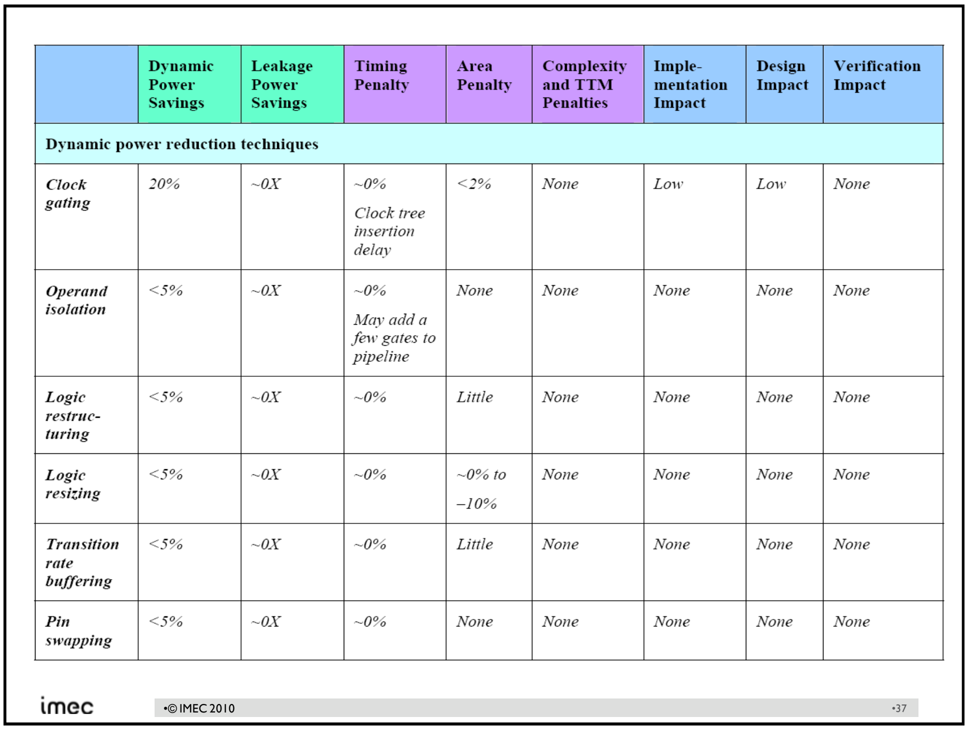

	Dynamic Power Savings	Leakage Power Savings	Timing Penalty	Area Penalty	Complexity and TTM Penalties	Imple-mentation Impact	Design Impact	Verification Impact
Dynamic power reduction techniques								
Clock gating	*20%*	*~0X*	*~0%* *Clock tree insertion delay*	*<2%*	*None*	*Low*	*Low*	*None*
Operand isolation	*<5%*	*~0X*	*~0%* *May add a few gates to pipeline*	*None*	*None*	*None*	*None*	*None*
Logic restruc-turing	*<5%*	*~0X*	*~0%*	*Little*	*None*	*None*	*None*	*None*
Logic resizing	*<5%*	*~0X*	*~0%*	*~0% to –10%*	*None*	*None*	*None*	*None*
Transition rate buffering	*<5%*	*~0X*	*~0%*	*Little*	*None*	*None*	*None*	*None*
Pin swapping	*<5%*	*~0X*	*~0%*	*None*	*None*	*None*	*None*	*None*

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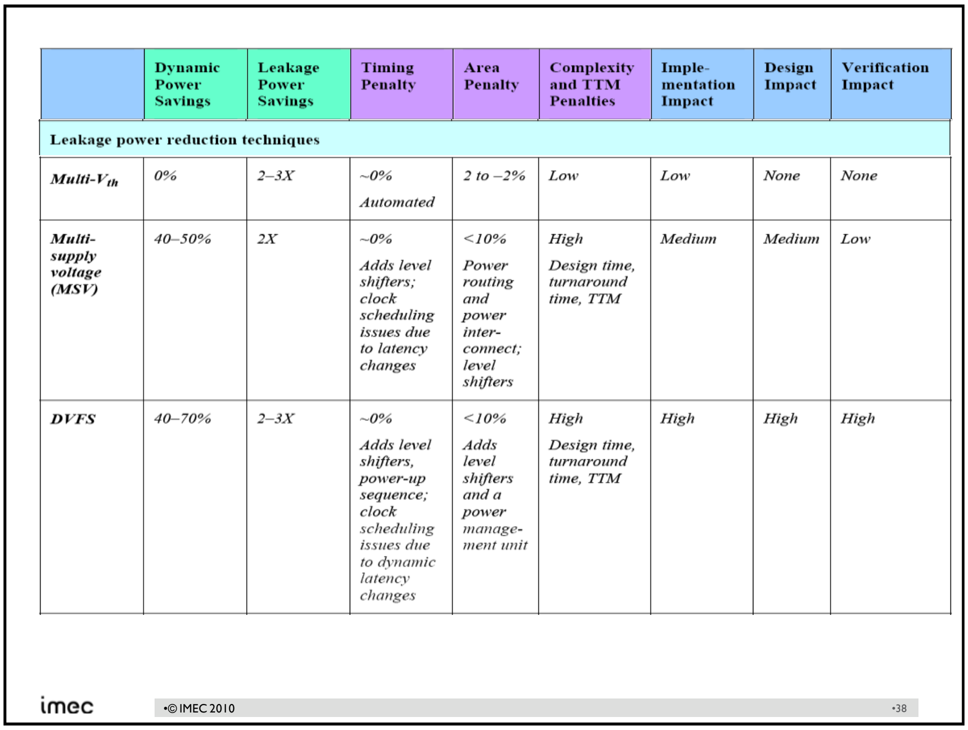

	Dynamic Power Savings	Leakage Power Savings	Timing Penalty	Area Penalty	Complexity and TTM Penalties	Imple-mentation Impact	Design Impact	Verification Impact
Leakage power reduction techniques								
Multi-V_{th}	*0%*	*2–3X*	*~0%* *Automated*	*2 to –2%*	*Low*	*Low*	*None*	*None*
Multi-supply voltage (MSV)	*40–50%*	*2X*	*~0%* *Adds level shifters; clock scheduling issues due to latency changes*	*<10%* *Power routing and power inter-connect; level shifters*	*High* *Design time, turnaround time, TTM*	*Medium*	*Medium*	*Low*
DVFS	*40–70%*	*2–3X*	*~0%* *Adds level shifters, power-up sequence; clock scheduling issues due to dynamic latency changes*	*<10%* *Adds level shifters and a power manage-ment unit*	*High* *Design time, turnaround time, TTM*	*High*	*High*	*High*

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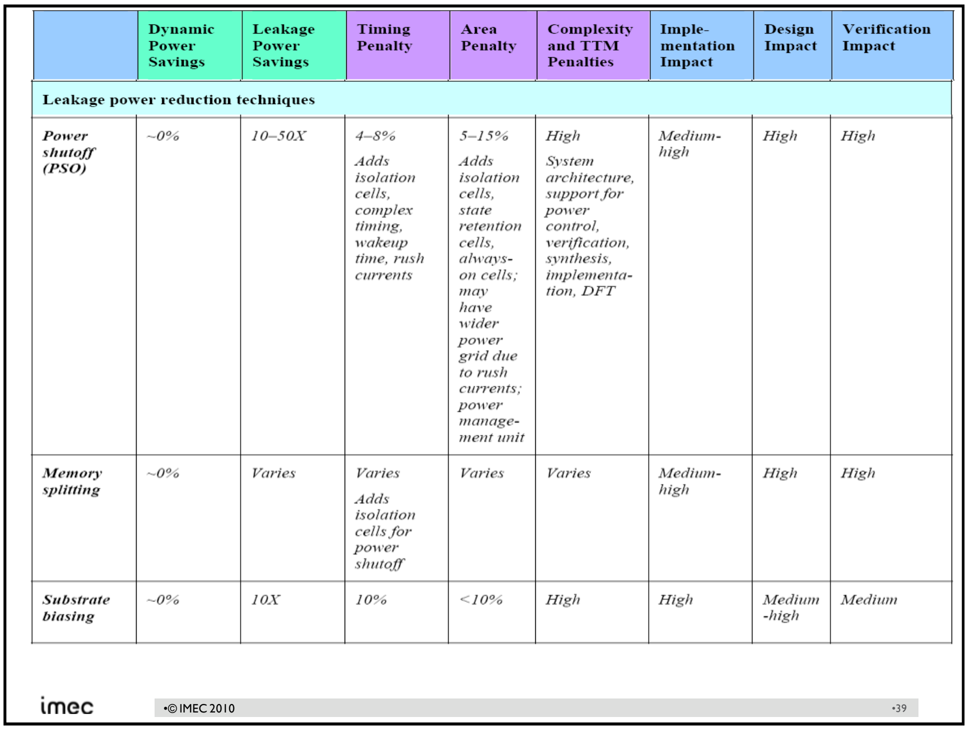

	Dynamic Power Savings	Leakage Power Savings	Timing Penalty	Area Penalty	Complexity and TTM Penalties	Imple-mentation Impact	Design Impact	Verification Impact
Leakage power reduction techniques								
Power shutoff (PSO)	*~0%*	*10–50X*	*4–8%* *Adds isolation cells, complex timing, wakeup time, rush currents*	*5–15%* *Adds isolation cells, state retention cells, always-on cells; may have wider power grid due to rush currents; power manage-ment unit*	*High* *System architecture, support for power control, verification, synthesis, implementa-tion, DFT*	*Medium-high*	*High*	*High*
Memory splitting	*~0%*	*Varies*	*Varies* *Adds isolation cells for power shutoff*	*Varies*	*Varies*	*Medium-high*	*High*	*High*
Substrate biasing	*~0%*	*10X*	*10%*	*<10%*	*High*	*High*	*Medium -high*	*Medium*

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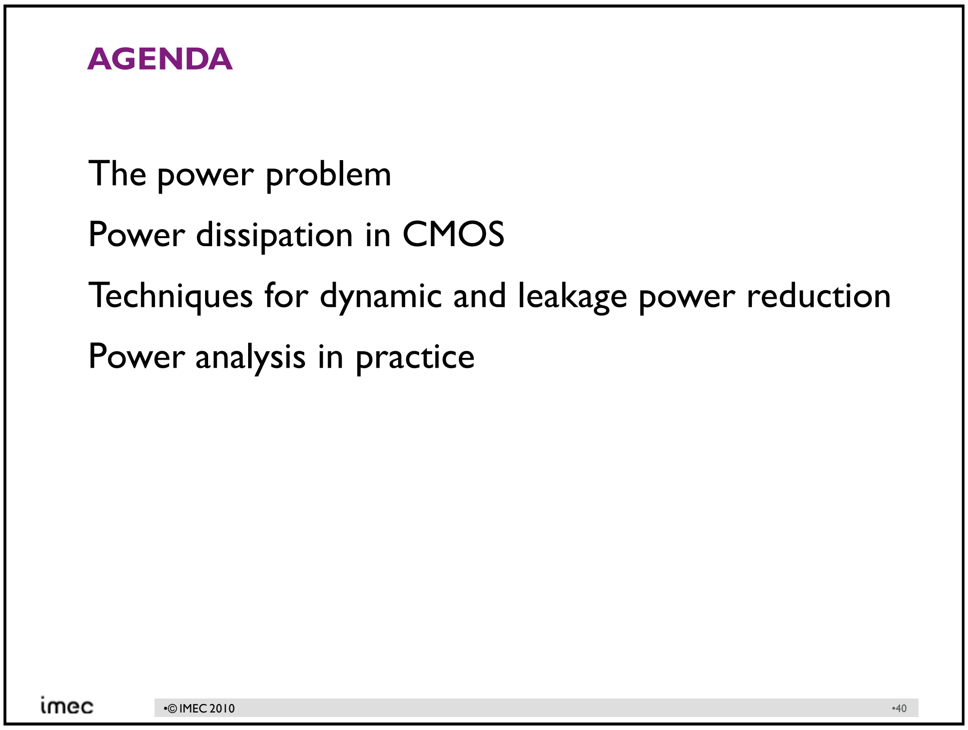

AGENDA

The power problem

Power dissipation in CMOS

Techniques for dynamic and leakage power reduction

Power analysis in practice

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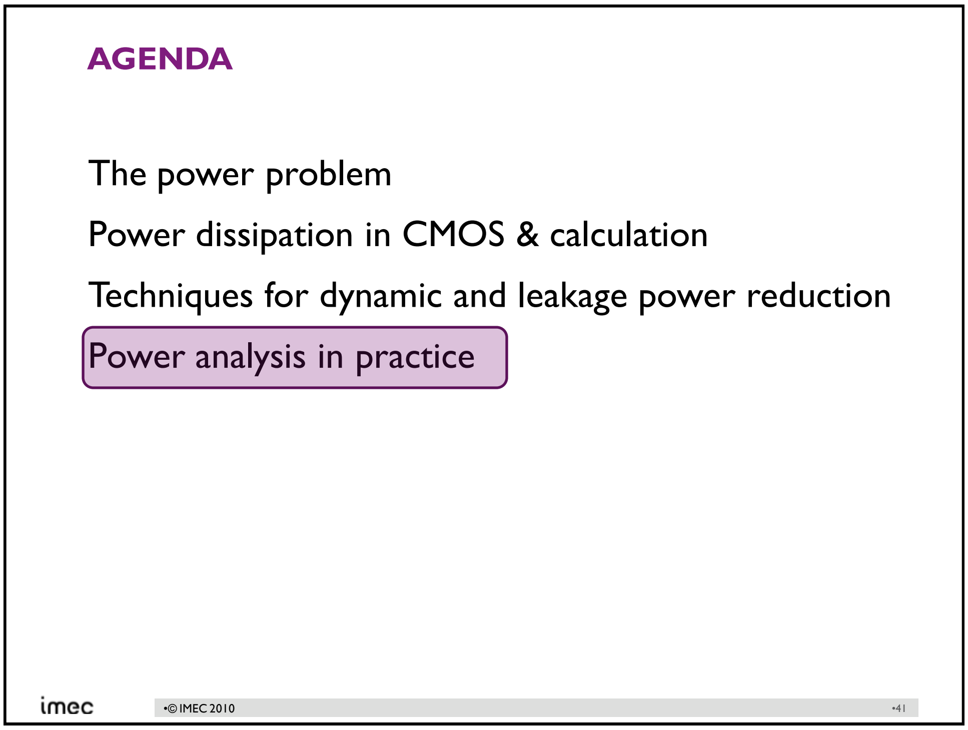

AGENDA

The power problem

Power dissipation in CMOS & calculation

Techniques for dynamic and leakage power reduction

Power analysis in practice

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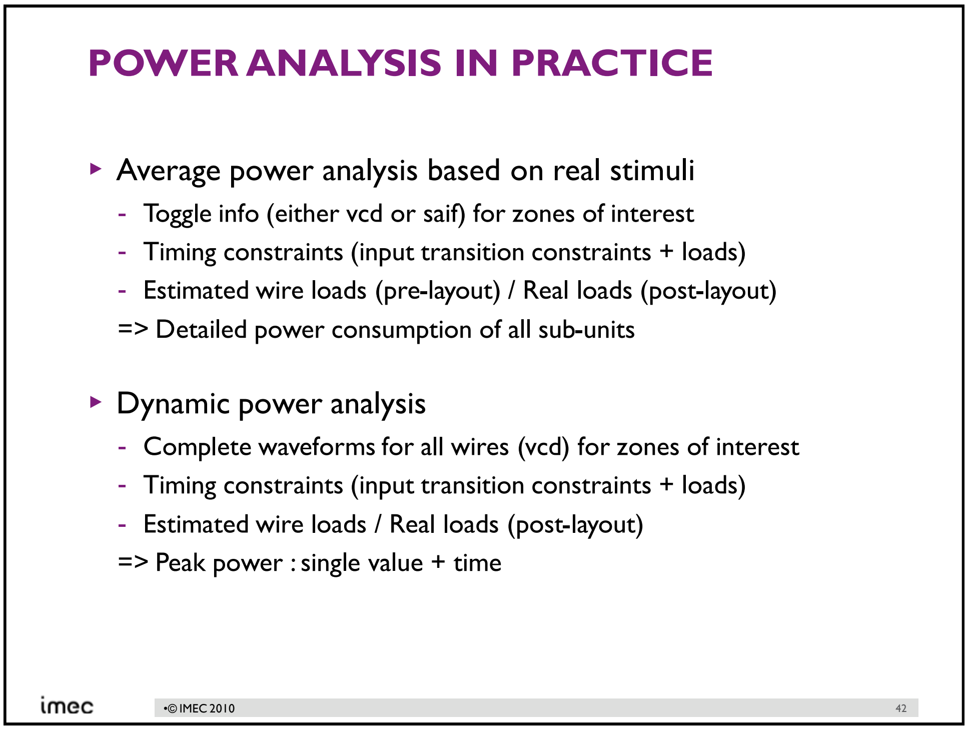

POWER ANALYSIS IN PRACTICE

- Average power analysis based on real stimuli
  - Toggle info (either vcd or saif) for zones of interest
  - Timing constraints (input transition constraints + loads)
  - Estimated wire loads (pre-layout) / Real loads (post-layout)

  => Detailed power consumption of all sub-units

- Dynamic power analysis
  - Complete waveforms for all wires (vcd) for zones of interest
  - Timing constraints (input transition constraints + loads)
  - Estimated wire loads / Real loads (post-layout)

  => Peak power : single value + time

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POWER ANALYSIS IN PRACTICE

Example of tools that may be used

- primetime : generate timing of the cells (=> sdf)
  based on input transitions and loads
- modelsim : simulate the testbenches (=> vcd)
  instantiating gate level netlist (+sdf)
- primetime-px : power analysis

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GENERATE TIMING OF CELLS (=> SDF)

Pre-layout problem :

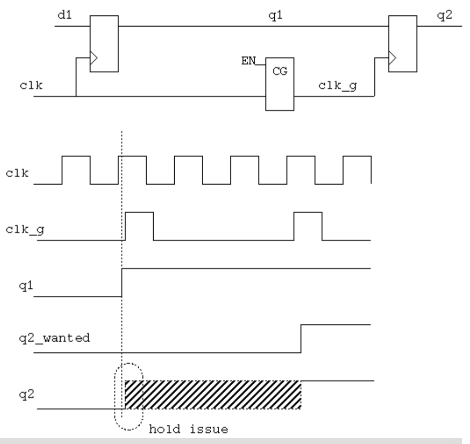
Non-balanced clock tree in the netlist

- Clock nets = ideal
- Clock gates(=delay)

⇒Possible hold time issues during simulation

⇒Propagation of X

⇒Useless vcd file



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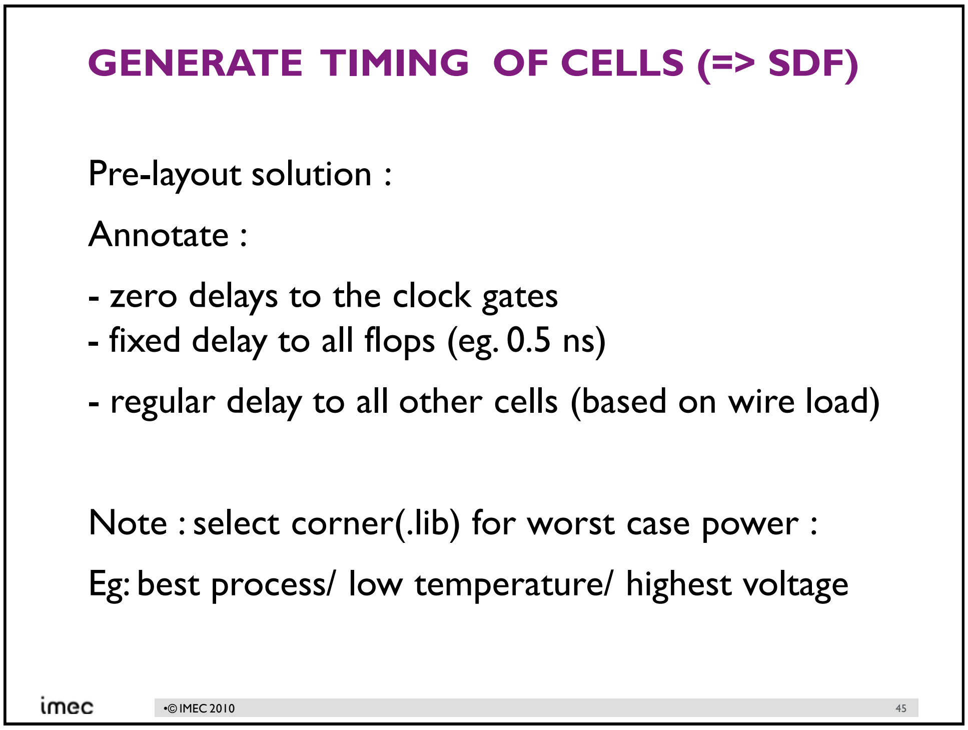

GENERATE TIMING OF CELLS (=> SDF)

Pre-layout solution :

Annotate :

- zero delays to the clock gates
- fixed delay to all flops (eg. 0.5 ns)
- regular delay to all other cells (based on wire load)

Note : select corner(.lib) for worst case power :

Eg: best process/ low temperature/ highest voltage

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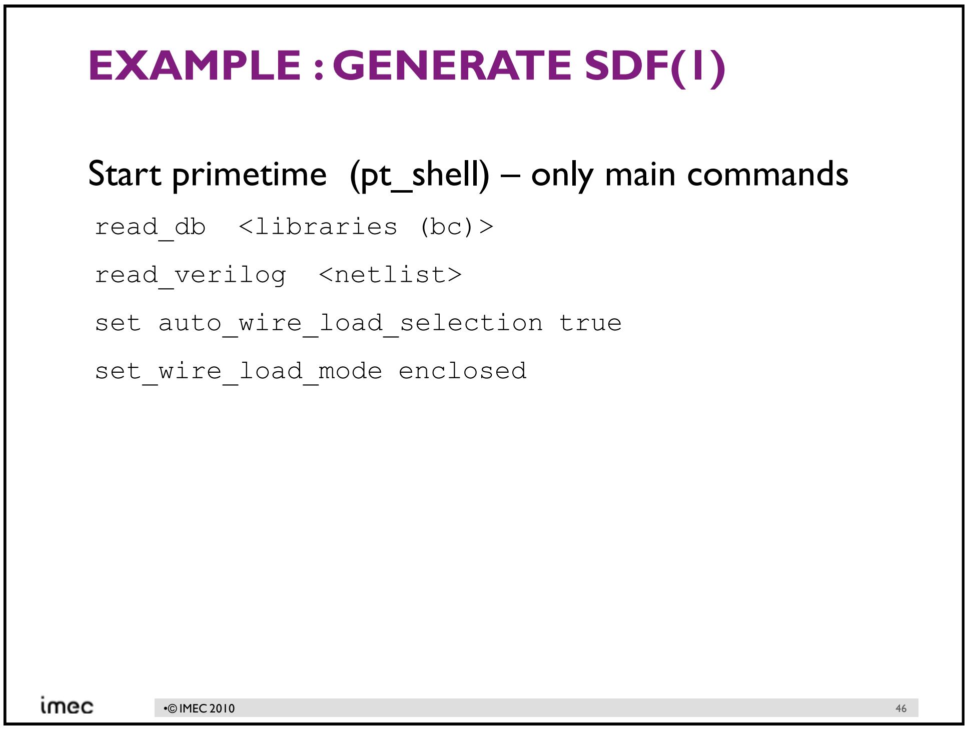

EXAMPLE : GENERATE SDF(1)

Start primetime (pt_shell) – only main commands

```
read_db  <libraries (bc)>
read_verilog  <netlist>
set auto_wire_load_selection true
set_wire_load_mode enclosed
```

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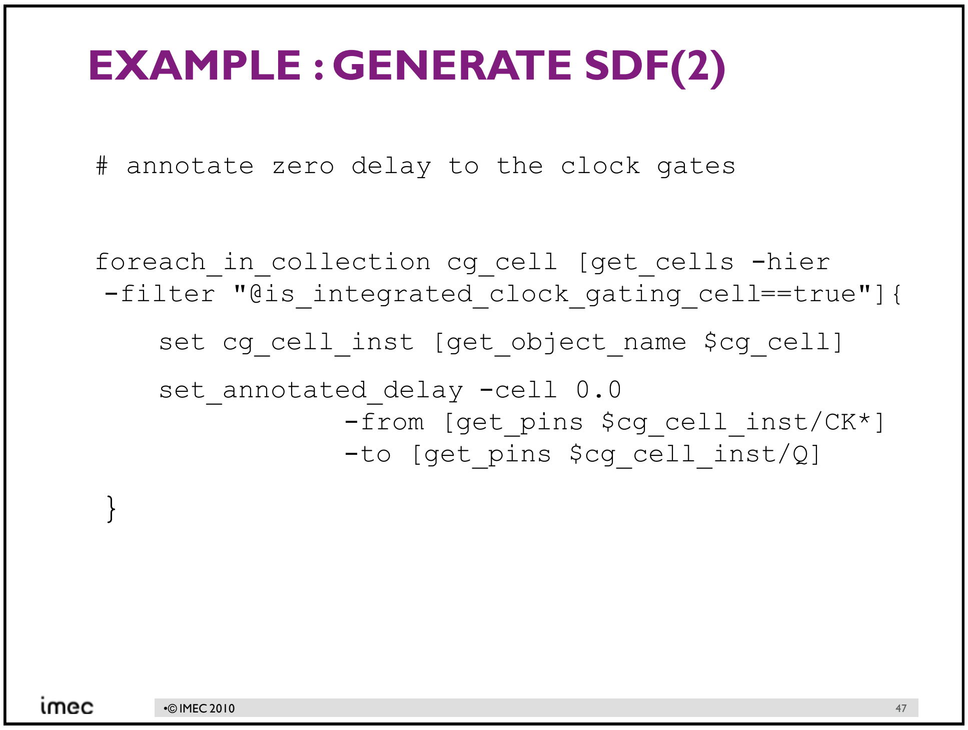

EXAMPLE : GENERATE SDF(2)

```
# annotate zero delay to the clock gates


foreach_in_collection cg_cell [get_cells -hier
 -filter "@is_integrated_clock_gating_cell==true"]{
    set cg_cell_inst [get_object_name $cg_cell]
    set_annotated_delay -cell 0.0
                 -from [get_pins $cg_cell_inst/CK*]
                 -to [get_pins $cg_cell_inst/Q]
 }
```

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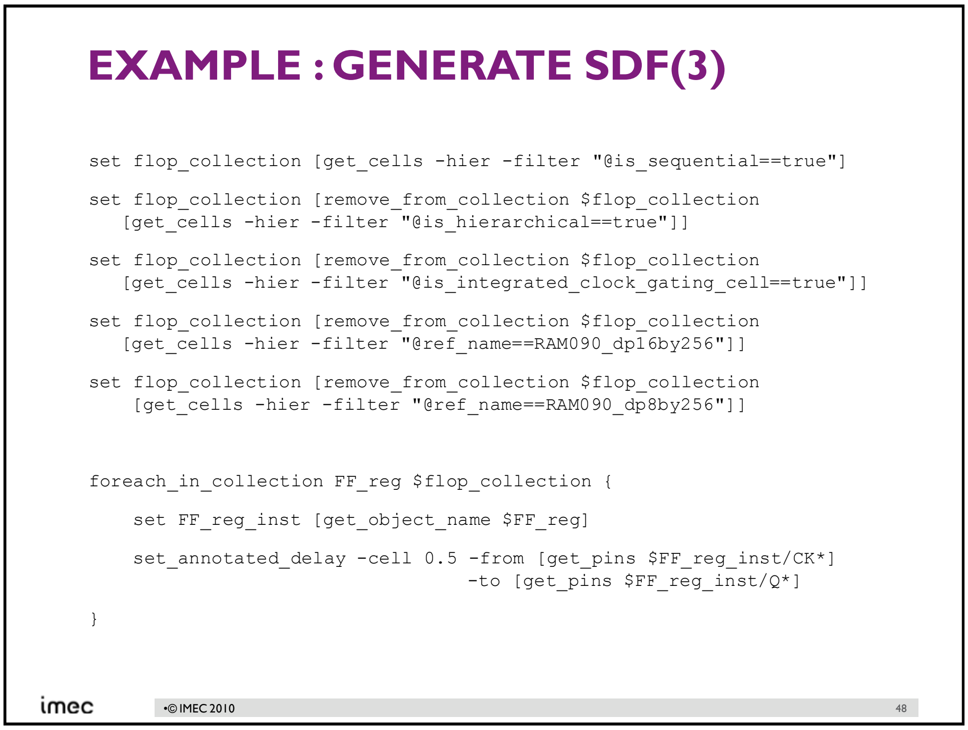

EXAMPLE : GENERATE SDF(3)

```
set flop_collection [get_cells -hier -filter "@is_sequential==true"]

set flop_collection [remove_from_collection $flop_collection
   [get_cells -hier -filter "@is_hierarchical==true"]]

set flop_collection [remove_from_collection $flop_collection
   [get_cells -hier -filter "@is_integrated_clock_gating_cell==true"]]

set flop_collection [remove_from_collection $flop_collection
   [get_cells -hier -filter "@ref_name==RAM090_dp16by256"]]

set flop_collection [remove_from_collection $flop_collection
    [get_cells -hier -filter "@ref_name==RAM090_dp8by256"]]


foreach_in_collection FF_reg $flop_collection {

    set FF_reg_inst [get_object_name $FF_reg]

    set_annotated_delay -cell 0.5 -from [get_pins $FF_reg_inst/CK*]
                                  -to [get_pins $FF_reg_inst/Q*]

}
```

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EXAMPLE : GENERATE SDF(3)

```
report_annotated_delay -list_annotated
write_sdf -context verilog
         -version 3.0
         ~~-include {SETUPHOLD RECREM}~~
    $SDF_DIR/${TopEntity}ZeroDelay0d5.sdf
```

```
...
(CELL
  (CELLTYPE "UYFNGA")
  (INSTANCE IObus_in_4_pad/U_inputpad_padlim)
  (DELAY
    (ABSOLUTE
    (CONDELSE (IOPATH I O (0.296::0.296) (0.320::0.320)))
    (CONDELSE (IOPATH IE O (1.249::1.249) (0.525::0.525)))
    (COND SMT==0  (IOPATH I O (0.296::0.296) (0.320::0.320)))
    (COND SMT==0  (IOPATH IE O (1.249::1.249) (0.525::0.525)))
     ......
```

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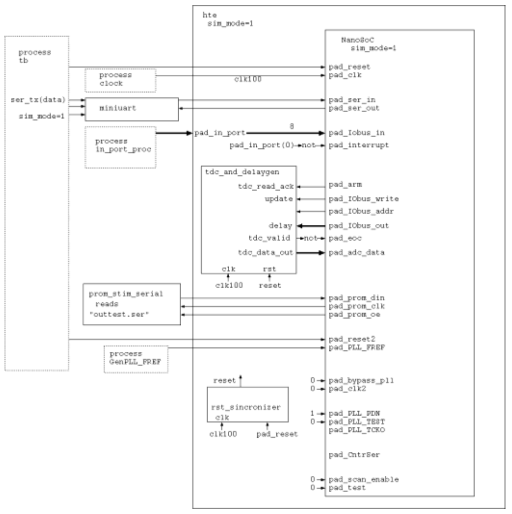
EXAMPLE : SIMULATION (1)

RTL

Top level testbench

Note : design was synthesized with generic sim_mode=1



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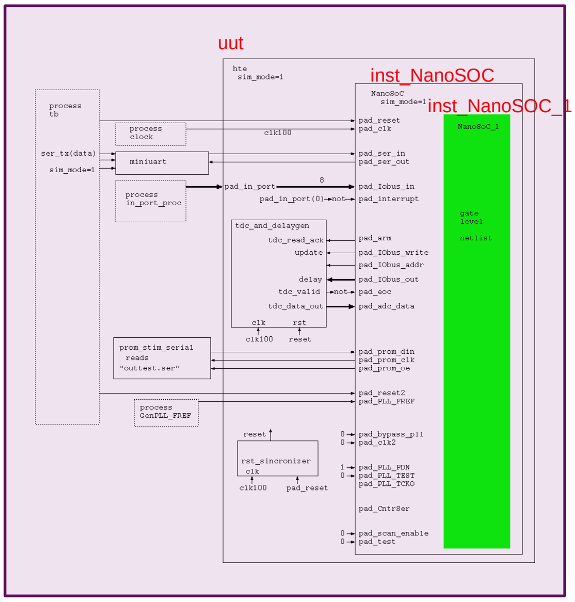
EXAMPLE : SIMULATION (2)

Extra level

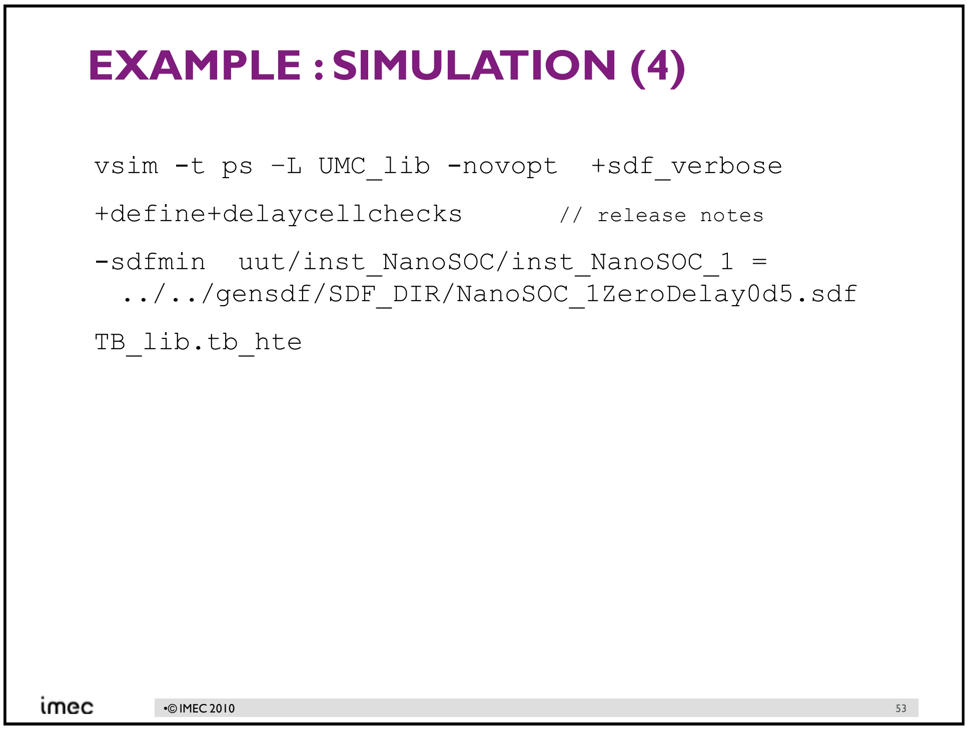
-Due to name change during synthesis



tb_hte

EXAMPLE : SIMULATION (3)

```
#compile verilog libraries & netlist
vlog  -work UMC_lib $UMC_CORE
vlog  -work UMC_lib $UMC_IOS
vlog  -work UMC_lib $UMC_RAM1
vlog  -work UMC_lib $UMC_RAM2
vlog  -work UMC_lib $UMC_PLL
vlog  -work NanoSoc_lib $NETLIST
#compile extra VHDL levels on top of NanoSOC_1 into NanoSoc_lib
vcom  -work NanoSoc_lib $TB/nanoSOC_gate_level.vhd
vcom  -work NanoSoc_lib $RTL/nanoSoc_package.vhd   # only component
#compile all VHDL testbench files into TB_lib
vcom  -work TB_lib $TB/tdc_and_delaygen.vhd
.....
vcom  -work TB_lib $TB/tb_hte.vhd
```



EXAMPLE : SIMULATION (4)

```
vsim -t ps –L UMC_lib -novopt  +sdf_verbose
+define+delaycellchecks       // release notes
-sdfmin  uut/inst_NanoSOC/inst_NanoSOC_1 =
  ../../gensdf/SDF_DIR/NanoSOC_1ZeroDelay0d5.sdf
TB_lib.tb_hte
```

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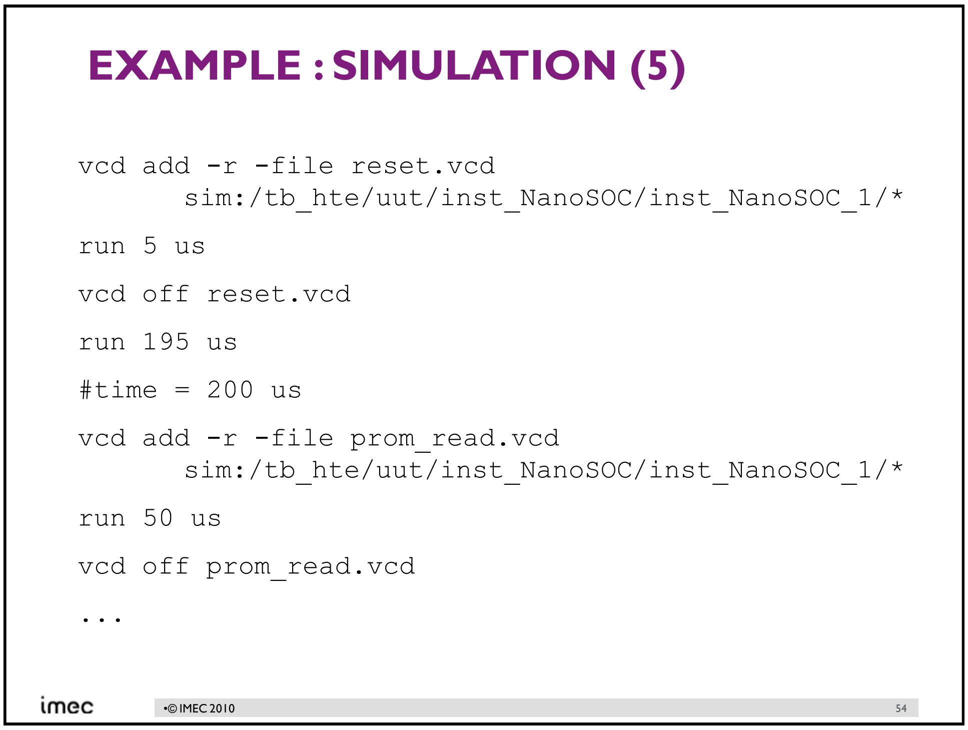

EXAMPLE : SIMULATION (5)

```
vcd add -r -file reset.vcd
        sim:/tb_hte/uut/inst_NanoSOC/inst_NanoSOC_1/*
run 5 us
vcd off reset.vcd
run 195 us
#time = 200 us
vcd add -r -file prom_read.vcd
        sim:/tb_hte/uut/inst_NanoSOC/inst_NanoSOC_1/*
run 50 us
vcd off prom_read.vcd
...
```

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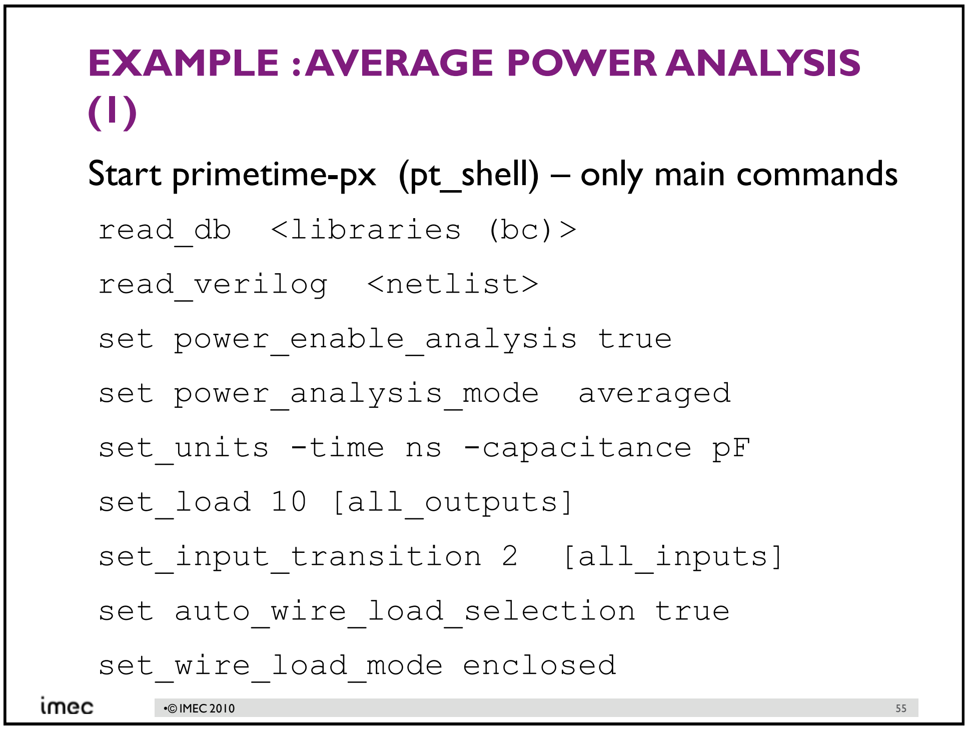

EXAMPLE :AVERAGE POWER ANALYSIS (1)

Start primetime-px (pt_shell) – only main commands

```
read_db  <libraries (bc)>
read_verilog  <netlist>
set power_enable_analysis true
set power_analysis_mode  averaged
set_units -time ns -capacitance pF
set_load 10 [all_outputs]
set_input_transition 2  [all_inputs]
set auto_wire_load_selection true
set_wire_load_mode enclosed
```

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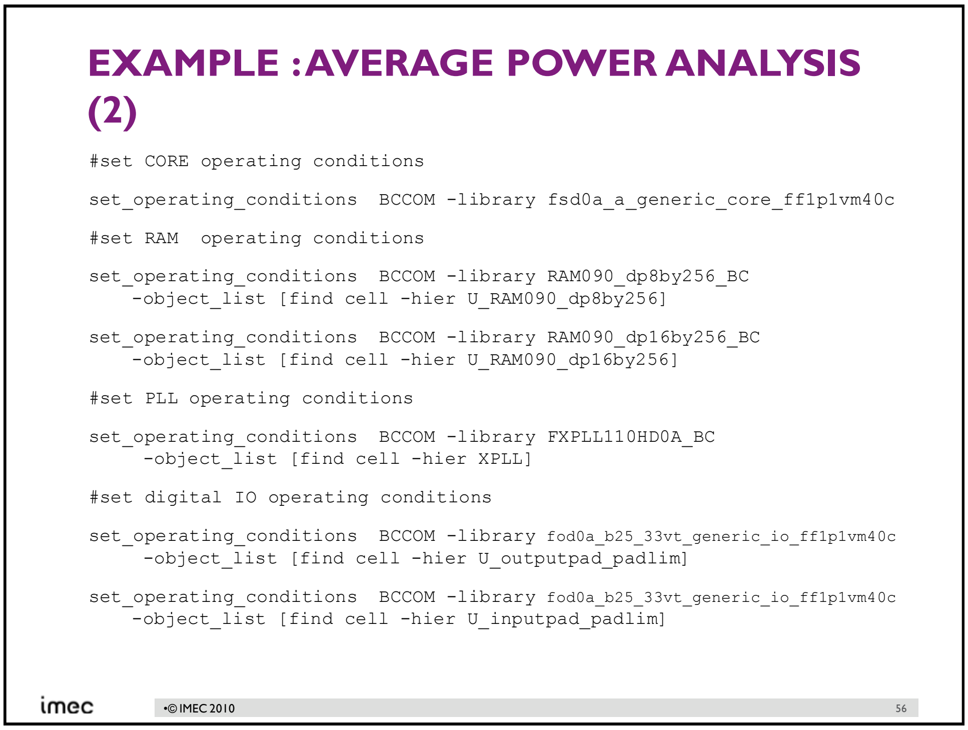

EXAMPLE :AVERAGE POWER ANALYSIS (2)

```
#set CORE operating conditions
set_operating_conditions  BCCOM -library fsd0a_a_generic_core_ff1p1vm40c
#set RAM  operating conditions
set_operating_conditions  BCCOM -library RAM090_dp8by256_BC
    -object_list [find cell -hier U_RAM090_dp8by256]
set_operating_conditions  BCCOM -library RAM090_dp16by256_BC
    -object_list [find cell -hier U_RAM090_dp16by256]
#set PLL operating conditions
set_operating_conditions  BCCOM -library FXPLL110HD0A_BC
     -object_list [find cell -hier XPLL]
#set digital IO operating conditions
set_operating_conditions  BCCOM -library fod0a_b25_33vt_generic_io_ff1p1vm40c
     -object_list [find cell -hier U_outputpad_padlim]
set_operating_conditions  BCCOM -library fod0a_b25_33vt_generic_io_ff1p1vm40c
    -object_list [find cell -hier U_inputpad_padlim]
```

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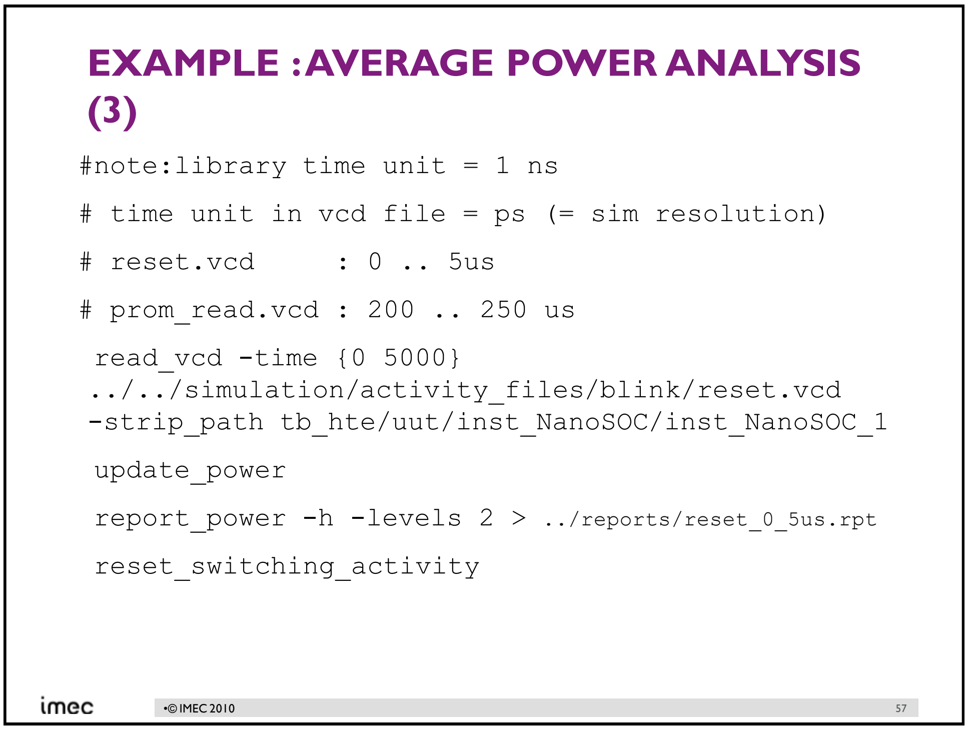

EXAMPLE :AVERAGE POWER ANALYSIS (3)

```
#note:library time unit = 1 ns
# time unit in vcd file = ps (= sim resolution)
# reset.vcd     : 0 .. 5us
# prom_read.vcd : 200 .. 250 us
 read_vcd -time {0 5000}
../../simulation/activity_files/blink/reset.vcd
-strip_path tb_hte/uut/inst_NanoSOC/inst_NanoSOC_1
 update_power
 report_power -h -levels 2 > ../reports/reset_0_5us.rpt
 reset_switching_activity
```

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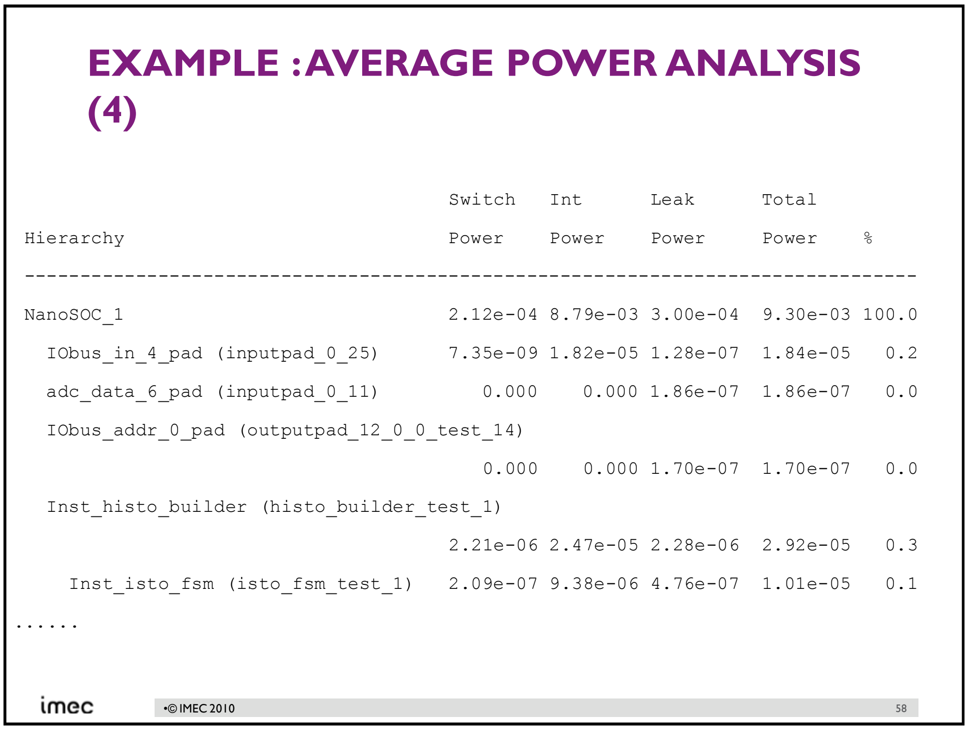

EXAMPLE :AVERAGE POWER ANALYSIS (4)

```
                                      Switch   Int      Leak      Total
Hierarchy                             Power    Power    Power     Power    %
--------------------------------------------------------------------------------
NanoSOC_1                             2.12e-04 8.79e-03 3.00e-04  9.30e-03 100.0
  IObus_in_4_pad (inputpad_0_25)      7.35e-09 1.82e-05 1.28e-07  1.84e-05   0.2
  adc_data_6_pad (inputpad_0_11)         0.000    0.000 1.86e-07  1.86e-07   0.0
  IObus_addr_0_pad (outputpad_12_0_0_test_14)
                                         0.000    0.000 1.70e-07  1.70e-07   0.0
  Inst_histo_builder (histo_builder_test_1)
                                      2.21e-06 2.47e-05 2.28e-06  2.92e-05   0.3
    Inst_isto_fsm (isto_fsm_test_1)   2.09e-07 9.38e-06 4.76e-07  1.01e-05   0.1
......
```

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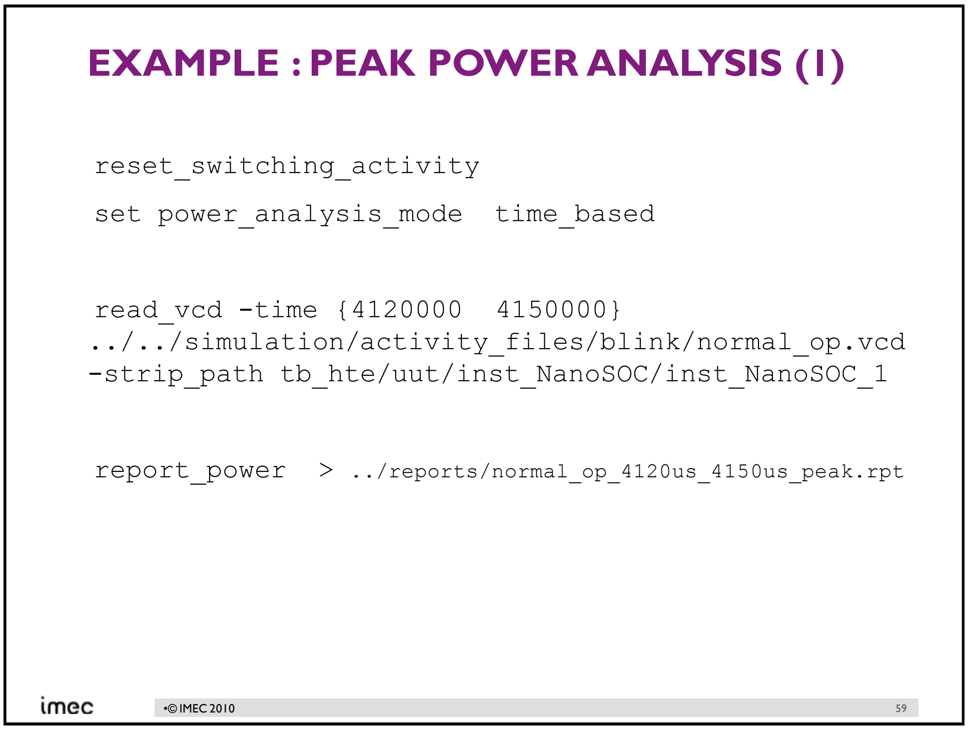

EXAMPLE : PEAK POWER ANALYSIS (1)

```
reset_switching_activity
set power_analysis_mode  time_based


read_vcd -time {4120000  4150000}
../../simulation/activity_files/blink/normal_op.vcd
-strip_path tb_hte/uut/inst_NanoSOC/inst_NanoSOC_1


report_power  > ../reports/normal_op_4120us_4150us_peak.rpt
```

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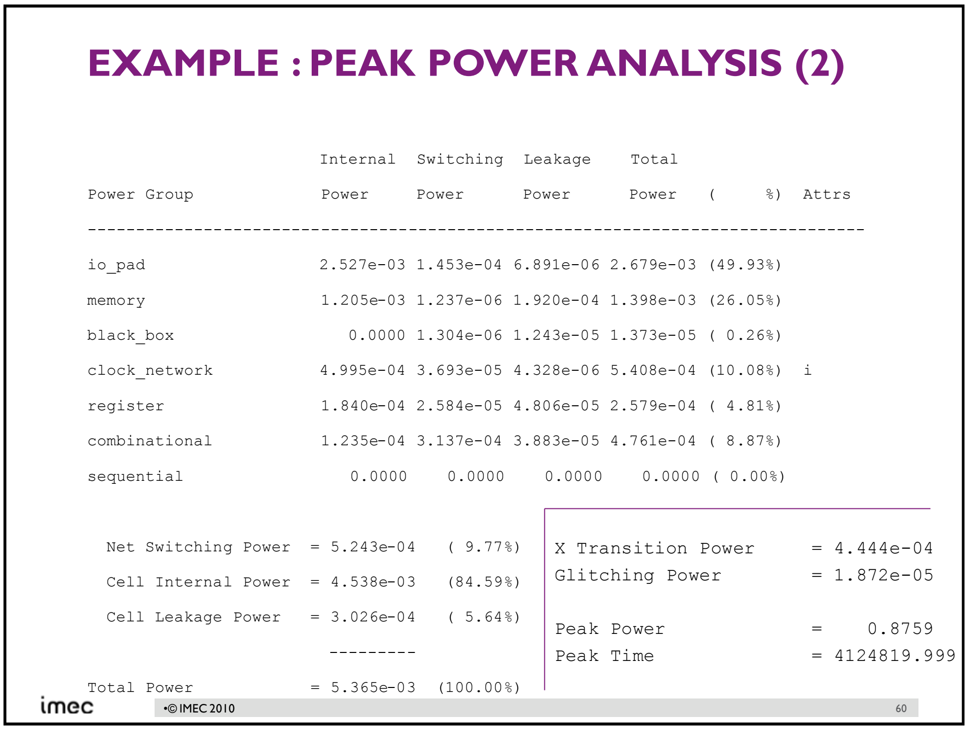

EXAMPLE : PEAK POWER ANALYSIS (2)

```
                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power    (     %)  Attrs
--------------------------------------------------------------------------------
io_pad                  2.527e-03 1.453e-04 6.891e-06 2.679e-03 (49.93%)
memory                  1.205e-03 1.237e-06 1.920e-04 1.398e-03 (26.05%)
black_box                  0.0000 1.304e-06 1.243e-05 1.373e-05 ( 0.26%)
clock_network           4.995e-04 3.693e-05 4.328e-06 5.408e-04 (10.08%)  i
register                1.840e-04 2.584e-05 4.806e-05 2.579e-04 ( 4.81%)
combinational           1.235e-04 3.137e-04 3.883e-05 4.761e-04 ( 8.87%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)


  Net Switching Power  = 5.243e-04   ( 9.77%)
  Cell Internal Power  = 4.538e-03   (84.59%)
  Cell Leakage Power   = 3.026e-04   ( 5.64%)
                         ---------
Total Power            = 5.365e-03  (100.00%)
```

```
X Transition Power      = 4.444e-04
Glitching Power         = 1.872e-05

Peak Power              =    0.8759
Peak Time               = 4124819.999
```

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