





ASIC packaging in ceramic

- Introduction
- Difference plastic/ceramic
- Overview ceramic packages
- Wirebonding techniques
- Practical rules

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Introduction

- Why is a package needed?
 - Protection of silicon against hostile environment (humidity, scratches, dust, human handling,...)
 - Simplify connection of silicon to the outside world.
 - Heat removal
- Package is important in determining:
 - size of the component.
 - price of final component.
 - overall performance.
- Packaging is a dynamic technique, fully in development.

Introduction

- Package classification:
 1. Board mounting: "Through-hole" versus "Surface mount" (SMD).
 2. Pin/lead configuration: "Area array" versus "outline pins".
 3. Material: "Ceramic" versus "Plastic".
 4. Assembly techniques. (glob-top, flip-chip,...)

Focus on Ceramic assembly.



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Difference plastic/ceramic

Plastic	Ceramic
Package itself is molded after wirebonding	Empty package with cavity
Production (1k.. >1M pcs.)	Prototyping (10..100 pcs.)
Porous structure	Hermetic (used in space)
Aggressive pad-pitch (35um)	Conservative pad-pitch (typical 90um, down to 45um)
Strict assembly rules (wafer thickness,...)	Flexible assembly rules
Variety in pin counts (2..1000)	Limited pin counts (max. ~ 476)
Automated flow	Manual flow
NRE: ~ \$2k..\$20k Unit: ~ \$0.5..\$5	NRE:none Unit: ~\$15..\$150

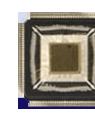
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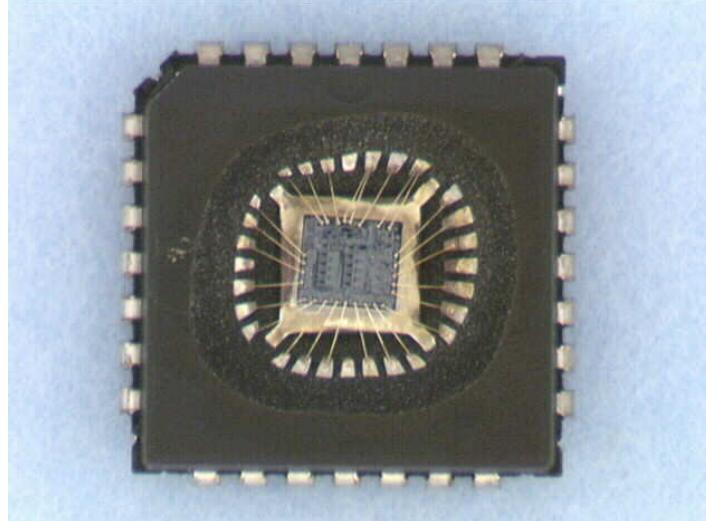


Difference plastic/ceramic

- Special case: Open-Cavity package.
 - What?
 - Newly molded or etched?
- ✓ Pro:
 - same package for prototyping and volume product.
 - Prototyping quantities.
 - Reasonable pricing (NRE ~\$500 + ~\$50/pcs.).
- ✗ Contra:
 - Difficult for wirebonding
 - Typically only for small pin counts.
 - Difficult/impossible to access silicon
(visual check of wiring and measurements on-silicon).



Difference plastic/ceramic



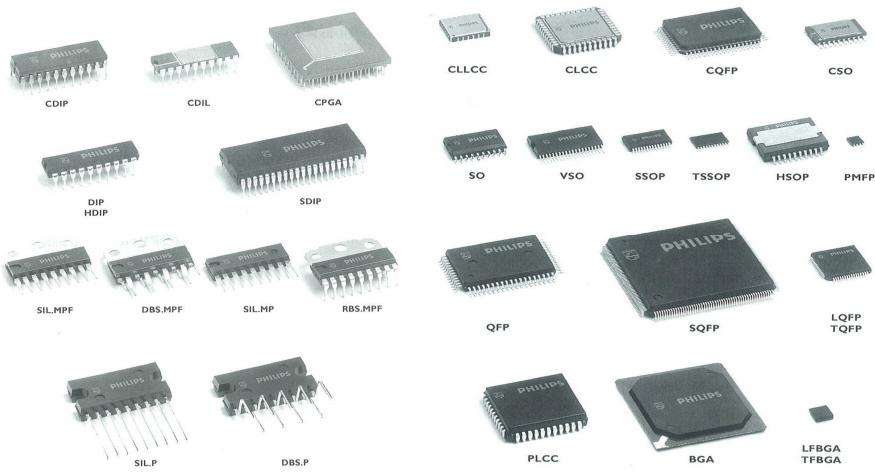


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Overview ceramic packages

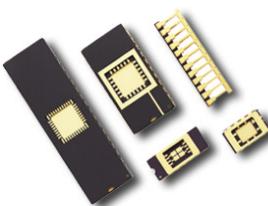
Examples of ceramic and plastic packages:



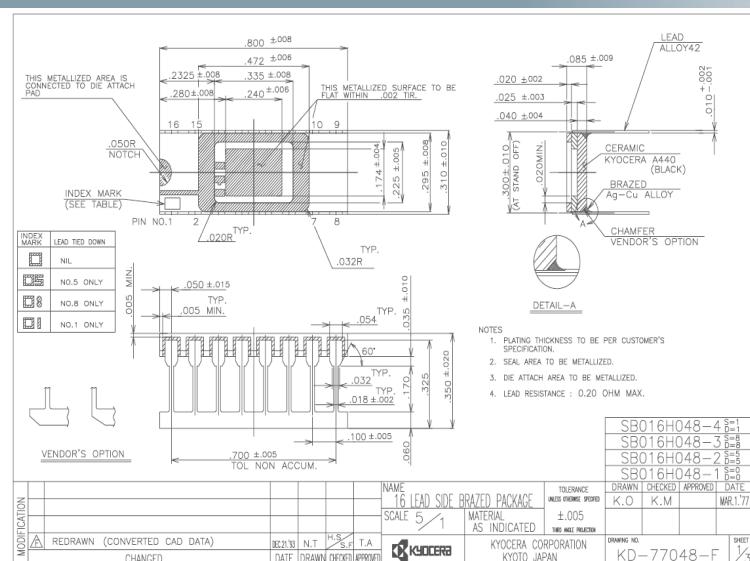


Overview ceramic packages

- **DIL (DIP) = Dual In Line Package**
 - Oldest package available. Example: opamp, TTL,...
 - Exist in 2 different widths: .300mil and .600mil (1 mil=25.4mm)
 - Through-Hole type
 - ✓ Cheap.
 - ✓ Easy to handle and mount on a pcb.
 - ✓ Socket is easy to find.
 - ✓ Mechanically strong.
 - ✗ Limited pin-count (max. 48 pins).
 - ✗ Pin-trace length not equal for all leads.

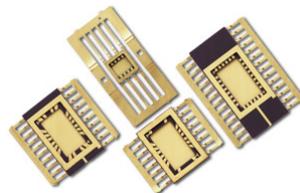


Overview ceramic packages



Overview ceramic packages

- **CSOIC** = Ceramic Small Outline IC
 - Surface mount (SMD).
 - ✓ Footprint compatible with plastic SOIC.
 - ✗ Currently only manufactured in 16, 20, 24, 28, 30 lead configurations.
 - ✗ Pin-trace length not equal for all leads.

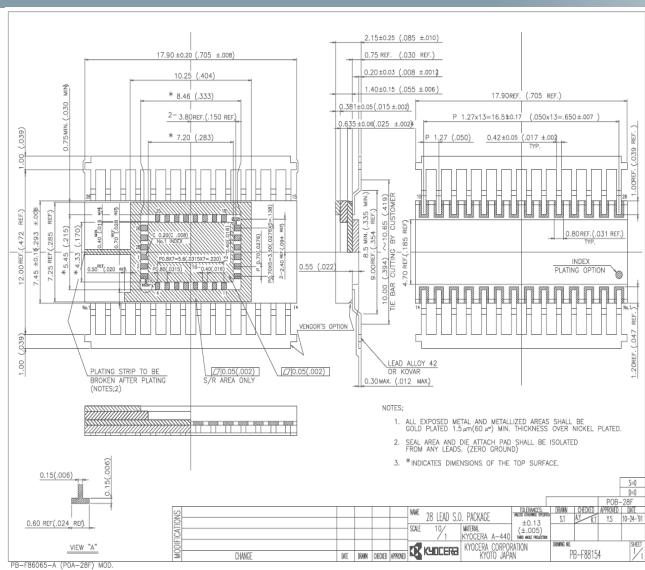


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Overview ceramic packages



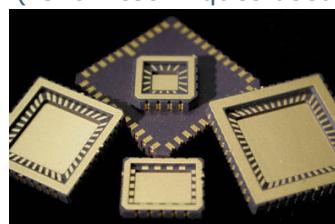
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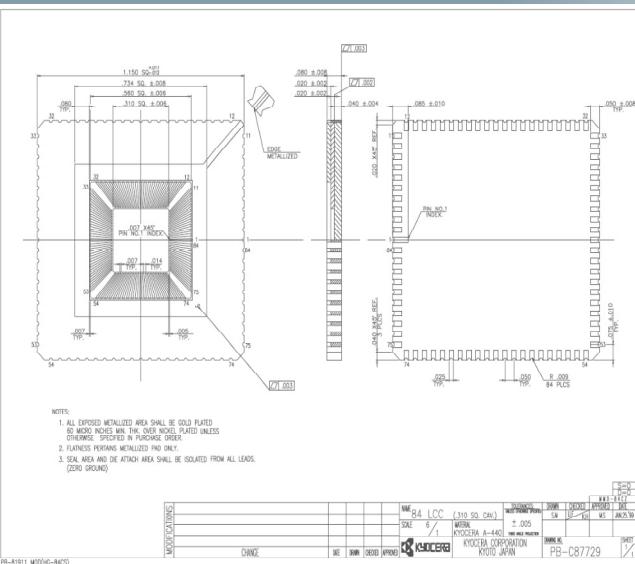
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Overview ceramic packages

- **CLCC** = Ceramic Leadless Chip Carrier
 - Leadless design = no leads outside boundary.
 - Connection on 4 sides.
 - Pin-count: 3..84.
 - ✓ Mechanically strong.
 - ✗ No manual mounting on pcb (reflow techniques used).
Typically used in a socket.



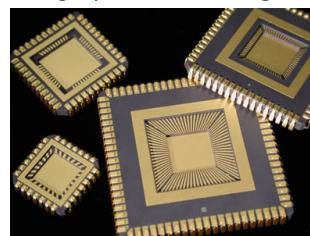
Overview ceramic packages





Overview ceramic packages

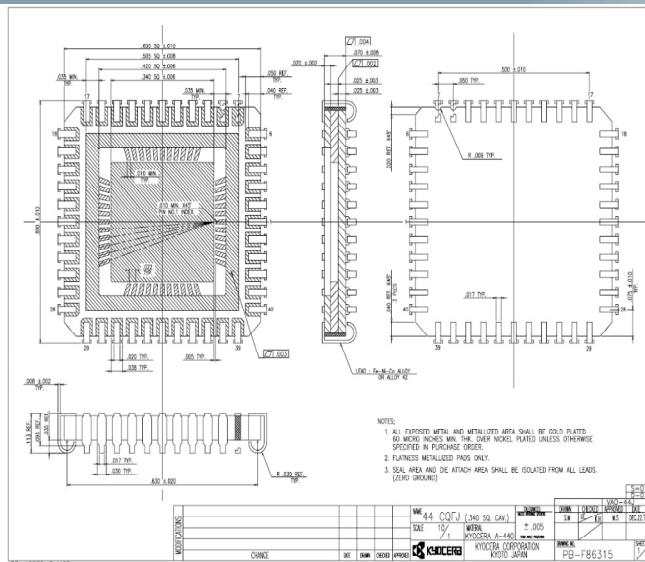
- **JLCC = J-Leaded Chip Carrier**
 - Leads in J-shape.
 - Connection on 4 sides.
 - Pin-count: 28..84.
- ✓ More or less compatible with Plastic PLCC.
- ✓ Lead shape reduce thermal stress. High power handling.
- ✗ Vulnerable leads.



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Overview ceramic packages



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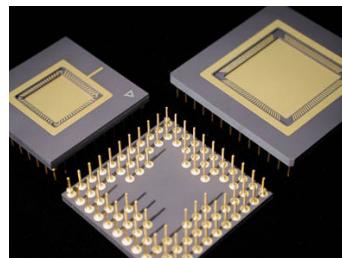
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Overview ceramic packages

- **CPGA = Ceramic Pin Grid Array**

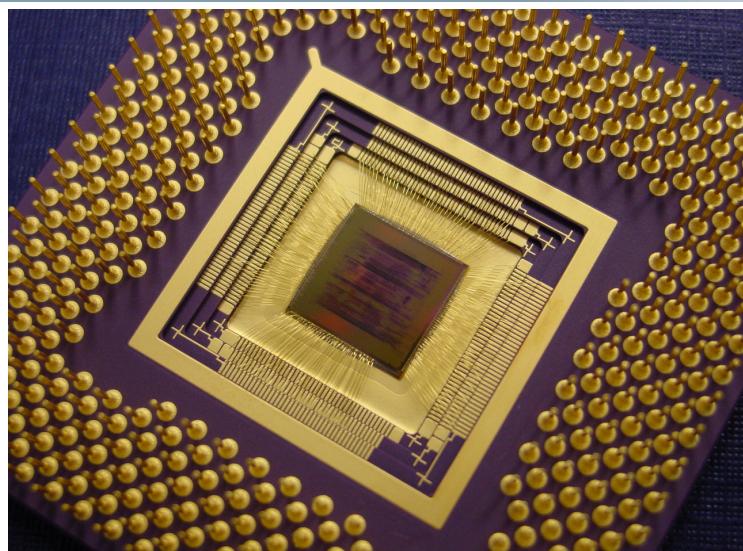
- Pins arranged in an array on bottom (pcb) side.
- Package contains 2..6 layer pcb for redistribution to array.
- Exists as cavity-up or cavity-down.
- Pin-count: 64..476.



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Overview ceramic packages



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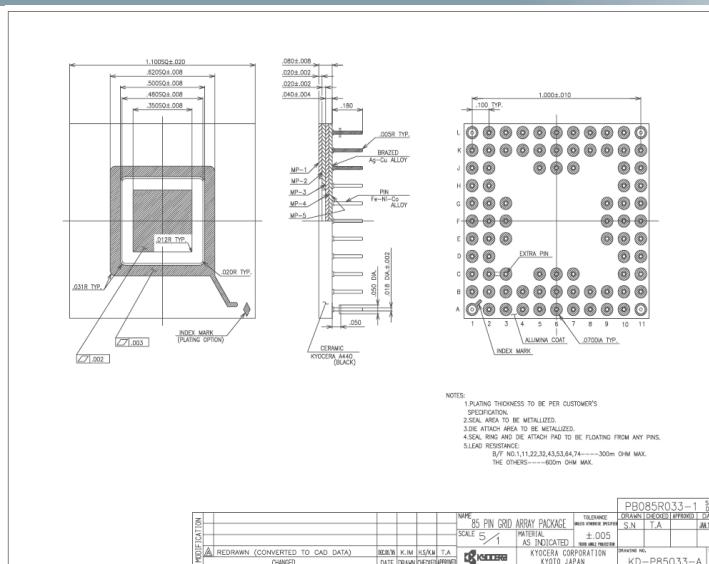
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Overview ceramic packages

- ✓ Relatively high pin count available (476 pins).
- ✓ Very robust package.
- ✓ Excellent heat dissipation. Thermal resistance $\Theta_{ja} < 20 \text{ }^{\circ}\text{CW}$
- ✓ Possible to create custom made PGA (Kyocera, NTK).
- ✗ Multiple cavity rings makes bondingdiagram complex.
- ✗ Power-ring and dedicated pins makes bondingdiagram complex.
- ✗ No standardized pin assignment table.
- ✗ Impossible to access silicon with cavity-down PGA.
- ✗ Large body size – occupies a lot of space on a pcb.

Overview ceramic packages





Overview ceramic packages

BONDING PATTERN

NAME	85 PIN GRID ARRAY PACKAGE	TOLERANCE	W.M.	DRAWN	CHECKED	APPROVED	DATE
SCALE	20:1	NOTES	TYPICAL				
MODIFICATION	A (REDRAWN (CONVERTED TO CAD DATA))	RECD BY	K.I.M	H.S/K.W	T.A.	SHEET	1/2
CHANGED	DATE	DRAWN	CHECKED	APPROVED	RECD BY	DATE	1/2
KYOCERA CORPORATION KYOTO JAPAN DRAWING NO. KD-P85033-A							

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Overview ceramic packages

WIRE BOND PAD / CONNECTOR PIN INTERCONNECTION PLAN

W/B NO.	PIN NO.								
1	B 2	21	L 1	41	K 9	61	B11	81	A 3
2	C 2	22	K 2	42	L11	62	C10	82	A 2
3	B 1	23	K 3	43	K10	63	A11	83	B 3
4	C 1	24	L 2	44	J10	64	B10	84	A 1
5	D 2	25	L 3	45	K11	65	B 9		
6	D 1	26	K 4	46	J11	66	A10		
7	E 3	27	L 4	47	H10	67	A 9		
8	E 2	28	J 5	48	H11	68	B 8		
9	E 1	29	K 5	49	F10	69	A 8		
10	F 2	30	L 5	50	G10	70	B 6		
11	F 3	31	K 6	51	G11	71	B 7		
12	G 3	32	J 6	52	G 9	72	A 7		
13	G 1	33	J 7	53	F 9	73	C 7		
14	G 2	34	L 7	54	F11	74	C 6		
15	F 1	35	K 7	55	E11	75	A 6		
16	H 1	36	L 6	56	E10	76	A 5		
17	H 2	37	L 8	57	E 9	77	B 5		
18	J 1	38	K 8	58	D11	78	C 5		
19	K 1	39	L 9	59	D10	79	A 4		
20	J 2	40	L10	60	C11	80	B 4		

S/R	N C
D/A	N C
EXTRA PIN (C3) C 2	

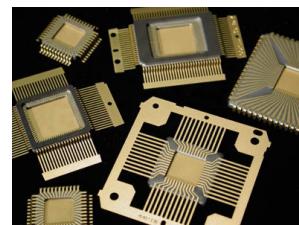
NAME	85 PIN GRID ARRAY PACKAGE	TOLERANCE	W.M.	DRAWN	CHECKED	APPROVED	DATE
SCALE	X	NOTES	TYPICAL				
MODIFICATION	A (REDRAWN (CONVERTED TO CAD DATA))	RECD BY	K.I.M	H.S/K.W	T.A.	SHEET	1/2
CHANGED	DATE	DRAWN	CHECKED	APPROVED	RECD BY	DATE	1/2
KYOCERA CORPORATION KYOTO JAPAN DRAWING NO. KD-P85033-A							

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Overview ceramic packages

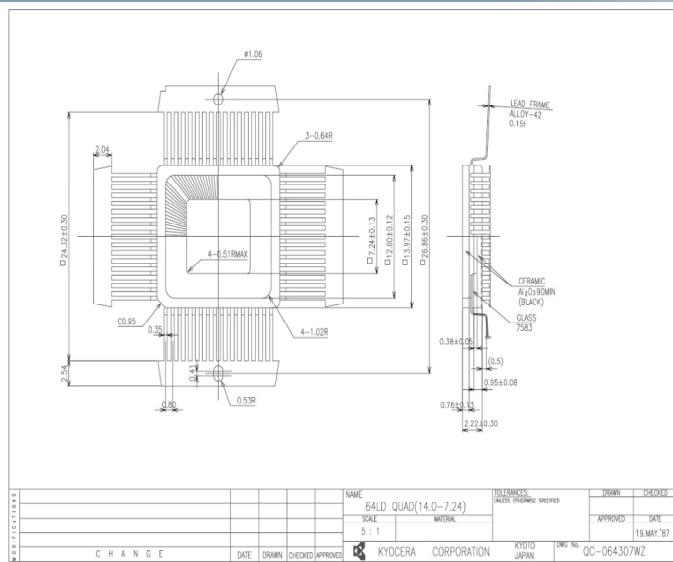
- **CQFP = Ceramic Quad Flat Package**
 - Connection on 4 sides.
 - ✓ High pin count possible (304 pins).
 - ✓ Compact body.
 - ✗ Vulnerable leads when cut (coplanarity).
 - ✗ Small lead-pitch (0.5mm) is difficult to handle.
 - ✗ Manual cut of pins.



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Overview ceramic packages



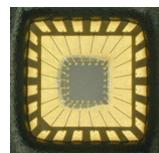
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Overview ceramic packages

- **Open Cavity QFN = Quad Flatpack No lead**
 - Chip Scale Package (CSP).
 - Leadless design = no leads outside boundary.
 - ✓ Compact body (example QFN24 - 5x5mm).
 - ✓ Excellent thermal and electrical properties (RF applications).
 - ✗ Impossible to access silicon due to sealed lid.
(visual check of wiring and measurements on-silicon).
 - ✗ Rather expensive (additional setup cost).



Overview ceramic packages

Cost Effective Alternative to Ceramic Packaging

Product Data Sheet—QFN / MLP

Package Materials:

Plastic Body: Semi conductor grade plastic, black
Dielectric Constant = 4.4 at 1MHz

Lead Frame:

194 Copper (Cu) FH

Plating:

50 micro-inches Au over 30 micro-inches Ni

Distance from Lead frame (Die Pad) to Bonding

Lead is:

8 mm Package = .174 mm

7 mm Package = .160 mm

5 mm Package = .164 mm

4 mm Package = .160 mm

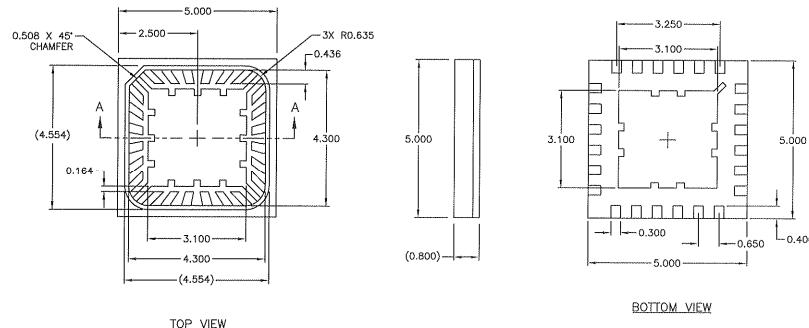


ELECTRICAL AND THERMAL DATA

PACKAGE	INDUCTANCE (nH)	CAPACITANCE (pF)	RESISTANCE (M-OHMS)	THETA J °C/W
4X4	.691	.251	.32	35.3 TYP.
5X5	.865	.289	.44	34.8 TYP.
7X7	1.37	.416	.56	24.4 TYP.
8X8	1.47	.475	.63	20.9 TYP



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Wirebonding techniques

Wirebonding =

electrical interconnection technique using thin wire and a combination of heat, pressure and/or ultrasonic energy.

- Wirebonding process:

	Pressure	Temperature	Ultrasonic	Wire	Pad
Thermocompression (T/C)	High	300-500°C	No	Au	Al,Au
Ultrasonic (U/S)	Low	25°C	Yes	Au, Al	Al,Au
Thermosonic (T/S)	Low	100-150°C	Yes	Au	Al,Au

Wirebonding techniques

- Wedge/Ball wirebonding

1. Ball bonding - flow

- The wire passes a hollow capillary.
- A EFO (Electronic Flame Off) melts a small portion of wire just beneath the capillary.
- The surface tension forms a spherical shape (ball) as the metal solidifies.
- Ball is pressed to the bondpad to cause plastic deformation and atomic interdiffusion of the wire.
- The capillary is raised and repositioned and a second bond (wedge, fishtail) is created.
- The wire clamp is closed. The movement of capillary cuts the wire.



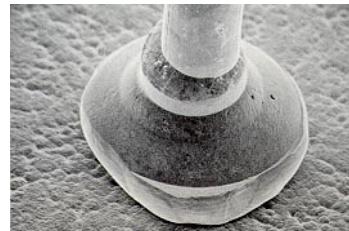
Wirebonding techniques

Typically T/C, T/S is used with gold wire.

Speed of 10 bonds/sec. are possible.

Loop length recommended below 100x wire-diameter.

Ball diameter typically 2,5x a 3x wire-diameter.



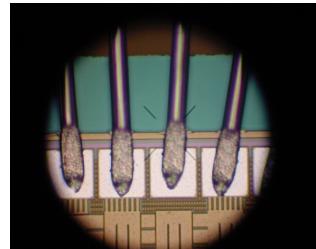
Wirebonding techniques

2. Wedge bonding -flow

- Wire is fed at an angle of typically 30°-60°
- The wedge/capillary descend onto the bondpad, after which U/S or T/S energy melts the wire onto the pad surface.
- The wedge/capillary is raised and repositioned and a second bond (wedge) is created.

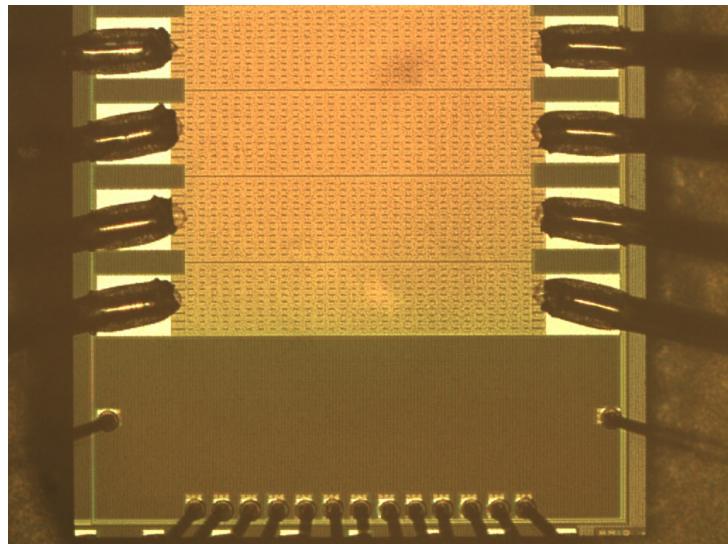
Named after the shape of the tool.

Typically U/S with Al.
T/S with Au.





Wirebonding techniques



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Wirebonding techniques

- Wires and metallurgic systems

Mainly 3 types of wire are used:

1. Gold – Au
2. Aluminium – Al
3. Copper – Cu

For prototyping, typically 1mil (=25.4mm) gold wire is used.

Electrical specs – see page 50.

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Wirebonding techniques

- Different metallurgic systems exist (wire-pin).
- **Au-Au:** Extreme reliable. Requires gold plating. Affected by surface contamination.
 - **Au-Al:** Typically used for prototyping. Reduced reliability of bonds (intermetallic compounds, Kirkendall voids).
 - **Au-Cu:** Difficult. Cleaning is extremely important. Poor reliability and quality. For this reason, typical redistribution to Al (BEOL=Cu in 0.13um and below).
 - **Au-Ag:** Very reliable. Requires silver plating. High temperature required to avoid Sulpher contamination.

Wirebonding techniques

- **Al-Al:** Extremely reliable. Typical U/S.
- **Al-Ag:** Rarely used because of tendency to degrade due to oxidation.
- **Al-Ni:** Typically used in power devices and high temperature operation.
- **Cu-Al:** Similar to Al-Cu. Adequate reliable on condition that some oxygen in package is available (prevents voids).



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Practical rules

- Selection criteria:
 - Pin count
 - Availability of test-socket
 - Price
 - Cavity size (wirelength, die-size)
 - Body size (area on pcb?)
 - Thermal performance
 - Electrical performance
 - ...

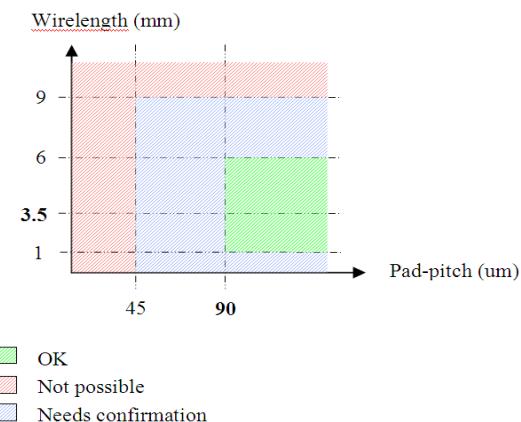


Practical rules

- Major assembly constraints for ceramic packages:
 - **wirelength:** ideal wirelength is 3,5mm. Preferably wirelength is between 1mm and 6mm. Absolute maximum is 9mm.
 - **pad-pitch:** preferred pad-pitch (= distance between centre of adjacent bondpads) is above 90um. Absolute minimum pad-pitch is 45um (status Q1 2010).

Especially the combination of long wires and small pad-pitch is technically challenging. If pitch is below 90um and/or wirelength above 6mm, it needs to be investigated case-by-case whether assembly is possible.

Practical rules

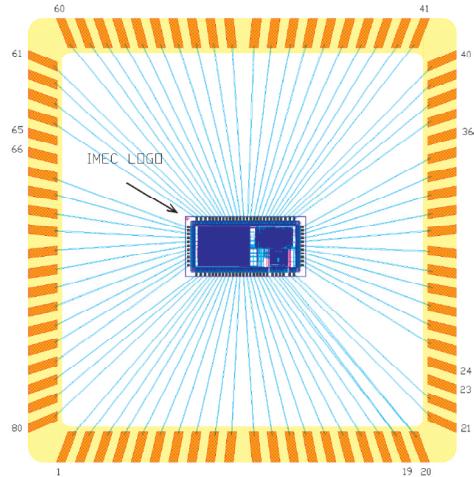
Wirelength versus Pad-pitch

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Practical rules

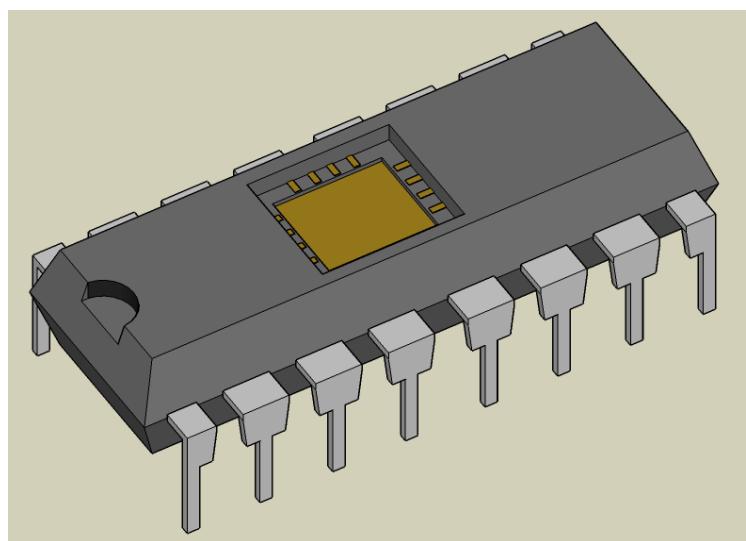
- Example bondingdiagram:



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Practical rules

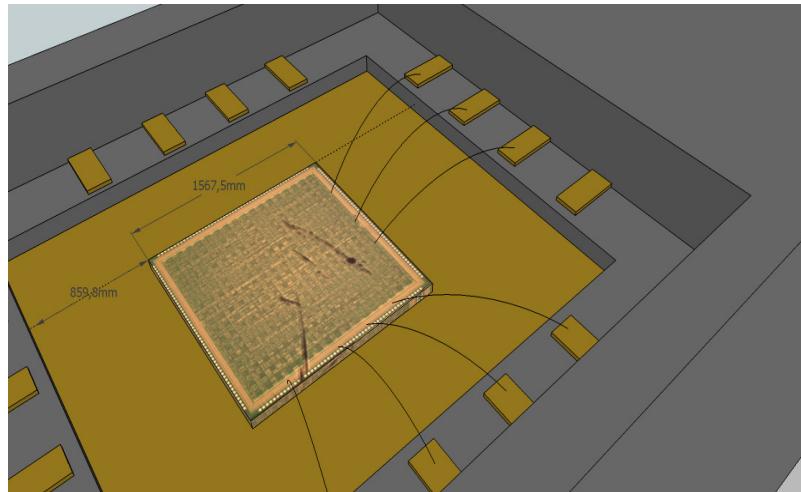


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Practical rules



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Practical rules

- Assembly remarks:
 - Crossing bondwires are not allowed.
 - Bondwire angle (between cavity edge and circuit edge) should be above 45°
 - Double bonds (= 2 wires starting from 1 package pin) are possible. The opposite (= 2 wires starting from 1 bondpad) is not allowed, unless bondpads has double dimensions.
 - Maximum 2 overbonds (= wire starting on a bondpad and ending on a package pin from adjacent side) are acceptable.
 - If desired, a cavity-strap (= electrical connection to cavity) can be added. In this case, conductive glue must be used.

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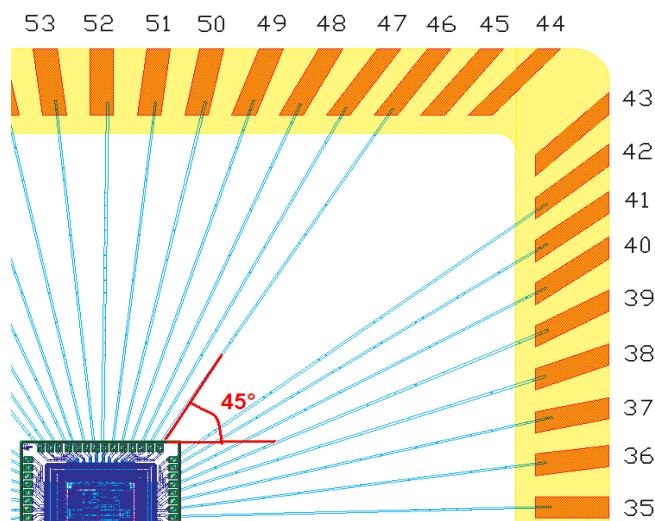
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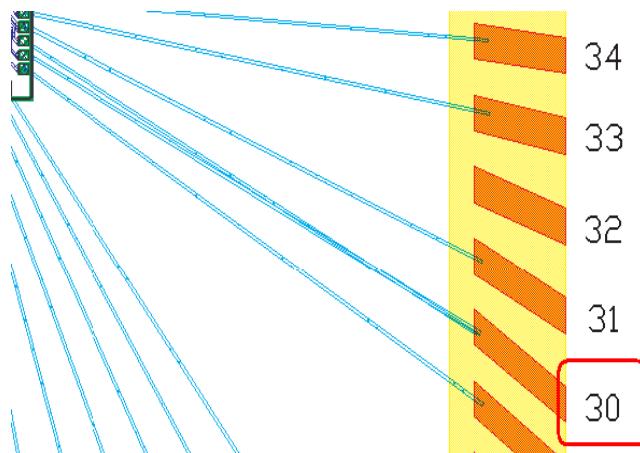




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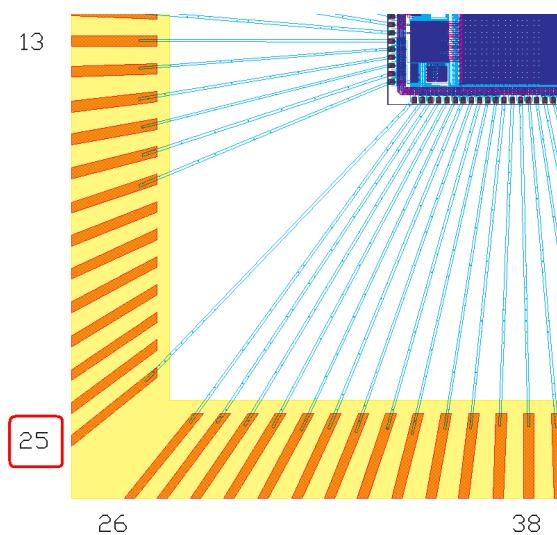




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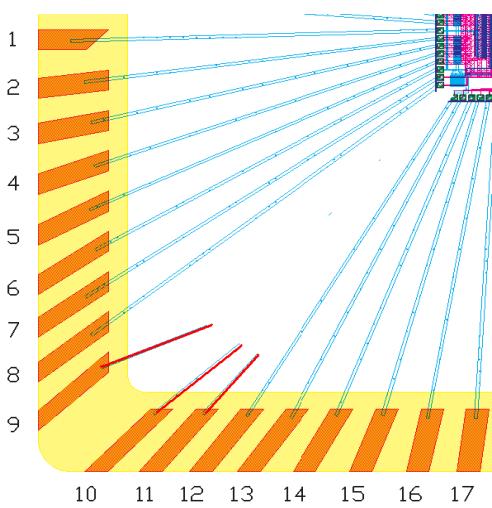




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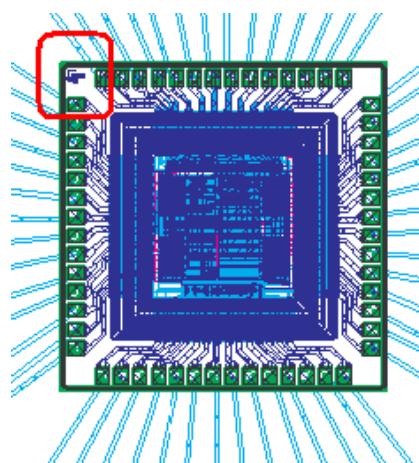




Practical rules

- To facilitate orientating of the die in the package, it is recommended to place a DRC-error-free clearly visible logo - for example in the upper-left corner.
- If possible, not-connected bondpads should be avoided, as these are difficult to identify. Not-connected package pins are no problem, as these have a pin-number assigned.
- Cavity size should be minimum 1,5mm larger than circuit size. On all sides, 750um clearance is required.
- Die-thickness is not important for ceramic assembly.
- Bondpad size: recommended > 60umx60um (passivation opening)

Practical rules

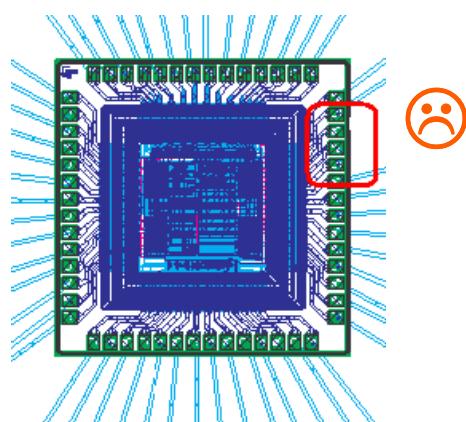




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Practical rules

- To fascillate orientating of the die in the package, it is recommended to place a DRC-error-free clearly visible logo - for example in the upper-left corner.
- If possible, not-connected bondpads should be avoided, as these are difficult to identify. Not-connected package pins are no problem, as these have a pin-number assigned.
- Cavity size should be minimum 1,5mm larger than circuit size. On all sides, 750um clearance is required.
- Die-thickness is not important for ceramic assembly.
- Bondpad size: recommended > 60umx60um (passivation opening)

Practical rules

- Thermal performance:

$$T_j - T_a = P \times \Theta_{ja}$$

T_j = Junction temperature.

T_a = Ambient temperature.

P = power dissipation.

Θ_{ja} = Thermal resistance between junction and ambient.

Example: CLCC24: $\Theta_{ja} = 75^{\circ}\text{CW}$, $T_j = 125^{\circ}\text{C}$, $T_a = 50^{\circ}\text{C}$

→ Max. power << 1.0 W

Airflow improves power handling significantly, as Θ_{ja} decreases.



Practical rules

Thermal Resistance Coefficients

		θ_{JA} [°C/W]	Airflow = 0 ft/min
Ceramic DIP	24D9DW3	9	65
	24D6DW6	10-15	45
	28D6DW6	10-15	45
	32D6DW6	10	45
	40D6DW6	7	40
Plastic DIP	20P3	19	65
	24P3	22	60
	24P6	39	60
	28P6	36	55
	32P6	34	50
Leadless Chip Carrier (LCC)	40P6	30	45
	28L1W	12	68
	32L1W	10	65
	44L1W	8-10	60
	68L1W	6-8	50 - 60
Plastic Leaded Chip Carrier (PLCC)	20J	35	42
	28J	16	38
	32J	16	36
	44J	14	30
	68J	13	25
J-leaded Chip Carrier (JLCC)	84J	13	22
	28K/KW	16	72
	32K/KW	16	72
	44K/KW	16	68
Capack	44K/KW	10-14	47
	24C/CW	15	81

Thermal Resistance Coefficients (Continued)

		θ_{JA} [°C/W]	Airflow = 0 ft/min
Flatpack	28F	10	65
	32F	8-10	60
PGA	28U	10	65
	30U	10	65
Sidekraze	32S	8-10	40-50
SOIC	20S	17	56
	24S	17	46
PQFP	44Q	15	38
	100Q	12	32
	160Q	8	30
TQFP	44A	17	41
	100A	10	34
	28T	66	55
	32T	45	55
	40T	35	50
TSOP	40(V)	55	53
	46T	30	47
	20X	64	72
TSSOP	24X	60	67
	28X		65
MLF	32M	39	32
	44M	23	25
	64M	12	20

Practical rules

Package Type	Mkt Dwg	JEDEC Spec	Typical Thermal Data			
			Die Size (sq mils)	θ_{JA} (°C/W) (Note 1) Air Flow = LFM (Linear Feet/Minute)	θ_{JC} (°C/W)	
			0	225	500	1000
Ceramic Pin Grid Array (CPGA)	U44A	None	59048	24	31	22
	U45B	MO-007-AB	14702	31	34	30
	U48C	MO-006-AC	14702	46	36	32
	U86D	None	14702	46	36	32
	U90e	MIL-005-A01	14702	46	31	27
	U75A	MO-006-AC	14702	41	32	27
	U44A	MO-006-AC	48400	32	22	16
	U94S	MO-007-AB	14702	43	33	28
	U84C	MO-006-AB	59048	30	17	13
	U90A	MO-006-A0	59048	30	17	13
	U100A	MO-006-AB		Data Not Available at This Time		2
	U109A	MO-006-AE		Data Not Available at This Time		
	U120A	None	59048	35	22	17
	U1170C	MO-006-AP	59048	35	22	17
	U124A	MO-006-A0	59049	38	25	19
	U132A	MO-006-AP	25000	32	25	18
	U132B	MO-006-AP		Data Not Available at This Time		3
	U144A	MO-007-AG	67600	28	20	16
	U158A	MO-006-A0	59048	27	15	12
	U156B	MO-006-A0		Data Not Available at This Time		
	U169A	MO-007-AJ	132884	20	12	8
	U170A	MO-006-AP	132880	21	12	9
	U175A	MO-007-AB	21200	21	12	7
	U150A	MO-007-AG	132000	26	18	14
	U223A	MO-007-AM	386050	16	9	6
	U224A	MO-007-AL	122650	26	15	11
	U225A	MO-006-AM		Data Not Available at This Time		3
	U259A	MO-007-AL		Data Not Available at This Time		
	U269A	MO-007-AM		Data Not Available at This Time		
	U301A	MO-007-AM	100000	18	14	11
	U303A	MO-007-AM	160000	19	14	11
	U323A	None	160000	19	14	10



Practical rules

• Electrical performance

Parasitic RLC components, caused by:

1. Bondwires

Length	Wire Length	Bond Wire	Diameter	
	0.8 mil	1.0 mil	1.2 mil	1.3 mil
Resistance (Ohm)	5 mm	0.363	0.257	0.196
	2 mm	0.154	0.103	0.079
				0.072
Inductance (nH)	5 mm	6.103	5.869	5.668
	2 mm	2.089	1.996	1.915
				1.879
Capacitance (pF)	5 mm	0.202	0.242	0.279
	2 mm	0.104	0.122	0.140
				0.149
Mutual Inductance (nH)	5 mm	3.320	3.318	3.314
	2 mm	0.9798	0.9787	0.9770
				0.9758
Mutual capacitance (pF)	5 mm	-0.0374	-0.0468	-0.0602
	2 mm	-0.0204	-0.0261	-0.0327
				-0.0364

Practical rules

2. Package itself

Table 4-6. Summary of CQFP Electrical Data

Electrical Parameter	Lead Count	
	164L	196L
L_{lead} (nH)	3.3	3.3
R_{lead} (Ω)	0.004	0.004
$L_{\text{trace}(I/O)}$ (nH)	5.0	6.0
$R_{\text{trace}(I/O)}$ (Ω)	0.8	0.9
C_{loss} (pF)	4.0	5.0
$L_{\text{trace}(Vcc/Vss)}$ (nH)	1.5	2.5
$R_{\text{trace}(Vcc/Vss)}$ (nH)	0.2	0.4
L_{wire} (nH)	3.0	3.0
R_{wire} (Ω)	0.08	0.08
$C_{(\text{Vcc Plane to Vss Plane})}$ (pF)	170.0	240.0

