# Soroush Khaleghi

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## Education

- **Ph.D., University of Illinois at Chicago (UIC)**, IL, USA — Aug. 2012 – May 2018 (Expected)
  Computer Engineering, GPA: 4.0/4.0
  Advisor: Prof. Wenjing Rao
- **B.Sc., Sharif University of Technology**, Tehran, Iran — Aug. 2007 – May 2012
  Electrical Engineering, Control Systems
  - Thesis: "*Implementation of a microgrid control system on FPGA using hardware-in-the-loop simulation*"

## Research Interests

- Hardware Security, designing techniques and architectures for secure and trusted hardware
- VLSI design, HDL programming
- Designing techniques and architectures for reliable nanoelectronic systems

## Technical Skills

- **Programming Languages:** C/C++, Python, Verilog, Assembly (MIPS, 8085, 8051, x86), Matlab
- **Engineering Software and Tools:** Quartus II, ModelSim, Simulink, Cadence Virtuoso, Design Compiler, Cadence Encounter, HSpice, Atalanta

## Related Course Work

- **VLSI Design**: ASIC/FPGA Chip Design, Introduction to VLSI Design, Testing and Reliability of Digital Systems, Digital Systems Design, Advanced Computer Architecture, Computer Structure and Microprocessors, Microprocessor System Design, Logic Circuits and Digital Systems
- **Algorithm and Computer**: Data Mining and Text Mining, Computer Algorithms, C++ Programming, Object Oriented Programming, Artificial Neural Networks, Linear Algebra, Codes and Cryptography, Computer Security

## Research and Project Experience

- **Research Assistant, UIC:** — Fall 2012 – Present
  - **Hardware Security and Design for Trust**
    - Developed an IC protection scheme through withholding partial design information as the key and correlating the key cells to increase the system security exponentially at a linear hardware cost
    - Employed strong Physically Unclonable Functions in an IC protection framework to achieve a unique key per chip, in order to prevent powerful side-channel and invasive attacks
  - **Reliability and Fault Tolerance of Nanoscale Systems**
    - Developed and analyzed various algorithms for constructing reliable scalable systems via spare sharing (hardware redundancy) under limited interconnection constraints.
    - Developed and analyzed various repair algorithms to enhance the reliability of spare sharing networks
- **Related Projects:**
  - **FPGA/ASIC Implementations** — Fall 2011 – Spring 2014
    - Implemented a microgrid control system on FPGA using hardware-in-the-loop simulation (B.Sc. thesis)
    - Implemented the MIPS 5-stage pipeline that handles ALU and load/store instructions
    - Implemented an animation on screen using the Video Graphics Array (VGA) adapter on *Altera DE2* board
    - Implemented an OFDM symbol synchronizer using ASIC design flow
  - **VLSI Design** — Fall 2013
    - Design of a 4-bit ALU layout: creating the transistor level circuit, as well as the layout for a 4-bit ALU using *Cadence*. Layout involved Design Rule Checking (DRC), Layout Versus Schematic (LVS), and Parameter Extraction (PEX) for eventual simulation for delay evaluation and functional verification.

- **Data Mining and Test Mining** Fall 2014
  - Implemented MS-GSP algorithm for mining sequential patterns in *Python*
  - Implemented Tweets classification using SVM and Naive Bayesian algorithms on 2012 presidential candidates

## Teaching Experience

- **Computer Organization II** (Teaching Assistant (TA), UIC) Fall 2015 & Fall 2014
  - *Verilog* implementation of digital circuits, including the MIPS 5-stage pipeline; simulations using *ModelSim* with test-benches in *Verilog*
  - Assembly language programming of MIPS Processors
- **Testing and Reliability of Digital Systems** (TA, UIC) Spring 2015 & Spring 2014
  - Involves several projects, including test vector generation for combinational and sequential circuits, and implementation of test volume/time reduction techniques; *Atalanta* is the main tool in this course
- **Digital System Design** (TA, UIC) Fall 2013
  - Responsible for preparing a tutorial on *Altera Quartus II*, including schematic capture, hierarchical design, power analysis, and timing simulation
  - Design and implementation of the optimization techniques for digital circuits in *Quartus II* using the schematic capture and *Verilog*
- **Computer Structure and Microprocessors** (TA, Sharif University of Technology) Spring 2011
  - Responsible for designing the new laboratory experiments on *8085* Microprocessor
- **Linear Control Systems** (TA, Sharif University of Technology) Fall 2011
  - Analysis and design of linear control systems using *Simulink*
- **Logic Circuits and Digital Systems** (TA, Sharif University of Technology) Fall 2010
  - Responsible for holding *Verilog* sessions
- **C++ Programming** (**Instructor,** Farzanegan Highschool, Tehran, Iran) Fall 2009

## Publications

- **S. Khaleghi**, W. Rao, "*IC Piracy Prevention: Engaging Strong PUFs to Achieve a Unique Key per Chip*", Submitted to Design, Automation and Test in Europe Conference (DATE), 2016.
- **S. Khaleghi**, K. D. Zhao, W. Rao, "*IC Piracy Prevention via Design Withholding and Entanglement*", Asia and South Pacific Design Automation Conference (ASP-DAC), Pages 821-826, 2015.
- **S. Khaleghi**, W. Rao, "*Spare Sharing Network Enhancement for Scalable Systems*", *IEEE* International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Pages 249-254, 2013.
- **S. Khaleghi**, W. Rao, "*Constructing Spare Sharing Network for Reliability Enhancement of Scalable Systems*", *IEEE* Workshop on Signal Processing Systems (SiPS), Pages 336-341, 2013.

## Academic Service

- **Reviewer for the following Journals and Conferences:** International Conference On Computer Aided Design (ICCAD); Design, Automation and Test in Europe (DATE); Journal of Emerging Technologies in Computing (JETC); IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH); IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC); IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
- **IEEE Student Member**: Computer Engineering Society