Single Cycle CPU

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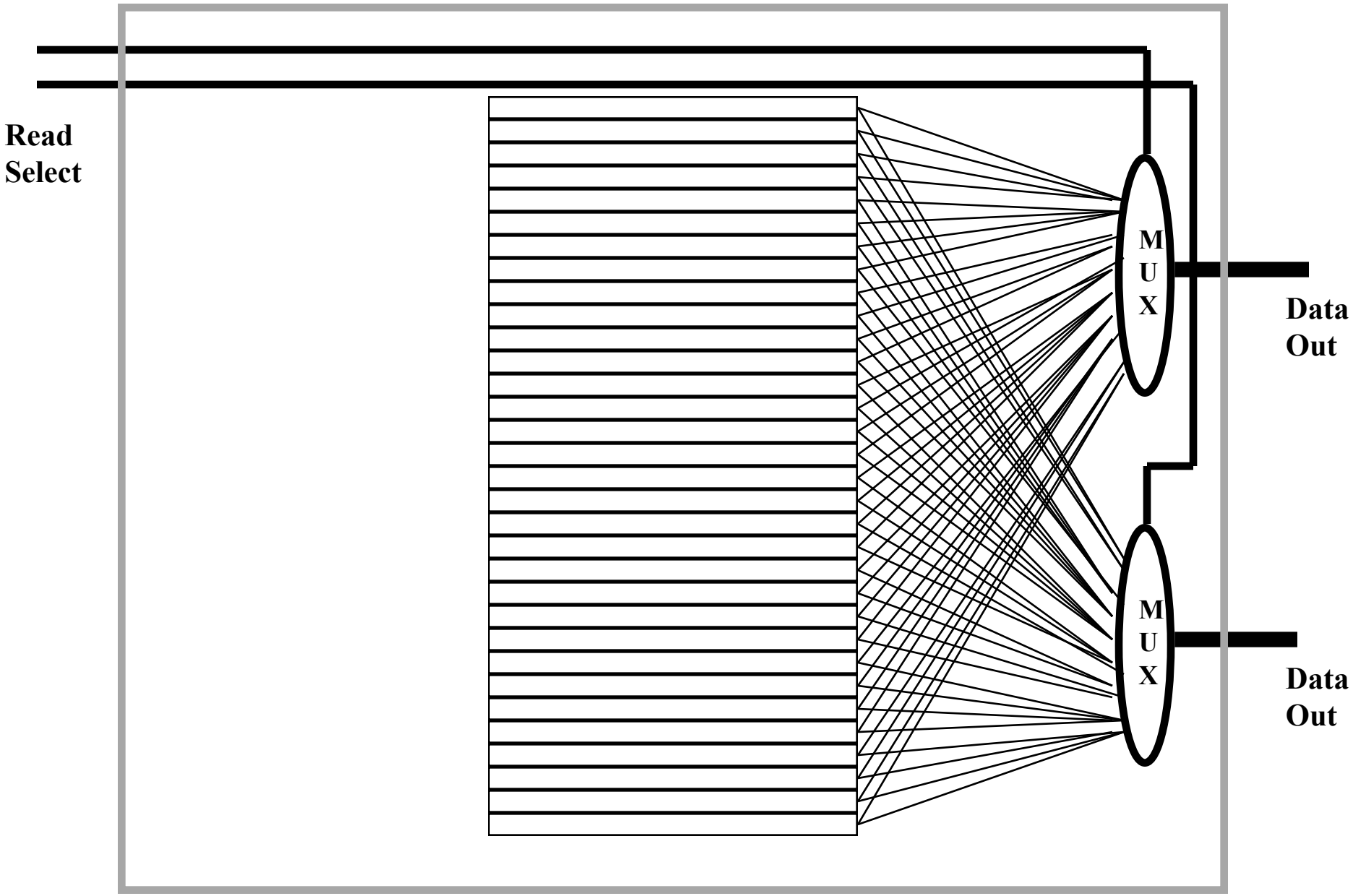
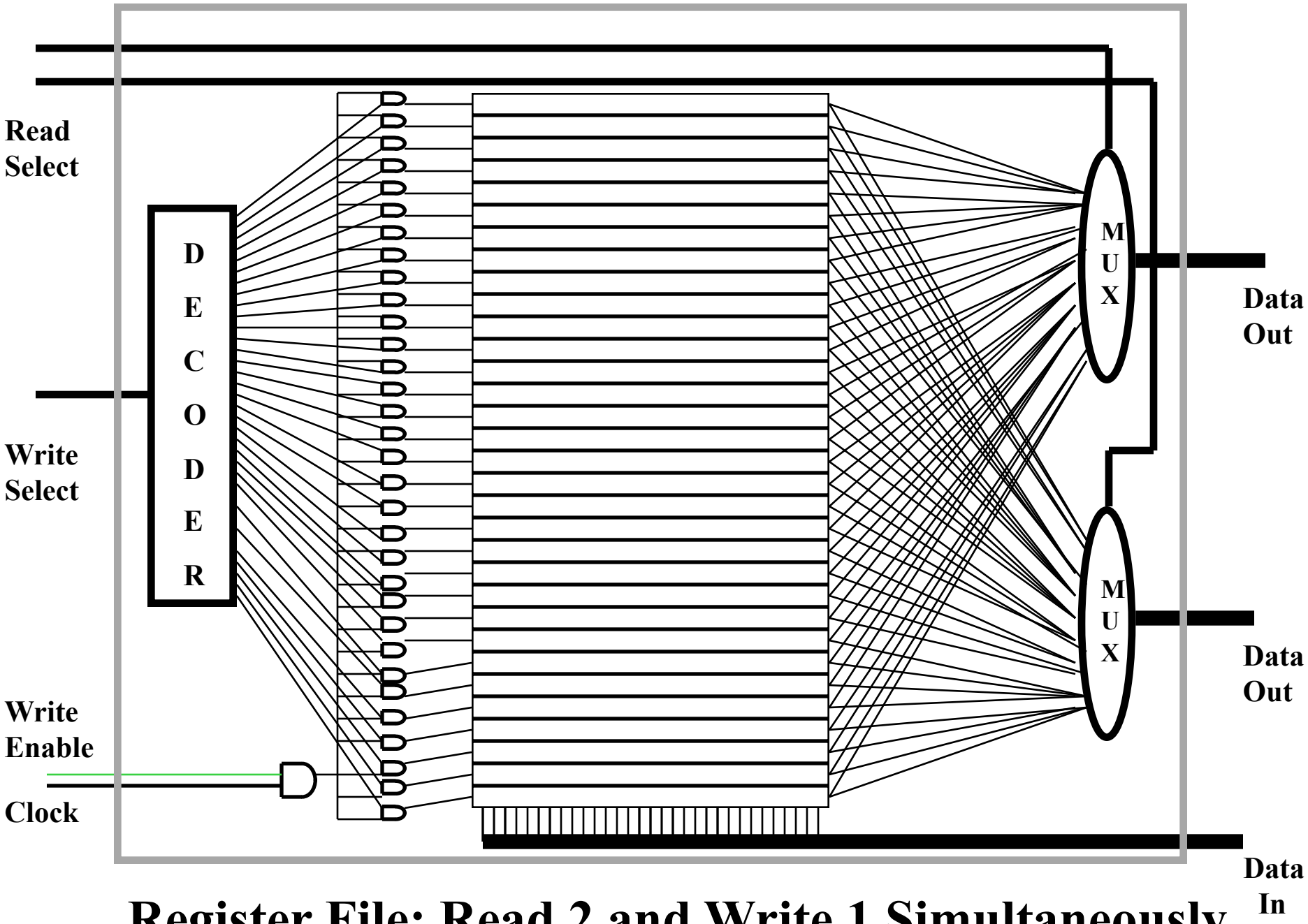
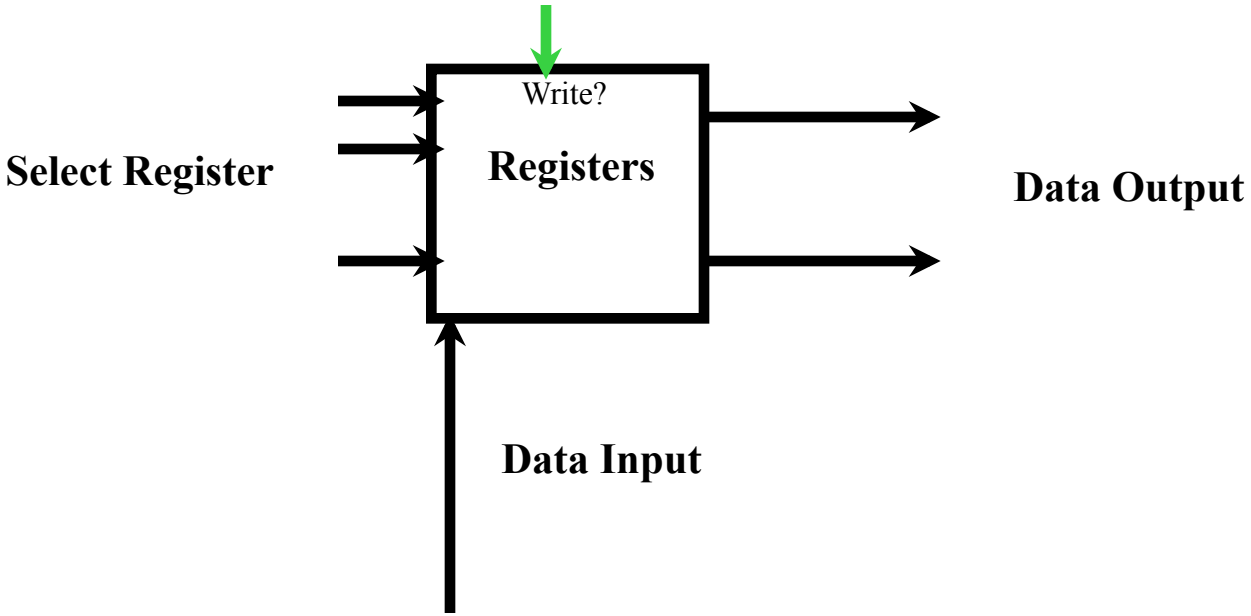
(with minor modifications by Alyce Brady, Kalamazoo College)



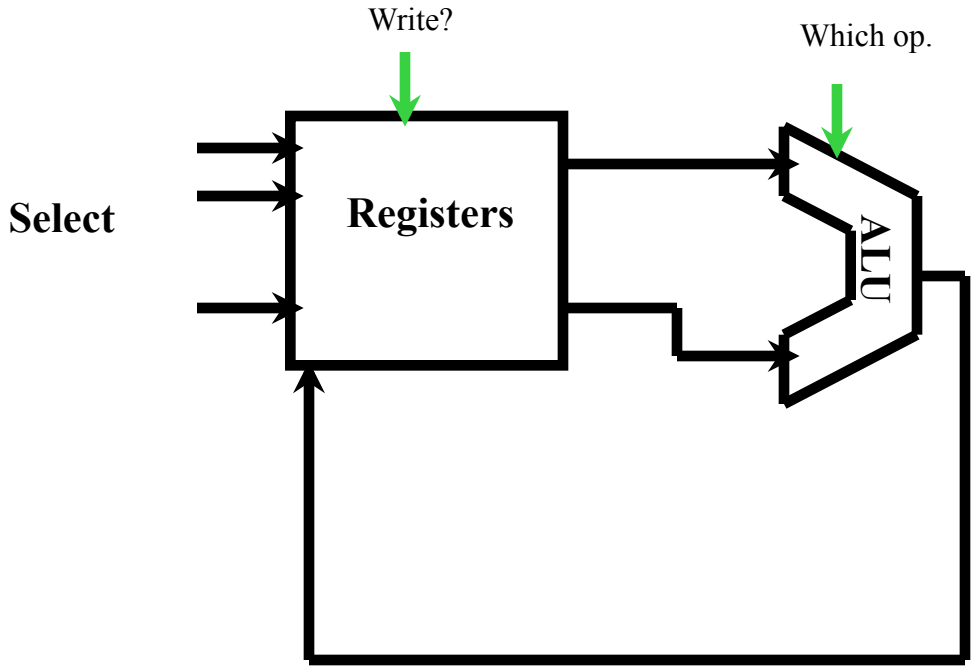
Register File: Read 2 Registers Simultaneously



Register File: Read 2 and Write 1 Simultaneously

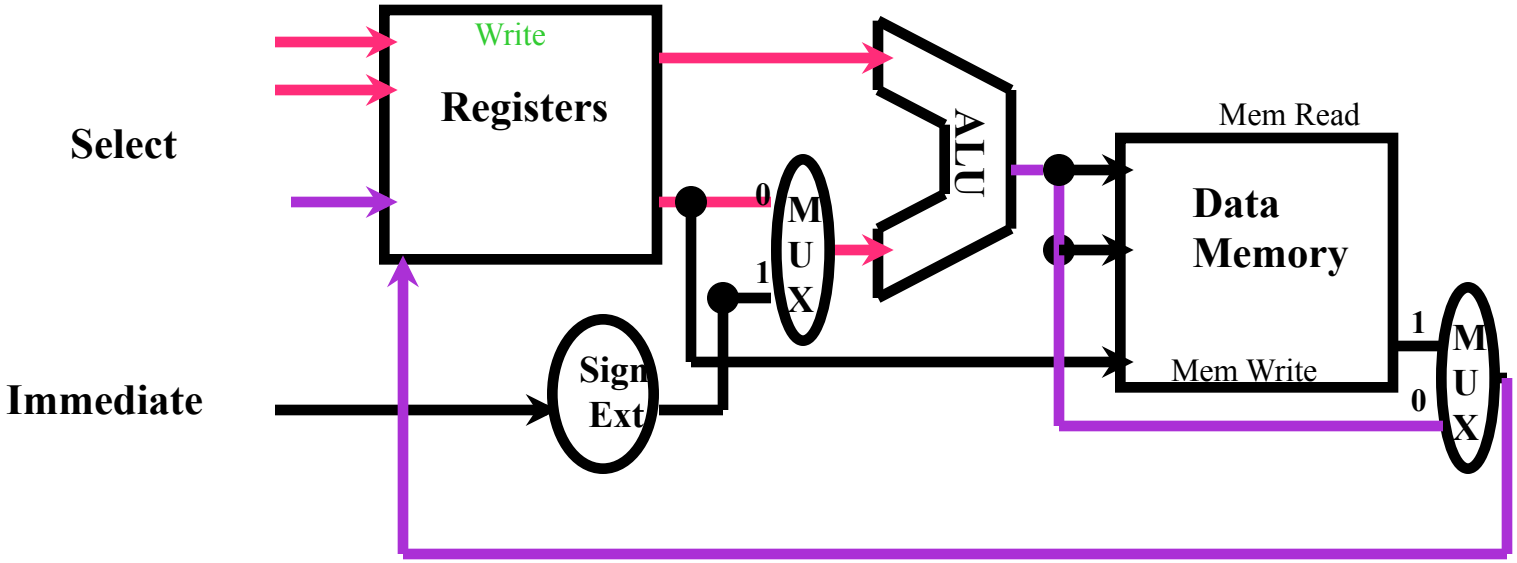


One Step Back



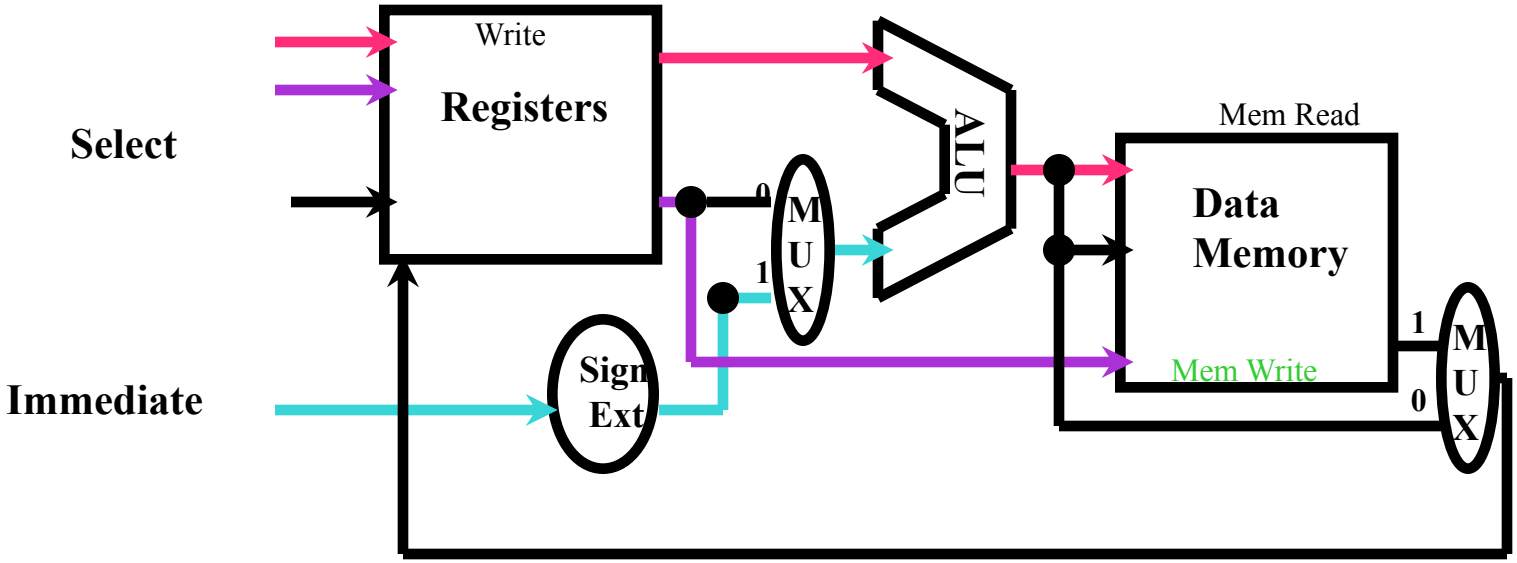
R-Type Instruction Path

e.g., add $t0, $t1, $t2



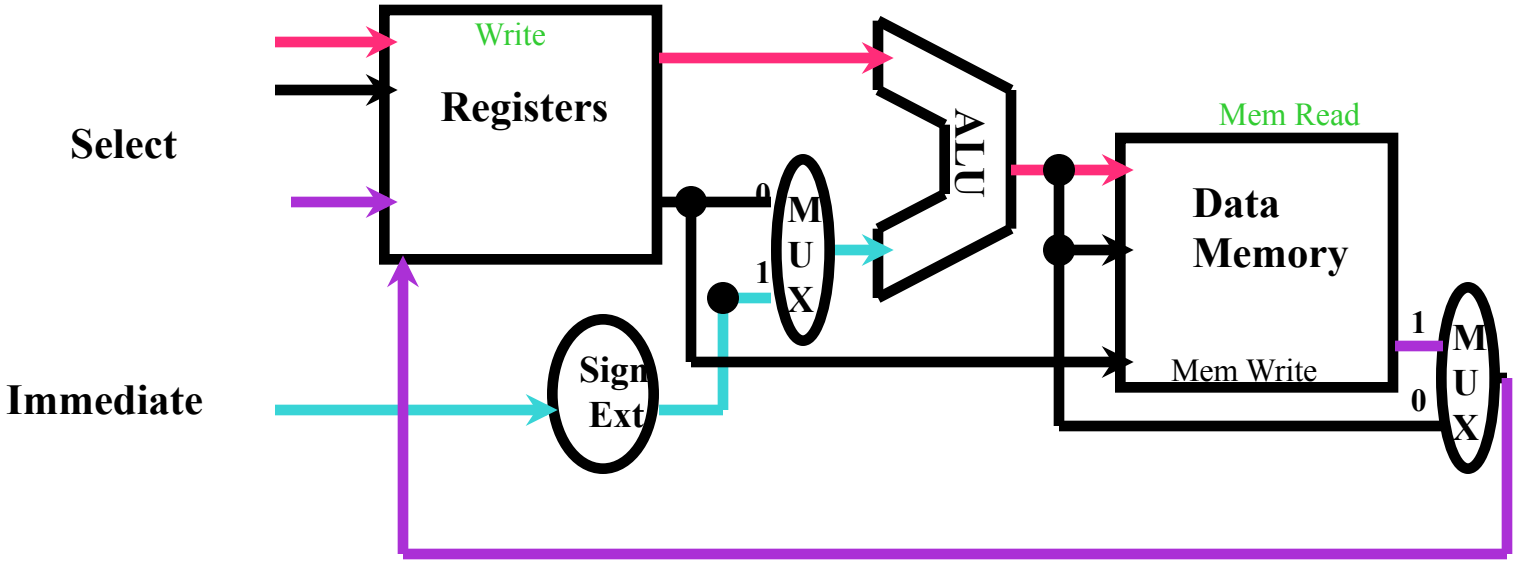
R-Type Instruction Path (in a larger context)

e.g., add $t0, $t1, $t2



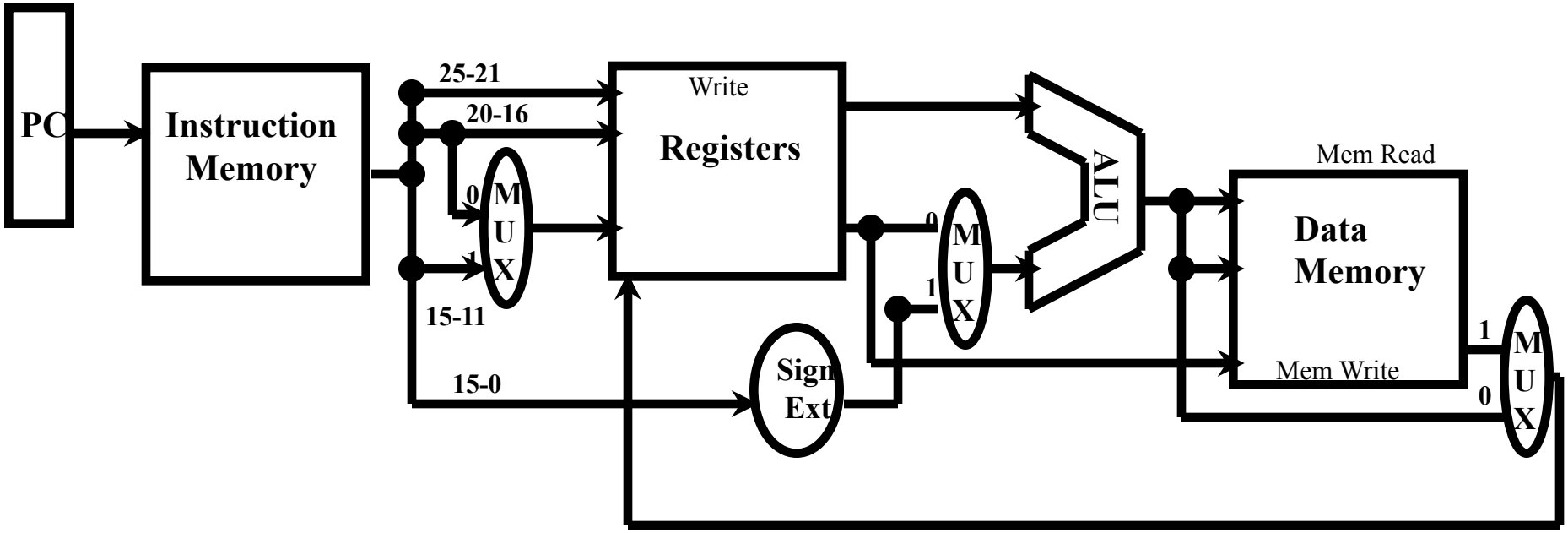
Load/Store Instruction Path

e.g., sw $t0, 100($s0)



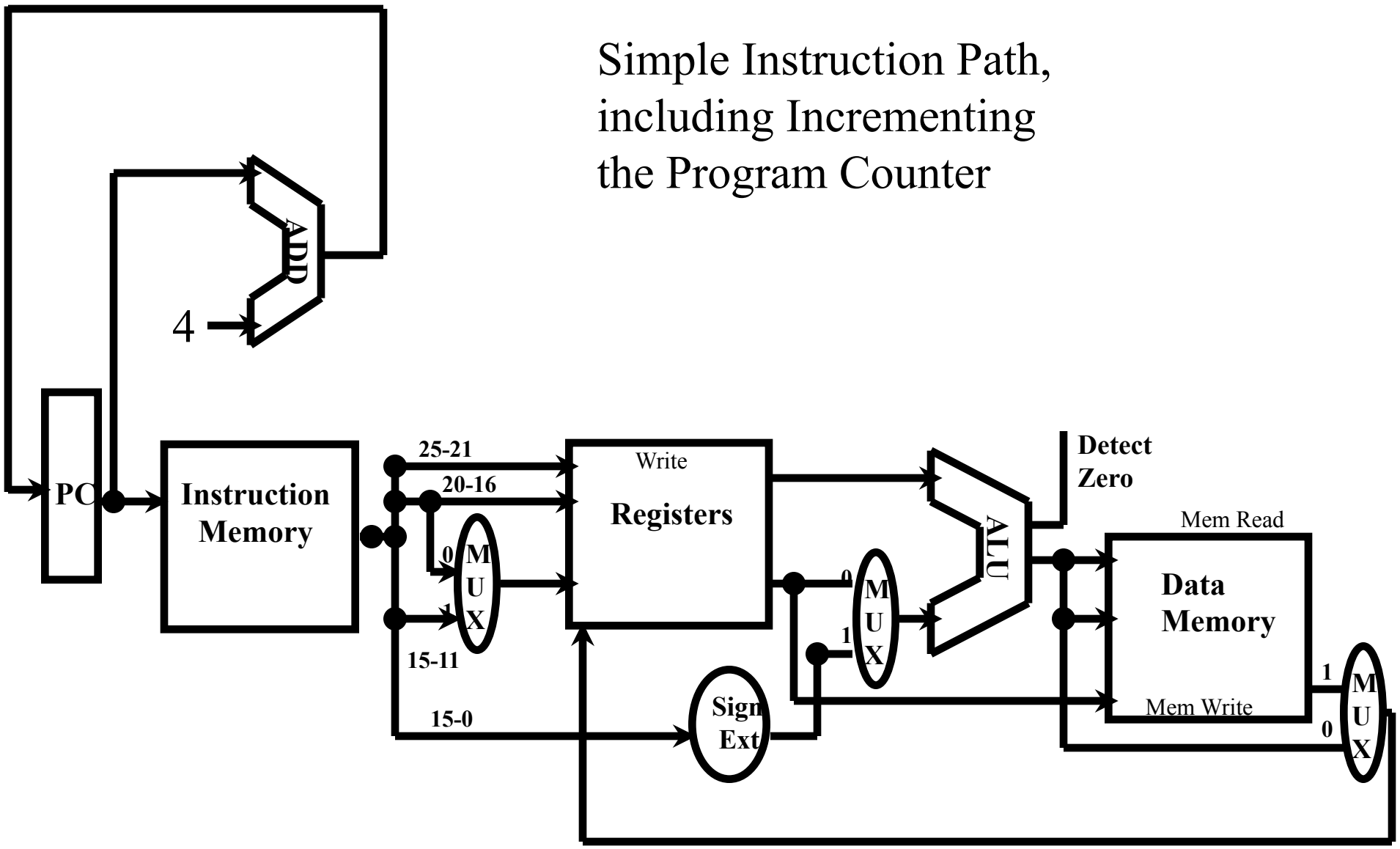
Load/Store Instruction Path

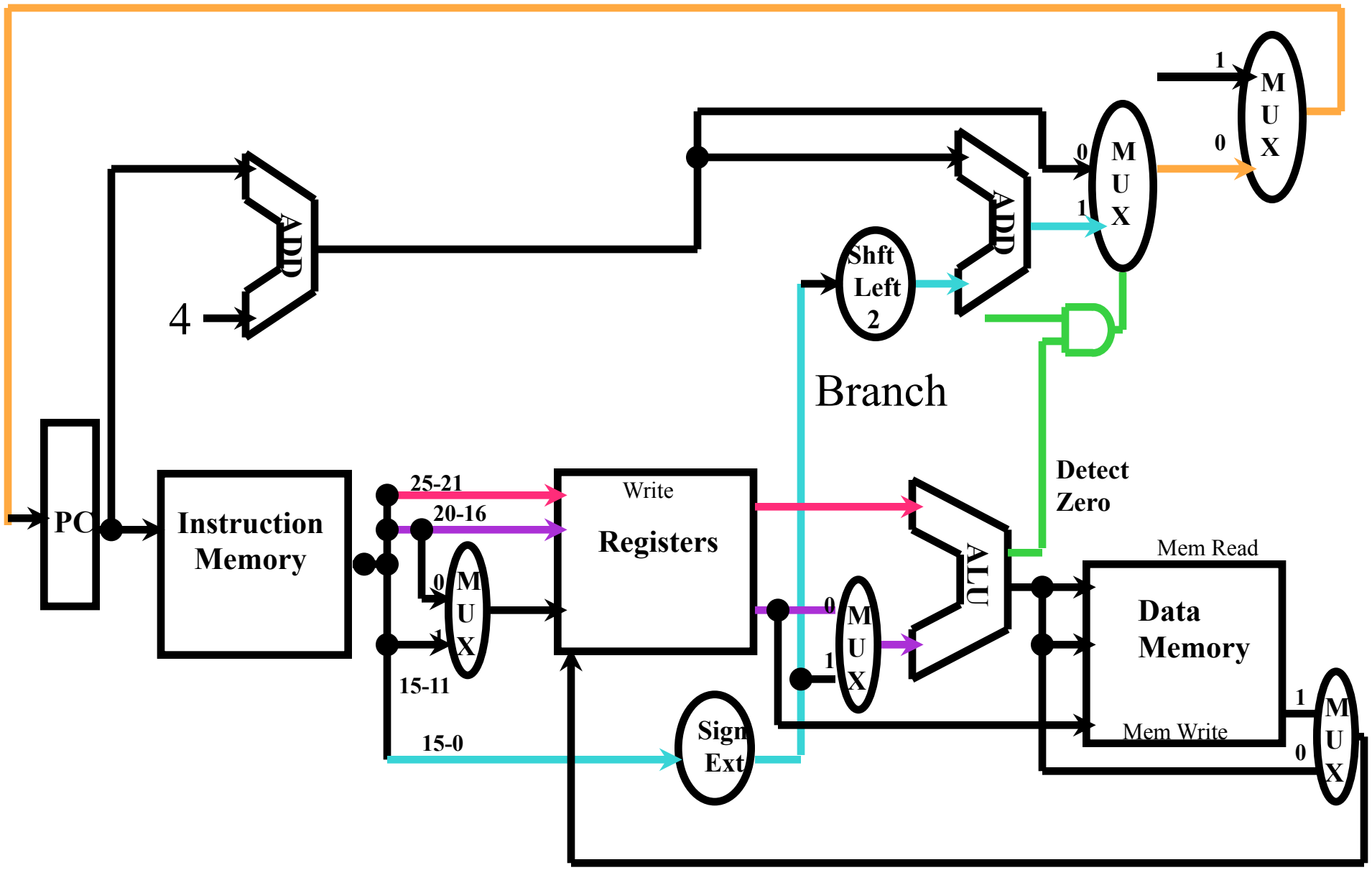
e.g., lw $t0, 100($s0)



Instruction Path with Instruction from Memory

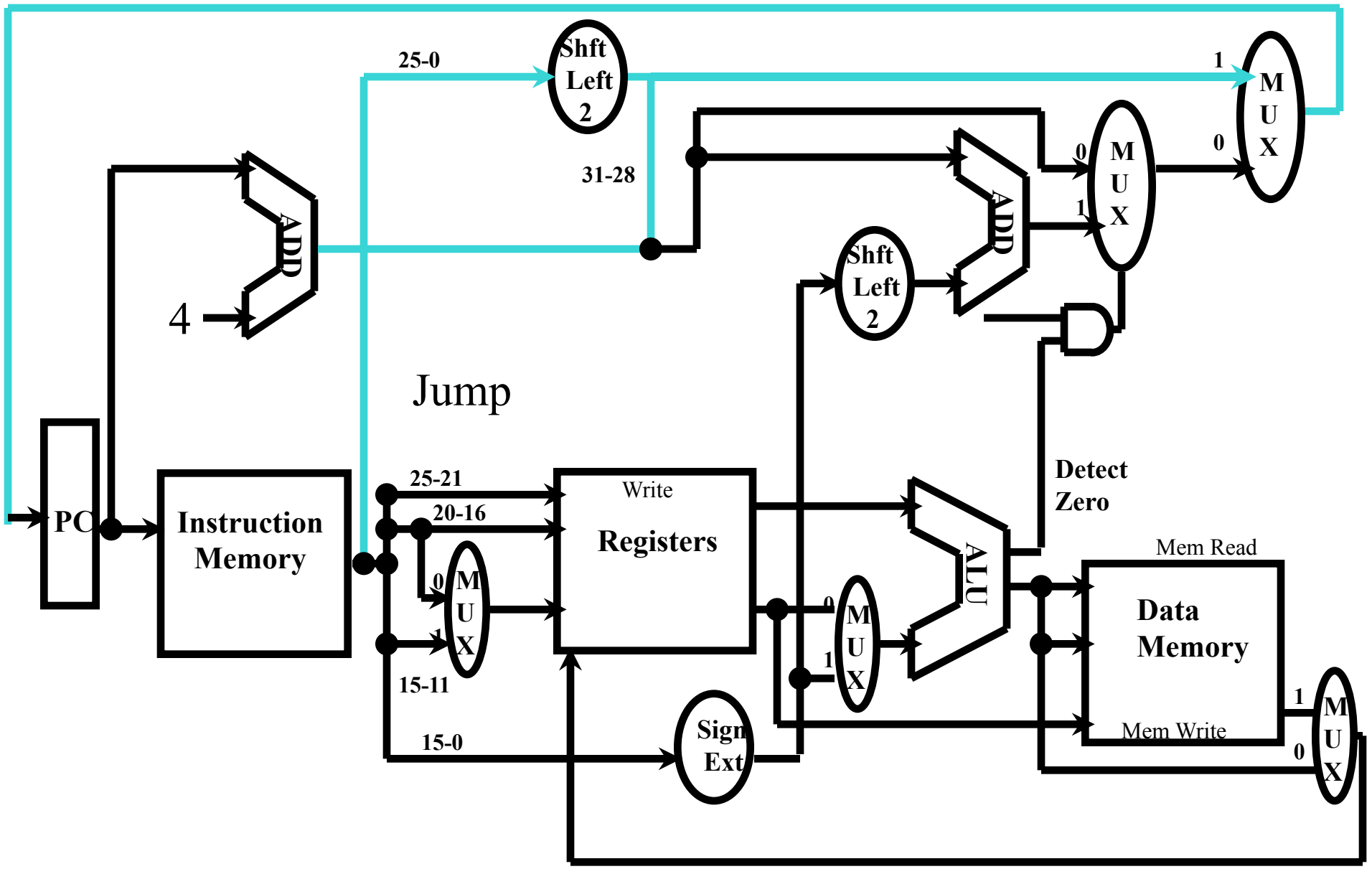
Simple Instruction Path, including Incrementing the Program Counter





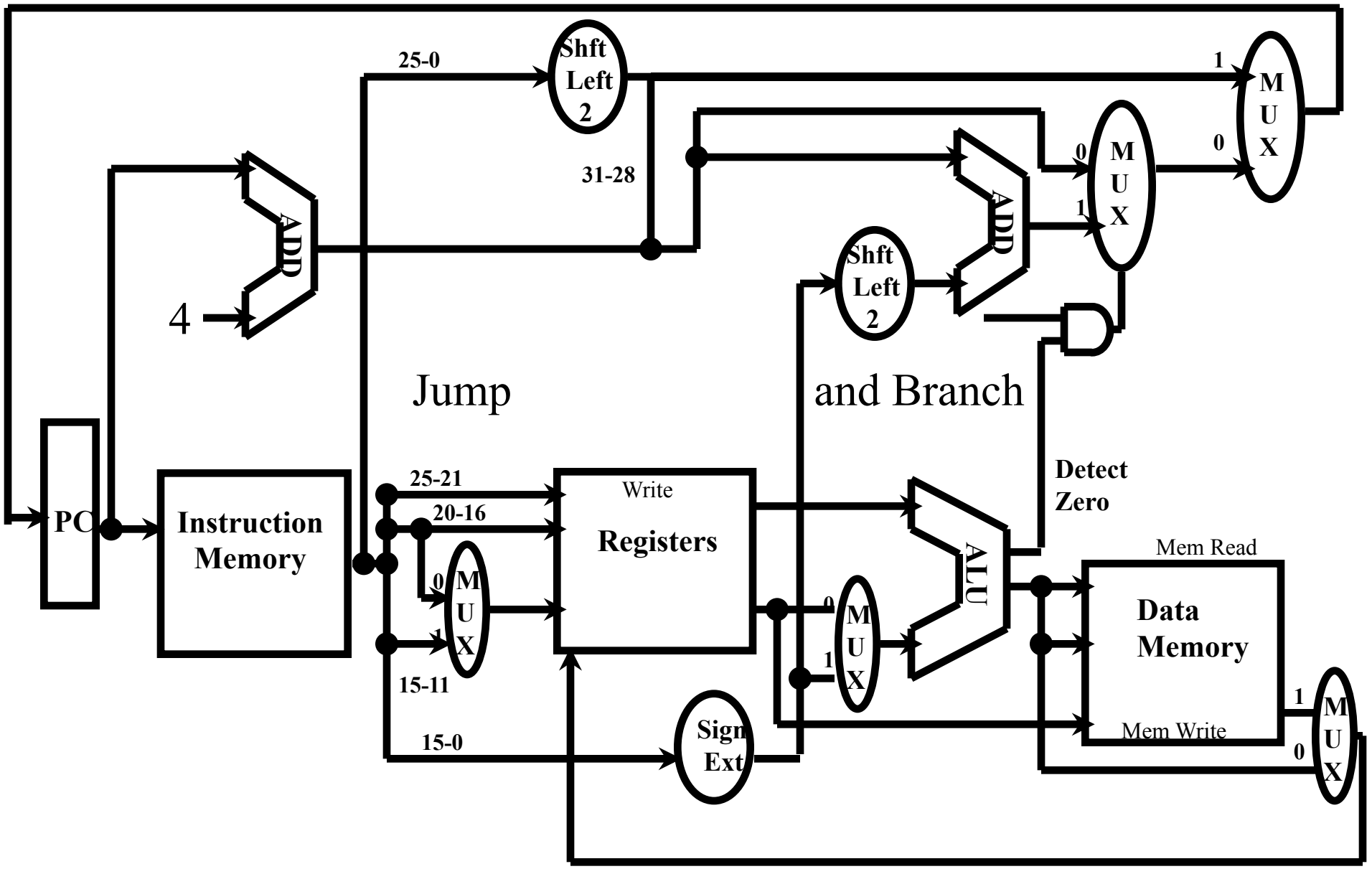
Branch Instruction Path

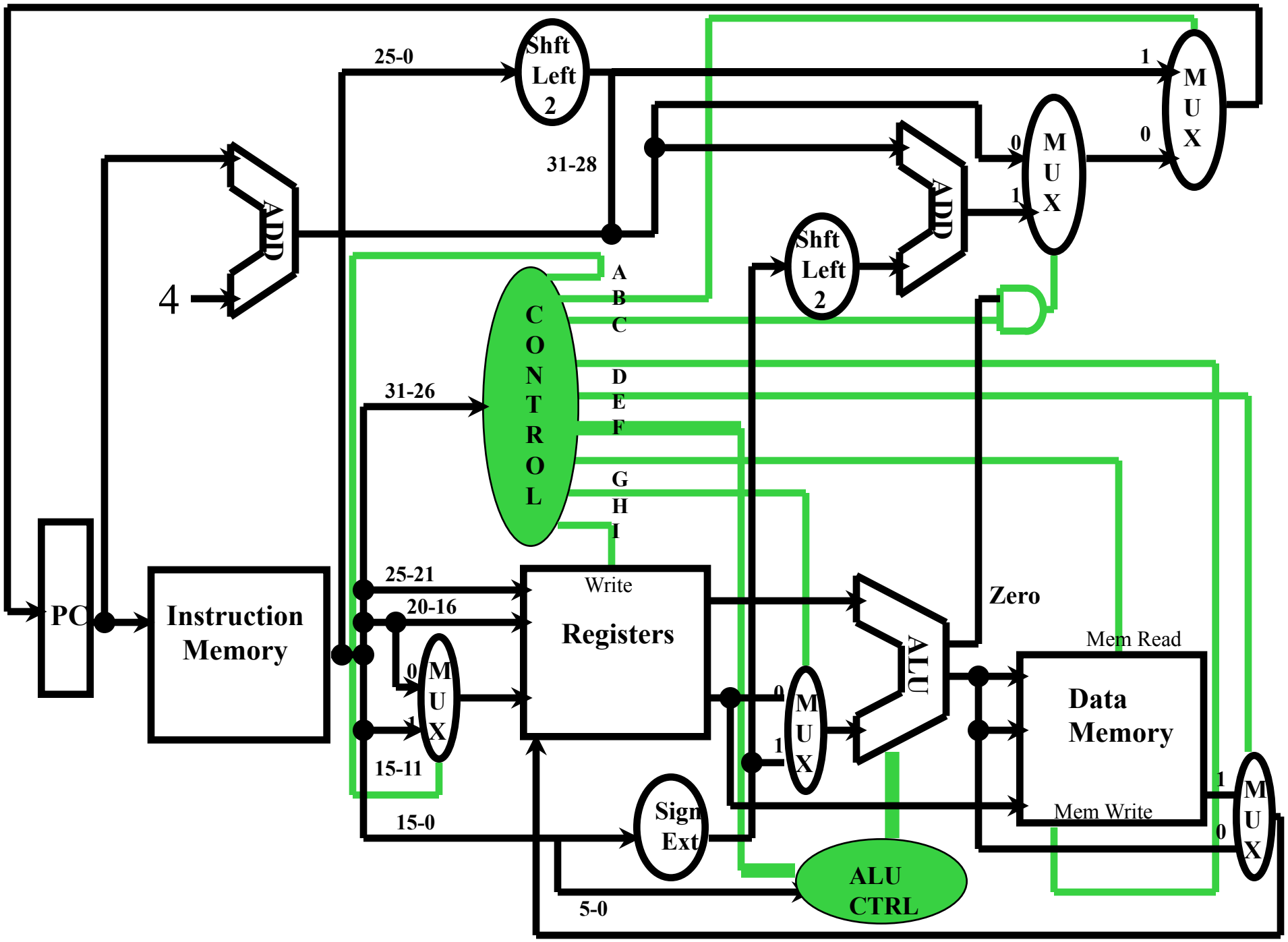
e.g., beq $s0, $zero, addr



Jump Instruction Path

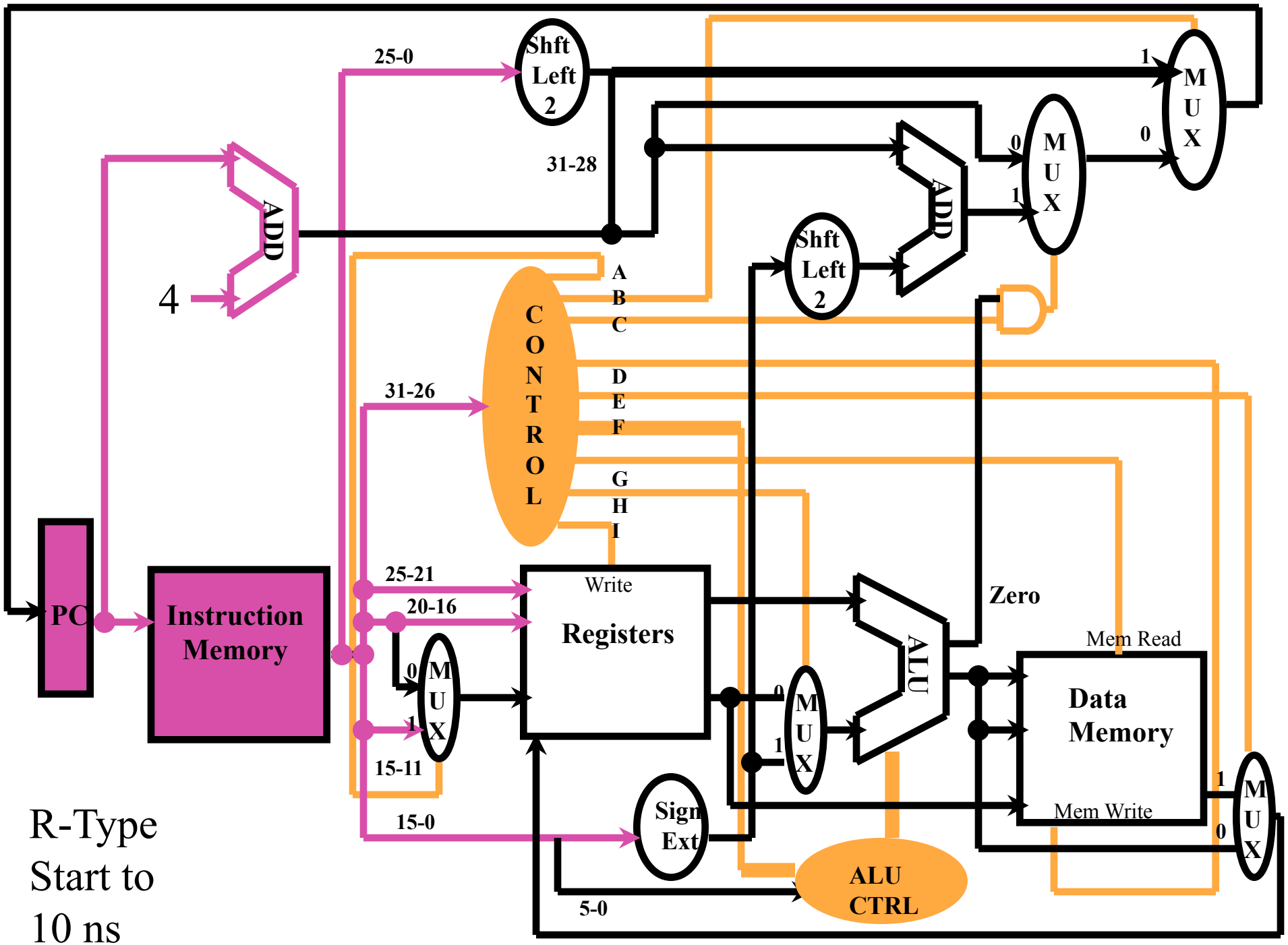
e.g., j addr


25-0
Shft Left 2
1
M U X
0
31-28
0
M U X
1
ADD
ADD
4
Shft Left 2
Jump
and Branch
Detect Zero
PC
Instruction Memory
25-21
20-16
Write
Registers
ALU
Mem Read
0
M U X
1
Data Memory
15-11
15-0
Sign Ext
Mem Write
1
M U X
0

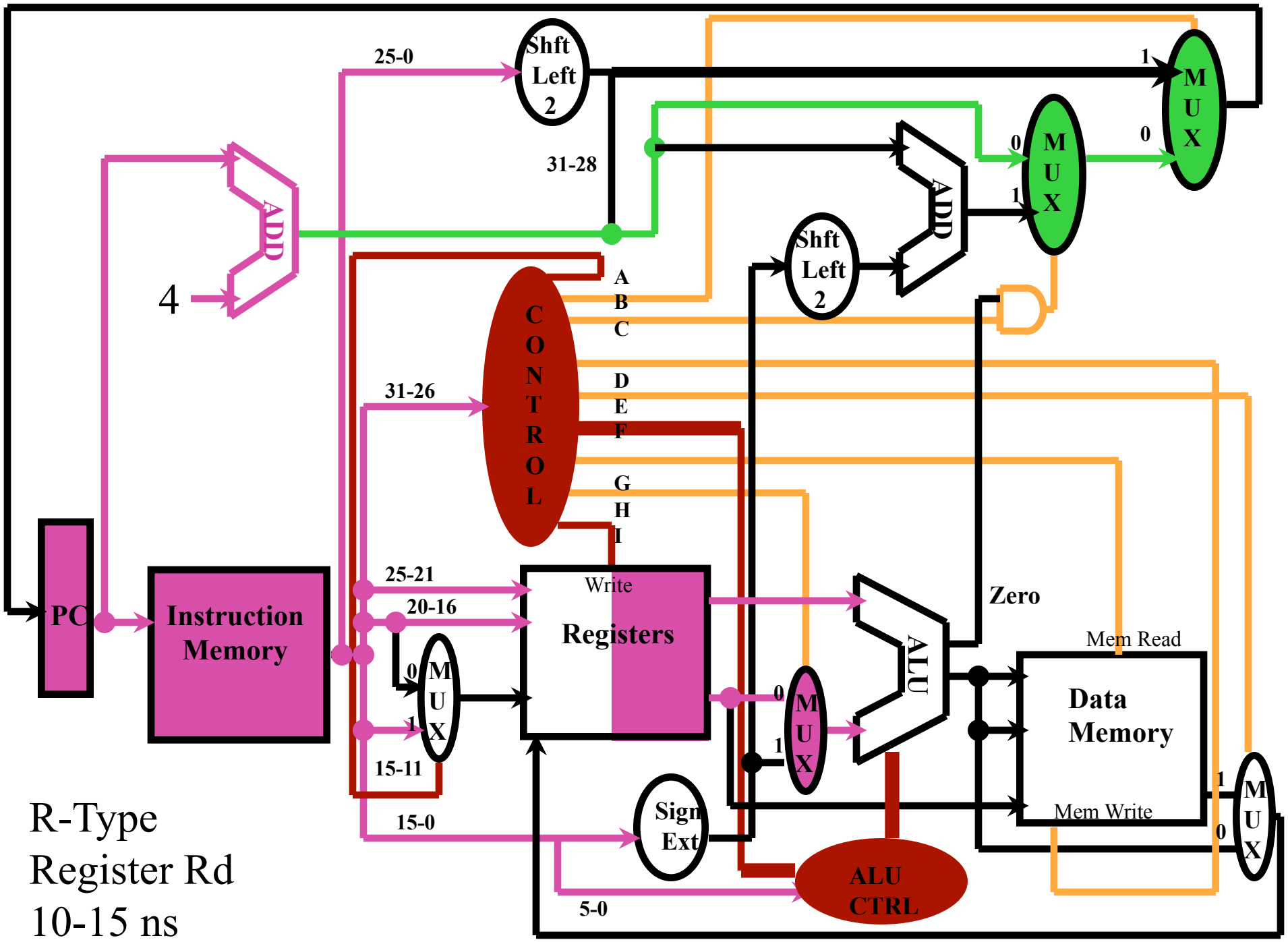

25-0
Shft Left 2
1
M U X
0
31-28
ADD
0
M U X
1
ADD
4
Shft Left 2
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
Zero
ALU
Mem Read
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0

Control Lines, Top to Bottom

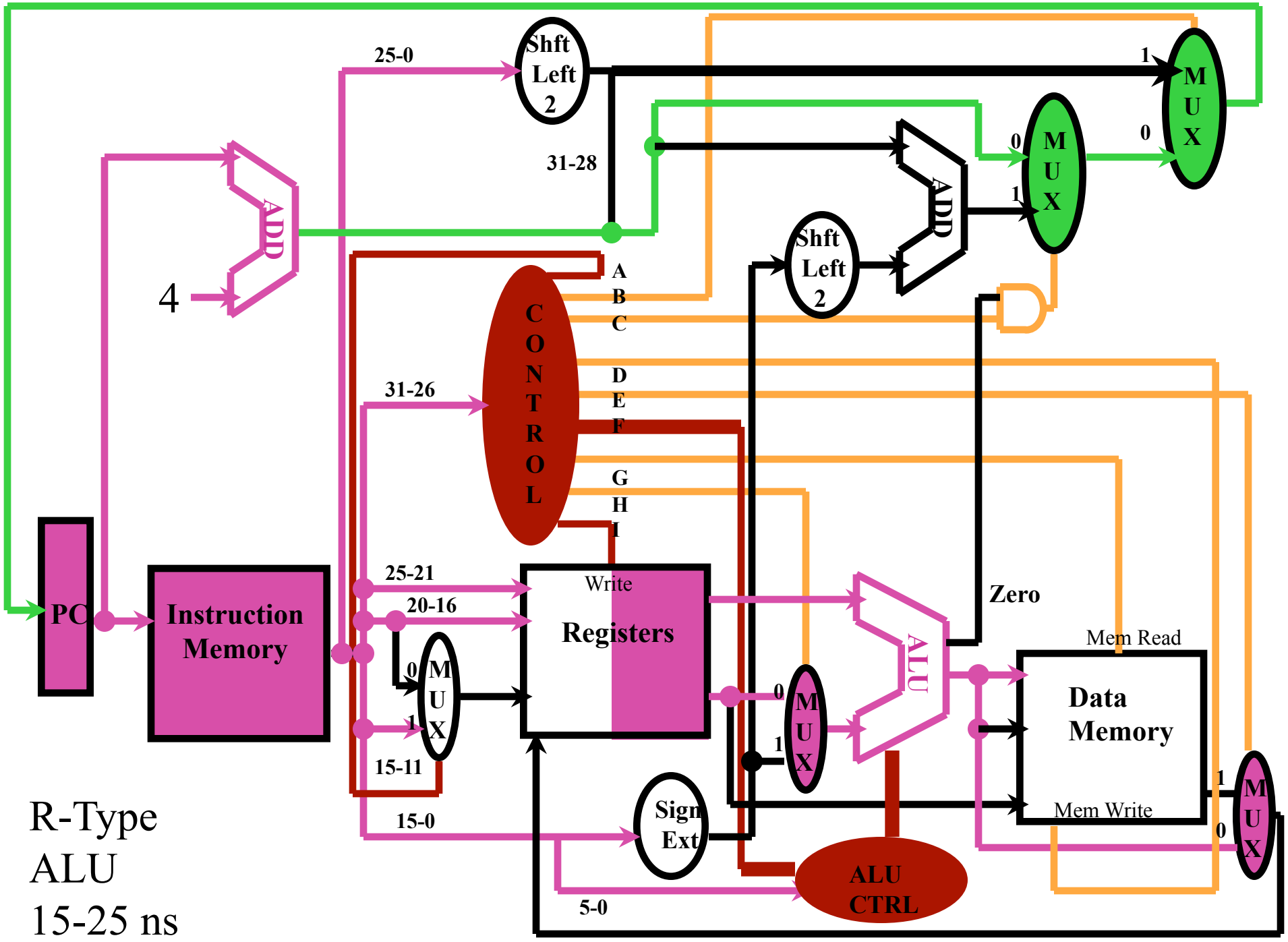
- A RegDst
- B Jump
- C Branch
- D MemWrite
- E MemToReg
- F ALUOp
- G MemRead
- H ALUSrc
- I RegWrite



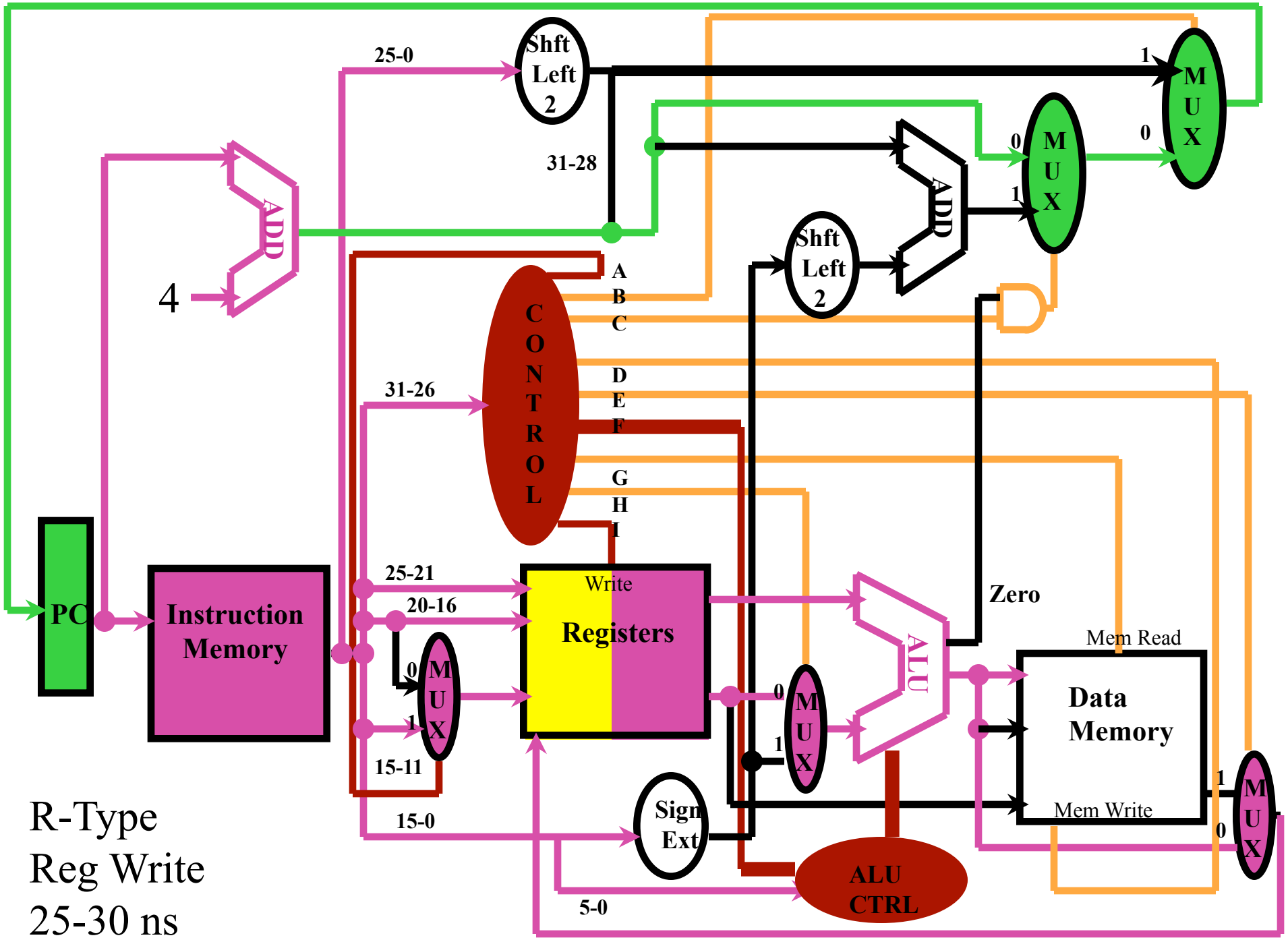
R-Type
Start to
10 ns

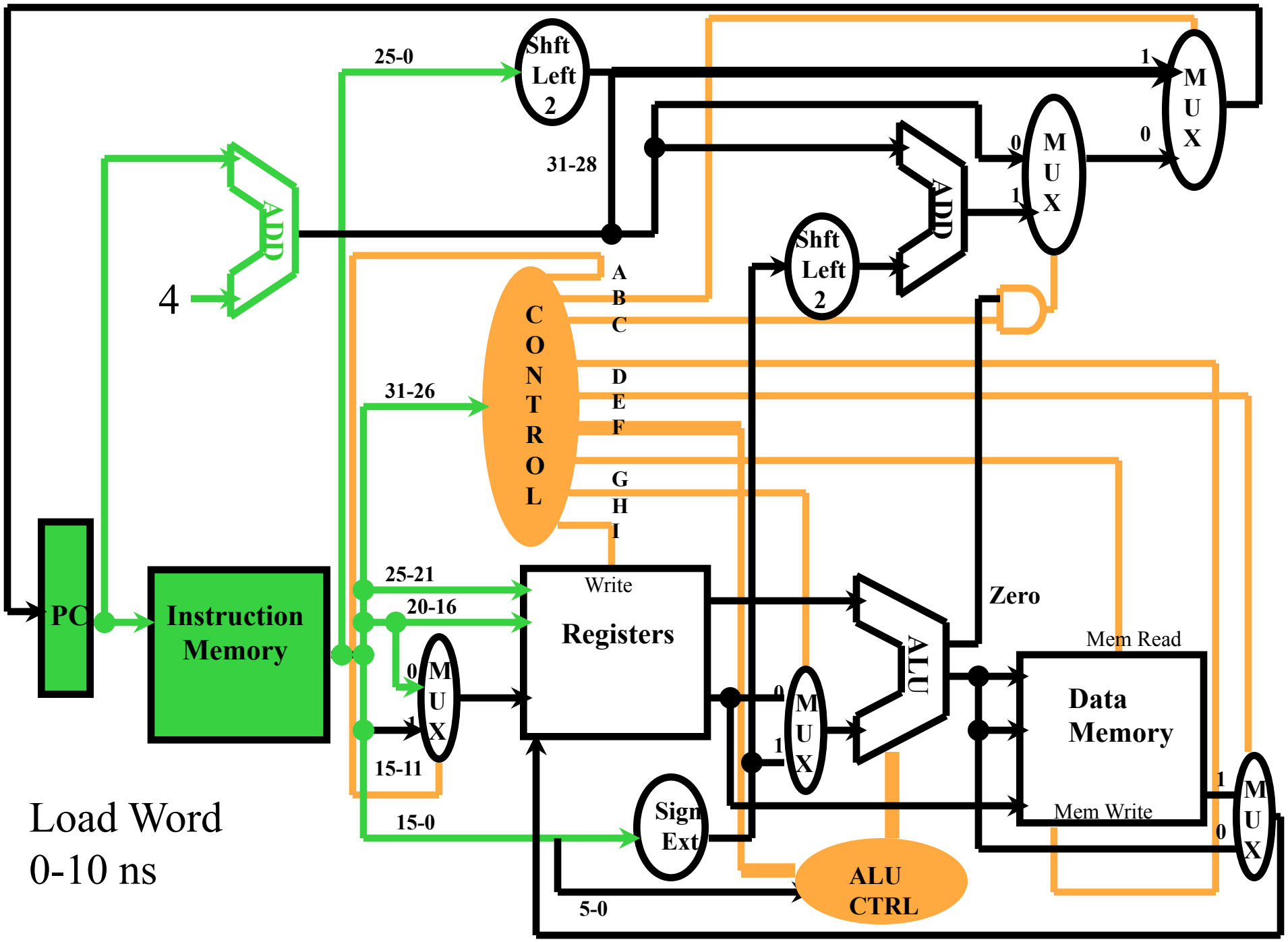


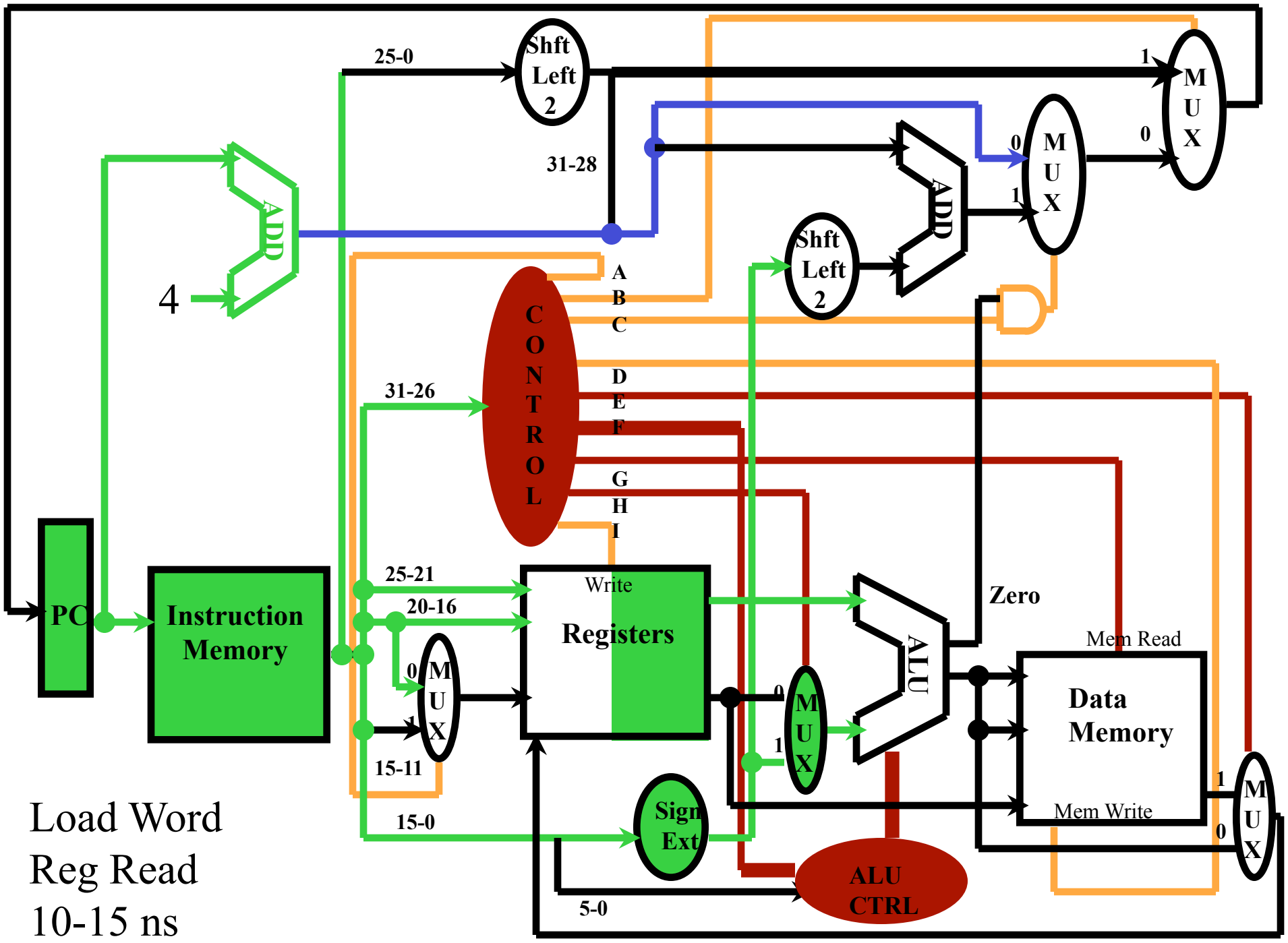
R-Type
Register Rd
10-15 ns

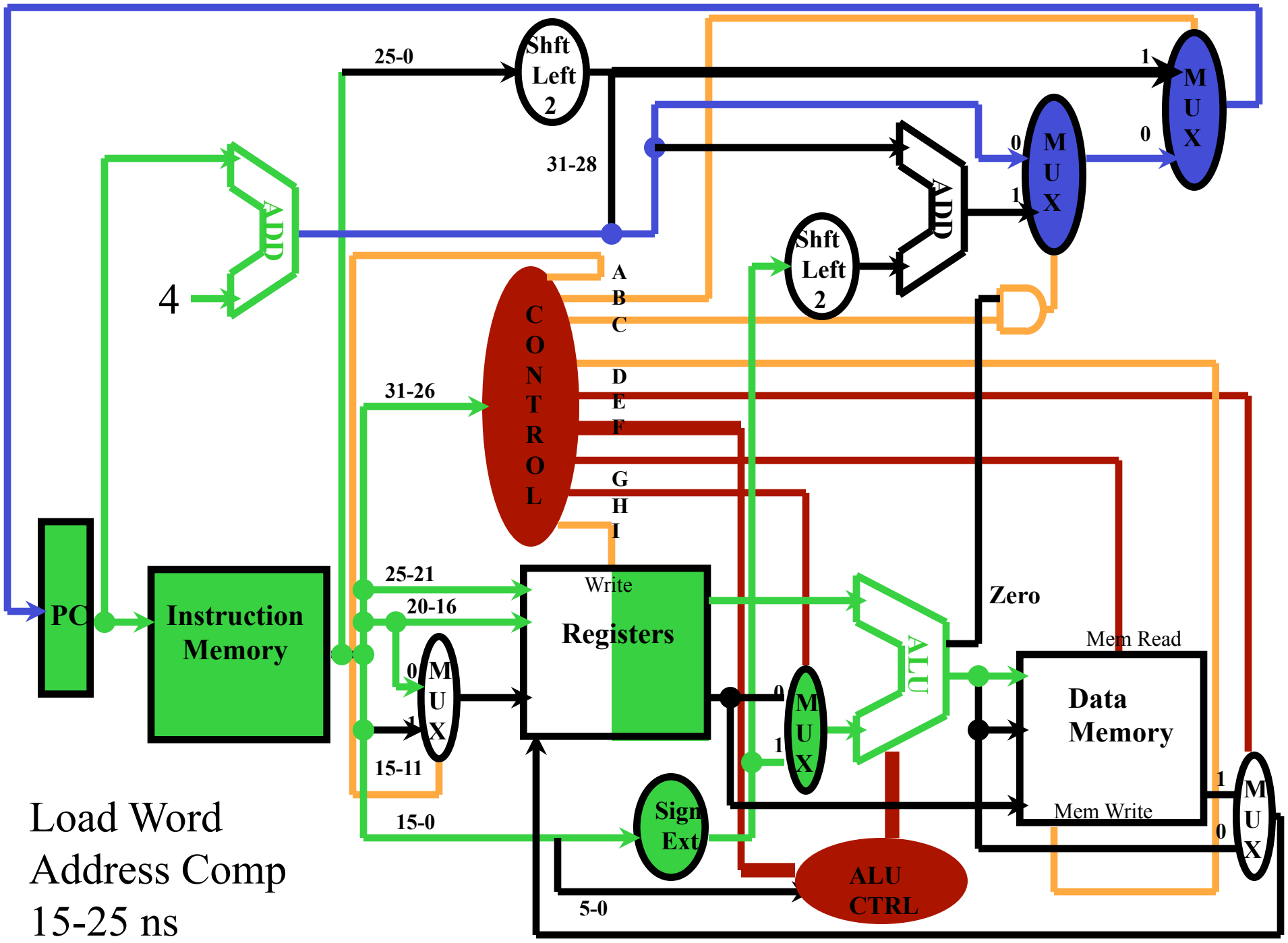


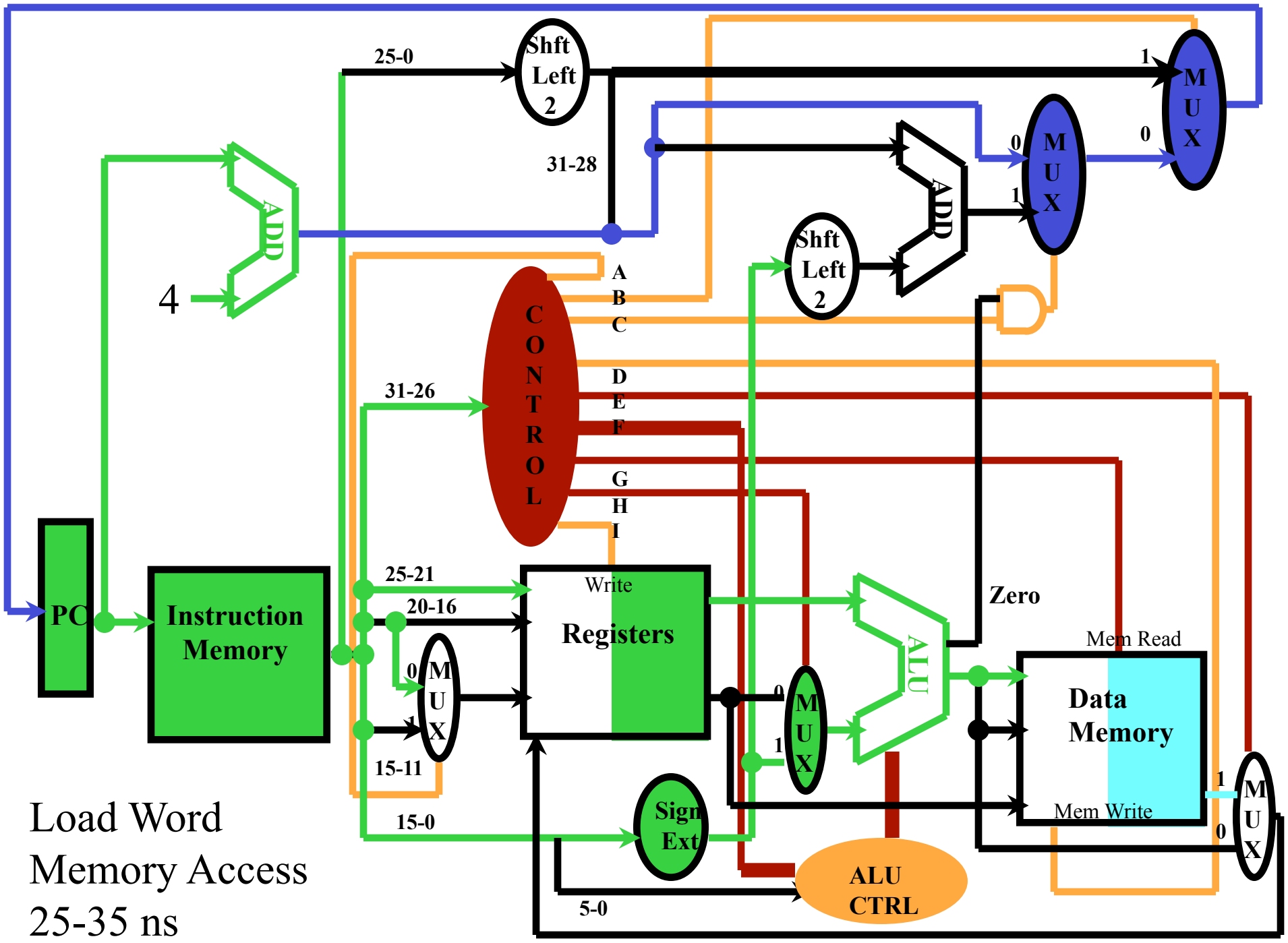
R-Type
ALU
15-25 ns


25-0
Shft Left 2
1
M U X
0
31-28
ADD
0
M U X
1
ADD
Shft Left 2
4
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
ALU
Zero
Mem Read
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0
R-Type
Reg Write
25-30 ns

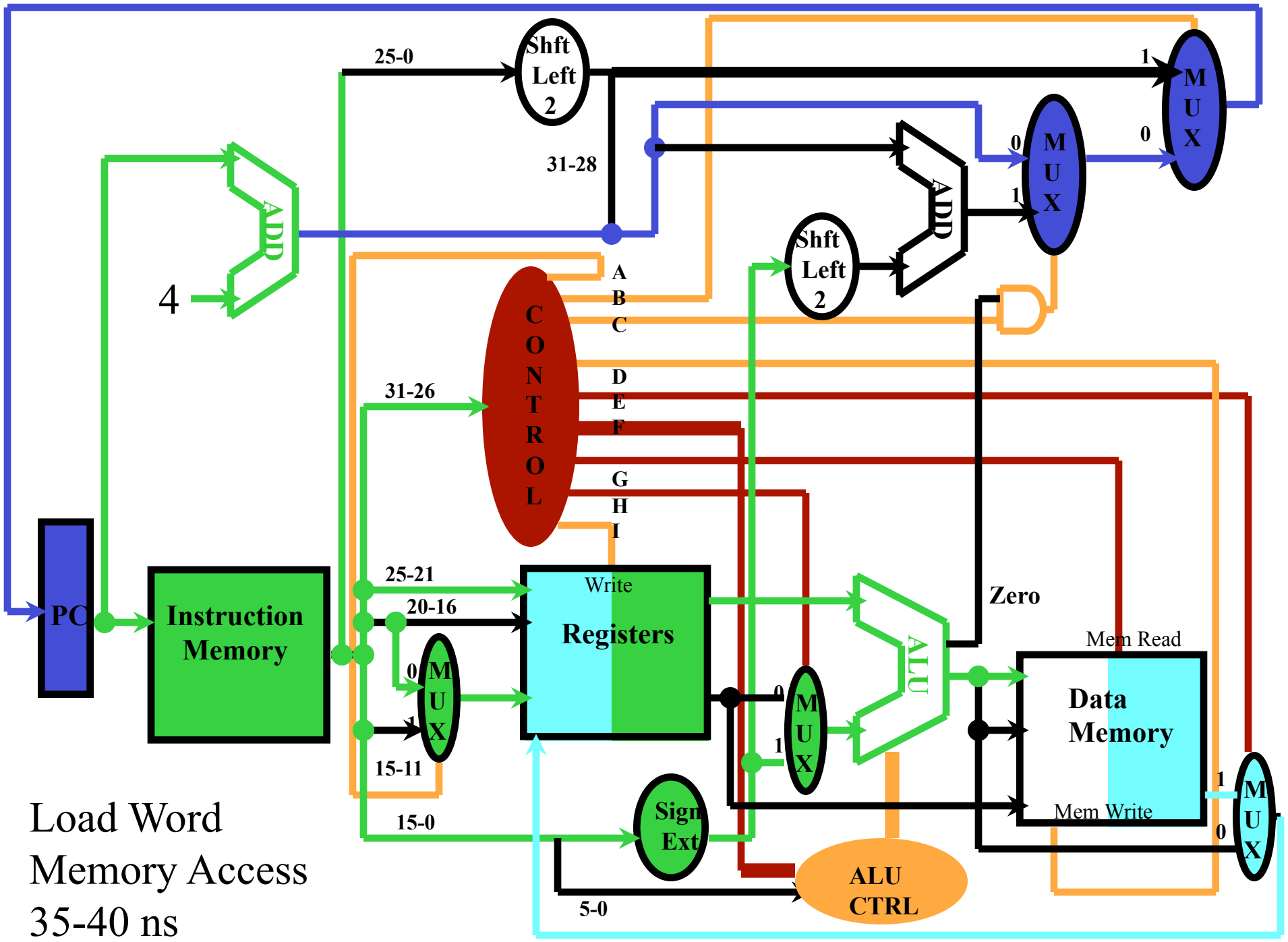

25-0
Shft Left 2
1
M U X
0
31-28
ADD
0
M U X
1
ADD
4
Shft Left 2
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
ALU
Zero
Mem Read
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0
Load Word
0-10 ns


25-0
Shft Left 2
1
M U X
0
31-28
0
M U X
1
ADD
ADD
4
Shft Left 2
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
ALU
Zero
Mem Read
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0
Load Word
Reg Read
10-15 ns

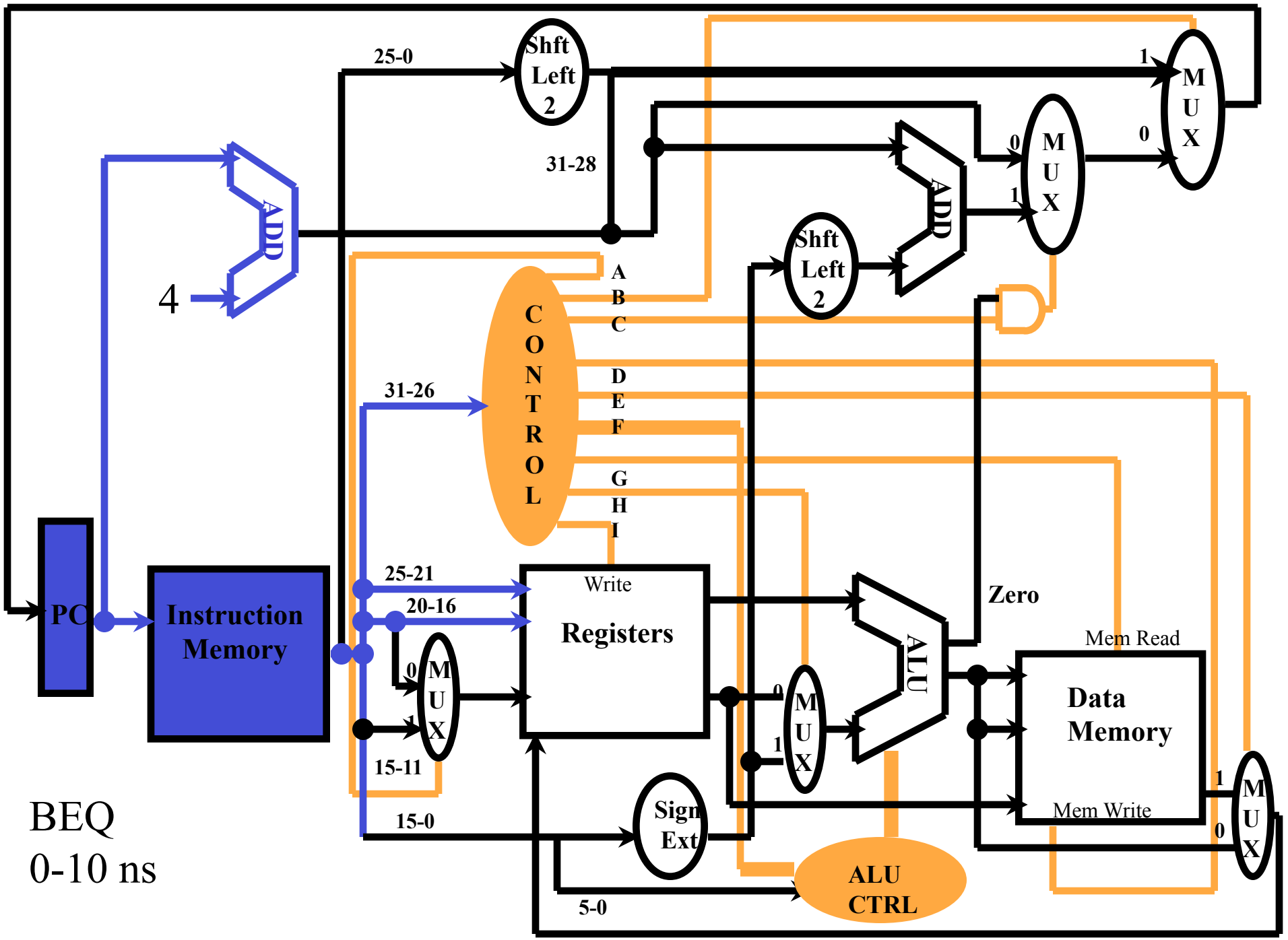

25-0
Shft Left 2
1
M U X
0
31-28
0
M U X
1
ADD
Shft Left 2
ADD
4
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
ALU
Zero
Mem Read
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0
Load Word
Address Comp
15-25 ns

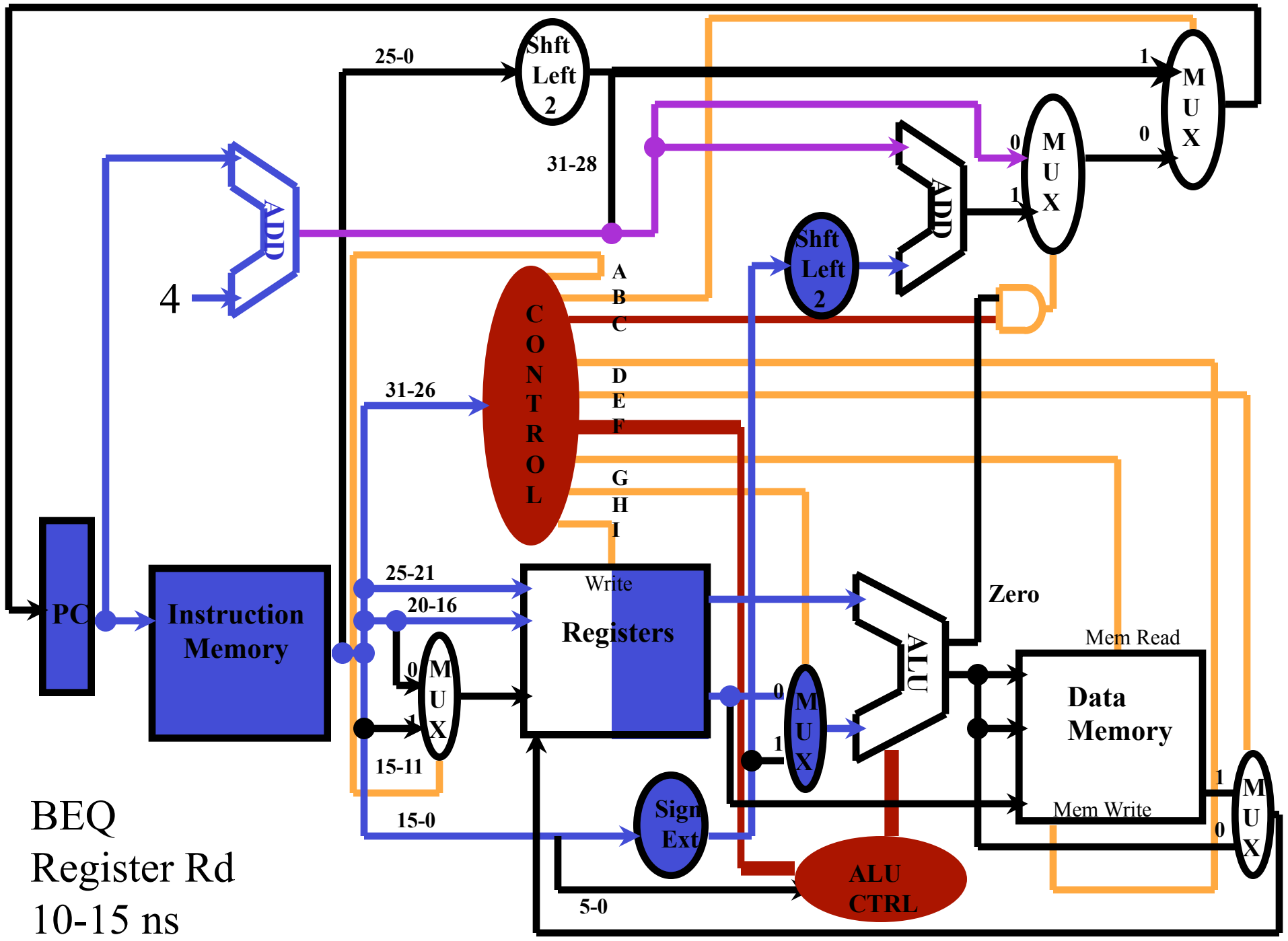


Load Word
Memory Access
25-35 ns

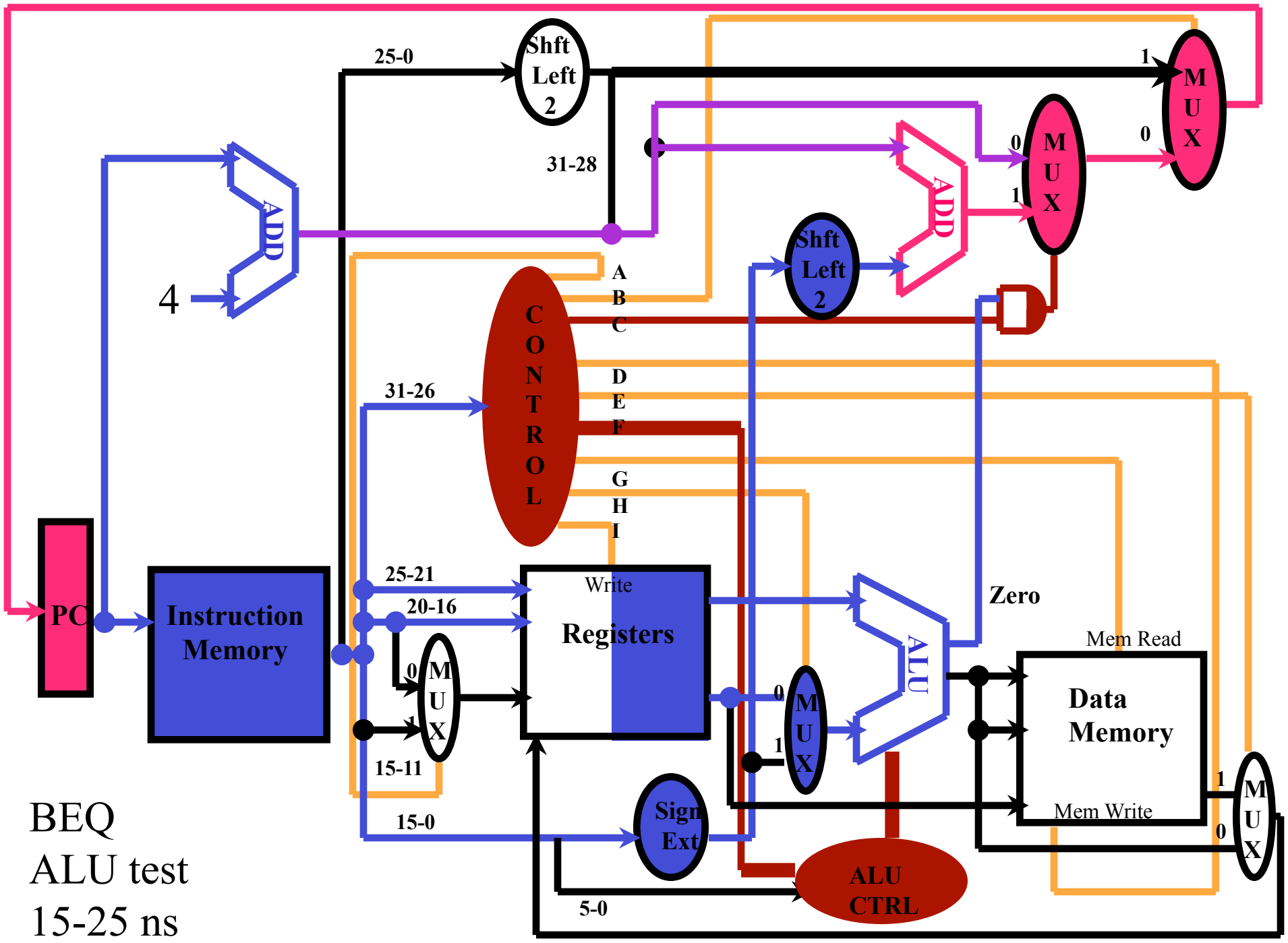


Load Word
Memory Access
35-40 ns


25-0
Shft Left 2
1
M U X
0
31-28
ADD
0
M U X
1
ADD
4
Shft Left 2
A
B
C
CONTROL
D
E
F
G
H
I
31-26
PC
Instruction Memory
25-21
20-16
Write
Registers
0
M U X
1
15-11
15-0
Sign Ext
0
M U X
1
ALU
Zero
Mem Read
Data Memory
Mem Write
1
M U X
0
ALU CTRL
5-0
BEQ
0-10 ns



BEQ
Register Rd
10-15 ns



BEQ
ALU test
15-25 ns