

Chhattisgarh Swami Vivekananda Technical University, Bhilai

Name of program: Bachelor of	Semester: III Code: B000311(014) Total Tutorial Periods: 01 Assignments: Two Maximum Marks: 100 Minimum
Technology Branch: All Branches	
Subject: Mathematics – III	
Total Theory Periods: 03	
Class Tests: Two (Minimum)	
ESE Duration: Three Hours	
Marks: 35	

Course Objectives:

1. To provide knowledge of Laplace transform of elementary functions including its properties and applications to solve ordinary differential equations.
2. To have thorough knowledge of partial differential equations which arise in mathematical descriptions of situations in engineering.
3. To study about a quantity that may take any of a given range of values that can't be predicted as it is but can be described in terms of their probability.
4. To provide a thorough understanding of interpolation and methods to solve ordinary differential equation.

UNIT-I Laplace transform: Definition, Transform of elementary functions, Properties of Laplace transform, Transform of derivatives & integrals, Multiplication by t^n , Division by t, Evaluation of integrals, Inverse Laplace Transform, Convolution theorem, Unit step function, Unit impulse function, Periodic function, Application to solution of ordinary differential equations.

UNIT- II Partial differential equation: Formation, Solution by direct integration method, Linear equation of first order, Homogeneous linear equation with constant coefficients, Non-homogeneous linear equations, Method of separation of variables.

UNIT- III Random variable: Discrete and continuous probability distributions, Mathematical expectation, Mean and Variance, Moments, Moment generating function, probability distribution, Binomial, Poisson and Normal distributions.

UNIT- IV Interpolation with equal and unequal intervals: Finite differences, Newton's Forward & Backward Difference Formulae, Central Difference Formula, Stirling's Formula, Bessel's Formula, Lagrange's Formula and Newton's Divided Difference Formula.

UNIT-V Numerical Solution of Ordinary Differential Equations: Picard's Method, Taylor's Series Method, Euler's Method, Euler's Modified Method, Runge-Kutta Methods, Predictor-corrector Methods- Milne's Method, Adams-Bashforth Method.

Text Books:

1. "Higher Engg. Mathematics", Dr. B.S. Grewal– Khanna Publishers.
2. "Advanced Engg. Mathematics" , Erwin Kreyszig – John Wiley & Sons.
3. "Numerical Methods in Engineering and Science" , Dr. B.S. Grewal, Khanna Publishers.
4. "Numerical Methods for Scientific and Engineering Computation" , M .K. Jain, S. R. K

Reference Books:

1. "Applied Mathematics", P. N. Wartikar& J. N. Wartikar. Vol-II Pune Vidyarthi Griha Prakashan, Pune.
2. "Applied Mathematics for Engineers & Physicists", Louis A. Pipes- TMH.
3. "Numerical Methods for Scientists and Engineers" K. Shankar Rao, Prentice Hall of India.
4. "Numerical Methods" P. Kandasamy, K. Thilagavathy and K. Gunavathi, S. Chand publication.

Course outcomes: After studying the contents of the syllabus in detail the students will be able to: Define (mathematically) unit step unit impulse, Laplace transform its properties, inverse and applications to solve ordinary differential equations and find Numerical solution of differential equations, which may be arising due to mathematical modelling based on engineering problems. Hands on these Mathematical topics will make them equipped to prepare for higher studies through competitive examinations.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Principles of Programming Languages	Course Code: B022313(022)
Total / Minimum-Pass Marks (End Semester Exam): 100 / 35	L: 2 T: 1 P: 0 Credits: 3
Class Tests & Assignments to be conducted: 2 each	Duration (End Semester Exam): 03 Hours

UNIT- I Program Design: Introduction- fundamental design concepts - Modules and modularization criteria – Design notation: Procedure template, Pseudo code - Structured flow chart decision. Tables - Design techniques: Stepwise refinement, Levels of abstraction, Top down- Test Plans-Design guidelines.

UNIT-II Programming language processors: Characteristics of programming languages, Factors influencing the evolution of programming language, Development in programming methodologies, desirable features and design issues, Structure and operations of translators, software simulated computer, syntax, semantics, structure, virtual computers, binding and binding times, storage management comparisons.

UNIT- III Functional & Logic programming languages: Introduction, comparison and applications of functional and logic programming languages; fundamentals of LISP (Objects, Control constructs, List processing) & PROLOG (Syntax, Lists, Operators and arithmetic, Control constructs).

UNIT-IV Object-Oriented Programming Concepts-I: Introduction to Basic Object-Oriented Concepts: (Object, Class, Encapsulation, Abstraction, Data Hiding, Inheritance, Polymorphism, Message Passing), Basic structure of a C++ program, C++ Compiler, C++ Classes, Methods, Objects, Nested Class, Const, Static members, this pointer, Comparison between Pointer and Reference Variables, Comparison between New and Delete Operators.

UNIT-V Object-Oriented Programming Concepts-II: Constructor, Destructor, Function and Operator Overloading, Friend functions and Friend classes, Inheritance, Abstract classes, Polymorphism, Virtual Function and Classes, Dynamic Binding, Exception Handling and Templates.

Text Books:

1. “Software Engineering Concepts” by Richard Fairley, Tata McGraw Hill,
2. “Programming Languages, Design and implementation” by Terrance W. Pratt, and Marvin V. Zelkowitz, Prentice-Hall of India, Fourth edition, 2002.
3. E. Balagurusamy, Object Oriented Programming with C++, Tata McGraw Hill

Reference Books:

1. “Programming Languages – Concepts and Constructs” by Ravi Sethi, Addison-Wesley, 2nd Ed. 1996.
2. “Programming Languages: Principles and Paradigms” by Allen B. Tucker, Robert Noonan, TMH, 2006.

Course Outcomes [After undergoing the course, students will be able to:]

1. Obtain broad understanding of the role of computer science, fundamental software design concepts and notations.
2. Get an overview of various programming language paradigms, processors & software simulation types.
3. Understand key concepts in the implementation of common features of programming languages.
4. Acquire knowledge of basic concepts about object-oriented programming languages.
5. Program in object-oriented programming language paradigm using various computational methods.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Data Structures & Algorithms	Course Code: B022312(022)
Total / Minimum-Pass Marks (End Semester Exam): 100 / 35	L: 3 T: 1 P: 0 Credits: 4
Class Tests & Assignments to be conducted: 2 each	Duration (End Semester Exam): 03 Hours

UNIT- I Introduction: Basic Terminology, Elementary Data Organization, Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations: Big-Oh, Time-Space trade-off. Abstract Data Types (ADT) Arrays: Definition, Single and Multidimensional Arrays, Row Major & Column Major Order Representation of Arrays, Application of arrays, Sparse Matrices and their representations. Linked lists: Array Implementation and Dynamic Implementation of Singly Linked Lists, Doubly Linked List, Circularly Linked List, Operations on a Linked List. Insertion, Deletion, Traversal, Polynomial Representation and Addition, Generalized Linked List.

UNIT-II Stacks: Abstract Data Type, Primitive Stack operations: Push & Pop, Array and Linked Implementation of Stack in C, Application of stack: Prefix and Postfix Expressions, Evaluation of postfix expression, Recursion, Tower of Hanoi Problem, Simulating Recursion, Principles of recursion, Tail recursion, Removal of recursion Queues, Operations on Queue: Create, Add, Delete, Full and Empty, Circular queues, Array and linked implementation of queues in C, Dequeue and Priority Queue.

UNIT- III Trees: Basic terminology, Binary Trees, Binary Tree Representation: Array Representation and Dynamic Representation, Complete Binary Tree, Algebraic Expressions, Extended Binary Trees, Array and Linked Representation of Binary trees, Search Trees: Binary Search Trees (BST), Insertion and Deletion in BST Trees, Traversal algorithms: Inorder, Preorder and Postorder, Threaded Binary trees, Traversing Threaded Binary trees.

UNIT-IV Graphs: Terminology, Sequential and linked Representations of Graphs: Adjacency Matrices, Adjacency List, Adjacency Multi list, Graph Traversal: Depth First Search and Breadth First Search, Connected Component, Spanning Trees, Minimum Cost Spanning Trees: Prims and Kruskal algorithm. Transistive Closure and Shortest Path algorithm: Warshal Algorithm and Dijikstra Algorithm.

UNIT-V Searching: Sequential search, Binary Search, Comparison and Analysis Internal Sorting: Insertion Sort, Selection, Bubble Sort, Quick Sort, Two Way Merge Sort, Heap Sort, Radix Sort, Tree (BST) Sort; Complexity of Search Algorithm, AVL trees, Introduction to m-way Search Trees, B Trees & B+ Trees, Hashing: Hash Function, Collision Resolution Strategies, Storage Management: Garbage Collection and Compaction.

Text books:

1. Aaron M. Tenenbaum, YedidyahLangsam and Moshe J. Augenstein “Data Structures Using C and C/C++”, PHI
2. Horowitz and Sahani, “Fundamentals of Data Structures”, Galgotia Publication.
3. Lipschutz, “Data Structures” Schaum’s Outline Series, TMH

References books:

1. Jean Paul Trembley and Paul G. Sorenson, “An Introduction to Data Structures with applications”, McGraw Hill
2. R. Kruse etal, “Data Structures and Program Design in C”, Pearson Education
3. G A V Pai, “Data Structures and Algorithms”, TMH

Course Outcomes [After undergoing the course, students will be able to:]

1. Have a comprehensive knowledge of the data structures and algorithms on which file structures and data bases are based.
2. Understand the importance of data and be able to identify the data requirements for an application.
3. Have in depth understanding and practical experience of algorithmic design and implementation.
4. Have practical experience of developing applications that utilize databases.
5. Understand the issues involved in algorithm complexity and performance.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Digital Electronics	Course Code: B022314(022)
Total / Minimum-Pass Marks (End Semester Exam): 100 / 35	L: 3 T: 1 P: 0 Credits: 4
Class Tests & Assignments to be conducted: 2 each	Duration (End Semester Exam): 03 Hours

UNIT- I Digital Fundamentals: Weighted & Non-weighted codes, Sequential codes, self-complementing codes, Cyclic codes, 8-4-2-1 BCD code, Excess-3 code, Gray code: Binary to Gray and Gray to binary code conversion, Error detecting code, Error correcting code, 7-bit Hamming code, ASCII code, Binary Arithmetic, Boolean Algebra, Minimization of Switching Function , Demorgan's Theorem, Karnaugh's Map Method, Quine-McCluskey's Method (Tabular Method). Basic and Universal logic Gates, Realization of switching functions using gates.

UNIT-II Digital Logic Families and Memory: Transistor Inverter: Basic Concepts of RTL and DTL; TTL: Open collector gates, TTL subfamilies, IIL, ECL; MOS Logic: CMOS Logic, Dynamic MOS Logic, Interfacing: TTL to ECL, ECL to TTL, TTL to CMOS, CMOS to TTL, and Comparison among various logic families. Memories: ROM and RAM, PLA, PAL and FPGA;

UNIT- III Combinational Circuits: Adder & Subtractor: Half adder, Full adder, Half-subtractor, Full-subtractor, Parallel Binary adder, Look Ahead carry adder, Serial adder, BCD adder. Code converter, Parity bit generator/Checker, Comparator. Decoder: 3-line to 8-line decoder, 8-4-2-1 BCD to Decimal decoder, BCD to Seven segment decoder. Encoder: Octal to binary and Decimal to BCD encoder. Multiplexer: 2-input multiplexer, 4-input multiplexer. De- multiplexer: 1-line to 4-line, study of Multiplexer as Universal Logic Function Generator.

UNIT-IV Sequential Circuits: Flip-Flops: SR, JK, T, D, Master/Slave JK FF and their conversion, Excitation Tables. Introduction to registers (SISO, SIPO, PIPO, PISO) and Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

UNIT-V Machines and Application: Finite State Machine, Mealy Machine, Moore Machine, **Introduction to VHDL:** Behavioral – data flow and algorithmic and structural description, lexical elements, data objects types, attributes, operators; VHDL coding examples.

Text Books:

1. R. P. Jain: "Modern Digital electronics", TMH.
2. B. Somanathan Nair, "Digital Electronics & Logic Design", Prentice-Hall of India.
3. Pedroni V.A., "Digital Circuit Design with VHDL", Prentice Hall, India 2nd Edition.

Reference Books:

1. R J Tocci, "Digital System principles and Applications"
2. "Digital Electronics " by A.K.Maini, Wiley India.
3. M.M. Mano: "Digital logic and computer design", PHI.
4. Floyd: "Digital fundamentals", UBS.

Course Outcomes [After undergoing the course, students will be able to:]

1. Apply digital coding concepts to simplify circuit design.

2. Analyze the operations of various logic families and different semiconductor memories.
3. Design and implement various combinational circuits
4. Outline the concepts of latch circuits, flip flops and counters.
5. Design and develop basic digital systems using VHDL.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Operating System	Course Code: B022315(022)
Total / Minimum-Pass Marks (End Semester Exam): 100 / 35	L: 3 T: 1 P: 0 Credits: 4
Class Tests & Assignments to be conducted: 2 each	Duration (End Semester Exam): 03 Hours

UNIT- I Introduction: Operation System objectives and functions, The Evolution of operating Systems, Batch Systems, interactive systems, time sharing and real time systems, Protection. Operating System Structure, System Components, operating system service, System structure. Distributed Computing.

UNIT-II Concurrent Processes: Process concept: Introduction, Definitions, Process States, Process State Transitions, The process Control Block, Operations on Processes, Suspend and Resume, Interrupt Processing. Mutual Exclusion, the Producer / Consumer problem, the critical section problem, Semaphores, Classical problems in concurrency, inter process communication. CPU scheduling: concepts, performance criteria, and scheduling Algorithms. Algorithm evaluation, Multiprocessor scheduling.

UNIT- III Dead Locks: System model, Deadlock characterization. Prevention, Avoidance and Detection, Recovery from deadlock, combined approach.

UNIT-IV Memory Management: Base machine, Resident Monitor, multiprogramming with fixed partition, Multiprogramming with variable partitions, Paging, Segmentation, paged - segmentation, virtual Memory concepts, Demand paging, performance, Page Replacement algorithms, Allocation of frames, Thrashing, cache memory organization.

UNIT-V I/O Management & Disk Scheduling: I/O system Interrupts Direct Memory Access, I/O Buffering, File system: File Concepts – File organization and Access mechanism, File Directories, File sharing, Implementation issues. Disk Scheduling algorithms. Case Study on LINUX: Kernel and Buffer Cache Architecture, concept of inode file & directory structure, Basic system calls (Open, Read, Write, namei, File and Record Close, File Creation, Creation of Special Files, Change Directory and Change Root, Change Owner and Change Mode

Text Books:

1. Operating system concepts Galvin by Silberschatz, John Wiley & Sons
2. Operating System Design & Implementation by Tanenbaum, A.S., PHI.
3. The Design of Unix Operating System, Maurice J. Bach, Pearson Education.

Reference Books :

1. Modern Operating System: Andrew S. Tanenbaum, PEARSON EDUCATION INTERNATIONAL
2. Operating System concepts by Silberschatz A and Peterson, J.L, PE- LPE.
3. Operating systems: Internals & Design Principles, William Stallings, PHI.

Course Outcomes [After undergoing the course, students will be able to:]

1. Identify the role of operating system in making computers execute data-processing jobs.
2. Realize managing computer's resource complexity during concurrent process execution through OS layers.
3. Analyse the reasons of resource bottlenecks-concurrency, deadlock and various synchronization mechanisms available.
4. Understand the functioning of operating system components in Memory Management techniques, Virtual Memory Management.
5. Understand disk organization, file system structure, Secondary Storage Management functions of OS.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Data Structures (Laboratory)	Course Code: B022321(022)
Total / Minimum-Pass Marks (End Semester Exam): 40 / 20	L: 0 T: 0 P: 2 Credit(s): 1

List of Experiments: (At least 10 experiments are to be performed by each student)

1. Write a program to perform following operations in one dimensional array, Insertion, Deletion and Searching (Linear & Binary).
2. Write a program to implement stack and perform push and pop operations.
3. Write a program to convert infix to postfix expressions using stack.
4. Write a program to perform following operations on a linear queue - addition, deletion, traversing.
5. Write a program to perform following operations on a circular queue - addition, deletion, traversing.
6. Write a program to perform following operations on a double ended queue - addition, deletion, traversing.
7. Write a program to perform following operations on a single link list-creation, insertion, deletion.
8. Write a program to perform following operations on a double link list – creation, insertion, deletion.
9. Write a program to implement polynomial in link list and perform.
 - a) Polynomial arithmetic
 - b) Evaluation of polynomial
10. Write a program to implement a linked stack and linked queue.
11. Write programs to perform Insertion, selection and bubble sort.
12. Write a program to perform quick sort.
13. Write a program to perform merge sort.
14. Write a program to perform heap sort.
15. Write a program to create a Binary search tree and perform –insertion, deletion & traversal.
16. Write a program to traversal of graph (Breadth-first Search, Depth-first Search methods)

Remarks: The students are free to choose any programming platform from (C++ / JAVA / PYTHON) to perform the above-mentioned set of laboratory experiments.

Laboratory Outcomes [After undergoing the course, students will be able to:]

1. Understand the importance of abstract data types, structure types and their usability in different applications through different programming platforms.
2. Implement various data structure operations (traversal, accession, insertion, deletion & updation) on stacks, linked lists, queues, trees & graphs.
3. Design and analyse the time and space efficiency of implemented data structures
4. Identify the selection of appropriate data structure for given problem situations.
5. Implement various kinds of searching and sorting techniques.

Recommended Books:

1. Aaron M. Tenenbaum, YedidyahLangsam and Moshe J. Augenstein “Data Structures Using C and C/C++”, PHI
2. Jean Paul Trembley and Paul G. Sorenson, “An Introduction to Data Structures with applications”, McGraw Hill.
3. Lipschutz, “Data Structures” Schaum’s Outline Series, TMH

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Digital Electronics Laboratory	Course Code: B022322(022)
Total / Minimum-Pass Marks (End Semester Exam): 40 / 20	L: 0 T: 0 P: 2 Credit(s): 1

List of Experiments: (At least 10 experiments are to be performed by each student)

1. To study the characteristics and operations of TTL Inverters, OR, AND, NOR and NAND gate using ICs.
2. To study NAND and NOR gates as a universal logic.
3. To study and prove Demorgan's Theorem .
4. To design Half and Full adder circuits using logic gates.
5. To design Half and full subtractor circuits using logic gates.
6. To study the binary parallel adder.
7. To design 4 bit magnitude comparator circuits.
8. To study the 7 segment decoder .
9. To design 4:16 decoder using two 3:8 decoder and four 2:4 decoder
10. To design 16: 1 Multiplexer using 4:1 Multiplexer.
11. To study various types of flip flops using logic gates and ICs.
12. To design Mode-N and divide by K counter.
13. To construct a 4 bit binary to gray converter and vice versa using IC 7486 .
14. To study Up-Down counter.
15. To study programmable shift registers.

Experiments using VHDL (At least 4 Experiments are to be performed by each student)

1. Design AND,OR,XOR gates.
2. Design Half Adder (Data Flow Style)
3. Design Half Adder (Behavioural Style)
4. Design Half Adder (Structural style Direct entity instantiation)
5. Design Half Adder (Structural style indirect entity instantiation(Component))
6. Design Half Adder (Mixed Style)
7. Design 4 bit comparator Using std_logic_vector inputs.
8. Design 4:1 Multiplexer using Boolean expression
9. Design the 7 segment decoder .
10. Design 3:8 decoder

Laboratory Equipment / Machine Requirements: Logic gate trainer, Digital ICs Trainer, Various ICs 7400,7402,7404,7408,7432,7486,74138,74151,74155 etc, Xilinx ISE WebPACK

Laboratory Outcomes [After undergoing the course, students will be able to:]

1. Acknowledge about the fundamentals of digital circuit Design.
2. Understand the concepts of logic families.
3. Take interest to design and develop ICs in VLSI industries.
4. Understand the operations of latch circuits, flip flops, counters & semiconductor memories.
5. Understand and design combinational circuits.

Recommended Books:

1. M.M. Mano : "Digital Logic and Computer Design";
2. Kenneth L. SHORT "VHDL FOR ENGINEERS", Pearson Education.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Operating Systems (UNIX) Laboratory	Course Code: B022323(022)
Total / Minimum-Pass Marks (End Semester Exam): 40 / 20	L: 0 T: 0 P: 2 Credit(s): 1

List of Experiments: (At least 10 experiments are to be performed by each student)

1. Practice session: Study the features of Linux environment, basic Linux commands (echo, who, date, pwd, cd, mkdir, rmdir, ls, cp, mv, rm, cat, more, wc, find, tail, head, sort, nl, uniq, grep, egrep, fgrep, cut, paste, join, tee, comm, cmp, diff, tr); also document the syntax and semantics of those commands.
2. Write a shell script that accepts a name from the user and displays whether it is a file, directory or something else.
3. Write a shell script that creates users; also check if a particular user has logged in or not. If not, continue the loop till he/she logins. Once the required user logins, display a message.
4. Write a shell script that searches for a given string in a text input file.
5. Write a shell script that compiles all C files in your home directory and creates executable files.
6. Write a shell script that given a filename as argument, deletes all even lines in a file & removes duplicate lines from a file.
7. Write a shell script that enhances find command by adding error messages that explain why the command failed.
8. Write a shell script to input marks of five subjects Physics, Chemistry, Biology, Mathematics and Computer. Calculate percentage and grade according to following logic:

Percentage $\geq 90\%$: Grade A, Percentage $\geq 80\%$: Grade B, Percentage $\geq 70\%$: Grade C, Percentage $\geq 60\%$: Grade D, Percentage $\geq 40\%$: Grade E, Percentage $< 40\%$: Grade F.

9. Write a shell script to accept the name, grade, and basic salary from the user. Write the details into a file called employee, separating the fields with a colon (:) continue the process till the user wants.
10. Write an Awk' script to count the number of lines in a file that do not contain vowels.
11. Write an Awk' script to find the number of characters, words and lines in a file.
12. Write a C program to simulate following non-preemptive CPU scheduling algorithms: a) FCFS b) SJF c) Round Robin (pre-emptive) d) Priority scheduling techniques.
 - a. to find average turnaround times and waiting times;
 - b. to display / print Gantt Chart (in any convenient format).
13. Implement the Producer – Consumer problem using semaphores (using UNIX system calls).
14. Write a C program to simulate disk-scheduling algorithms: a) FCFS b) SCAN c) C-SCAN techniques.
15. Write a C program to simulate page replacement algorithms: a) FIFO b) LRU c) LFU d) OPT techniques.

Remarks: The laboratory experiments may be performed in with of the LINUX shell environments: BOURNE Shell / KORN Shell / 'C' Shell.

Laboratory Outcomes [After undergoing the course, students will be able to:]

1. Understand the concept of Unix and shell programming.
2. Learn the working of Linux OS Kernel.
3. Analyse the differences between features provided in Windows and Linux operating system.
4. Learn the concept of loops and decision-making statements.
5. Analyse the logic & procedure of problem solving through Scripts.

Recommended Books:

1. Advance UNIX, a Programmer's Guide, S. Prata, BPB Publications, New Delhi.
2. The Complete Reference Unix, Rosen, Host, Klee, Farber, Rosinski, Second Edition, TMH.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Software Laboratory (SciLAB / MATLAB)	Course Code: B022324(022)
Total / Minimum-Pass Marks (End Semester Exam): 40 / 20	L: 0 T: 0 P: 2 Credit(s): 1

List of Experiments: (At least 10 experiments are to be performed by each student)

1. Identification of different matrix types.
2. Properties and Operations of arrays and matrices.
3. Write a program to find probability of tossing a coin and rolling a die through large no. of experimentation.
4. Compute y- coordinates of a STRAIGHT LINE $y = mx + c$, where slope of line $m = 0.5$, intercept $c = -2$ and x-coordinates : $x = 0$ to 10 for 0.5 increments.
5. Plot $y = \sin x$ where $0 \leq x \leq 2$.
6. Plot $y = e^{-0.4x} \sin x$ where $0 \leq x \leq 4$.
7. Find the solution of linear algebraic equations in 2 variables, 3 variables:
 - a. $x + 4y = 18; 2x + 3y = 16$
 - b. $x + 2y + 3z = 1; 3x + 3y + 4z = 1; 2x + 3y + 3z = 2$
8. Determination of roots of a given polynomial & quadratic equations.
9. Determination of Eigen Value & Eigen Vectors for matrices.
10. Write a script file to draw a unit circle.
11. Write a function factorial to compute the factorial $n!$ for any integer n .
12. Write a function factorial to compute the factorial $n!$ using RECURSION for any integer n .
13. Write a function to compute the geometric series

$$1 + r + r^2 + r^3 + \dots + r^n$$
 for given r and n .
14. Write a function file *crossprod* to compute the cross product of two vectors u and v .
15. Design of a toy project as an independent study towards problem-based learning.

Laboratory Equipment: The experiments may be performed in FOSS (Spoken Tutorials SciLAB Project: www.scilab.org, www.scilab.in).

Laboratory Outcomes [After undergoing the course, students will be able to:]

1. Understand the main features of the MATLAB/SCILAB program development environment to enable their usage in the higher learning.
2. Realize the power of interactive calculation, programming, graphics, animation in SciLAB / MATLAB and complete portability across platforms.
3. Enjoy SciLAB / MATLAB as a scientific computing and visualization tool.
4. Explore Interactive Computation with matrices and arrays of n-dimensions.
5. Interpret and visualize simple mathematical functions and operations there on using plots/display.

Recommended Books:

1. Getting started with MATLAB: A Quick Introduction for Scientists and Engineers by Rudra Pratap, IIS Banaglore.
2. Scilab Manual for Probability Theory and Statistics Lab by Prof S N Chandra Shekhar; https://scilab.in/lab_migration_run/82
3. Scilab Manual for Numerical techniques lab by Prof Kanika Gupta; https://scilab.in/lab_migration_run/82
4. Scilab Manual for Probability Theory and Random Processes by Prof Shital Thakkar; https://scilab.in/lab_migration_run/82
5. Scilab Manual for Numerical Techniques by Dr Javed Dhillon; https://scilab.in/lab_migration_run/82

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

Program / Semester: B.Tech (III)	Branch: Computer Science &Engineering
Subject: Soft Skills & Personality Development	Course Code: B000306(046)
Total Marks (Internal Assessment): 10	L: 0 T:0 P: 2 Credit(s): 0
Internal Assessments to be conducted: 02	Duration (End Semester Exam): NA

UNIT-1 Communication Skills-Basics: Understanding the communicative environment, Listening: What to listen for and why, When to speak and how, Starting and sustaining a conversation, Presentation and Interaction, Common errors during communication, Humour in Communication.

UNIT-2 Interpersonal communication: Building Relationships, Understanding Group Dynamics- I, Emotional and Social Skills, Groups, Conflicts and their Resolution, Social Network, Media and Extending Our Identities

UNIT- 3 Vocational skills: Managing time: Planning and Goalsetting, managing stress: Types of Stress; Making best out of Stress, Resilience, Work-life balance, Applying soft-skills to workplace

UNIT-4 Mindsets and Handling People: Definitions and types of Mindset, Learning Mindset, Developing Growth Mindset, Types of People, How to say NO

UNIT-5 Inner Development: Motivating oneself, Persuasion, Survival Strategies, Negotiation, Leadership and motivating others, controlling anger, Gaining Power from Positive Thinking.

Text Books:

1. Petes S. J., Francis. Soft Skills and Professional Communication. New Delhi: Tata McGraw-Hill Education, 2011.
2. Stein, Steven J. & Howard E. Book. The EQ Edge: Emotional Intelligence and Your Success. Canada: Wiley & Sons, 2006.
3. Dorch, Patricia. What Are Soft Skills? New York: Execu Dress Publisher, 2013.

Reference Books:

- Kamin, Maxine. Soft Skills Revolution: A Guide for Connecting with Compassion for Trainers, Teams, and Leaders. Washington, DC: Pfeiffer & Company, 2013.
- Canfield, Jack. The Success Principles (TM) — 10th Anniversary Edition: How to get from Where You Are to Where You want to Be. New York Times. 2009.
- Peale Norman Vincent. The Power of Positive Thinking: 10 Traits for Maximum Result. Paperback Publication. 2011.
- Klaus, Peggy, Jane Rohman & Molly Hamaker. The Hard Truth about Soft Skills. London: Harper Collins E-books, 2007.

Course Outcomes [After undergoing the course, students will be able to:]

1. Learn to listen actively to analyse audience and tailor the delivery accordingly.
2. Increase their awareness of communication behaviour by using propriety profiling tool.
3. Master three “As” of stressful situation: Avoid, Alter, Accept; to cope with stressors and create a plan to reduce or eliminate them.
4. Develop growth mindset and able to handle difficult person and situations successfully.
5. Develop technique of turning negativity into positivity and generate self-motivation skills.

Printed Pages- 4

Roll No.

B022314(022)

**B. Tech. (Third Semester) Examination,
Nov.-Dec. 2020**

(Computer Science and Engg. Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt all questions. Each question carries equal marks. Part (a) is compulsory and answer any two parts from (b), (c) and (d).

1. (a) Fill in the blanks : 4
- (84-2-1) code for decimal digit 3 is
 - 2's complement of 101100 is
 - Binary of gray code 00110110 is
 - Excess 3 code of decimal number 9 is

- (b) Solve the following using K-map : 8

[2]

- (i) $F_1(A, B, C, D) = \Sigma m(1, 5, 6, 12, 13, 14) + \Sigma d(24)$
- (ii) $F_2(A, B, C, D) = \Pi m(0, 1, 2, 4, 6, 8, 9, 11, 12)$
- (c) Simplify the following using Tabulation method : 8

$$F(A, B, C, D) = \Sigma m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

(d) The message below coded in the 7-bit hamming code is transmitted through channel. Decode the message assuming that single error occurred in each code word.

- (i) 1001001
(ii) 0111001
(iii) 1110110
(iv) 0011011

Find the correct code in each case. 8

2. (a) Compare RTL, DTL, TTL and ECL on the basis of : 4
- (i) Component used
(ii) Fan out
(iii) Propagation delay and
(iv) Application

[3]

- (b) With the help of neat diagram, explain the working of:
(i) CMOS inverter and
(ii) CMOS NOR gate 8
- (c) Explain the working of TTL circuit with Totem pole output configuration. 8
- (d) Implement the following Boolean function using:

- (i) PLA
(ii) PLA

$$F_1(A, B, C) = \Sigma m(3, 4, 5, 6, 7)$$

$$F_2(A, B, C) = \Sigma m(2, 5, 6, 7)$$

3. (a) Fill in the blanks : 4

- (i) consists of logic gates where output at any instant is determined by present combination of input as well as previous state of output.
(ii) is an example of combinational circuit.
(iii) Logical expression of carry out in half adder is

[4]

- (iv) Minimum number of NAND gates required for designing Half Adder is
- (b) Design 4-bit look ahead carry adder with suitable diagram. 8
- (c) Design full adder using 4 : 1 MUX. 8
- (d) Design and implement comparator. 8
4. (a) Convert SR flip-flop to T flip-flop. 4
- (b) What is race around condition for J-K flip-flop?
How it can be avoided in master slave flip-flop? 8
- (c) Design and implement 4 bit synchronous up counter. 8
- (d) Design Serial in Serial Out (SISO) and parallel in Serial Out (PISO) shift register using D flip-flop. 8
5. (a) Discuss the various operators used in VHDL. 4
- (b) Write short notes on Mealy and Moore machine. 8
- (c) Write a program in VHDL using data flow modelling for half adder. 8
- (d) Write a program in VHDL using behavioural modelling for AND gate. 8

B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2024

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d). Part (a) is of 4 marks each. Part (b), (c) and (d) are of 8 marks each.

Unit-I

1. (a) Convert :

- (i) Decimal number $(25)_{10}$ to Binary number

[2]

- (ii) Gray code (100111) into Binary number
- (b) Simplify the following Boolean function,
 $f(W, X, Y, Z) = \sum m(2, 6, 8, 9, 10, 11, 14, 15)$ using
Quine-McCluskey tabular method.
- (c) Minimise the following function using K-map :
- (i) $F(A, B, C, D) = M(6, 7, 8, 9) + d(12, 13, 14, 15)$
in POS minimal form
- (ii) $F(A, B, C, D) = m(1, 2, 6, 7, 8, 13, 14, 15) + d(0, 3, 5, 12)$
in SOP minimal form.
- (d) Describe briefly error correcting code. If a seven bit Hamming code is received as 1111101. Find the correct code.

Unit-II

2. (a) Define Noise Margin, Fan-in, Fan-out & Power Dissipation.
- (b) Describe Transistor Transistor Logic (TTL) in Totem Pole output arrangement.
- (c) Explain the operation of CMOS NOR Gate with suitable diagram.

[3]

- (d) Explain ECL logic family with reasons why it is the fastest among the logic family.

Unit-III

3. ✓(a) Design Half Adder using NAND gates.
(b) Design & explain working of BCD adder.
(c) Design 32:1 multiplexer using two 16:1 multiplexer & one 2:1 multiplexer.
(d) Design 4-bit comparator circuit.

Unit-IV

4. (a) Define edge triggering & level triggering.
(b) Describe in brief various types of shift registers.
(c) What is Race-around Condition? Explain the operation of master slave JK flip-flop.
(d) Design 4-bit binary Ripple Counter (Up/Down).

Unit-V

5. (a) Describe four VHDL operators.
(b) For Half Subtractor write a program in VHDL using Data Flow.

[4]

- (c) Describe Moore Machine & Meelay Machine with block diagram.
- (d) Write a program in VHDL for OR gate.

B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2023

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory from each unit and carry equal 4 marks. attempt any two parts from (b), (c) and (d) from each question and carry equal 8 marks.

Unit-I

1. (a) Convert 10101001 in Gray code.

(b) State & Prove Demorgan's law.

| 2 |

- (c) Describe NAND and NOR gate as universal gate.
- (d) For 7 bit hamming code received code is 1111101
find error. Use even parity.

Unit-II

2. (a) Define Fan in & Fan out.
- (b) Describe CMOS NAND gate.
- (c) Describe CMOS NOR gate.
- (d) Describe TTL open collector circuit.

Unit-III

3. (a) Define the term combinational circuit.
- (b) Describe full adder circuit with diagram & truth table.
- (c) Design 4×16 decoder using 3×8 decoder.
- (d) Implement the Boolean expression $F(A, B, C) = \sum m(0, 2, 5, 6)$ using $4 : 1$ multiplexer.

Unit-IV

4. (a) Define sequential circuits.

[3]

- (b) Describe S-R Flip-Flop with diagram
- (c) What is race around condition and also describe master slave Flip-Flop.
- (d) Describe how to convert D flip flop into T flip-flop.

Unit-V

- 5. (a) Define State diagram.
- (b) Describe Mealy State Machine.
- (c) Describe Moore State Machine.
- (d) Describe Basic Components of ASM charts.

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Roll No. :

B022314(022)

B. Tech. (Third Semester) Examination,

April-May 2021 2022 .

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Passing Marks - 35

Note : Part (a) is compulsory and attempt any two parts from (b), (c) and (d).

Unit-I

1. (a) Explain laws of Boolean Algebra.

4

[2]

- (b) Minimize the following expression using k-map and realize using logic gates. 8

(i) $F_1(w, x, y, z) =$

$$\sum m(0, 3, 4, 8, 10, 12, 15) + d(1, 13)$$

(ii) $F_2(A, B, C, D) = \pi m(2, 4, 5, 6, 8, 9, 12, 13, 15)$

- (c) The Hamming code 101101101 is received. Correct it if any errors. Odd parity is used. 8

- (d) Minimize the following digital function using Mc_Cluskey method. 8

$F(P, Q, R, S)$

$$= \sum (0, 1, 5, 8, 9, 10, 11, 13)$$

$$+ \sum d(4, 12, 14)$$

Unit-II

2. (a) Write short notes on : 4

(i) Noise margin

(ii) Propagation Delay

[3]

- (b) Compare the performance TTL, CMOS and ECL logic. 8

- (c) Implement following function using PLA. 8

$$F_1(A, B, C) = \sum m(4, 5, 7)$$

$$F_2(A, B, C) = \sum m(4, 5, 7)$$

- (d) Implement following function using suitable PAL. 8

$$W(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$$

$$X(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 15)$$

$$Y(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 12)$$

$$Z(A, B, C, D) = \sum m(2, 3, 8, 9, 12, 13)$$

Unit-III

3. (a) What is Multiplexer? Explain with example. 4

- (b) Design BCD adder to add to BCD number. 8

- (c) Give a block diagram of 4×16 Decoder using 3×8 decoders and explain its working. 8

- (d) Design full adder using multiplexer. 8

Unit-IV

4. (a) What is flip flop? 4

[4]

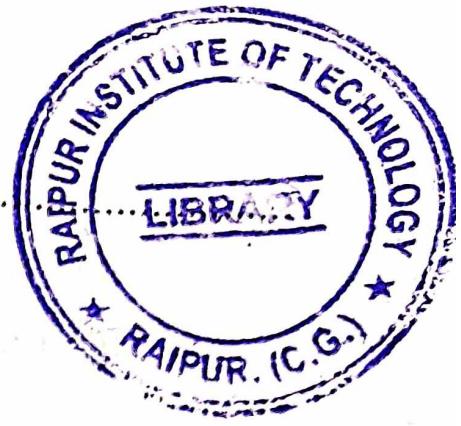
- (b) What is Shift Register? Explain application of Shift Register. 8
- (c) Design mod 5 synchronous counter. 8
- (d) Design UP/DOWN ripple counter. 8

Unit-V

5. (a) Write difference between Moore and Mealy Machine. 4
- (b) Explain lexical element and data object types in VHDL. 8
- (c) Write syntax for :
 (i) entity and
 (ii) architecture in VHDL 8
- (d) Explain Mealy machine with example. 8

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Roll No. :



B022314(022)

**B. Tech. (Third Semester) Examination,
April-May 2024**

(New Scheme)

(CSE Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

***Note : Attempt all questions of part (a) compulsory
(each of 4 marks). Attempt any two from part
(b), (c) and (d) (Each of 8 Marks)***

Unit-I

1. (a) Solve the following :

- (i) Convert the binary number $(11001010)_2$ into gray code.

[2]

- (ii) Convert (1010000) gray code to decimal code.
(iii) Find the value of base X

$$(193)_v = (623)_s$$

- (iv) Convert $(3C9A)_{16}$ into decimal. 4

- (b) A message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word : 1110110 8
(c) Simplify the following using Tabulation method
 $F = \Sigma m(0, 2, 3, 5, 8, 10, 11, 13)$ 8
(d) Simplify the logic expression using K-map
 $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and also design logic circuit using gates. 8

Unit-II

2. (a) What do you understand by PLA, PAL, and FPGA? 4
(b) What is ECL logic? With the help of a neat circuit diagram, explain the working of a two input ECL OR/NOR gate. 8

[3]

- (c) With the help of diagram, explain CMOS NAND and NOR gate. 8
(d) Explain the comparison of DTL, RTL, TTL and ECL logic families. 8

Unit-III

3. (a) Design half adder using basic gates with truth table. 4
(b) Implement $F = \Sigma m(0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$
Design MUX using (i) 4 : 1 & (ii) 8 : 1 8
(c) Draw and explain look ahead Carry adder. 8
(d) Design a 4 bit (Digit) BCD adder circuit. 8

Unit-IV

4. (a) Draw the logic diagram of ring counter and explain it. 4
(b) Design JK flip flop using SR flip flop. 8
(c) Write short notes on
(1) SISO
(2) SIPO

[4]

- (3) PIFO
(4) PISO
(d) Design synchronous 3-bit up-down counter using JK flip-flop. 8

Unit-V

5. (a) Discuss lexical elements and data objects types. 4
(b) Write a program in VHDL using structural modelling for 4×1 multiplexer. 8
(c) Write difference between Mealy and Moore Machine. 8
(d) Write a program in VHDL using behavioral and data flow for OR gate. 8

**B022314(022)****B. Tech. (Third Semester) Examination,****April-May 2023****(AICTE Scheme)****(CSE Engg. Branch)****DIGITAL ELECTRONICS & LOGIC DESIGN*****Time Allowed : Three hours******Maximum Marks : 100******Minimum Pass Marks : 35***

Note : Part (a) is compulsory from each unit and carry equal 4 marks. attempt any two parts from (b), (c) and (d) from each question and carry equal 8 marks.

Unit-I

1. (a) Convert the Boolean Expression $\overline{((A+B)C)} D$ using NAND gates only.

| 2 |

- (b) Reduce the following function using Karnaugh map and implement using basic gates

$$f(A, B, C, D) = \overline{AB}D + AB\overline{C}\overline{D} + \overline{A}BD + ABC\overline{D}$$

- (c) Reduce the following equation using Quine Meclusky method of minimisation

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$$

- (d) Do as directed :

- (i) Convert $(2AC5\cdot D)_H$ to decimal, octal and binary
- (ii) Solve $(DDCC)_{16} + (BBA4)_{16} = (\dots\dots\dots)_{16}$.

Unit-II

2. (a) Define the following parameter.

- (i) Noise margin
- (ii) Power dissipation
- (iii) Propogation delay
- (iv) Fan out

- (b) Draw the circuit diagram and explain the operation of 2-input TTL NAND gate with open collector output.

| 3 |

- (c) Explain with neat diagram interfacing of a TTL gate driving CMOS gate and Vice versa

- (d) Write short note on :

(i) PLA

4

(ii) PAL and FPGA

4

Unit-III

3. (a) Explain design procedure for combinational circuit.
(b) Draw and explain the block diagram of n -bit parallel adder circuit.
(c) Design 32 to 1 multiplexer using two 74LS150 ICs
(d) Draw and explain circuit for 3 to 8 decoder

Unit-IV

4. (a) What is race around condition? How it is avoided.
(b) Explain the working of 4 bit asynchronous counter.
(c) What are registers. Differentiate between Buffer Register & shift register

- (d) Design the counter that goes through state 1, 2, 4, 5, 7, 10, 11, 1 using J-K flip flops.

Unit-V

5. (a) Define finite state machine.
(b) Differentiate between Mealy machine and Moore machine.
(c) What is VHDL. Give data flow and algorithmic and structural description.
(d) Write VHDL code to design 4 to 1 MUX.

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B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2021

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory and attempt any two parts from (b), (c) and (d).

Unit-I

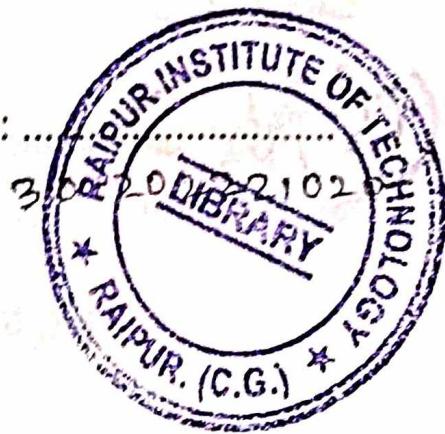
1. (a) Convert 10101001 in Gray code.

4

<p>[2]</p> <p>(b) State and prove Demorgan's law. 8</p> <p>(c) Describe NAND and NOR gate as universal gate. 8</p> <p>(d) For 7 bit hamming code received code is 1111101 find error use even parity. 8</p>	<p>[3]</p> <p>Unit-IV</p> <p>4. (a) Define sequential circuits. 4</p> <p>(b) Describe S-R flip-flop with diagram. 8</p> <p>(c) What is race around condition and also describe master slave flip-flop? 8</p> <p>(d) Describe how to convert D flip flop into T flip-flop. 8</p>
<p>Unit-II</p> <p>2. (a) Define Fan in and Fan out. 4</p> <p>(b) Describe CMOS NAND gate. 8</p> <p>(c) Describe CMOS NOR gate. 8</p> <p>(d) Describe TTL open collector circuit. 8</p>	<p>Unit-V</p> <p>5. (a) Define state diagram. 4</p> <p>(b) Describe Mealy State Machine. 8</p> <p>(c) Describe Moore State Machine. 8</p> <p>(d) Describe basic components of ASM charts. 8</p>
<p>Unit-III</p> <p>3. (a) Define the term Combinational Circuit. 4</p> <p>(b) Describe full adder circuit with diagram and truth table. 8</p> <p>(c) Design 4×16 decoder using 3×8 decoder. 8</p> <p>(d) Implement the Boolean expression</p> $F(A, B, C) = \Sigma m(0, 2, 5, 6)$ <p>using 4 : 1 multiplexer. 8</p>	

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Roll No. :



B022314(022)

**B. Tech. (Third Semester) Examination,
Nov.-Dec. 2022**

(AICTE Scheme)

(CSE Engg. Branch) *T.T.*

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory from each unit and attempt any two parts from (b), (c) and (d) from each question.

Unit-I

1. (a) Discuss weighted code with example.

4

| 2 |

- (b) Simplify the following boolean function using Quine McCluskey method :

8

$$F(A, B, C, D) = \sum_m(0, 1, 3, 7, 8, 9, 11, 15)$$

| 3 |

- (d) Design a BCD to 7-segment decoder with truth table and K-maps.

8

Unit-IV

- (c) What do you understand by error correcting code?

Construct (7, 4) hamming code for the message (1000).

8

- (d) Explain about Demorgan's theorem.

8

4. (a) Define universal shift register.

4

- (b) Explain about SISO shift register with example.

8

- (c) Explain JK flip-flop with truth table excitation table.

8

- (d) Explain ring counter with state table and wave forms.

8

Unit-II

2. (a) Explain propagation delay time with example.

4

- (b) Explain ECL with circuit diagram.

8

- (c) Explain the difference between TTL and CMOS.

8

- (d) Explain difference between ROM and RAM.

8

Unit-V

5. (a) What is HDL? What are various uses of VHDL?

4

- (b) What are the application of finite state machine model? Compare Mealy machine with Moore m/c with block diagram.

8

- (c) Explain structure of VHDL code.

8

- (d) Explain VHDL Data types.

8

Unit-III

3. (a) Describe Half Adder with its truth table.

4

- (b) Draw the circuit-diagram of universal gates using n -channel MOS logic and explain their working.

8

- (c) Convert T flip-flop to D flip-flop and design the circuit.

8