

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

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|------------------------------------------------------------------------|--------------------------------------------------|
| Program / Semester: B.Tech (III) | Branch: Computer Science &Engineering |
| Subject: Digital Electronics | Course Code: B022314(022) |
| Total / Minimum-Pass Marks (End Semester Exam): 100 / 35 | L: 3 T: 1 P: 0 Credits: 4 |
| Class Tests & Assignments to be conducted: 2 each | Duration (End Semester Exam): 03 Hours |

UNIT- I Digital Fundamentals: Weighted & Non-weighted codes, Sequential codes, self-complementing codes, Cyclic codes, 8-4-2-1 BCD code, Excess-3 code, Gray code: Binary to Gray and Gray to binary code conversion, Error detecting code, Error correcting code, 7-bit Hamming code, ASCII code, Binary Arithmetic, Boolean Algebra, Minimization of Switching Function , Demorgan's Theorem, Karnaugh's Map Method, Quine-McCluskey's Method (Tabular Method). Basic and Universal logic Gates, Realization of switching functions using gates.

UNIT-II Digital Logic Families and Memory: Transistor Inverter: Basic Concepts of RTL and DTL; TTL: Open collector gates, TTL subfamilies, IIL, ECL; MOS Logic: CMOS Logic, Dynamic MOS Logic, Interfacing: TTL to ECL, ECL to TTL, TTL to CMOS, CMOS to TTL, and Comparison among various logic families. Memories: ROM and RAM, PLA, PAL and FPGA;

UNIT- III Combinational Circuits: Adder & Subtractor: Half adder, Full adder, Half-subtractor, Full-subtractor, Parallel Binary adder, Look Ahead carry adder, Serial adder, BCD adder. Code converter, Parity bit generator/Checker, Comparator. Decoder: 3-line to 8-line decoder, 8-4-2-1 BCD to Decimal decoder, BCD to Seven segment decoder. Encoder: Octal to binary and Decimal to BCD encoder. Multiplexer: 2-input multiplexer, 4-input multiplexer. De- multiplexer: 1-line to 4-line, study of Multiplexer as Universal Logic Function Generator.

UNIT-IV Sequential Circuits: Flip-Flops: SR, JK, T, D, Master/Slave JK FF and their conversion, Excitation Tables. Introduction to registers (SISO, SIPO, PIPO, PISO) and Design of Counters- Ripple Counters, Ring Counters, Shift registers, Universal Shift Register.

UNIT-V Machines and Application: Finite State Machine, Mealy Machine, Moore Machine, **Introduction to VHDL:** Behavioral – data flow and algorithmic and structural description, lexical elements, data objects types, attributes, operators; VHDL coding examples.

Text Books:

1. R. P. Jain: "Modern Digital electronics", TMH.
2. B. Somanathan Nair, "Digital Electronics & Logic Design", Prentice-Hall of India.
3. Pedroni V.A., "Digital Circuit Design with VHDL", Prentice Hall, India 2nd Edition.

Reference Books:

1. R J Tocci, "Digital System principles and Applications"
2. "Digital Electronics " by A.K.Maini, Wiley India.
3. M.M. Mano: "Digital logic and computer design", PHI.
4. Floyd: "Digital fundamentals", UBS.

Course Outcomes [After undergoing the course, students will be able to:]

1. Apply digital coding concepts to simplify circuit design.

2. Analyze the operations of various logic families and different semiconductor memories.
3. Design and implement various combinational circuits
4. Outline the concepts of latch circuits, flip flops and counters.
5. Design and develop basic digital systems using VHDL.

Chhattisgarh Swami Vivekananda Technical University, Bhilai (C.G.)

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|------------------------------------------------|--------------------------------------------------|
| Program / Semester: B.Tech (III) | Branch: Computer Science &Engineering |
| Subject: Soft Skills & Personality Development | Course Code: B000306(046) |
| Total Marks (Internal Assessment): 10 | L: 0 T:0 P: 2 Credit(s): 0 |
| Internal Assessments to be conducted: 02 | Duration (End Semester Exam): NA |

UNIT-1 Communication Skills-Basics: Understanding the communicative environment, Listening: What to listen for and why, When to speak and how, Starting and sustaining a conversation, Presentation and Interaction, Common errors during communication, Humour in Communication.

UNIT-2 Interpersonal communication: Building Relationships, Understanding Group Dynamics- I, Emotional and Social Skills, Groups, Conflicts and their Resolution, Social Network, Media and Extending Our Identities

UNIT- 3 Vocational skills: Managing time: Planning and Goalsetting, managing stress: Types of Stress; Making best out of Stress, Resilience, Work-life balance, Applying soft-skills to workplace

UNIT-4 Mindsets and Handling People: Definitions and types of Mindset, Learning Mindset, Developing Growth Mindset, Types of People, How to say NO

UNIT-5 Inner Development: Motivating oneself, Persuasion, Survival Strategies, Negotiation, Leadership and motivating others, controlling anger, Gaining Power from Positive Thinking.

Text Books:

1. Petes S. J., Francis. Soft Skills and Professional Communication. New Delhi: Tata McGraw-Hill Education, 2011.
2. Stein, Steven J. & Howard E. Book. The EQ Edge: Emotional Intelligence and Your Success. Canada: Wiley & Sons, 2006.
3. Dorch, Patricia. What Are Soft Skills? New York: Execu Dress Publisher, 2013.

Reference Books:

- Kamin, Maxine. Soft Skills Revolution: A Guide for Connecting with Compassion for Trainers, Teams, and Leaders. Washington, DC: Pfeiffer & Company, 2013.
- Canfield, Jack. The Success Principles (TM) — 10th Anniversary Edition: How to get from Where You Are to Where You want to Be. New York Times. 2009.
- Peale Norman Vincent. The Power of Positive Thinking: 10 Traits for Maximum Result. Paperback Publication. 2011.
- Klaus, Peggy, Jane Rohman & Molly Hamaker. The Hard Truth about Soft Skills. London: Harper Collins E-books, 2007.

Course Outcomes [After undergoing the course, students will be able to:]

1. Learn to listen actively to analyse audience and tailor the delivery accordingly.
2. Increase their awareness of communication behaviour by using propriety profiling tool.
3. Master three “As” of stressful situation: Avoid, Alter, Accept; to cope with stressors and create a plan to reduce or eliminate them.
4. Develop growth mindset and able to handle difficult person and situations successfully.
5. Develop technique of turning negativity into positivity and generate self-motivation skills.

Printed Pages- 4

Roll No.

B022314(022)

**B. Tech. (Third Semester) Examination,
Nov.-Dec. 2020**

(Computer Science and Engg. Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt all questions. Each question carries equal marks. Part (a) is compulsory and answer any two parts from (b), (c) and (d).

1. (a) Fill in the blanks : 4
- (84-2-1) code for decimal digit 3 is
 - 2's complement of 101100 is
 - Binary of gray code 00110110 is
 - Excess 3 code of decimal number 9 is

- (b) Solve the following using K-map : 8

[2]

- (i) $F_1(A, B, C, D) = \Sigma m(1, 5, 6, 12, 13, 14) + \Sigma d(24)$
- (ii) $F_2(A, B, C, D) = \Pi m(0, 1, 2, 4, 6, 8, 9, 11, 12)$
- (c) Simplify the following using Tabulation method : 8

$$F(A, B, C, D) = \Sigma m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$$

- (d) The message below coded in the 7-bit hamming code is transmitted through channel. Decode the message assuming that single error occurred in each code word.

- (i) 1001001
(ii) 0111001
(iii) 1110110
(iv) 0011011

Find the correct code in each case. 8

2. (a) Compare RTL, DTL, TTL and ECL on the basis of : 4
- (i) Component used
(ii) Fan out
(iii) Propagation delay and
(iv) Application

[3]

- (b) With the help of neat diagram, explain the working of:
(i) CMOS inverter and
(ii) CMOS NOR gate 8
- (c) Explain the working of TTL circuit with Totem pole output configuration. 8
- (d) Implement the following Boolean function using:

- (i) PLA
(ii) PLA

$$F_1(A, B, C) = \Sigma m(3, 4, 5, 6, 7)$$

$$F_2(A, B, C) = \Sigma m(2, 5, 6, 7)$$

3. (a) Fill in the blanks : 4

- (i) consists of logic gates where output at any instant is determined by present combination of input as well as previous state of output.
(ii) is an example of combinational circuit.
(iii) Logical expression of carry out in half adder is

[4]

- (iv) Minimum number of NAND gates required for designing Half Adder is
- (b) Design 4-bit look ahead carry adder with suitable diagram. 8
- (c) Design full adder using 4 : 1 MUX. 8
- (d) Design and implement comparator. 8
4. (a) Convert SR flip-flop to T flip-flop. 4
- (b) What is race around condition for J-K flip-flop?
How it can be avoided in master slave flip-flop? 8
- (c) Design and implement 4 bit synchronous up counter. 8
- (d) Design Serial in Serial Out (SISO) and parallel in Serial Out (PISO) shift register using D flip-flop. 8
5. (a) Discuss the various operators used in VHDL. 4
- (b) Write short notes on Mealy and Moore machine. 8
- (c) Write a program in VHDL using data flow modelling for half adder. 8
- (d) Write a program in VHDL using behavioural modelling for AND gate. 8

B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2024

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d). Part (a) is of 4 marks each. Part (b), (c) and (d) are of 8 marks each.

Unit-I

1. (a) Convert :

- (i) Decimal number $(25)_{10}$ to Binary number

[2]

- (ii) Gray code (100111) into Binary number
- (b) Simplify the following Boolean function,
 $f(W, X, Y, Z) = \sum m(2, 6, 8, 9, 10, 11, 14, 15)$ using
Quine-McCluskey tabular method.
- (c) Minimise the following function using K-map :
- (i) $F(A, B, C, D) = M(6, 7, 8, 9) + d(12, 13, 14, 15)$
in POS minimal form
- (ii) $F(A, B, C, D) = m(1, 2, 6, 7, 8, 13, 14, 15) + d(0, 3, 5, 12)$
in SOP minimal form.
- (d) Describe briefly error correcting code. If a seven bit Hamming code is received as 1111101. Find the correct code.

Unit-II

2. (a) Define Noise Margin, Fan-in, Fan-out & Power Dissipation.
- (b) Describe Transistor Transistor Logic (TTL) in Totem Pole output arrangement.
- (c) Explain the operation of CMOS NOR Gate with suitable diagram.

[3]

- (d) Explain ECL logic family with reasons why it is the fastest among the logic family.

Unit-III

3. ✓(a) Design Half Adder using NAND gates.
(b) Design & explain working of BCD adder.
(c) Design 32:1 multiplexer using two 16:1 multiplexer & one 2:1 multiplexer.
(d) Design 4-bit comparator circuit.

Unit-IV

4. (a) Define edge triggering & level triggering.
(b) Describe in brief various types of shift registers.
(c) What is Race-around Condition? Explain the operation of master slave JK flip-flop.
(d) Design 4-bit binary Ripple Counter (Up/Down).

Unit-V

5. (a) Describe four VHDL operators,
(b) For Half Subtractor write a program in VHDL using Data Flow.

[4]

- (c) Describe Moore Machine & Meelay Machine with block diagram.
- (d) Write a program in VHDL for OR gate.

B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2023

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory from each unit and carry equal 4 marks. attempt any two parts from (b), (c) and (d) from each question and carry equal 8 marks.

Unit-I

1. (a) Convert 10101001 in Gray code.

(b) State & Prove Demorgan's law.

| 2 |

- (c) Describe NAND and NOR gate as universal gate.
- (d) For 7 bit hamming code received code is 1111101
find error. Use even parity.

Unit-II

2. (a) Define Fan in & Fan out.
- (b) Describe CMOS NAND gate.
- (c) Describe CMOS NOR gate.
- (d) Describe TTL open collector circuit.

Unit-III

3. (a) Define the term combinational circuit.
- (b) Describe full adder circuit with diagram & truth table.
- (c) Design 4×16 decoder using 3×8 decoder.
- (d) Implement the Boolean expression $F(A, B, C) = \sum m(0, 2, 5, 6)$ using $4 : 1$ multiplexer.

Unit-IV

4. (a) Define sequential circuits.

[3]

- (b) Describe S-R Flip-Flop with diagram
- (c) What is race around condition and also describe master slave Flip-Flop.
- (d) Describe how to convert D flip flop into T flip-flop.

Unit-V

- 5. (a) Define State diagram.
- (b) Describe Mealy State Machine.
- (c) Describe Moore State Machine.
- (d) Describe Basic Components of ASM charts.

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Roll No. :

B022314(022)

B. Tech. (Third Semester) Examination,

April-May 2021 2022 .

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Passing Marks - 35

Note : Part (a) is compulsory and attempt any two parts from (b), (c) and (d).

Unit-I

1. (a) Explain laws of Boolean Algebra.

4

[2]

- (b) Minimize the following expression using k-map and realize using logic gates. 8

(i) $F_1(w, x, y, z) =$

$$\sum m(0, 3, 4, 8, 10, 12, 15) + d(1, 13)$$

(ii) $F_2(A, B, C, D) = \pi m(2, 4, 5, 6, 8, 9, 12, 13, 15)$

- (c) The Hamming code 101101101 is received. Correct it if any errors. Odd parity is used. 8

- (d) Minimize the following digital function using Mc_Cluskey method. 8

$F(P, Q, R, S)$

$$= \sum (0, 1, 5, 8, 9, 10, 11, 13)$$

$$+ \sum d(4, 12, 14)$$

Unit-II

2. (a) Write short notes on : 4

(i) Noise margin

(ii) Propagation Delay

[3]

- (b) Compare the performance TTL, CMOS and ECL logic. 8

- (c) Implement following function using PLA. 8

$$F_1(A, B, C) = \sum m(4, 5, 7)$$

$$F_2(A, B, C) = \sum m(4, 5, 7)$$

- (d) Implement following function using suitable PAL. 8

$$W(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14)$$

$$X(A, B, C, D) = \sum m(1, 3, 4, 6, 9, 11, 12, 14, 15)$$

$$Y(A, B, C, D) = \sum m(0, 2, 4, 6, 8, 12)$$

$$Z(A, B, C, D) = \sum m(2, 3, 8, 9, 12, 13)$$

Unit-III

3. (a) What is Multiplexer? Explain with example. 4

- (b) Design BCD adder to add to BCD number. 8

- (c) Give a block diagram of 4×16 Decoder using 3×8 decoders and explain its working. 8

- (d) Design full adder using multiplexer. 8

Unit-IV

4. (a) What is flip flop? 4

[4]

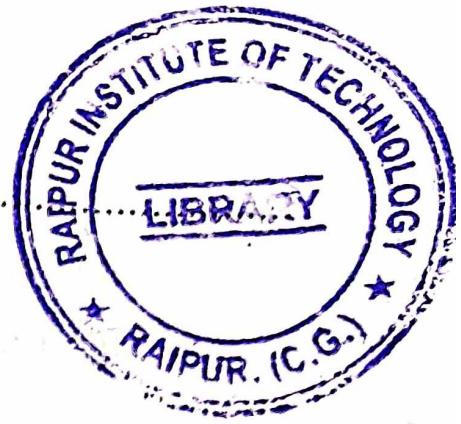
- (b) What is Shift Register? Explain application of Shift Register. 8
- (c) Design mod 5 synchronous counter. 8
- (d) Design UP/DOWN ripple counter. 8

Unit-V

5. (a) Write difference between Moore and Mealy Machine. 4
- (b) Explain lexical element and data object types in VHDL. 8
- (c) Write syntax for :
 (i) entity and
 (ii) architecture in VHDL 8
- (d) Explain Mealy machine with example. 8

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Roll No. :



B022314(022)

**B. Tech. (Third Semester) Examination,
April-May 2024**

(New Scheme)

(CSE Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

***Note : Attempt all questions of part (a) compulsory
(each of 4 marks). Attempt any two from part
(b), (c) and (d) (Each of 8 Marks)***

Unit-I

1. (a) Solve the following :

- (i) Convert the binary number $(11001010)_2$ into gray code.

[2]

- (ii) Convert (1010000) gray code to decimal code.
(iii) Find the value of base X

$$(193)_v = (623)_s$$

- (iv) Convert $(3C9A)_{16}$ into decimal. 4

- (b) A message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word : 1110110 8
(c) Simplify the following using Tabulation method
 $F = \Sigma m(0, 2, 3, 5, 8, 10, 11, 13)$ 8
(d) Simplify the logic expression using K-map
 $F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ and also design logic circuit using gates. 8

Unit-II

2. (a) What do you understand by PLA, PAL, and FPGA? 4
(b) What is ECL logic? With the help of a neat circuit diagram, explain the working of a two input ECL OR/NOR gate. 8

[3]

- (c) With the help of diagram, explain CMOS NAND and NOR gate. 8
(d) Explain the comparison of DTL, RTL, TTL and ECL logic families. 8

Unit-III

3. (a) Design half adder using basic gates with truth table. 4
(b) Implement $F = \Sigma m(0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$
Design MUX using (i) 4 : 1 & (ii) 8 : 1 8
(c) Draw and explain look ahead Carry adder. 8
(d) Design a 4 bit (Digit) BCD adder circuit. 8

Unit-IV

4. (a) Draw the logic diagram of ring counter and explain it. 4
(b) Design JK flip flop using SR flip flop. 8
(c) Write short notes on
(1) SISO
(2) SIPO

[4]

- (3) PIFO
(4) PISO
(d) Design synchronous 3-bit up-down counter using JK flip-flop. 8

Unit-V

5. (a) Discuss lexical elements and data objects types. 4
(b) Write a program in VHDL using structural modelling for 4×1 multiplexer. 8
(c) Write difference between Mealy and Moore Machine. 8
(d) Write a program in VHDL using behavioral and data flow for OR gate. 8

**B022314(022)**

**B. Tech. (Third Semester) Examination,
April-May 2023
(AICTE Scheme)**

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory from each unit and carry equal 4 marks. attempt any two parts from (b), (c) and (d) from each question and carry equal 8 marks.

Unit-I

1. (a) Convert the Boolean Expression $\overline{((A+B)C)} D$ using NAND gates only.

| 2 |

- (b) Reduce the following function using Karnaugh map and implement using basic gates

$$f(A, B, C, D) = \overline{AB}D + AB\overline{C}\overline{D} + \overline{A}BD + ABC\overline{D}$$

- (c) Reduce the following equation using Quine Meclusky method of minimisation

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 5, 7, 10, 13, 14, 15)$$

- (d) Do as directed :

- (i) Convert $(2AC5\cdot D)_H$ to decimal, octal and binary
- (ii) Solve $(DDCC)_{16} + (BBA4)_{16} = (\dots\dots\dots)_{16}$.

Unit-II

2. (a) Define the following parameter.

- (i) Noise margin
- (ii) Power dissipation
- (iii) Propogation delay
- (iv) Fan out

- (b) Draw the circuit diagram and explain the operation of 2-input TTL NAND gate with open collector output.

| 3 |

- (c) Explain with neat diagram interfacing of a TTL gate driving CMOS gate and Vice versa

- (d) Write short note on :

(i) PLA

4

(ii) PAL and FPGA

4

Unit-III

3. (a) Explain design procedure for combinational circuit.
(b) Draw and explain the block diagram of n -bit parallel adder circuit.
(c) Design 32 to 1 multiplexer using two 74LS150 ICs
(d) Draw and explain circuit for 3 to 8 decoder

Unit-IV

4. (a) What is race around condition? How it is avoided.
(b) Explain the working of 4 bit asynchronous counter.
(c) What are registers. Differentiate between Buffer Register & shift register

- (d) Design the counter that goes through state 1, 2, 4, 5, 7, 10, 11, 1 using J-K flip flops.

Unit-V

5. (a) Define finite state machine.
(b) Differentiate between Mealy machine and Moore machine.
(c) What is VHDL. Give data flow and algorithmic and structural description.
(d) Write VHDL code to design 4 to 1 MUX.

Printed Pages – 3

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B022314(022)

B. Tech. (Third Semester) Examination,

Nov.-Dec. 2021

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

Note : Part (a) is compulsory and attempt any two parts from (b), (c) and (d).

Unit-I

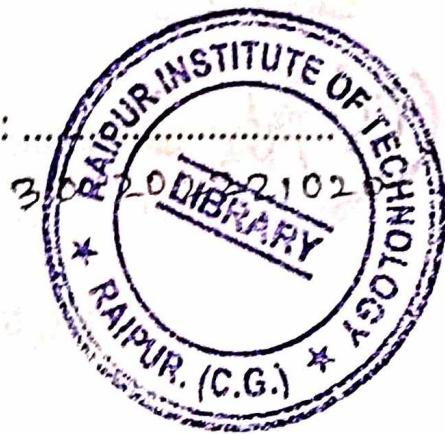
1. (a) Convert 10101001 in Gray code.

4

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|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>[2]</p> <p>(b) State and prove Demorgan's law. 8</p> <p>(c) Describe NAND and NOR gate as universal gate. 8</p> <p>(d) For 7 bit hamming code received code is 1111101 find error use even parity. 8</p> | <p>[3]</p> <p>Unit-IV</p> <p>4. (a) Define sequential circuits. 4</p> <p>(b) Describe S-R flip-flop with diagram. 8</p> <p>(c) What is race around condition and also describe master slave flip-flop? 8</p> <p>(d) Describe how to convert D flip flop into T flip-flop. 8</p> |
| <p>Unit-II</p> <p>2. (a) Define Fan in and Fan out. 4</p> <p>(b) Describe CMOS NAND gate. 8</p> <p>(c) Describe CMOS NOR gate. 8</p> <p>(d) Describe TTL open collector circuit. 8</p> | <p>Unit-V</p> <p>5. (a) Define state diagram. 4</p> <p>(b) Describe Mealy State Machine. 8</p> <p>(c) Describe Moore State Machine. 8</p> <p>(d) Describe basic components of ASM charts. 8</p> |
| <p>Unit-III</p> <p>3. (a) Define the term Combinational Circuit. 4</p> <p>(b) Describe full adder circuit with diagram and truth table. 8</p> <p>(c) Design 4×16 decoder using 3×8 decoder. 8</p> <p>(d) Implement the Boolean expression</p> $F(A, B, C) = \Sigma m(0, 2, 5, 6)$ <p>using 4 : 1 multiplexer. 8</p> | |

Printed Pages - 3

Roll No. :



B022314(022)

**B. Tech. (Third Semester) Examination,
Nov.-Dec. 2022**

(AICTE Scheme)

(CSE Engg. Branch)

DIGITAL ELECTRONICS & LOGIC DESIGN

Time Allowed : Three hours

Maximum Marks : 100

Minimum Pass Marks : 35

**Note : Part (a) is compulsory from each unit and
attempt any two parts from (b), (c) and (d)
from each question.**

Unit-I

- 1. (a) Discuss weighted code with example.**

4

| 2 |

- (b) Simplify the following boolean function using Quine McCluskey method :

8

$$F(A, B, C, D) = \sum_m(0, 1, 3, 7, 8, 9, 11, 15)$$

| 3 |

- (d) Design a BCD to 7-segment decoder with truth table and K-maps.

8

Unit-IV

- (c) What do you understand by error correcting code?

Construct (7, 4) hamming code for the message (1000).

8

- (d) Explain about Demorgan's theorem.

8

4. (a) Define universal shift register.

4

- (b) Explain about SISO shift register with example.

8

- (c) Explain JK flip-flop with truth table excitation table.

8

- (d) Explain ring counter with state table and wave forms.

8

Unit-II

2. (a) Explain propagation delay time with example.

4

- (b) Explain ECL with circuit diagram.

8

- (c) Explain the difference between TTL and CMOS.

8

- (d) Explain difference between ROM and RAM.

8

Unit-III

3. (a) Describe Half Adder with its truth table.

4

- (b) Draw the circuit-diagram of universal gates using n -channel MOS logic and explain their working.

8

- (c) Convert T flip-flop to D flip-flop and design the circuit.

8

Unit-V

5. (a) What is HDL? What are various uses of VHDL?

4

- (b) What are the application of finite state machine model? Compare Mealy machine with Moore m/c with block diagram.

8

- (c) Explain structure of VHDL code.

8

- (d) Explain VHDL Data types.

8