RAMAIAH
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Project Report on

LOW POWER 3-BIT FLASH ADC USING TIQ COMPARATOR

Submitted to

Ramaiah Institute of Technology, Bangalore
(Autonomous Institute Affiliated to VTU)
In partial fulfilment of the requirement for the award of degree of

BACHELOR OF ENGINEERING
IN
ELECTRONICS & TELECOMMUNICATION ENGINEERING

For the Academic Year 2023-2024

Submitted by

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May 2024

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CERTIFICATE

Certified the project work entitled "Low Power 3-bit Flash ADC using TIQ Comparator" carried out by Adhiraj Kar(USN 1MS20ET002), Eish Raj(USN 1MS20ET020), Souhardya Dey(USN 1MS20ET051), bonafide student of Ramaiah Institute of Technology, Bangalore, in partial fulfilment for the award of Bachelor of Engineering in Electronics & Telecommunication Engineering of the Visvesvaraya Technological University, Belgaum during the year 2023-2024. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the department library. The project report has been approved as it satisfies the academic requirements in respect of project work prescribed for the said degree.

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DECLARATION

I/We hereby declare that the project entitled "Low Power 3-bit Flash ADC using TIQ Comparator" has been carried out independently by me/us, under the guidance of Dr. H.R. Ramya Assistant Professor, Electronics & Telecommunication Engineering, Ramaiah Institute of Technology, Bangalore. This report has been submitted in partial fulfilment for the award of degree, Bachelor of Engineering in Electronics & Telecommunication Engineering of Ramaiah Institute of Technology (Autonomous Institute, affiliated to VTU, Belgaum) during the year 2023-2024.

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ACKNOWLEDGEMENTS

It is our profound gratitude that we express my indebtedness to all who have guided us to complete this project successfully.

We extended our sincere thanks to the management of MSRIT, for providing us with excellent infrastructure and facilities.

We are grateful to our HOD **Dr. B K Sujatha** for allowing us to undertake this Project work and also providing us with support and sharing her knowledge whenever needed.

We are thankful to our principal **Dr. N.V.R Naidu** for his guidance and support to complete our project.

We also extend our thanks to the project coordinators Dr. S G Shivaprasad Yadav and Dr. Parimala P for their continuous support in completing this project.

The valuable guidance, the exemplary support and timely suggestions made available to us by our guide **Dr. H.R. Ramya**, Assistant Professor, Electronics & Telecommunication dept., RIT went a long way in completion of the project. We sincerely acknowledge her help, guidance and constant support which were ever present throughout the project work.

We also thank my friends and the staff members of Electronics & Telecommunication dept. and also our family for the help and support provided by them in successful completion of the project.

We would also like to thank the other members of the lab, workplace, and our friends for being there for us during my hardships and creating an amiable atmosphere to work in.

Our accomplishments would be incomplete without my beloved parents, for without their support and encouragement we would not have reached up to this level. We owe my achievements to them.

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ABSTRACT

In designing a 3-bit Flash Analog to Digital Converter (ADC) employing Threshold Inverter Quantizer (TIQ) comparators, the choice of encoder significantly impacts power and timing efficiency. The Flash ADC necessitates 2N-1 comparators, requiring an encoder to convert thermometer code to binary code.

Among the three evaluated encoders – Wallace Tree, Rom Based, and MUX Based – each demonstrates distinct power consumption characteristics. In the simulation conducted using Tanner tool and TSpice, power consumption varies across the encoders: Wallace Tree consumes 6.32135x10^-5, Rom Based consumes 5.8564x10^-5, and MUX Based consumes 3.7978x10^-5.

Notably, the MUX Based encoder exhibits the lowest power consumption, potentially offering enhanced energy efficiency for the ADC design. While power efficiency is crucial, timing efficiency also plays a vital role in ADC performance.

The choice of encoder must consider not only power consumption but also timing constraints to ensure proper operation within desired specifications. Overall, the evaluation of encoders for the Flash ADC design underscores the importance of balancing power and timing efficiency to achieve optimal performance in analog-to-digital conversion applications.

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LIST OF ACRONYMS

1. ADC: Analog to Digital converter
2. TIQ: Threshold Inverter Quantization
3. ROM: Read only memory
4. VNC: Virtual Network Computing
5. VLSI: Very-large scale Integration
6. CMOS: Complementary Metal Oxide Semiconductor
7. MOSFET: Metal Oxide Semiconductor Field Effect Transistor
8. PMOS: p-channel Metal Oxide Semiconductor
9. NMOS: n-channel Metal Oxide Semiconductor
10. T-SPICE: T-simulation program with Integrated circuit emphasis

Project Outcome mapping

Course Outcomes:

CO1	Review the literature and identify a suitable problem by analyzing the requirements based on current trends and societal needs in the domain of interest and arrive at the specifications
CO2	Identify the clear objectives & methodology for implementing the project by visualizing the Hardware and Software
CO3	Design and Implementation of identified Problem using appropriate modern tools and Techniques in the area of telecommunication/ multidisciplinary areas
CO4	Validate the achieved results and demonstrate good project defense, presentation skills, leadership and punctuality as a team/individual
CO5	Ability to write the thesis following ethical values and publish the work in quality conferences/journals supporting lifelong learning abilities

Mapping of Course outcome to Program outcome

ETP : Project work															
CO	**Statement**	**Program Outcomes (POs)**												**PSOs**	
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
ETP.1	Review the literature and identify a suitable problem by analyzing the requirements based on current trends and societal needs in the domain of interest and arrive at the specifications	3	3		3		2	2		3			2	3	2	1
ETP.2	Identify the clear objectives & methodology for implementing the project by visualizing the Hardware and Software	3	3	3	3		2	2		3		3	2	3	2	2
ETP.3	Design and Implementation of identified Problem using appropriate modern tools and Techniques in the area of telecommunication/ multidisciplinary areas	3	3	3	3	3	2	2		3		3	2	3	2	2
ETP.4	Validate the achieved results and demonstrate good project defense, presentation skills, leadership and punctuality as a team/individual	3	3						3	3	3	3	1	2	-	3
ETP.5	Ability to write the thesis following ethical values and publish the work in quality conferences/journals supporting lifelong learning abilities								3	3	3		3	-	-	3
Course Articulation		3	3	3	3	3	2	2	3	3	3	3	2	2.75	2	2.2

Program Outcomes

PO1: Comprehensive knowledge of 3-Bit Flash ADC using TIQ comparator: Graduates will have a deep understanding of the principles, theories and technologies that underpin Flash ADC, including software design, modelling, control systems, data algorithms and hardware implementation.

PO2: Proficiency in developing Flash ADC using TIQ comparator Graduates will possess the necessary skills to design, develop, and implement Flash ADC including software and hardware components, to enable safe and efficient simulator operations.

PO3: Ability to analyse and solve complex problems: Graduates will be equipped with analytical and problem – solving skills necessary to identify and address challenges associated with Flash ADC such as control system design, hardware integration of sensors and actuators, modelling of the control system and telemetry data extraction algorithms.

PO4: Effective collaboration and teamwork: Graduates will have developed strong teamworkand collaboration skills through hands – on projects, enabling them to work efficiently in multidisciplinary teams consisting of engineers, researchers, and other professionals involvedin Flash ADC development.

PO5: Ethical and responsible Flash ADC development: Graduates will understand the ethical considerations and societal impacts of 3-bit Flash ADC, including issues related to safety, privacy, liability, and the potential effects on employment and automotive market.

PO6: Effective communication skills: Graduates will possess strong communication skills, both written and verbal, allowing them to effectively convey complex technical concepts and ideas related to 3-bit Flash ADC to diverse audiences.

PO7: Adaptable and lifelong learning: Graduates will have the ability to adapt to evolving technologies and industry trends, demonstrating a commitment to

continuous learning and staying up to date with advancements in Flash ADC technology and related fields.

PO8: Safety focused mindset: Graduates will prioritize safety in the design and implementation of 3-bit Flash ADC, understanding the importance of robust learning, validation, and fail-safe mechanisms to ensure the protection of both participants and the general public.

PO9: Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with theengineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological changes.

Justification:

1. **CO1 mapped to (POs 1, 2, 4, 6, 7, 9, 12) (PSO 1, 2, 3):** Understand the fundamentals of Flash ADC using TIQ comparator: Gain a comprehensive understanding of the basic principles, components and technologies involved in 3-Bit Flash ADC, including TIQ, Encoders etc.
2. **CO2 mapped to (POs 1, 2, 3, 4, 6, 7, 9, 11, 12) (PSO 1, 2, 3):** Familiarity with Flash ADC and TIQ Architecture: Learn about the different architectural designs and configurations used in 3-Bit Flah ADC, such as software design, Varying width of different PMOS and NMOS to achieve the required result, Used Tanner Lab for designing purposes of CMOS schematics, Tspice for compilation.
3. **CO3 mapped to (POs 1, 2, 3, 4, 5, 6, 7, 9, 11, 12) (PSO 1, 2, 3):** Knowledge of hardware design and development: The whole system can be fabricated inside the chip using silicon wafers. The process involved are floor planning, placement, clock tree synthesis, routing and physical verification.
4. **CO4 mapped to (POs 1, 2, 8, 9, 10, 11, 12) (PSO 1, 3):** Proficiency in control systems for Flash ADC: Learn about TIQ, encoders, Priority encoders and different types of priority encoders such as Wallace tree encoder, rom based encoder, and mux-based encoder to achieve low power efficiency and better timing closure.
5. **CO5 mapped to (POs 8, 9, 10, 12) (PSO 3):** Collaboration and teamwork skills: Foster the ability to work effectively in multidisciplinary teams, reflecting the collaborative nature of 3-bit Flash ADC whole system and encouraging communication, project management, and problem - solving skills.

1. INTRODUCTION

1.1 Need for Flash ADC

A Flash Analog-to-Digital Converter (ADC) is essential in applications requiring extremely high-speed data conversion. Flash ADCs, known for their fast conversion times, are capable of converting an analog signal to a digital output in a single clock cycle. This speed is achieved through a parallel processing architecture, where the input signal is simultaneously compared against multiple reference voltages by a bank of comparators. Each comparator corresponds to a specific output bit, and the resulting digital code represents the input signal's amplitude.
The primary need for flash ADCs arises in high-frequency and broadband applications such as digital oscilloscopes, radar systems, high-speed data acquisition, and communication systems, where rapid signal processing is crucial. These converters are indispensable in scenarios requiring real-time analysis and minimal latency, ensuring that high-speed signals are accurately captured and processed without delay.

Furthermore, flash ADCs are crucial in achieving high-resolution conversion at high sampling rates, making them suitable for modern digital signal processing tasks where precise and rapid data conversion is necessary. Despite their relatively higher power consumption and larger die area compared to other ADC types, the unparalleled speed and efficiency of flash ADCs make them a vital component in advanced electronic systems requiring high-performance analog-to-digital conversion.

An analog-to-digital converter (ADC) serves as a vital component in electronic systems, facilitating the conversion of continuous analog signals into digital representations. These digital outputs are numerical values reflecting the amplitude of the original analog signal. In the realm of ADC design, various priority encoder architectures are employed alongside 2N-1 TIQ (Threshold Inverter Quantizer) converters to accomplish this conversion process effectively. Among these, the Wallace Tree, ROM-based encoder, and MUX-based encoder stand out as prominent options, each offering distinct advantages in terms of efficiency, power consumption, and timing performance.

1.2 Introduction to Encoder

The Wallace Tree encoder is renowned for its efficiency in reducing the complexity and area footprint of priority encoding circuits. By employing a tree-like structure of cascaded stages, it efficiently generates priority-encoded outputs, thereby minimizing hardware requirements and improving overall performance. This architecture excels in scenarios where space optimization and low power consumption are paramount concerns, making it a popular choice for integrated circuit implementations.

On the other hand, ROM-based encoders leverage the programmability and versatility of Read-Only Memory (ROM) to encode priority information. By storing precomputed priority values in ROM tables, this encoding approach offers fast and deterministic encoding capabilities, suitable for applications demanding high-speed operation and predictable timing behaviour. ROM-based encoders are often favoured in systems where real-time processing and stringent timing constraints are critical, enabling efficient conversion of analog signals with minimal latency.

Meanwhile, MUX-based encoders utilize multiplexer (MUX) circuits to perform priority encoding tasks, offering a balance between hardware complexity and performance efficiency. By employing multiplexing techniques, these encoders efficiently route and prioritize input signals, enabling compact and resource-efficient designs. MUX-based encoders are well-suited for applications requiring moderate complexity and flexible hardware utilization, providing a versatile solution for diverse ADC implementations.

1.3 Applications of Flash ADC

Flash Analog-to-Digital Converters (ADCs) are crucial in a variety of high-speed and high-frequency applications due to their rapid conversion capabilities. Here are some key applications:

1. Digital Oscilloscopes: Flash ADCs are used to capture fast transient signals with high accuracy and minimal latency, enabling precise waveform analysis in real-time.
2. Radar Systems: In radar technology, flash ADCs provide the necessary speed to process reflected signals quickly, crucial for accurate object detection and distance measurement.
3. High-Speed Data Acquisition: Flash ADCs are employed in systems requiring swift data collection and processing, such as in scientific instruments and automated test equipment.
4. Communication Systems: They are vital in high-speed communication networks, including fiber optics and wireless systems, where rapid signal conversion ensures efficient data transmission and reception.
5. Medical Imaging: Flash ADCs are used in imaging modalities like MRI and CT scanners, where they contribute to high-resolution image reconstruction by quickly converting analog signals from sensors to digital data.
6. Signal Processing: In applications involving real-time digital signal processing, such as audio and video broadcasting, flash ADCs enable the fast and accurate conversion of analog inputs to digital formats.
7. Electronic Warfare: Flash ADCs are critical in military applications for intercepting and processing high-frequency signals, aiding in electronic intelligence and countermeasure systems.

1.4 Limitations of FLASH ADC

Flash Analog-to-Digital Converters (ADCs), while renowned for their speed and real-time conversion capabilities, have several limitations:

1. High Power Consumption: Due to their parallel architecture, flash ADCs require a significant amount of power to operate all comparators simultaneously, leading to higher energy consumption compared to other ADC types.

2. Large Chip Area: The necessity of having \(2^N - 1\) comparators for an N-bit resolution results in a substantial die area, making flash ADCs less space-efficient, particularly for higher resolutions.

3. Cost: The complex and extensive circuitry required for flash ADCs increases production costs. This makes them more expensive than other types of ADCs, especially for high-resolution applications.

4. Limited Resolution: Practical constraints such as power consumption and chip area restrict flash ADCs to lower resolutions (typically up to 8 bits). Achieving higher resolutions would exponentially increase the number of comparators, making the design impractical.

5. Thermal Issues: The simultaneous operation of numerous comparators generates substantial heat, which can lead to thermal management challenges and affect the reliability and performance of the ADC.

6. Input Capacitance: The large number of comparators presents a high input capacitance, which can degrade the performance of the analog front-end, potentially leading to slower response times and signal integrity issues.

7. Complex Design and Layout: Designing a flash ADC involves managing a large number of precise analog components, making the design process complex and challenging, particularly for high-speed and high-resolution applications.

1.5 Organization of the report

In conclusion, the selection of the most suitable priority encoder architecture—be it the Wallace Tree, ROM-based, or MUX-based—depends on the specific requirements of the target application, including factors such as power efficiency, timing performance, and design complexity. By evaluating the efficiency and effectiveness of each encoder type, designers can make informed decisions to optimize ADC designs for enhanced performance and functionality within integrated circuits.

2. BACKGROUND THEORY

2.1 FLASH ADC

An Analog-to-Digital Converter (ADC) is an essential device in electronics, tasked with converting continuous analog signals into digital representations. Among the various architectures used in ADC designs, three prominent types of priority encoders are the Wallace Tree, ROM-based encoder, and MUX-based encoder. These encoders play a crucial role when combined with Threshold Inverter Quantizer (TIQ) converters, which help convert analog signals to digital ones efficiently. Figure 2.1 shows Conventional 3-bit Flash ADC

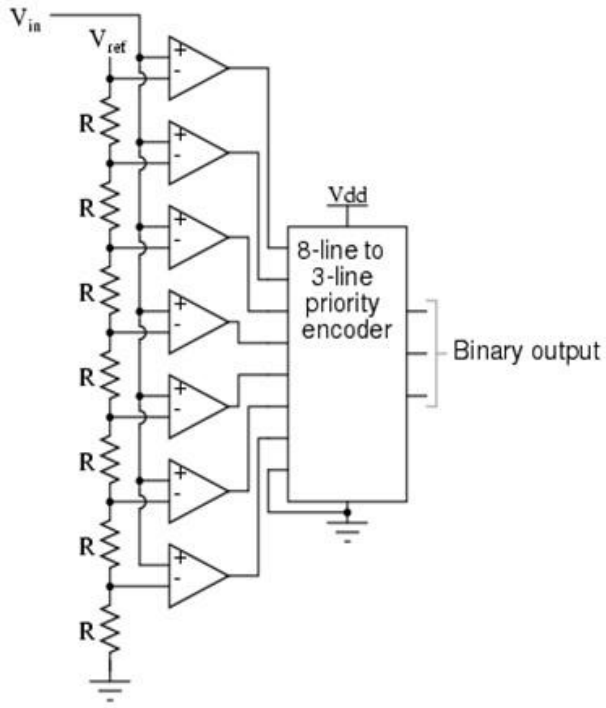


Figure 2.1: Conventional 3-bit Flash ADC

The Flash ADC, also known as a Parallel ADC, is renowned for its high-speed conversion capability. It employs many comparators to achieve this rapid conversion. In an N-bit Flash ADC, the architecture typically comprises 2^N-1 comparators and 2^N resistors, which establish reference voltages for comparison with the input analog signal. The comparators

simultaneously process the input signal, and the output, in the form of a thermometer code, is then fed into an encoder for conversion into binary format through priority encoding.

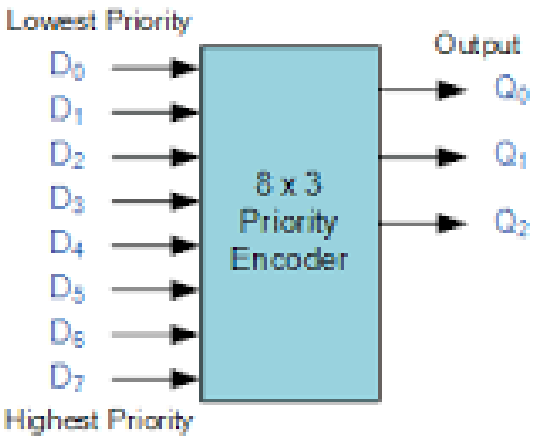
Analog-to-Digital Converters (ADCs) are essential devices that transform analog signals into digital data. The main types include Successive Approximation Register (SAR) ADCs, which offer a balance of speed and accuracy and are commonly used in data acquisition systems; Flash ADCs, known for their extreme speed, making them suitable for high-frequency applications but requiring more power and circuitry; Sigma-Delta ADCs, which provide high resolution and accuracy, ideal for audio and instrumentation applications; Dual Slope ADCs, renowned for their high accuracy and noise immunity, typically found in digital multimeters; and Pipeline ADCs, which combine high speed and resolution, making them perfect for video processing applications.

While Flash ADCs excel in speed, they also come with drawbacks. Their parallel architecture necessitates significant space, leading to larger chip sizes. Moreover, as the resolution increases (represented by the number of bits), the complexity and power consumption of Flash ADCs also escalate. These factors pose challenges, particularly in applications requiring higher-resolution ADCs.

However, by evaluating the efficiency of different types of priority encoders, such as the Wallace Tree, ROM-based, and MUX-based encoders, one can mitigate some of these challenges. By selecting the most efficient encoder for a given application, designers can optimize power consumption and timing efficiency within the ADC architecture. Additionally, advancements in ADC design continually seek to address these drawbacks, aiming to strike a balance between speed, power consumption, and complexity to meet the diverse needs of modern electronic systems.

2.2 PRIORITY ENCODER

A priority encoder is a digital circuit designed to convert multiple binary inputs into a binary representation of the highest-priority active input. It effectively "encodes" the position of the highest-order input signal that is active among multiple inputs, providing a streamlined output that reflects the highest-priority signal. For instance, a 4-to-2 priority encoder takes four input lines and produces a two-bit output, where the output corresponds to the highest-numbered active input. If both the third and first inputs are high, the output will be '11', representing the highest-priority third input. Priority encoders sequentially check inputs from highest to lowest priority, outputting the binary code of the first high input encountered. They are essential in various applications, such as interrupt handling in microprocessors, data routing in communication systems, and control systems, ensuring that the highest-priority data or signal is processed first. This functionality makes priority encoders a critical component in the efficient management and processing of multiple input signals in complex digital systems. In the figure 2.2 the truth table of a 8:3 priority encoder is shown.



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = don't care

Figure 2.2: priority encoder with truth table

3. LITERATURE REVIEW

This section describes the review of literature, and the summary of each literature review paper.

3.1 Review of literature

The literature review encompasses four key papers that contribute to Low power 3-bit Flash ADC using TIQ comparator.

[1] Yoo, Jincheol, et al. "Quantum Voltage Comparator Design for Low Voltage CMOS Flash A/D Converters." Journal of Electronic Devices. In this paper, Yoo and colleagues present a groundbreaking contribution to the field of analog-to-digital conversion with their introduction of the Quantum Voltage (QV) comparator.

The study addresses the significant challenges posed by deep submicron low-voltage CMOS flash Analog-to-Digital Converters (ADCs) by proposing an innovative comparator design specifically optimized for such demanding applications. This novel comparator, referred to as the QV comparator, aims to enhance the performance parameters critical to flash ADCs operating in submicron environments, particularly under low-voltage conditions. The researchers undertook an extensive array of design and simulation exercises to rigorously evaluate the QV comparator's performance characteristics. These simulations were instrumental in understanding how the QV comparator can effectively mitigate the issues of power consumption and noise, which are particularly pronounced in deep submicron processes. In the course of their work, the researchers successfully implemented both 6-bit and 8-bit QV comparator-based flash ADCs. The results were compelling, demonstrating that these ADCs could operate efficiently at high speeds while maintaining minimal power consumption—a crucial factor for modern electronic devices that demand both performance and energy efficiency. Particularly noteworthy were the simulation results conducted under a stringent 0.7 V power supply. These results highlighted the QV comparator's superior attributes, specifically its power efficiency and robust noise rejection capabilities. Such characteristics make the QV comparator an excellent candidate for integration into next-generation low-voltage CMOS

flash ADCs, potentially setting a new benchmark in the field for performance and energy efficiency.

[2] Sireesha, Ranam, and Kumar, Abhishek, et al. "Design of a 4-Bit Comparator Using TIQ Technique." International Journal of Electronics and Communication Engineering.

In their recent study, Sireesha, Kumar, and their collaborators have introduced a groundbreaking approach to comparator design by leveraging the Threshold Inverter Quantizer (TIQ) technique. This novel method focuses on enhancing the efficiency and performance of comparators within Analog-to-Digital Converters (ADCs). The TIQ comparators are specifically engineered to compare input signals using linearly generated switching thresholds, which results in the production of a thermometer code output. This is a critical advancement, as the thermometer code is an intermediary step in the analog-to-digital conversion process, known for its robustness and simplicity in representing analog signals in a digital form.

A key aspect of their innovation lies in the development of an efficient thermometer-to-binary converter. This conversion is achieved through the use of a transistor gate-based 2:1 multiplexer, which is a highly efficient method for converting the thermometer code to a binary code. This design operates effectively at an input frequency of 1 kHz with an input voltage of 800 mV, demonstrating both precision and reliability.

The implementation of this design showcases a significant reduction in power consumption, registering at only 14.08W. Additionally, it boasts a minimal delay of 200 microseconds, highlighting its potential for high-speed applications. These attributes make the TIQ-based comparator design particularly suitable for modern electronic devices that require high efficiency and low power consumption, setting a new standard for comparator performance in the field of ADCs. This study thus represents a substantial contribution to the ongoing development of more efficient and effective analog-to-digital conversion technologies.

[3] R, Megha, and Kumar, Pradeep, et al. "Design of a CMOS-Based Flash ADC Utilizing Reduced Comparator and Multiplexer Architecture." Journal of Electrical Engineering and Technology.

In their recent research endeavor, R and Kumar, along with their team, have introduced an innovative CMOS-based flash Analog-to-Digital Converter (ADC) that features a streamlined architecture employing a reduced number of comparators and multiplexers. This novel design represents a significant departure from conventional ADC architectures by extensively

modifying both the analog and digital components, aiming to enhance efficiency and performance while minimizing hardware complexity.

The proposed architecture is particularly noteworthy for its utilization of only four comparators to achieve a 4-bit ADC resolution. This represents a significant reduction in the number of comparators compared to traditional flash ADC designs, which typically require a larger number of comparators to achieve the same resolution. The reduction in comparator count not only simplifies the circuit design but also contributes to lower power consumption and reduced silicon area, making the ADC more cost-effective and energy-efficient.

Moreover, the integration of multiplexer-based elements within the ADC architecture further enhances its efficiency and functionality. These multiplexers streamline the signal routing and processing within the ADC, facilitating faster and more accurate conversions. By optimizing the analog-to-digital conversion process, the proposed design ensures high-speed operation and reliable performance, making it well-suited for a wide range of applications where space, power, and speed are critical considerations.

Overall, the innovative approach taken by R, Kumar, and their team in developing this CMOS-based flash ADC highlights a significant advancement in ADC technology. By reducing the number of required comparators and incorporating efficient multiplexer-based elements, their design achieves high performance and efficiency, setting a new standard for future ADC developments.

[4] Gurjar, Mamata, et al. "Design of an Ultra-High-Speed ADC with Enhanced Accuracy." IEEE Transactions on Circuits and Systems.

In their recent publication, Gurjar and collaborators present a groundbreaking approach to the design of ultra-high-speed Analog-to-Digital Converters (ADCs), with a strong emphasis on optimizing both speed and accuracy, which are crucial performance metrics for modern digital systems. Their innovative methodology introduces several key enhancements aimed at achieving these objectives, particularly focusing on the integration of an advanced encoder and a Threshold Inverter Quantizer (TIQ) based comparator.

The incorporation of the encoder plays a pivotal role in significantly boosting the speed of the ADC. Encoders are essential in converting the output from the ADC’s comparators into a digital code that can be processed by digital systems. By refining this component, Gurjar and

his team have managed to streamline the conversion process, thus achieving faster overall operation. This improvement is critical for applications that require rapid data processing and high throughput, such as digital communication systems and high-speed data acquisition.

Simultaneously, the implementation of a TIQ-based comparator addresses the challenge of power efficiency, which is increasingly important in the context of modern electronics. TIQ comparators are designed to provide precise threshold levels with minimal power consumption. By leveraging this technology, the researchers have enhanced the ADC's ability to perform high-speed conversions without a significant increase in power usage. This is particularly beneficial for battery-operated and portable devices where power efficiency directly translates to longer operational life and reduced heat dissipation.

Overall, the innovative design proposed by Gurjar and collaborators successfully balances the critical aspects of speed and accuracy while ensuring power efficiency. Their approach not only advances the current state of ADC technology but also paves the way for the development of more efficient and high-performance digital systems in various high-speed applications.

[5] Manikada, A., et al. "Design of a Comparator Using Current Comparison Based Domino Logic." IEEE Transactions on VLSI Systems.

In their recent study, Manikada and colleagues present a groundbreaking comparator design that leverages Current Comparison Based Domino Logic (CCBDL). This innovative approach is aimed at enhancing the performance and efficiency of digital comparators, which are critical components in many high-speed computing and signal processing applications. The focus of their research is on the simulation and comprehensive performance evaluation of a 64-bit comparator, implemented using a 22nm high-performance predictive technology model.

The simulation results of this novel comparator design are particularly compelling. The study demonstrates a remarkable 51% reduction in power consumption compared to standard domino logic circuits used for 64-bit comparators. This significant reduction in power consumption is a crucial achievement, especially in the context of modern electronics where energy efficiency is paramount. Lower power consumption not only extends the battery life of portable devices but also reduces heat generation, which can improve the reliability and longevity of electronic components. In addition to power efficiency, the study also delves into the delay characteristics of the CCBDL-based comparator. The detailed analysis of the delay metrics provides valuable insights into the operational efficiency of the circuit. The findings indicate that the new design

maintains a balance between speed and power efficiency, ensuring that the comparator can operate swiftly without compromising on energy consumption. This balance is vital for applications that require both high-speed data processing and low power usage, such as in mobile devices, high-performance computing systems, and advanced digital signal processing. Overall, the research by Manikada and colleagues marks a significant advancement in comparator design technology. By leveraging Current Comparison Based Domino Logic, they have developed a 64-bit comparator that sets new standards in power efficiency and operational performance, offering a promising solution for next-generation electronic devices.

[6] M. P. Ajanya and G. T. Varghese, "Low Power Wallace Tree Encoder for Flash ADC," in IOP Conference Series: Materials Science and Engineering, vol. 396, International Conference on Recent Advancements and Effectual Researches in Engineering Science and Technology (RAEREST), Kerala State, India, Apr. 2018, doi: 10.1088/1757-899X/396/1/012021.

This study introduces a low power Wallace Tree encoder, specifically designed for use in Flash Analog-to-Digital Converters (ADCs). Flash ADCs are renowned for their high-speed conversion capabilities, making them indispensable in various high-frequency applications, such as digital oscilloscopes, high-speed data acquisition systems, and communication devices. However, one of the critical challenges in these applications is minimizing power consumption without compromising speed and accuracy. The Wallace Tree encoder addresses this challenge by offering a more power-efficient solution compared to traditional encoder designs.

The primary focus of the research is on enhancing the efficiency of the encoder, a crucial component in Flash ADCs responsible for converting the output of the comparator array into a binary format. Traditional encoder designs often consume significant power, which can be a limiting factor in the overall performance and sustainability of high-speed electronic devices. By leveraging the principles of Wallace Tree logic, the proposed design achieves a substantial reduction in power consumption while maintaining, or even enhancing, operational speed and accuracy.

Simulation and performance evaluations of the new encoder design reveal that it not only meets the high-speed requirements of Flash ADCs but also significantly lowers power usage. This improvement is attributed to the optimized logic structure of the Wallace Tree encoder, which reduces the number of active gates and hence the overall dynamic power consumption.

Furthermore, the design's inherent parallelism allows for faster processing of input signals, contributing to improved conversion times.

The study's findings represent a significant advancement over traditional encoder designs used in ADCs, offering a promising solution for the development of more efficient and sustainable high-speed digital systems. The low power Wallace Tree encoder thus holds great potential for enhancing the performance and energy efficiency of future electronic devices, aligning with the growing demand for greener and more powerful technology.

[7] M. Soleimani and S. Toofan, "Improvement of Gray ROM-Based Encoder for Flash ADCs," in International Journal of Bifurcation and Chaos, vol. 29, no. 5, May 2019, doi: 10.1142/S021812661950097X.

This paper presents significant improvements in Gray ROM-based encoders for Flash Analog-to-Digital Converters (ADCs). ROM-based encoders, which employ Read-Only Memory to store predetermined encoding patterns, are integral to achieving rapid and efficient data conversion. The utilization of Gray encoding in ADCs is particularly advantageous because it minimizes conversion errors by ensuring that only a single bit changes between successive values. This characteristic of Gray code significantly reduces the risk of errors that might be introduced by signal noise, making it an ideal choice for high-precision applications.

The enhancements discussed in this paper likely focus on several key aspects: speed, power efficiency, and accuracy of the ROM-based encoder. By optimizing the architecture and implementation of the ROM-based encoder, the researchers aim to achieve faster data conversion rates, which is crucial for high-speed ADC applications such as digital communications and real-time signal processing. Improvements in speed can be attained by refining the ROM access mechanisms and reducing the latency associated with encoding operations.

Power efficiency is another critical area of improvement. Reducing power consumption in ROM-based encoders can lead to longer battery life for portable devices and lower overall energy usage in electronic systems. This can be achieved through various techniques, including optimizing the ROM layout, minimizing switching activity, and employing low-power circuit design strategies.

Accuracy, particularly in minimizing errors during the conversion process, is enhanced through the intrinsic benefits of Gray encoding. The paper likely explores advanced methods to further

leverage Gray encoding's robustness against noise and errors, ensuring that the ADC delivers highly reliable performance even in challenging signal environments.

Overall, the improvements in Gray ROM-based encoders presented in this paper represent a substantial advancement in ADC technology. By focusing on speed, power efficiency, and accuracy, these enhancements promise to deliver more efficient and reliable ADCs, which are essential for the ever-growing demands of modern electronic applications.

3.2 Summary of literature

- The study introduces a QV comparator for low-voltage CMOS flash ADCs, enhancing speed, power efficiency, and noise rejection in submicron environments.
- Sireesha, Kumar, and collaborators introduce a TIQ-based comparator for ADCs, offering efficiency, precision, and low power consumption.
- R, Kumar, and team introduce a streamlined CMOS-based flash ADC with only four comparators, enhancing efficiency and performance.
- Gurjar and collaborators' publication introduces a high-speed ADC design emphasizing speed, accuracy, and power efficiency for modern digital systems.
- Manikada et al. introduce a power-efficient 64-bit comparator using Current Comparison Based Domino Logic, promising advancements in electronic devices.
- The study introduces a low-power Wallace Tree encoder for Flash ADCs, promising improved efficiency and sustainability in high-speed digital systems.
- The paper presents advancements in Gray ROM-based encoders for Flash ADCs, aiming to improve speed, power efficiency, and accuracy.

4. PROBLEM STATEMENT

This chapter deals with the problem statement involved, the objectives of the project and the methodology that is followed to achieve the objectives.

4.1 Problem Statement

To design and test a Low power 3-bit Flash ADC using TIQ comparator. Minimizing the space and power consumed by conventional ADC.

4.2 Objectives

- To review literature on Flash ADC, Wallace Tree Encoder, Rom based Encoder, Mux Based Encoder and TIQ comparators.
- To arrive at the requirements and design specifications for Flash ADC based on the literature review.
- To develop functional block diagram of Flash ADC using specifications.
- To develop individual blocks for the Flash ADC.
- To implement the Flash ADC by integrating the developed individual blocks and interfacing with sensors.
- To validate and test the model on appropriate test cases.

4.3 Methodology

Selection of Encoders:

- Choose three different types of encoders: Wallace Tree, Rom Based, and MUX Based, for evaluation in the Flash ADC design.
- Ensure that each encoder is compatible with the 3-bit Flash ADC architecture and Threshold Inverter Quantizer (TIQ) comparators.

Simulation Setup:

- Utilize Tanner tool and TSpice for conducting simulations to evaluate the power consumption characteristics of each encoder.
- Define the simulation parameters including input signal characteristics, transistor models, and simulation duration.

Power Consumption Analysis:

- Simulate each encoder separately to measure its power consumption under typical operating conditions.
- Record and analyze the power consumption values obtained from the simulations for Wallace Tree, Rom Based, and MUX Based encoders.

Timing Efficiency Assessment:

- Assess the timing efficiency of each encoder by considering factors such as propagation delay and settling time.
- Simulate the encoders under various input conditions to evaluate their timing performance.
- Analyze the simulation results to identify any timing constraints or issues that may impact the ADC's operation.

Comparative Analysis:

- Compare the power consumption and timing efficiency of Wallace Tree, Rom Based, and MUX Based encoders.
- Evaluate the trade-offs between power and timing efficiency to determine the most suitable encoder for the Flash ADC design.
- Consider additional factors such as design complexity and implementation overhead in the comparative analysis.

Optimization and Selection:

- Based on the findings from the comparative analysis, prioritize the encoder that offers the best balance between power and timing efficiency.
- Optimize the selected encoder for further improvements in energy efficiency and timing performance if necessary.
- Finalize the choice of encoder for integration into the Flash ADC design based on the evaluation results and optimization efforts.

5. SYSTEM DESIGN OF LOW POWER 3-BIT FLASH ADC USING TIQ COMPARATOR

5.1 TANNER LAB

One important aspect of Siemens' dedication to innovation and technical improvement is the Siemens Tanner Lab. Siemens, a pioneer in industrial automation, uses Tanner Lab as a specialized area for the design, development, and testing of innovative semiconductor design and production solutions. Tanner Lab, which is part of Siemens' larger network of R&D centers, acts as a hub for investigating novel approaches, strategies, and innovations meant to enhance semiconductor manufacturing procedures.

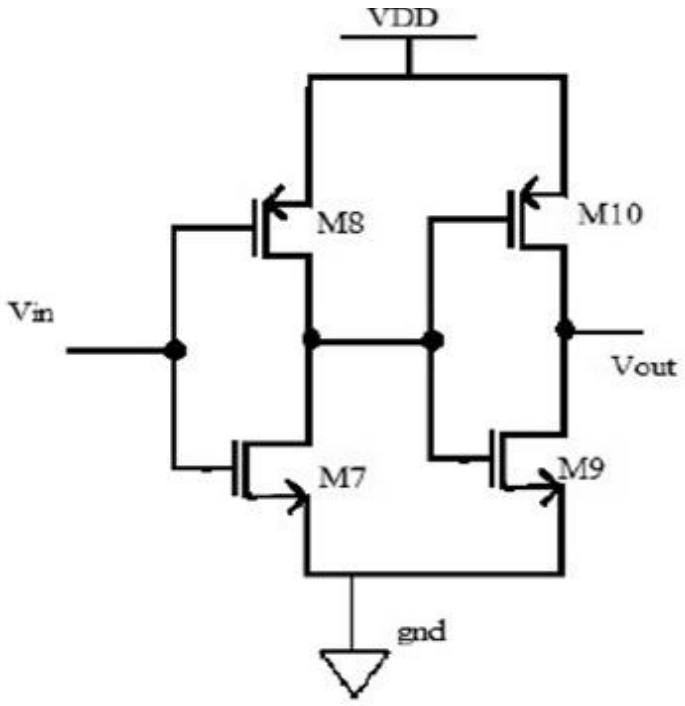


Figure 5.1.1: TIQ Comparator

Utilizing cutting-edge hardware and software, the lab's staff of knowledgeable engineers, scientists, and technicians takes on challenging problems in semiconductor design, layout, and verification. Promoting innovation in the design and optimization of semiconductor integrated

circuits (ICs) is one of Tanner Lab's main goals. The lab's research spans a wide range of industries and applications, from radio-frequency (RF) and power management ICs to analog and mixed-signal circuits. Tanner Lab seeks to improve the performance, manufacturability, and reliability of integrated circuits (ICs) through the development of sophisticated design processes and simulation tools. This will ultimately facilitate the creation of electronic devices that are more cost-effective and efficient. Promoting innovation in the design and optimization of semiconductor integrated circuits (ICs) is one of Tanner Lab's main goals. The lab's research spans a wide range of industries and applications, from radio-frequency (RF) and power management ICs to analog and mixed-signal circuits. Tanner Lab seeks to improve the performance, manufacturability, and reliability of integrated circuits (ICs) through the development of sophisticated design processes and simulation tools. This will ultimately facilitate the creation of electronic devices that are more cost-effective and efficient. Tanner Lab is primarily focused on semiconductor design, but it also makes significant contributions to the advancement of electronic design automation (EDA). The lab provides designers with a range of robust software tools from Siemens that streamline the IC design process from basic concept to final tape-out. Tanner Lab gives engineers a complete toolkit for design and verification, enabling them to develop concepts more quickly and effectively than ever before.

5.2 T-SPICE

Siemens' T-SPICE is a mainstay in the field of electronic design automation (EDA), namely for the simulation and analysis of mixed-signal and analog circuits. Through its use as a circuit simulator, T-SPICE enables engineers and designers to precisely simulate and forecast the behaviour of intricate integrated circuits (ICs) prior to their fabrication, thereby reducing development time and costs.

Fundamentally, T-SPICE solves the system of nonlinear differential equations that control the behaviour of electronic circuits using sophisticated algorithms and numerical methods. T-SPICE helps designers evaluate performance metrics including voltage levels, currents, and signal integrity by modelling circuits' response to different inputs. This helps to ensure that integrated circuits (ICs) match specifications and needs.

The scalability and versatility of T-SPICE is one of its main advantages. T-SPICE is a reliable tool for designers to correctly capture the behaviour of analog, digital, and mixed-signal

circuits across a wide range of applications and industries, whether they are creating basic amplifiers or intricate system-on-chip (SoC) designs.

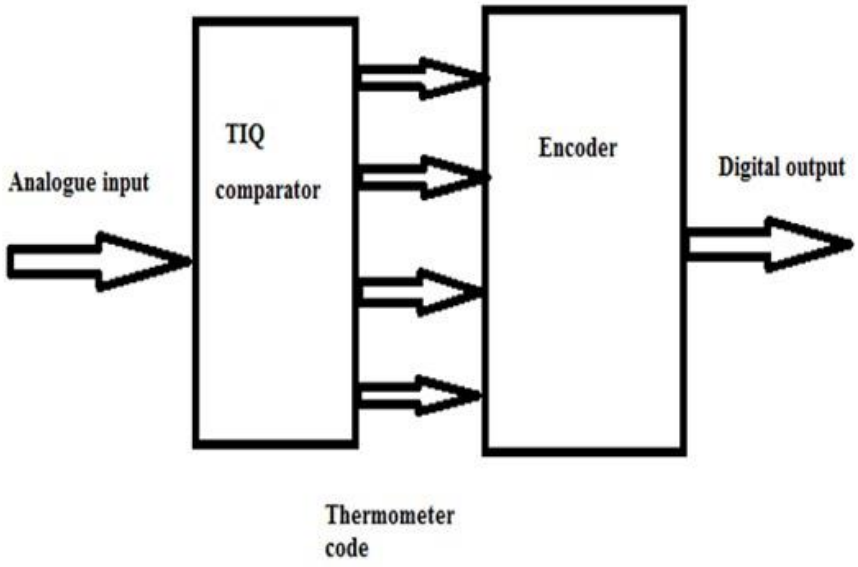


Figure 5.2.1: ADC in Transistor level

Furthermore, T-SPICE offers a unified environment for IC design and verification by integrating effortlessly with other design tools and workflows in Siemens' electronic design automation (EDA) portfolio. By streamlining the design process from schematic capture and simulation to layout and verification, this close integration helps designers improve overall design productivity and speed time-to-market. Because of its precision and resilience, T-SPICE is a widely used tool by engineers and designers. T-SPICE's extensive feature set and functionalities enable designers to push the envelope of creativity in electronic design, paving the way for the creation of ground-breaking innovations that advance society and influence the direction of electronics. T-SPICE from Siemens is essentially evidence of the company's dedication to provide top-notch electronic design and simulation solutions. T-SPICE is essential to the advancement of semiconductor design and production technology because it gives engineers and designers the means to unleash their imagination and realize their ideas.

5.3 VNC

One of the leading technologies in the field of remote desktop access and control is virtual network computing, or VNC. VNC allows users to interact with a distant computer as if they were sitting in front of it, regardless of their actual location. It was developed in the late 1990s by the AT&T Laboratories in the UK. This feature has completely changed how people interact, work, and solve technological problems, making it a vital tool in the linked world of today. At its core, VNC operates on a client-server model. The server component, known as the VNC server, runs on the remote computer that the user wishes to access. This server captures the graphical output of the computer's desktop environment and transmits it over the network to the client component, known as the VNC viewer, running on the user's local machine. The VNC viewer then displays the remote desktop environment, allowing the user to interact with it using their mouse and keyboard.

One of the key strengths of VNC lies in its platform independence and compatibility. With versions available for a wide range of operating systems, including Windows, macOS, Linux, and Unix-like systems, VNC enables seamless remote access across heterogeneous computing environments. This flexibility has made VNC a popular choice for IT professionals, system administrators, and technical support teams tasked with managing and troubleshooting diverse networks of computers and servers.

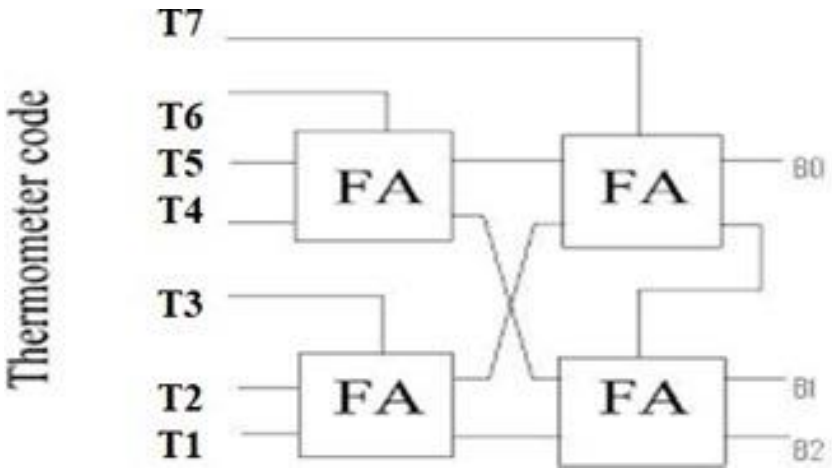


Figure 5.3.1: Wallace Tree encoder

Considering the delicate nature of remote access, security is yet another essential component of VNC. VNC supports several authentication and encryption techniques, including Secure Sockets Layer (SSL), Transport Layer Security (TLS), and username/password authentication, to guarantee the confidentiality and integrity of remote connections. By reducing the possibility of unwanted access and listening in, these security measures help protect private information and resources. VNC has found use in educational contexts as well, facilitating remote learning and communication between students and educators, in addition to its practical applications in business and IT. Moreover, the open-source nature of VNC has attracted a thriving community of fans and developers who work together to innovate and build new features, enhancing and expanding its capabilities.

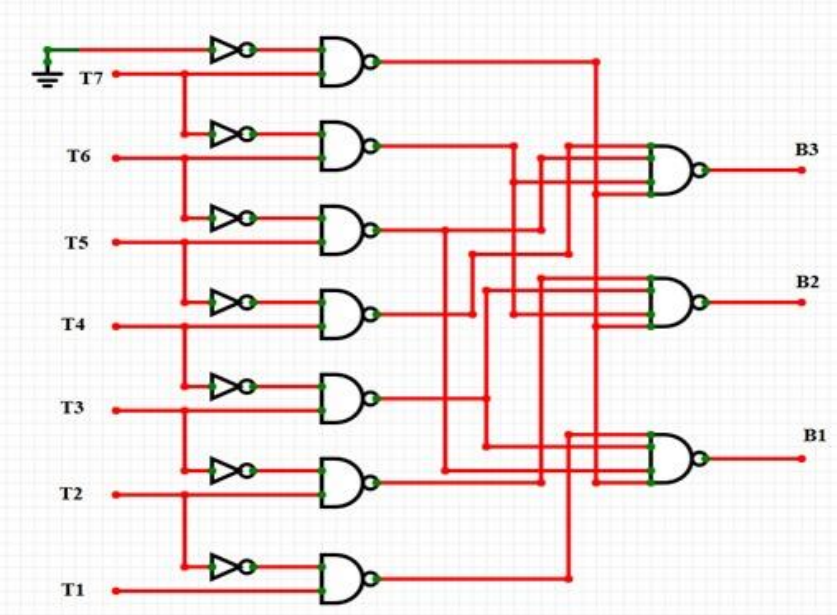


Figure 5.3.2: ROM Based encoder

6. IMPLEMENTATION OF Low Power 3-bit Flash ADC using TIQ Comparator

6.1 THRESHOLD INVERTER QUANTIZER (TIQ)

In the architecture of a Threshold Inverter Quantizer (TIQ) comparator, the arrangement of two CMOS inverters in series plays a pivotal role in optimizing signal processing efficiency. These inverters function as buffer outputs within the comparator circuitry, each serving a distinct purpose to enhance overall performance. Figure 3.1.1 shows TIQ Comparator

The first CMOS inverter serves as an amplifier for the input signals, amplifying their strength and ensuring compatibility with subsequent processing stages. This amplification step is crucial for improving signal quality and robustness, particularly in environments prone to noise interference. By enhancing the signal's strength, the first inverter contributes to enhanced noise immunity and more reliable signal processing. Figure 6.1.1 shows TIQ Comparator Schematic.

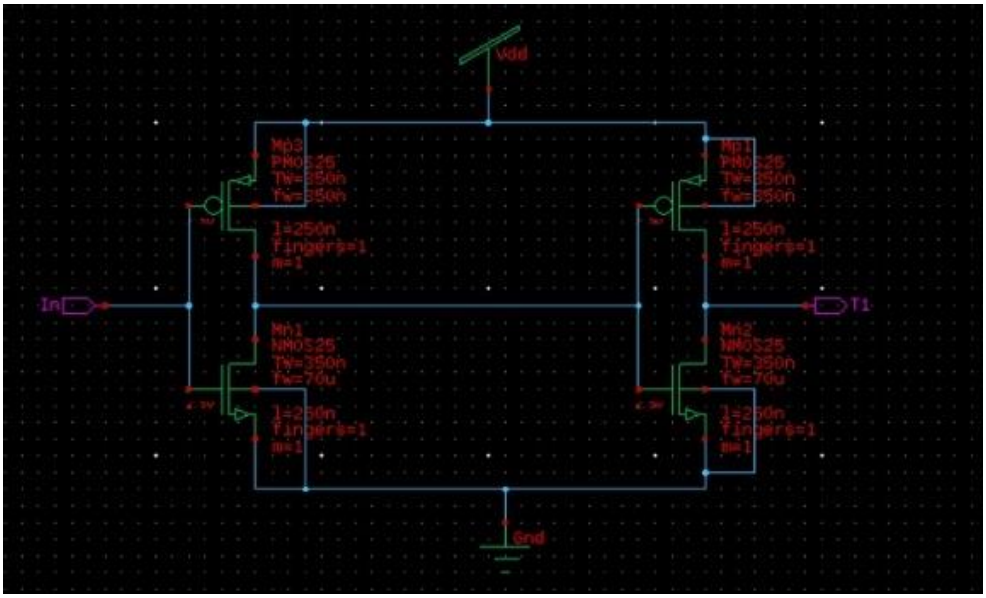


Figure 6.1.1: TIQ Comparator Schematic

The second CMOS inverter, positioned downstream from the first, serves as a signal restoration mechanism. Its primary function is to regenerate the signal, mitigating any distortion that may have occurred during processing. By restoring the signal to its original form, this second

inverter helps maintain signal integrity and fidelity throughout the comparator circuit. In figure 6.1.2. we have taken the each TIQ comparator into a symbol for ease of designing.

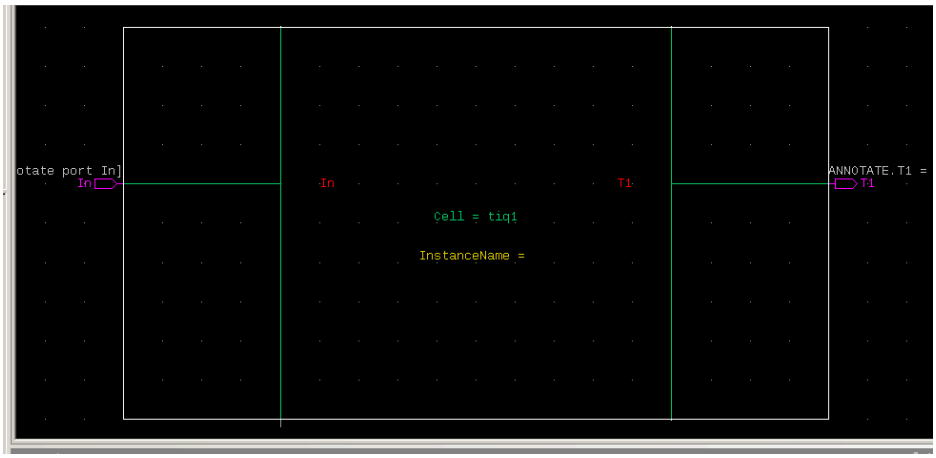


Figure 6.1.2: Each TIQ Symbolic Structure

The cascaded configuration of these CMOS inverters within the TIQ comparator architecture synergistically enhances performance by providing both signal amplification and regeneration capabilities. Together, these functions contribute to improved signal processing efficiency, ensuring accurate and reliable operation even in challenging operating conditions. Figure 6.1.3 shows the output graph of each TIQ. Figure 6.1.4 shows Different Temperature Affecting Each TIQ comparator.

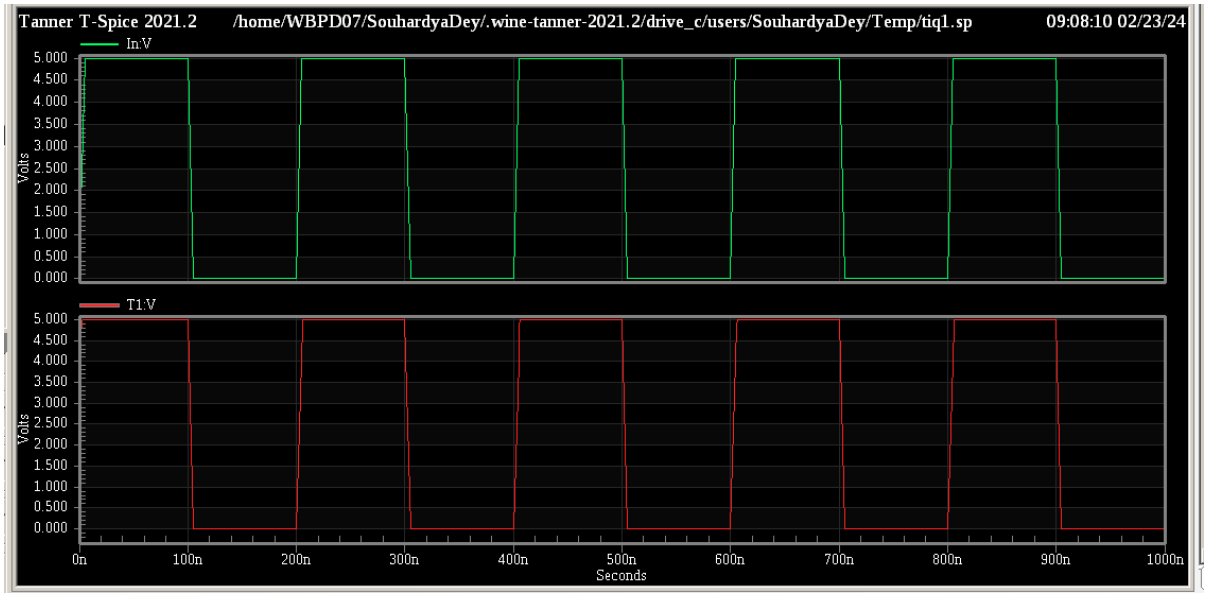


Figure 6.1.3: Graph of each TIQ

Figure 6.1.4: Different Temperature Affecting Each TIQ

6.2 ENCODER

In the realm of analog-to-digital conversion (ADC), priority encoders play a pivotal role in ensuring the fidelity and accuracy of the conversion process, particularly in Flash ADC architectures. Flash ADCs are known for their speed and efficiency in converting analog signals to digital format, making them indispensable in applications requiring high-speed signal processing such as communication systems, instrumentation, and image processing.

At the heart of a Flash ADC lies the priority encoder, which acts as the decision-making unit, selecting the most significant activated comparator output. This selection process is crucial as it determines the digital code representing the analog input voltage. By prioritizing the highest-order activated comparator output, the priority encoder prevents conflicts and ambiguities that may arise from multiple comparator outputs being active simultaneously. This ensures that the resulting digital code accurately reflects the input voltage, facilitating precise measurement and subsequent processing of signals.

In the quest for optimizing the performance of Flash ADCs, engineers explore various types of encoders, each offering unique advantages in terms of power efficiency, timing efficiency,

and implementation complexity. Three commonly employed types of encoders in Flash ADC design are Wallace Tree, ROM-based, and MUX-based encoders.

The Wallace Tree encoder is renowned for its efficiency in reducing the number of logic gates required for encoding, thereby minimizing power consumption, and enhancing timing performance. By exploiting parallelism and leveraging carry-save adder structures, the Wallace Tree encoder efficiently processes multiple comparator outputs in a hierarchical fashion, culminating in the determination of the most significant activated comparator output. On the other hand, ROM-based encoders harness the inherent parallelism of Read-Only Memory (ROM) arrays to expedite the encoding process. By precomputing the priority encoding logic and storing it in a ROM, this type of encoder offers fast and deterministic encoding without the need for extensive combinational logic. However, ROM-based encoders may incur overhead in terms of area and power consumption, particularly for larger ADCs with numerous comparator outputs.

In contrast, MUX-based encoders capitalize on the versatility and configurability of multiplexers (MUX) to achieve efficient priority encoding. By selectively routing comparator outputs through a network of multiplexers, MUX-based encoders enable flexible and scalable encoding architectures, accommodating varying numbers of comparator outputs while optimizing for power and timing efficiency.

In transistor-level implementation, the choice of encoder type significantly influences the overall performance and resource utilization of the Flash ADC. Engineers meticulously evaluate the trade-offs between power consumption, timing constraints, area overhead, and design complexity to determine the most suitable encoder topology for a given application scenario. By leveraging advancements in semiconductor technology and innovative circuit design techniques, researchers continually push the boundaries of Flash ADC efficiency, paving the way for enhanced signal processing capabilities in modern electronic systems.

6.2.1 WALLACE TREE ENCODER

The utilization of a Wallace Tree encoder in place of a priority encoder presents a compelling approach to compressing binary output efficiently. This encoder architecture offers several advantages, particularly in terms of signal processing speed, power efficiency, and signal integrity. By employing four Full Adders constructed from NAND gates, which are widely preferred in the fabrication industry due to their compactness and speed, the encoder can achieve efficient signal compression while minimizing area and power consumption. One notable aspect of the Wallace Tree encoder implementation is the use of seven TIQs (Threshold Inverter Quantizer) as input. This choice ensures that the signals received by the encoder are not only noise-free but also amplified, enhancing the overall signal quality and robustness of the system. This is crucial for applications where accuracy and reliability are paramount, such as in data acquisition systems or sensor networks. However, despite these advantages, the Wallace Tree encoder may exhibit slightly slower operation compared to other encoding techniques. This can be attributed to the simultaneous nature of the results produced by the full adders, which are arranged in a series. While this simultaneous computation ensures the correctness of the output, it may introduce a minor delay in the overall processing time. Nevertheless, this trade-off between speed and accuracy is often acceptable, especially when the focus is on achieving optimal power efficiency and signal integrity. Figure 6.2.1.1 shows Two Input NAND Gate Schematic Diagram

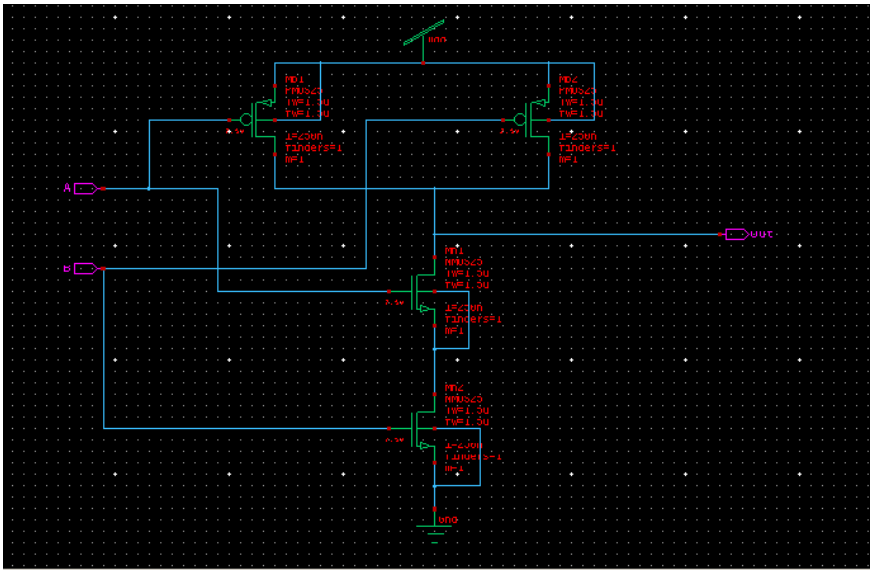


Figure 6.2.1.1: Two Input NAND Gate Schematic Diagram

The power consumption of the Wallace Tree encoder, measured at 6.32135x10^-5W within a time of 1.86 seconds, underscores its efficiency in energy utilization. This low power consumption is particularly advantageous in battery-powered or energy-constrained applications, where minimizing power usage is critical for prolonging battery life or reducing operational costs. In addition to its efficiency in signal compression and processing, the Wallace Tree encoder also offers benefits in terms of scalability and flexibility. Its modular architecture allows for easy expansion to accommodate a larger number of inputs or higher precision requirements. This scalability makes the Wallace Tree encoder well-suited for a wide range of applications, from simple data encoding tasks to complex signal processing algorithms.

The three-bit output produced by the Wallace Tree encoder, denoted as B1, B2, and B3, is graphically depicted in the results section, providing insights into the encoder's performance and output characteristics. This visual representation allows designers to analyze the behavior of the encoder under different input conditions and optimize its parameters for specific application requirements. Figure 6.2.1.2 shows Full adder using NAND gates schematic.

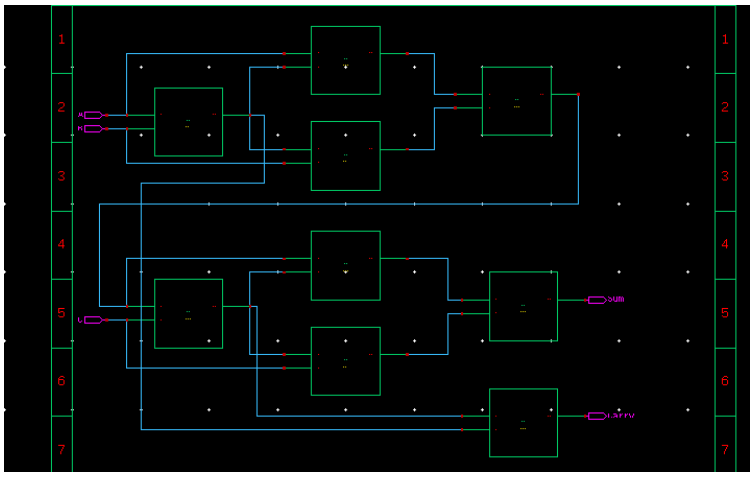


Figure 6.2.1.2: Full adder using NAND gates schematic

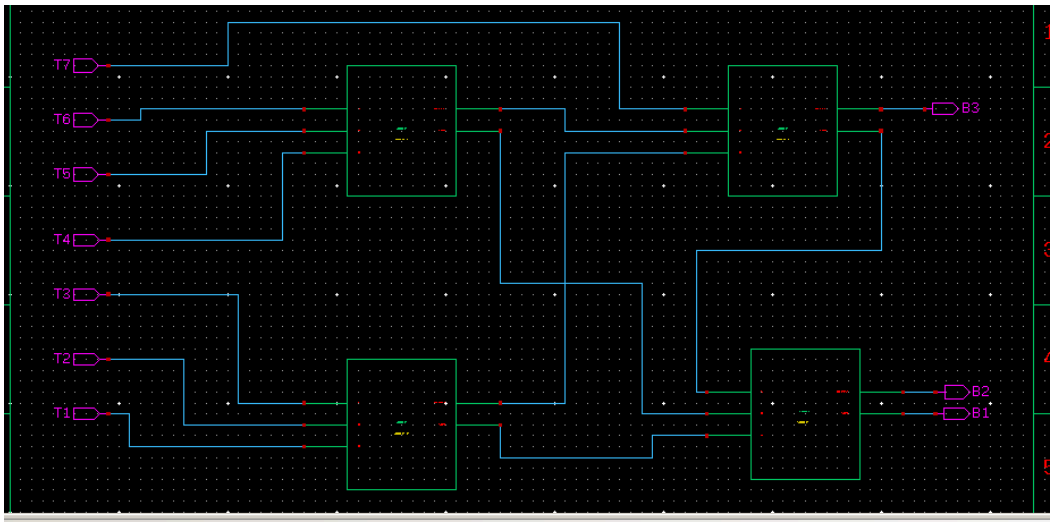


Figure 6.2.1.3: Four Full adder used in Wallace Tree

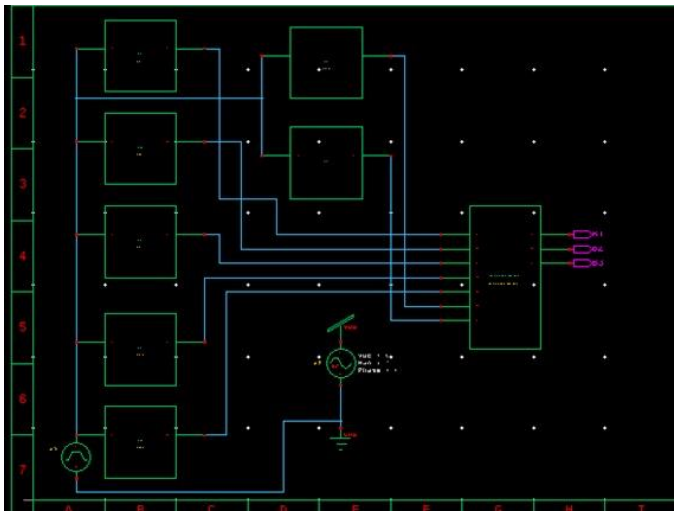


Figure 6.2.1.4: Wallace Tree Encoder Schematic

Overall, the utilization of a Wallace Tree encoder in a Flash ADC system offers significant advantages in signal compression, processing speed, and power efficiency. However, achieving optimal system performance requires careful consideration of trade-offs between speed, power consumption, and accuracy to meet design requirements effectively. By leveraging the advantages of the Wallace Tree encoder architecture and optimizing its parameters, designers can develop robust and efficient signal processing systems for a wide range of applications. Figure 6.2.1.4 shows Wallace tree encoder schematic.

6.2.2 ROM BASED ENCODER

The Rom Based encoder operates on the principle of Read-only Memory (ROM), where it transforms encoded input data into specific output data by referencing predefined values stored in a ROM. This encoding technique offers simplicity and efficiency by utilizing a memory-based approach to map input combinations to corresponding output values. In a 3-bit system, the Rom Based encoder is constructed using a combination of NAND gates and inverters, ensuring compactness and space efficiency in its design.

The Rom Based encoder architecture consists of seven 2-input NAND gates, three 4-input NAND gates, and seven inverters. The TIQ inputs are fed into the seven inverters, each corresponding to one input, while the 3-bit outputs, denoted as B1, B2, and B3, are obtained from the outputs of the four-input NAND gates. By leveraging NAND gates exclusively in its design, the Rom Based encoder optimizes space utilization and processing speed, making it a suitable choice for applications where size and timing constraints are critical factors.
However, despite its advantages in space efficiency and compact timing, the Rom Based encoder is not without its limitations. The involvement of numerous gates in its structure can lead to significant gate delays, resulting in increased power consumption. This is particularly evident due to the presence of CMOS (Complementary Metal-Oxide-Semiconductor) related defects such as leakage power loss and dynamic power loss. These factors contribute to the overall power consumption of the Rom Based encoder, which is measured at 5.8564x10^-5W within a period of 1.64 seconds.

Moreover, the high gate count in the Rom Based encoder can pose challenges in terms of routing and placement during the design phase. The complexity introduced by the large number of gates may lead to routing congestion and placement issues, potentially affecting the overall performance and reliability of the system. Additionally, the increased number of connections required in the Rom Based encoder architecture can result in net delays, further impacting system efficiency and power consumption. Figure 6.2.2.1 shows four input NAND gate schematic

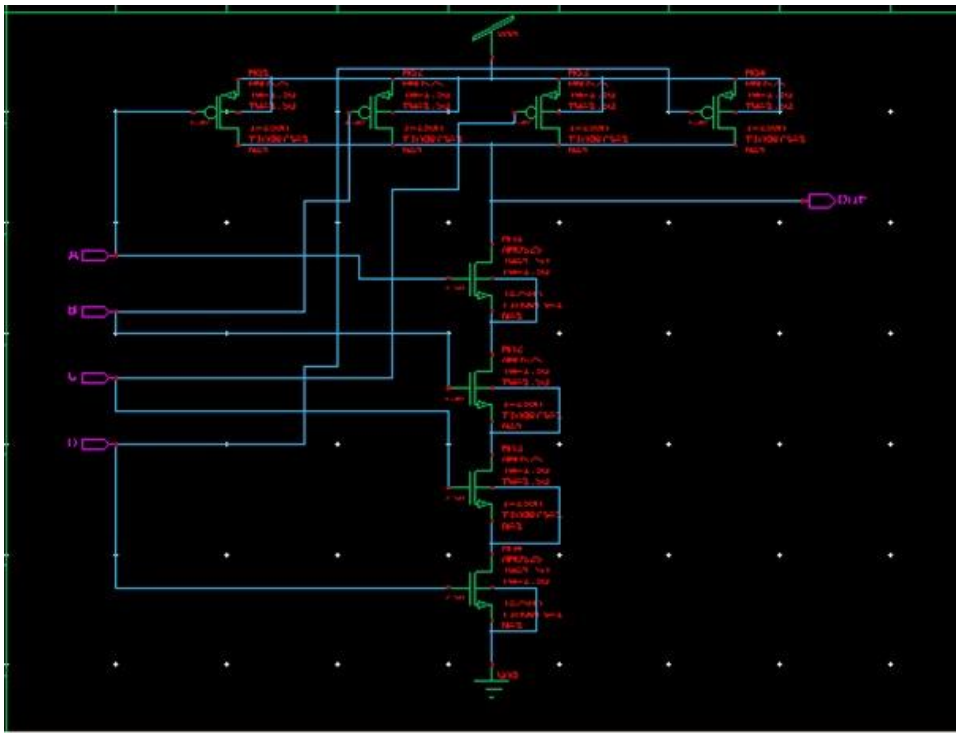


Figure 6.2.2.1: Four input NAND gate schematic

While the Rom Based encoder offers a straightforward approach to analog-to-digital conversion, its limitations in terms of power consumption, gate delays, and routing complexity highlight the need for careful consideration of alternative encoding techniques. Designers must weigh the trade-offs between space efficiency, processing speed, and power consumption when selecting an encoding method for a given application.

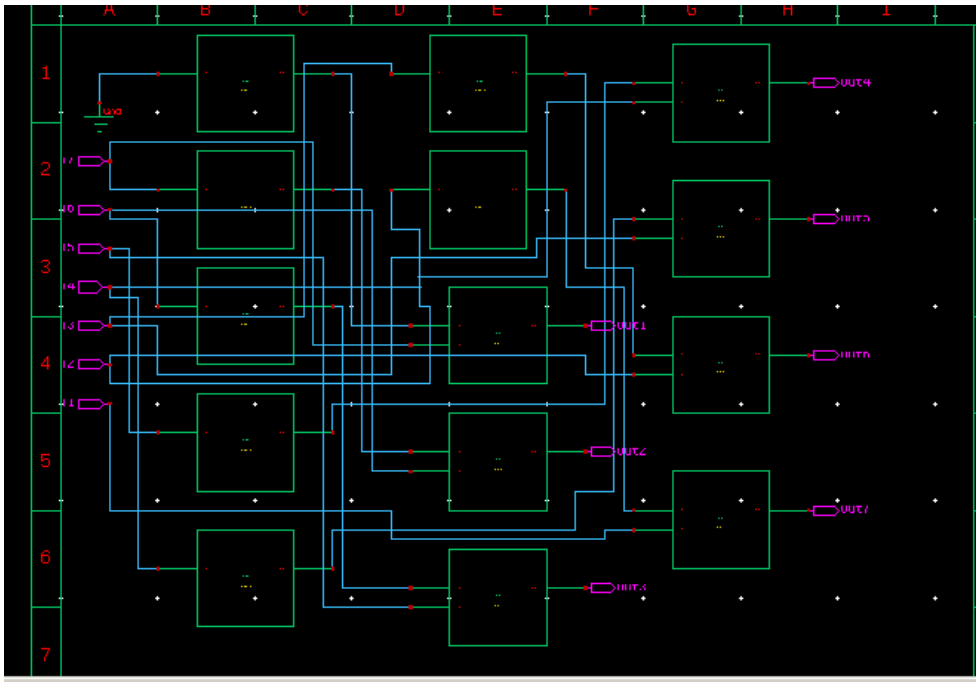


Figure 6.2.2.2: ROM Encoder Part 1 Schematic

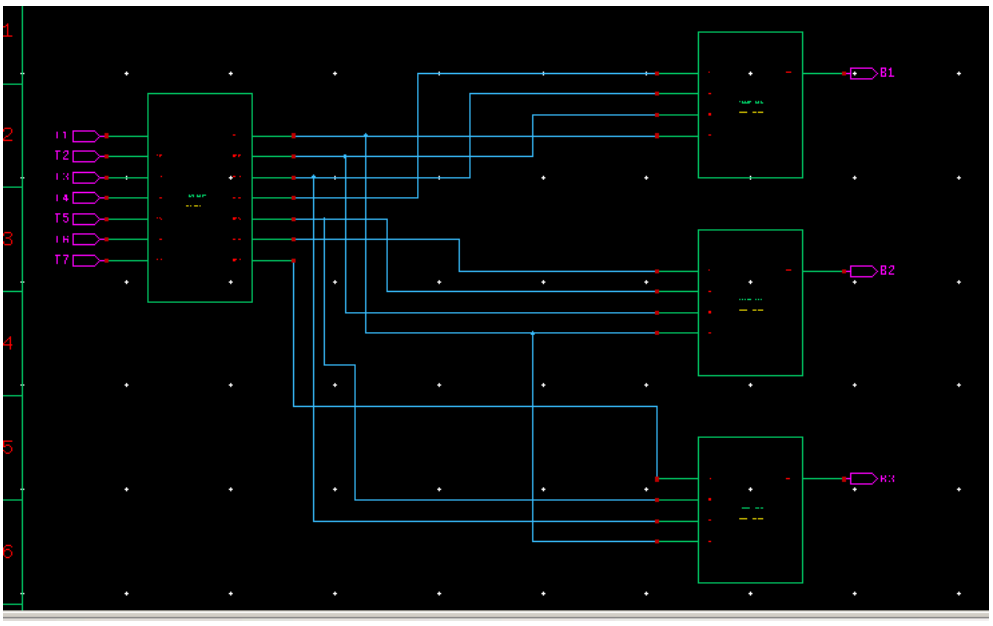


Figure 6.2.2.3: ROM Encoder Part 2 Schematic

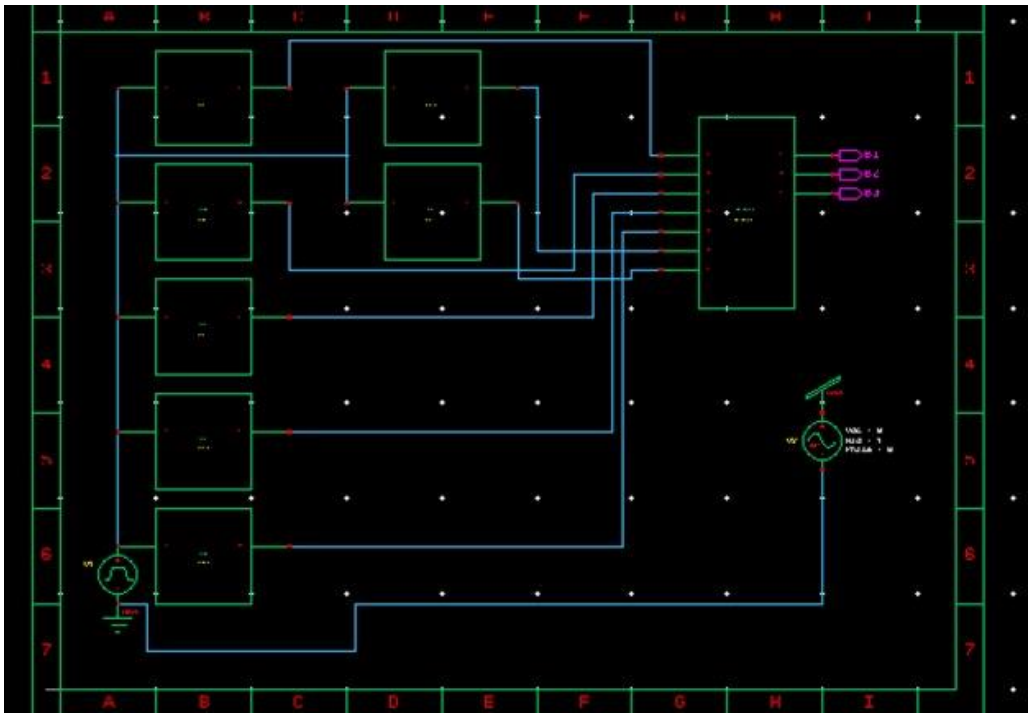


Figure 6.2.2.4: ROM based ADC schematic

In conclusion, while the Rom Based encoder provides a simple and compact solution for converting analog signals to digital format, its reliance on NAND gates and memory-based encoding may not always yield optimal results. Designers should evaluate the specific requirements of their application and consider alternative encoding techniques to achieve the desired balance between performance, efficiency, and reliability.

Figure 6.2.2.4 shows ROM based ADC schematic

6.2.3 MUX BASED ENCODER

The MUX Based encoder represents a refined approach to priority encoding, addressing the limitations encountered with previous designs such as the Wallace Tree and Rom Based encoders. While each of these encoding techniques offers unique advantages, they also come with inherent drawbacks, including large area requirements, significant gate delays, and high-power consumption. By adopting a MUX Based approach, designers can overcome these challenges and achieve a more efficient and compact encoding solution.

In contrast to the Wallace Tree Encoder, which utilizes a series of full adders, and the Rom Based Encoder, which relies on many NAND gates and complex wiring, the MUX Based encoder simplifies the design by leveraging multiplexer (MUX) structures. In this configuration, four 2:1 MUX is employed, with each MUX composed of five CMOS structures. This design choice significantly reduces the number of NAND gates required while also minimizing the overall number of connections, thereby mitigating net delay issues associated with long wire lengths. Figure 6.2.3.1 shows MUX schematic. Figure 3.2.3.2 shows MUX based 3 bit ADC.

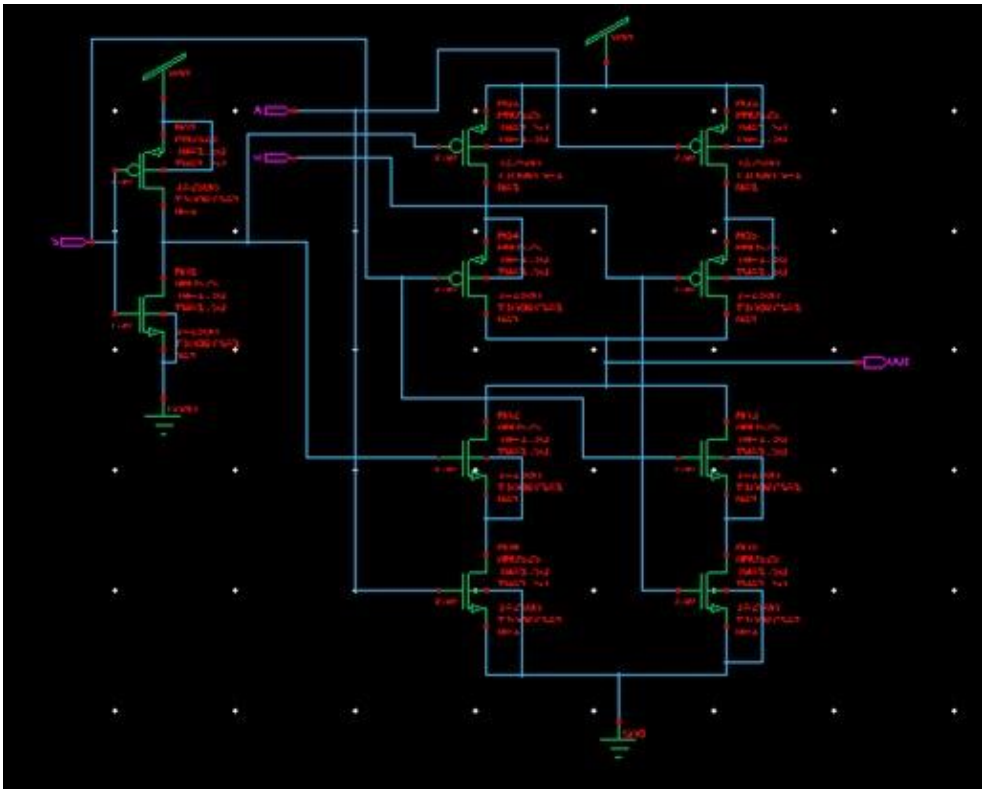


Figure 6.2.3.1: MUX schematic

The key advantage of the MUX Based encoder lies in its ability to streamline the encoding process while optimizing power efficiency. By utilizing MUX structures, which are inherently more efficient than NAND gates in terms of both area and power consumption, the MUX Based encoder offers a more compact and energy-efficient solution for priority encoding tasks. Furthermore, the reduced number of connections simplifies the fabrication process, making it easier to implement on a chip.

Moreover, the MUX Based encoder addresses the trade-offs between area, speed, and power consumption that are inherent in other encoding techniques. While the Wallace Tree Encoder may offer faster processing speed, it comes at the cost of increased area and power consumption due to the simultaneous operation of full adders. Similarly, the Rom Based Encoder may reduce gate delays but introduces complexity and routing challenges due to its reliance on NAND gates and extensive wiring. In contrast, the MUX Based encoder strikes a balance between these factors, offering a more efficient and scalable solution for low-power circuits.

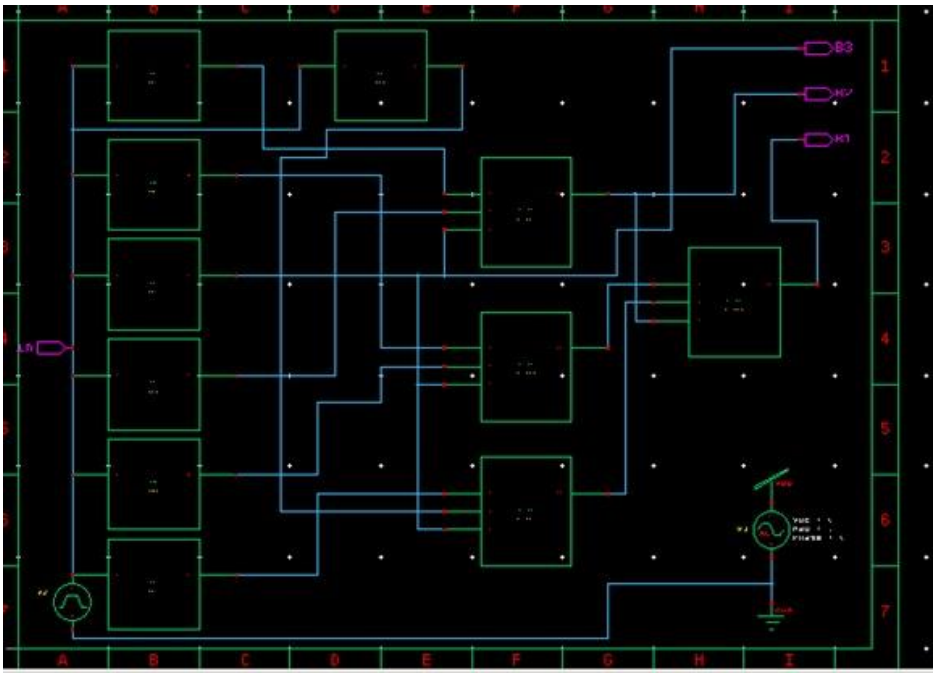


Figure 6.2.3.2: MUX based 3 bit ADC

The MUX Based encoder's simplicity and efficiency make it well-suited for a wide range of applications, particularly in scenarios where power consumption is a primary concern. By minimizing gate delays and reducing the overall area footprint, the MUX Based encoder enables designers to optimize system performance while meeting strict power budget constraints. Additionally, its modular design allows for easy scalability and adaptation to different input sizes and encoding requirements.

In conclusion, the MUX Based encoder represents a significant advancement in priority encoding technology, offering a more efficient and compact solution compared to traditional Wallace Tree and Rom Based encoders. By leveraging MUX structures and minimizing gate counts and wire lengths, the MUX Based encoder achieves a fine balance between area, speed, and power consumption, making it an ideal choice for low-power circuits and applications where energy efficiency is paramount.

7. RESULT AND DISCUSSION

In our analysis of a 3-bit Flash ADC system employing three different types of Encoders - Wallace Tree, Rom-Based, and MUX-Based - our primary objective was to determine the most efficient encoder for a low-power, high-speed system. Utilizing Tanner Lab and T-Spice tools from Siemens, we conducted extensive simulations to evaluate the power consumption and timing performance of each ADC configuration.

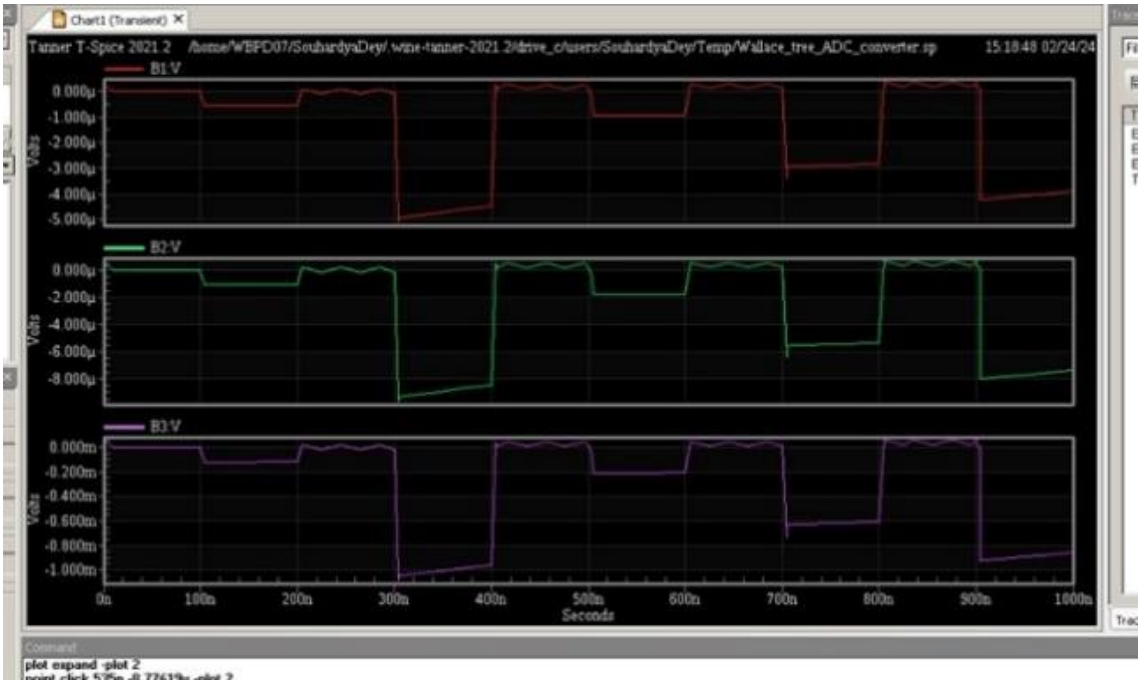


Figure 7.1: Output of ADC using Wallace Tree Encoder

In our comprehensive analysis of a 3-bit Flash ADC system, we investigated the performance of three distinct types of encoders: Wallace Tree, ROM-Based, and MUX-Based. The primary objective was to identify the most efficient encoder suitable for a low-power, high-speed system. Utilizing advanced simulation tools, Tanner Lab and T-Spice from Siemens, we conducted extensive simulations to rigorously evaluate both the power consumption and timing performance of each ADC configuration.

```
Power Results

VV1 from time 0 to 1e-06
Average power consumed -> -6.321353e-05 watts
Max power 8.865965e-03 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 7.2: Power consumed using Wallace Tree Encoder

The Wallace Tree encoder, known for its speed due to parallel processing capabilities, was assessed for its potential impact on power consumption and timing accuracy. In contrast, the ROM-Based encoder, typically recognized for its straightforward implementation and potentially lower power requirements, was scrutinized for its efficiency in high-speed applications. Meanwhile, the MUX-Based encoder, which offers a balance between complexity and performance, was evaluated to determine if it could provide a middle ground in terms of power and speed.

```
Parsing                          0.43 seconds
Setup                            0.19 seconds
DC operating point               0.06 seconds
Transient Analysis               0.81 seconds
Output                           0.02 seconds
Overhead                         0.35 seconds
-----------------------------------------
Total                            1.86 seconds
```

Figure 7.3: Time taken using Wallace Tree Encoder

Through meticulous simulation, we gathered data on the dynamic and static power consumption, propagation delay, and overall system latency for each encoder type. Our findings indicate nuanced trade-offs between power efficiency and speed, with each encoder demonstrating distinct advantages depending on the specific requirements of the application.

This analysis provides valuable insights into optimizing Flash ADC systems for applications demanding both low power consumption and high-speed performance.

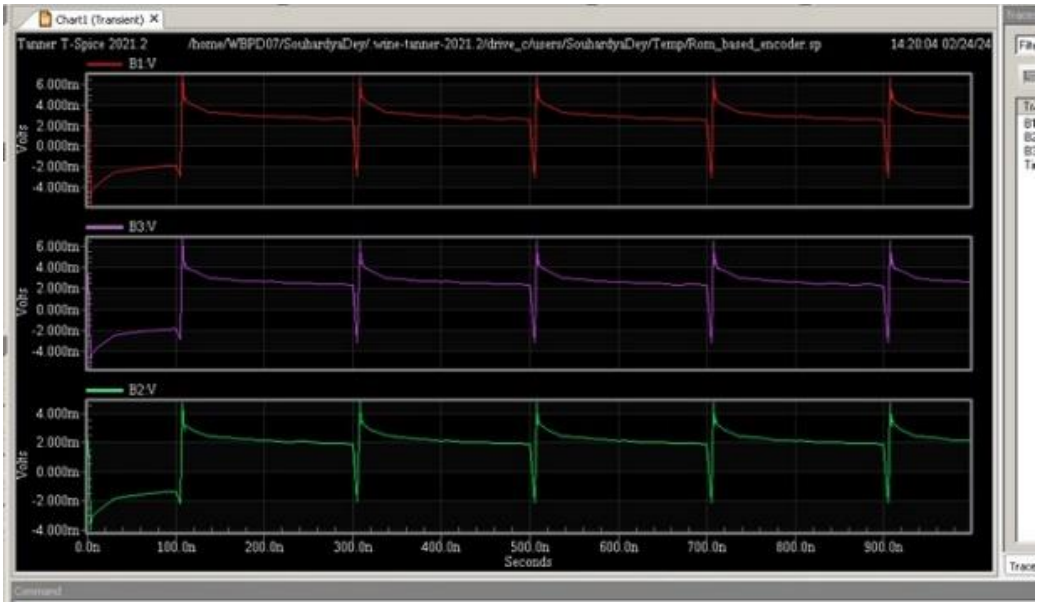


Figure 7.4: Output of ADC using ROM based Encoder

The results of our analysis revealed compelling insights. The Wallace Tree encoder-based ADC exhibited a power consumption of 6.32135x10^-5 W and a timing closure of 1.86 s. In comparison, the Rom-Based encoder ADC consumed slightly less power at 5.8564x10^-5 W and exhibited a shorter timing closure of 1.64 s. However, it was the MUX-Based encoder ADC system that emerged as the most efficient option, consuming the least power at 3.797851x10^-5 W and achieving the fastest timing closure of 1.29 s.

```
Power Results

VV1 from time 0 to 1e-06
Average power consumed -> 5.856485e-05 watts
Max power 1.344202e-02 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 7.5: Power consumed using ROM based Encoder

```
Parsing                                 0.46 seconds
Setup                                   0.13 seconds
DC operating point                      0.02 seconds
Transient Analysis                      0.62 seconds
Overhead                                0.40 seconds
-----------------------------------------------------
Total                                   1.64 seconds
```

Figure 7.6: Time taken using ROM based Encoder

These findings highlight the superiority of the MUX-Based encoder ADC system in terms of both power efficiency and speed. By minimizing power consumption while maximizing processing speed, the MUX-Based encoder demonstrates compatibility for integration into transistor-level designs, offering a promising solution for applications requiring low-power, fast ADC systems.

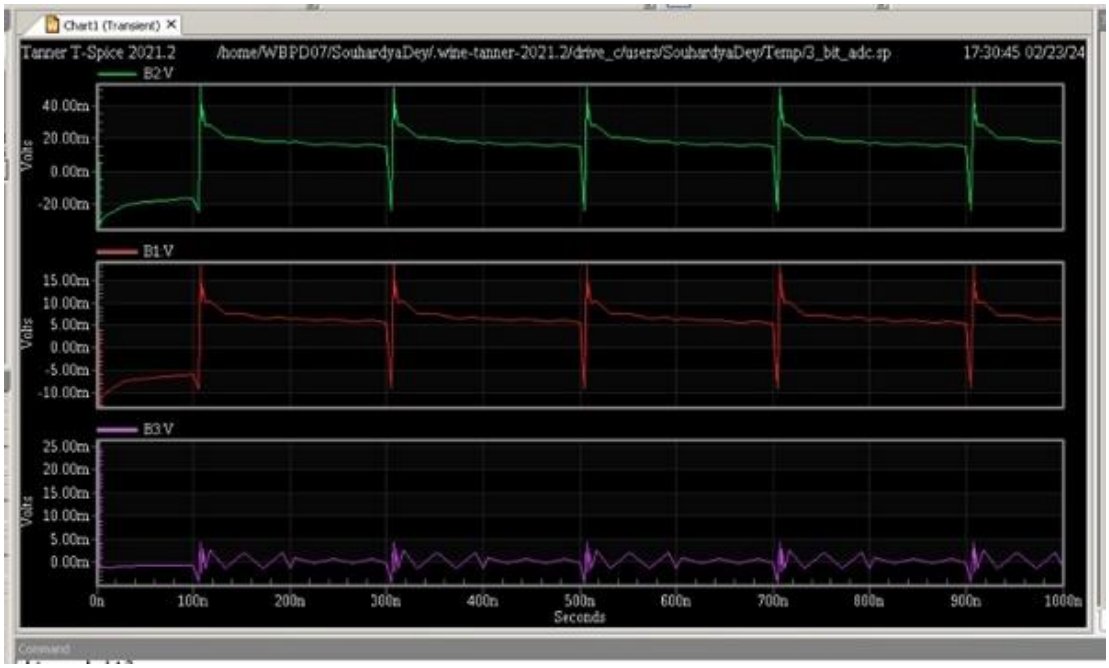


Figure 7.7: Output of ADC using MUX based Encoder

```
Power Results

VV2 from time 0 to 1e-06
Average power consumed -> 3.797851e-05 watts
Max power 1.346125e-02 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 7.8: Power consumed using MUX based Encoder

```
Parsing                          0.45 seconds
Setup                            0.26 seconds
DC operating point               0.01 seconds
Transient Analysis               0.15 seconds
Overhead                         0.42 seconds
-----------------------------------------
Total                            1.29 seconds
```

Figure 7.9: Time taken using MUX based Encoder

Overall, our analysis underscores the importance of selecting the appropriate encoder architecture to optimize the performance of ADC systems in terms of power consumption and timing efficiency. The MUX-Based encoder's superior performance positions it as the preferred choice for achieving efficient operation in high-speed, low-power electronic systems.

8. CONCLUSION

8.1 Conclusion of Project Work

In conclusion, the rapid evolution of Very Large-Scale Integration (VLSI) technology underscores the growing imperative for the development of low-power, high-speed Analog-to-Digital Converters (ADCs) within System-on-Chip (SoC) designs. Traditional ADC architectures often grapple with challenges related to power consumption and circuit complexity, necessitating innovative solutions to meet the escalating demands of modern electronic systems.The proposed Flash ADC, leveraging Threshold inverter quantizer (TIQ) comparators, emerges as a promising alternative to conventional designs. By circumventing the need for resistor ladder networks inherent in traditional approaches, TIQ comparators offer a pathway to substantial reductions in power consumption and circuit complexity. This paradigm shift not only addresses the pressing need for power-efficient ADC solutions but also streamlines the design process, facilitating the integration of ADC functionalities into SoC designs with greater ease. Furthermore, the study delves into the optimization of the priority encoder component, evaluating the efficiency of three distinct encoder types: Wallace Tree Encoder, Rom-Based Encoder, and MUX-Based Encoder. Through meticulous analysis of power and timing efficiency metrics, the MUX-Based Encoder emerges as the most viable option for a 3-bit ADC implementation at the transistor level. Its streamlined architecture and efficient operation make it an ideal candidate for enhancing the overall performance of the ADC while minimizing resource utilization. Overall, the findings underscore the pivotal role of innovative design methodologies in advancing ADC technology to meet the evolving demands of modern electronic systems. By prioritizing power efficiency and performance optimization, the proposed Flash ADC architecture with TIQ comparators, complemented by the selection of an efficient MUX-Based Encoder, holds promise for driving advancements in VLSI design and facilitating the realization of energy-efficient, high-performance SoCs for diverse applications. The future scope for developing low power flash ADCs using Threshold Inverter Quantizer (TIQ) comparators in FinFET technology is promising and multifaceted.

8.2 Scope for future work

1. Power Efficiency: The integration of TIQ comparators with FinFET technology offers the potential to significantly reduce power consumption. Research can focus on optimizing the TIQ comparator design to leverage the low leakage and high drive current characteristics of FinFETs, leading to lower power operation.

2. Scaling and Miniaturization: FinFET technology is well-suited for scaling down to smaller nodes. Future work can explore how to maximize the benefits of FinFETs for flash ADCs at advanced process nodes (e.g., 5nm and beyond), improving density and enabling higher resolution within a smaller footprint.

3. Thermal Management: Developing innovative thermal management techniques to address heat dissipation in densely packed FinFET-based ADCs can enhance performance and reliability. This can involve advanced cooling solutions or materials with better thermal properties.

4. Enhanced Linearization Techniques**: Research can be directed towards improving the linearity of TIQ comparators in FinFET-based flash ADCs. This involves refining the comparator design to minimize non-linearities and enhance the accuracy of the ADC.

5. Low-Noise Design: Investigating noise reduction strategies in TIQ comparators implemented in FinFETs can lead to higher fidelity signal conversion. This can include advanced layout techniques and circuit design methodologies that mitigate noise.

6. Adaptive Power Management: Implementing adaptive power management techniques that dynamically adjust power consumption based on the input signal characteristics can further optimize power efficiency. This could involve techniques such as power gating and dynamic voltage scaling.

7. Mixed-Signal Integration: Future work can explore the integration of flash ADCs with other mixed-signal components on the same FinFET-based chip. This could lead to more compact and efficient systems, suitable for applications in IoT, mobile devices, and wearable technology.

8. Algorithmic Enhancements: Incorporating advanced digital correction algorithms that compensate for inherent inaccuracies in the analog components can improve the overall performance of flash ADCs. These algorithms can be optimized to work efficiently with FinFET-based TIQ comparators.

9. Benchmarking and Standardization: Establishing benchmarks and standardized testing methods for FinFET-based flash ADCs using TIQ comparators can help in comparing performance metrics and guiding future development efforts.

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Power efficiency and timing closure for different encoders in 3 bit Flash ADC using TIQ comparator

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***Abstract*— In this paper, a 3bit flash analog to digital converter is designed with TIQ comparators. It requires 2N-1 comparators, an encoder to convert thermometer code to binary code. We have compared the power and timing efficiency of 3 encoders here. The encoders are Wallace Tree, Rom Based and Mux Based. The design is simulated in Tanner tool and TSpice. The power consumed by the respective encoders are: $6.32135x10^{-5}$, $5.8564x10^{-5}$ and $3.7978x10^{-5}$.**

Keywords—Threshold Inverter Quantizer (TIQ), Wallace Tree Encoder, Rom Based Encoder, Mux Based Encoder, Power consumed, timing, Flash ADC

I. INTRODUCTION

An analog-to-digital converter (ADC) is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. Wallace Tree, Rom based encoder and Mux based encoder are three types of priority encoders that can be used along with 2N-1 TIQ converters to convert analog to digital signal. Here we are showcasing the efficiency of the three types of encoders, so that the more efficient want can be used inside a chip for a better power and timing efficiency.An analog to digital converter converts input analog signal to digital signal.

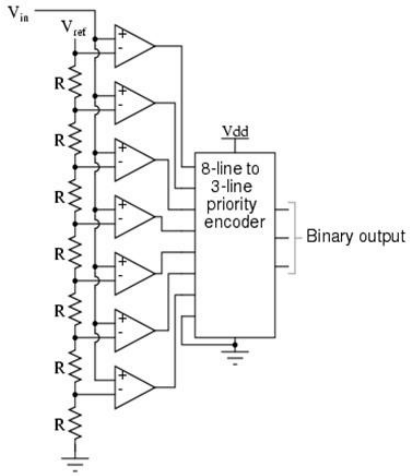

Figure 1: Conventional 3-bit Flash ADC

Flash ADC is(also known as Parallel ADC) uses large number of comparators. Flash ADC are fastest type of ADC due to fast conversion speed from analog to digital signal. An N bit flash ADC consists of 2n-1 comparators and 2n resistors(which generates the reference voltage and is compared with input voltage) where N represents resolution in bits. The input analog signal is applied to all the comparators at once which passes through encoder and we receive digital signal as output. the fast conversion rate have some drawbacks as well. Since it is constructed in a parallel architecture, it takes a lot of space. Flash ADC also leads to high power consumption and complexity for higher resolution bits. The output of thermometer code(comparator) is given to encoder which converts comparator array into binary code(Priority encoding) that can be read by digital equipment.

II. THRESHOLD INVERTER QUANTIZER (TIQ)

TIQ comparator architecture play a crucial role in enhancing signal processing efficiency. Two CMOS inverters are placed in series to each other and worked as buffer output. In a TIQ (Two-Input Quasi-Delay Insensitive) comparator, the cascaded CMOS inverters serve essential functions.

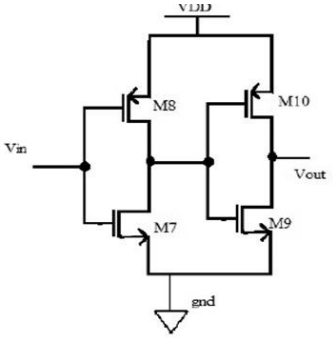

Figure 2: TIQ Comparator

The first inverter helps to amplify the input signals and enhance their strength for further processing. It ensures compatibility with subsequent stages and improves noise immunity. The second inverter aids in signal restoration, mitigating distortion and maintaining signal integrity. This cascaded configuration enhances the comparator's performance by providing signal amplification and regeneration.

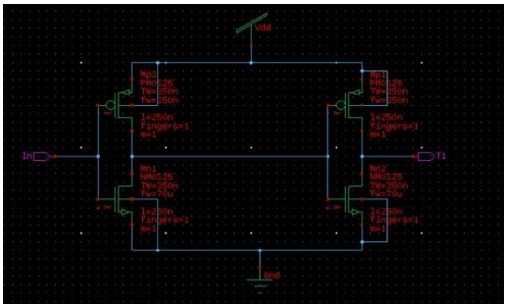

Figure 3: TIQ Comparator Schematic

III. ENCODER

A priority encoder in a Flash ADC selects the highest-order activated comparator output, preventing multiple outputs from conflicting. This ensures accurate conversion of analog voltages to digital codes by encoding only the most significant comparator output, crucial for precise measurement and processing of input signals. Here we are using three types of encoder : Wallace Tree, Rom Based and Mux Based Encoder to detect the best power and timing efficiency for the whole flash ADC in transistor level.

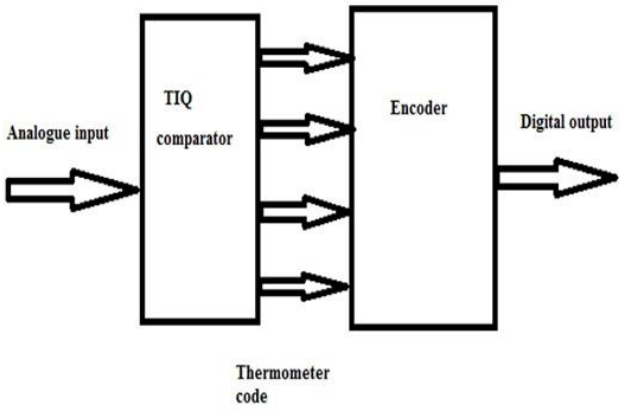

Figure 4: ADC in Transistor level

A. *Wallace Tree Encoder*

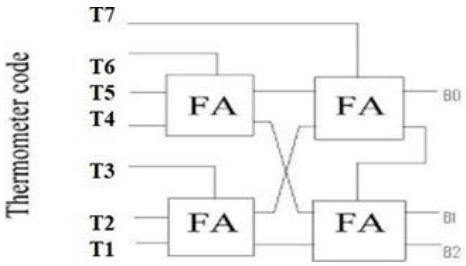

Figure 5: Wallace Tree encoder

In place of priority encoder, Wallace Tree encoder is being used to compress the binary output. Four Full Adder is being used and the Full adders are made by Nand gates because in fabrication industry Nand gates are mainly used. Nand gates take much lesser area and are much faster than other gates. Wallace Tree is consuming 6.32135x10^-5W power within a time period of 1.86 seconds in overall process. We are using seven TIQs as input so that the signal received by the encoder will be noise free and amplified version. The Wallace Tree encoder then produces three bit output denoted as B1, B2, B3. All these three outputs graphs are shown in the result section. But the whole thing is a little bit slower and the full adders always produce result in simultaneous way as we put them in series manner.

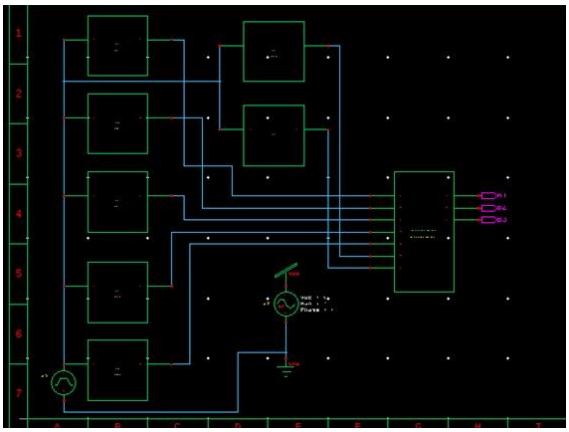

Figure 6: Two input NAND Gate schematic

The utilization of a Wallace Tree encoder in a Flash ADC system offers advantages in signal compression and processing. However, careful consideration of trade-offs between speed, power consumption, and accuracy is essential for optimizing overall system performance and meeting design requirements.

B. *ROM based Encoder*

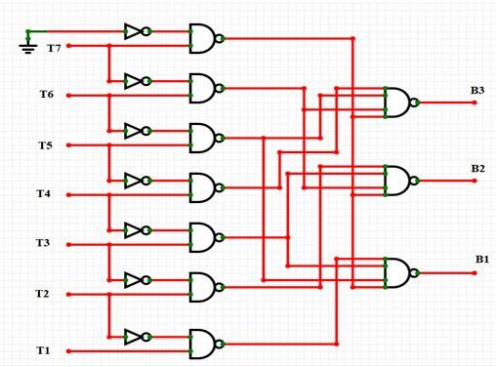

Figure 7: ROM based Encoder

Rom based encoder works on Read-only Memory concept where it coverts encoded input data into a specific output data. The ROM stores predefined output values corresponding to different input combinations. For 3 bit system the Rom Based is made by using seven 2 input Nand gates and three 4 input Nand gates and seven inverters. The TIQ inputs are given to the seven inverters respectively and the 3 bit outputs are taken from the four input Nand gates. The outputs are denoted by B1, B2, and B3. Rom Based encoder is mainly designed using NAND gates only. So it will consume much lesser space along with compact timings. But in this structure there are too many gates are involved which may lead to significant gate delays and hence consuming more power also due to some CMOS owing defects like leakage power loss and dynamic power loss. Again owing to handsome number of gates, this will cause a problematic number of connection which may leads to routing and placing problem. Power loss may also occur which is known as net delay owing to large number of connections. So Rom Based is not the optimised way to convert analog to digital. The ROM Based system is consuming 5.8564x10^-5W power within a time period of 1.64 seconds in overall process.

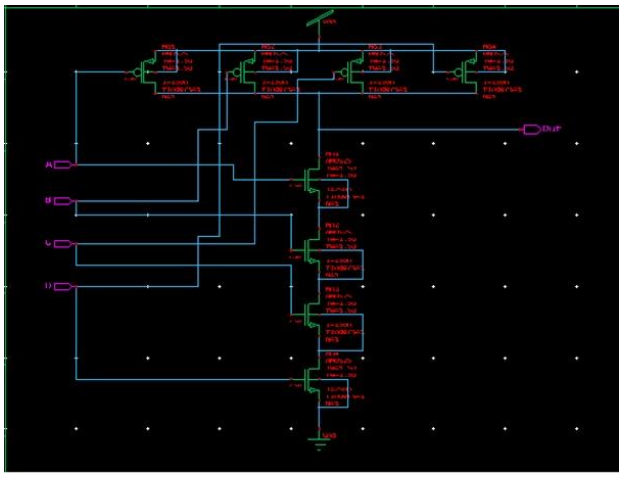

Figure 8: Four input NAND gate schematic

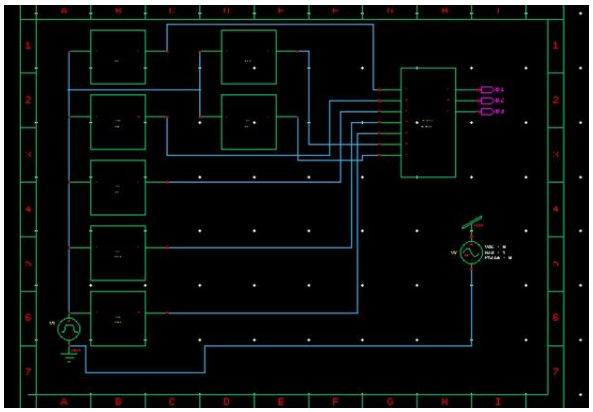

Figure 9: ROM based ADC schematic

C. MUX based Encoder

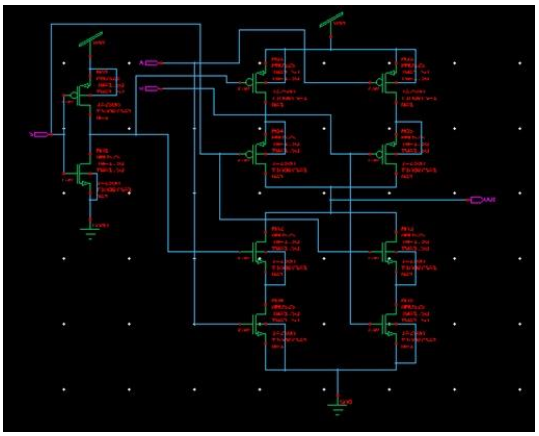

Figure 10: 2:1 MUX schematic

There are various ways to design a priority encoder. First we are using Wallace Tree Encoder. For 3 bit system the Wallace tree is using four full adders in series manner. But it takes much larger area with a handsome delay as the result of the full adder always occur simultaneously. To overcome the problem we used Rom Based Encoder. But it takes a large number of nand gates along with three 4 input nands. Again the wire length in the Rom based is much larger which results in the net delay situation. To get rid of all those problems, a MUX based encoder is used. Here we have taken four 2:1 Mux. Each mux has used five cmos structure. For this the number of Nand gates are reduced as well as it requires much lesser number of connections so net delay also drastically falls. So overall it will be easy to fabricate on the chip. For this Mux Based Encoder is the best choice for low power circuits.

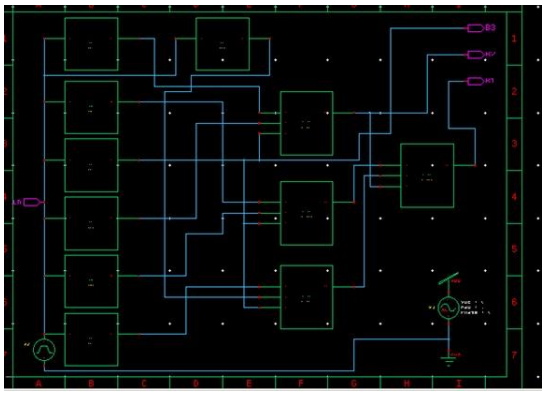

Figure 11: 2:1 MUX based 3 bit ADC

IV. RESULT

We are calculating the power consumed and timing closure of the 3 bit flash ADC by connecting the three types of Encoders (Wallace Tree, Rom Based and Mux Based) simultaneously. We have received the graphs of output values for the 3 types of ADC along with their power consumed and timing in the whole part. In this process we have used Tanner Lab and T-spice tools which are made by Siemens. Our main aim is to find the most efficient encoder which can be used for a low power fast system.

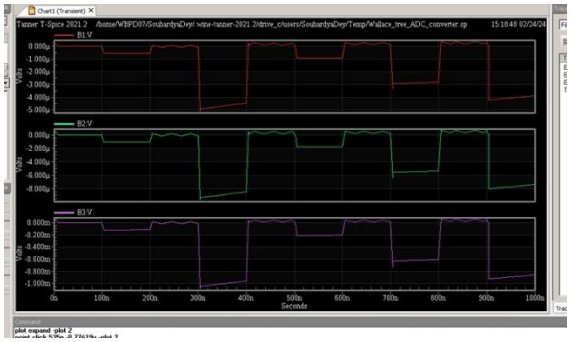

Figure 12: Output of ADC using Wallace Tree Encoder

```
Power Results

VV1 from time 0 to 1e-06
Average power consumed -> -6.321353e-05 watts
Max power 8.865965e-03 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 13: Power consumed using Wallace Tree Encoder

Parsing	0.43 seconds
Setup	0.19 seconds
DC operating point	0.06 seconds
Transient Analysis	0.81 seconds
Output	0.02 seconds
Overhead	0.35 seconds
Total	1.86 seconds

Figure 14: Time taken using Wallace Tree Encoder

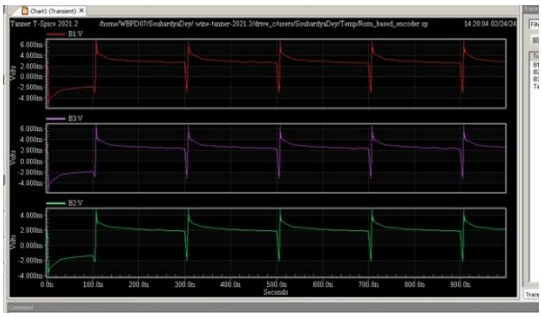

Figure 15: Output of ADC using ROM based Encoder

```
Power Results

VV1 from time 0 to 1e-06
Average power consumed -> 5.856485e-05 watts
Max power 1.344202e-02 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 16: Power consumed using ROM based Encoder

```
Parsing                          0.46 seconds
Setup                            0.13 seconds
DC operating point               0.02 seconds
Transient Analysis               0.62 seconds
Overhead                         0.40 seconds
-----------------------------------------
Total                            1.64 seconds
```

Figure 17: Time taken using ROM based Encoder

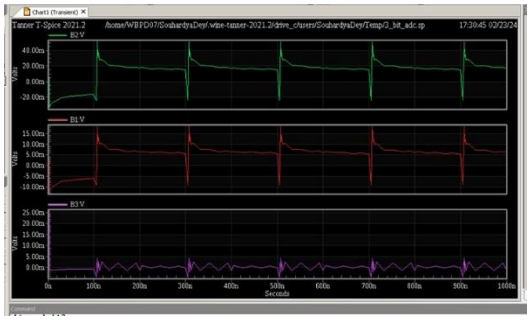

Figure 18: Output of ADC using MUX based Encoder

```
Power Results

VV2 from time 0 to 1e-06
Average power consumed -> 3.797851e-05 watts
Max power 1.346125e-02 at time 5e-09
Min power 0.000000e+00 at time 0
```

Figure 19: Power consumed using MUX based Encoder

```
Parsing                          0.45 seconds
Setup                            0.26 seconds
DC operating point               0.01 seconds
Transient Analysis               0.15 seconds
Overhead                         0.42 seconds
-----------------------------------------
Total                            1.29 seconds
```

Figure 20: Time taken using MUX based Encoder

In this process we have figured out that the power consumed by the Wallace Tree encoder ADC system is 6.32135x10^-5W and time taken is 1.86 s. The Rom Based encoder ADC system consumed 5.8564x10^-5 W power and it takes 1.64 s time. While the Mux Based Encoder ADC system consumed 3.797851x10^-5 W power and it takes 1.29s time. So overall the Mux Based 3 bit Flash ADC system is much more compatible to be use in the transistor level.

V. Conclusion

In conclusion, as VLSI technology advances, the demand for low-power, high-speed ADCs becomes increasingly crucial in SoC designs. While conventional ADCs pose challenges with power consumption and complexity, the proposed Flash ADC employing TIQ comparators offers a promising solution. By eliminating the need for resistor ladder networks, TIQ comparators significantly reduce power consumption and circuit complexity. For the priority encoder part we have used mainly three types Wallace Tree Encoder, Rom Based Encoder, Mux Based Encoder and compare their power and timing efficiency. Among them Mux Based Encoder for 3 bit ADC become the most efficient one to be used in the ADC in transistor level.

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