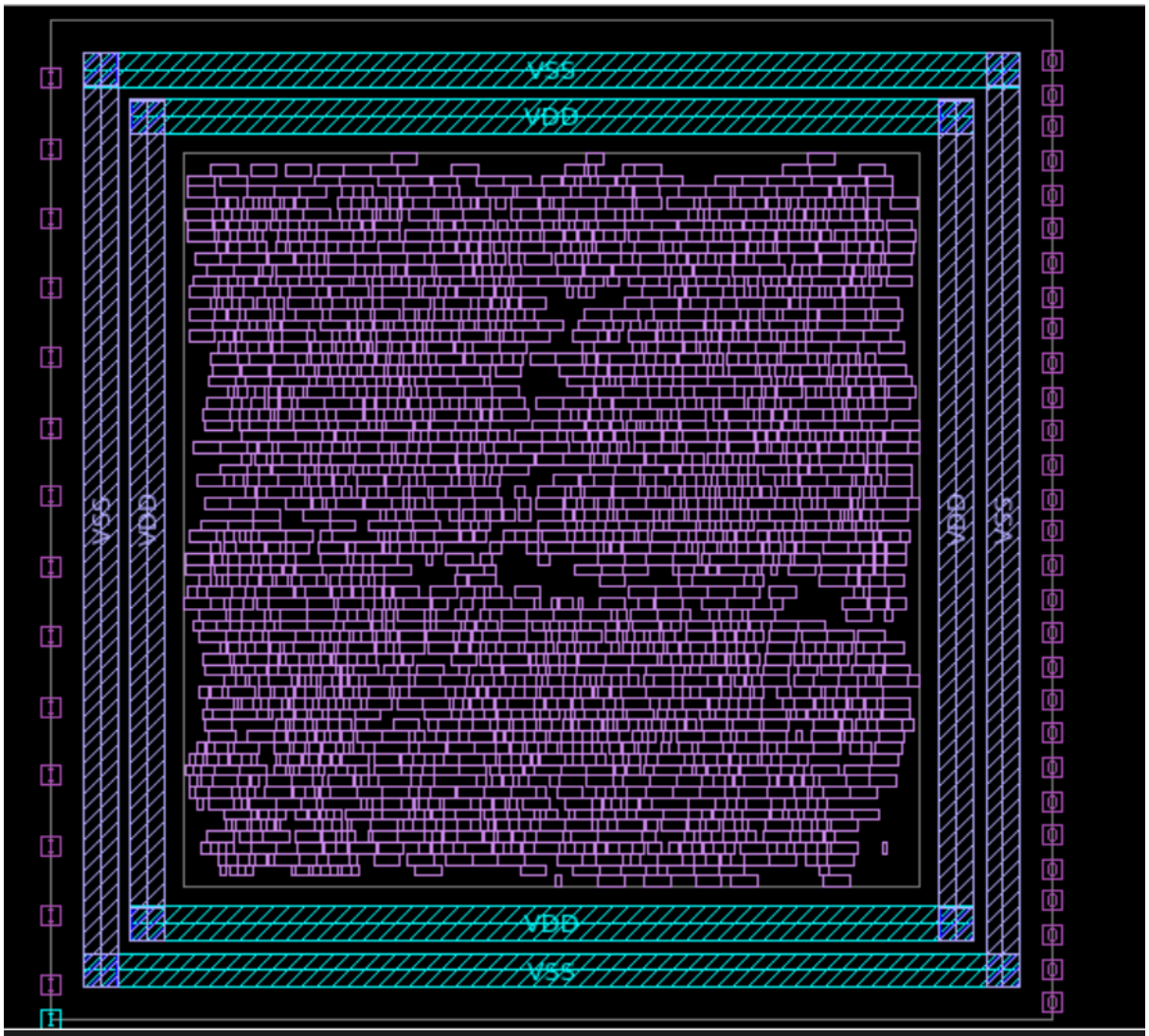



```
icc2_shell> report_qor -summary
****************************************
Report : qor
        -summary
Design : router_top
Version: T-2022.03-SP4
Date   : Fri May 17 21:09:35 2024
****************************************
Information: Timer using 'CRPR'. (TIM-050)

Timing
--------------------------------------------------------------------------------
Context                                 WNS             TNS             NVE
--------------------------------------------------------------------------------
Design             (Setup)            -0.00           -0.00               1

Design             (Hold)              1.44            0.00               0
--------------------------------------------------------------------------------

Miscellaneous
--------------------------------------------------------------------------------
Cell Area (netlist):                              7624.07
Cell Area (netlist and physical only):            7624.07
Nets with DRC Violations:        2
1
```

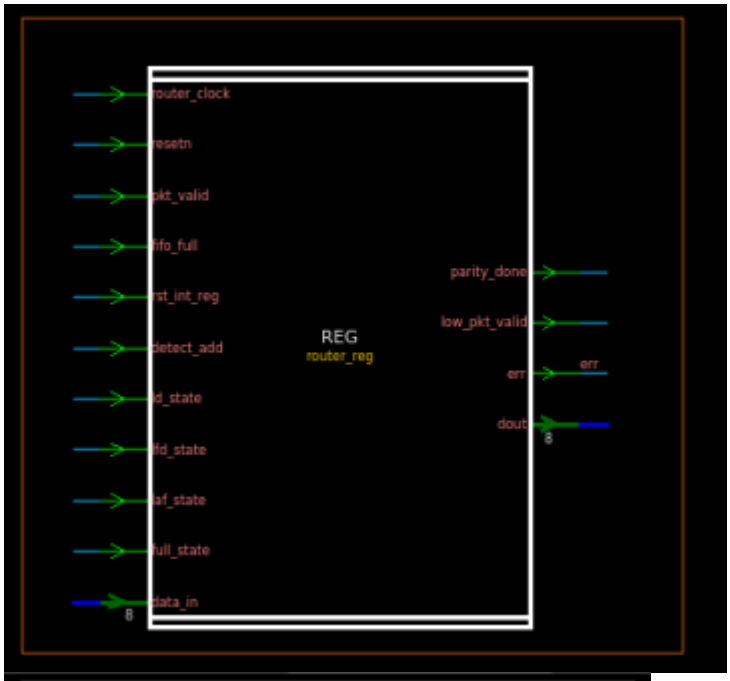
Power Group	Internal Power	Switching Power	Leakage Power	Total Power	(%)	Attrs
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
clock_network	1.59e+08	2.94e+07	1.28e+06	1.89e+08	(74.4%)	i
register	4.74e+06	4.24e+05	1.31e+07	1.83e+07	(7.2%)	
sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00	(0.0%)	
combinational	3.22e+06	4.57e+06	3.90e+07	4.68e+07	(18.4%)	
Total	1.67e+08 pW	3.44e+07 pW	5.34e+07 pW	2.54e+08 pW		

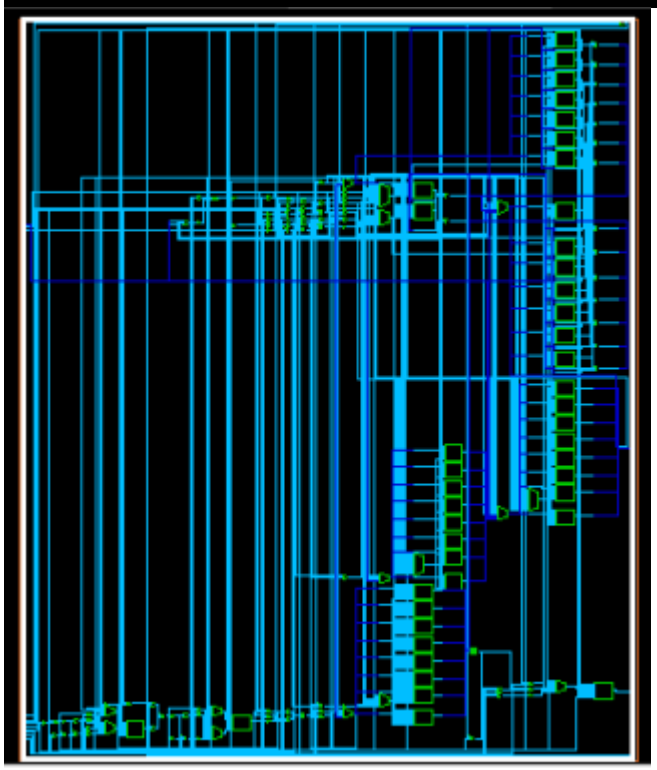
1

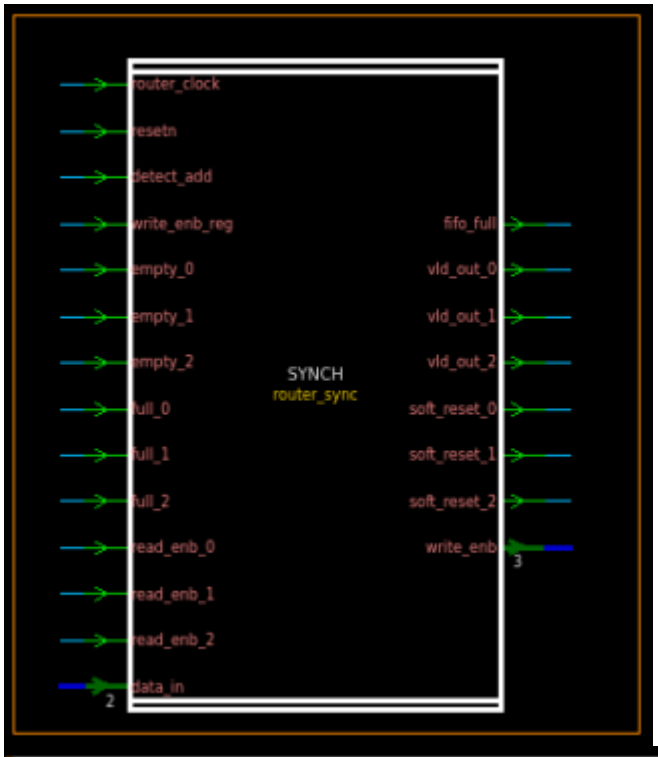
```
icc2_shell> report_mode
****************************************
Report : mode
Design : router_top
Version: T-2022.03-SP4
Date   : Fri May 17 21:11:57 2024
****************************************

--------------------------------------------------------------------------------
Mode default
--------------------------------------------------------------------------------

Current: true  Default: true  Empty: false

Scenarios associated with this mode:
```

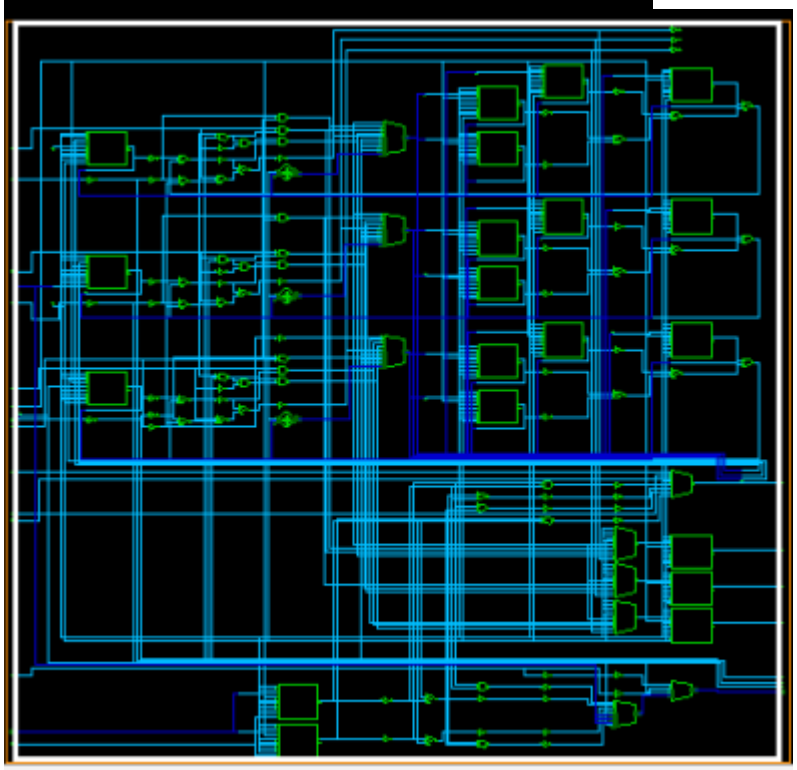
Scenario	Corner	Active	Setup	Hold	Leakage Power	Dynamic Power	Max_tran	Max_cap	Min_cap	Cell_em	Signal_em
default	default	true	true	true	true	true	true	true	true	false	false

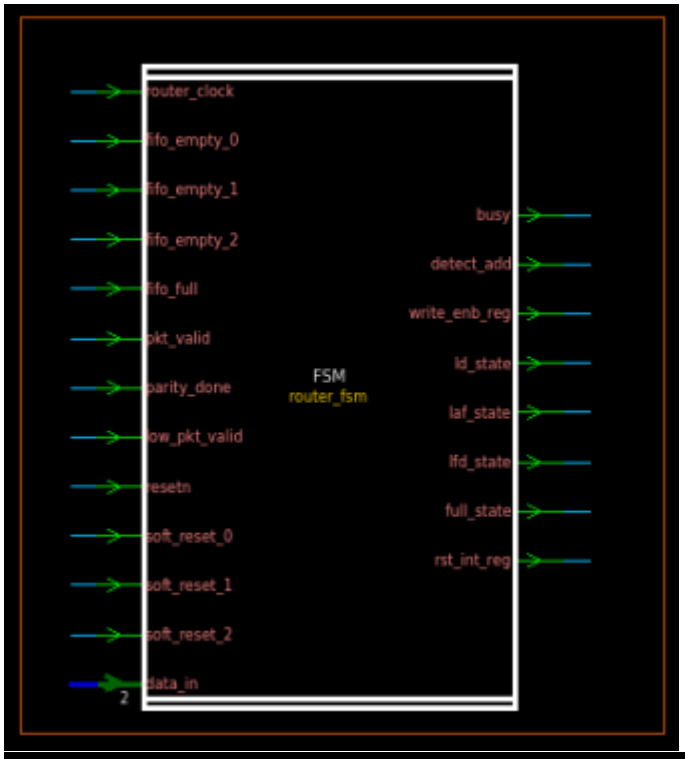
```
Point                                                   Incr       Path
------------------------------------------------------------------------
clock clk (rise edge)                                   0.00       0.00
clock network delay (propagated)                        0.13       0.13

FIFO_1/read_ptr_reg[0]/CLK (DFFX1_HVT)                  0.00       0.13 r
FIFO_1/read_ptr_reg[0]/Q (DFFX1_HVT)                    2.39       2.52 f
FIFO_1/U53/Y (AND3X1_HVT)                               1.20       3.72 f
FIFO_1/ZBUF_605_inst_485/Y (NBUFFX2_HVT)                0.87       4.59 f
FIFO_1/U106/Y (AOI22X1_RVT)                             0.42       5.01 r
FIFO_1/U107/Y (NAND4X1_HVT)                             2.39       7.40 f
FIFO_1/U114/Y (OA22X1_RVT)                              0.47       7.86 f
FIFO_1/U115/Y (AO22X1_RVT)                              0.22       8.08 f
FIFO_1/U158/CO (FADDX1_RVT)                             0.22       8.31 f
FIFO_1/U156/CO (FADDX1_RVT)                             0.18       8.49 f
FIFO_1/U166/CO (FADDX1_RVT)                             0.17       8.66 f
FIFO_1/U154/Y (XOR2X1_RVT)                              0.21       8.88 r
FIFO_1/U155/Y (AO22X1_RVT)                              0.13       9.01 r
FIFO_1/count_reg[6]/D (DFFX1_HVT)                       0.00       9.01 r
data arrival time                                                  9.01

clock clk (rise edge)                                  10.00      10.00
clock network delay (propagated)                        0.13      10.13
clock reconvergence pessimism                           0.01      10.13
FIFO_1/count_reg[6]/CLK (DFFX1_HVT)                     0.00      10.13 r
library setup time                                     -1.12       9.01
data required time                                                 9.01
------------------------------------------------------------------------
data required time                                                 9.01
data arrival time                                                 -9.01
------------------------------------------------------------------------
slack (VIOLATED)                                                  -0.00

icc2_shell> report_clock
****************************************
Report : clock
Design : router_top
Mode   : default
Version: T-2022.03-SP4
Date   : Fri May 17 21:12:56 2024
****************************************


Attributes:
    p - Propagated clock
    G - Generated  clock
    U - Unexpanded generated clock

Clock          Period   Waveform            Attrs     Sources
------------------------------------------------------------------------
clk             10.00   {0 5}               p         {router_clock}
```

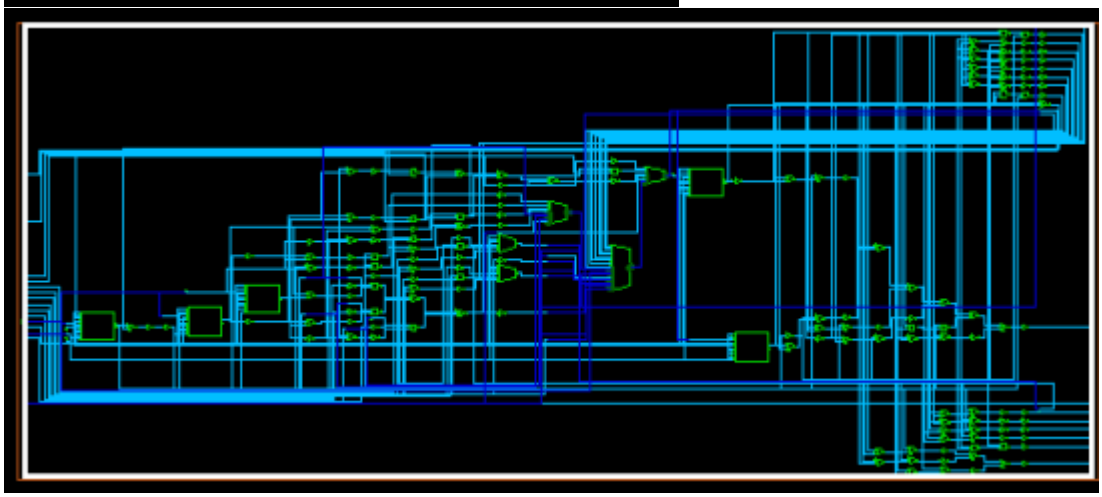

router_clock
resetn
pkt_valid
fifo_full
rst_int_reg
detect_add
ld_state
lfd_state
laf_state
full_state
data_in
8
REG
router_reg
parity_done
low_pkt_valid
err
err
dout
8

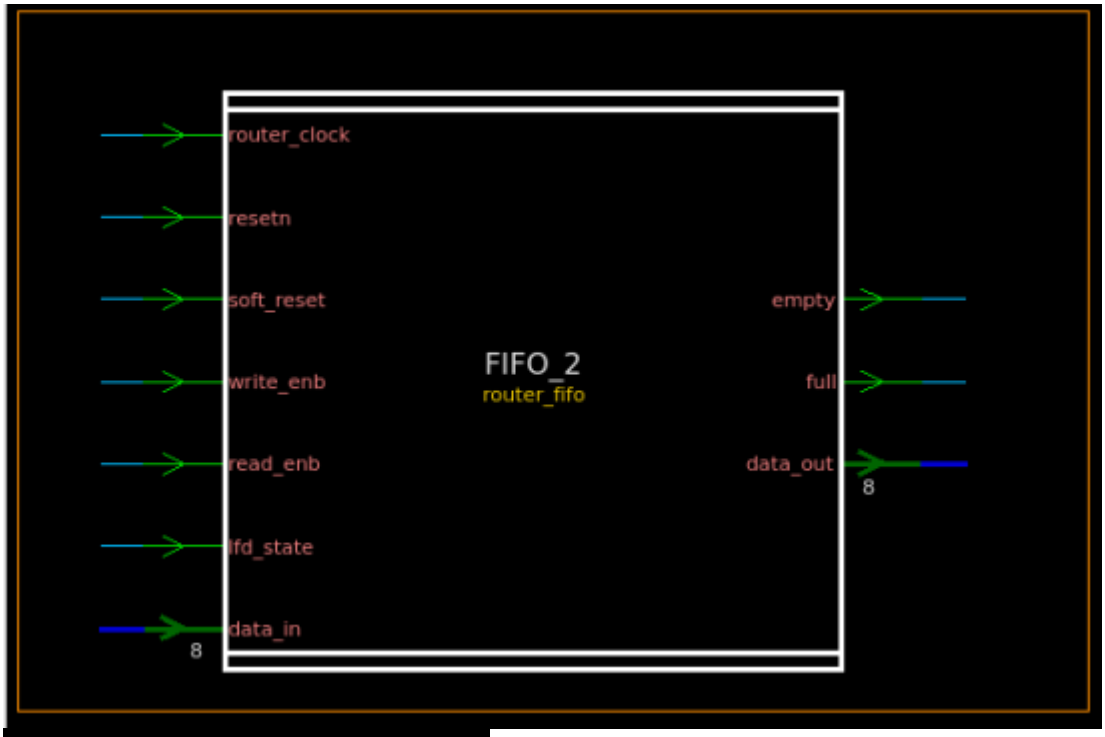


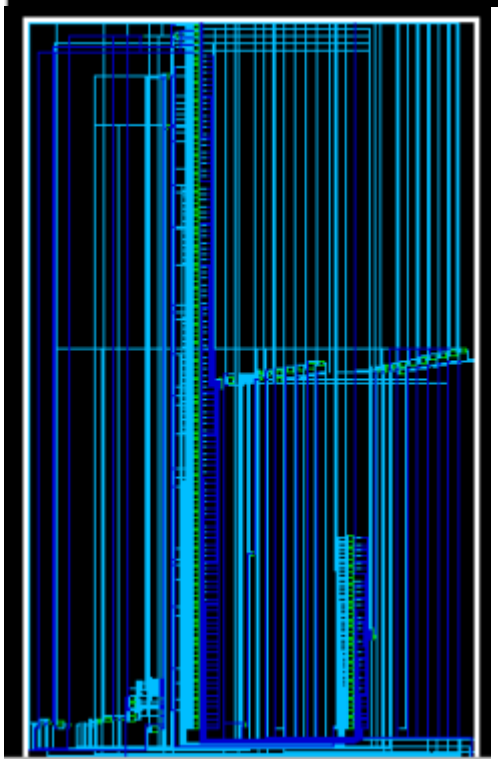

router_clock
resetn
detect_add
write_enb_reg
empty_0
empty_1
empty_2
full_0
full_1
full_2
read_enb_0
read_enb_1
read_enb_2
data_in
2
SYNCH
router_sync
fifo_full
vld_out_0
vld_out_1
vld_out_2
soft_reset_0
soft_reset_1
soft_reset_2
write_enb
3

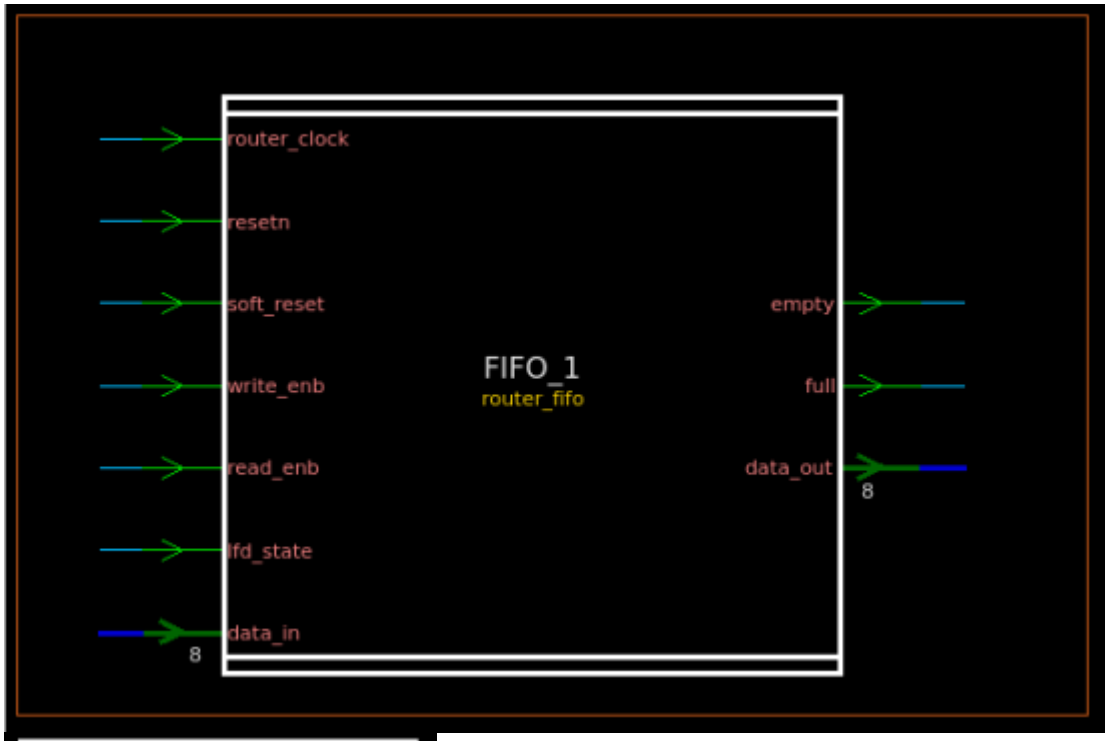


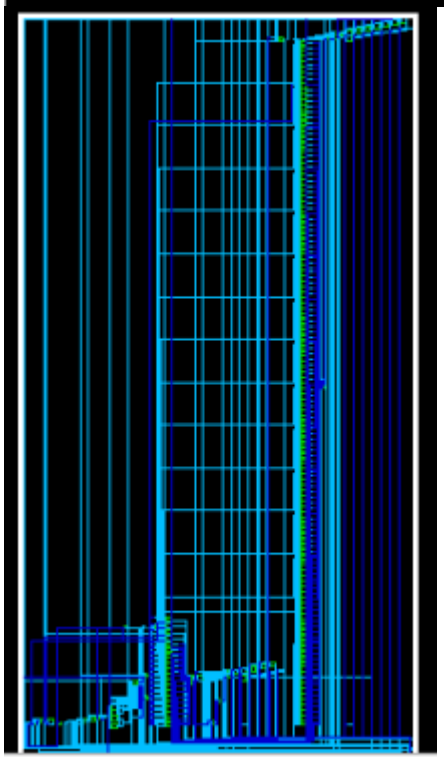

router_clock
fifo_empty_0
fifo_empty_1
fifo_empty_2
fifo_full
pkt_valid
parity_done
low_pkt_valid
resetn
soft_reset_0
soft_reset_1
soft_reset_2
data_in
2
FSM
router_fsm
busy
detect_add
write_enb_reg
ld_state
laf_state
lfd_state
full_state
rst_int_reg

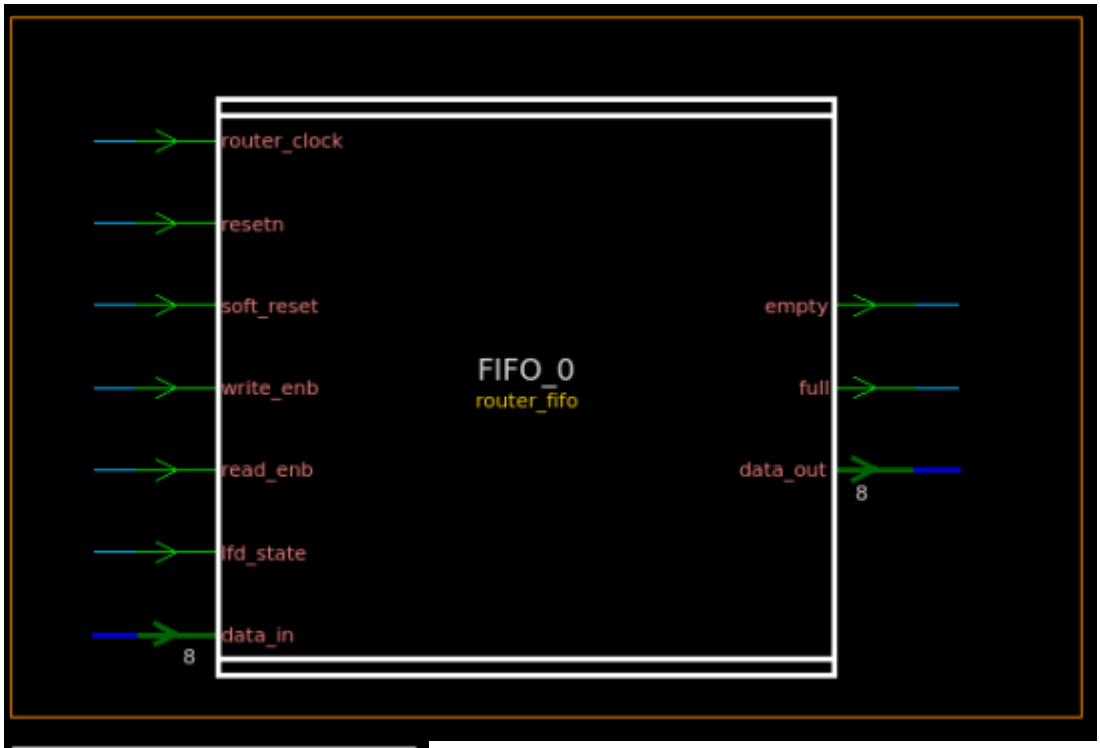



router_clock
resetn
soft_reset
write_enb
read_enb
lfd_state
data_in
8
FIFO_2
router_fifo
empty
full
data_out
8




router_clock
resetn
soft_reset
write_enb
read_enb
lfd_state
data_in
8
FIFO_1
router_fifo
empty
full
data_out
8




router_clock
resetn
soft_reset
write_enb
read_enb
lfd_state
data_in
8
FIFO_0
router_fifo
empty
full
data_out
8