Electronics Club

Task-1

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Interleaving block:

Design.v:

```
module fourByteInterleaver(
  input  [31:0] inFourBytes,
  output  [31:0] outFourBytes
);
  wire [7:0] byte0;
  wire [7:0] byte1;
  wire [7:0] byte2;
  wire [7:0] byte3;
  wire [7:0] out0;
  wire [7:0] out1;
  wire [7:0] out2;
  wire [7:0] out3;

  assign byte0 = inFourBytes[7:0];
  assign byte1 = inFourBytes[15:8];
  assign byte2 = inFourBytes[23:16];
  assign byte3 = inFourBytes[31:24];
  assign out3 = {byte0[1:0],byte1[1:0],byte2[1:0],byte3[1:0]};
  assign out2 = {byte0[3:2],byte1[3:2],byte2[3:2],byte3[3:2]};
  assign out1 = {byte0[5:4],byte1[5:4],byte2[5:4],byte3[5:4]};
  assign out0 = {byte0[7:6],byte1[7:6],byte2[7:6],byte3[7:6]};
  assign outFourBytes = {out3,out2,out1,out0};

endmodule


module interleavingModule(
  input [95:0] data,
  output [95:0] int_data
);
       fourByteInterleaver T1(data[31:0],int_data[31:0]);
       fourByteInterleaver T2(data[63:32],int_data[63:32]);
       fourByteInterleaver T3(data[95:64],int_data[95:64]);
endmodule
```

Testbench.v:

```
module t_interleaver;

  reg [95:0] data;
  wire [95:0] int_data;

  interleavingModule M1(.data(data),.int_data(int_data));

  initial begin

data=96'b010001010110110001100101011000110111010001110010011011110011111001000100;

  end


initial begin
  $monitor("%b",int_data);
end
endmodule
```

Output:

```
010000000100000000000000010000000011010001000111111010100101010100101110011111100001110110100010
Done
```