# Task 2 Electronics Club

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## Design.v

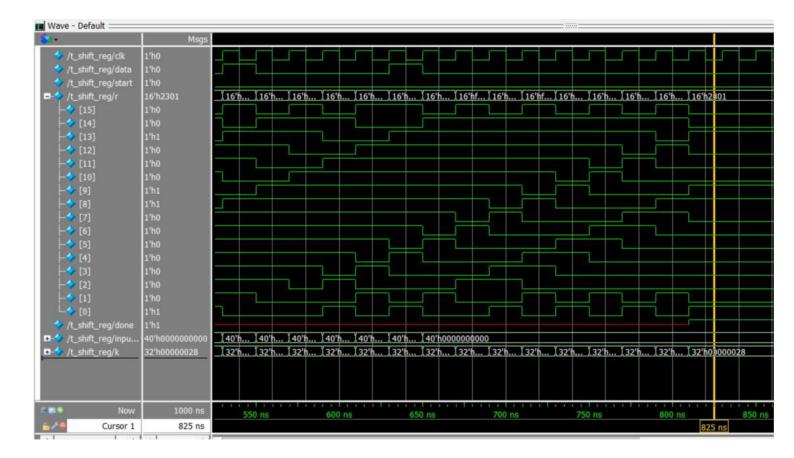
```
module shift_reg(
input clk,
input data, start,
output reg [15:0] r,
output reg done
);
  wire temp=data;
  reg [5:0] count=0;
  always @(posedge clk, posedge start) begin
    if(start) begin
      r=16'hFFFF;
      count=40;
    end
    else if(count!=0) begin
      r[15] <= r[14]+r[15]+temp;
      r[14:3] \leftarrow r[13:2];
      r[2] <= r[1] + temp + r[15];
      r[1] <= r[0];
      r[0] <= temp + r[15];
      count<=count-1;</pre>
     // $display("%d",count); //Debugging
      if(count==1) begin
         done<=1;</pre>
      end
    end
  end
endmodule
```

### Testbench.v

```
module t shift reg;
  reg clk;
  reg data;
  reg start;
 wire [15:0] r;
 wire done;
  reg [39:0] input data = 40'h01 90 10 21 00; //Roll no- 190102100
  integer k;
  initial forever #10 clk = !clk ;
  shift_reg M1 (.clk(clk),.data(data),.start(start),.r(r),.done(done));
  initial begin
    clk=0;
    start=0;
    data=0;
    #10;
    start=1;
    #10 start=0;
    for(k=0;k<40;k=k+1)
      begin
        data=input data[39];
        @(posedge clk) input_data = input_data<<1;</pre>
      #10 $display("%h %h ",r[15:8],r[7:0]);
  end
  initial @(posedge done) begin
    $display("%b",done);
  end
 // Debugging
 /* initial begin
    $monitor("%h %d %b",r[15:0],k,);
*/
initial #1000 $finish;
endmodule
```

r[15:0] : 23\_01

#### Waveforms



```
# Loading work.shift_reg
add wave -position insertpoint sim:/t_shift_reg/*
VSIM 51> run -all
# 1
# 23 01
# ** Note: $stop : C:/Modeltech_pe_edu_10.4a/examples/t_Club_Assign_T2.v(52)
# Time: 1 us Iteration: 0 Instance: /t shift reg
```