Task 2

Electronics Club

Chirag Hegde

190102100

Design.v

```
module shift_reg(
input clk,
input data, start,
output reg [15:0] r,
output reg done
);
  wire temp=data;
  reg [5:0] count=0;

  always @(posedge clk, posedge start) begin
    if(start) begin
      r=16'hFFFF;
      count=40;
    end

    else if(count!=0) begin
      r[15] <= r[14]+r[15]+temp;
      r[14:3] <= r[13:2];
      r[2] <= r[1]+temp+r[15];
      r[1] <= r[0];
      r[0] <= temp+r[15];
      count<=count-1;
     // $display("%d",count); //Debugging
      if(count==1) begin
         done<=1;
      end
    end
  end
endmodule
```

Testbench.v

```
module t_shift_reg;
  reg clk;
  reg data;
  reg start;
  wire [15:0] r;
  wire done;
  reg [39:0] input_data = 40'h01_90_10_21_00; //Roll no- 190102100

  integer k;
  initial  forever #10 clk = !clk ;

  shift_reg M1 (.clk(clk),.data(data),.start(start),.r(r),.done(done));

  initial begin
    clk=0;
    start=0;
    data=0;

    #10;
    start=1;
    #10 start=0;

    for(k=0;k<40;k=k+1)
      begin
        data=input_data[39];
        @(posedge clk) input_data = input_data<<1;
      end
      #10 $display("%h %h ",r[15:8],r[7:0]);
  end

  initial @(posedge done) begin
    $display("%b",done);
  end
  // Debugging
 /* initial begin
    $monitor("%h %d %b",r[15:0],k,);
    end
 */
 initial #1000 $finish ;
endmodule
```

r[15:0] : 23_01

Waveforms